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Research Article

Interface Study on Amorphous Indium Gallium Zinc Oxide Thin Film Transistors Using High-k Gate Dielectric Materials

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We investigated amorphous indium gallium zinc oxide (a-IGZO) thin film transistors (TFTs) using different high-k gate dielectric materials such as silicon nitride (Si_3N_4) and aluminum oxide (Al_2O_3) at low temperature process (<300°C) and compared them with low temperature silicon dioxide (SiO_2). The IGZO device with high-k gate dielectric material will expect to get high gate capacitance density to induce large amount of channel carrier and generate the higher drive current. In addition, for the integrating process of integrating IGZO device, postannealing treatment is an essential process for completing the process. The chemical reaction of the high-k/IGZO interface due to heat formation in high-k/IGZO materials results in reliability issue. We also used the voltage stress for testing the reliability for the device with different high-k gate dielectric materials and explained the interface effect by charge band diagram.

1. Introduction

The emergence of transparent thin film transistors (TTFTs) has enabled satisfying consumer requirements for electronic products. Because of their numerous advantages, TTFTs are anticipated to become the next generation of transistor materials. Among the various types of transparent thin film materials currently in use, indium gallium zinc oxide (IGZO) is extremely promising [1–6]. IGZO is highly flexible and has a carrier mobility of up to 10 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [7]. These properties have had a considerable impact on advancing the applications of TTFTs.

The energy gap of IGZO approximates 3.1 eV [8]. The transmittance rate of IGZO can reach up to 90%, exceeding 80% under certain annealing conditions [9]. The main structure of IGZO is ZnO doped with In^{3+} and Ga^{3+}; trivalent indium and gallium can be used as replacements for divalent zinc to provide additional cations for enhancing carrier mobility. According to previous studies, doping IGZO with indium enhances its carrier mobility, whereas including gallium reduces its carrier mobility. Including indium provides extra cations; In–O has a weak bond that can be broken easily to produce oxygen vacancies. Although including gallium reduces carrier mobility, it does not have a marked effect on distorting the original lattice because the bond length of Ga–O approximates to that of Zn–O and Zn^{2+} and Ga^{3+} have a nearly identical radius. The bonding of Ga–O is far stronger than those of In–O and Zn–O; thus, oxygen vacancies can be inhibited by utilizing the Ga–O bond. Because of these properties, fabricating IGZO thin films does not introduce excessive defects and cause deterioration in their electrical property. The doping ratio of indium, gallium, and zinc can influence the crystal structure and carrier mobility. Currently, IGZO doped with indium : gallium : zinc : oxygen at a ratio of 1 : 1 : 1 : 4 has been used in many studies [10–13].

Nowadays, many semiconductor manufacture companies are currently using the high-k dielectric materials as replacement materials for SiO_2 as the gate dielectric materials for complementary metal-oxide-semiconductor (CMOS) process [14–16]. The required properties of gate dielectrics need considering the key guidelines such as high dielectric constant, proper conduction and valence-band offset, thermodynamic stability, interface quality, process compatibility, and device reliability. With high-k gate dielectric materials, the high drive currents with large capacitance, low leakage current, and low operation voltage could be achieved for CMOS devices.

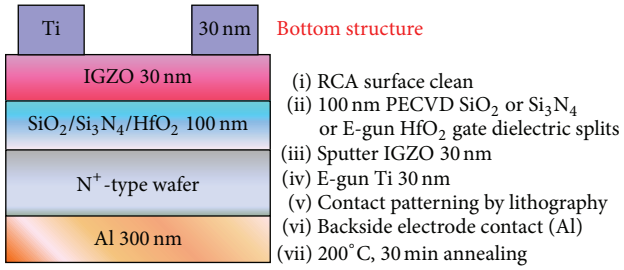

Figure 1: Cross section of the fabricated bottom-gate a-IGZO TFTs using high-k materials.

In this paper, we integrate the a-IGZO thin film transistors by using different high-k gate dielectric materials and research the interface between the high-k dielectric thin film/IGZO interfaces through the thermal annealing. We use the low temperature PECVD SiO_2, PECVD Si_3N_4, and room temperature E-gun Al_2O_3 thin film for the gate dielectric material. The effect of temperature treatment on a-IGZO TFTs was studied due to the interface reaction. The thermal budget is crucial and will influence the device characteristics such as subthreshold swing (SS), I_{ON}/I_{OFF} ratio, carrier mobility, and stress characteristics. Moreover, the stress effect of the IGZO device was explained by using energy band diagram for the electrical characteristics of a-IGZO TFTs.

2. Fabrication

The a-IGZO TFTs with different high-k dielectric were fabricated by using N^+-type wafers and a bottom gate structure, as shown in Figure 1. By using the bottom structure, we could focus on the interface between the high-k dielectric thin film/IGZO interfaces through thermal annealing [17, 18]. First, after the RCA clean, three different gate dielectric materials were deposited with thickness of 10 nm. The splits were SiO_2 by using PECVD method at 300°C, Si_3N_4 by using PECVD method at 300°C, and Al_2O_3 by using E-gun method at room temperature, respectively. For comparison with above layers, we also use furnace SiO_2 at 950°C as optimized gate oxide to eliminate the interface effect. Then, a 30 nm a-IGZO layer was deposited using sputtering method with $IGZO_4$ targets (In : Ga : Zn : O ratio of 1 : 1 : 1 : 4) in ambient oxygen gas (O_2). The cosputtering process was performed at 4×10^{-3} Torr in room temperature with precursors of O_2 (6 sccm) and Ar (24 sccm), and the DC sputter power was set at 150 W. After active region patterning, 30 nm titanium (Ti) thin film was deposited and used for source and drain electrodes, using the E-gun method at room temperature. After source/drain patterning, postannealing treatment was performed for 30 minutes at temperature of 200°C. The dimensions of the devices were length/width dimensions of 200/1000 μm.

3. Results and Discussion

The basic I_d-V_g curve of the a-IGZO TFTs using high-k materials is shown in Figure 2(a). For the measurement, the gate voltage varied from −5 to 5 V and the drain voltage was 1 V. Figure 2(b) shows the I_d-V_d curve of the a-IGZO TFTs, and the drain voltage varied from 0 to 10 V and the gate voltages were 0, 2.5, and 5 V. We could observe that the Si_3N_4 sample has higher I_{ON}, lower I_{OFF}, higher I_{ON}/I_{OFF} ratio, and high mobility due to the higher dielectric constant compared to SiO_2 sample and Al_2O_3 sample. However, the SiO_2 sample has good SS compared to others because of good interface with IGZO. The a-IGZO TFTs with Si_3N_4 gate dielectric exhibited superior characteristics. The summary table of the measurement data is shown in Table 1.

Table 1: The summary table for the a-IGZO TFTs using high-k materials.

	V_t (V)	S.S (V/dec.)	μ (cm^2/V-s)	I_{ON}/I_{OFF}
PECVD SiO_2	0.09	0.100	3.50	2.1×10^{-5}
PECVD Si_3N_4	0.20	0.151	8.96	8.5×10^{-6}
E-gun Al_2O_3	−0.03	0.270	8.07	8.4×10^{-6}

As shown in Figures 3(a)–3(d), following a gate voltage stress of −5 V, V_t of PECVD SiO_2 and E-gun Al_2O_3 sample increased as the stress time lengthened, and V_t slightly shifted to the right; by contrast, for the PECVD Si_3N_4 sample, V_t shifted to the left. Following a gate voltage stress of +5 V, PECVD SiO_2 and E-gun Al_2O_3 sample have deterioration just like device on, and the E-gun Al_2O_3 sample deteriorated more apparently than did the PECVD SiO_2 sample. By contrast, for the PECVD Si_3N_4 sample, V_t shifted to the right as the stress time increased and did not deteriorate. To determine the problem causing the observed phenomena, SiO_2 gate-insulating layer with the same thickness was developed using a horizontal furnace tube through the dry oxide method at 950°C, as shown in Figure 3(d). The dry oxide formed using horizontal furnace was used as the control sample. The results showed that, following numerous sweeps of negative gate voltage stress, the components exhibited minimal change in characteristics. Following the positive voltage stress tests, V_t neither shifted to the left nor deteriorated. These results accord with the trend observed for Si_3N_4 sample and the characteristics of positive gate voltage stress [19–21]. This phenomenon is attributed to the interface effect between the gate-insulating layer and the IGZO. Thus, the problem was related to changes in the interface after stressing. Moreover, we could also calculate the interface trap density (D_{it}) by the difference of the subthreshold swing (SS) between the original sample and stressed sample. The interface trap density (D_{it}) was calculated based on the equation $SS = kT/q \times \ln 10 \times (1 + (C_b + C_{it})/C_{HK})$, where C_b is the depletion capacitance density of IGZO and C_{it} ($= qD_{it}$) is the capacitance density from charged interface traps [22, 23]. By neglecting C_b, D_{it} for the original PECVD SiO_2 sample, PECVD Si_3N_4 sample, and E-gun Al_2O_3 sample are 2.9×10^{12}, 6.6×10^{12}, and 5.3×10^{12} cm^{-2} eV^{-1}, respectively. After voltage positive gate voltage stress for 10 seconds, D_{it} for the stressed PECVD SiO_2 sample, PECVD Si_3N_4 sample, and E-gun Al_2O_3 sample are 3.5×10^{12}, 6.9×10^{12}, and 7.1×10^{12} cm^{-2} eV^{-1}, respectively. For the comparison with the original and the stressed device, the degradation ratios of the PECVD SiO_2 sample, PECVD

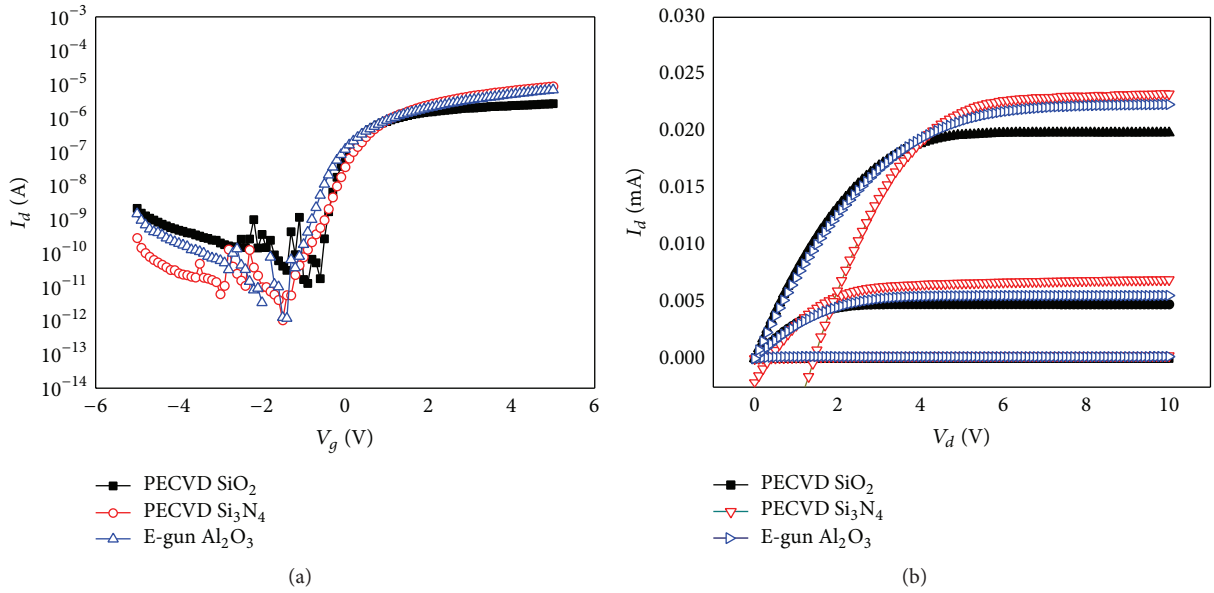

FIGURE 2: (a) I_d-V_g curve of the a-IGZO TFTs using high-k materials. (b) I_d-V_d curve of the a-IGZO TFTs using high-k materials.

Si_3N_4 sample, and E-gun Al_2O_3 sample are 20.6%, 4.5%, and 34.0%, respectively. As a result, the IGZO TFTs with Si_3N_4 gate dielectric have the lowest D_{it} after stressing.

According to the experimental results, the type of gate oxide layer had a substantial influence on the performance of the IGZO thin film transistor (TFT). As indicated in previous studies, stress-induced component characteristics are analogous to those of PECVD Si_3N_4 sample and dry oxide sample (control), demonstrating shifts in their V_t. Such shift is attributed to the donor-like trap at the interface between the insulating layer and IGZO layer. As shown in Figure 4, generally, a donor-like carrier located below the Fermi level is considered as a neutral carrier, whereas one located above the Fermi level is considered as a positively charged carrier. When positive voltage stress is applied to a gate, the conduction band bends downward because of the electric field, reducing the distance between the contact surface and the Fermi level. This behavior suggests that the number of positively charged donor-like carriers between the conduction band and Fermi level decreases, increasing the number of neutral carriers. If the conduction band that bends because of stress is measured before it returns to its unbent state, then V_t becomes large and shifts to the right because of the decrease in the number of positive charges; consequently, the conduction band cannot attract more electrons and higher voltage is required to obtain the same number of electrons. Conversely, when negative voltage stress is applied to a gate, the conduction band bends upward, the number of positively charged donor-like carriers increases, and the number of neutral carriers decreases, thus diminishing V_t and shifting V_t to the left [21].

In low temperature processes, except for PECVD Si_3N_4 sample in the gate-insulating layer, the channels of other insulting layer materials cannot close under positive voltage stress. Disregarding the fact that this phenomenon is a result of I_g current induced by the collapse of the insulating layer, this study considered interface-related problems. Some IGZO carriers are provided by oxygen vacancies; therefore, in this study, the responses of the interface between the IGZO and insulating layer materials were examined to determine whether the IGZO and the insulating layer materials competed for oxygen and whether the IGZO produces extra oxygen vacancies. The standard heat of formation ΔH_f° indicates that Al_2O_3 < SiO_2 < Si_3N_4 [24, 25]. As shown in Table 2, the forming of negative heat indicates that a chemical compound is stable, the probability of interface formation is large, and the chemical compounds in IGZO compete for oxygen (according to the table, the heat formation in ZnO is close to zero; thus, the oxygen in ZnO is most likely occupied). The behaviors of the SiO_2 control sample formed through using a horizontal furnace tube and SiO_2 sample developed through plasma-enhanced chemical vapor deposition have resulted from oxide layer defects near the interface.

TABLE 2: Gate-insulating layer and heat formation in IGZO compounds.

	Gate-insulating layer			IGZO		
Heat of formation	Si_3N_4	SiO_2	Al_2O_3	In_2O_3	Ga_2O_3	ZnO
ΔH_f° (kJ/mol)	−743.5	−910.7	−1675.7	−925	−1089.1	−350.5

According to the aforementioned hypothesis, the following explanations for deterioration were proposed. When a gate is influenced by positive voltage stress, accumulated IGZO electrons may be trapped in the interface or in the oxide layer defects. These trapped electrons generate electric fields even when voltage stress is not applied. Accordingly, the conduction band can bend downward without positive voltage stress causing electrons to accumulate. If the insulating layer accepts oxygen in the IGZO, then additional oxygen vacancies and electrons are produced. Once additional electrons under positive voltage stress are trapped in the interface

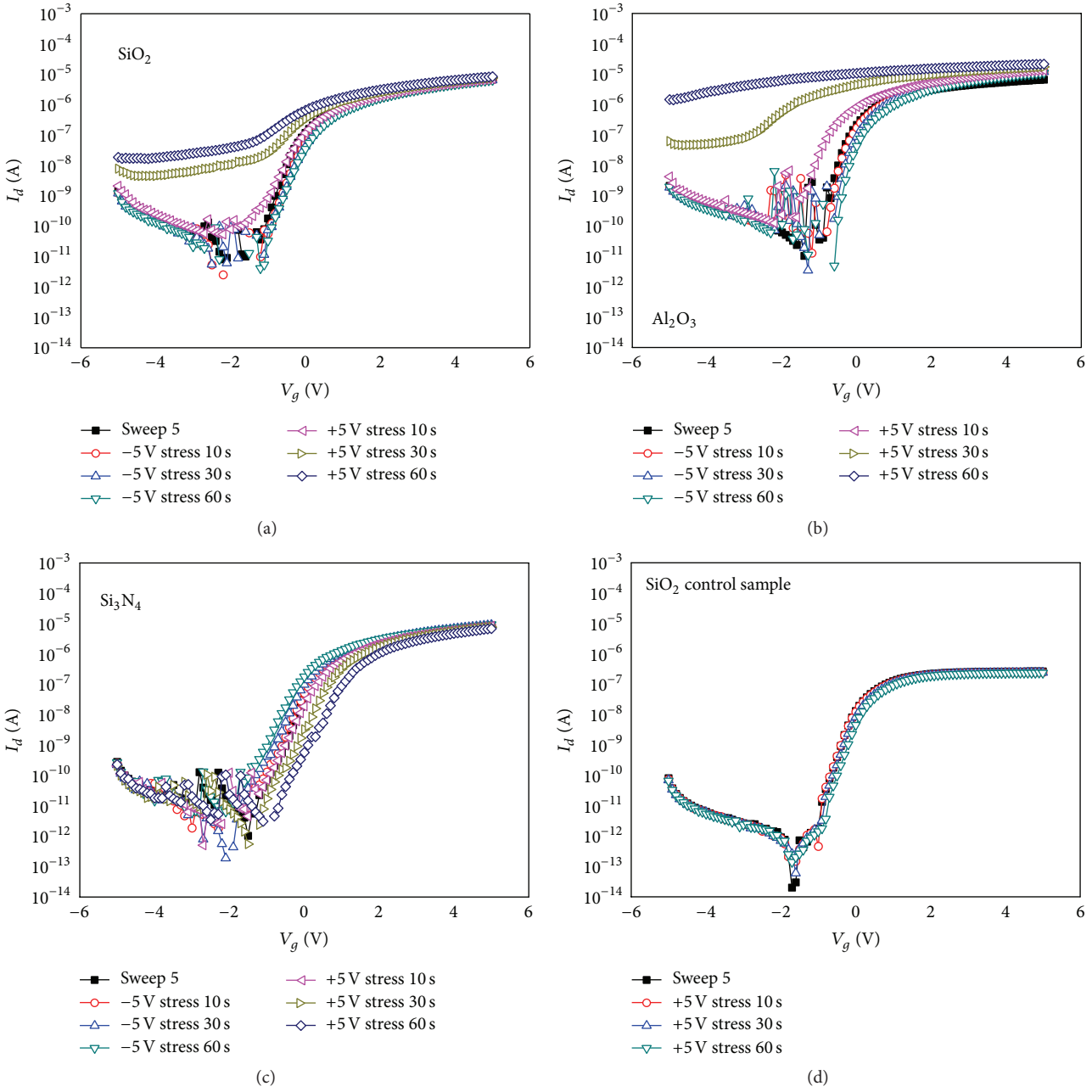

FIGURE 3: Various insulating layers with ±5 V stress for I_d-V_g comparison: (a) PECVD SiO_2, (b) E-gun Al_2O_3, (c) PECVD Si_3N_4, and (d) SiO_2 control sample of furnace process.

or in the oxide layer defects, the conduction band is severely bent downward and a considerable number of electrons accumulate. Consequently, the component channels cannot close and the band diagram was shown in Figure 5.

4. Conclusion

In this paper, we demonstrate the low temperature IGZO TFT device with different high-k gate dielectric materials such as PECVD Si_3N_4 (300°C) and E-gun Al_2O_3 (room temperature) and they are compared to the PECVD SiO_4 (300°C). The PECVD Si_3N_4 sample could yield high mobility, high I_{ON}/I_{OFF} ratio, high I_{ON}, low I_{OFF}, and better stress effect than others. The stability between the high-k dielectric thin film and IGZO thin film caused interface roughness due to the heat formation difference during temperature annealing. The charge is generated in the interface and results in V_t shift during stress. The stress effect could be explained in the interface by charge band diagram. As a result, the IGZO TFTs with Si_3N_4 gate dielectric exhibit good characteristics with acceptable reliability in the low temperature process.

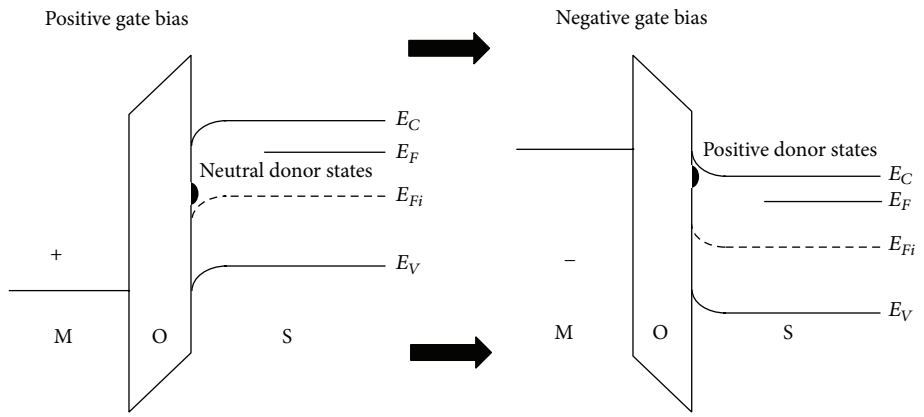

Figure 4: Mechanisms of positive and negative gate voltage stress.

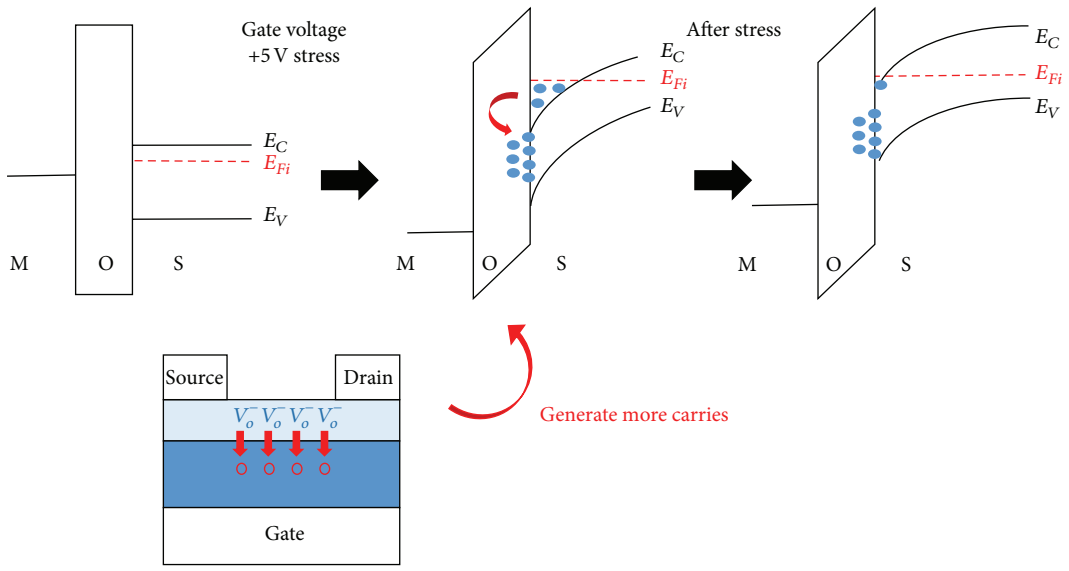

Figure 5: Deterioration of components after applying positive gate voltage stress.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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