

Research Article

Chemical-Vapor-Deposited Graphene as Charge Storage Layer in Flash Memory Device

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We demonstrated a flash memory device with chemical-vapor-deposited graphene as a charge trapping layer. It was found that the average RMS roughness of block oxide on graphene storage layer can be significantly reduced from 5.9 nm to 0.5 nm by inserting a seed metal layer, which was verified by AFM measurements. The memory window is 5.6 V for a dual sweep of ± 12 V at room temperature. Moreover, a reduced hysteresis at the low temperature was observed, indicative of water molecules or $-OH$ groups between graphene and dielectric playing an important role in memory windows.

1. Introduction

Flash memory has been highly demanded for mobile phone, digital camera, communication system, and data storage owing to its small size, high density, and low power. However, lateral scaling in flash memory will increase the capacitive coupling between the adjacent floating gates [1]. This parasitic capacitive coupling between neighboring cells will induce a wide distribution of threshold voltage because of the cell-to-cell interference, leading to a remarkable read-out error in circuits. In particular beyond the 12 nm node, the issue of cell-to-cell interference will become much more severe [2]. To address this problem, the floating gate thickness reduction is one possible way. For conventionally used poly-Si floating gates, its thickness can be reduced to several nanometers; however, it will bring a large ballistic current during program processes [3], causing significant reliability issues. On the other hand, the charge storage capability in floating gates will degrade because of reduced density of state of poly-Si under such continuous scaling along the thickness direction [4]. Although thin metal layer was proposed to replace poly-Si floating gate, there are many other issues introduced at high temperatures, such as diffusion of metal into the blocking and tunneling oxide layer, and metal induced dielectric crystallization [5–7].

Recently, graphene, a two-dimension single layer of carbon atoms with sp^2 hybridized structure, has emerged as a promising material for future electronic applications owing to its unique physical and electrical properties [8–13]. Because the interlayer spacing between two monolayer graphene sheets is 0.34 nm [8], then the thickness of multilayer (e.g., 4–8 layers) graphene is around 1.5–3 nm, which may be implemented into flash memory for the thickness reduction in the floating gate. Note that its work function of ~ 4.6 eV can be stabilized when the number of graphene layers reaches 4 [14]. Moreover, its thermal stability ($>1000^\circ\text{C}$) vanishes the diffusion issues at high temperatures, offering the benefits to the integration of memory devices. There are additional advantages for multilayer graphene as a floating gate, for example, (1) being compatible with conventional planar CMOS process line; (2) suppression of the ballistic current along the thickness direction because of reduced conductivity between layers; (3) large DOS; and (4) high work function which can increase the capability for storage and long-term data retention [5, 15]. It was reported that graphene layers can be utilized as not only a floating gate for conventional silicon MOS capacitors [5, 15] but also a novel channel material of transition metal dichalcogenide, for example, MoS_2 [16], high-k stack or PZT based charge-trap memory [17–20], organic nonvolatile memory [21], and transparent

flexible charge-trap memory [22]. A large hysteresis (memory window) of ~ 6 V was observed under a low voltage program/erase process [15]. In addition, graphene oxide (GO) was also incorporated into TANOS as a trapping layer, while it suffers the reliability issues since the charge storage capability will significantly degrade at high temperatures [23].

In this work, we demonstrated a flash memory device with chemical-vapor-deposited graphene as a charge trapping layer. The fabricated devices exhibit an increased memory window as a dual sweep bias was enhanced. Interestingly, we also observed a reduced hysteresis at low temperature, indicative of $-\text{OH}$ or water molecules between graphene and dielectric playing an important role in memory windows.

2. Experimental Details

Graphene layers were prepared by a chemical-vapor-deposition (CVD) technique in a home-made tube furnace. An 850 nm thick Cu film was thermally evaporated on the mica substrate at 500°C , where atomically flat surface of single crystal mica substrate was obtained by a tape cleaving [8]. To remove oxidized layer and contaminations on Cu surface, Cu/mica substrates were annealed in H_2/Ar gas ambient at 1000°C for half hours prior to the graphene growth [24]. Then graphene was grown on the Cu/mica substrate by introducing CH_4 in the tube at the same temperature and the pressure inside the tube was kept roughly at one atmosphere. Graphene size ($50\ \mu\text{m} \times 50\ \mu\text{m}$) was patterned by definition by lithography and followed by an O_2 -plasma etching. The Cu film on mica was dissolved in HCl aqueous solution. The schematic device structure, optical image of the fabricated device, and its fabrication processes are illustrated in Figures 1(a), 1(b), and 1(c), respectively.

The tunneling oxide was a thermally grown 5 nm thick SiO_2 . The thickness of the tunneling oxide is determined from both ellipsometer spectrometry and separate electrical C - V measurements. Graphene was then transferred onto the SiO_2 (5 nm)/p-Si substrate using the polymethyl methacrylate-(PMMA-) assisted transfer method [24]. Prior to the growth of the blocking oxide, a seed layer of Al was deposited onto graphene/ SiO_2 /Si and oxidized in the O_2 ambient. A 20 nm thick Al_2O_3 was subsequently deposited by atomic-layer deposition (ALD), where Al_2O_3 was grown using trimethyl aluminum (TMA) and H_2O as precursors at 200°C . The relative dielectric constant of Al_2O_3 is extracted to be 7.5 from the control sample. Finally the top electrode was formed in turn by electron-beam lithography, thermal evaporation of Au, and a lift-off process in acetone. The Raman characterization was carried out by an Ar laser unit of 488 nm excitation. The surface roughness (RMS) was analyzed by atomic force microscopy (AFM). The electrical I - V and C - V measurements were performed using a semiconductor (Agilent B1500A) device analyzer and a precise impedance analyzer (Agilent 4294A) with a 50 mV AC amplitude at 100 KHz, respectively.

3. Results and Discussion

Figure 2(a) shows the optical image of as-transferred graphene film on SiO_2 /Si substrate. To better characterize

CVD graphene, a silicon substrate with 90 nm SiO_2 was used here for the best optical contrast. The surface coverage of as-transferred bilayer graphene is more than 50%. Note that all the Raman spectra shown in this paper are calibrated using silicon peak at $520\ \text{cm}^{-1}$. Figure 2(b) shows the typical Raman spectra of monolayer and bilayer CVD graphene. It can be clearly seen that there is a D band in the as-transferred CVD graphene. It is quite different from the pristine one mechanically exfoliated from bulky graphite, which only has two main characteristic peaks of G and 2D. This infers that transfer process needs to be further improved for the high quality graphene on SiO_2 /Si substrate. Note that a sharp line width ($\sim 30\ \text{cm}^{-1}$) and a single Lorentzian lineshape in 2D band were also observed for bilayer CVD graphene. It is due to an ordered AB stacking, resulting in a weak electronic coupling between graphene layers [25].

Owing to its inherent characteristic of no dangling bonds, the top gate dielectric is quite tough to be formed on graphene. In order to alleviate this issue, a seed layer of Al was deposited and oxidized into an Al_2O_3 layer. Figures 3(a) and 3(b) show the AFM images of an atomic-layer-deposited 100-cycle Al_2O_3 film on highly oriented pyrolytic graphite (HOPG) substrate without and with an Al seed layer, respectively. It was observed that a striped pattern of Al_2O_3 film was formed along grain boundaries and defects sites without an Al seed layer, while a fairly uniform Al_2O_3 surface was achieved on HOPG with an Al seed layer. This prominent difference in Al_2O_3 /HOPG lies in the chemical inertness of HOPG surface, thus leading to a deep cluster or nucleation of Al_2O_3 dielectric film preferentially in the sites of grain boundaries [26, 27]. It is worthwhile to mention that, in contrast to the pristine graphene, the functionalized surface is prone to ALD growth of a uniform high- k dielectric film although the film quality still needs further improvement [28]. The surface roughness (RMS) of an atomic-layer-deposited 100-cycle Al_2O_3 film on HOPG using various thickness of Al seed layer was summarized in Figure 3(c). Without an Al seed layer, its average RMS is as large as ~ 5.9 nm, while it decreases to 0.55 nm when a 0.2 mg Al metal (~ 1 nm Al_2O_3) target was evaporated for the seed layer. It was also found that the RMS roughness can be further reduced if the thickness of an Al seed layer increases, as shown in Figure 3(c).

Next, we turn to the C - V measurements of fabricated graphene flash memory cell with the help of an Al seed layer. Figure 4(a) shows the representative C - V characteristics of fabricated graphene flash cell at room temperature. There is a clear hysteresis of ~ 2.3 V under a dual sweep of ± 8 V for the Au/ Al_2O_3 /graphene/ SiO_2 /p-Si cell. For the control sample, almost no noticeable hysteresis was observed, as shown in the inset of Figure 4(a). The comparison of hysteresis for both graphene flash memory and control cell under various dual sweep biases is illustrated in Figure 4(b). It can be noticed that the memory window is 1.0 V, 2.3 V, 4.0 V, and 5.6 V for the dual sweep of ± 6 V, ± 8 V, ± 10 V, and ± 12 V, respectively. The amount of charge storage in graphene layers can be estimated by $\Delta n = C_{\text{con}} \times \Delta V / q$, where C_{con} is the unit control gate capacitance, that is, the capacitance of Al_2O_3 layer, ΔV is the memory window, and q is the unit electron charge. As

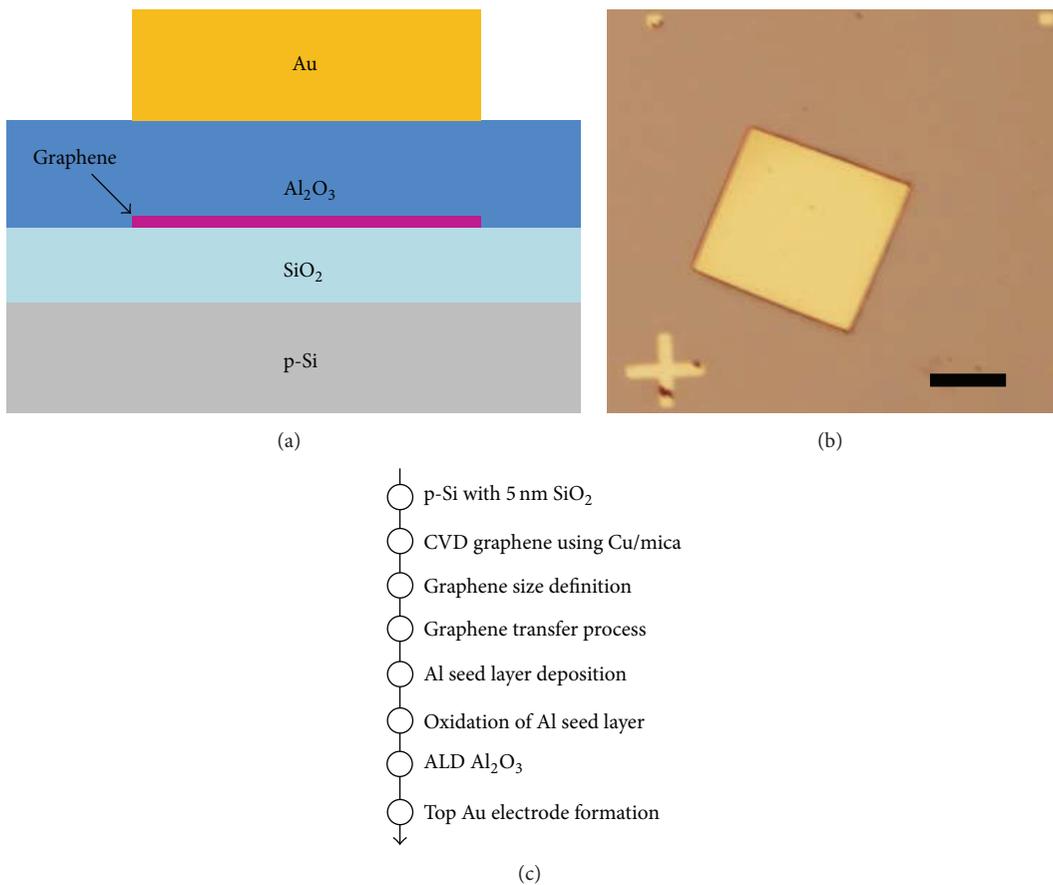


FIGURE 1: (a) The schematic of graphene flash memory cell (Au/Al₂O₃/graphene/SiO₂/p-Si). (b) Top-view of fabricated graphene flash memory cell. The scale bar is 20 μm. (c) Process flow of fabricated graphene flash memory cell.

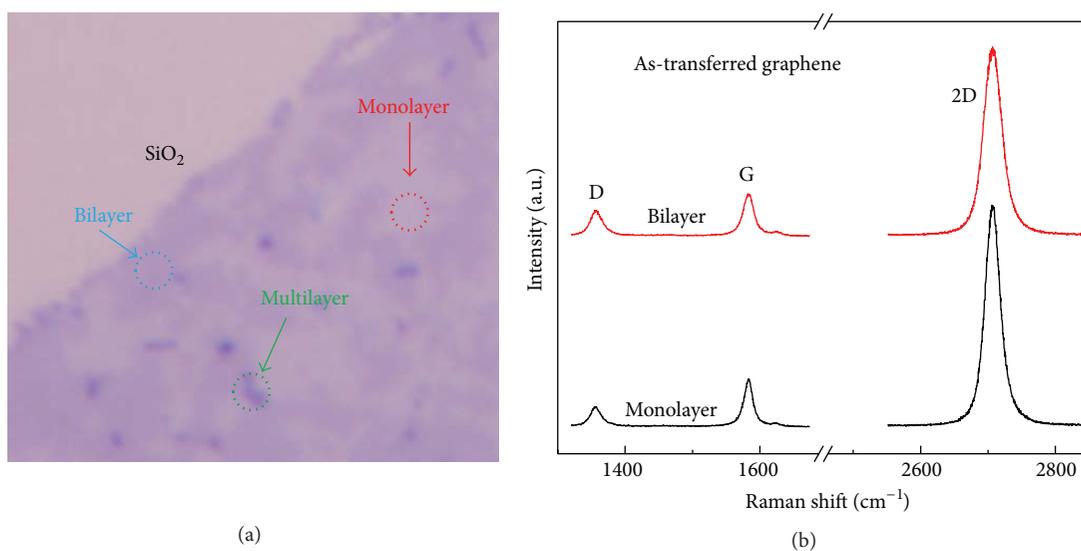


FIGURE 2: (a) The optical image of as-transferred CVD graphene on SiO₂/Si substrate. The image size is 20 μm × 20 μm. (b) Raman spectra of as-transferred monolayer and bilayer graphene.

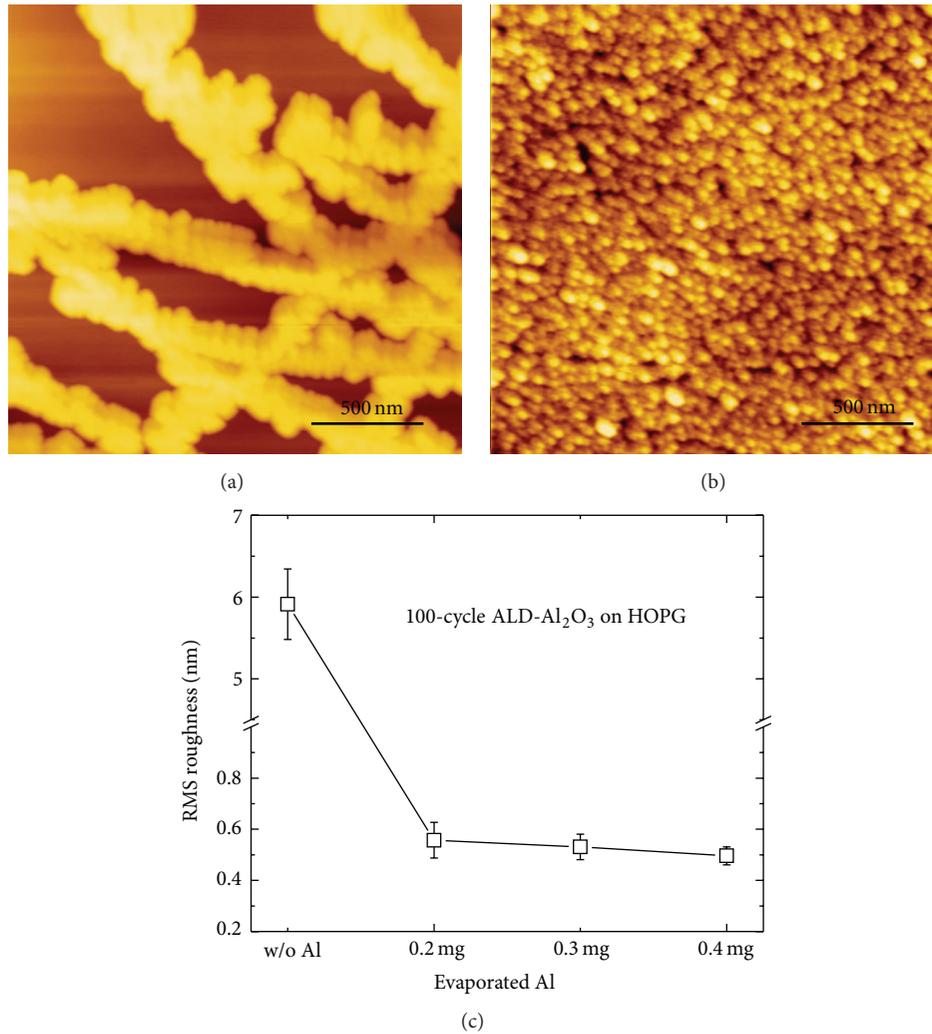


FIGURE 3: (a) Atomic force microscopy (AFM) image of an atomic-layer-deposited 100-cycle Al_2O_3 film on highly oriented pyrolytic graphite (HOPG) substrate without and with an Al seed layer. The scale bar is 500 nm. (b) Surface roughness (RMS) of an atomic-layer-deposited 100-cycle Al_2O_3 film on HOPG without and with 0.2 mg, 0.3 mg, and 0.4 mg Al for the seed layer thermal evaporation.

a result, the storage charge density in graphene layer for the hysteresis of ~ 2.3 V in Figure 4(a) is accordingly around $4.76 \times 10^{12} \text{ cm}^{-2}$. In contrast to graphene flash memory cell, only a small hysteresis of ~ 40 mV at the dual sweep of ± 12 V remains for the control cell at room temperature; see Figure 4(b). This indicates a pronounced memory window in graphene flash memory cell, where the memory effect results from the charge storage in graphene film, consistent with the previous reports [7, 15]. Compared to monolayer and bilayer graphene, a significant hysteresis may take place in few layer graphene based flash memory because of its large density of state [15]. The process improvement of the growth of multilayer graphene is further needed to realize large memory windows.

We also examined the C - V characteristics of graphene flash cells at low temperature of 250 K. It is interesting that the memory window for graphene flash memory cell decreases significantly, as shown in Figure 4(b), that is, even only a small hysteresis of 1.5 V for a dual sweep of ± 12 V.

Similar hysteretic behaviors have also been observed in the $I_d - V_g$ behaviors for a dual sweep V_g in the back-gated graphene field-effect transistor [29], and Dirac point shift in a quantum capacitance measurement [30]. This reduction in the hysteresis in graphene or carbon nanotube field-effect transistors was attributed to the orientation polarization of water [29–36]. Hydroxyl groups ($-\text{OH}$) can couple to the dangling bonds of Si and build up a layer of silanol (SiOH) groups, which is very hydrophilic [37, 38]. Water molecules can easily attach to the SiOH and contribute to the charge transfer [36]. It was reported that the formation of Si-O-Si siloxane from the hydration of silanol groups will take place at more than 450°C [39]. In case of our transfer process, water molecules bonding to Si-OH silanol groups will thus inevitably be introduced in the interfaces between graphene and dielectrics (e.g., SiO_2). The fact that the hysteresis reduces significantly at low temperatures indicates there is a clear mechanism difference in electron trapping in graphene flash

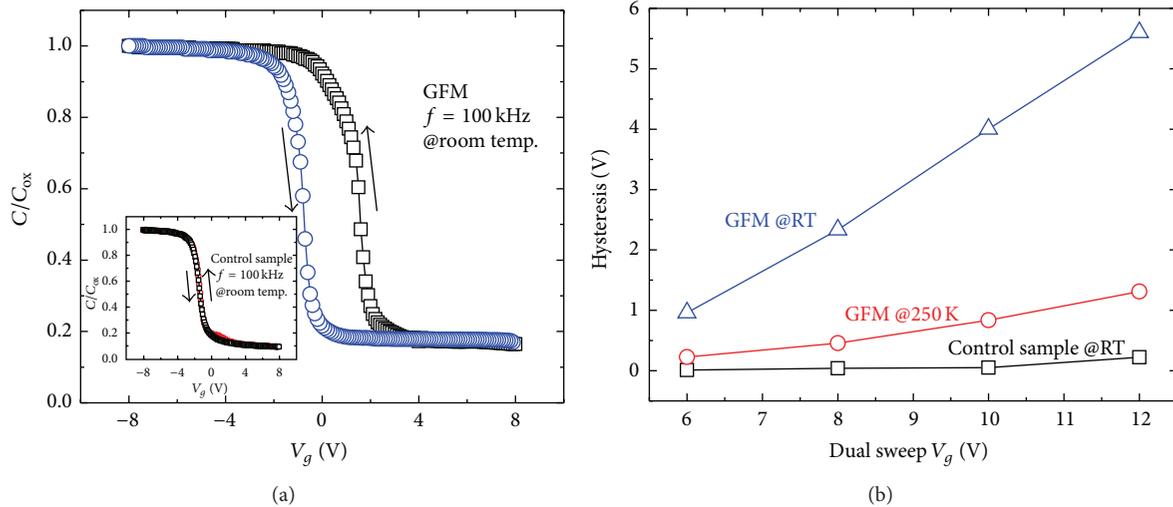


FIGURE 4: (a) Representative capacitance-voltage (C - V) characteristics of fabricated graphene flash memory at room temperature (RT). Inset shows C - V characteristics of the control sample. The arrows denote the sweep directions. (b) Comparison of hysteresis of graphene flash memory cell and control sample at both RT and 250 K.

cell. Thus, it is believed that the orientation polarization of water molecules plays a crucial role in the memory window for graphene memory devices at the low temperature.

4. Conclusion

In summary, a flash memory device with chemical-vapor-deposited graphene as a charge trapping layer was fabricated. A buffer Al_2O_3 layer oxidized from a seed layer can reduce one order of magnitude of the average RMS roughness, prior to the growth of ALD Al_2O_3 blocking oxide, which is important to achieve high performance graphene memory devices. In addition, large memory window of 5.6 V was observed for a dual sweep of ± 12 V at room temperature. It exhibits a remarkable reduction in memory window at the low temperature, which is attributed to the decrease of water polarization.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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