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Research Article

Characteristics of a Multiple-Layered Graphene Oxide Memory Thin Film Transistor with Gold Nanoparticle Embedded as Charging Elements

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In this study, we report the highest mobility in the reduced graphene oxide- (rGO-) based TFTs embedded with Au NPs. In addition, we fabricated a reduced graphene oxide memory device (rGO-capacitor), a reduced graphene oxide thin film transistor (rGO-TFT), and a reduced graphene oxide memory thin film transistor (rGO-MTFT) and characterized their electrical performances. While the rGO-TFT device was investigated for nonambipolar channel performance, the rGO-capacitor and rGO-MTFT were examined for nonvolatile memory capabilities in a metal-graphene-insulator-silicon (MGIS) structure. The incorporation of the gold nanoparticles (Au NPs) between the rGO and an insulator silicon dioxide (SiO_2) layer served as a charging element. The rGO-capacitor revealed the memory effect of hysteretic capacitance-voltage (C-V) loops, and the flat-band voltage shift (ΔV_{FB}) was measured as 0.1375 V after 100 s retention time. The rGO-TFT shows the p-channel characteristics with high hole mobility of 16.479 cm^2/V·s. The threshold voltage shift (ΔV_{th}) of the rGO-MTFT was detected as 5.74 V from 10 V to -30 V sweep, demonstrating high mobility of 22.887 cm^2/V·s.

1. Introduction

Since the discovery of graphene by Novoselov and Geim in 2004, two-dimensional (2D) materials have ushered in a new era for next-generation nanoelectronics [1, 2]. Graphene is a monolayer of high-density 2D carbon atoms, which has been intensively investigated for its high electron mobility and versatile electrochemical resources [3–13]. Even though the graphene inherently has zero bandgap, the bandgap could be manipulated in its conductance via charged impurity centers, ribbon or ripple shape, and chemical modifications [5–7]. In particular, the graphene can be used for an active layer [5–10], charging nodes for nonvolatile floating gate (FG) device and resistive switching device [11–13], and even dielectrics for electronic applications depending on its chemical modification [14]. In addition, the graphene sheets can serve as charging and discharging layers for memory devices [15–17]. A reduced form of graphene oxide has been extensively utilized for a variety of devices including sensors, solar cells, and TFTs [7–9]. Moreover, the graphene or GO has been recently adopted as components for resistive switching devices [11, 12, 15]. Since the graphene oxide could be prepared by a chemical exfoliation method, it is adequate for simple, economical, and large-scale production compared with a chemical vapor deposition (CVD) method, etc. Through the thermal or chemical reduction process, a moderate level of conductance of the graphene is recovered in the rGO, which is still acceptable in the nanoelectronics as electrical charging nodes or active channel [13, 14].

On the other hand, remarkable advancement in organic memory devices has proceeded with NP embodiment [17–19]. For a single-layered graphene, NP embodiment could enhance mobility [12].

Due to cost-effectiveness and facile manufacturability, NP-based nonvolatile memory devices have been developed in the fields of electronics, sensor arrays, and memory cards. The popularity of organic memory devices becomes increasing as an alternative to overcome the limitations of the conventional silicon-based semiconductors such as the reduction of channel length (pinch-off), thermal power issues, and conductivity modulation. The flash device that uses FG transistors is a basic format of memory devices. By applying a voltage pulse on the gate electrode, electrons or holes can tunnel from the semiconductor channel to the storage layer, which induce charging or memory effects. For the organic nanoelectronic applications, the GO or rGO is often employed as a charge trapping mediator intervened in the structure of metal/insulator/silicon (MIS) layers. However, the role of the GO and rGO is reverse in the charge trapping mechanism to differentiate the speed of the device operation [7–9, 17, 20]. The hole mobilities of the GO-based memory TFTs have been reported as low values even less than $1\,cm^2/V{\cdot}s$ [9, 17, 18], while the rGO-based graphene TFT could show a very high hole mobility of $300\,cm^2/V{\cdot}s$ even on a flexible substrate [14]. However, the rGO-TFT did not show memory functionality without FG array structure, and a relatively complicated Langmuir-Blodgett (LB) process was required to have the rGO active layer instead of a simple dip-coating process along with additional passivation layer [14].

Although there have been many reports of memory effects using active rGO layers and embedded metal NP devices, fundamental studies of memory windows on charging behavior or charge storage in NPs with solution-processed rGO and reduced graphene oxide quantum dot (rGOQDs) films have not been extensively reported [16–22]. Furthermore, conventional graphene memory devices have been frequently involved in complicated processes to form a dielectric layer with an atomic layer deposition (ALD) using high k materials like Al_2O_3 [16–18]. In addition, most of the devices were realized in very small channel width and length of 3 to 7 μm, which cannot be applied to a flexible substrate with large area [17, 20].

In other hand, a number of two-dimensional (2D) semiconductor active materials have been continuously introduced including semimetallic graphene, rGO, molybdenum disulfide (MoS2), and phosphorene [23–25]. However, the graphene or rGO still affords relatively high mobility for field effect transistor (FET) and stability in air compared to other 2D channel materials [25].

In this study, we present the reduced graphene oxide memory thin film transistor (rGO-MTFT) device with high mobility of $22.887\,cm^2/V{\cdot}s$. This is the highest mobility in the reduced graphene oxide- (rGO-) based TFTs embedded with Au NPs. The MTFT fabrication was based on the formation of Au NPs as charge storage elements, and the monolayer of rGO was accomplished at room temperature using a dip-coating process. Self-assembly monolayer (SAM) Au NPs on SiO_2 displayed efficient charging effect underneath the rGO channel. We also demonstrated the performance of rGO-MTFT with large scale of channel width (100 μm) and length (100 μm), which can be confirmed from a threshold voltage shift (ΔV_{th}) of transfer curve after bias in a gate electrode.

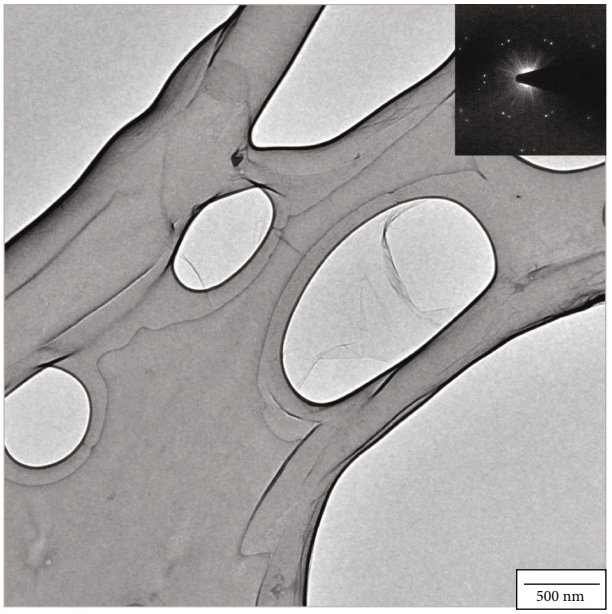
2. Experimental Section

Graphite oxide was prepared through a modified process by Hummer's method [19, 20]. Graphite (flakes, 99% carbon basis, Sigma-Aldrich) were added into furic acid (H_2SO_4) 34 mL (95%-extra pure grade, Junsei) containing sodium nitrate ($NaNO_3$) 0.75 g (99.0%, Sigma-Aldrich) in a 250 mL flask, kept in an ice-water bath and vigorously stirred by a magnetic stirring bar. Potassium permanganate ($KMnO_4$) 5.0 g (97.0%, Sigma-Aldrich) was added slowly, and then, the temperature was increased to 35°C. After the mixture was stirred for 2 h, ultrapure deionized water (50 mL) was added into the ice-bathed flask. Then, addition of 4.0 mL hydrogen peroxide (H_2O_2) (35.0%, Junsei) solution was followed drop by drop into the above mixture with stirring for 2 h. The mixture was filtered with a 1 : 10 ratio hydrochloric acid (HCl, 35%-extra pure grade, Junsei)/DI water 500 mL. Then, the graphite oxide flakes were washed with DI water under the sedimentation by centrifugation until the suspensions reached pH 7. Finally, the resulting graphene oxide (GO) aqueous solution was sonicated for 5 h and centrifuged at 4000 rpm for 30 min to collect a stable GO solution from a supernatant. Figure 1(a) shows TEM image and selected area electron diffraction (SAED) pattern image (inset) of the solution-processed GO sheets by the modified Hummer's method.

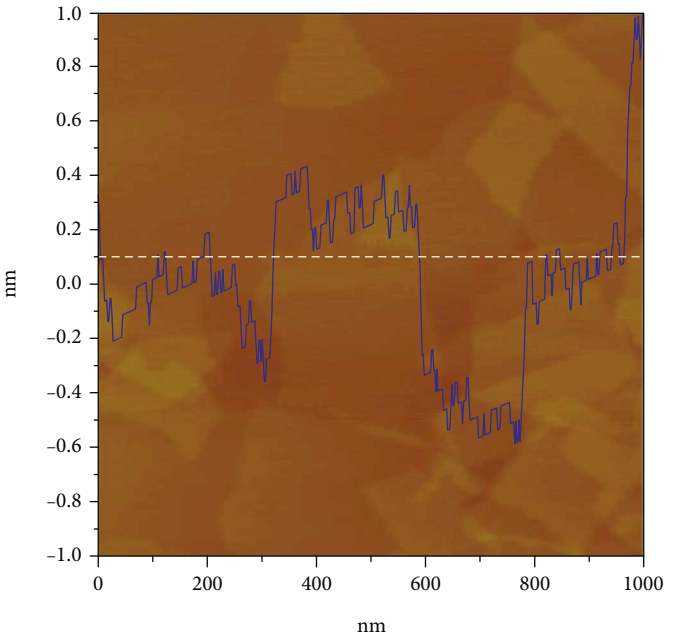
For the preparation of the reduced graphene oxide (rGO), GO films were exposed to hydrazine hydrate (H_2N_4) vapor states, which drives conversion of the GO into the rGO from an insulator to a semimetal [23–25]. The condition of reduction condition with the hydrazine vapor state was at 200°C for 1 min.

Au nanoparticle (Au NP) colloids (5 nm) were purchased from British Biocell International (BBI). Then, Au NPs were capped by a 1.0 M citric acid solution (Sigma-Aldrich) by mixing 1 : 1 ratio and incubating it overnight. The mixture was centrifuged with a membrane filter (Vivaspin 500, Satorius Biotech) to collect selectively the citrate-coated Au NPs. The collected citrate-capped Au NPs were resuspended in ultrapure DI water. A self-assembled monolayer (SAM) of the Au NPs and the 3-aminopropyl-triethoxysilane (APTES) on the substrate were executed by vertically immersing in the solution of the citrate-capped Au NPs and APTES. The SAM of APTES was uniformly prepared, and both GO and Au NPs were stably adsorbed on the Si substrate through electrostatic attraction between the negatively charged citric acid-capped Au NPs and the positively charged amino groups (NH_3^+). Figure 1(b) shows atomic force microscopy (AFM) image of the evenly formed GO SAM film.

Figure 2(a) shows the schematics for fabricating the rGO-based memory device, TFT and memory TFT. Figure 2(a), A shows the initial substrate that was a boron-doped p-type



(a)



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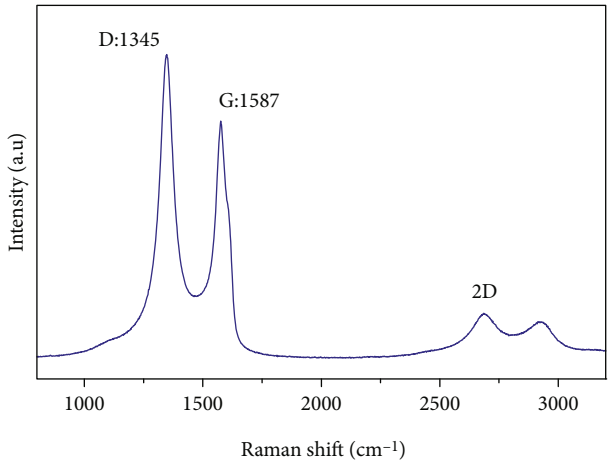
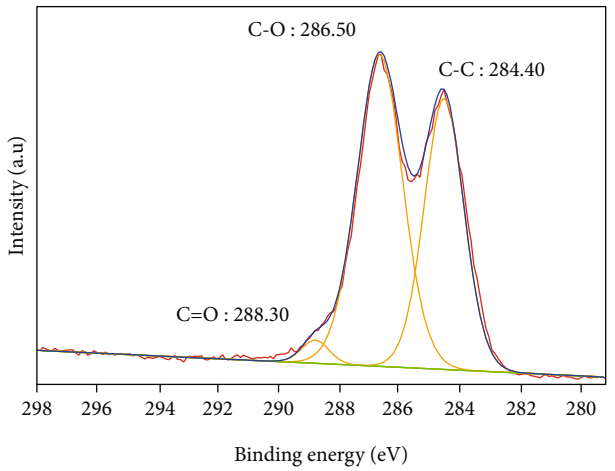
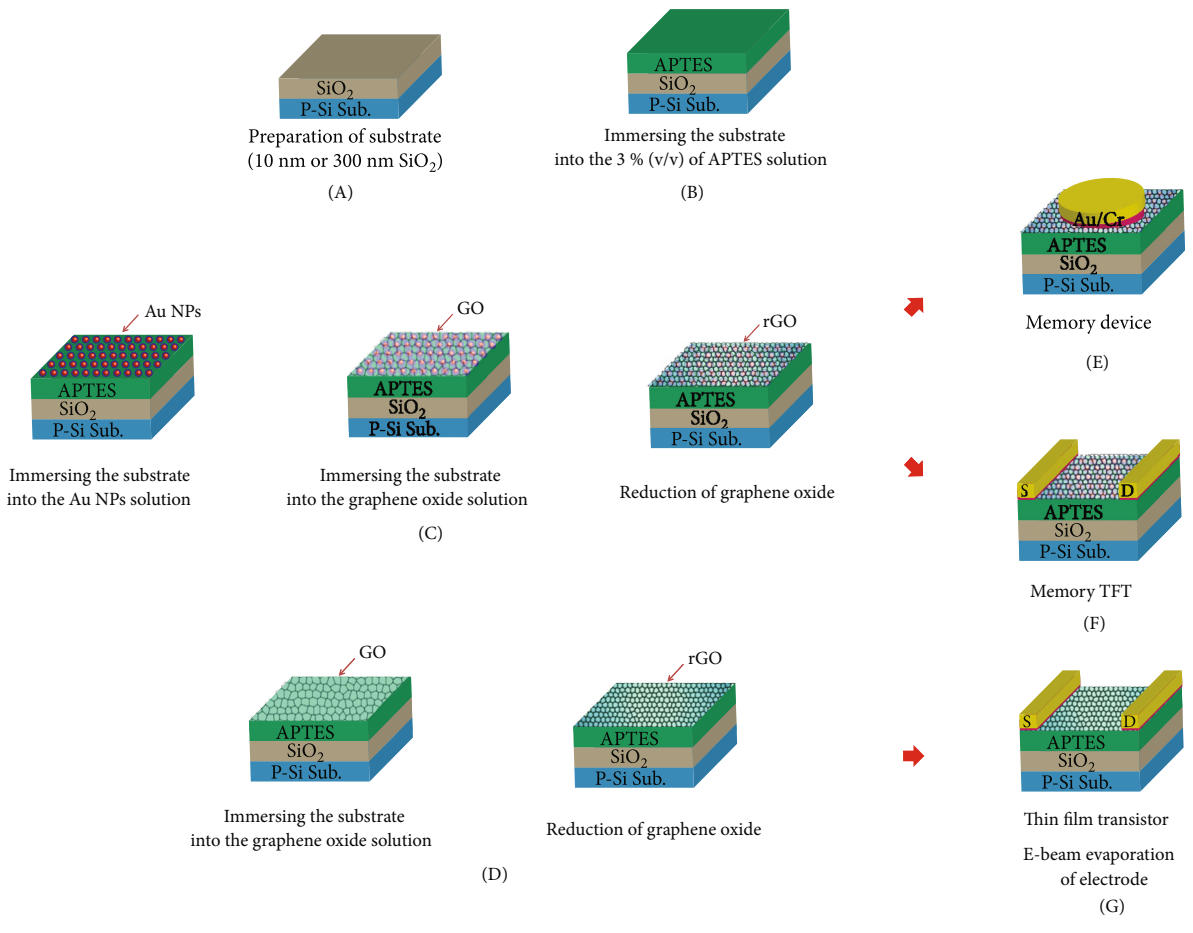




(c)

Figure 1: (a) TEM image of a graphene oxide (GO) sheet and the SAED pattern image (inset). (b) AFM image of graphene oxide (GO) sheets. The average height was 0.5 nm. (c). Analysis of GO Raman and XPS (top) Raman spectrum D: 1345 cm^{-1} and G: 1587 cm^{-1} and 2D (bottom) XPS spectrum C=C bond: 284.40 eV, C-O bond: 286.50 eV, and C=O bond 288.30 eV.



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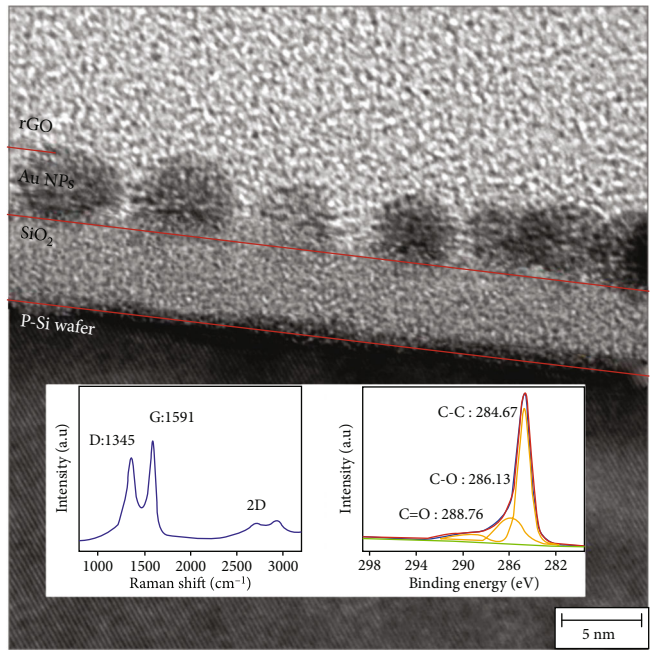

(b)

Figure 2: (a) Schematics for the fabrication of the-rGO based devices. (A) Rinsing the SiO_2 coated Si wafer. (B) Dipping the substrate into the APTES solution. (C) Dip-coating the substrate into the Au NP solution and in the GO solution and then reducing under H_2N_4 vapor. (D) Dip-coating the substrate into the GO solution and then reducing under H_2N_4 vapor. (E–G) Depositing the Au/Cr electrode on the rGO devices. (b) TEM image of rGO-memory device (scale bar: 5 nm) with inset graphs of Raman (left) and XPS (right) spectra of the rGO.

silicon wafer (100) coated with 10 or 300 nm thick SiO_2 layer (a resistivity of 0.001~0.003 Ω-cm). The Si substrate was serially washed by sonication in acetone (J. T. Baker, cMOS), 2-propanol (IPA, J. T. Baker, cMOS), and deionized (DI) water. After blowing with a N_2 gas gun, the substrate was dried on the hotplate at 80°C for 5 min. Figure 2(a), B shows the modification of the SiO_2 surface with 3-aminopropyltriethoxysilane (APTES) by dip-coating the substrate in 3% (v/v) APTES dissolved in anhydrous ethanol for 1 h. For the formation of the self-assembly of Au monolayer on the SiO_2 layer, a dip-coating process was adopted. The substrate was dip-coated into the citric acid-capped Au NP solution in DI water for 12 h (Figure 2(a), C). The preparation of the capped Au NPs was described in the supplementary information. Then, the substrate was immersed in the GO solution for dip-coating and undergone with a reducing process with hydrazine hydrate (H_2N_4) at 200°C for 1 min [11, 12]. For the rGO-memory device (capacitor), a top circular electrode (500 μm radius) made of Cr (10 nm thickness) and Au (100 nm thickness) was deposited by an e-beam evaporator (Figure 2(a), E). For the rGO-MTFT, the electrodes for source and drain were patterned at the end with 10 μm width and 100 μm length (Figure 2(a), F). The rGO-TFT was fabricated following the same procedure as above on the 300 nm thick SiO_2 substrate except the monolayer formation of Au NPs (Figure 2(a), D). Then, the electrodes for source and drain were deposited by an e-beam evaporator (Figure 2(a), G). Figure 2(b) shows a TEM image of rGO-MTFT device (scale bar: 5 nm) with inset graphs of Raman (left) and XPS (right) spectra of the rGO after completion of the sequential fabrication steps illustrated in Figure 2(a).

Electrical characterization methods for the rGO-capacitor, rGO-TFT, and rGO-MTFT: the memory effect of the Au NP embedded device was systematically investigated from hysteresis of capacitance-voltage (C-V), breakdown current-voltage (I-V), and retention measurement from 10 s to 100,000 s in ambient condition without any passivation or encapsulation. The retention test for the charge storage of Au NPs was measured at 1 MHz frequency. The capacitance-voltage measurement of the device was performed by an HP 4284A LCR meter at the frequency of 1 MHz (a step by 0.1 V), and the current-voltage measurement was executed by an HP 4145B semiconductor parameter analyzer (a step by 0.5 V).

3. Result and Discussions

3.1. Analysis of the GO Sheets. The GO sheets were analyzed by high-resolution transmission electron microscope (HR-TEM, Tecnai G2 F30). The size of the GO sheet was between 500 nm and 1 μm. The selected area electron diffractions (SAED) show clearly the crystalline structure of GO as shown in Figure 1(a). The GO surface was further investigated by an atomic force microscopy (AFM, Veeco D3100, USA). The surface roughness was ~1 nm as shown in the line scans, which was probably originated from the folds or wrinkles at the GO flake edge as identified in Figure 1(b). Raman spectroscopy in Figure 1(c) (top) revealed the D band at 1345 cm^{-1} and the G band at 1587 cm^{-1}, while the X-ray photoelectron spectroscopy (XPS) showed the typical GO peaks at 288.30 eV for C=O, 286.50 eV for C-O bond, and 284.40 eV for C-C bond as shown in Figure 1(c) (bottom) [12, 15].

3.2. Characterization of the rGO-Capacitor. Figure 2 shows the cross-sectional TEM image of the device. The layer-by-layer assembly of 5 nm Au NPs and the 1 nm thick rGO film on the SiO_2 (10 nm) layer was clearly shown. The rGO film was uniformly covered on the substrate due to the electrostatic interaction between the positively charged APTES surface and the negatively charged GO during the dip-coating process. The Raman spectrum of rGO shows higher G band peak at 1591 cm^{-1}, and the XPS spectrum reveals lower C-O bond peak at 268.13 eV than those of GO (the inset of Figure 2) [12, 14].

As the first step for the behavior characterization of the active layer, we examined the semiconducting property of the rGO film, which was constructed as a charge injection layer in the rGO-capacitor. The capacitance-voltage characteristics of the rGO-capacitor device were measured at 1 MHz frequency under various voltage sweep ranges. The rGO-capacitor without the incorporation of Au NPs resulted in a near-zero hysteretic C-V curve as shown in Figure 3(a) with ±5 V bias. In the C-V curve, the depletion area was sharply decreased from accumulation area to inversion area [16]. It implies that the interface between the rGO and the APTES layer on the SiO_2 surface has low contents of traps and mobile ions, which accelerated the charging phenomena. Such a sharp depletion curve in the C-V could not be obtained with a device fabricated with other organic semiconducting materials such as pentacene [22]. This discrepancy may come from fast movement of holes or electrons in the graphene.

The memory effect of Au NPs in the rGO-capacitor was examined from the hysteresis of capacitance-voltage (Figure 3(b)). Voltage bias ranged from ±1 V to ±7 V and the voltage sweep range was between -1.5 V and 1.5 V at 1 MHz. The increase of the voltage sweeping range from ±1 V to ±7 V augmented the flat-band voltage shift (ΔV_{FB}). The ΔV_{FB} of ±1 V sweep range was measured as 0.03 V, while the ΔV_{FB} was 0.38 V for ±7 V sweep range. Particularly, the hysteresis loops were measured in a counterclockwise direction. These characteristics would come from a mechanism that electrons were injected and charged efficiently through the thin oxide in the depletion region of p-type Si [16, 22]. As the sweep range increased to ±7 V, the ΔV_{FB} was shifted to negative or positive directions depending on the forward or backward sweep direction. These results indicate that the charge transport from the p-type Si and the top electrode through the rGO was efficient with a slim discrepancy [16, 17, 21].

Figure 4(a) shows the breakdown voltage (I_d-V_d) of the rGO-capacitor, which was observed at -7.51 V and 7.62 V. Thus, we have measured the C-V characteristic of the rGO-capacitor in the range of ±7 V. Figure 4(b) shows the capacitive charge retention characteristics of the rGO-memory device. The measurement was started by biasing -7 V for 10 s. Then, the C-V measurements were executed

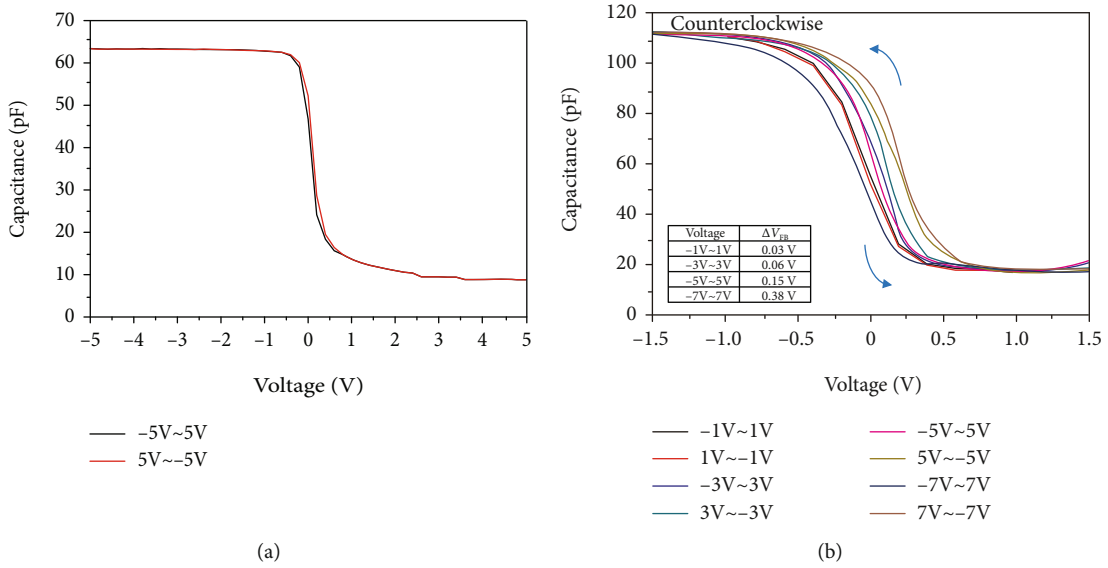

Figure 3: (a) The C-V performance of the rGO device without Au NP incorporation at ±5 V bias. (b) Counterclockwise C-V characteristics of the rGO-capacitor. Voltage bias was from ±1 V to ±7 V, and the voltage range was between -1.5 V and 1.5 V.

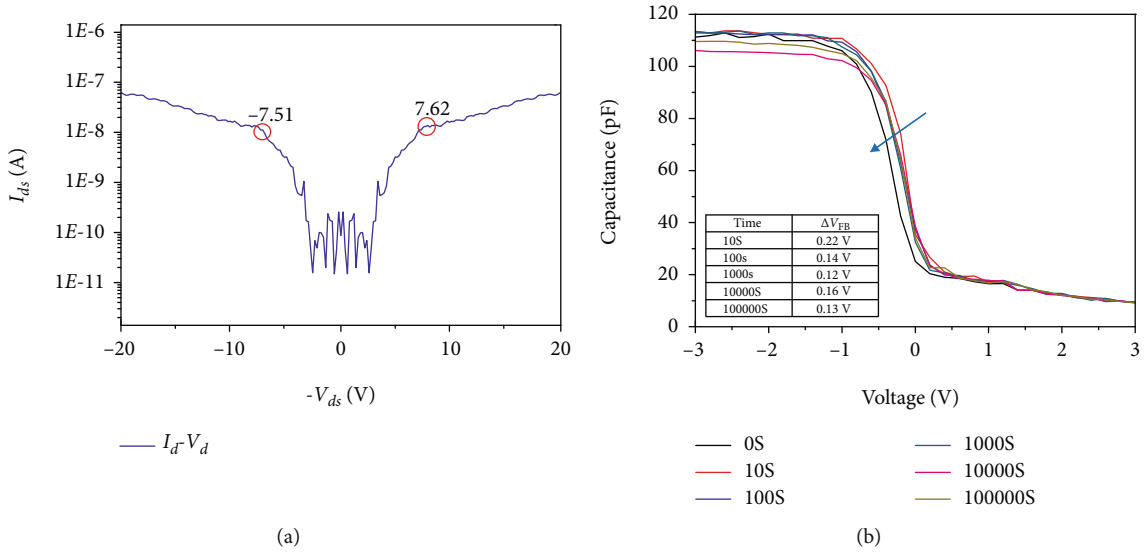

Figure 4: (a) Breakdown voltage test of the rGO-capacitor. The voltage range was from -7.51 V to 7.62 V. (b) Retention measurement of the rGO-capacitor from 10 s to 100,000 s shows almost unconverted performances.

sequentially after 0 s, 10 s, 100 s, 1,000 s, 10,000 s, and 100,000 s after the bias. The C-V curve shifted from the initial charging of Au NPs was consistent even after 100,000 s, which could not be obtained with pentacene in the organic memory device [21]. Therefore, the stored charge with the rGO could be retained for fairly long time. The ΔV_{FB} could be compared as a function of retention time. At 10 s, the ΔV_{FB} was shown as 0.22 V. However, as the retention time has passed to 100 s, 1,000 s, 10,000 s, and 100,000 s, the ΔV_{FB} was converged as 0.14 V, 0.12 V, 0.16 V, and 0.13 V, respectively. The average ΔV_{FB} value after 100 s was calculated around 0.1375 V.

3.3. Characterization of the rGO-TFT. Next, we examined the semiconducting property of the rGO active layer and a switch effect of rGO-TFT. The output (I_d-V_d) and the transfer (I_d-V_g) characteristics of the rGO-TFT were shown in Figures 5(a) and 5(b). The rGO-TFT device without Au NP embodiment shows a linear current behavior. The linear region of the I_d-V_g curve can be derived from the equation of $(dI_d/dV_g) = (W/L)_* \mu_* C_{o*} V_d$. The C_o is the capacitance per unit area that is given by $C_o = \varepsilon_* \varepsilon_o / t$, where ε (the dielectric constant for SiO_2), ε_o (the electric constant), and the t (the thickness of the SiO_2 dielectric layer) are 3.9,

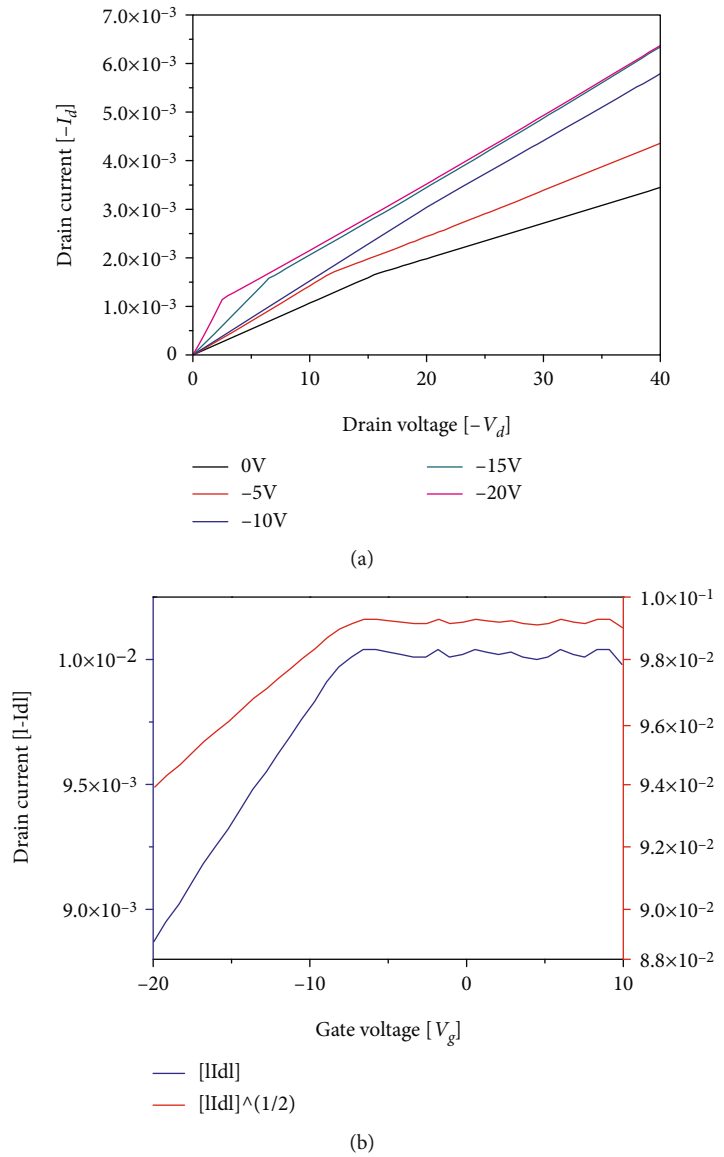

Figure 5: (a) Output (I_d-V_d) characteristics of the rGO-TFT. (b) Transfer (I_d-V_g) characteristics of the rGO-TFT.

8.854×10^{-12} F m^{-1}, and 300 nm, respectively [26]. From these values, C_o was obtained as 11.5 nF/cm^2 and $V_d = -20$ V. Thus, hole mobility was determined as $\mu_h = 22.887$ cm^2/V·s after program bias. Interestingly, the rGO-TFT has shown the p-channel instead of n-channel characteristics [8, 9, 14, 17, 18]. In addition, the hole mobility in Figure 5(b) was higher than the mobility (3.5 cm^2/V·s) of single-layered rGO-TFT [8]. Main reason for the high mobility was believed that a moderate temperature (200°C) of H_2N_4 reduction was efficient for the active layer reduction instead of high reduction temperature (1000°C) with H_2 along with solution-phased H_2N_4 reduction of GO [8].

3.4. Characterization of the rGO-MTFT. Finally, we demonstrated the memory effect and switch characteristics of rGO-MTFT. Figure 6(a) shows the I_d-V_d relationship of the rGO-MTFT, and Figure 6(b) displays the I_d-V_g graph of the rGO-MTFT with +40 V program and -40 V erase bias. The first threshold voltage (ΔV_{th}) shifts approximately 7.84 V between the initial and the program bias. The program and reprogram biases did not produce significant differences in the output characteristics (Figure 6(b)). The window memory of ΔV_{th} between the program and reprogram was measured as 5.74 V. From these results, the hole mobility of $\mu_h = 22.887$ cm^2/V·s was measured with the rGO-MTFT, which was counter-intuitive to have an enhanced mobility with the Au NPs embedding compared to rGO-TFT's mobility as shown in Figure 5(a) [19]. It has been reported that the enhanced mobility or reduced resistivity of single-layered graphene could be attainable with iron oxide NP (~14 nm) physisorption due to a drastic shift of Dirac point of graphene [19].

Moreover, such a high mobility in the rGO-MTFT indicates that the carrier trapping in the rGO channel was minimized, and the charging phenomena were taken placed solely on the Au NPs [17, 18].

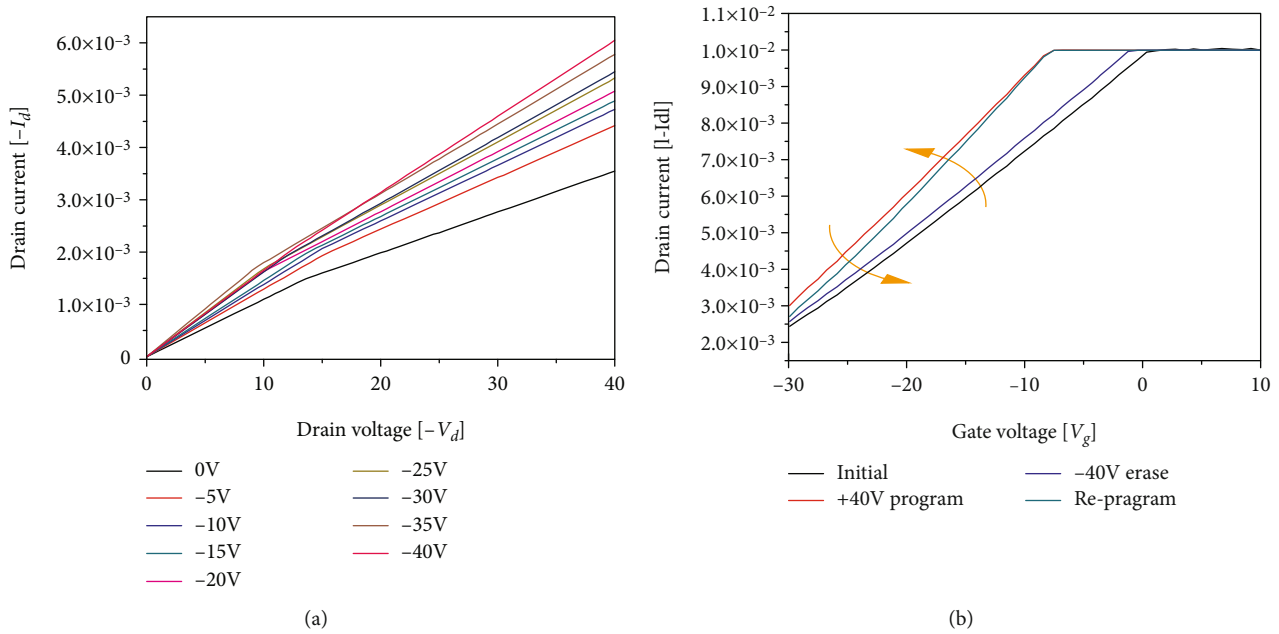

FIGURE 6: (a) Output (I_d-V_d) characteristics of the rGO-MTFT. (b) Transfer (I_{dl}-V_g) characteristics of the rGO-MTFT with +40 V program or reprogram bias and -40 V erase bias.

4. Conclusion

In this study, we fabricated and characterized the nonvolatile memory performances of the rGO-capacitor, the rGO-TFT, and the rGO-MTFT. Au NPs were adopted as charging elements in nonvolatile memory devices in the structure of MGIS. Even though the multiple rGO nanosheets were patterned on a substantially large channel area, no adverse effect derived from discontinuity in the rGO film was detected. While memory effect of the rGO-capacitor was small, the retention characteristics were consistent. The hole mobility of the rGO-TFT was $\mu_h = 16.479\,\text{cm}^2/\text{V}\cdot\text{s}$ with a p-channel property. The rGO-MTFT shows $\mu_h = 22.887\,\text{cm}^2/\text{V}\cdot\text{s}$ with a threshold voltage (ΔV_{th}) shift approximately 7.84 V with the program/erase biases. This is the highest mobility in the reduced graphene oxide- (rGO-) based TFTs embedded with Au NPs. The Au NPs served as efficient charge storage elements in the MTFT. Program and reprogram biases did not produce significant differences in the output performance. The window memory of the threshold voltage shift was 5.74 V. These results can contribute to the development of an entirely organic or plastic electronics used for fast memory devices or biosensor applications.

Data Availability

All data included in this study are available upon request by contact with the corresponding author.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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