Hindawi
Journal of Nanomaterials
Volume 2022, Article ID 1370919, 9 pages
https://doi.org/10.1155/2022/1370919

Research Article

Forming-Free Pt/Ti/AlO_x/CeO_x/Pt Multilayer Memristors with Multistate and Synaptic Characteristics

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Received 10 December 2021; Revised 20 August 2022; Accepted 8 September 2022; Published 5 October 2022

Academic Editor: Shijun Liao

Due to their unique electrical performance and simple structure, memristors exhibit excellent application prospects for future information technology. In this work, we fabricated Pt/Ti/AlO_x/CeO_x/Pt memristors demonstrating electroforming-free bipolar resistive switching behavior with low operating voltage (−1 to 1 V), stable endurance, and retention. Space-charge limited conduction (SCLC) as well as the formation and rupture of conductive filaments are responsible for the resistive switching behavior. Increasing the magnitude of the RESET voltage could generate multistate resistive switching. We studied the synaptic characteristics of the device by obtaining multilevel conductance states and investigating the relationship between the device resistance, pulse amplitude, pulse width, and pulse number. By applying programmed pre and postsynaptic spiking pulses, spike-timing dependent plasticity was observed. This study shows that the device is suitable for multivalue storage and can be used as an electronic synapse device in artificial neural networks.

1. Introduction

The rapid development of complementary metal-oxide-semiconductor (CMOS) integrated circuit technology has brought the information age [1]. However, the emergence of memory walls has limited its further development [2–4]. In addition, artificial neural networks (ANNs) and large-scale calculations have brought significant challenges to current computing hardware [5–7]. The two-terminal structure and unique electrical characteristics of memristors have been widely studied [3, 8, 9]. The resistance of a memristor can be modulated by applying voltage or electron flux through it, where it will remain after electrical stimulation is stopped [8, 10–12]. Furthermore, the resistance of a memristor can be incrementally modulated by voltage pulses, offering significant potential for multilevel data storage [13–15]. Moreover, these multilevel conductances can also be used to simulate the weights of ANN, which has also been considered an ideal device for hardware neural networks (HNNs) [14, 16–18].

The resistance switching mechanism of the memristor primarily includes metal ion migration, oxygen vacancy migration [19], and charge effects [18, 20–25]. In the oxygen vacancy migration mechanism, the multilayer memristor generally exhibits better performance than the single-layer memristor due to the more controllable formation/breakage of conductive filaments (CF) between the electrodes [26]. CeO_x is a promising multilevel switching material because it can generate and modulate oxygen vacancies by changing the valence states of Ce cations (Ce^{3+} and Ce^{4+}) under different applied electric fields [27–31]. Therefore, the resistance of the CeO_x layer can be modulated by applied voltages.

Recently, some studies have reported on the characteristics of cerium oxide-based memristors and their related

multilayer film structures. Kim et al. reported on $Pt/CeO_2/Pt$ devices with artificial synaptic characteristics, which exhibit polarity-dependent analog memristive switching [32]. Hsieh et al. reported on HfO_x/CeO_x bilayer memristors, which have forming-free, low-voltage, and analog characteristics [33]. In addition, Muhammad et al. demonstrated multilevel bipolar resistive switching characteristics in $Ni/CeO_{2-x}/ITO/$ glass devices by controlling RESET voltage and current compliance [34]. However, the realization of both multivalue storage and use as an electronic synapse device based on the pulse voltage (less than 1 V in amplitude) of the CeO_x multilayer film device has not been reported. We observed that by rationally designing the device structure of multiple layers, memristors could exhibit better and more diverse performance [27, 28, 33, 35]. Compared to these studies [27–34], our study designed a $Pt/Ti/AlO_x/CeO_x/Pt$ multilayer structure memristor that has a low working voltage and good working properties such as multivalued characteristics, neuroplasticity, and learning mechanism simulation. In this work, all characteristics of the $Pt/Ti/AlO_x/CeO_x/Pt$ multilayer memristor were studied.

The innovation in this work consisted of the design of a ceria-based multilayer memristor device structure, which provided regulation and improvement to the performance of a single-layer ceria memristor. Compared to previous ceria-based memristors, the memristor designed in the present study exhibits a variety of multistate, synaptic and forming-free performance characteristics under a small operating voltage. This improves the usability and practicality of the ceria-based memristors. This multilayer memristor design method, based on a single functional layer, provides an ideal approach for the expansion and improvement of memristor performance.

This device has forming-free and multivalued characteristics by DC voltage sweep. Furthermore, the $Pt/Ti/AlO_x/CeO_x/Pt$ device can also modulate the resistance based on the input pulse amplitude and emulate the STDP learning rule with good repeatability. The storage device based on $Pt/Ti/AlO_x/CeO_x/Pt$ has the potential to be used for adaptive calculations in neuromorphic systems. Furthermore, we systematically explained the multivalue and synaptic characteristics of the device and reveal the relationship between the electrical performance and the conduction mechanism.

2. Materials and Methods

A JGP560C15 ultrahigh vacuum magnetron sputtering coating system was used to manufacture the device along chamber pressure below $5 \times 10 - 5$ Pa. A CeO_x layer (~50 nm) was deposited onto the $Pt/Ti/SiO_2/Si$ substrates by radio frequency (RF) magnetron sputtering, and Ar and O_2 at a rate of 1 : 2 were used as the working gases. The chamber pressure was maintained at 2.5 Pa with an RF power value of 60 W. Then, an AlO_x layer (~50 nm) was deposited onto the $CeO_x/Pt/Ti/SiO_2/Si$ substrate with high-purity Ar. The working pressure was maintained at 2.5 Pa with an RF power value of 60 W. Additionally, a Ti layer (~20 nm) was deposited onto the $AlO_x/CeO_x/Pt/Ti/SiO_2/Si$ substrates by sputtering the high purity Ti target (99.99%) in high-purity Ar. The chamber pressure was maintained at 1 Pa with an RF power value of 60 W. Finally, the Pt top electrode with a diameter of ~400 μm was deposited using a shadow mask. X-ray photoelectron spectroscopy (XPS, ESCALAB 250Xi) was used to analyze the composition of the multilayer structure, and the current-voltage (I-V) characterizations of the $Pt/Ti/AlO_x/CeO_x/Pt$ devices were measured by a Keithley 4200 semiconductor parameter analyzer.

3. Results and Discussion

Figure 1(a) depicts the structure of the device consisting of the Ti insert layer, AlO_x/CeO_x switching layer, and Pt electrodes. We applied voltage to the top Pt electrode while the bottom Pt electrode was grounded. Figure 1(b) shows the Ce 3d levels of the CeO_x film, where the red line corresponds to the Ce^{4+} ions with peaks at 882 eV (v), 888.5 eV (v2), 897.9 eV (v3), 900.5 eV (u), 907 eV (u2), and 916.3 eV (u3). The blue line corresponds to the Ce^{3+} ions with peaks at 883.7 eV (v1) and 902.1 eV (u1). Symbol u and v represent the $3d_{5/2}$ and $3d_{3/2}$ spin-orbit components, respectively, [36]. This shows that Ce^{3+} and Ce^{4+} coexist in the CeO_x film, and the device contains some oxygen vacancies in the CeO_x film layer. The deconvoluted O 1 s in CeO_x is shown in Figure S3. These peaks are related to the oxygen vacancies, lattice oxygen, and surface oxygen species.

Figure 1(c) shows the I–V curve of the $Pt/Ti/AlO_x/CeO_x/Pt$ device under direct current (DC) sweeping at room temperature, where no forming process was needed. The sweeping rate was 0.24 V/s; the sweeping step was 0.01 V, and the voltage-time curve of the DC sweep is shown in Figure S2 (a). The pristine device was in a high resistance state (HRS). Then, a positive sweep voltage was applied to the device with current compliance (I_{cc}) of 8 mA to prevent a dielectric breakdown. When the voltage reached 0.6 V, the current of the device suddenly increased to I_{cc}, and the device changed into the low resistance state (LRS), which is denoted as the SET process. The device remained in LRS when the sweep voltage decreased from 1 V to 0 V. When the voltage bias was swept from 0 V to −1 V, the cell transformed from LRS to HRS, and this process is called RESET. Then, a negative sweep voltage of $-1\,V \rightarrow 0\,V$ was applied again, and the device remained in HRS. Resistive switching where the SET and RESET processes occur at opposite polarities and is considered as bipolar switching behavior. Figure 1(d) shows the retention characteristics of HRS and LRS measured at room temperature. The 0.01 V read voltage was applied every 1 s, and the resistance values of LRS and HRS were observed as stable over 2000 s. The DC I–V curve of the $Pt/Ti/AlO_x/CeO_x/Pt$ device in 100 consecutive cycles is shown in Figure S1(a). The distribution of SET and RESET voltages of the $Pt/Ti/AlO_x/CeO_x/Pt$ device is shown in Figure S1(b), and the mean and standard deviation for Vset and Vreset are shown in Figure S1(c). The cell to cell variation is shown in Figure S1(d). The device has a small operating voltage, as well as forming-free and retention characteristics, which can contribute to the decreased complexity of the peripheral circuit design.

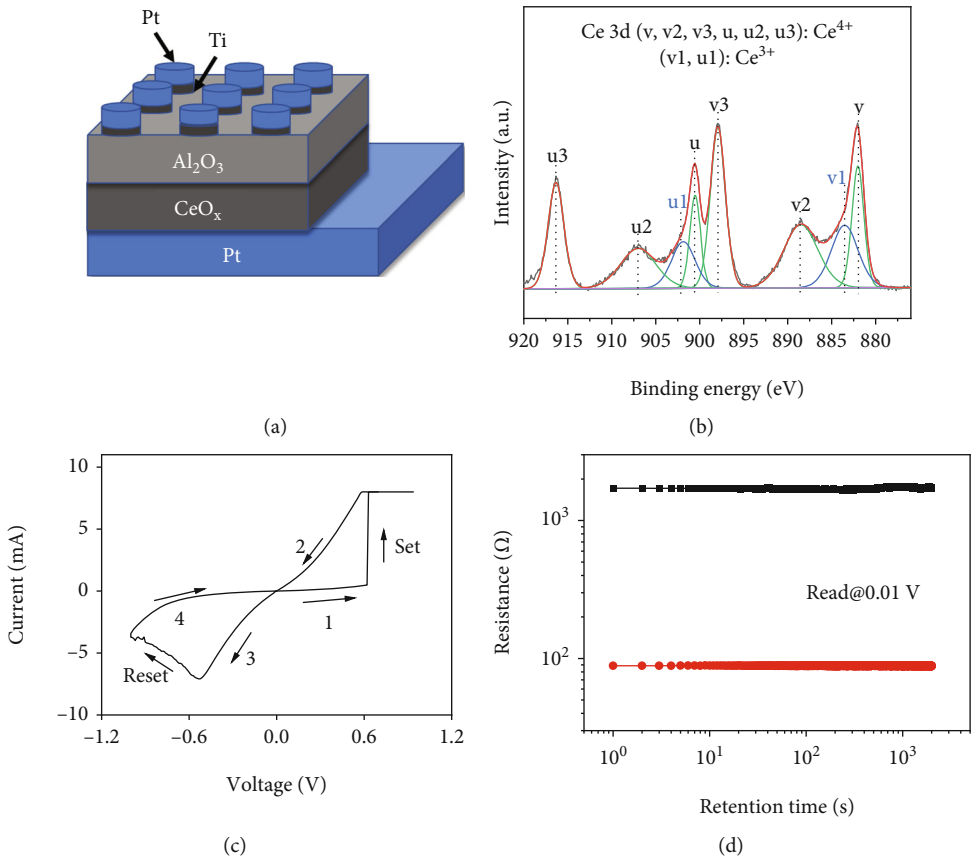

FIGURE 1: (a) Schematic of the Pt/Ti/AlO_x/CeO_x/Pt device. (b) Ce 3d levels of CeO_x film. (c)Typical bipolar I–V curve of the Pt/Ti/AlO_x/CeO_x/Pt device. (d) The retention test of the Pt/Ti/AlO_x/CeO_x/Pt device with a 0.01 V read voltage.

To understand the conduction and switching mechanisms of the Pt/Ti/AlO_x/CeO_x/Pt device, the ln(|V|)–ln(|I|) characteristic curve was studied, and the fitted curves of the positive and negative sweep region are shown in Figure 2(a) and Figure 2(b). In LRS, we observed that Ohmic conductance best fit the curve in both the positive and negative bias voltage regions, which is usually observed in the conductive filament model. In HRS, the two fitted slopes suggest that the carrier transport mechanism in the HRS followed space-charge limited conduction (SCLC) model [30, 37–42]. SCLC has three different regions, the Ohmic region (I∝V), the modified Child's law region (I ∝ V^2), and the trap-filled-limit (TFL) region ($I \propto V^n$, $n > 2$) in a high electric field. The Child's law region can be described by [43]

$$I = \left(\varepsilon\mu 0 N c e^{-E/KT}/N_t d^3\right) V^2, \quad (1)$$

where ε is the dielectric constant; μ_0 is the carrier mobility; N_c is the density of states in the valence band; E is the effective trapping potential; k is the Boltzmann's constant; T is the temperature; N_t is the number of traps, and d is the effective film thickness.

According to the curve fitting and XPS analysis results, we determined the conduction and resistance switching mechanisms of the device. As shown in Figure 2(c), at first, the sweep voltage was small, and most of the electrons injected into the resistive switching layer were thermally generated electrons. The fitted slope was approximately 1.29. This I-V curve region corresponded to $I \propto V$. As the positive voltage increased, the unfilled trap center was gradually occupied by electrons, and the slope of the fitted plot increased to 1.93 which corresponded to the $I \propto V^2$ region. When the applied voltage was sufficiently high, and most of the traps were completely occupied by electrons, the slope of the fitted plot increased to 2.83 which corresponded to the $I \propto V^n$ region. The fitting mechanism data (Ohmic and SCLC) are shown in Figure S4 (a–d) and Figure S5 (a–d).

When a sufficient internal electric field was generated, oxygen vacancy CFs were formed. Afterward, the resistance of the device abruptly switched from HRS to LRS. Due to the oxygen vacancy, CF has small resistance; the I-V curve region corresponded to $I \propto V$. When a negative voltage was applied to the top Pt electrode, the CFs gradually broke, leading to the resistance switching from LRS to HRS. The HRS in the negative sweep region (from −1 V to 0 V) where the slope decreased from 3.66 to 1.66, and finally to 1.11, also followed SCLC model. In summary, the resistance switching of the device results from SCLC and the oxygen vacancy CFs mechanism. Because some oxygen vacancies formed after the device was fabricated, the device does not require the forming process.

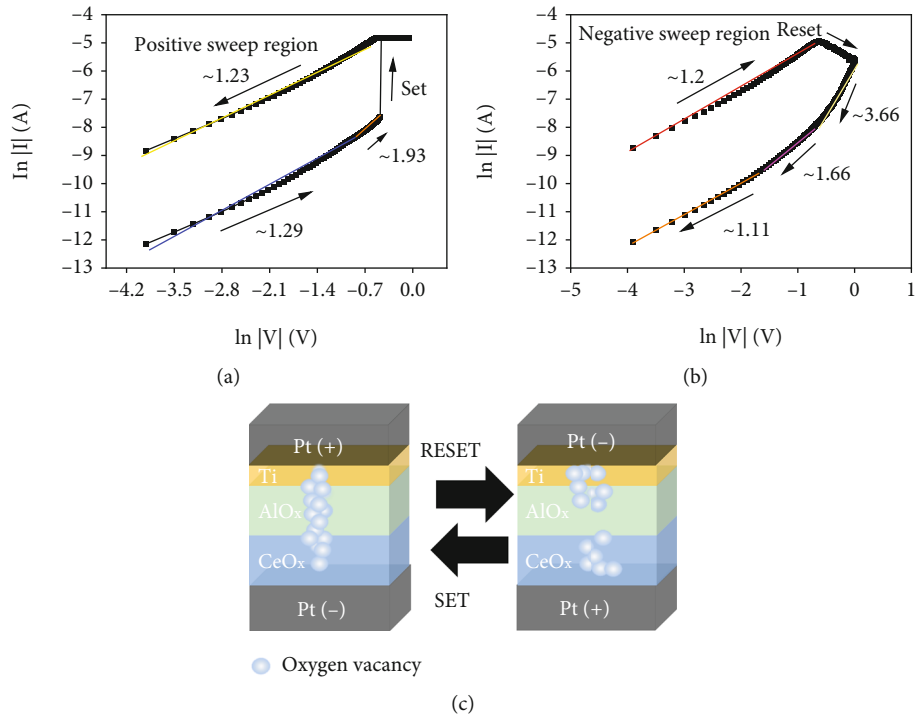

Figure 2: The ln(|V|)–ln(|I|) characteristic curves for the Pt/Ti/AlO_x/CeO_x/Pt device under (a) positive bias voltage and (b) negative bias voltage. (c) The speculative conduction and resistance switching mechanisms of the device.

Next, we studied the multilevel resistive switching on another Pt/Ti/AlO_x/CeO_x/Pt device. As Figure 3(a) shows the different RESET stop voltages (−0.6 V, −0.7 V, −0.8 V, −0.9 V, and −1 V) to achieve a five-level HRS. The reading voltage was 0.01 V, and the resistance was 94 Ω, 434 Ω, 865 Ω, 1357 Ω, and 2102 Ω, respectively. The controllability of the resistance during the reset process is found to be appropriate for multivalue storage. Figure 3(b) shows the resistance uniformity of the 5 resistance states in the 70 continuous cycles. Figure 3(c) shows the data retention performance of the Pt/Ti/AlO_x/CeO_x/Pt multilayer memristor with a 0.01 V read voltage. Moreover, this device can obtain different R_LRS by controlling different compliance currents. Figure S6 shows different Vreset limitations to control R_HRS and different compliance currents to control R_LRS.

The five-level HRS corresponds to the partial rupture of the multifilaments with increasing negative voltage in the multilayer film. As larger negative voltages were applied to the device, more filaments were ruptured and the device showed higher resistance states. A similar physical model was explained by Kim et al. [32]. This device is promising for high-density storage memory applications due to its reliable multilevel data storage ability.

Subsequently, we studied the synaptic weight modification of the device which is similar to biological synapses. As shown in Figure 4(a), at first, the resistance of the device was set to about 1000 Ω. Then, 11 pulses of 50 ms with the amplitudes of voltage consecutively increasing from 0.45 to 0.55 V with a step of 0.01 V were applied. With these positive voltage pulses, the resistance gradually decreased. 8 pulses of 50 ms with the amplitudes of voltage consecutively decreasing from −0.6 to −0.75 V with a step of 0.025 V were applied, and the resistance gradually increased. A read voltage of 0.01 V was used to measure its resistance state after each pulse voltage. The conductance can be adjusted repeatedly by applying pulse cycles composed of pulses with different amplitudes. The applied pulse cycle is shown in Figure S2(b). As shown in Figure 4(b), within the cycles of 500 pulses, the continuously adjustable conductance of the device shows good stability.

Furthermore, the relationships between device resistance modulation, pulse amplitude, pulse width, and pulse number were studied. As shown in Figures 5(a–d), the greater the amplitude and width of the pulse is, the greater modulation of device resistance is in both the depression and potentiation parts. However, when continuous pulses were applied to the device, the resistance of the device gradually decreased or increased, and finally reached a limit, where the greater the amplitude and width of the pulse is, the greater the limit is. Hence, each method for the modulation of device conductance has its corresponding limit. After reaching this limit, its conductive state will remain stable, which is similar to the phenomenon of biological synaptic saturation, and further research is needed [44].

For biological synapses, the most important rule will be STDP [45–49]. Generally, STDP indicates that if the prespike precedes the postspike ($\Delta t > 0$); then, long-term potentiation (LTP) will occur, and synaptic weight (w) will increase [14]. If the prespike follows the postspike ($\Delta t > 0$), long-term depression (LTD) will happen and the synaptic

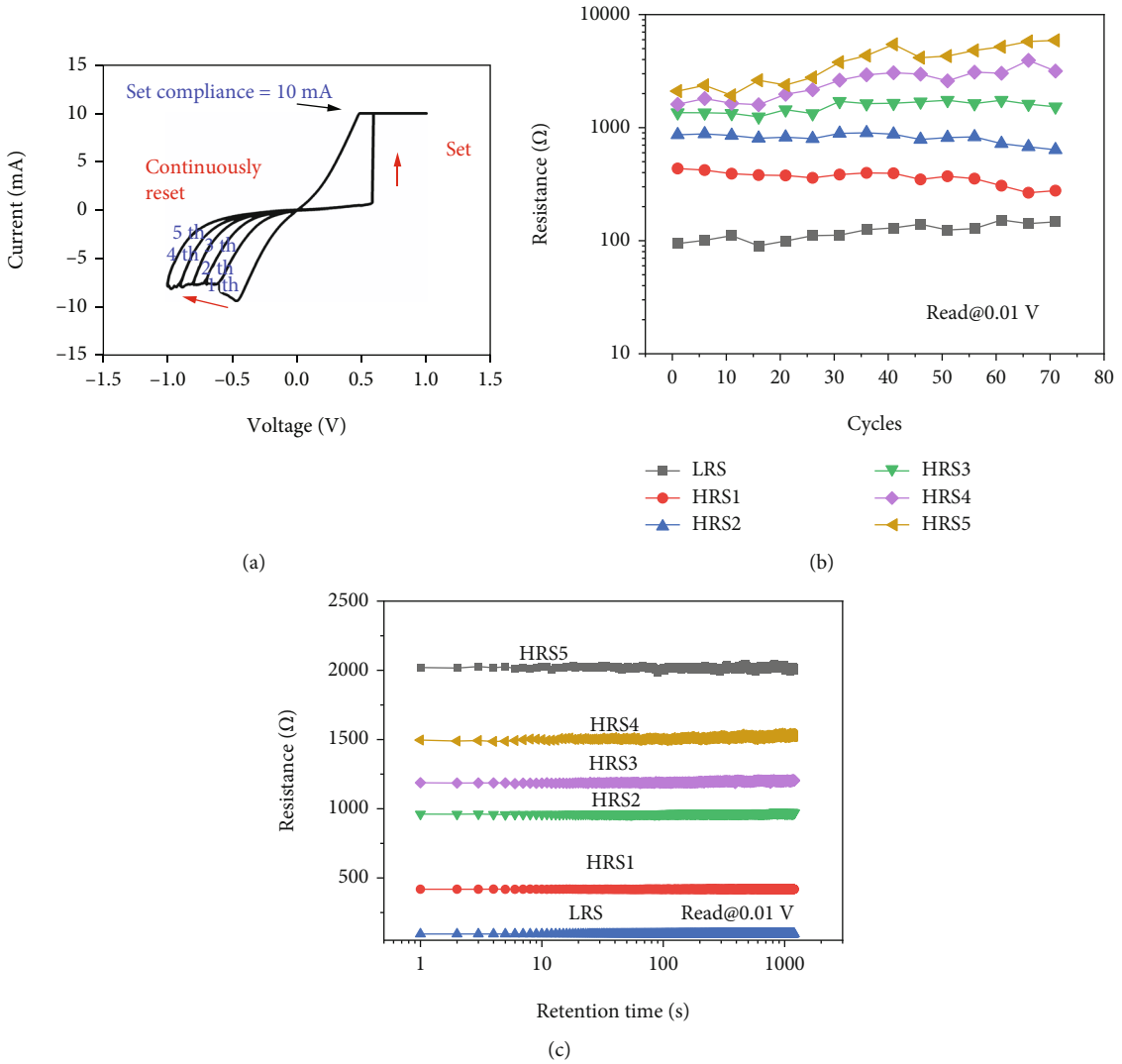

Figure 3: (a) I-V curves of the Pt/Ti/AlO_x/CeO_x/Pt multilayer memristor measured by DC double sweeping. Different RESET stop voltages (−0.5 V, −0.6 V, −0.7 V, −0.8 V, −0.9 V, and −1 V) were used to achieve five-level resistive switching. (b) Cycles test of the Pt/Ti/AlO_x/CeO_x/Pt multilayer device in different RESET stop voltages. (c) Time retention characteristics of different resistance states.

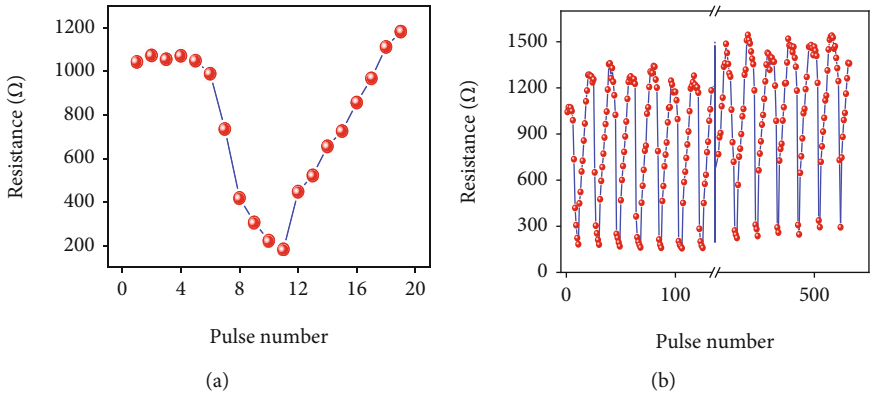

Figure 4: (a) Resistance evolution of the Pt/Ti/AlO_x/CeO_x/Pt multilayer device for a pulse cycle, where pulse width was 50 ms. (b) Resistance evolution of the Pt/Ti/AlO_x/CeO_x/Pt multilayer device over 500 pulse cycles.

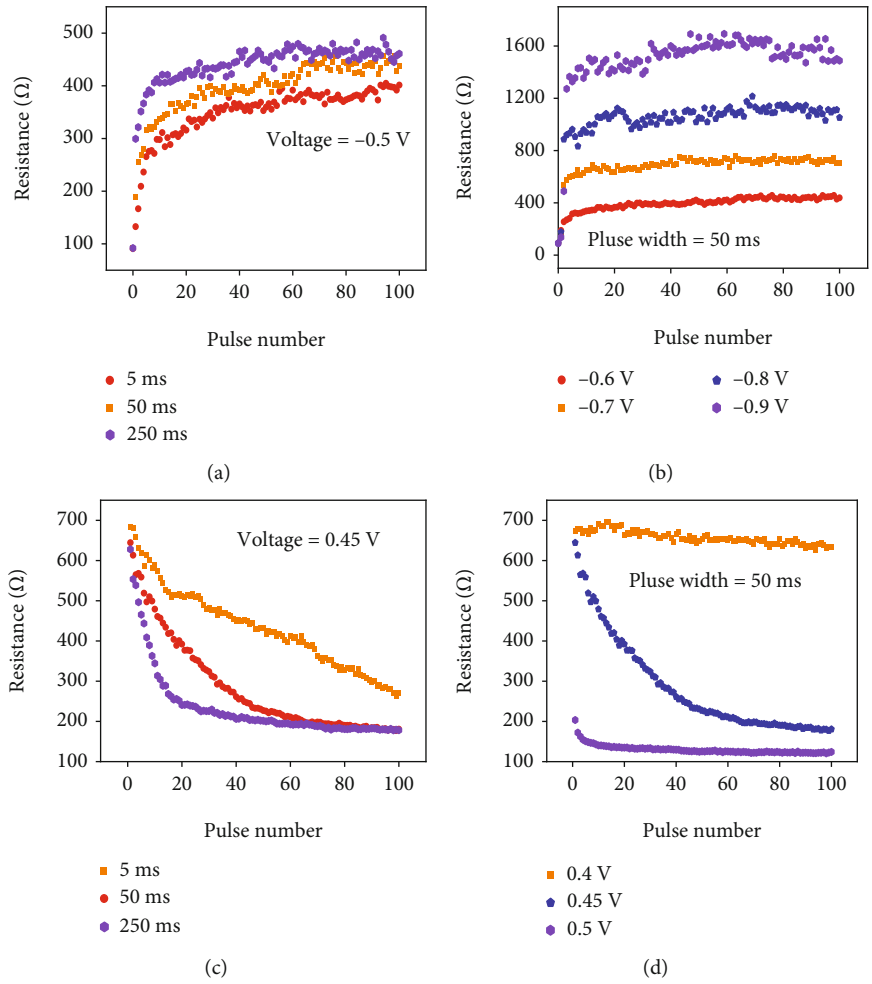

Figure 5: (a) Device resistance modulation by applying 100 voltage pulses. (−0.6 V) with different pulse widths (5 ms, 50 ms, and 250 ms). (b) Device resistance modulation by applying 100 voltage pulses (50 ms) with various amplitudes (−0.6 V, −0.7 V, −0.8 V, and−0.9 V). (c) Device resistance modulation by applying 100 voltage pulses (0.45 V) with different pulse widths (5 ms, 50 ms, and 250 ms). (d) Device resistance modulation by applying 100 voltage pulses (50 ms) with various amplitudes (0.4 V, 0.45 V, and 0.5 V).

weight (w) will decrease. At the same time, the smaller $|\Delta t|$ and the greater $|\Delta w|$, where Δw can be defined as $(G_{after} - G_{before})/G_{before}$, and the range of Δw follows $(0, +\infty)$ and $(-1, 0)$.

As shown in Figure 6(a), the waveform was designed to generate the STDP phenomenon and is composed of continuous single pulses. The negative pulse occupied the first time slot, and then the positive pulse with reduced amplitude followed in the subsequent time slot. When the prespike and postspike overlapped, a programming pulse could be generated with an amplitude sufficient to modulate the resistance. The voltage dropped on the device is defined as the prespike voltage minus the postspike voltage. As the spike timing was tighter, the negative pulse would overlap the positive pulse with a larger amplitude, resulting in a larger resistance modulation. If the prespike preceded the postspike, a positive programming pulse (left in the Figure 6(a)) would be generated. Otherwise, a negative programming pulse would be generated (right in the Figure 6(a)). As shown in Figure 6(b), we simulated this STDP learning rule with this device. At $\Delta t > 0$ and $\Delta w > 0$, LTP occurred; while for $\Delta t < 0$ and $\Delta w < 0$, LTD occurred, and the spike timing was tighter, resulting in a larger resistance modulation. The experimental learning data for the STDP rule was well fitted to the exponential function, and fitting parameters are shown in Figure 6(b).

$$\Delta W = A exp(-\Delta t/\tau) + \Delta w0, \tag{2}$$

where ΔW is the change in synaptic weights; A is the scaling factor, and τ is the time constant. The characteristics of adjustable conductance, synaptic saturation, and simulating the STDP learning rules indicate that storage devices based on Pt/Ti/AlO_x/CeO_x/Pt have the potential to be used for adaptive calculations in neuromorphic systems.

In addition, the endurance and robustness of the Pt/Ti/AlO_x/CeO_x/Pt device need to be further optimized for commercial applications of multivalued and synaptic

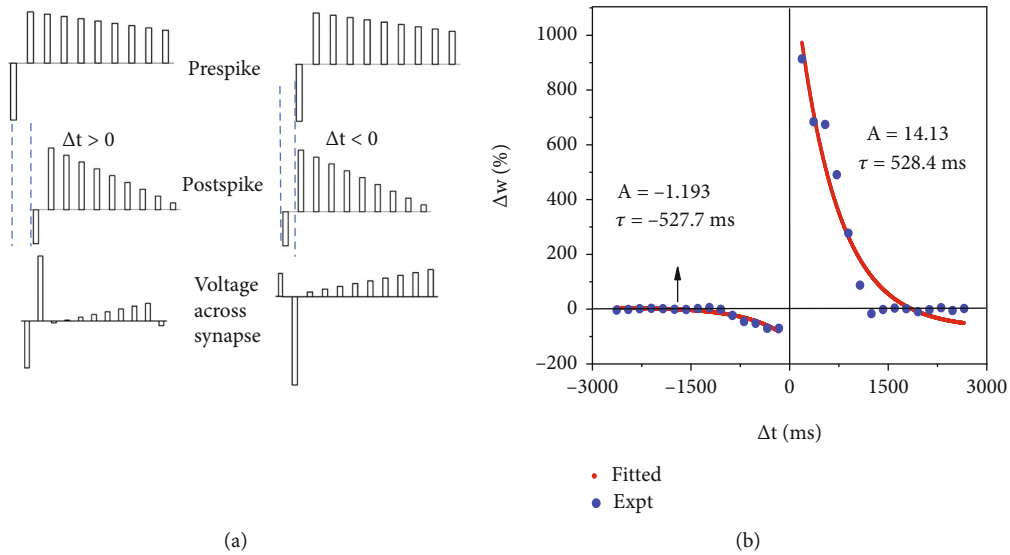

Figure 6: (a) STDP realization schemes by pulse amplitude modulation. The pulse amplitudes for the prespike are −0.5, 0.45, 0.43, 0.41, 0.39, 0.37, 0.35, 0.33, 0.31, and 0.29 V, consecutively, and for the postspike, they are −0.25, 0.45, 0.4, 0.35, 0.3, 0.25, 0.2, 0.15, 0.1, and 0.05 V, consecutively. The width of each pulse is 50 ms. The interval between two pulses is 150 ms. (b) Implementation of STDP learning by the Pt/Ti/AlO_x/CeO_x/Pt memristor.

characteristics, according to Mario Lanza et al. [50]. In further experiments, we plan to insert a layer with good endurance performance or dope in the switching layer to effectively improve the tolerance of the device.

4. Conclusions

In this work, we fabricated a multilayer structure of Pt/Ti/AlO_x/CeO_x/Pt device. The SCLC and oxygen vacancy CFs mechanisms were used to explain the electrical characteristics of the device. There are several key advantages of this device: (i) this device is forming-free and has cycle-to-cycle as well as device-to-device consistency, which is beneficial to lowering the complexity of the circuit architecture; (ii) this device has nonvolatile and recyclable multivalued characteristics, which could address the major concern in the memory industry; (iii) this device has synaptic properties such as adjustable conductance, synaptic saturation, and simulating STDP learning rules, which has immense potential in artificial neuromorphic computing. All of these unique electrical performances suggest that the device has the potential to avoid the von Neumann bottleneck and shows great potential in both the emerging neuromorphic computation system and multivalue storage applications.

Data Availability

The data that support the findings of this study are available within the article and its supplementary material.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

This work was supported by Open Fund of Key Laboratory of New Processing Technology for Nonferrous Metal & Materials, Guangxi Key Laboratory of Optical and Electronic Materials and Devices, Guilin University of Technology (19AA-1).

Supplementary Materials

Figure S1 shows the endurance characteristic, the distribution of SET and RESET voltage, the standard deviation and mean for Vset and Vreset and cell to cell variation of the Pt/Ti/AlO_x/CeO_x/Pt device. Figure S2. shows the voltage-time curve of DC sweep and the pulse cycle curve of figure 4(a). Figure S3. shows the deconvolution of the O 1 s spectrum of CeO_x. Figure S4. shows the double logarithmic I-V characteristics of Pt/Ti/AlOx/CeOx/Pt device in positive bias. Figure S5. shows the double logarithmic I-V characteristics of Pt/Ti/AlOx/CeOx/Pt device in negative bias. Figure S6. shows the I-V sweep cruve of different Vreset limitations to control R_HRS and different compliance currents to control R_LRS, respectively. *(Supplementary Materials)*

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