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Research Article

Adiabatic CMOS-Based Electrostatic MEMS Actuation for Reduced Dynamic Power and Switching Activity

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The basic purpose of MEMS actuation is to miniaturize the actuators and sensors for applications in nanoelectronics. The transistor switching current and power supply noises due to voltage drops across the metal lines can impair circuit timing and performance, posing a continuing problem for high-performance chip designers. This work presents an empirical concept of a reconfigurable charge pump based on FPGA for electrostatic actuation of the Microelectromechanical System (MEMS). The goal of the design is to produce enough on-chip voltages for actuating the MEMS that are continuously adaptive and reconfigurable. In this proposed method, pumping capacitors lying in the range of 1-pF have been deployed to decrease the area of design concerned. The various voltages are programmable digitally and created by dynamically altering the number of phases as well as the clock drive levels. The dynamic model is designed by adjusting the number of stages to produce on-chip voltages including clock drive speeds, assuming a purely capacitive load. The proposed model's power consumption can be lowered in the steady state by lowering its clock frequency and electrostatic MEMS actuators with capacitive load. An average of 0.62 W is dissipated by the circuit when the eight stages are triggered. Consequently, with adiabatic and without adiabatic architecture, 0.0186 mW of minimum power difference is obtained.

1. Introduction

In recent years, new adiabatic MEMS actuation paradigms have contributed to an exponential growth in microelectronics. The most important obstacle in designing high performance microelectronic systems is the dissipation of energy. CMOS technology is one of the most prominent technologies in the field of computer chip design and is extensively used today in numerous and varied applications to construct integrated circuits. Due to several main benefits, today's computer memories, CPUs, and cellular phones make use of this technology. Both *P* channel and *N* channel semiconductor devices make use of this technology. Similarly, it is proposed to design low-power circuits employing dynamic logic families, but after each test period, the circuit must be precharged [1, 2]. As an alternate, [3] suggested energy recovery circuits called adiabatic circuits to design electronic circuits. But change in voltage levels is sufficiently slow in adiabatic circuits in which no heat loss or gain occurs. A node's charge and discharge are rendered sufficiently slow to make it equal to a current source's charge/discharge. To accomplish the purpose, the power clocks are used in place of DC power supply as implemented in traditional circuits [4].

MEMS technology or Microelectromechanical Systems can be described at its most basic context as electromechanical devices and structures as scaled up elements manufactured through micromanufacturing techniques. MEMS devices can vary in critical physical properties from less than one micron dimension to many millimeters. A key criterion of MEMS is that, whether or not these elements can move, there are at the minimum some elements which have mechanical functionality. In various parts of the world, the definition used to describe MEMS varies. They are primarily called MEMS in the United States, although they are called "Microsystems Technology" or "micromachined machines" in some other parts of the globe.

This paper provides a comprehensive investigation of the actions of the suggested adiabatic electrostatic MEM actuation. As a result of the previous research, MEMS have a higher temperature drift, which can be a problem for those without temperature compensation or heating capabilities. The current design has one of the lowest supply voltages, as well as a low voltage gain per step [i.e., (V/V)/stage] while prior works use either more steps or a higher supply voltage than the current design, which results in an accumulation of voltage from an 8-stage 1.2 V supply. Since the circuit is not connected to any recycling equipment, energy cannot be recycled. The voltage phase size will not be consistently tuned. Hence, the proposed work recycles energy in a more efficient way with lower supply voltage. This facilitates the implementation of energy efficient gates in the design of reversible logic circuits.

2. Dynamic Power and Switching Activity

Dynamic, sometimes referred to as switching power and static, and sometimes referred to as leakage power, are two forms of power consumed in a system. Leakage power has been the dominant power user in geometries smaller than 90 nm, while switching is the greater contributor for larger geometries. As shown in Figure 1, it is possible to use power reduction techniques to minimize both kinds of power. Total power, as shown in Figure 2, is a feature of the process of voltage, switching, capacitance, and transistor arrangement itself. Because switching activity and clock frequency influence output voltage, lowering capacitance and supply voltage can reduce dynamic power dissipation.

3. Background

The recent developments of M/NEMS logic devices based on resonator [5] are reviewed, experimental works in that area are explored, and logic circuits are designed based on cascadability and frequency tuning of these digital logic circuits. An empirical model of the Stepwise Adiabatic Circuits (SAC) for energy consumption was proposed [6, 7] when discharge of the load capacitor is required. Another application for low-power was proposed ([8] which mathematically modeled an Adiabatic DCVSL. In terms of dissipation of power, the Adiabatic-DCVSL circuit performs better and could be modified suit low power implementation layout.

In the standard CMOS of 0.13 μm technology, an 8-stage reconfigurable charge pump was developed for Microelectromechanical system (MEMS) electrostatic actuation and also manufactured from a 1.2 V supply. The circuit achieves a calculated max *o*/*p* voltage of about 10 V [9]. The maximum output ripple for a 10 pF load is 1.1 V, meaning that MEMS electrostatic actuation can handle a 0.31% relative deviation. The circuit is made of CMOS technology with a 0.8 m high voltage and a 675 m X1100 m area [10]. The regulatory algorithm devised by [11] improves the power efficiency of a switched-capacitor DC-DC converter by automatically changing the voltage gain and switching frequency in response to input voltage and load current. The converter will produce a balanced 1.2 V output rail with an input of 0.5 V to 2.5 V and deliver a load capacity of 100A, according to simulation results. Most MEMS (Microelectromechanical Systems) actuators [12] need high control voltage, such as 20 V.

In [13], one of the major reasons for implementing MEMS on Si CMOS is that the control voltage approaches the knee voltage of the PN-junction diode. This work proposed an adiabatic charge pump, by adding sufficient bias voltages to both the back gate as well as deep-N-well of N-MOSFETs, and can produce greater output voltage than that of the breakdown voltage. Results reveal that perhaps the prototype can produce a 21 V DC voltage at 0.18 μm Si CMOS to 11 V but 15 V PN-junction breakdown voltage. MEMS have a higher temperature drift, which can be a problem for those without temperature compensation or heating capabilities. Prior works either used more steps or a greater supply voltage than the current design, which resulted in an accumulation of voltage from an 8-stage 1.2 V supply. Energy cannot be recycled since the circuit is not connected to any recycling equipment. The size of the voltage phase will not be consistent. As a result, with reduced supply voltage, the suggested work recycles energy more efficiently.

4. Nonadiabatic Electrostatic MEMS Actuation Using Charge Pump

The current system consists of different blocks and their functionalities in Figure 3. To regulate the clock at each point, a 4-to-8 thermometer decoder is incorporated to circuit in this block diagram, allowing the no/- of active clocks to be dynamically vary by changing the input signals, CTRL*i*. The actual circuit block diagram in Figure 3 is made up of a digital control circuit, a charge pump with its clock, and a discharge point.

The proposed work is aimed at achieving higher output voltage for the given supply voltage and moreover at also providing dynamic configurability of such a voltage, in contrast to traditional charge pumps. The charge pump circuit is designed specifically to dynamically configure a switched capacitor array through switches, which are conceptually seen from Figure 3. For each point, the capacitive array consists of 8 pairs of pumping capacitor, C_1 and C_2.This is of greater significance if MEMSs that need many different actuation voltages concurrently need to be used on a multitude

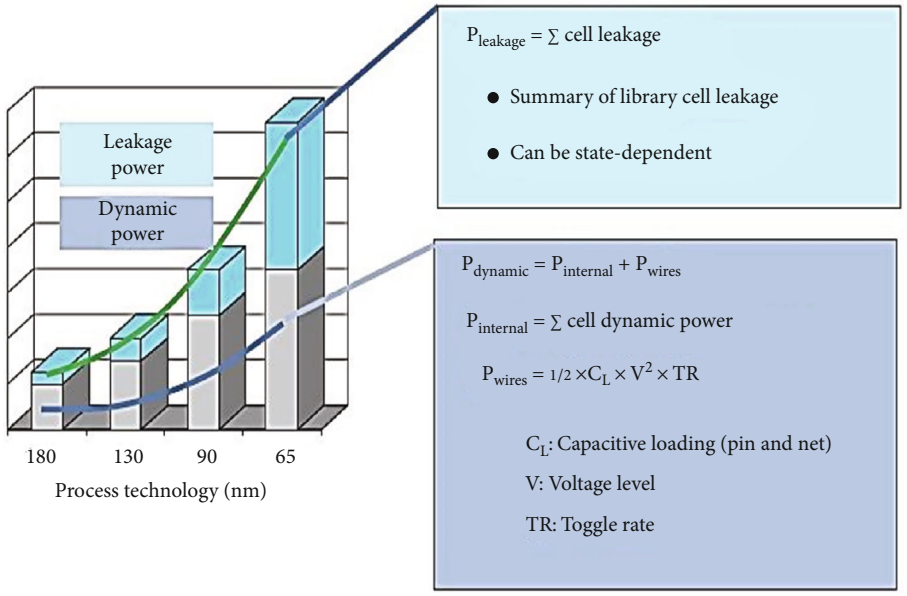

Figure 1: Leakage power and dynamic power.

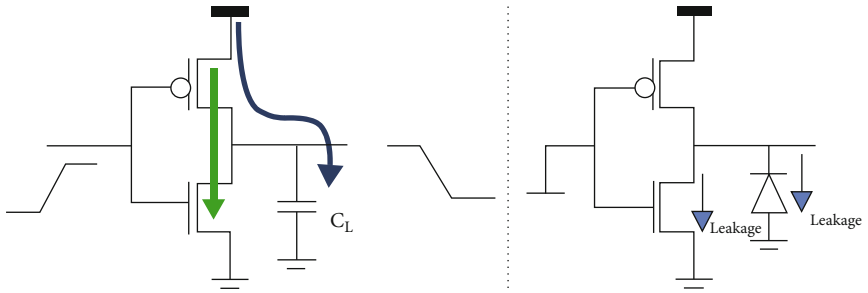

Figure 2: Power dissipation during charging and discharging.

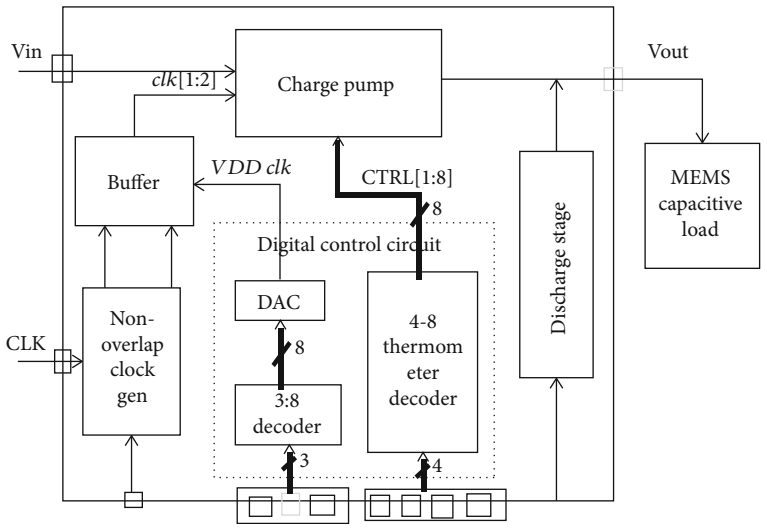

Figure 3: Charge pump-based electrostatic MEMS actuation.

of charge pumps. The top plate of pumping capacitor is connected to the *i*/*p* and *o*/*p* terminals via switches, and bottom plate connecting to a pair of CLK1·CTRL*i*and CLK2·CTRL*i* regulated nonoverlapping clock signals and CTRL*i*are control signals to activate each level.

A 4×8 decoder is incorporated into capacitor charge pump circuit. The capacitor charge pump works in all eight stages when CTRL1 to CTRL8 is high. For example, by making CTRL8 small, the number of points can be minimized to seven.

The stage is turned off, resulting in a charging pump with seven stages. In the same way, the number of stages is reduced: each stage is turned off one by one by lowering the CTRL*i* control signals, as shown in Table 1. The proposed design utilizes control parameters and 9-bit programming word as seen from Figure 4.

An adiabatic controller attached to MEMS overcomes the big downside of charge pump controller dependent MEMS actuation. Implementing an adiabatic controller in the proposed device would not only activate the MEMS for a short time, but it will also recycle the wasted energy and store it in micro capacitors, enabling a few digital circuits to be activated. The adiabatic theory also helps to minimize power consumption. The system's value is that it makes effective use of power and has small design architecture for such a large idea.

Table 1: Array control scheme for switched capacitor.

Active control signals	Active switches	Output
CTRL	S_1-S_4	$2V_{\text{in}}$
CTRL1–CTRL2	S_1-S_8	$3V_{\text{in}}$
CTRL1–CTRL3	S_1-S_{12}	$4V_{\text{in}}$
CTRL1–CTRL4	S_1-S_{16}	$5V_{\text{in}}$
CTRL1–CTRL5	S_1-S_{20}	$6V_{\text{in}}$
CTRL1–CTRL6	S_1-S_{24}	$7V_{\text{in}}$
CTRL1–CTRL7	S_1-S_{28}	$8V_{\text{in}}$
CTRL1–CTRL8	S_1-S_{32}	$9V_{\text{in}}$

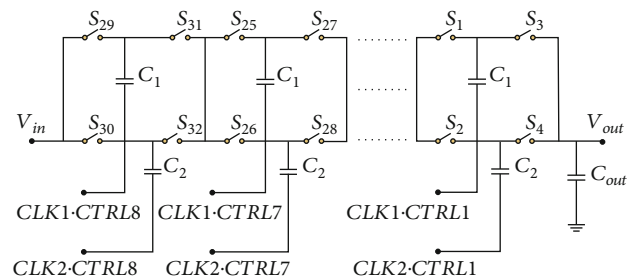

Figure 4: Schematic of reconfigurable switched capacitor array.

5. Adiabatic Controller-Based Electrostatic MEM Actuation

The major two blocks connected with proposed system are as follows:

(i) Adiabatic logic controller

(ii) Low power blocks

These two blocks are important in our project for recycling the circuit's dissipated power. Since it does not dissipate electricity, adiabatic activity offers significant reductions in power consumption. Unlike traditional logic switching, where only the input signals with different final logic states change, adiabatic circuits require all input signals to undergo a controlled transition in the form of a ramp [14]. Logic switching cannot be instantaneous in order to minimize energy dissipation; instead, it must be incremental.

Two main blocks have been included in the proposed block diagram, 4as shown in Figure 5, the adiabatic controller and the low power blocks that are related to the MEMS capacitive load. The buffer is used to provide enough drive power to transfer signals or data bits to the next level. Nonoverlapping clock generation is used to prevent signal overlapping between circuits. DAC, 3:8 decoder, and 4-8 thermometer decoders make up the optical based control circuit. As illustrated in Figure 5, a DAC, Digital to Analog Converter, is a system that converts digital data into an analogue signal. The output of a thermometer decoder is similar to that of a thermometer.

The architecture includes replicated output thermometer code to boost basic converter specifications. The signal of the thermometer decoder and buffer is provided to the charge pump, but these three signals control all of the signals from its outer circuit. The charge pump was used in the circuit raise voltage, and the discharge stage is coupled to the capacitive load. The small pumping stages are allowed by this stage. As compared to other related families, it used a special logic called Positive Feedback Adiabatic Logic employed in the adiabatic controller because it consumes minimum energy and a strong robustness to technical dynamic characteristics. The PFAL gate is depicted in general in Figure 6. 8:1 multiplexer controls the low-power blocks that feed the MEMS capacitive load.

In this design, a Multiplexer (MUX) is used as the key element in these low-power blocks, which should be operated by a 1.2 V supply. The adiabatic controller's recycled energy is being used to drive another circuit, in which the energy is only useful for digital circuits. Low-power blocks perform these functions. As a result, get two types of recycled clock signals; CLK1 and CLK2 are obtained, based on the capacitance value, during charging and discharging. These dual clocks, start mux and start clk, are provided as inputs to another circuit. The capacitor has begun to charge after the start mux has been activated, and waste energy recycling has begun. As a result, this process will continue until the heat has dissipated. The dissipated energy can be recycled using adiabatic logic, and then, this energy could be used to drive another circuit. For storing thousands of capacitance values, the proposed device used digital MEM capacitance. Since there are so many reconfigurable pumping stages involved, the pace of operation is

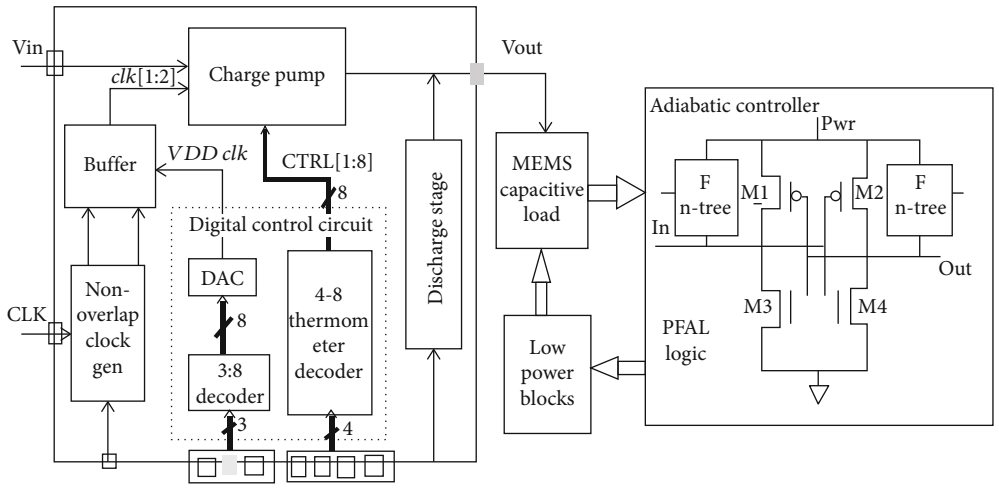

Figure 5: Block diagram of the proposed system.

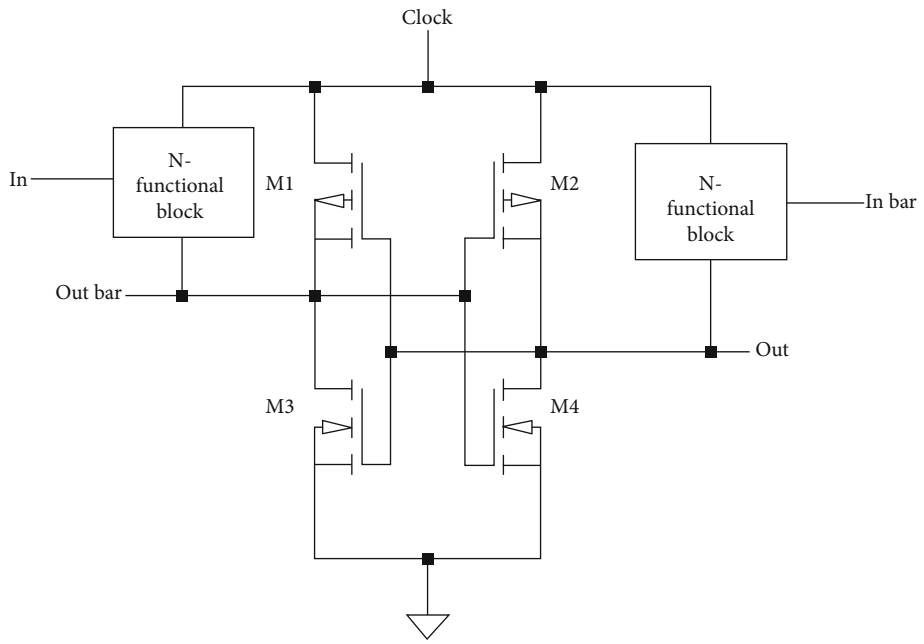

Figure 6: Schematic of PFAL gate.

increased. The use of a regulated clock frequency has decreased power consumption.

6. Results and Discussion

The complete system was created in a CPLD environment and then analysed with a DSO. Because the clock inverter's driving ability is reduced when the clock voltage is reduced, the rise time is affected. Furthermore, clock levels below 0.4 V significantly decrease output voltage because they are well below inverter's optimum operational threshold. This necessitates a 0.5 V minimum operating voltage for Vdd Clk. At a clock frequency of 40 MHz, the maximum output voltage (Vdd = VddClk = 1.2 V) is developed and the dissipated power observed is 0.62 W. The power consumption of the auxiliary electronics compensates for this scaling.

6.1. Multiplexer Design. As shown in Figure 7, this circuit has 2 blocks (i.e., mux0 and mux1). These circuits have 3 inputs and 2 outputs. In mux0 circuit, the involt input takes 4-bit value and generates output as 8-bit value adcout. This adcout is given as input to the mux1 circuit. Finally, we get the 32 combinations of memout values. Based on the input values, the memout value gets changed.

6.2. Control Signal Design. As shown in below design, the memout taken from the multiplexer design is given as the input to the digital circuit of 4 bits (deign) as shown in Figure 8. The clock and clear signal is given common to both the threshold_

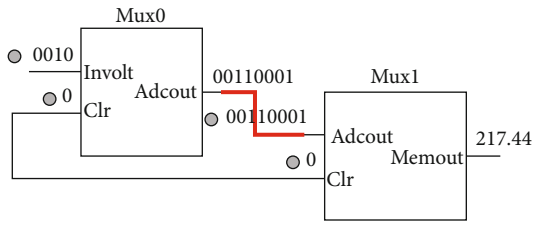

Figure 7: Memout design.

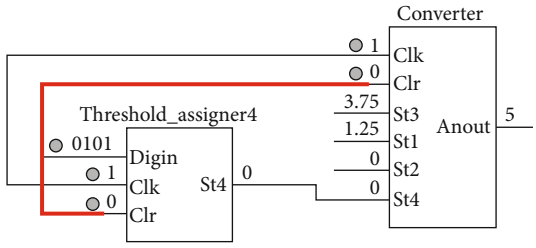

Figure 8: Analog output design.

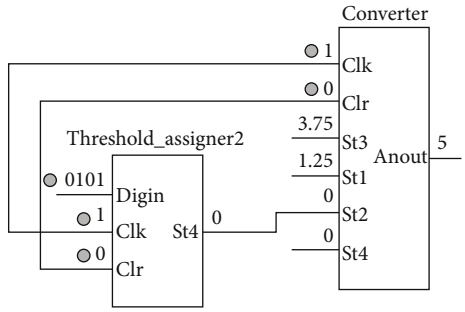

Figure 9: Digital converter design.

assigner4 and converter. Thus, the particular signal has been selected and delivers the anout in the converter.

6.3. DAC Design. In DAC design, the clock and clear input is given common to both the threshold_assigner2 and converter as the same to all the other three designs. The 4-bit digital input is converted into analogous output by using this design as shown in Figure 9.

6.4. Integration Design

(i) From the above three designs such as multiplexer, control signal, and DAC design, these are integrated in a single integration design as shown in Figure 10

(ii) The selected signal is given as common input to all the other four threshold assigners, and the 4-bit input values are given commonly and produce different single bit values

7. Simulation Results

The proposed model generates the range of voltages for an 8-stage 1.2 V supply. Since low supply voltage is beneficial because it lets an improved tuning of MEMS actuator's output voltage by increasing the tuning resolution obtained by adjusting the number of levels. To make up the difference for higher resolution, more bits can be used in VddClk, but balancing the range of drive levels in VddClk with the series of stages allows for well-spread tuning characteristics. The design is 0.0645 mm^2 in size, which is very thin. It is indeed important to note although the reported region encompasses the entire system (i.e., charge pump, control, and clocking).

(i) The calculated output voltage reaches its full value with a 1-pF load, an electrostatic MEMS actuator, and an oscilloscope probe. The discharge transistors' size could be increased to improve release performance

(ii) From the MEMS output as referenced with Figure 11, it is observed that based on the given input the charging and discharging amplitude values varied from one time period to another period

7.1. Control Signal

(i) The stray capacitance and leakage current rise the dynamic power consumption of the circuit, explaining the difference between observed and calculated power consumption as shown in Figure 12

(ii) These control signals are used as a reference signals to the overall circuit, and overlapping of signals can be prevented and controlled

(iii) According to the selection line, the control signal can be varied from one clock to another clock

7.2. DAC. The DAC can be synthesized entirely in an FPGA and does not require the use of external components. Even though power consumption limits the maximum number of bits that can be used and that this DAC is not the most linear one, the FPGA-based DAC may be used in many applications.

(i) Based on the given digital input, DC-DC level signal can be generated

(ii) The required analog output is obtained, where the analogous output value depends upon the given digital input as highlighted in Figure 13

(iii) Improve the resolution of the DAC to provide finer clock drive levels, particularly in the relatively high output voltage scale

7.3. Adiabatic Controller. As shown in Figure 14, a rise time of 80 ns and a fall time of 6.40 s are observed in this state. In an adiabatic controller, the capacitive load has

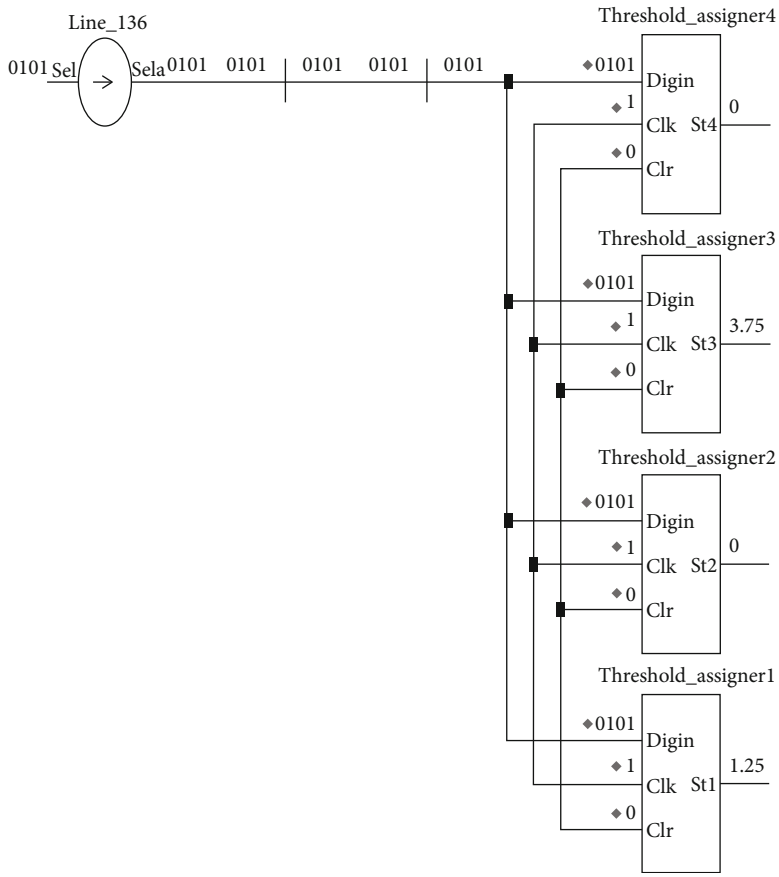

Figure 10: Integration design.

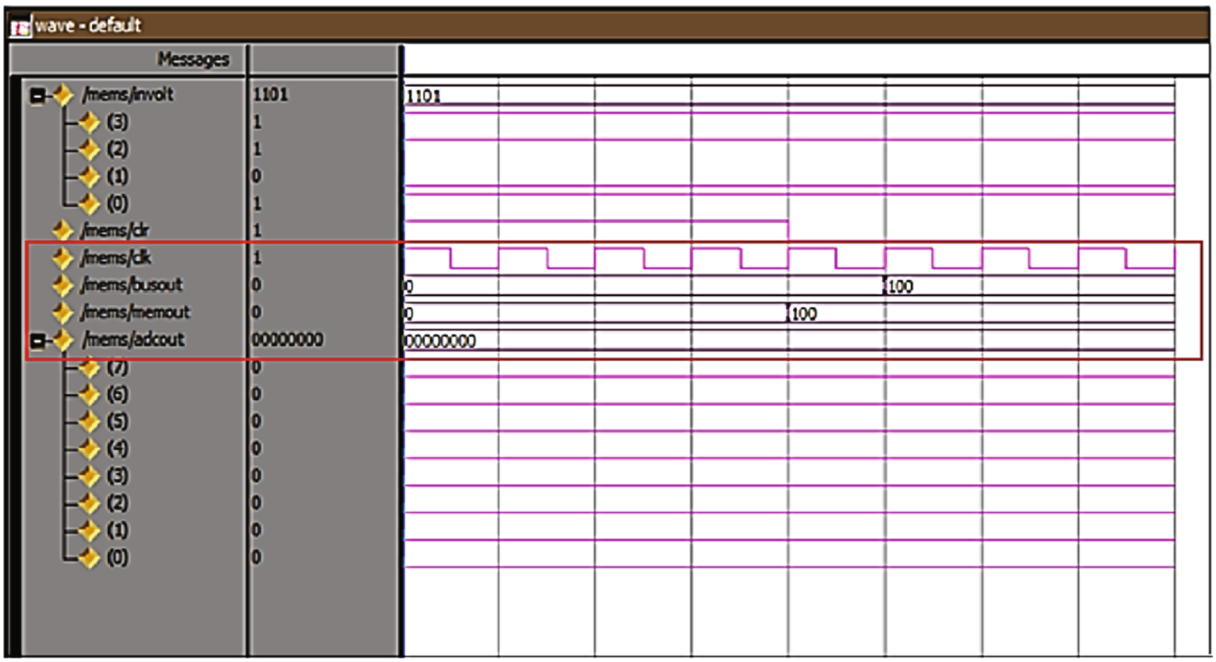

Figure 11: MEMS actuator with 1-pF load.

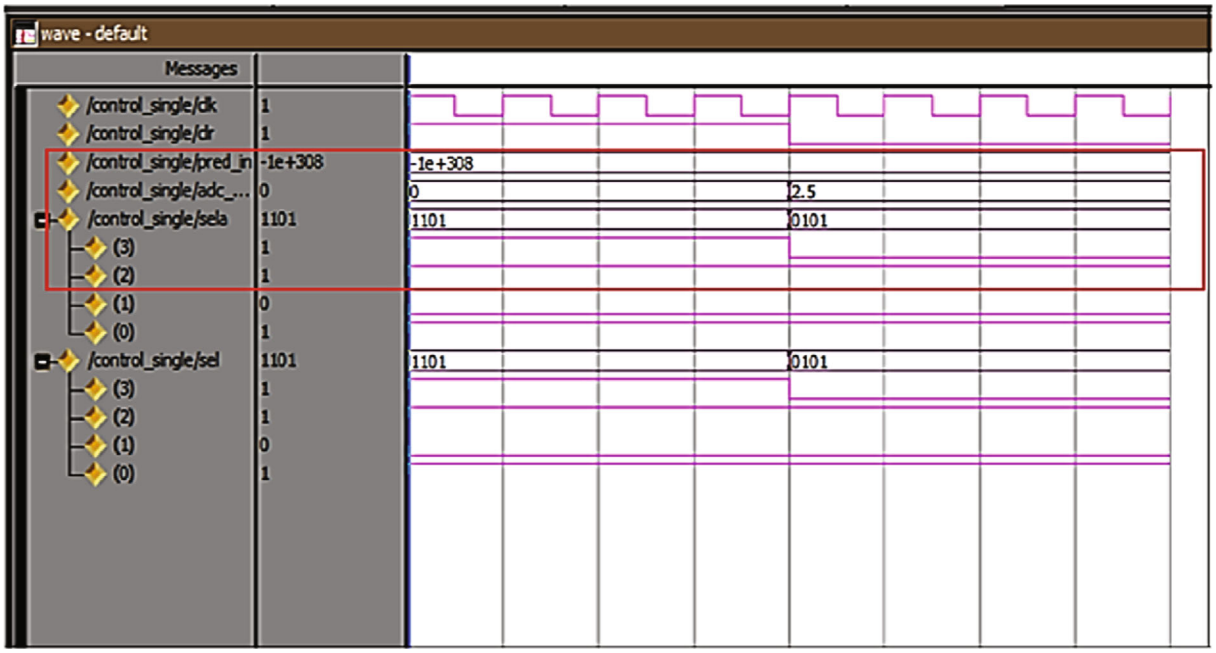

Figure 12: Control signal output.

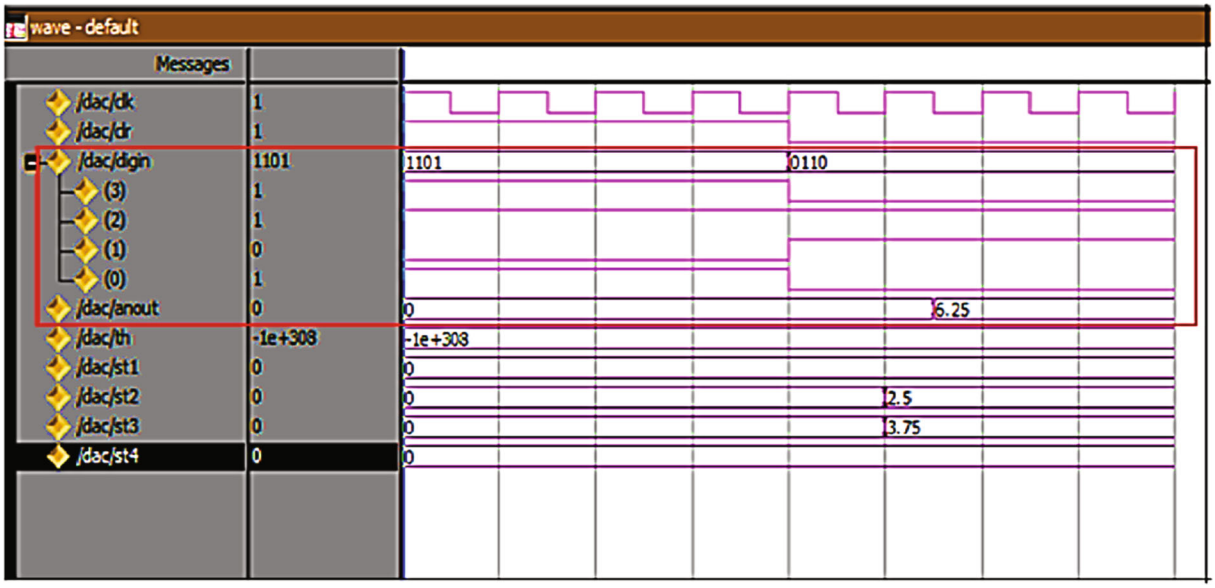

Figure 13: DAC output.

been stored as an energy and it can be recycled by decoder recycled count to enable the circuits, where the circuit does not work while giving 0's as an input and alternatively by giving 1's it works as indicated in Figure 15.

7.4. Integration

(i) By integrating the above three modules, we can get the final output as shown in Figure 16

(ii) During charging and discharging, we get two types of recycled clock signals as CLK1 and CLK2 based on the capacitance value

(iii) These two clocks are given as an input to another circuit (i.e., start_mux and start_clk)

(iv) After enabling the start mux, the capacitor has been started to charge and recycling of wasted energy gets started

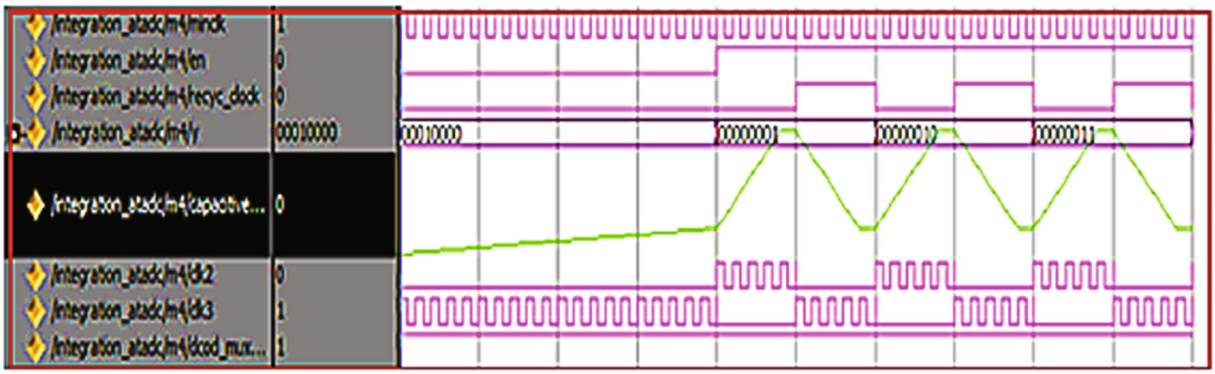

Figure 14: Integration output showing rise time and fall time.

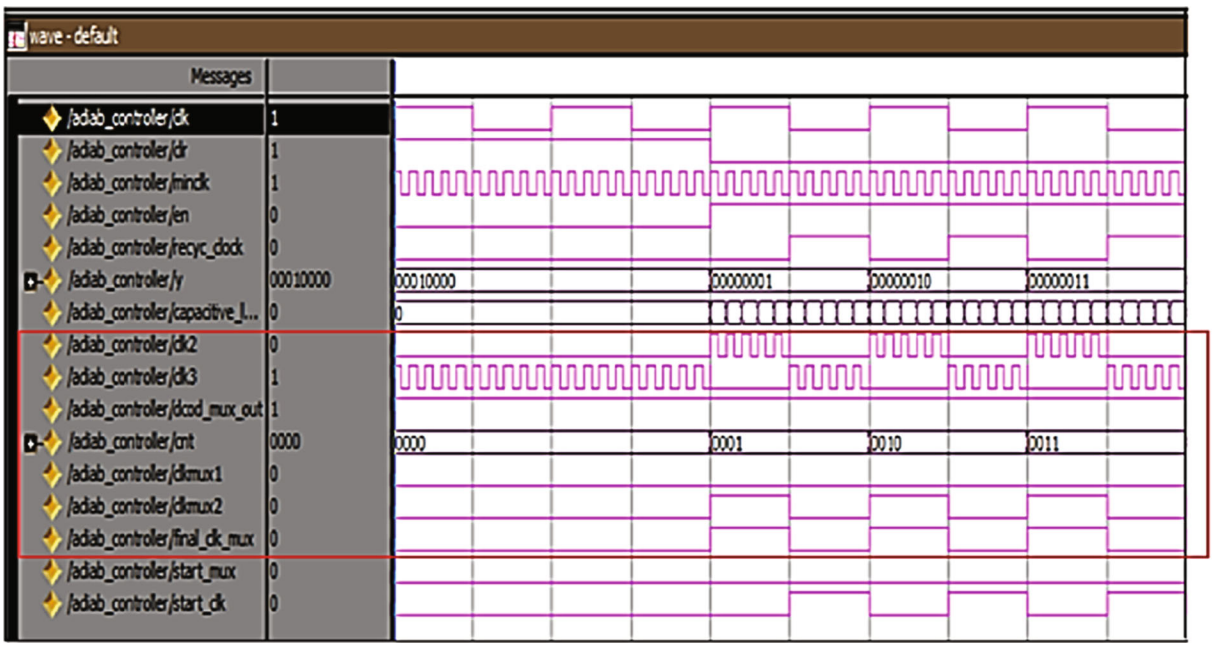

Figure 15: Adiabatic controller output.

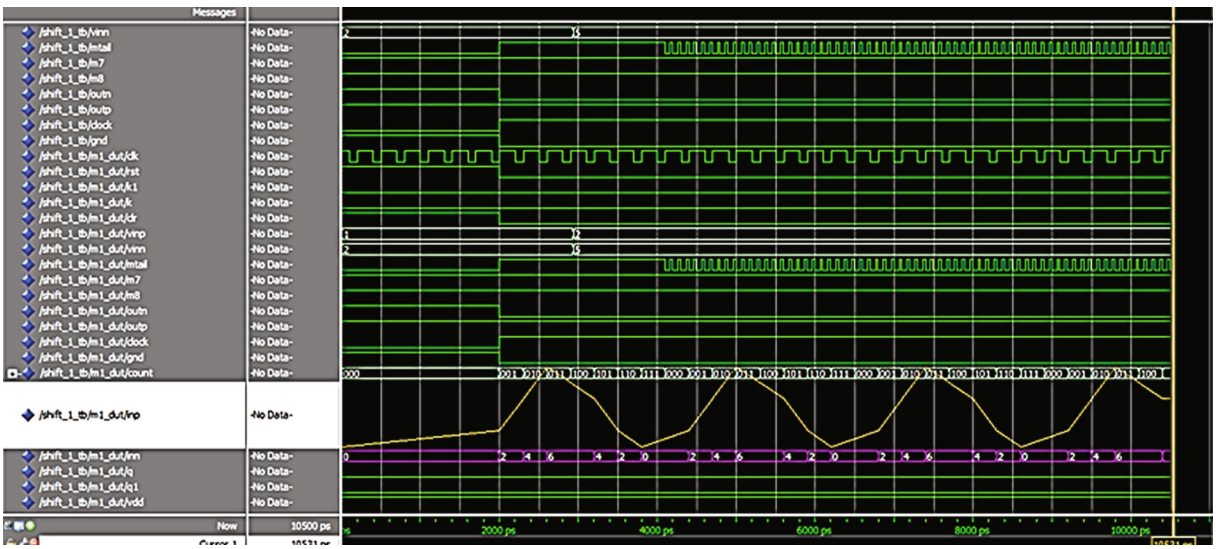

Figure 16: Integration output.

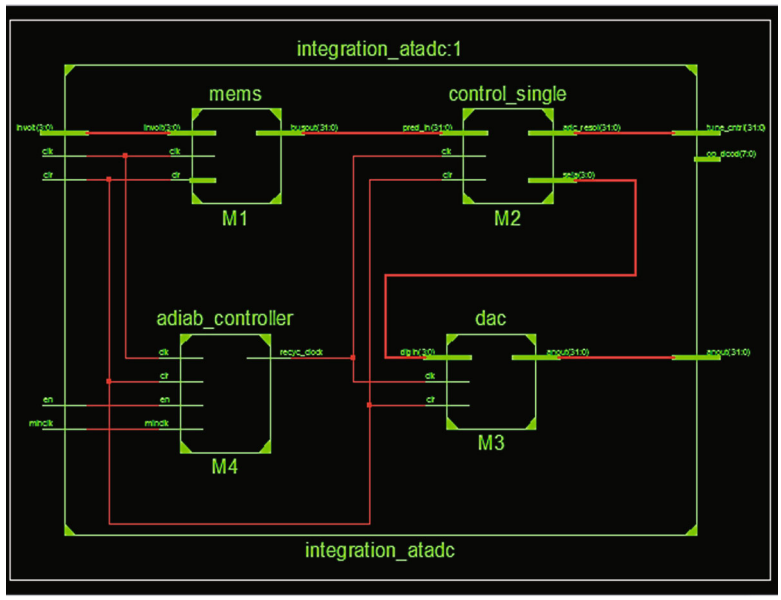

Figure 17: Architectural design of integration module.

(v) Finally, as more and more CMOS technologies progress to lower supply voltages, this makes the proposed circuit well-suited for this operation, with a comparatively low voltage

7.5. Architectural Circuit Design. The architectural design circuit of integration module is shown in Figure 17. The blocks present in the circuit are MEMS, control signal, DAC, and adiabatic controller. The integration modules integrate all these blocks, and then finally, it generates two types of recycled clock pulses CLK1and CLK2 during charging and discharging of capacitive process. CLK1 and CLK2 are used to enable another circuits like AND and MUX. These clocks are only valid for 5 V DC circuits.

7.6. CPLD Implementation. In this work, we had done the partial configuration of FPGA design which is shown in Figure 18. From this board, we have used only few components such as input switches, output led L3, power supply, and ground pin. MEMS value was programmed by using 8 bits; this can be varied as 20 types of input combinations. First, SW16 was kept in LOW position, and according to the truth table, SW1-SW8 can be varied. Based on the input values, LED brightness and clock width of the signal also varied. If clock width increases, LED brightness will decrease. The rise time and fall time values are varied based on clock width.

8. Comparison

8.1. Area Utilization. The area utilized in this design is brought up in the table as device utilization summary. The number of usage of each logic, availability, and their utilization are clearly shown in Tables 2 and 3. The average area utilized in proposed versus existing is also indicated in the following tables.

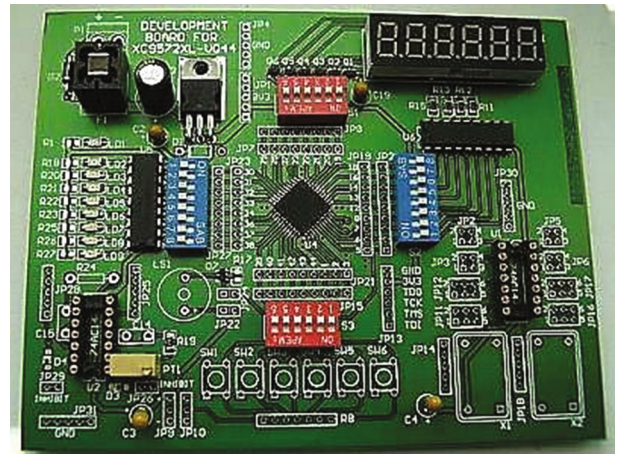

Figure 18: CPLD implementation.

Therefore, the average area utilized in this design is 2.95 which is 20% less than that of existing design, where the existing design occupied 3.31 which is 20% higher than that of proposed design.

8.2. Power Analysis. Finally, Figures 19 and 20 show the analysis of leakage power and the amount of power consumed with adiabatic and without adiabatic controller. In Table 2, the total utilization is 55% and 2% shown in the H column. So totally, 57% is occupied in the existing design, and the leakage power is about 0.62 W as shown in Figure 19.

$$0.62 \times (57\%) = 0.3534 \quad (1)$$

Thus, the required signal and logic power can be obtained by altering the signal rate in the navigator. In existing data, 0.00006 W out of 0.00154 W is obtained.

Table 2: Area utilization without energy recycling.

Logic utilization	Used	Available	Utilization
No/- of slice flip flops	26	7168	1%
No/- of 4 input LUTs	131	7168	1%
No/- of occupied slices	96	3584	2%
Number of slices containing only related logic	96	96	100%
Number of slices containing only unrelated logic	0	96	0%
Total number of 4 input LUTs	157	7168	2%
Number of bonded IOBs	78	141	55%
Average fan-out	3.31		

Table 3: Area utilization summary employing adiabatic controller.

Logic utilization	Used	Available	Utilization
No/- of slice flip flops	67	7168	1%
No/- of 4 input LUTs	175	7168	2%
No/- of occupied slices	124	3584	3%
Number of slices containing only related logic	124	124	100%
Number of slices containing only unrelated logic	0	124	0%
Total number of 4 input LUTs	209	7168	2%
Number of bonded IOBs	80	141	56%
Average fan-out	2.95		

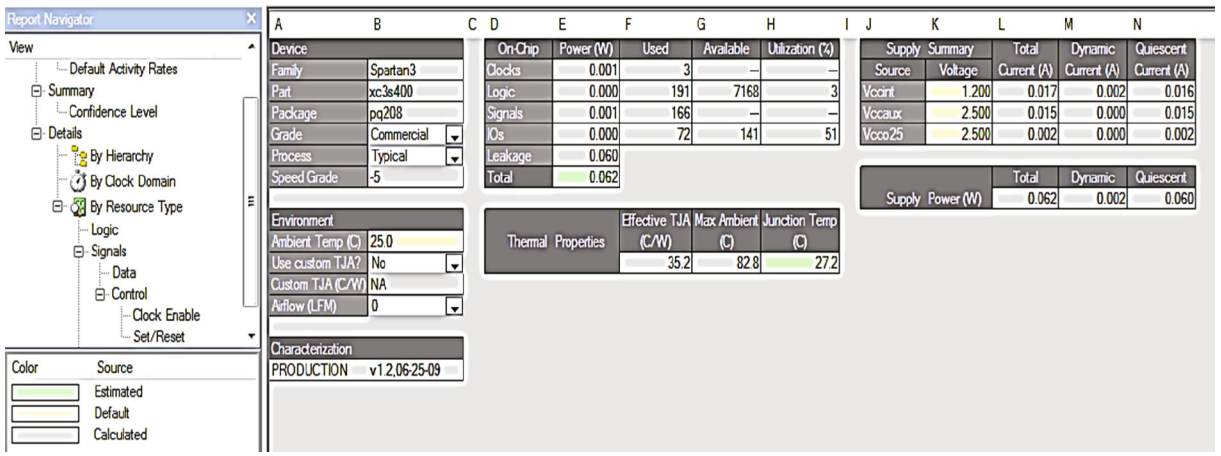

Figure 19: Leakage power without adiabatic architecture.

In Table 3, the total utilization is 51% and 2% shown in the H column. So in total, 53% is occupied in the proposed design and the leakage power is about 0.62 W as shown in Figure 20.

$$0.62 \times (53\%) = 0.3348 \quad (2)$$

Thus, the required signal and logic power can be obtained by altering the signal rate in the navigator. In existing data, 0.00006 W out of 0.00099 W is obtained (0.3534-0.3348 = 0.0186 MW). Therefore, 0.0186 MW of minimum power difference is there in with adiabatic and without adiabatic designs.

By significantly reducing the clock frequency at steady state, as well as the power consumption of the circuits which are ancillary mostly to charging pump, it will greatly reduce dynamic power consumption as indicated in Table 4. When the 8 stages are powered, the circuit dissipates 0.62 W on average. As a result, the minimum power difference between adiabatic and adiabatic architecture is 0.0186 MW. The proposed circuit is a flexible bias circuit that is well suited to MEMS electrostatic actuation due to these requirements.

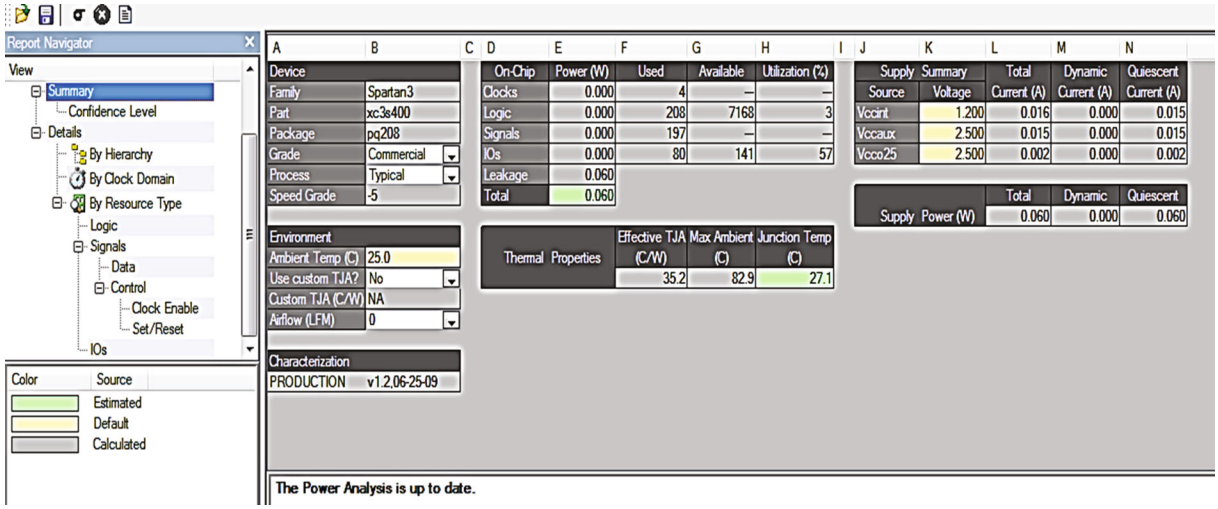

Figure 20: Leakage power with adiabatic architecture.

Table. 4: Comparison of parameters.

Parameters	Charge pump-based MEMS electrostatic actuator [8]	Adiabatic controller-based MEMS electrostatic actuator
CMOS technology	0.13 μm	0.13 μm
Clock frequency	50 MHz and 80 MHz	40 MHz
Area (mm^2)	0.0645	0.0645
Load impedance	1 pF	1 pF
Rise time (ns)	7 μs	80 ns
Fall time (ns)	6.11 μs	6.40 μs
Nonclock sets of fan-out	3.31	3.11
Leakage power consumption (W)	0.00006	0.00006
Power consumption (W)	0.00154	0.00099
Supply voltage	1.2	1.2
Number of stages	8	8
Number of bonded IOBs	55%	51%
Total number of 4 LUTs	2%	2%

9. Conclusion

This research work describes a nonconventional electrostatic MEMS-specific reconfigurable charge pump. In a steady state, the circuit's energy consumption can be reduced by lowering the clock frequency, which takes advantage of the solely capacitive load characteristics of MEMS electrostatic actuators. To allow for short output voltage rise times for stable MEMS actuation, a 50 MHz clock frequency was used, and the clock frequency was also decreased in steady-state operation to save power. A circuit that can be reconfigured to create a variety of voltage levels and dynamically changing output voltage is required for an ideal MEMS actuator. To reduce power dissipation, the adiabatic logic controller allows for dynamically altering output voltage. Reduced power consumption is achieved by using a variable frequency clock. The major findings of the work are listed as follows:

(1) A rising time of 80 ns and a fall time of 6.40s are accomplished with a 40 4MHz clock. The circuit consumes 0.00099 W of power at the max output voltage for a 40 MHz clock. The output load of this circuit is a MEMS capacitive actuator; hence, no significant output DC current is delivered

(2) By significantly reducing the clock frequency at steady state, as well as the power consumption of the circuits which are ancillary mostly to charging pump, it will greatly reduce dynamic power consumption. When the 8 stages are powered, the circuit dissipates 0.62 W on average. As a result, the minimum power

difference between adiabatic and adiabatic architecture is 0.0186 MW. The proposed circuit is a flexible bias circuit that is well suited to MEMS electrostatic actuation due to these requirements

(3) Because of the circuit's small size, it can be integrated with MEMS in the same box, or multiple bias circuits can be used for MEMS that require multiple actuation voltages. In recent years, VLSI technology has been the most common and advanced technology. This technology could able to reduce power consumption by using adiabatic logic and low power blocks. Power can be recycled and is used in portable wireless devices including pressure sensing, blood pressure measurement, and cell phones using the adiabatic circuit. Recycled power has been stored in devices for a long time and automatically withstands the capacity

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest regarding the publication.

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References

[1] R. Uma, J. Ponnian, and P. Dhavachelvan, "New low power adders in self resetting logic with gate diffusion input technique," *Journal of King Saud University-Engineering Sciences*, vol. 29, pp. 118–134, 2017.

[2] S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis & Design*, McGraw-Hill, New York, NY, USA, 2002.

[3] W. C. Athas, J. Svensson, J. G. Koller, N. Tzartzanis, and Y. C. Chou, "Low-power digital systems based on adiabatic-switching principles," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 2, no. 4, pp. 398–407, 1994.

[4] S. Jain, S. Garg, N. Pandey, and K. Gupta, "Sinusoidal power clock based PFAL," *ICTACT Journal on Microelectronics*, vol. 5, pp. 801–806, 2019.

[5] S. Ilyas and M. I. Younis, "Resonator-based M/NEMS logic devices: Review of recent advances," *Sensors and Actuators A: Physical*, vol. 302, article 111821, 2020.

[6] A. Khorami and R. Saeidi, "Energy consumption analysis of the stepwise adiabatic circuits," *Microelectronics Journal*, vol. 104, article 104868, 2020.

[7] R. M. Bommi and R. S. Selvakumar, "A survey on adiabatic logic families for implementing reversible logic circuits," in *2018 IEEE International Conference on Computational Intelligence and Computing Research (ICCIC)*, pp. 1–4, Madurai, India, 2018.

[8] K. Gupta and N. P. VishwasGosain, "Adiabatic Differential Cascode Voltage Switch Logic (A-DCVSL) for low power applications," *Journal of King Saud University - Engineering Sciences*, vol. 34, no. 3, pp. 180–188, 2022.

[9] A. H. Alameh and F. Nabki, "A 0.13- μm CMOS dynamically reconfigurable charge pump for electrostatic MEMS actuation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 4, pp. 1261–1270, 2017.

[10] P. Beaulieu, A. H. Alameh, M. Menard, and F. Nabki, "A 360 V high voltage reconfigurable charge pump in 0.8 μm CMOS for optical MEMS applications," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1630–1633, Montreal, QC, Canada, 2016.

[11] I. Vaisband and E. G. Friedman, "Stability of distributed power delivery systems with multiple parallel on-chip LDO regulators," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5625–5634, 2016.

[12] A. Shirane, H. Ito, N. Ishihara, and K. Masu, "A 21 V output charge pump circuit with appropriate well-bias supply technique in 0.18 μm Si CMOS," in *2011 International SoC Design Conference*, pp. 28–31, Jeju, Republic of Korea, 2011.

[13] A. H. Alameh, A. Robichaud, and F. Nabki, "A reconfigurable charge pumps in 0.13 μm CMOS for agile MEMS actuation," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 670–673, Marseille, France, 2014.

[14] R. M. Bommi and M. S. Christo, "Adiabatic Configurable Reversible Synthesizer for 5G Applications," *Arabian Journal for Science and Engineering*, vol. 47, 2022.