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Research Article

Low-Voltage Low Noise Figure Down-Conversion Mixer for Band #1 of MB-OFDM System in 180 nm Complementary Metal Oxide Semiconductor Technology

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Low-voltage design is a challenge for Gilbert cell-based mixers due to stacking transconductance and switching stage. This work addresses this issue by proposing a design of a low-voltage down-conversion mixer for band #1 of multiband orthogonal frequency division multiplexing (MB-OFDM) system in 180 nm complementary metal oxide semiconductor (CMOS) technology. The mixer is tuned at band #1 at RF frequency of 3.432 GHz and IF frequency of 264 MHz. The proposed mixer uses folded cascode connection of LO and RF in order to increase headroom and to reduce the DC supply voltage for low-voltage operation. Common gate configuration is used at RF transconductance stage to enhance the input bandwidth of the mixer. RF and LO ports are matched to 50 Ω using differential T and LC matching, respectively. The resistive source denegation technique is used to linearize transconductance with respect to the bias point. The common source stage is used at the IF port as a buffer cum matching circuit it. The simulation results of the mixer show the maximum conversion gain of 9.76 dB, 1 dB compression point (P1dB) of -16.25 dBm, the third-order input intercept point (IIP3) of -4.70 dBm, an SSB noise figure of 9.036 dB, and S11of -19.490 dB at the supply voltage of 1.2 V. Excluding off chip components, proposed mixer records an active area of 926.35 μm^2.

1. Introduction

Vision of Industry 4.0 is the transformation of entire manufacturing unit into an IoT-enabled unit. MB-OFDM system is next-generation wireless standard for high-speed wireless personal area networks. It can be a potential candidate for wireless standard for some of the Internet of Things (IOT) applications. The MB-OFDM spectrum covers 14 bands, each with a 528 MHz bandwidth. Band 1 ranges from 3.168 GHz to 3.696 GHz with center frequency of 3.432 GHz. The MB-OFDM frequency plan as shown in Figure 1 is composed of five orthogonal band groups (BG) and one additional overlapping band group. Most band groups are composed of three separate bands except for BG#5, which has only two bands [1–3].

Heterodyne receiver architecture is preferred over homodyne receiver architecture due to higher selectivity and low power amplifier pulling issues. Down-conversion mixer is an essential block of the heterodyne receiver which converts high-frequency RF to IF signal. Being a nonlinear system, mixer dominates the overall performance of a transceiver system including gain, distortion, and noise figure.

Most of the active mixer architecture uses Gilbert cell [4–15] as a core of the mixer due to its double differential and double-balanced feature, which results in good port to port isolation and low even order distortion and low noise figure. The schematic of double-balanced Gilbert cell mixer is shown in Figure 2. Gilbert cell mixer consists of three stack stages, namely, transconductance stage, LO switching stage, and load

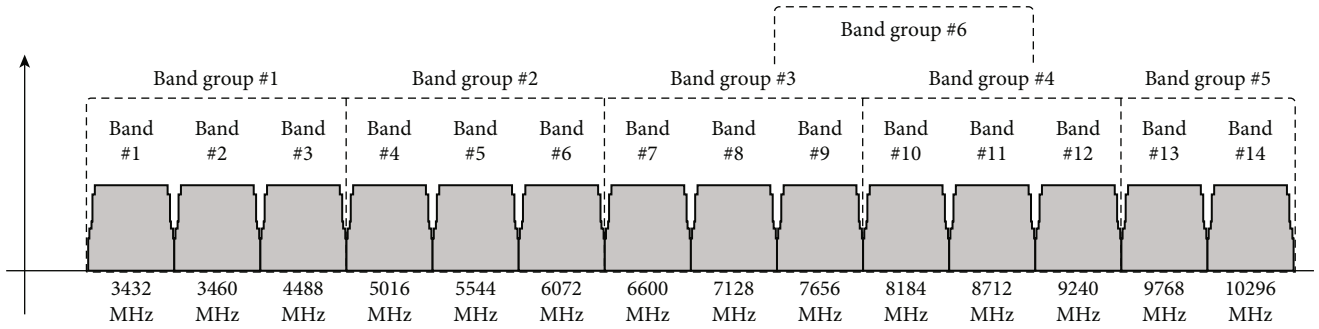

Figure 1: MB-OFDM frequency plan.

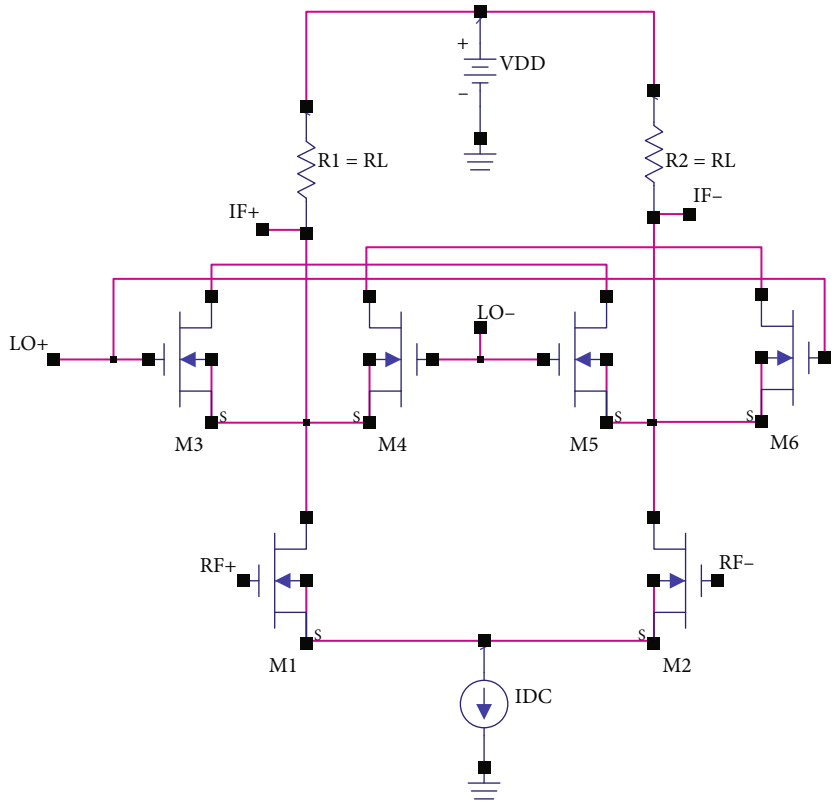

Figure 2: Schematic of Gilbert cell mixer.

stage as shown in Figure 2. As VDD drops across multiple stacked stages so voltage swing (Vds), available across the transistors decreases, which limits the operation for low-voltage applications. If input voltage increases beyond the headroom available, then clipping of voltage occurs which results in distorted waveforms. In Gilbert mixer as shown Figure 2, RF stage transistors M1 and M2 work as a differential amplifying stage. Transistors M3–M6 work as a differential switch controlled by differential LO signal. Primary causes of distortion in Gilbert mixer are low value of headroom at the low operating voltage and third-order nonlinearity. The problem of low value of headroom arises due to drop of VDD across three stacked stages, i.e., RF transconductance stage, LO switching stage, and load stage.

Voltage conversion gain (A_V) of the mixer is given by the following equation, A_V = Amplitude of IF voltage/Amplitude of RF voltage.

$$A_V = \frac{((4/\pi)I_{\mathrm{RF}}R_L)}{2V_{\mathrm{RF}}} = \frac{2}{\pi}g_m R_L. \quad (1)$$

Basic Gilbert cell mixer is based on cascode connection of RF transconductance and LO stages as shown in Figure 2. In cascode connection, both RF and LO stages use NMOS transistors. Cascode structure has the advantage as higher gain bandwidth product, but it results in low headroom available due to staking of RF and LO stage transistors. The use of folded cascode structure helps to maintain voltage headroom in a differential configuration, which allows for low-voltage operation. Different versions of folded cascode techniques in the Gilbert mixer are reported. Folded Gilbert cell with three supply voltages is proposed for improved linearity [16]. A 2.4-GHz-folded transconductor RF mixer is proposed using CMOS 70 nm

technology at 2.4 GHz [17]. Folded Gilbert cell mixer is proposed for analog to digital converter in 0.18 μm technology [18]. A folded cascode mixer with active balun integrated in the transconductance for single-ended input and differential output is proposed for UWB applications [19]. An integrated low noise amplifier (LNA) mixer using folded cascode form of LNA and folded sub-threshold mixer is proposed for 2.4–2.48 GHz frequency band [20]. A folded Gilbert cell-based mixer with a current-bleeding technique is proposed for 2.4 GHz and 5.2 GHz frequencies [21]. A folded down-conversion Gilbert cell mixer in 0.13 μm CMOS technology is proposed for 5–6 GHz frequency band [22]. A low-voltage down-conversion mixer using folded Gilbert cell topology is presented in 0.13 μm CMOS technology for UWB band of 3–7 GHz [23]. A folded Gilbert cell mixer with low power and low flicker noise in 0.18 μm CMOS process is presented for 3.5-10 GHz UWB band [24]. A low-voltage CMOS wideband folded Gilbert cell mixer is designed for 3.5-8.0 GHz frequency [25]. A low-voltage high-linearity folded switching CMOS mixer in 0.13 μm technology is presented for direct-conversion UWB receiver in 3-5 GHz frequency range [26]. A mixer with folded cascode configuration of Gilbert cell in 0.18 μm RF CMOS process is proposed at 1.8 GHz frequency for the radio receivers for the use for navigation, aviation, and other related applications [27]. A down-conversion mixer with folded Gilbert cell for the UWB (4.2-4.8 GHz) and IMT advanced (3.4-3.6 GHz)) bands with reconfiguration feature are proposed. Capacitive cross-coupling is used for input matching at the RF stage [28]. A modified feedforward compensated differential transconductance, LC folded cascode mixer is proposed 0.18 μm CMOS technology for ultra-wideband applications [29]. A differential multiple gated transistor quadrature mixer with folded structure in a 0.18 μm CMOS process is proposed for 150 kHz to 1.5 GHz frequency range [30]. A folded cascode mixer LC-tank bias circuit is proposed for 2.3 GHz and 5.2 GHz bands [31].

2. The Proposed Mixer

A double-balanced down-conversion mixer utilizing folded cascode connection of RF and LO stages and common gate transconductance stage as a modification of Gilbert cell is proposed for band #1 of MB-OFDM system at RF frequency of 3.432 GHz and IF frequency of 264 MHz. Folded cascode connection in Gilbert mixer avoids the problem of stacking of transistors across a low-voltage power supply using PMOS transistors at LO stage as a folded cascode connection. Common gate RF transconductance stage configuration is used in the proposed mixer. Common gate configuration is chosen for transconductance stage as it offers larger bandwidth than the common source configuration. Effective transconductance $g_{m(\text{eff})}$ in case of common gate configuration is given by

$$g_{m(\text{eff})} = \frac{g_m}{1 + g_m R_s + sR_s C_{\text{gs}}}, \tag{2}$$

where g_m is transconductance and C_{gs} is the gate to source internal parasitic capacitance of RF stage MOSFETs. Parasitic capacitance is a significant problem in high-frequency circuits, and it limits the operating frequency and bandwidth of the circuit. R_s is the series resistance of RF signal source whose standard value is taken as 50 Ω.

If

$$g_m \gg \frac{1}{R_s}, \tag{3}$$

Then

$$g_{m(\text{eff})} \approx \frac{1}{R_s}. \tag{4}$$

It is indicated by (4) that common gate shows a wideband transconductance with corner transition frequency ω_T given by

$$\omega_T = \frac{1 + g_m R_S}{R_s C_{\text{gs}}} \approx \frac{g_m}{C_{\text{gs}}}. \tag{5}$$

It is clearly indicated from (5) that corner transition frequency ω_T decreases with increase in parasitic capacitance C gs. In addition to wideband characteristics, common gate configuration also offers lower input impedance in comparison to a common source, which helps in the matching of input RF port to the low value of the standard port impedance of 50 Ω. The schematic of the proposed down-conversion mixer circuit is shown in Figure 3. Transconductance stage NMOS transistors (M1, M2) are biased in common gate configuration. R3 and R4 are used as source degenerated resistors. Source degeneration technique is used for linearizing gm in addition to common gate configuration. Linearization of gm helps in wideband input RF matching. Inductor-resistor pairs (R1, L1) and (R2, L2) are used as RF chokes to provide a high impedance to RF currents [23] at a frequency of 3.432 GHz so that most of the RF currents can pass through the folded cascode LO switching stage. LO switching stage consists of PMOS transistors (M3-M6) which are connected in a folded cascode configuration. Folded cascode connections help in independent biasing of RF and LO stages and remove the stacking of RF and LO stages transistors and result in increased headroom. Transistors (M7, M8) are used in common source configuration as an output buffer due to high input impedance and moderate output impedance offered by common source configuration.

Differential T matching as shown in Figure 4 is used at the RF port (RF+, RF-). Differential T matching is a type of three element matching circuit. Three element matching provides the flexibility to control the quality factor and hence bandwidth of the system. Design equations of differential T matching are given as follows.

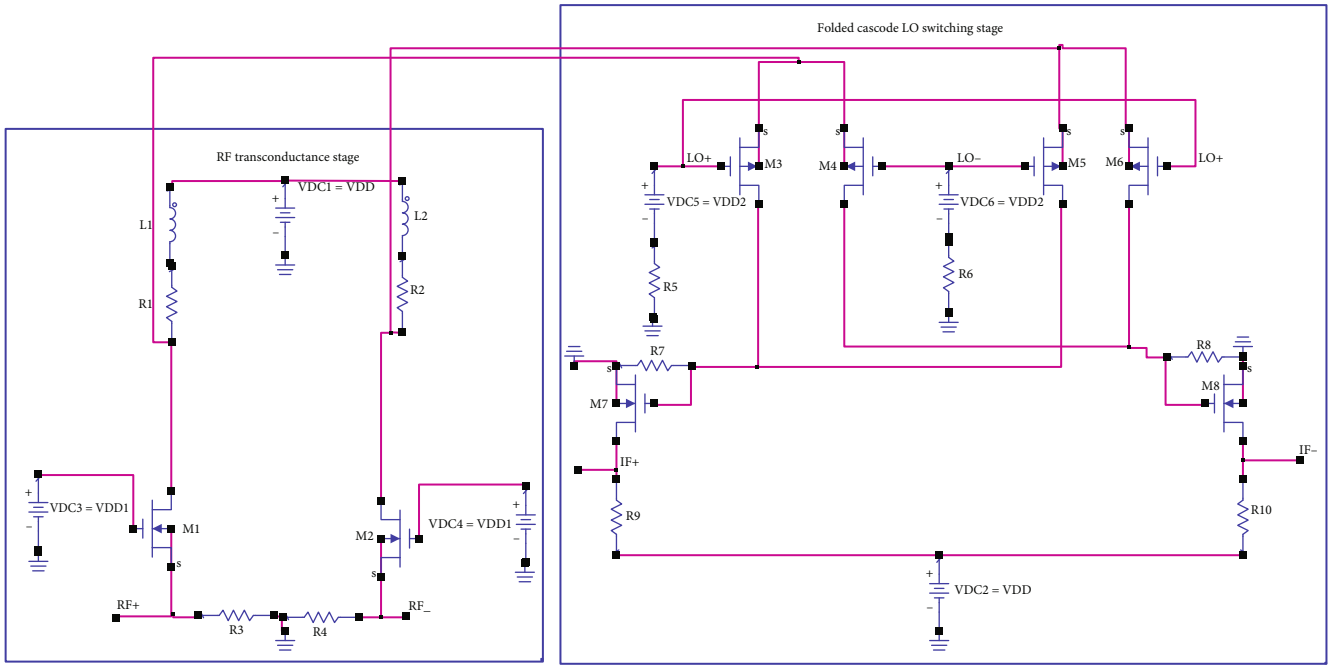

Figure 3: Schematic of proposed mixer.

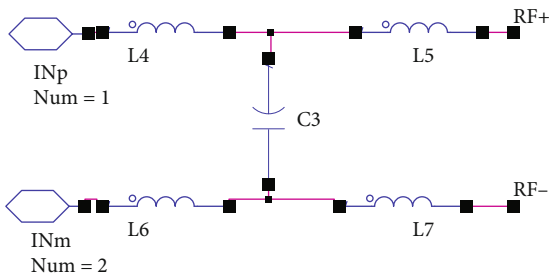

Figure 4: Schematic of differential T matching circuit at RF port.

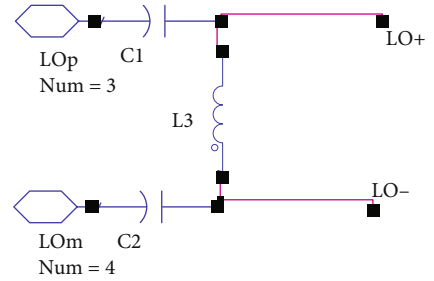

Figure 5: Schematic of differential LC matching circuit at LO port.

$$
\begin{aligned}
Q &= \sqrt{\left(\frac{R_I}{R_{\text{in}}} - 1\right)} + \sqrt{\left(\frac{R_I}{\text{Re}\,(Z_{\text{RF}})} - 1\right)},\\
Q_1 &= \sqrt{\left(\frac{R_I}{R_{\text{in}}} - 1\right)}, Q_2 = \sqrt{\left(\frac{R_I}{\text{Re}\,(Z_{\text{RF}})} - 1\right)},\\
C_1 &= \frac{Q_1}{\omega_{\text{RF}} R_I}, C_2 = \frac{Q_2}{\omega_{\text{RF}} R_I},\\
C_3 &= C_1 + C_2,\\
L4 = L6 &= \frac{Q_1 R_{\text{in}}}{2\omega_{\text{RF}}}, L5 = L7 = \frac{Q_2\ \text{Re}\,(Z_{\text{RF}})}{2\omega_{\text{RF}}},
\end{aligned}
\tag{6}
$$

where $R_{\text{in}} = 50\,\Omega$ is the standard port impedance required to be matched to impedance (Z_{RF}) looking towards input of RF stage. Re (Z_{RF}) is the resistive part of Z_{RF}. The capacitive reactance of Z_{RF} is accommodated in the value of $L5$and $L6$.

Differential LC matching as shown in Figure 5 is used at the LO stage (LO+, LO-). Differential LC matching is a type of two element matching circuit. It does not allow arbitrarily selection of quality factor. Being a switching control signal, LO signal does not require to use a specific value of quality factor so being of a simple circuitry, differential LC matching is used to match LO port.

Design equations of differential LC matching are given as follows.

$$
\begin{aligned}
Q &= \sqrt{\left(\frac{R_e(Z_{\text{LO}})}{R_{\text{in}}} - 1\right)},\\
C_s &= \frac{1}{\omega_{\text{RF}} Q R_{\text{in}}},\\
C_1 = C_2 &= 2C_s\left(\frac{Q^2}{1+Q^2}\right),\\
L_3 &= \frac{1}{\omega_{\text{RF}}^2 C_s},
\end{aligned}
\tag{7}
$$

where $R_{\text{in}} = 50\,\Omega$ is the standard at LO port impedance required to be matched to impedance Z_{LO} looking towards LO port. Re (Z_{LO}) is the resistive part of Z_{LO}. The capacitive reactance of Z_{LO} is accommodated in the value of C_1 and C_2.

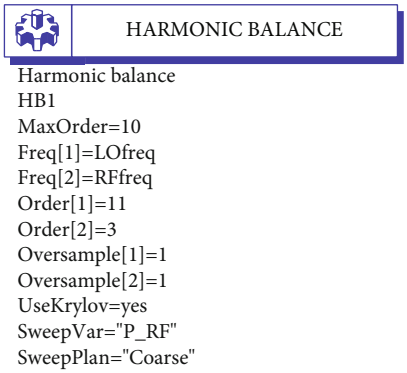

Figure 6: Harmonic balance simulation parameters.

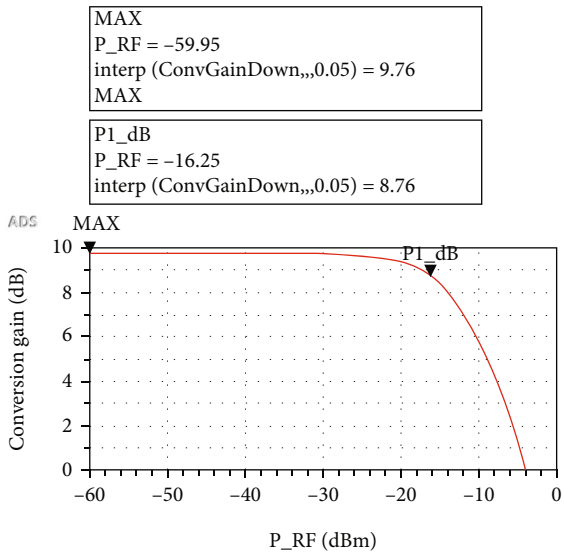

Figure 7: Conversion gain versus RF power level (P_RF).

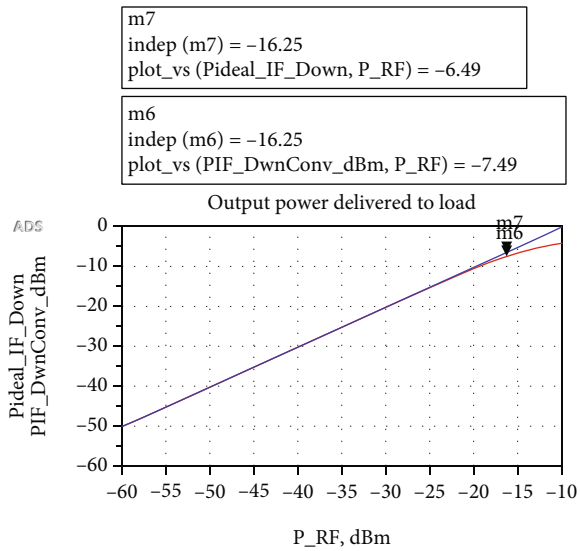

Figure 8: Ideal and simulated IF output power level (PIF) versus input RF power level (P_RF).

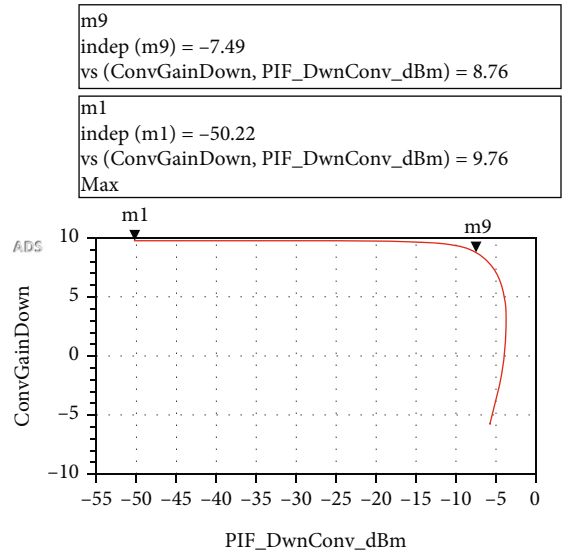

Figure 9: Conversion gain versus IF power level (P_IF).

CMOS process technology is widely used in analog and digital hardware design due to certain advantages such as CMOS devices are mechanically robust, nonsalicided poly layer is generally used for fabrication of linear resistors in analog CMOS IC design, CMOS hardware is highly integrable and compact due to sharing of diffusion regions, and very low values of static power dissipation are there with the availability of high noise margin [32–39]. Reason for choosing 180 nm technology is that cut off frequencies of 180 nm nMOSFETs ranges from 50 GHz to 80 GHz for diverse layout states which lies in the of operating frequency range of the proposed mixer [40]. Further possibility of short channel effects is lesser in 180 nm CMOS technology compared to sub-180 nm CMOS technology.

3. Simulation Results

The proposed mixer is designed using GPDK 0.18 μm CMOS technology using ADS software with 0 dBm LO power with VDD = 1.2 V, VDD1 = 0.7 V, and VDD2 = 0.1 V. RF frequency (f_{RF}) is taken as center frequency of band 1 of MB-OFDM that is equal to 3.432 GHz. The channel bandwidth recommended for MB-OFDM UWB system is 528 MHz. So IF frequency is chosen equal to half of channel bandwidth; *i.e.*, 528/2 = 264 MHz. LO frequency is higher or lower by RF frequency by amount of intermediate frequency (f_{IF}) as given by

$$f_{LO} = f_{LO} \pm f_{RF}. \tag{8}$$

Higher value of LO frequency (high side injection) is chosen as it results in better (lower) tuning range of LO.

$$f_{LO} = 3.432\ \text{GHz} + 264\ \text{MHz} = 3.696\ \text{GHz}. \tag{9}$$

Harmonic balance simulation parameters are shown in Figure 6. Harmonic balance simulation is done to observe distortion in nonlinear circuits and systems in frequency domain at RF and microwave frequencies. LO power (0 dBm) is higher

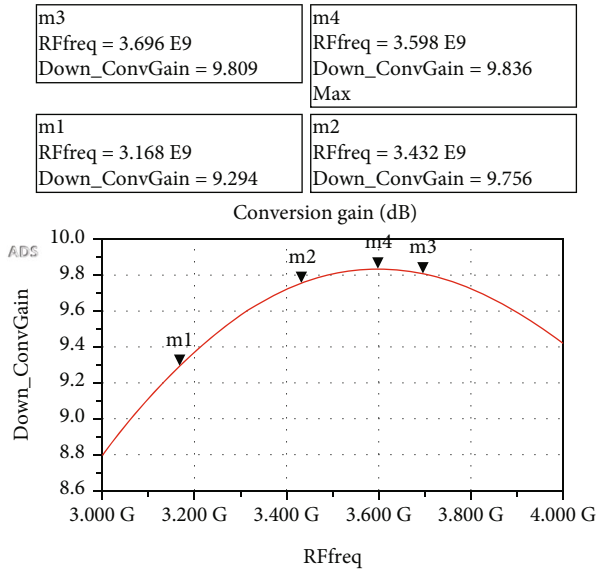

Figure 10: Simulated conversion gain versus input RF frequency.

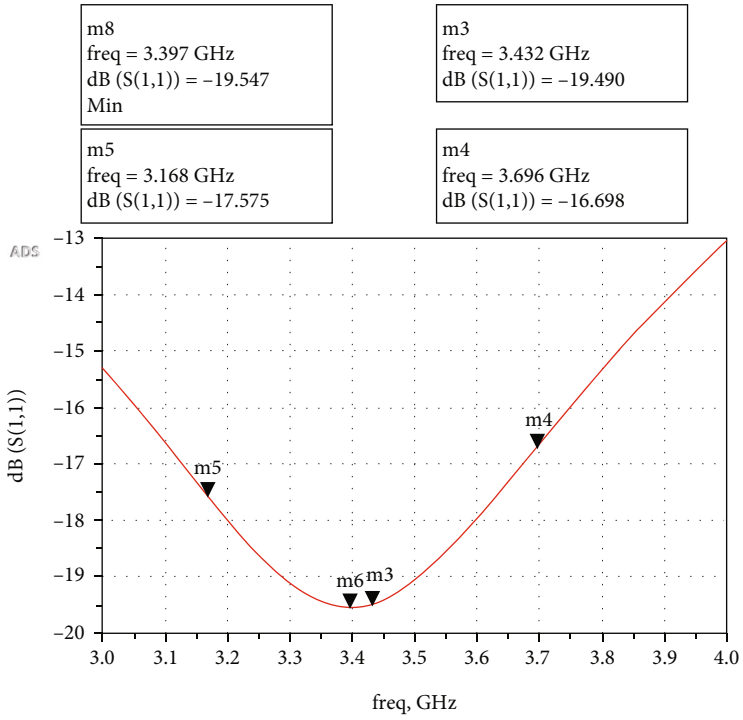

Figure 11: S11 versus RF frequency.

than RF signal power (-65 dBm onwards) so maximum harmonic order is chosen as 11 and 3 for LO and RF signal, respectively. Maximum intermodulation order for mix frequency components is chosen as 10.

Gain compression simulation is done to observe the variation of conversion gain as a function of input RF power level as shown in Figure 7. Results show that the maximum conversion gain achieved by the mixer is 9.76 dB. Conversion gain remains constant for the range of input RF power levels and starts decreasing at higher values of input RF power levels, which validates the gain compression phenomenon in the proposed mixer circuit. Gain compression is an indication of the nonlinearity of the circuit. The amount of gain compression (nonlinearity) of the circuit is measured through 1 dB compression point (P1dB), whose value is observed as -16.25 dBm at which gain is reduced to 8.76 dB.

Gain compression phenomenon is also observed through simulation results of ideal and delivered IF power versus RF

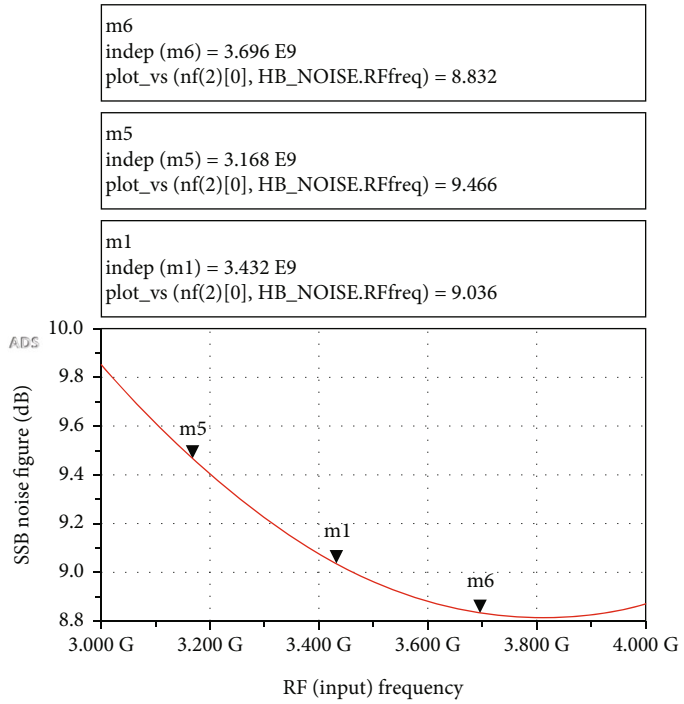

Figure 12: Single side band noise figure versus RF frequency.

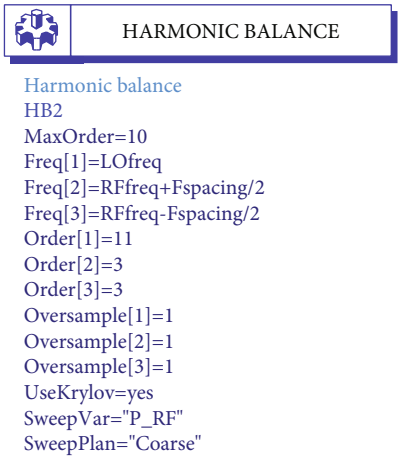

Figure 13: Harmonic balance simulation parameters for IM simulation.

power as shown in Figure 8. Ideal gain can be calculated through ideal IF power variation as 9.76 dB (-6.49+16.25). Compressed conversion gain at a power level of -16.25 dBm is calculated as 8.76 dB (-7.49+16.25), which is 1 dB lower than the ideal gain. P1dB value of -16.25 dBm is revalidated by this result.

The variation of simulated conversion gain with IF power level is shown in Figure 9. The maximum flat conversion gain is shown as 9.76 dB, and gain is reduced by 1 dB at an IF power level of -7.49 dB. These results are in exact agreement with earlier results as shown in Figures 7 and 8.

Simulated conversion gain with RF frequency is shown in Figure 10. Maximum conversion gain achieved as 9.836 dB across band #1 of MB-OFDM system. Conversion gain of 9.294 dB, 9.756 dB, and 9.809 dB is observed at the lowest frequency of 3.168 GHz, center frequency of 3.432 GHz, and highest frequency of 3.696 GHz, respectively, of band #1 of MB-OFDM system.

S parameter simulation is done to observe the matching performance of the proposed mixer circuit at the RF port. The simulated result of S11 at the RF port is shown in Figure 11. The minimum value of S11 of -19.547 dB is observed at a frequency of 3.397 GHz. The value of S11 of -17.575 dB, 19.490 dB, and -16.698 dB is observed at the lowest frequency of 3.168 GHz, center frequency of 3.432 GHz, and highest frequency of 3.696 GHz, respectively, of band #1 of MB-OFDM system. This shows that the value of S11 is quite low from -10 dB across whole band #1 of the MB-OFDM system, which implies that the mixer is well matched in wideband nature to 50 Ω standard port impedance at RF input.

Figure 12 shows the variation of the single side band noise figure (SSB NF) with RF frequency. The values of SSB noise figure of 9.466 dB, 9.036 dB, and 8.832 dB are observed at the lowest frequency of 3.168 GHz, center frequency of 3.432 GHz, and highest frequency of 3.696 GHz, respectively, of band #1 of MB-OFDM system.

For simulation of intermodulation (IM) products of the proposed mixer, two frequencies f_1 and f_2 of equal power levels are required to be inputted to the mixer such that resultant third-order IM products f_{USB} (upper side band third-order IM product) $=2f_1 - f_2$ and f_{LSB} (lower side band third-order IM product) $=2f_2 - f_1$, $(f_1 > f_2)$. Two frequencies are set for this purpose as $f_1 = f_{\text{RF}} + f_{\text{spacing}}/2$ and $f_2 = f_{\text{RF}} -$

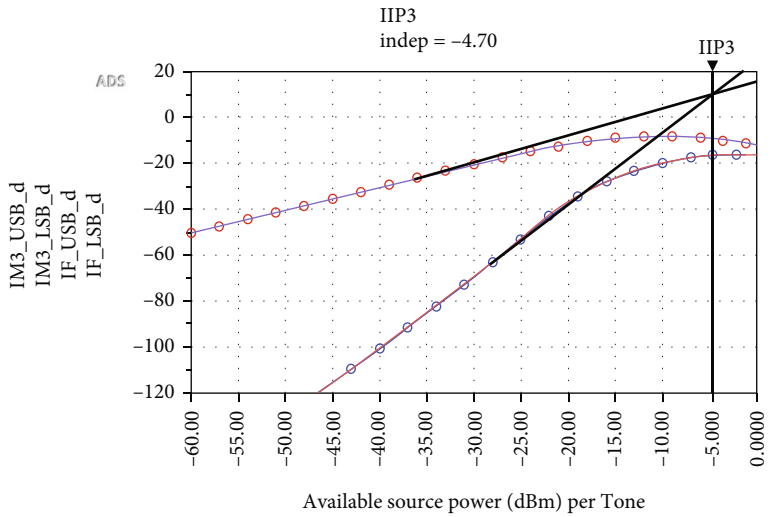

Figure 14: Simulated results of two tone IMD simulation.

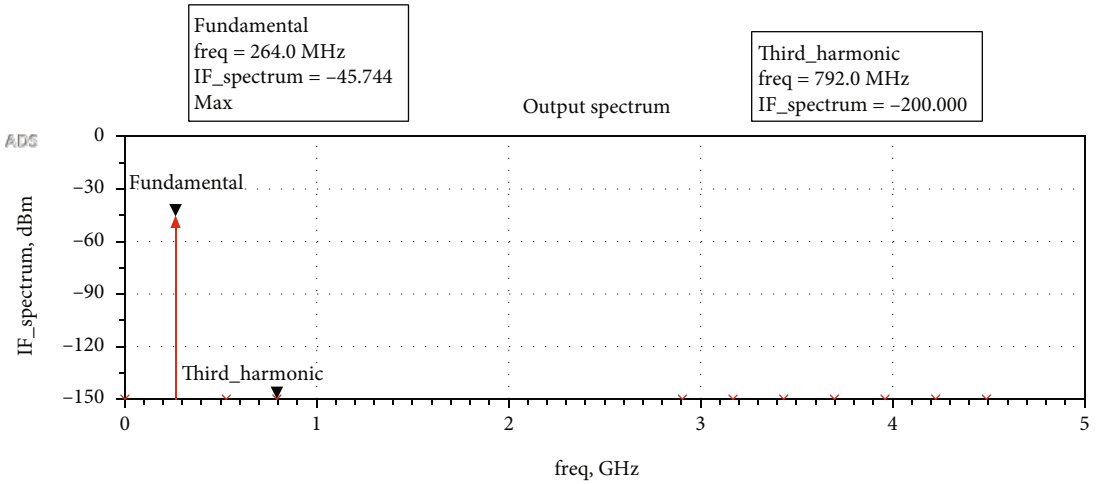

Figure 15: Simulated output IF power spectrum.

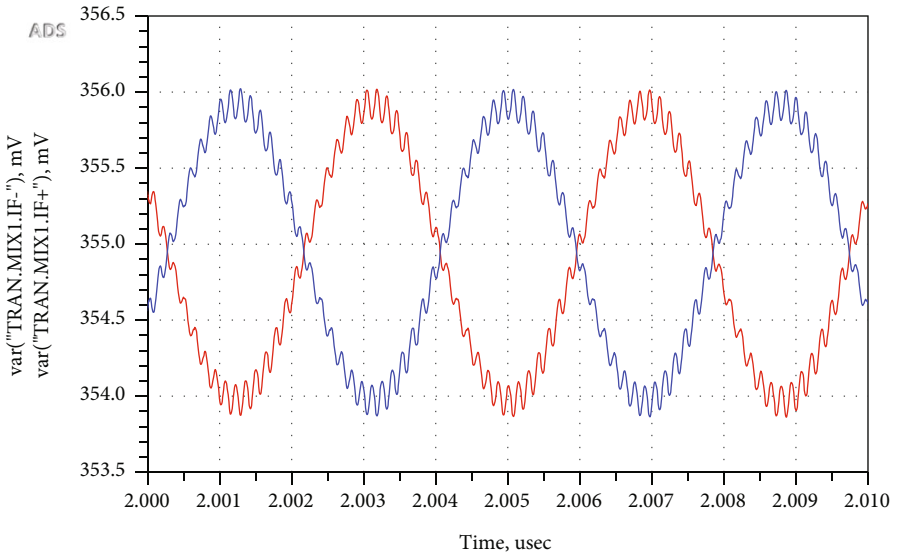

Figure 16: IF+ and IF- waveforms after transient simulation.

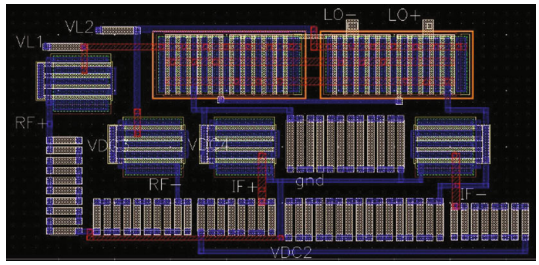

Figure 17: Layout of proposed mixer.

Table 1: Performance summary and comparison with the other works.

Ref.	Technology (CMOS process)	DC voltage (V)	RF frequency (GHz)	Conversion gain (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)	S11 (dB)
[18]	0.18 μm	1.8	0.01-0.3	2.82-8.2	(-3.86)–(-2.06)	—	34.64-11.35 (SSB)	—
[24]	0.18 μm	1.8	3.5-10	5	-2.52	—	21 (SSB)	—
[21]	0.18 μm	1.8	5.2/5.1	13.07	-2.84	-14.44	30.33	—
[21]	0.18 μm	1.8	2.4/2.3	16.1	-3.14	-14.93	27.26	—
This work	0.18 μm	1.2	3.432	9.76	-4.7	-16.25	9.036 SSB	-19.49

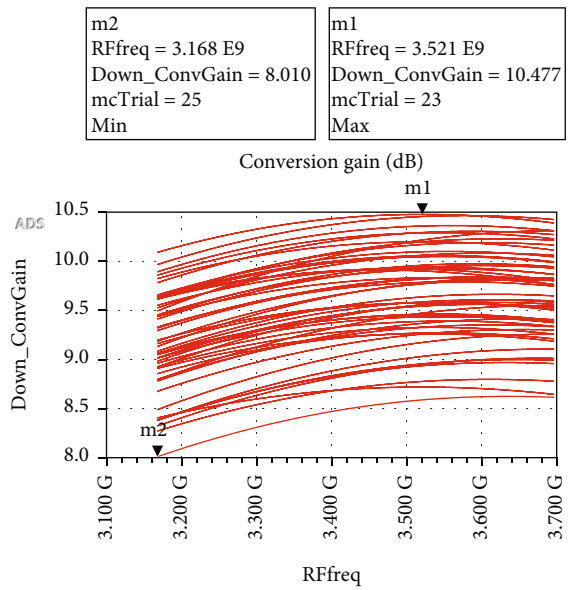

Figure 18: Monte-Carlo analysis of conversion gain.

$f_{spacing}/2$. The value of $f_{spacing}$ should be chosen such that mix frequency products corresponding to f_{USB} and f_{LSB} should be within IF bandwidth. For f_{RF} = 3.432 GHz and $f_{spacing}$ = 200 KHz, the vales of third-order IM products come out as f_{USB} = 3432.3 MHz and f_{LSB} = 3431.7 MHz. Mix frequency products corresponding to these are $f_{IM3USBd} = f_{USB} - f_{LO}$ = 263.7 MHz and $f_{IM3LSBd} = f_{LSB} - f_{LO}$ = 264.3 MHz, which lie within the IF bandwidth. Harmonic balance simulation parameters for IM simulation are shown in Figure 13.

Simulated results of two tone IM simulations are shown in Figure 14. The graph of $f_{IM3USBd}$ and $f_{IM3LSBd}$ overlaps each other as a result of equal power of f_1 and f_2; also, the graph of $f_{USBd} = f_1 - f_{LO}$ and $f_{LSBd} = f_2 - f_{LO}$ also overlaps each other due to the same reason. IIP3 value, which is the intersection of extrapolated graph of these corresponding graphs, is observed at -4.70 dBm.

Table 2: Component values of proposed mixer.

Components	Values
Widths of ($M1$, $M2$, $M7$, $M8$)	20 μm
Widths of ($M3$, $M4$, $M5$, $M6$)	30 μm
$R1$, $R2$	50 Ω
$R3$, $R4$	400 Ω
$R5$, $R6$	2.5 kΩ
$R7$, $R8$	760 Ω
$R9$, $R10$	330 Ω
$L1$, $L2$	6.5 nH
($C1$, $C2$), $L3$	100 pF, 17 nH
$C3$, ($L4$, $L6$), ($L5$, $L7$)	0.34 pF, 1.61, 3 nH

The simulated output IF power spectrum is shown in Figure 15. A fundamental IF frequency of 264 MHz is observed at a power level of -45.744 dBm. This result is also in exact agreement with results as observed in Figures 7–9. In these results, the value of conversion gain at an RF frequency of 3.432 GHz at a power level of -55.5 dBm is observed as 9.76 dB. So the output IF power level = Conversion gain (9.76 dB) + RF power level (−55.5 dBm) = −45.74 dBm. Output spectrum shows no second harmonic and highly reduced third harmonic at 792 MHz at a power of -200 dBm. The mixer shows no (highly reduced) level of second (even) harmonic due to its double-balanced differential configuration.

Transient analysis is done to observe the time domain waveforms of IF output. Output waveforms of IF+ and IF- are shown in Figure 16. Both the waveforms are exactly out of phase as expected. Some jitter is observed in output waveforms due to the presence of noise. No clipping is observed in the waveforms, which implies that sufficient headroom is available across all the transistors.

The layout of the proposed mixer is drawn and shown in Figure 17. Inductor L1 and L2 and matching network components for LO and RF ports are selected as off chip components. This selection of components as off chip facilitates very large saving in active area.

Table 1 summarizes the performance parameters of the proposed mixer in comparison to those of other reported low-voltage mixers. Mixer proposed by [21] shows a high value of conversion gain, but NF reported is quite high. Mixer proposed in this work shows a high gain, high IIP3, high P1dB, and low noise figure and suitably matching at RF port with a very low value of S11 for band #1 of MB-OFDM system. Proposed mixer operates at a very low supply voltage of 1.2 V.

Monte-Carlo analysis is performed on 50 samples to observe the overall sensitivity of the proposed mixer to the process variations and mismatch. Results corresponding to conversion gain are shown in Figure 18. These results demonstrate a reasonable discrepancy that does not affect the mixer output.

Table 2 provides the list of the final component values of the proposed mixer.

4. Conclusion

A low-voltage low noise figure and low S11 double-balanced down-conversion mixer are proposed for band #1 of MB-OFDM system. The mixer is tuned at a center frequency of RF frequency of 3.432 GHz and IF frequency of 264 MHz. The proposed mixer uses Gilbert cell as a core of the mixer. Folded cascode connection of LO and RF stages is used so that mixer can operate at low voltage without compromising on voltage headroom across the transistors. Common gate configuration and differential T matching are used at the RF transconductance stage in order to enhance the bandwidth with minimal reflections at the RF port. Mixers show a very low value of S11 of lesser than or equal to -16.698 dB across whole band #1 of MB-OFDM. Differential LC matching is used at the LO port. Resistive source degeneration technique is applied at the RF stage to linearize RF transconductance against bias variations. The common source stage is used at the IF port as a buffer cum matching circuit due high input and low output impedance characteristics. The mixer achieves the maximum conversion gain of 9.76 dB, P1dB compression point of -16.25 dBm, the third-order input intercept point (IIP3) of -4.70 dBm, an SSB noise figure of 9.036 dB, and value of S11 -19.490 dB at the bias voltage of 1.2 V. Mixer shows superior characteristics in terms low-voltage low noise figure with a low value of input reflection coefficient for the targeted band #1 of MB-OFDM system.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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