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Research Article

Electrostatic Potential Distribution Analysis of Silicon Nanowire Field Effect Transistor with Various Channel Length

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Silicon nanowire FET plays a vital role in building of nanoscale electronic device applications. In this article, the silicon nanowire field effect model is designed with different channel lengths. By using the SiNW FET device model, various electrostatic potential distribution studies are done. This SiNW FET model is reducing the complexity in design. Two types of the device geometries are studied by changing the silicon nanowire channel length as 1000 nm and 200 nm. The 1000 nm channel provides high penetration to the active region of the nanowire FET than the 200 nm channel. This silicon nanowire FET model can apply to many nanoscale biochemical elements sensing applications.

1. Introduction

In nanomaterials, one-dimensional nanostructures play a great role in the detection of biochemical elements due to their excellent sensitivity at the nanoscale level. Nanowires provide high surface to volume ratio for getting great sensitivity with the conduction pathways being very small [1, 2]. So, it can cross the level of the detection limits of planar ISFETs. Due to their higher surface to volume ratio and the efficient gate filed penetration, the backgated nanowire FET shows the higher transconductance 4-10 times above the classical standard ISFETs [3]. When using ISFET for biological sensing applications, the liquid environment also works as a local gate electric field. These changes in the field vary the surface potential that produces conductance changes in the channel. Compared to the planar ISFETs, the surface potential highly influences the conduction channel of nanowires. In general, single crystalline silicon nanowires are used with p- or n-type doping in conduction channel that creates charge carriers attracted or repelled by the attached charged biological element.

In the present study, the undoped silicon nanowire is used [4, 5]. It works with the Schottky barrier FET [6, 7]. The dopant-free single crystalline silicon nanowire is free

from impurities, and it provides higher performance compared to the doped silicon nanowires.

Growing semiconductor industry is requiring faster and smaller electronics for emerging electronics applications compared to the conventional MOSFETs. The one-dimensional nanostructures have the potential to meet the requirement of this field because the scaling theory makes the nanostructures decrease in dimension in nanoscale [8–10]. The FETs made from the nanostructures such as carbon nanotube [11, 12], graphene [13], and silicon nanowires [14] provide great electronic properties for the building blocks of nanoelectronic applications. Even CNT Schottky barrier FET shows the excellent electrical characteristics [15–17]; the chirality control of the CNT and the determination of the semiconducting or metallic behaviour are still problematic for their practical application. Silicon nanowires have the advantage of natural semiconduction and can be easily integrated into industry fabrication and processing while being compared with the other nanostructures like carbon nanotubes with metallic or semiconducting properties and graphene. While comparing with the conventional MOSFET channel, the silicon nanowire itself acts as a conductive channel, connected with the source and the drain contacts. Additionally, below the substrate, the nanowire can be used as a back gate, electrically isolated by a silicon dioxide insulator.

Silicon nanowire FET has various benefits than that of the CMOS devices. Silicon nanowire is expected to have high on-currents for three reasons.

(i) One-dimensional ballistic conduction of thin nanowires has less freedom for the carrier scattering angle [18]. Hence, its conduction would be high

(ii) Silicon nanowire FET uses multiquantum channels for conduction. The band structures of silicon nanowires are different from those of bulk silicon conductors, and many conduction subbands appear near the lowest subband [19]. These subbands cater to the conduction as the gate voltage increases

(iii) Multilayered nanowires can be implemented easily using Si/Ge multilayers [20–23]. This is a good production because the risk and cost of developing a new process technology get reduced

SiNW FETs take advantage of existing and developed silicon industry processing techniques and fabrications. In the engineered responses that prepare SiNWs, distinctive sizes, shapes, and dopants of SiNWs might be fully customized. Since SiNWs might be well controlled in the wire development, they have high reproducibility. In the same way, the n-/p-type semiconducting property, doping density, and charge mobility in a SiNW FET can be designed in advance. Additionally, the SiNWs provide benefits of smaller size and incorporating with the living systems or cells is simple without affecting the performance of the biological system. The intrinsic SiNW studies are very less [24–26]. Inclusive of all the studies, transport mechanism of undoped silicon nanowire Schottky barrier FETs is very few to understand. This creates interest to study the significance of the modelling of the dopant-free silicon nanowire Schottky barrier FET and its characteristics while the channel length is decreasing. In this article, the SiNW FET device model is designed. Electrostatic potential distribution studies with the various channel lengths are examined. Channel length of 1000 nm and the 200 nm silicon nanowire channels are used. This Silicon nanowire FET model is very important to determine the electrochemical properties of biosensors.

2. Device Model of Silicon Nanowire FET

The structure of silicon nanowire FET device follows generally three electrode system which consists of silicon nanowire channel placed in between drain and source electrode on a silicon dioxide (SiO_2) insulating substrate. The bottom silicon layer acts as the back gate, and it is split by insulating layer of SiO_2. With the change of small signal in gate field, there is a large variation in the conducting current in which the signal is amplified by the FET. Schottky barrier stands for the energy barrier between the band edge of the semiconducting material and the fermi energy of the metal. Its height is determined from the work function of the metal electrode. The Schottky interfaces considered in the study are nickel-silicide which can be designed by adding the Ni into the silicon nanowire. The undoped silicon nanowire FET shows p-type characteristics. Since they have different band bending properties based on the gate voltage, the Schottky contacts determine the type of the carrier.

Figure 1(a) represents 3-D device geometry, and Figure 2(b) represents the side view of the silicon nanowire FET device model which consists of conducting channel of silicon nanowire, and both the ends have the nickel-silicide ($NiSi_2$) contacts for the source and the drain contacts. The dimensions of the model for the source V_s, drain V_d contacts, length of the silicon nanowire channel, the thickness of the SiO_2 layer, and diameter of the nanowire are shown in Figures 1(a) and 1(b). The channel length of the semiconducting silicon nanowire is 1000 nm, and the diameter is 20 nm. Likewise, the length of the source and the drain contacts are 100 nm. The top of the layer is surrounding the air environment. Further, the thickness of the gate oxide insulator and the air environment are set to 300 nm and 100 nm, respectively. Gate, source, and drain electric potentials are applied to the respective contacts. The relative permittivity of the SiO_2 is 4.2, and that of silicon nanowire is 11.9.

3. Results and Discussions

3.1. Analysis of Electrostatic Potential in Silicon Nanowire FET. The Poisson equation indicates the relations between the electric potential and charge density. The electric field is produced with the divergence of the electric potential by solving the Poisson equation with the given boundary conditions and the surface charge distributions as given in

$$\nabla^2 V(r) = -\frac{\rho(r)}{\varepsilon_0 \varepsilon_r}, \quad (1)$$

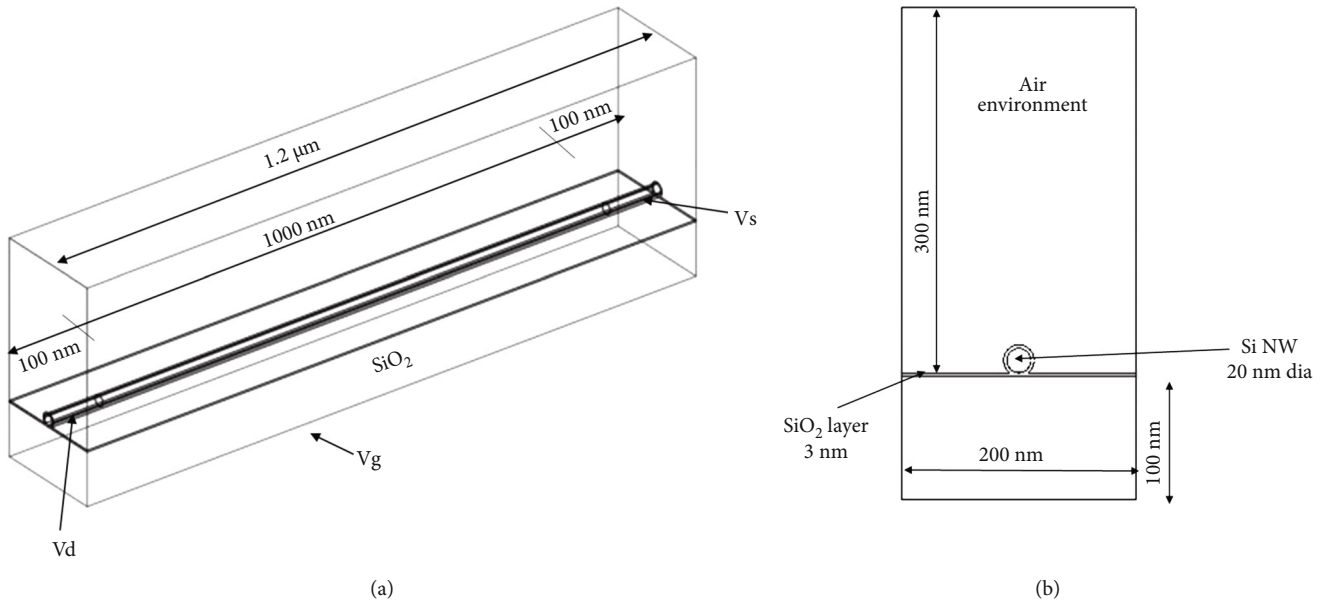

Figure 1: (a) 3-D geometry of the silicon nanowire FET. (b) 2-D side view of silicon nanowire FET.

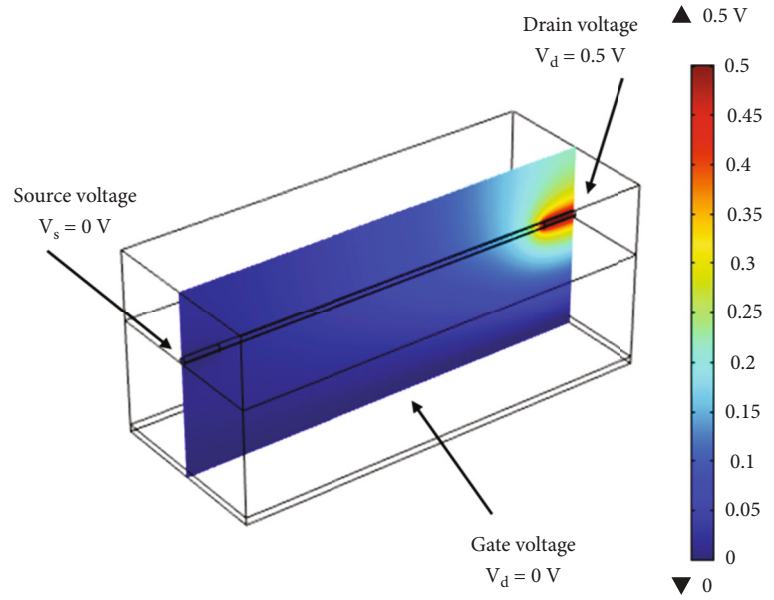

Figure 2: Electrostatic potential distribution for gate voltage 0 V and drain to source voltage $V_{ds} = 0.5$ V.

where ∇ is the divergence operator, $V(r)$ is the 3-D electric potential along the silicon nanowire axis, $\rho(r)$ is the charge density, and ε_0 and ε_r are permittivity of vacuum and relative permittivity or dielectric constant, respectively. After solving the Poisson equation with the use of finite element method from the 3-D electric potential, the 1-D electrostatic potential is taken along the silicon nanowire axis. Various boundary potentials are applied to the source, drain, and gate contacts, and the results are given in Figure 2. The finite element mesh of tetrahedral formulation for the model developed is generated automatically using the software. The electrostatic study starts with initially giving the electric potential from the drain to source voltage. Figure 2 shows the electrostatic potential distribution of the drain to source voltage $V_{ds} = 0.5$ V and gate voltage $V_g = 0$ V. The legend scale shows the applied potential variations for the corresponding colour changes.

3.2. Analysis of Electrostatic Potential on 1000 nm Channel SiNW FET. The one-dimensional electrostatic potential distribution of the silicon nanowire FET 1000 nm silicon nanowire channel is shown in Figure 3(a). The electric potential distributions at the gate voltage $V_g = 10$ V and drain source voltage $V_{ds} = 0.5$ V are applied. Electrostatic potential distribution for various gate voltages and the drain to source voltage for $V_{ds} = 0.5$ V and $V_{ds} = 0$ V is shown in Figure 3(b))

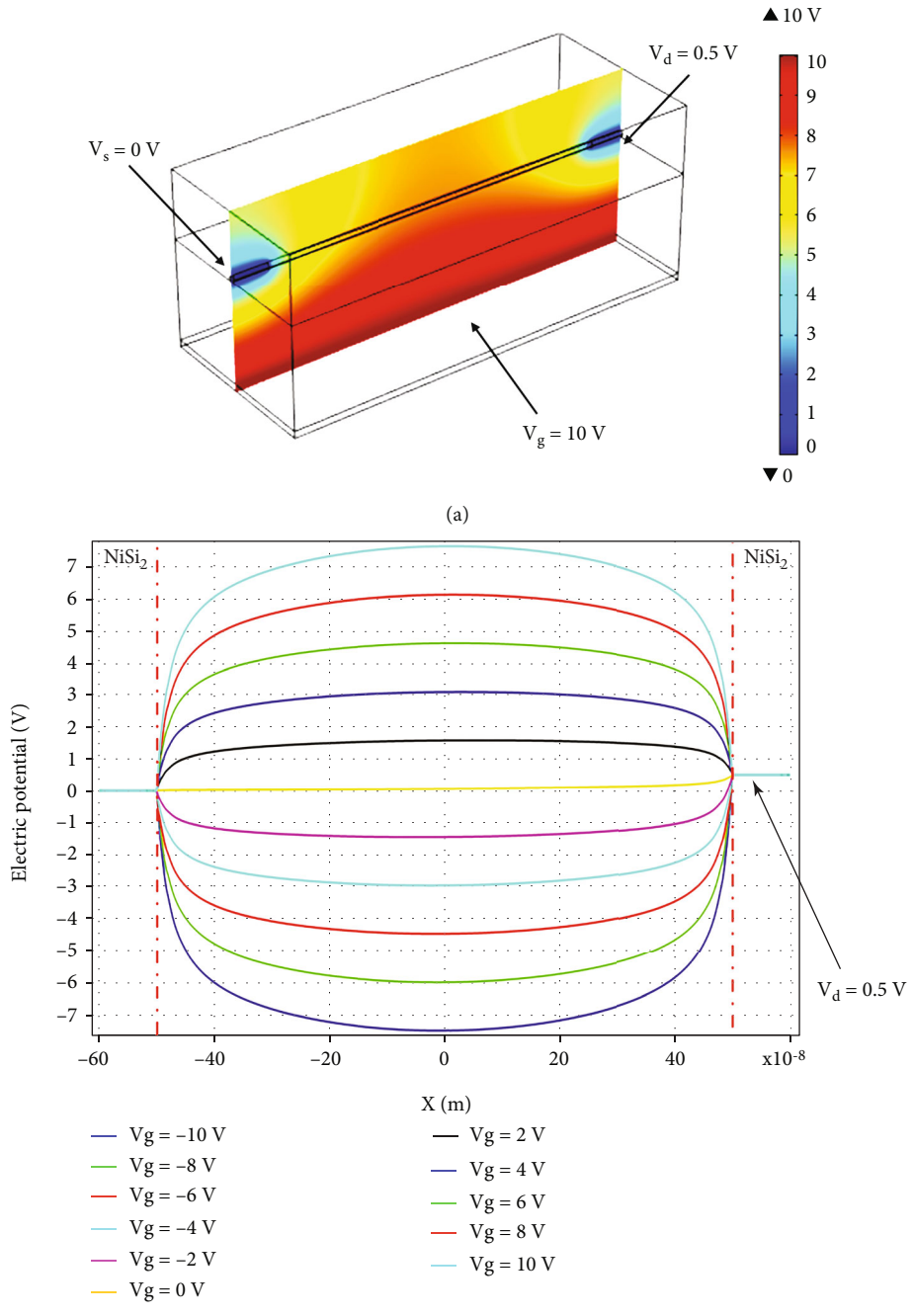

FIGURE 3: (a) Electrostatic potential distribution for the channel length of 1000 nm, gate voltage of V_g = 10 V, and drain to source voltage of V_{ds} = 0.5 V. (b) Representation of 1-D electrostatic potential along the 1000 nm silicon nanowire axis with V_g = −10 to 10 V and V_{ds} = 0.5 V.

The electrostatic potential distribution is measured along the silicon nanowire channel axis with the drain to source contacts. The gate voltage is varied from -10 V to 10 V. The one-dimensional electrostatic potentials along the silicon nanowire channel axis with various gate voltage values enable the calculation of the current through the channel of the device.

In the present model, the ballistic charge transport transmission is assumed by the silicon nanowire channel. This assumption can be accepted in the dopant-free channel if the length is equal to or less than 1 μm [6].

3.3. Analysis of Electrostatic Potential on 200 nm Channel SiNW FET. The one-dimensional electrostatic potential distribution of the silicon nanowire FET of the 200 nm silicon nanowire channel is shown in Figures 4(a) and 4(b)) Figure 4(a) shows the electric potential distribution at the gate voltage of V_g = 10 V with drain source voltage of V_{ds}

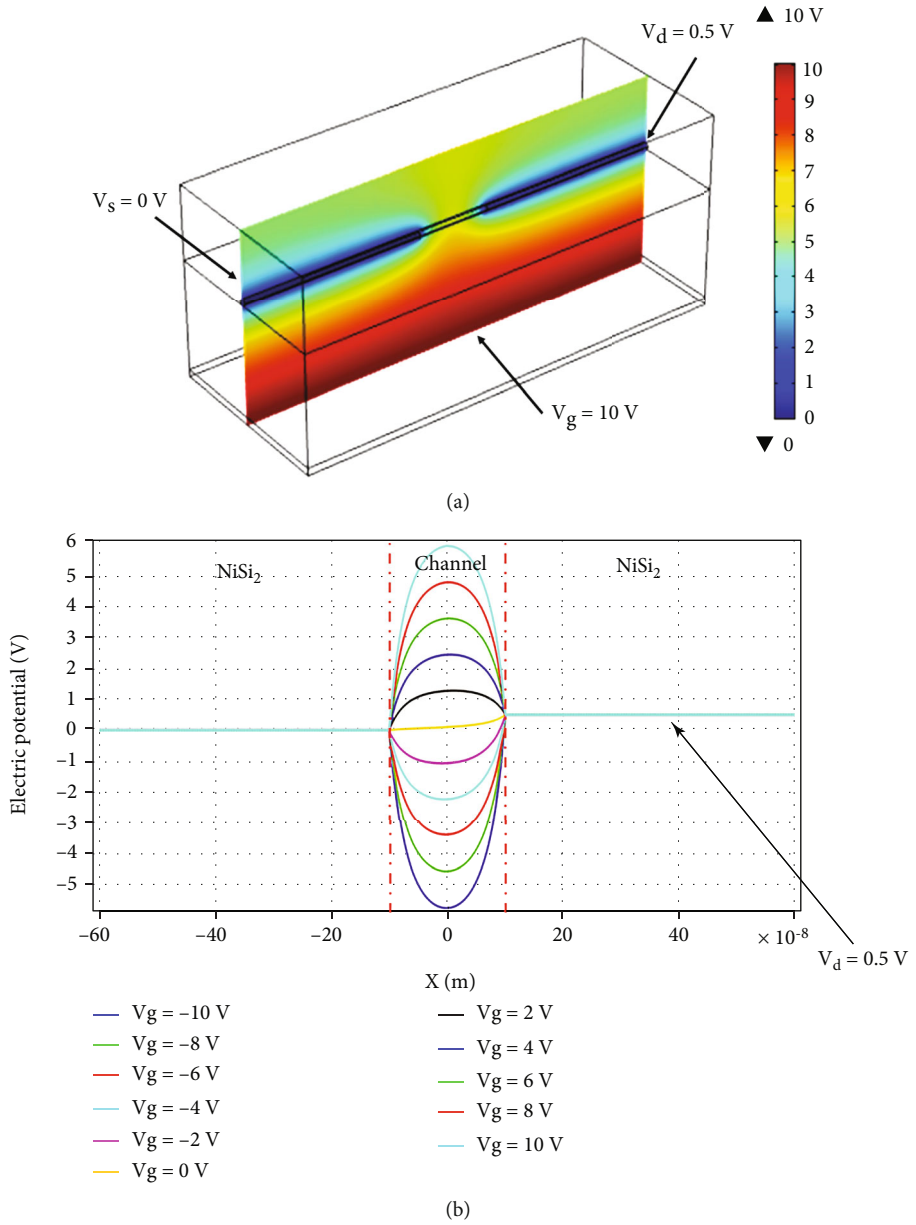

FIGURE 4: (a) Electrostatic potential distribution for the channel length of 200 nm, gate voltage of V_g = 10 V, and drain to source voltage of V_{ds} = 0.5 V. (b) Representation of 1-D electrostatic potential along the 200 nm silicon nanowire axis with V_g = −10 to 10 V and V_d = 0.5 V.

= 0.5 V. One-dimensional electrostatic potential distribution for the different gate voltage is shown in Figure 4(c). The electrostatic potential distribution is measured along the silicon nanowire channel axis with the drain to source contacts. The gate voltage is varied from -10 V to 10 V.

From the results of electrostatic potential analysis between 1000 nm and 200 nm silicon nanowire channels in the nanowire FETs, the 1000 nm silicon nanowire channel electric potential drop is higher than the 200 nm channel. From the results of Figure 3(b) and Figure 4(b)) the applied gate voltage highly penetrates to the active region of the 1000 nm nanowire channel, and in the 200 nm nanowire channel, the applied gate voltage cannot penetrate efficiently into the active region due to the short length of the nanowire. Thus, the gate control on the 200 nm silicon nanowire channel is highly weakened. From the studies, it can be understood that if the devices are shorter than 200 nm of the gate coupling to the contacts, the active region gets practically vanished.

4. Conclusion

Silicon nanowire FET provides the promising platform for building nanoscale electronic devices for biosensing applications. In this work, the silicon nanowire FET model is developed. Various electrostatic potential distribution studies are done using the Si nanowire FET. This model is promising in the complication design reduction. Two types of the device geometries are studied by changing the silicon nanowire channel length as 1000 nm and 200 nm. The 1000 nm

channel provides high penetration to the active region of the nanowire FET than the 200 nm channel. In the future, this silicon nanowire FET model and the device fabrication can be applied to determine the electrochemical properties of biosensors.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

On behalf of all authors, the corresponding author states that there is no conflict of interest. This study was performed as a part of the Employment of Authors.

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