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Research Article

Procedures and Properties for a Direct Nano-Micro Integration of Metal and Semiconductor Nanowires on Si Chips

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1-dimensional metal and semiconductor nanostructures exhibit interesting physical properties, but their integration into modern electronic devices is often a very challenging task. Finding the appropriate supports for nanostructures and nanoscale contacts are highly desired aspects in this regard. In present work we demonstrate the fabrication of 1D nano- and mesostructures between microstructured contacts formed directly on a silicon chip either by a thin film fracture (TFF) approach or by a modified vapor-liquid-solid (MVLS) approach. In principle, both approaches offer the possibilities to integrate these nano-meso structures in wafer-level fabrications. Electrical properties of these nano-micro structures integrated on Si chips and their preliminary applications in the direction of sensors and field effect transistors are also presented.

1. Introduction

Nanowires, that is, 1D metal and semiconductor structures, have gained immense research interest due to their potential role in the miniaturization of modern electronic devices, for example, sensors with improved responses, and so forth. Due to high surface-to-volume (S/V) ratio, nanowires exhibit extraordinary electrical features, and thus they have become the important components of micro- and nanoelectronic devices [1]. In the past few years, progress in the synthesis and characterization of nanowires is thus driven by the need to understand the novel physical properties of 1D nanoscale materials and their potential applications in constructing nanoscale electronic and optoelectronic devices [2]. As a result, the interest in 1D nano-microstructures has increased exponentially, and many synthesis techniques have already been disclosed to the scientific community in the last few years. However, understanding of the basic working principles and easy fabrications of nanowires are still under progress. One of the most challenging tasks is to integrate these 1D wires into device as one requires nanoscale connecting contacts. Possible options include an independent synthesis of nanowires as first step and then integrating them into the devices. However, it is more effective to perform direct fabrication of nanowires between the contacts on microstructured Si-chips. Various methods such as templates [3–5], solution growths [6], lithographic methods (electron beam and conventional) [7, 8], vapor-liquid-solid (VLS) and its modified versions [9–11], and several others have been employed to synthesize 1D structures. Many of these methods stated earlier are either too slow or too expensive when one looks from mass fabrication or market point of view. An optimal integration route should add minimal additional fabrication steps to the processes and has to be compatible either with the already structured circuits or allowing a further microstructuring of the circuit elements after the installation of nanostructures. In this paper, two direct integration recipes for metal and semiconductor nanostructures will be presented and discussed as well as their properties will be compared. One approach is based on a thin film fracture approach [12–14]; the other one is based on a modified vapor liquid solid process allowing bridging between the contacts through interpenetrating junctions.

2. Experimental: Fabrication of 1D Nano-Microstructures

The methods used here produce single- or polycrystalline nanostructures. In present work, two synthesis methods have been carried out which enable us for direct integration of nanowire structures into the micropatterned chips.

2.1. VLS and Modified VLS Approaches. The vapor-liquid-solid (VLS) or the vapor-solid (VS) processes are typically utilized to grow vertically aligned nanostructures such as nanorods, nanowires, nanoSails and nanocombs, and so forth. VLS growth process [15] can be performed in a simple tube furnace equipped with vacuum system and gas flow control. The needed recipes are the precursor material, catalytic nanoparticles, and the substrate on which structures will be grown. Experimental variants are temperature, gas flow rate, and relative distances between source and substrates. The precursor material, that is, ZnO powder, is mixed with graphite powder in appropriate ratio to adjust the Zn vapor pressure. Addition of graphite powder helps to reduce the decomposition temperature of ZnO via chemical reaction [16, 17]. The ceramic crucible filled with ZnO-graphite mixture is placed in the centre of the tube, and the substrates coated with catalytic particles are mounted both sides linearly at equal distances from the crucible along the tube axis in the tube furnace. The VLS growth process can be understood in the following 3 steps. (i) Heating the furnace above a critical temperature (>900°C), the ZnO: graphite mixture is transformed into Zn and CO vapor [18] and Zn vapor atoms are transported by the carrier gas (oxygen and Ar mixture) to the substrates carrying catalytic particles. (ii) Since the temperature of the substrates is higher than the eutectic melting point of the precursor material (Zn) and catalytic particles (Au) [19], Au-ZnO liquid alloy droplet is formed with the necessary oxygen utilized from the carrier gas. (iii) After supersaturation, the additional precursor material (ZnO) is continuously deposited at the bottom of alloy-droplet, and the droplet is lifted up due to capillary force. During cooling, the phase separation occurs resulting in formation of 1D rods with catalytic particles on the top [20–22]. In typical VLS process, temperature, amount of precursor material, size of catalytic particles, and the gas flow rate are the main controlling parameters for growth of 1D structures like nanorods, nanowires, nanoSails and so forth. The fabricated 1D nanostructures show various different growth directions resulting in different shapes of nanostructures ranging from nanorods to nanoSails, and so forth. Figures 1(a) to 1(d) show the nano-microstructures grown by conventional VLS approach in a tube furnace using gold nanoparticles (NPs) as the catalysts. In conventional VLS, catalytic Au NPs offer the main driving force for growth of ZnO structures, and they always remain on the top (circular marked regions) as can be clearly seen in Figures 1(a) and 1(d). It has already been emphasized that the size of Au NPs is an important parameter responsible for the geometry of ZnO nanostructures. When the diameter of gold NPs is relatively small, growth of ZnO nanorods occurs (Figure 1(a)) with NPs on the top; however, if the particle diameter is large enough formation of nanoSail type structures takes place as shown in Figures 1(b) to 1(d) with increasing order of magnifications. For instance, fabrication details of nanorods and nanoSails are described in our previous works [11, 23] whereas the corresponding electron microscopy images are shown in Figure 1.

Figures 1(e) to 1(g) demonstrate the SEM morphologies of different structures grown by modified VLS approach [24] without using the catalytic gold nanoparticles. Nanomast-type ZnO structures were reproducibly grown by MVLS approach and are shown in Figure 1(e). Different types of vertical standing ZnO nanowires (e.g., shown in Figure 1(f)) were also grown on different substrates by using MVLS technique. The working temperature in MVLS technique varies from 800°C to 1000°C, and more details about this are reported somewhere else [24]. In order to demonstrate the versatility of MVLS approach, experiments for growing nanostructures from other metal oxides were also performed, and successful results were obtained. For example, Figure 1(g) shows the SEM image of SnO_2 nanowires grown by MVLS approach.

Apart from the success of the conventional VLS process, several issues are still left undisclosed which motivated us to modify the VLS approach. We simplified VLS approach in terms of using simple muffle-type box furnace in air rather than tube furnace equipped with vacuum control. In modified vapor-liquid-solid (MVLS) approach [24], neither any catalytic particles are needed nor any substrate limitation is there; however, the relative output as well as degree of freedom for synthesizing different nano-meso-microstructures is higher. Several 1D nano-microstructures and their mesoscopic network can be synthesized in a reproducible manner by MVLS approach. Family of different structures have been found in a single growth process itself which could be an advantage for the device performance. Just for demonstration, we have shown some structures here; however, a detailed paper on the growth will be published elsewhere. In this work, our main focus is on a simple way to integrate such a type of nanostructure into Si-chips.

Various fabrication schemes exist to integrate 1D nanowires in Si-structures, for example, to utilize the large surface to volume ratio for a sensor, see [25–27]. All those fabrication schemes grow micro- or nanowires from one contact side to another side by utilizing several lithography steps. Furthermore, all approaches contain a certain statistics about how many bridges form between the contacts; see, for example, [27]. To simplify all those approaches to form a connection between two sides, we carry out growth from both contact sides in parallel and utilize those wires which interpenetrate in between the contacts. The connection formed by interpenetration is usually of high quality as only matching epitaxial directions allow a connection. Like the other approaches, our approach also relies on statistics; however, the following example shows that this does not mean a lack of control. The interconnection probability depends on the distance between the contacts, the length of the contacts, the density of the grown nanowire structures, and the thickness and length of the nanowires.

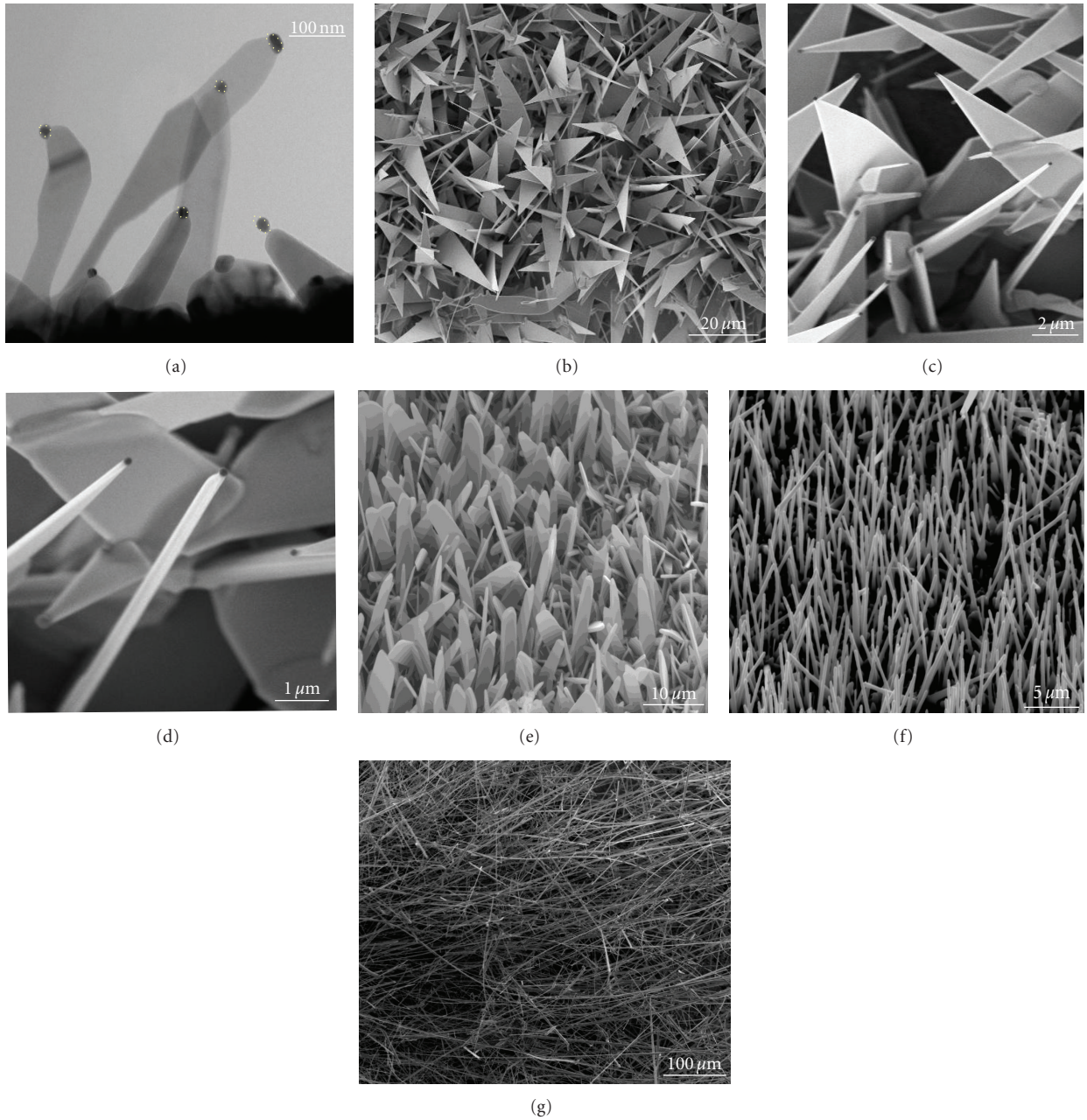

Figure 1: (a)–(d) show nanostructures grown by conventional VLS approach, (a) transmission electron microscope (TEM) image of ZnO nanorods with Au NPs on their heads (inside dotted circles); (b), (c), and (d) scanning electron microscopy (SEM) images ZnO nanoSails at different magnifications. The presence of Au NP on the top of nanoSail can be clearly seen in 1D (inside dotted circles). (e) and (f) show the structures grown by modified VLS approach [24] without any catalytic NPs: (e) ZnO nanomast structures, (f) ZnO nanorods, and (g) tin oxide nanowires.

An example on the smallest useful numbers of connections is with an average of 6-7 connections along the 200 μm wide contacts with an 8 μm gap. Estimating the statistics roughly from SEM analysis brings 80% of chips within a resistance variation of 25%. Doubling the contact length would bring 90% into 20% resistance variance. Longer contacts or higher wire densities further improve the statistic; however, a tradeoff has to be made between reliability and sensitivity, as the more the connections act in parallel the less sensitive the nanowire connection gets. Please see below an example of a UV sensor that shows the feasibility of the approach.

The advantage of MVLS approach over conventional VLS approach, however, is that the nanowires can be grown under ambient atmospheric conditions that one does not need special vacuum or gas environment specifications. Nanowires, for instance, have been directly grown on gold contact lines which were patterned on the 100 nm thick SiO_2-coated Si-chip. In contrast to the polycrystalline nature of the sputter deposited nanowires, the MVLS grown nanowires

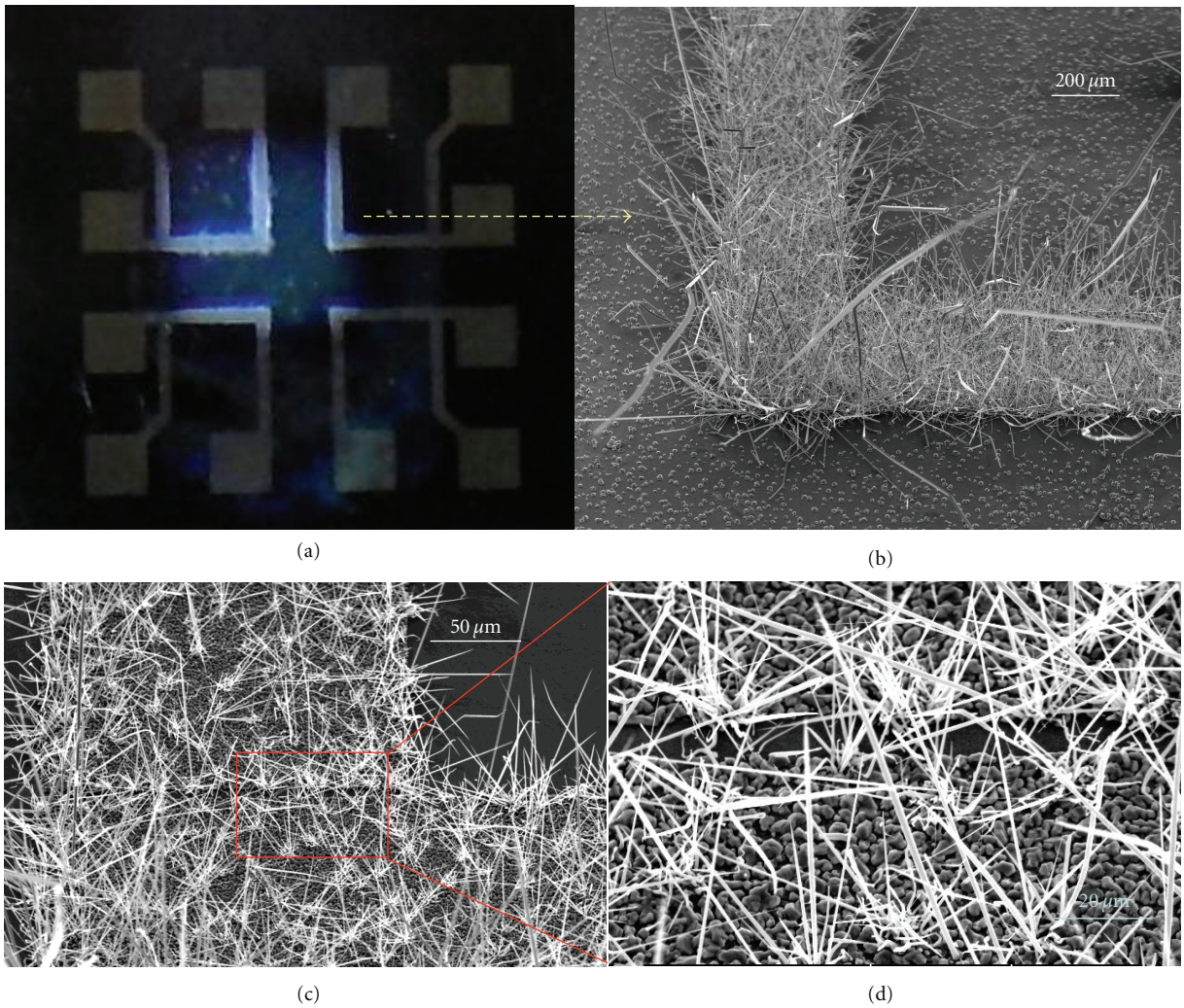

FIGURE 2: As-grown (a) optical image of 1D ZnO structures deposited area (white) where we have selective deposition around the 10 μm gap. SEM image (b) with high density ZnO nano- and microstructures, (c) relatively lower density networks on the contacts as well as within the 10 μm gap, and (d) magnified view of 10 μm gap part from (c) showing nanowires bridging between Au contact pads.

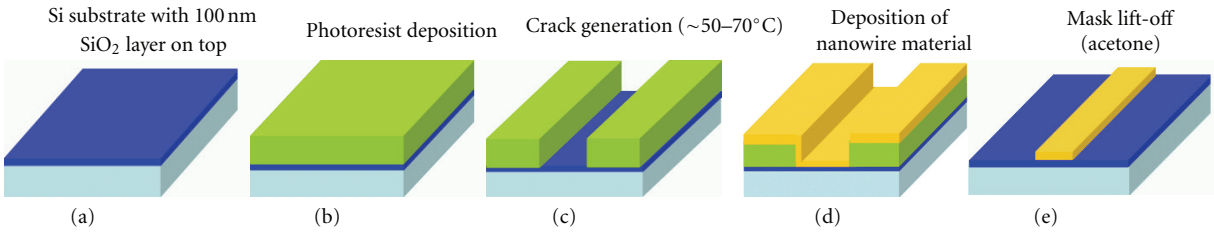

FIGURE 3: Schematic processes (a) to (e) involved in fabricating the nanowires by thin film fracture approach [12].

are exclusively single crystalline in nature with a variety of shapes which makes it similar to the conventional VLS. Many of oxide-forming materials such as Zn, Sn, Bi, and Fe have already been tested with MVLS approach, and the outcomes are very promising. Just for demonstration, growth of ZnO nanorods, at and between the 10 μm bridge between the gold contacts on the Si chip, is shown in Figure 2.

2.2. Fracture Approach. The main steps involved in thin film fracture (TFF) approach are described below in Figure 3. The photoresist is deposited (thickness varying from 550 nm to 1.5 μm) on the Si wafer which acts as a mask. The Si wafer with photoresist mask undergoes fracture (crack) formation process in which wafer is initially heated on the hot plate (~323 K to 348 K), and then it is subjected to quenching

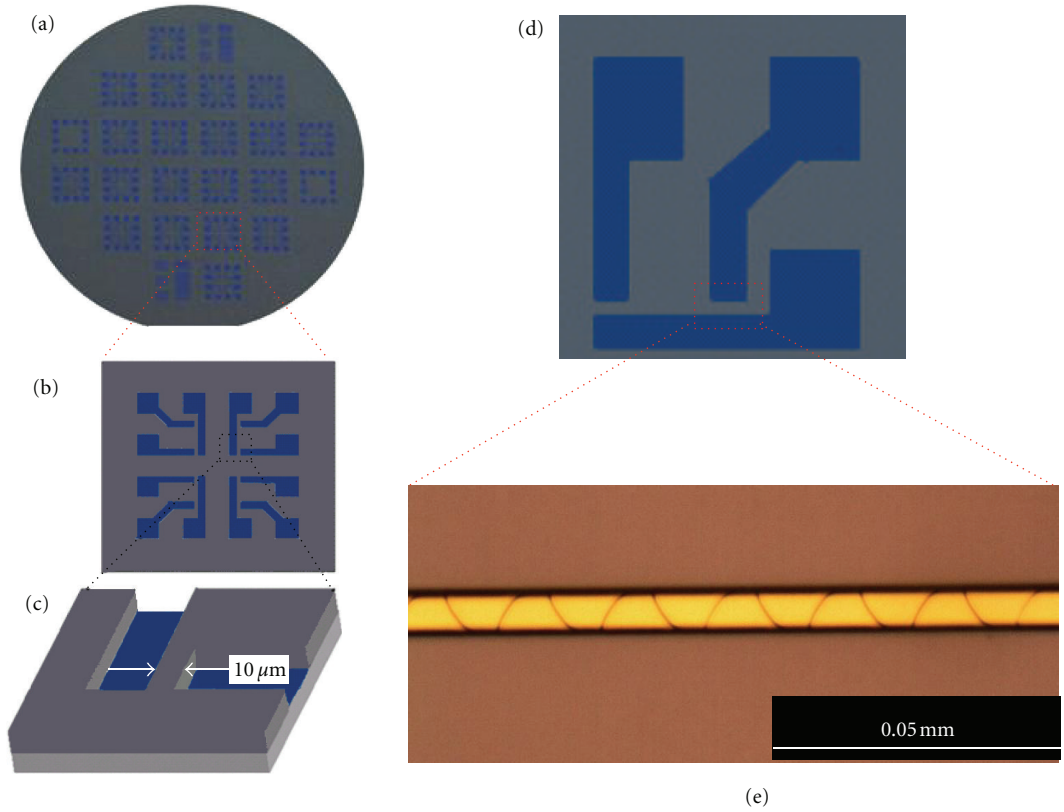

Figure 4: (a) Optical image of a microstructured photoresist film consisting of several microchips on a silicon wafer and a magnified view of a microchip. After UV lithography, each individual chip (b) consists of an open area for the later installed contact lines on the SiO_2 and a 10 μm wide rectangle of photoresist (c), where the nanowires will be installed. (d) Part of a chip cut from a chip design. (e) An optical micrograph of the 10 μm wide and 200 μm long photoresist after it is thermally fractured in liquid nitrogen—a periodic pattern of cracks occur. The cracks in (e) are observable optically as they are bended upwards because of the debonding of the resist from the substrate and causing it a delamination.

for about 5 seconds at cryogenic temperature (~77 K) using liquid nitrogen. As the result of difference in the coefficient of thermal expansion between the resist and the substrate, the drastic thermal shock creates fractures everywhere on the resist, but most importantly it creates well-patterned fractures on a 10 μm by 200 μm wide resist.

Following fracture formation is deposition. The material of interest as a nanowire is then deposited over the entire area of the wafer with fractured resist. A mask lift-off is then performed ultrasonically in acetone bath to lift the resist off the substrate. The undesired material covering to top of photoresist is also lifted off together with acetone leaving behind the nanowires of material within the cracks. The photoresists are mainly two types (i) positive and (ii) negative, and depending upon the requirement, a particular photoresist can be used. Till now we have successfully produced the desired cracks in controlled manner using positive photoresist; however, experiments about the utility of negative photoresist are under progress and will be published elsewhere. As already discussed above, the photoresist can be turned into a shadow mask after thin film cracks are produced in the microstructured photoresist. Depending on the dimensions of the photoresist on the substrate, different shapes of self-organized zig-zag cracks can be generated. In present case the cracks are formed in a rectangular strip of 10 μm width, 200 μm length, and ~700 nm height in the photoresist when the sample is quenched at cryogenic temperature (~77 K) after annealing the wafer to 55°C for 5 minutes. Figure 4 demonstrates a typical example of fractures formed in the 10 μm resist width on an Si wafer with TFF approach.

Commercially available Si wafer (~4 inch in diameter) was patterned by UV lithography and is shown as Figure 4(a). A magnified view of each pattern (1×1 cm^2) from Si wafer is depicted in Figures 4(b), 4(c), and 4(d) show the side view and the top view respectively from a magnified portion from Figure 3(b) where self-organized fractures are formed. Figure 4(e) is the optical micrograph image of cracks formed from fractured resist in a simple experiment.

The exact position of individual cracks can be precisely controlled, if they are confined by the lithographically produced microstructures. Depending on the thickness of the photoresist, cracks can propagate in straight line or follow curved paths or even some times lambda- (λ-) shaped cracks can be formed in the in lithographically confined position. The process has been performed at a wafer

Table 1: Summary of the TFF approach: Success statistics for a 10 μm sized gap width of resist. From approx.100 chips, 80 were fabricated with a 100% success rate at the optimized photoresist thickness between 850–1200 nm.

Thickness of photoresist	Crack formation (TFF approach)	Crack formation after oxygen plasma etching
≤550 nm	<50%	no
600 nm	>75%	no
650−850 nm	100%, straight and some times λ shaped	no
850–1200 nm	100%, bow shaped cracks	no
≥1200 nm	100%, bow shaped and strongly bended cracks, but delamination of the photoresist takes place	no

level, and the reproducibility has been proved for at least thousands of wafers. The formation of cracks with respect to the thickness of photoresist and influence of oxygen plasma treatment is summarized in Table 1. The treatment with oxygen plasma (ion) is a standard method to reduce the resist thickness. In this case it has a negative effect on the TFF approach, as it results in more branching in the polymer chains of the photoresist. This could enhance the crosslinking and entangling of the polymer chains which makes the bonds to be stiff for fracturing. Thus any oxygen plasma treatment will result in a more stiff photoresist which was the main reason to avoid the plasma etching of the resist as the final aim was to obtain fractures. It has been clearly observed that, when the thickness of photoresist is less than ∼550 nm, crack formation probability is less than 50%. With increase in thickness from 550 nm to 600 nm, the crack formation probability increases up to ∼75%. With photoresist thickness in the range of 650 nm to 850 nm, crack formation probability reaches maximum value. Individual cracks appear to be straight but the overall orientation of cracks being zig-zag. Some times λ-shaped cracks are also formed. It appears that critical value of photoresist thickness lies on average 750 nm as at this value, the crack formation probability is 100%, and with further increase in thickness beyond 750 nm crack probability is maximum and different shapes of cracks are formed. However, formation of crack disappears after plasma treatment (etching) for all thicknesses. If the width of the resist is other than 10 μm size, cracks of various shape and orientation could be the result.

As it has already been mentioned above that following the formation of cracks (fractures) is vacuum deposition of the nanowire material, both the electrode and the nanowire materials are deposited in single deposition process which makes this method easy and cost effective and also ensures a reliable contact between the nanowires and the electrodes. However, if it is necessary, with an additional deposition step, it is also possible to have different materials for contacts and nanowire structures. In this process step, the sample is tilted towards the deposition source. Due to the high aspect ratio of 8–10 of the fracture lines, no material penetrates to the bottom of the cracks, but the microstructure openings for the contact lines are filled with material. Subsequently a second nanowire-forming material can be deposited from top. The cracks which are employed here thus form an ideal shadow mask. Typically they have a width in the order of ∼100 nm and a depth all the way through the photoresist, resulting in aspect ratios of 5–10, depending on the used resist thickness. A resist film that is too thin does not allow a crack formation due to an insufficient amount of stress in the film during cooling, also a too thick film does not allow as it results in too much stress and a partial delamination of resist flakes. However, by changing the deposition angle, the width of the fabricated nanowires can be controlled independent of the crack width. Note that the height of the nanowire is below the nominal deposition thickness and below the height of the surrounding microstructures on the substrate as the steep walls of the resist masking already a part of the deposition source. After shadow mask liftoff in acetone bath, the electrode and the nanowire adhere to the substrate.

The nanowires produced by fracture approach using vacuum deposition are found to be polycrystalline with grainy features as shown in Figure 5. The inset in the figure shows grains of different size. This makes such kind of nanowires ideal for sensoric applications since the grain boundaries play crucial role in sensing. For instance, Favier et al. [28] have shown that palladium nanowires are excellent hydrogen sensors. The sensing quality originates from grainy structure of the nanowires which changes their electrical conductivity as a result of change in the nanogaps between the grains. The Pd nanowires were fabricated by the fracture approach which can also be used for hydrogen detection [29].

The fabrication of semiconductor nanowires demonstrated here follow either of two routes: (1) direct RF sputtering of semiconductor material or (2) sputtering of metal first followed by electrochemical anodization. One of the semiconductor candidates which was RF sputtered from a sputter target is ZnO. As deposited, both the ZnO film and/or NW sputtered at 40 Watt, 10^{-6} mbar chamber pressure, showed electrically insulating behaviour. However, after annealing the prepared nanowire samples above 400°C for about 1 hour in normal ambient, they showed electrical conductance which is a clear indication of microstructural change. The correlation between annealing conditions and the physical structure of the films (crystalline structure and microstructure) was investigated by X-ray diffraction (XRD) and atomic force microscopy (AFM). The XRD results on the annealed film showed that *c*-axis preferred orientation which is preferred growth direction of ZnO because of its hexagonal wurtzite crystal structure.

Sputtering of low layer thickness or small amount of semiconductors like ZnO is believed to come up with columnar Volmer Weber-type of growth or separate islands. The AFM image given in Figure 6(a) shows that the as-deposited ZnO film is quite rough which one possibly compares to the schematic in Figure 6(c) with a columnar microstructural growth with possible spacing among columns. Postdeposition annealing has resulted in remarkable changes in the microstructure as shown in Figure 6(b), and the film has been found to be dense and smooth beside a few larger tips and electrically conductive for which the

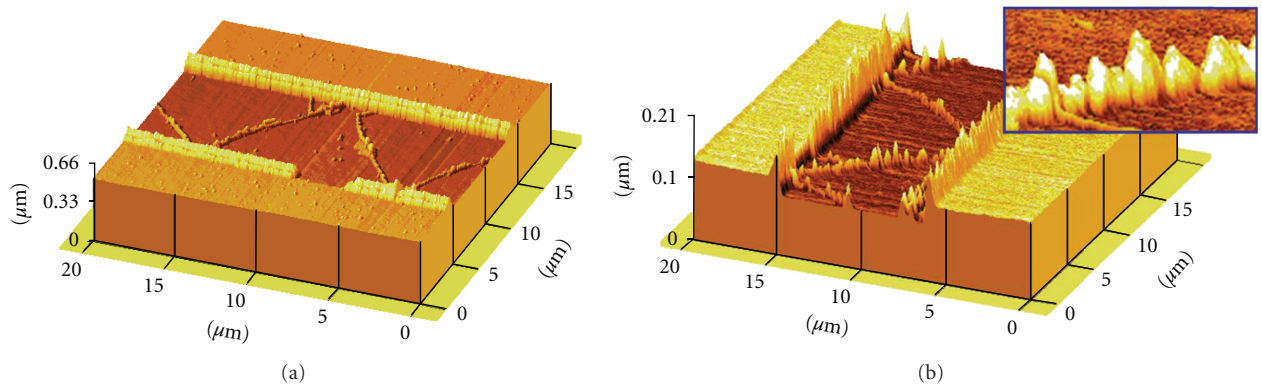

FIGURE 5: AFM Image of zig-zag-oriented (a) Ti nanowire and (b) Pd nanowire. The inset in (b) illustrates grainy features of the nanowires. Note that the z-scale is drastically overemphasized.

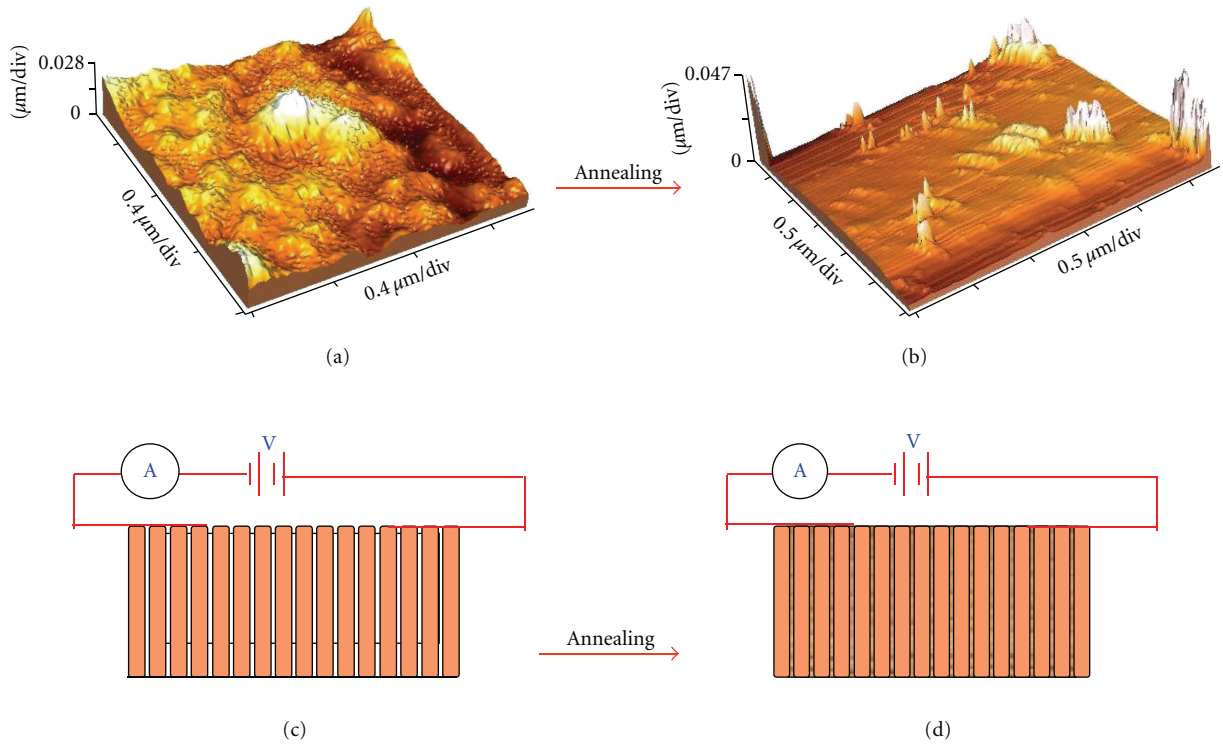

FIGURE 6: (a) AFM images of as deposited 50 nm ZnO thin film, (b) annealed at 400°C for 1 hour. Schematic views of ZnO thin film before (c) and after annealing (d).

microstructure cross-sectional view might be compared with Figure 6(d). Similar results were also reported by Chu et al. [30], although our samples were annealed under ambient atmosphere condition. The observed electrical conductivity is thus believed to come from islands interconnections which occur after post deposition annealing (the measured electrical conductivity curves before and after annealing of nanowires are shown in the discussion part in Figure 8(a)).

The other route for the fabrication of oxide semiconductor nanowire structures is to start from a metal nanowire followed by electrochemical anodization. Thin film fracture approach has also been used here for fabricating the nanowire. After fabrication of a networked crack structure, 70 nm thick Ti was deposited where the nanowires are located on a 100 nm SiO_2 and are anodized with 10 V for 10 minutes. The I-V characteristics before and after anodization are demonstrated in Figure 7.

From the linear I-V response, it can be observed that the resistance is increased from 0.076 MΩ to 217 MΩ after anodization, which is close to the resistance regime where electron tunneling can possibly be involved. The anodized nanowires exhibit several types of electrical conductivities,

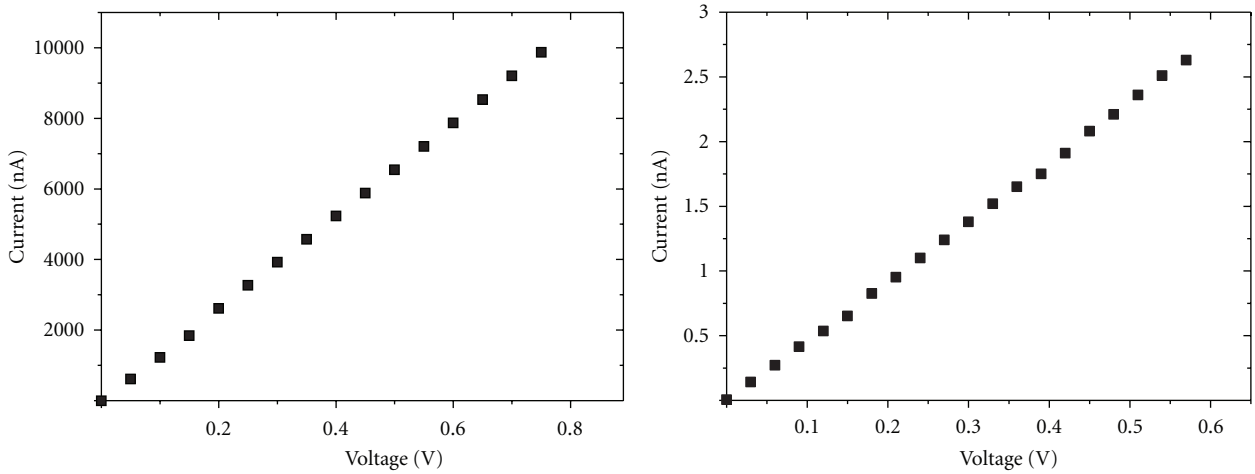

Figure 7: I-V characteristics (a) before anodization and (b) after anodization. The resistance increases from 0.076 MΩ to 217 MΩ.

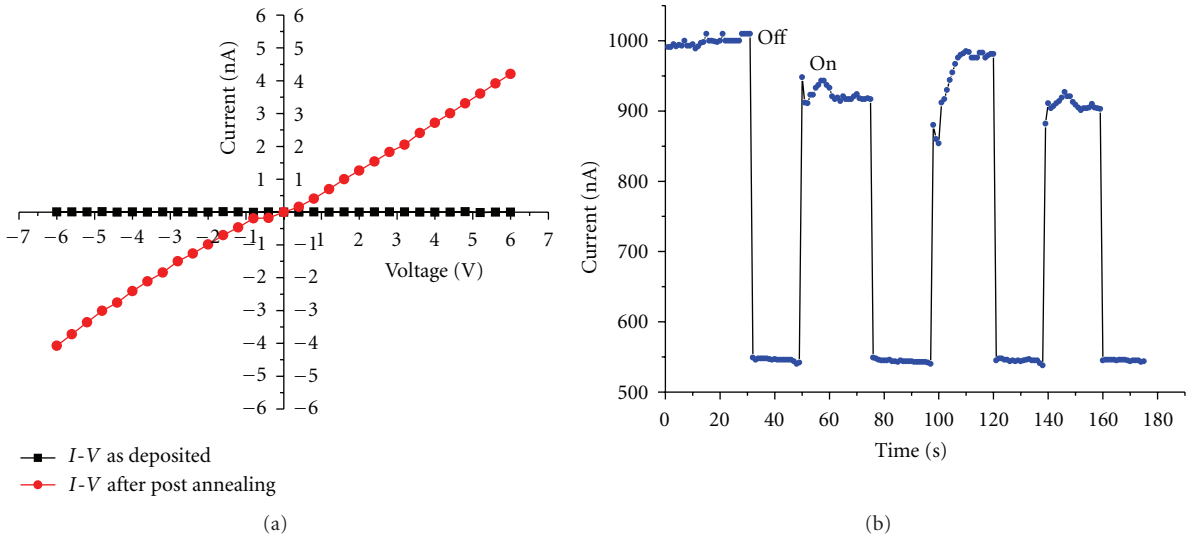

Figure 8: (a) Electrical conductivity of as-deposited and annealed (at 400°C-1 hr in air) 50 nm thick ZnO NW. (b) Current-time switching cycles curve at constant voltage of 2 V under UV illumination.

and the explanation for possible mechanisms or reasons for these variations are discussed in details in our previous paper [31].

3. Results and Discussion

Mainly we have demonstrated the fabrication and growth of metal and semiconductor nanowires by conventional and modified VLS approaches as well as by a thin film fracture approach here. The main intention was to integrate these nanowires on the chip with gold contacts for direct applications in electronic devices or sensor measurements. In the following section, we demonstrate the electronic characteristics of ZnO nanowires, anodized Ti nanowire field-effect transistors (NWFET), and sensor applications.

3.1. UV Photoresponse of the ZnO Nanowires. The UV photodetection of the ZnO nanostructures fabricated under the two approaches [12, 24] was measured under ambient condition (shown in Figure 8). The ZnO nanowires showed reversibly and rapidly switching of conductivity states. As the measurement was performed under open air condition, oxygen is adsorbed on the ZnO surface. Upon illumination with 365 nm UV lamp, the conductivity has increased as it is evidenced by the current versus time characteristics at a constant voltage supply.

Photons of energy greater than the bandgap will generate electron-hole pairs. According to Soci et al. the photogenerated holes migrate to the surface and are trapped, leaving behind unpaired electrons in the NW that contribute to the photocurrent [32]. The normal I-V responses and current

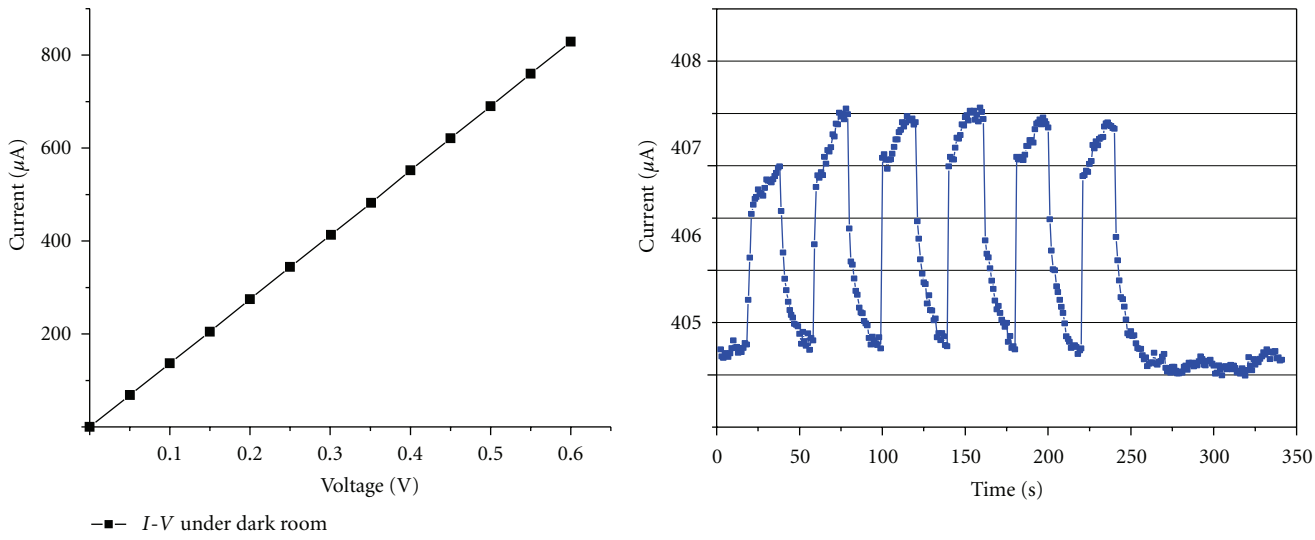

FIGURE 9: I-V characteristics of ZnO nanowires on chip fabricated by MVLS approach in dark (a) and the corresponding current-time switching response (b) under UV light illumination at constant voltage of 0.3 V.

switching in the ZnO nanowires synthesized by fracture and MVLS method are demonstrated in Figures 8 and 9, respectively. The holes then neutralize the chemisorbed oxygen resulting in increasing the conductivity as shown in Figures 8(b) and 9(b). When the UV light is turned on and off, the increase or decrease in photocurrent takes a time to reach to the saturation. This phenomenon is less pronounced in the case of nanowires produced under fracture approach as shown in Figure 8(b).

The photoresponse of the ZnO nanowires grown in fracture approach under 2 V applied voltage and up on illumination in Figure 8(b) shows the photoresponse is much faster than that of measured for ZnO micro- nano wires grown by modified VLS counterpart as shown in Figure 9(b). The reason would likely be the reduced influence of the surface states seen in that material in the case of modified VLS (MVLS) approach. Because we have got a combination of high-density nanowire networks connected in the MVLS approach in which the surface to volume would be smaller as compared to the fracture approach. Similar results have been reported by Pearton et al. [33].

3.2. Gas Response of the Anodized Titanium Nanowire FET. Before applying a gate bias voltage, the insulating behavior of the back gate was checked by connecting one electrode to gate (P^{++} Si) and the other electrode to drain and ramp voltage from 0 to 3 volts. The applied gate voltage was limited to 3 volts in order to avoid the breaking of the dielectric property of the oxide layer in the nanowire chip. Again in order to be sure that there is no leakage current through oxide, current measurements at several places on the oxide layer were performed, and almost zero leakage current was observed every time. However, there were positions where we observed a resistance in the order of 300 MΩ which might be due to the inhomogeneities in oxide layer thickness (thermally grown oxide layer supplied by Active Business Company GmbH, Munich). Those positions on the chip are excluded from further measurements. A bottom gate voltage was applied for the anodized Ti nanowire, and corresponding curves are shown in Figure 10(a). As the plot (Figure 10(a)) depicts, there is a high increase in source-drain (I_{sd}) current when a bottom gate-source voltage is applied (V_{gs}). In order to show the almost symmetric nature of current behavior in both forward and reverse directions, we have shown a magnified plot in Figure 10(b) corresponding to zero gate-source bias voltage. To demonstrate the increase in current due to applied gate bias, the logarithmic plots corresponding to Figure 10(a) are shown in Figure 10(c) which reveal that drain current is increased by more than two orders of magnitude. The increase in drain current indicates that the nanowires are n-type [34] as the conductance has increased by depleting electrons from the oxide. The transfer characteristics of the anodized Ti nanowire corresponding to different source-drain voltages are shown in Figure 10(d).

The observed field effect behavior might be used to shift the nanowire-operated devices, for example, as sensor, into a sensitive region of its conductivity curve. The TiO_2 nanowire FET, however, showed a drastic and fast response in the drain current when it is exposed to different pressures of oxygen (Figure 11). The reduction in drain current under the exposure of oxygen is believed to be the result of adsorption of O_2 at oxygen vacancy sites forming O_2^- and O^- through depleting electron from titania.

The FETs exhibit properties which are already suitable for applications as sensors. Thus the gas detection experiments were performed with nanowires synthesized with the help of the fracture approach. For comparison, Pd nanowires showed a drastic change in the conductance when exposed to H_2, but the anodized Ti nanowires showed no change in the conductance when the nanowires are exposed to

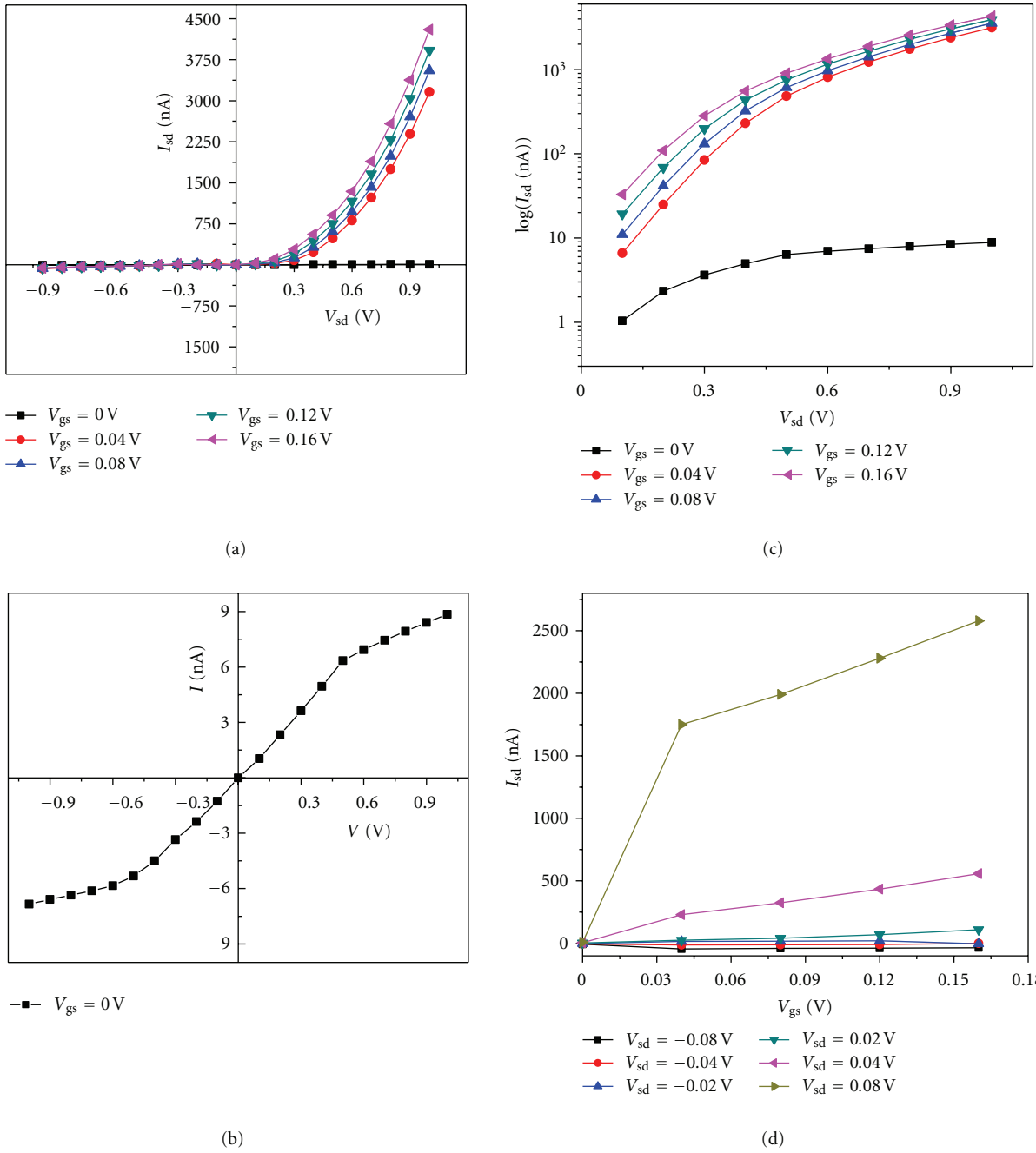

Figure 10: (a) I_{sd}-V_{sd} characteristic of anodized Ti nanowires as a NWFET, (b) the magnified I_{sd}-V_{sd} plot for zero gate voltage in forward and reverse bias, (c) logarithmic plot corresponding to (a), (d) transfer characteristics of nanowire-FET at different source drain voltages (V_{sd}).

H_2. The FETs produced possess properties already suitable for applications as sensors. In this context the gas-sensing capabilities of Pd and anodized Ti nanowires synthesized under fracture approach were also tested which are shown in Figure 12. Pd nanowires showed a drastic change in the conductance when exposed to H_2, but the TiO_2 nanowires showed no change in the conductance when the nanowires are exposed to H_2 as shown in Figures 12(a) and 12(b), respectively.

4. Conclusions

We have demonstrated two different routes for the micro-nano integration of metal oxide semiconducting nanostructures into Si microchips. Both routes allow the integration of nanowires and are in principle ready for upscaling; however, they both are best with individual advantages and disadvantages. The modified VLS type of growth on already existing current lines requires relatively high temperatures

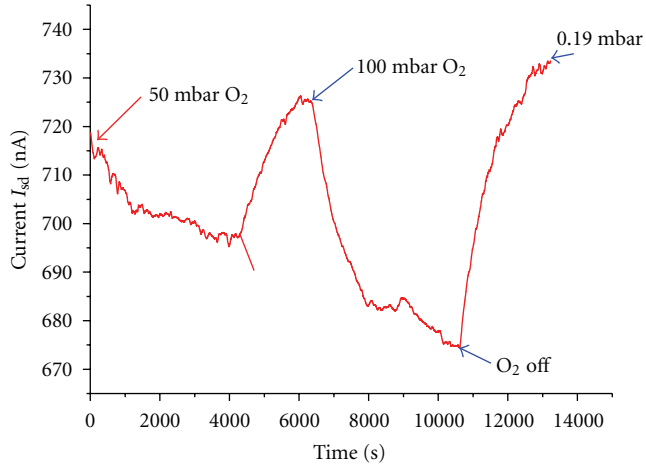

Figure 11: Sensing response of anodized Ti NWFET at different partial pressures of oxygen. A pronounced answer is visible.

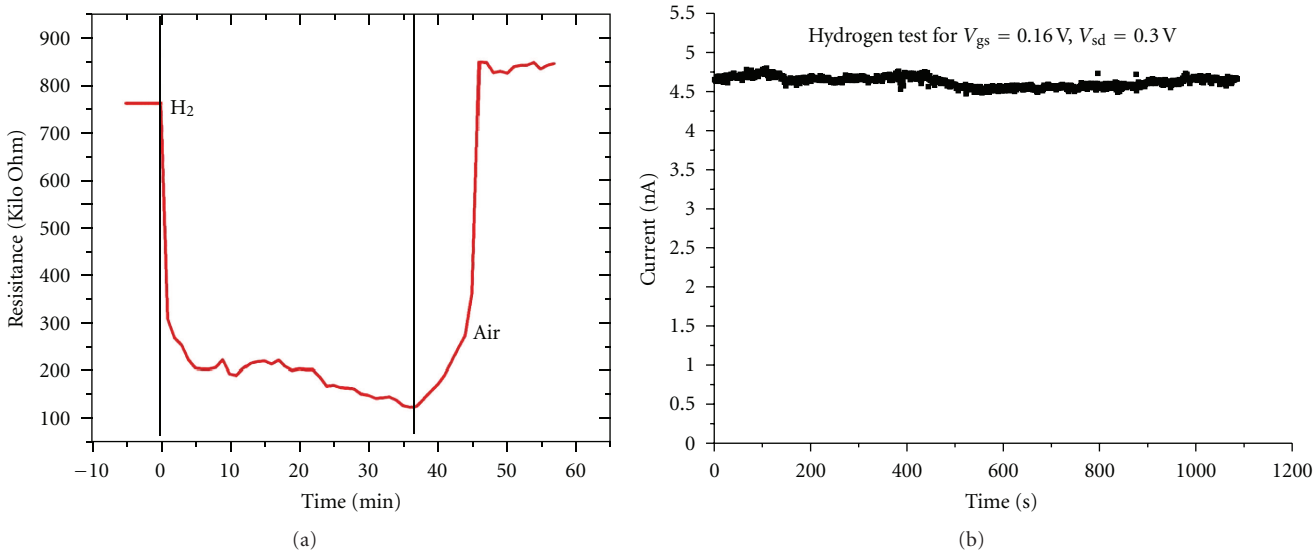

Figure 12: Comparison of sensor properties at H_2 containing atmospheric environments. (a) Palladium nanowire as hydrogen sensor, comparison [29], shows a pronounced answer in terms of increased conductivity. (b) The anodized Ti nanowire FET shows no response to hydrogen.

and therefore need an active cooling of the wafer during fabrication if circuit elements are already structured. On the other hand the approach allows an integration of a 3D network type of structure which might be interesting for sensors that are in touch with a medium like fluid or gas sensors, a housing could allow direct accesses of the media to the network but shield the rest of the electronics. First tests with ZnO nanowires and UV-light show a delayed response of the single crystalline nanowires compared with the polycrystalline nanowires fabricated with the fracture approach, probably due to the larger surface-to-volume ratio of the sputter deposited ZnO wires. The fracture approach allows a simpler integration; it requires only one additional step for the photoresist preparation. However, a simple straight forward sputter deposition can be insufficient to achieve a desired nanowire formation—; or example, experiments with the deposition of ZnO teach that a postannealing step must be carried out in order to obtain a nanowire of interconnected grains. Alternative heating can be avoided by depositing a metal first and carrying out an anodization to turn the metal into an oxide nanowire. The example of anodized Ti nanowires fabricated in this way allows the formation of a bottom gate field-effect transistor. Furthermore, the anodized titanium can serve as oxygen-sensitive element; it has already a selectivity towards hydrogen. In summary, several integration routes for nanowires are possible that can be carried out with standard processes and without E-beam lithography, focused

ion beam methods, or alignment processes for already prepared nanowires that are unlikely to allow a wafer level processing. For a final demonstration of the feasibility of the here suggested methods, a wafer-level processing should be carried out. The first tests of sensitivity are promising to allow the nanowires to serve in sensors; however, for a nanowire sensor a control electronics should be integrated, for example, for sensor drift correction and selectivity, as well as long-term stability tests have to be carried out.

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