

## Research Article

# Flat-Top and Stacking-Fault-Free GaAs-Related Nanopillars Grown on Si Substrates

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The VLS (vapor-liquid-solid) method is one of the promising techniques for growing vertical III-V compound semiconductor nanowires on Si for application to optoelectronic circuits. Heterostructures grown in the axial direction by the VLS method and in the radial direction by the general layer-by-layer growth method make it possible to fabricate complicated and functional three-dimensional structures in a bottom-up manner. We can grow some vertical heterostructure nanopillars with flat tops on Si(111) substrates, and we have obtained core-multishell Ga(In)P/GaAs/GaP nanowires with flat tops and their air-gap structures by using selective wet etching. Simulations indicate that a high-Q factor of over 2000 can be achieved for this air-gap structure. From the GaAs growth experiments, we found that zincblende GaAs without any stacking faults can be grown after the GaP nanowire growth. Pillars containing a quantum dot and without stacking faults can be grown by using this method. We can also obtain flat-top pillars without removing the Au catalysts when using small Au particles.

## 1. Introduction

Free-standing nanowires are promising for future nano-scale devices. The VLS growth method enables us to make quantum structures in nanowires, which will contribute to the development of nanodevices such as transistors [1], nanolasers [2], and nanosensors [3]. The VLS mechanism was first proposed for Si whiskers by Wagner and Ellis in the 1960s [4]. Later, after the encouraging studies on light-emitting diodes using nanowires by Hiruma et al. in the 1990s [5], many studies of semiconductor nanowires aiming at the production of functional devices have been reported. The VLS mechanism is similar to liquid-phase epitaxy but is driven catalytically in the nanoarea by nanosized particles of a metal such as Au. This feature is very useful from the viewpoint of reducing growth time and the consumption of both power and source materials for industrial fabrication. Moreover, VLS growth is suited for application to Si-based optoelectronic integrated circuits (OEICs) because it enables to connect various III-V materials and is performed at low temperature. As already demonstrated by several groups, vertical GaP nanowires can be grown on Si(111)

without dislocation at the interface between the nanowire and the substrate [6–8]. One of our future plans is to make nanolasers on Si substrates. The number of quantum dots can be defined in one pillar by the VLS process, which makes it easy to access quantum dots in an optical manner. And we believe that VLS growth is the most promising technique for realizing nanodevices by means of a fully bottom-up process in the future. We have recently reported core-multishell nanowires with flat tops and shown that air-gap structures can be formed just by using selective wet etching [9, 10]. These structures were grown by combining the VLS growth and MOVPE (metalorganic vapor phase epitaxy). Our fabrication methods are in general bottom-up approaches. In this paper, after briefly explaining the fabrication procedure and characterization methods, we first describe core-multishell nanowires with air gaps and show the possibility of photonic crystal (PhC) devices using nanowires. Next, we report stacking-fault-free GaAs nanopillars using GaP nanowires on Si. We show that zincblende GaAs can be formed over GaP nanowires without any stacking faults, which will lead to refined heterostructures and band engineering. A technique for removing Au particles helps us form pillars with flat tops,

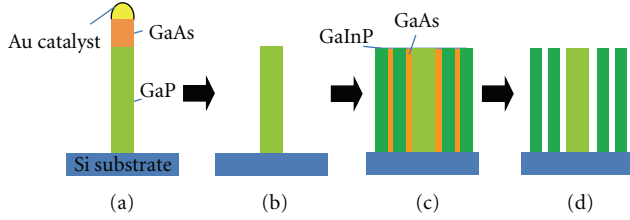


FIGURE 1: Cross-sectional schematic images of core-multishell nanowires with air gaps explaining the fabrication process. (a) GaAs/GaP nanowires on Si(111); (b) GaP nanowires after Au/GaAs removal; (c) alternated GaAs/GaInP shell growth at high temperature; (d) after removal of GaAs for air gaps.

which are very suitable for light propagation. Finally, we introduce an interesting phenomenon: the formation of flat-top nanowires achieved by using small-sized Au particles in only one growth procedure.

## 2. Experiments

The wire growth was carried out in a low-pressure (76 Torr) horizontal MOVPE reactor [7–10]. Trimethylgallium (TMGa), trimethylaluminum (TMAI), and trimethylindium (TMIn) were the group III sources. Phosphine ( $\text{PH}_3$ ) and arsine ( $\text{AsH}_3$ ) were the group V sources. The catalysts were Au particles obtained from Au colloids (5, 10, 20, and 40 nm in diameter).

First, GaP nanowires were grown on Si(111) substrates in two steps [7]. A small amount of GaP was grown for 5 s at  $550^\circ\text{C}$  by introducing TMGa of  $4.8 \times 10^{-6}$  mol/min and  $\text{PH}_3$  of  $4.5 \times 10^{-4}$  mol/min. Then, the remaining GaP wire growth was performed at  $480^\circ\text{C}$  by introducing the same source gasses. This two-step growth increased the probability of vertical nanowires.

Figure 1 shows the fabrication procedure for core-multishell nanowires with air gaps [10]. For core-multishell GaInP/GaAs/GaP nanowires, the flow rates of TMGa and  $\text{AsH}_3$  or  $\text{PH}_3$  were  $9.5 \times 10^{-6}$  and  $4.5 \times 10^{-4}$  mol/min for GaAs/GaP(core) nanowires, those of TMGa and  $\text{AsH}_3$  were  $4.6 \times 10^{-5}$  and  $1.1 \times 10^{-3}$  mol/min for GaAs shells, and those of TMGa and TMIn were the same,  $9.5 \times 10^{-6}$  mol/min. The flow rate of  $\text{PH}_3$  was  $1.6 \times 10^{-3}$  mol/min for the GaInP shells. The alternating GaAs/GaInP shell layers were grown at  $580^\circ\text{C}$  after the fabrication of GaP core nanowires from which gold had been removed. After the GaAs/GaP(core) nanowires had been grown, the GaAs with Au particles were removed by wet etching (etchant of one part 96%  $\text{H}_2\text{SO}_4$ , ten parts 30%  $\text{H}_2\text{O}_2$ , and 50 parts  $\text{H}_2\text{O}$ ) as shown in Figures 1(a) and 1(b). Then multishells were grown in the MOVPE chamber again (Figure 1(c)). Finally, air-gap structures were formed by removing GaAs layers with the same wet etchant (Figure 1(d)).

Stacking-fault-free nanopillars were also formed by combining the VLS growth mode and MOVPE mode. The flow rate of the group III sources was  $5\text{--}10 \times 10^{-6}$  mol/min and that of the group V sources was  $4 \times 10^{-4}$  mol/min. Figure 2 shows the procedure for obtaining the target nanostructure.

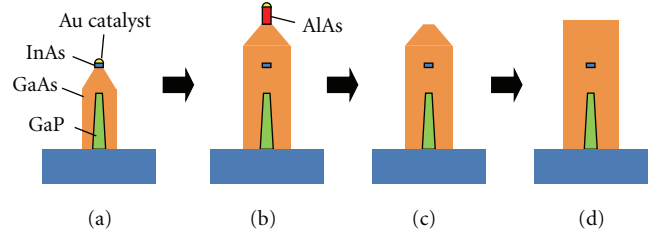


FIGURE 2: Cross-sectional schematic images of nanopillars explaining the fabrication process. (a) InAs/GaAs/GaP nanowires on Si(111); (b) GaAs and AlAs growth; (c) after removal of AlAs together with Au particles; (d) GaAs growth.

After the Au particles from the Au colloids had been dispersed on the surface, the temperature was raised to  $520^\circ\text{C}$  to grow GaP nanowires for one minute. Then GaAs growth was performed at  $550^\circ\text{C}$  (HT-GaAs) for 10 min, after which the nanostructures show pillars surrounded by  $\{112\}$  facets with tapered tops. Next, as shown in Figure 2(a), InAs growth was performed at  $460^\circ\text{C}$  for 3 s. The Au particles used here were 20 nm in diameter so quantum confinement was not strong enough in the lateral direction. In principle, we can make the InAs smaller in the lateral direction by using smaller Au particles. The thickness of the InAs was not optimized in this study, but we aimed at a thickness of under 10 nm. The InAs nanowire growth on GaAs pillars was confirmed at this temperature by other additional experiments. Finally, HT-GaAs was grown again for 10 min and AlAs nanowires were grown at  $460^\circ\text{C}$  for 20 s (Figure 2(b)). The process from (a) to (b) in Figure 2 was one continuous run in the chamber. After that, the sample was dipped in wet-etchant ( $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ , the same as described above) to remove AlAs nanowires together with the Au particles (Figure 2(c)). The sample again loaded into the growth chamber, and HT-GaAs was grown for 7 min to make flat-top pillars (Figure 2(d)). The nanopillars shown in the last section were formed by using the same flow rates as described here.

The structures of the nanowires were observed by scanning electron microscopy (SEM, Hitachi, S-5200, operated at 15 kV) and transmission electron microscopy (TEM, JEOL, JEM2100F, at 200 kV). High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) and energy dispersive X-ray spectrometry (EDS) analyses were also performed in the TEM chamber to evaluate the element distribution in the nanowires. For optical characterization, photoluminescence (PL) measurements were performed at 4 K using cw excitation (a Ti:sapphire laser: 710 nm, 100  $\mu\text{W}$ ). The collected luminescence was fed to a spectrometer equipped with a silicon charged-coupled device (CCD) and InGaAs diode array.

## 3. Results and Discussion

**3.1. Core-Multishell Nanowires with Air Gaps.** For most reported core-shell nanowires, the aim has been to just cap the core for protection against various surface effects in

order to improve the conductivity of electrons or holes or to enhance emission from the optical active part [11, 12]. Our purpose with the core-multishell structure here is to form a high-Q cavity utilizing the large difference of the refractive index between semiconductor and air [10]. Figure 3 shows core-multishell nanowires that we formed using GaP/GaAs in order to investigate heterostructure in the radial direction. The fabrication process was the same as that for GaInP/GaAs as explained in Figure 1. The TEM sample of the core-multishell GaP/GaAs/GaP nanowires was thinned to about 100 nm by using the FIB (focused ion beam) method. The nanowires were vertically aligned on the Si(111) substrates. To form flat-top structures, the removal of Au catalysts was performed. The nanowires appeared as hexagonal cross sections with six {110} sidewalls from the top view. From EDS data in Figure 3(b), the core and outer shells were confirmed to be GaP and the inner shell to be GaAs. Due to the removal of Au particles, the vertical growth in the VLS mode was completely suppressed. The species absorbed on the top face could not be crystallized there. Instead, they migrated to the sidewalls and contributed to the radial growth, since it was difficult for two-dimensional nucleation to occur on the (111)B faces under the currently used growth conditions. The nanowires had a [111]B-oriented zincblende structure. For general VLS-grown nanowires, stacking faults are observed when nanowires are grown along the [111]B orientation [13]. As seen in the TEM images, the stacking faults in the core apparently continue to the shell layers. These stacking faults indicate the formation of a polytypic structure, which makes it difficult to estimate the band structure and to evaluate the properties of carrier transport, emission, and so on. To improve the crystallinity, it is necessary to grow stacking-fault-free core nanowires as explained in the next section. The core nanowires had a hexagonal cross-section with {112} sidewalls, which were faceted by alternating {111}A and {111}B microfacets as has been explained by Johansson et al. [14]. After the growth of the shell layers, the {112} sidewalls changed into {110}. Different growth modes under certain growth conditions, namely, the VLS and MOVPE or layer-by-layer growth modes, may be responsible for the transition of the sidewalls. When the GaP nanowires were grown in the VLS mode at low temperatures, {112} sidewalls appeared. When the GaP shell layer was grown in the layer-by-layer growth mode at high temperatures, {110} sidewalls appeared.

On Si(111) substrates, we observed core-shell heterostructures whose interfaces continued to the tops and bottoms as shown in Figures 3(c) and 3(d). This is very important because it enables us to form air-gap structures by selective wet etching alone. If the layers were capped at the flat top, we would have to perform dry etching to remove the top layer. And we should also protect the side walls so that they are not etched off by the etchant. Some top-down process is therefore necessary here. Further, if the layers were deposited on the Si and had continued to the shell layers, the shells would come off easily after the wet etching. Actually, we have seen several samples with covered tops and continuous layers on the Si surface to shell layers, so the structure seen

in Figure 3 is rather rare. One possible way to obtain high yields for ideal structure is to fabricate Au-array patterns on the substrate, select proper precursor materials, and control the surface state and distance between each nanowires, that is, control the diffusion properties of reaction species on the surface.

GaP is not suitable for investigating optical characteristics because it is an indirect band-gap material. And the difference in the lattice constant between GaAs and GaP leads to defects or dislocations. We therefore tried to use ternary GaInP for shell growth. Actually, GaP shells were largely strained on GaAs so that cracks were easily formed after the removal of GaAs. By using GaInP, we can adjust the composition of the layer so that it is lattice matched to GaAs. Figure 4(a) shows a SEM image of a core-multishell GaInP/air-gap nanowire. On the surface, aggregated materials occupied a large area, and some structures were covered with a thin overgrown layer on the tops, which prevented the wet etchant from permeating the structures. We managed to observe a well-shaped pillar. The wet etching time was not optimized in this experiment, and it was not apparent if the GaAs shells were completely removed. Because it was difficult to find such well-shaped pillars as seen in Figure 4(a), we could not perform further experiments. Considering the border between the GaP shell and the substrate seen in Figure 3(d), it seems that GaP did not form chemical bonds to the Si substrate. Possibly, most GaP and also GaInP reaction species diffused largely on the substrate surface without epitaxial growth. These core-shell structures with air gaps are promising for PhCs. Due to the large difference in refractive index between semiconductor and air, we can make some efficient cavities. Expecting a high-Q factor and a small mode volume, we performed several simulations using the three-dimensional FDTD (finite differential time domain) method. As shown in Figure 4(b), a structure with three-alternated shells showed a high-Q factor of 2770 and small effective mode volume of  $0.8(\lambda/n)^3$  ( $\lambda$  is wavelength and  $n$  is refractive index) as a whispering gallery mode. The Q factor was comparable to that of vertical-cavity surface-emitting lasers (VCSELs), which is about 2100, but the mode volume was very small compared with that of VCSELs (about  $5(\lambda/n)^3$ ) [15]. We are planning further optimization for this kind of structures.

Here, we performed the Au particle removal by wet etching. Exposing nanowires to air permits surface oxidation and impurity contamination. A continuous process from core nanowire growth to shell growth in a growth chamber is a promising way to prevent this. Some in situ selective etching or selective removal of a certain material, like the technique we performed to make bending nodes by annealing [16], will be necessary for refinement of the crystal.

In this section, one possible way to make optical cavities using nanowires was described. At this stage, there are still many challenges in realizing ideal structures for devices. One of them is how to make structures without stacking faults, which is very important for band-gap engineering as stated above. The next section presents one solution for obtaining stacking-fault-free structures.



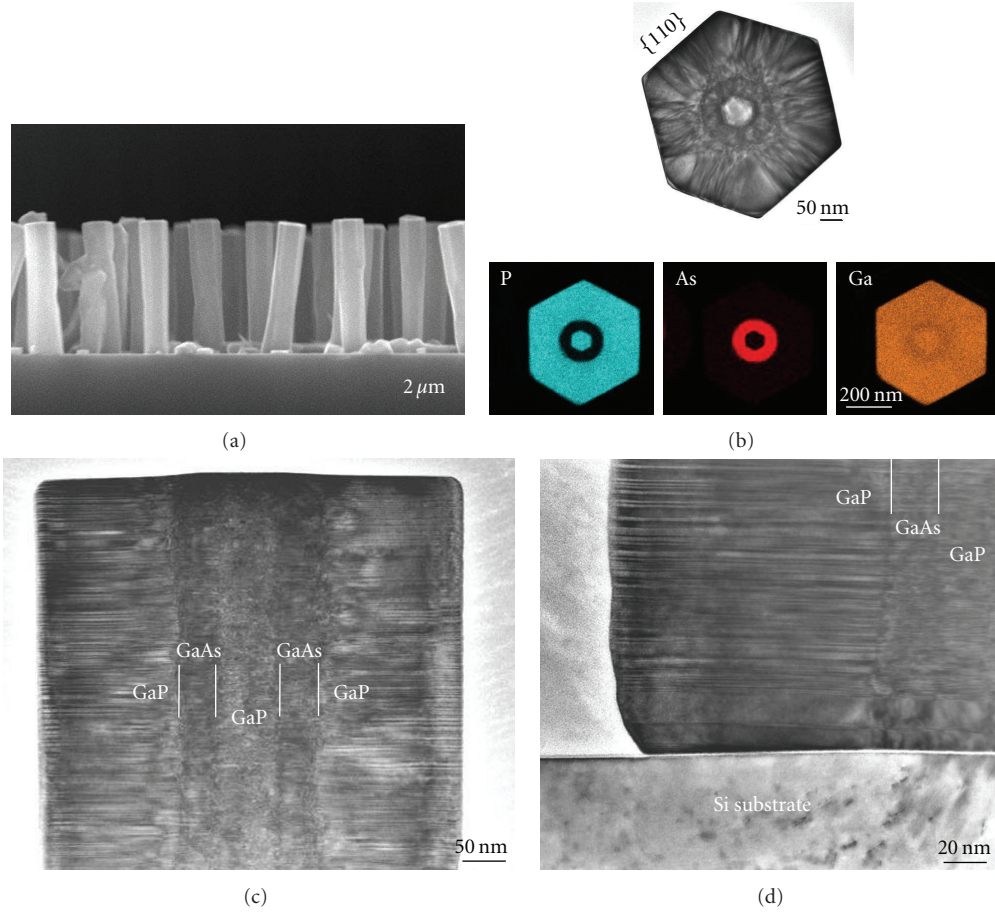


FIGURE 3: (a) SEM and (b)–(d) TEM images of the core-multishell GaP/GaAs/GaP nanowires. EDS mapping images are also included in (b). (a) Side view. (b)–(d) Sliced and thinned samples: (b) perpendicular to the axis; (c), and (d) along the axis.

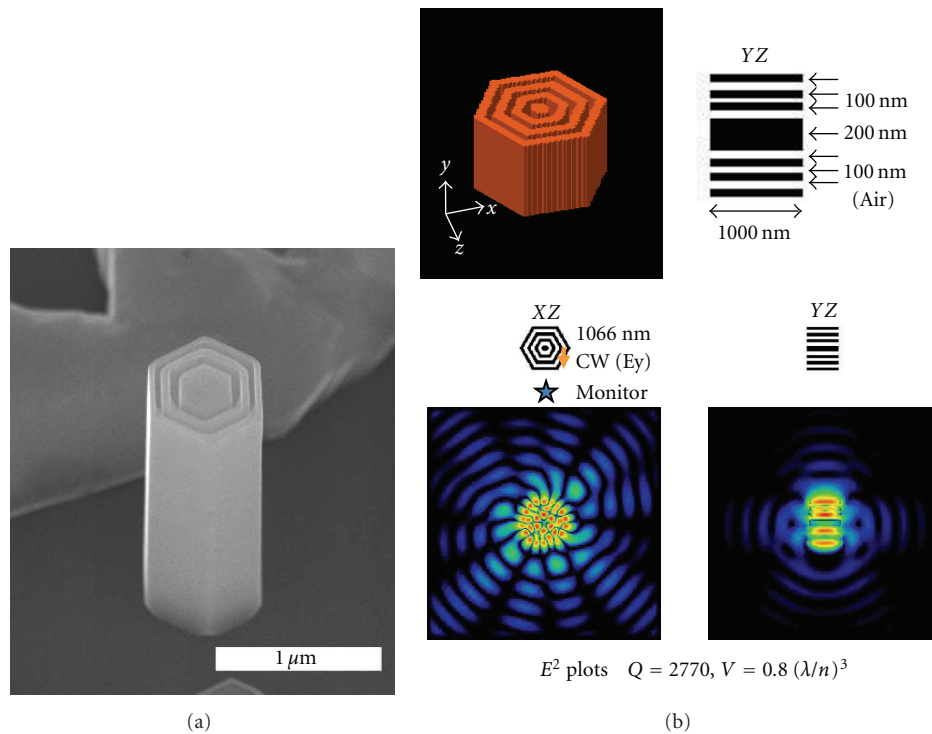


FIGURE 4: (a) SEM image of core-multishell (GaInP/air-gap)<sub>2</sub>/GaInP/GaP nanowires on Si(111). (b) One simulation result by 3D-FDTD for the illustrated structure.

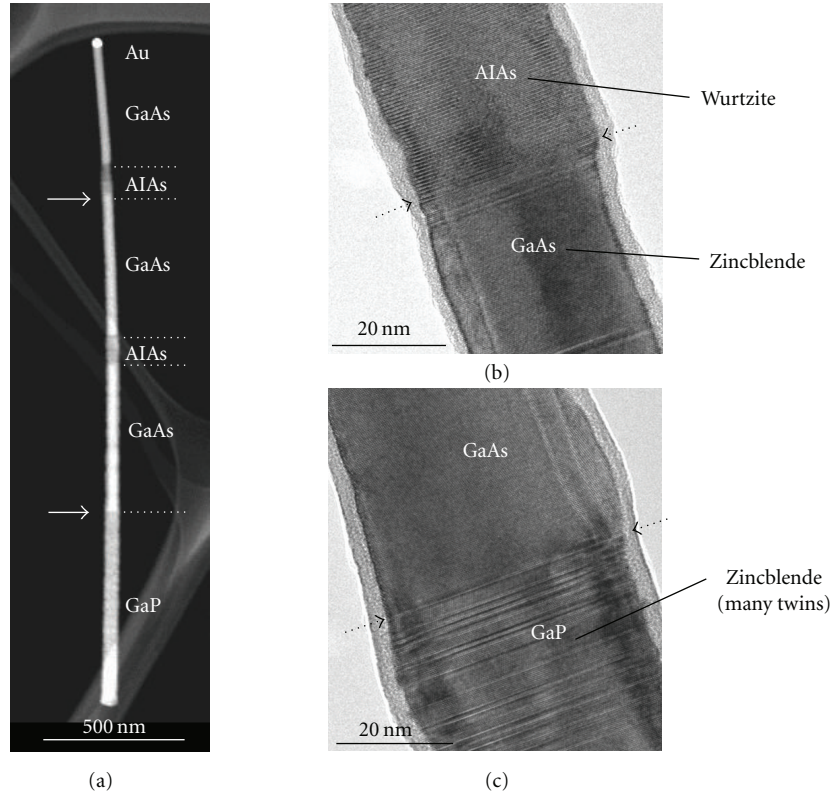


FIGURE 5: An AlAs/GaAs/GaP heterostructure nanowire. (a) A HAADF-STEM image; (b) and (c) HRTEM images of the areas near AlAs/GaAs and GaAs/GaP interfaces, respectively [17].

**3.2. Stacking-Fault-Free GaAs-Related Nanopillars.** Recently, we reported the structural characteristics of AlAs/GaAs/GaP nanowires on Si and found some interesting structures in them [17]. Figure 5 shows the TEM images on such nanowire. The GaP had a zincblende structure with many stacking faults. However, zincblende GaAs that was almost completely free of stacking faults was grown on this GaP. And AlAs with a wurtzite structure was grown on this GaAs. Among the three materials, we focused on the GaAs on GaP nanowires and studied it further.

Figure 6(a) shows a TEM image of the nanopillars on a Si substrate, whose fabrication process was explained in Figure 2. We could obtain flat-top nanopillars vertically grown on Si substrates. The TEM image and the selected area electron diffraction (SAED) patterns were observed through the  $[1\bar{1}0]$  projection. In contrast to the bottom SAED pattern that shows some satellite-like spots in between the main diffraction spots due to a polytypic structure containing rotational twins, the upper region is apparently a single-crystal zincblende structure. From the evaluation of the height, the boundary between the regions with and without stacking faults was the top of the GaP nanowires. Although we could obtain this unexpected and fortunate result, the mechanism for stacking-faults-free growth is not clear at present. After the growth on Si and a GaP nanowire, the Au particle contained much Si and GaP [8]. One hypothesis is that the Si and GaP in the Au alloy particle reduced the effective volume for

the supersaturation. This would prevent changes in the layer-stacking sequence (ABC-ABC stacking for zincblende structure), leading to stable and continuous nucleation [14, 18].

As shown in the growth procedure in Figure 2, we inserted an InAs quantum dot. From the evaluation of the height, the quantum dot was located in the stacking-fault-free region. To determine the quantum dot position more precisely, we performed EDS analysis as shown in Figure 6(b). However, no clear sign of an InAs quantum dot was detected. The InAs seemed to be so thin that the luminescence from the K line for In was under the detection limit. We also performed low-temperature PL measurement. Figure 6(c) shows the PL spectrum at 4 K obtained from a single pillar. Only one peak with shoulders was seen in the range from 750 to 1600 nm. The peak at 821 nm (1.51 eV) is attributed to zincblende GaAs [19, 20]. A shoulder at 832 nm (1.49 eV) is also seen, which is attributed to carbon-related emission [20]. Possible InAs-related emission around 1.46 eV as a shoulder is seen. The intensity is very weak, although the InAs is located in the twin-free region. Possible reasons are high concentrations of impurities and nonradiative centers. In addition, InAs dots were about 20 nm in diameter, which might cause stress around the dot region due to large lattice mismatch, and this stress would influence the emission. We have to reduce the impurities, especially carbon, by optimizing the growth conditions and should use low-strain quantum-dot material-like GaInAs.

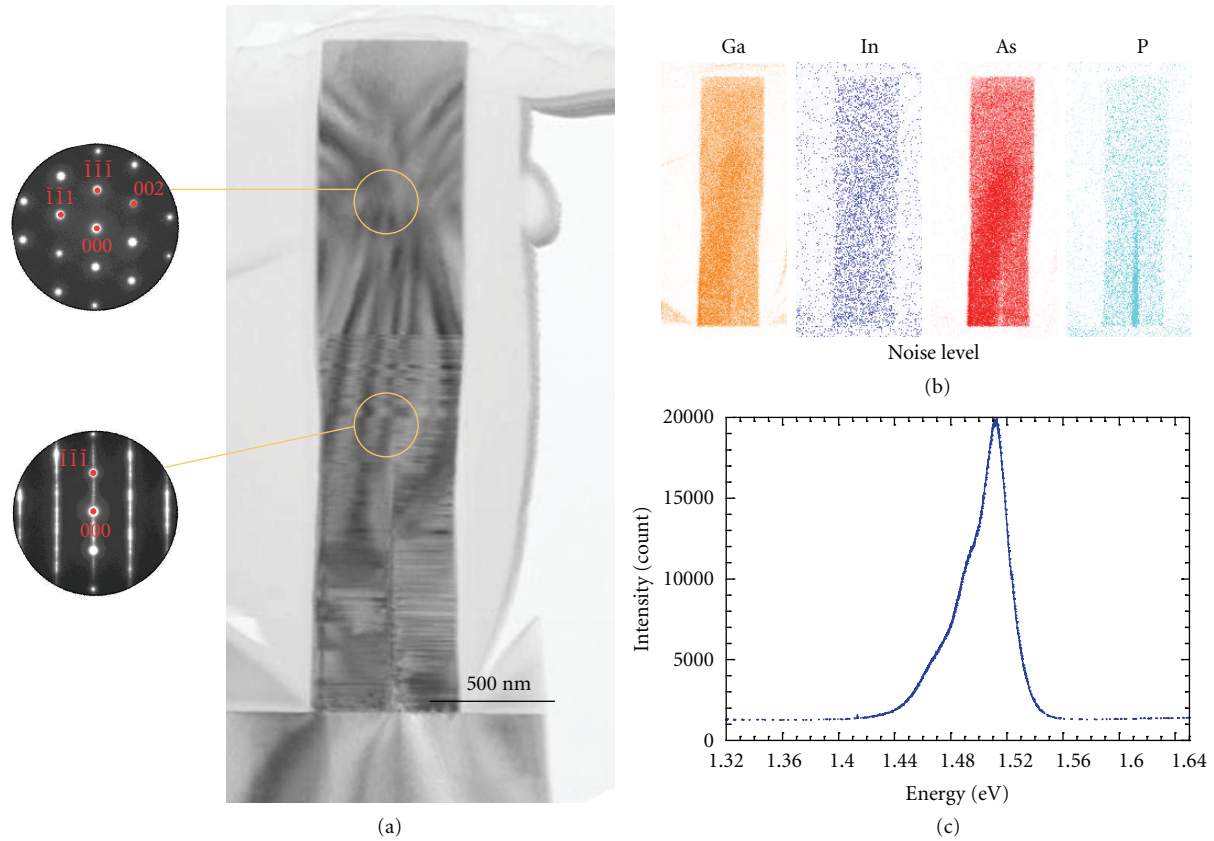


FIGURE 6: GaAs nanopillar containing an InAs dot. (a) HR-TEM image of the nanopillar and SAED patterns; (b) element mapping by EDS obtained from K lines; (c) PL spectrum of one nanopillar at 4 K.

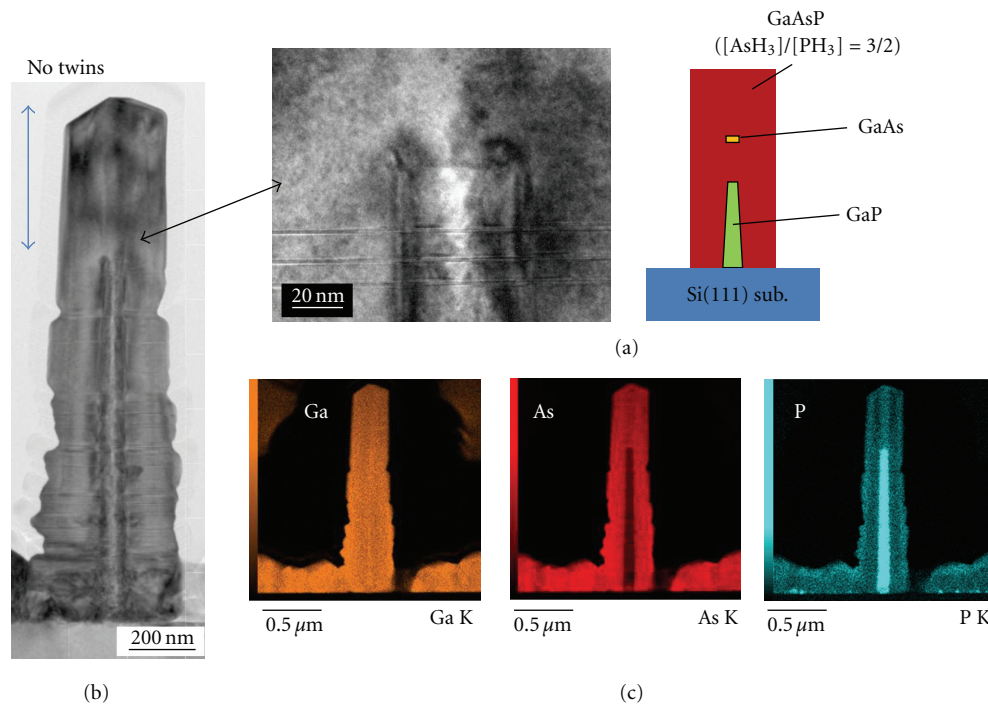


FIGURE 7: GaAsP nanopillar containing a GaAs dot. (a) Schematic illustration; (b) TEM images; (c) EDS mapping images. Here, an Au colloid with 60-nm diameter was used. The sample was thinned by the focused ion beam method. A stacking-fault-free region is confirmed above the GaP nanowire. However, we could not observe the dot in the pillar.



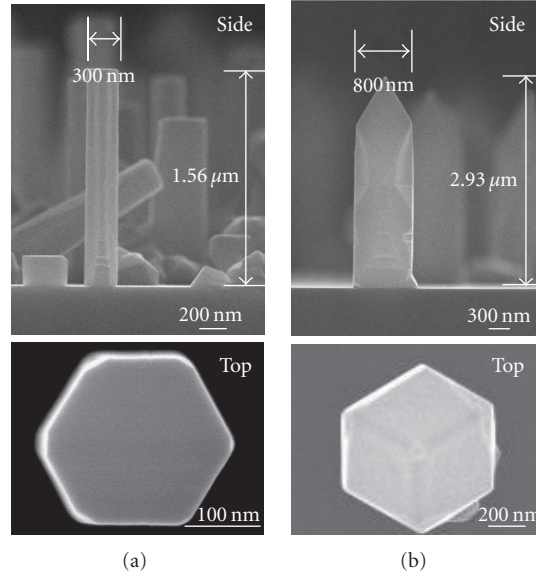


FIGURE 8: SEM images of GaAs/GaP nanopillars on Si. Diameters of Au colloids are (a) 5 and (b) 60 nm.

In order to observe a quantum dot in a pillar, we tried another experiment in which we changed the material combination and growth conditions. Figure 7 shows a GaAsP nanopillar with a GaAs dot. The fabrication process was the same as explained above (Figure 2), and the structure is schematically illustrated in Figure 7(a). For the growth of GaAsP, the flow ratio of  $\text{AsH}_3$  to  $\text{PH}_3$  was kept at 3/2 for both the core and shell regions. We sliced the sample for TEM measurement to about 100-nm thick with an FIB method so that we could see the crystal structure clearly. Figure 7(b) is the TEM image of this sample. Since we used 60-nm  $\phi$  Au colloids, the shell was not thick enough to make a flat top. The interface between the GaP and GaAsP is clearly seen. EDS mapping images in Figure 7(c) more clearly show the interface than those in Figure 6(b). A stacking-fault-free region is confirmed above the GaP nanowire. But unfortunately, we could not observe the dot in the pillar. This may be due to the high As content in the GaAsP region, whose intensity was not so different from that of the GaAs quantum dot. In our experiments, we failed to see a quantum dot in the pillar. Considering the growth process, we believe that the quantum dot could be formed in this zincblende stacking-fault-free region and will seek to identify it by another method in the near future.

**3.3. Flat-Top Nanowires by One Growth Procedure.** To make flat-top pillars, we have to remove Au particles, which still act as catalyst and selectively enhance the axial growth also at high growth temperature. There are several methods for removing Au particles as described in Section 3.1. Selective wet etching is a reliable method, but the nanowires have to be exposed to air which causes impurity contamination. We can remove Au particles just after the nanowire growth by selectively removing one part of the heterostructure nanowires by annealing or gas etching. In this case, possible material combinations are limited for achieving high selectivity. Here,

we introduce another method for making flat-top pillars. We found that, when we use small-sized colloids 5 nm in diameter, GaAs pillars showed flat tops. First, GaP nanowires were grown at 520°C, and then GaAs was grown at 600°C. Figure 8 shows SEM images for this sample and a sample with GaAs pillars formed by using Au colloids with 60 nm in diameter. The pillars with 60-nm Au have a tapered structure at the top region due to VLS growth mode. On the other hand, the pillars with 5-nm Au have flat tops and are surrounded by six {110} side facets. We also confirmed that the GaAs above GaP nanowires is a stacking-fault-free zincblende structure from TEM images (not shown here). At high growth temperature, the concentration of Ga in Au particles becomes high. So it is assumed that highly Ga-containing Au particles could not keep their hemispherical shape and were buried in the surrounding layer, forming stable facets of {110} and (111)B at the top. It resembles GaAs nanowires buried with AlGaAs layers which were grown at high temperature [21]. But in this case, it seems that there was no Au particle on the top surface. If this is the mechanism, the pillars may contain Au inside. We hope to confirm this experimentally and investigate its influence on device performance. Whether Au is in the core region or not, high-quality layers can be grown in the radial direction just after the core growth. The pillars are not exposed to air on the way, and the layers are epitaxially grown on the single-crystal GaAs core. By combining our techniques described above, we expect to be able to obtain a refined laser structure in the bottom-up manner; we can already make a quantum dot without stacking faults as described in Section 3.2 and cavity structures explained in Section 3.1. We hope to demonstrate this in the near future.

## 4. Conclusions

We grew vertical nanopillars with flat tops on Si substrates and were able to make cavity structures with air gaps and

stacking-fault-free GaAs regions containing a quantum dot in the upper part of the pillars. We obtained core-multishell Ga(In)P/GaAs (or air-gap)/GaP nanowires with flat tops, which we will be able to apply to photonic crystal devices. In the fabrication and characterization of GaAs nanopillars using GaP-based nanowires on Si(111), we found that zincblende GaAs without any stacking faults can be grown after the GaP nanowire growth. And we obtained flat-top pillars using small Au particles. We expect to obtain a refined laser structure in the bottom-up manner by combining these growth techniques.

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