Hindawi Publishing Corporation
Journal of Nanotechnology
Volume 2015, Article ID 395090, 6 pages
http://dx.doi.org/10.1155/2015/395090

*Research Article*

# Optimization and Characterization of CMOS for Ultra Low Power Applications

**Mohd. Ajmal Kafeel,[1] S. D. Pable,[2] Mohd. Hasan,[1] and M. Shah Alam[1]**

[1]*Department of Electronics Engineering, AMU, Aligarh, India*
[2]*Department of Electronics and Telecommunication Engineering, Matoshri College of Engineering and Research Centre, Eklahare, Nashik, Maharashtra, India*

Correspondence should be addressed to Mohd. Ajmal Kafeel; ajmal_kafeel@hotmail.com

Received 31 July 2015; Revised 2 November 2015; Accepted 2 December 2015

Academic Editor: Niraj K. Jha



Aggressive voltage scaling into the subthreshold operating region holds great promise for applications with strict energy budget. However, it has been established that higher speed superthreshold device is not suitable for moderate performance subthreshold circuits. The design constraint for selecting $V_{th}$ and $T_{OX}$ is much more flexible for subthreshold circuits at low voltage level than superthreshold circuits. In order to obtain better performance from a device under subthreshold conditions, it is necessary to investigate and optimize the process and geometry parameters of a Si MOSFET at nanometer technology node. This paper calibrates the fabrication process parameters and electrical characteristics for n- and p-MOSFETs with 35 nm physical gate length. Thereafter, the calibrated device for superthreshold application is optimized for better performance under subthreshold conditions using TCAD simulation. The device simulated in this work shows 9.89% improvement in subthreshold slope and 34% advantage in $I_{ON}/I_{OFF}$ ratio for the same drive current.

## 1. Introduction

While universal scaling trends of CMOS technology are mostly focused on achieving higher speed, selection of device fabrication process parameters for ULP applications with lower operating frequencies is still under exploration [1–5]. It has been shown recently that subthreshold circuits are significantly benefitted by optimizing the device parameters [3]. Process and geometry parameters of superthreshold circuits are largely governed by the different leakage currents and, hence, its static power dissipation [6–10]. However, due to lower supply bias, gate leakage current, DIBL, and punchthrough effects are negligible under subthreshold conditions [11]. Therefore, to some extent, design constraint for selecting $V_{th}$ and $T_{OX}$ becomes more flexible in case of device operated under subthreshold regime.

For superthreshold devices, scaling of $V_{th}$ is restricted by the amount of static leakage, mainly subthreshold leakage current in nanometer technology nodes [2, 3]. Such a high $V_{th}$ device will give significant performance penalty under subthreshold conditions due to lower subthreshold leakage current, which is used to perform necessary digital computations. Hence, the choice of $V_{th}$ is a tradeoff between speed and leakage power dissipation in case of superthreshold applications. However, in subthreshold region, lower static leakage power dissipation due to scaled $V_{DD}$ even below $V_{th}$ allows further reduction in $V_{th}$ to enhance the speed.

Along with subthreshold leakage current, gate leakage is also a major hurdle in aggressive scaling of $T_{OX}$ to obtain better control over the channel for a superthreshold device [2, 3]. In general, $T_{OX}$ scales down slowly from 130 nm technology node to keep minimum gate leakage current in case of high frequency applications [2] due to higher supply bias. However, it degrades "$S$" and causes lowering of $I_{ON}/I_{OFF}$ ratio. In subthreshold operating region due to lower $V_{DD}$, reducing $T_{OX}$ will not significantly increase the gate leakage current [11]. In addition, transistor input capacitance is smaller under subthreshold conditions than the

Table 1: Physical dimensions used for 35 nm gate length MOSFET [8].

| | Gate length | $T_{OX}$ (nm) | Junction depth (nm) | Poly silicon thickness (nm) | Spacer thickness |
|---|---|---|---|---|---|
| nFET | 35 | 1–1.2 | 20 | 150 | 52.5 |
| pFET | 35 | 0.95 | 33 | 150 | 52.5 |

Table 2: Simulation and experimental performance parameters.

| | Toshiba (experimental) | | This work (simulation) | |
|---|---|---|---|---|
| | n-MOSFET | p-MOSFET | n-MOSFET | p-MOSFET |
| $I_{ON}$ ($\mu$A/$\mu$m) | 676 | 272 | 676 | 300 |
| $I_{OFF}$ (nA/$\mu$m) | 100 | 100 | 106 | 110 |
| SS (mV/dec) | 86.1 | 92.3 | 83.88 | 90.56 |

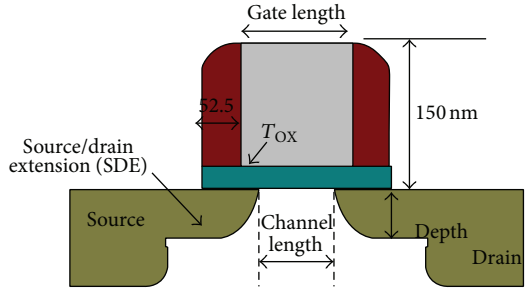


Figure 1: Cross-section drawing of a CMOS transistor.

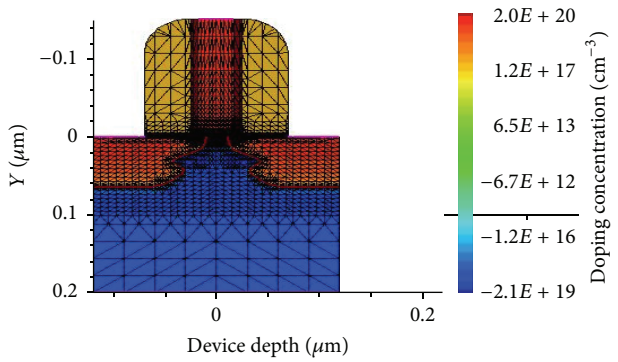


Figure 2: Simulation structure of 45 nm NMOS.

superthreshold regime [3]. Hence, more aggressive scaling of $T_{OX}$ is possible under subthreshold conditions to achieve higher speed and lower energy consumption.

In addition, it is an established fact that a superthreshold device in nanometer technology nodes requires halo and retrograde doping to suppress short channel effects. Halo and retrograde wells are used to reduce DIBL and punchthrough effects and to control $V_{th}$ of the device independent of its subthreshold slope. However, in subthreshold regime, due to supply bias lower than $V_{th}$, DIBL and punchthrough effects are negligible. Hence, subthreshold device characteristics are less sensitive to halo and retrograde doping. Therefore, this paper investigates the design of a subthreshold NMOS device at 45 nm technology node with better subthreshold slope and higher drive current capability.

## 2. Calibration of a MOS Device

Transistors $L_g$ and $T_{OX}$, as shown in Figure 1, primarily set the transistor performance parameters [12]. Authors in [13] fabricated the optimized 35 nm gate length NMOS device with 676 $\mu$A/$\mu$m drive current, subthreshold slope = 86 mV/dec., and $I_{OFF}$ = 100 nA/$\mu$m at $V_{DD}$ = 0.85 V. This device was fully optimized for short channel effect suppression and parasitic resistance reduction. In order to obtain an optimum subthreshold device, there is a need first to design a superthreshold device with better performance at 45 nm technology node. The physical dimensions of a 35 nm NMOS device, fabricated by Toshiba and listed in Table 1, are considered for simulation purposes [13]. The poly-Si thickness is 150 nm, while the distance of S/D contact to gate is 52 nm. In simulation, the source and drain electrodes are treated as ohmic contacts. The resulting SDE junction depth is 15 nm for NMOS and 28 nm for PMOS. Lower $T_{OX}$ for PMOS causes more drive current in PMOS which is comparable to NMOS. Lower $T_{OX}$ in case of PMOS will cause more vertical electric field in channel which further increases subthreshold drive current in PMOS.

Furthermore, channel doping and halo doping are tuned to calibrate our device with the NMOS fabricated in [13] and corresponding electrical characteristics are listed in Table 2. At first, the simulation project matches the published process details of real structure as accurately as possible. It includes the physical parameters as given in Table 1. The calibrated 45 nm device structure, as shown in Figure 2, is obtained with physical parameters as listed in Table 1. The drain current versus gate voltage ($I_{DS}$-$V_{GS}$) and drain current versus drain voltage are the primary targets for calibration in device simulations. The calibration starts by adjusting the electrostatic to match subthreshold slope, drain current, and $I_{OFF}$. Finally, device measurements are matched to the previously published calibrated device [13] by doping profiles adjustment so as to achieve the desired $I$-$V$ characteristics. The flowchart of the calibration process is given in Figure 3 [14]. For process calibration, tuned mobility parameters are used. The matched calibrated electrical characteristics are then obtained through TCAD simulation. The important figures of merit, extracted from simulation, are then compared with the experimental data in Table 2. This is the starting point for investigating the effect of physical and process parameters under subthreshold conditions.

## 3. Effect of Oxide Thickness and Channel Length on Device Parameters

As seen in Section 1, one of the key methods to enable gate length scaling over the past several generations is to scale

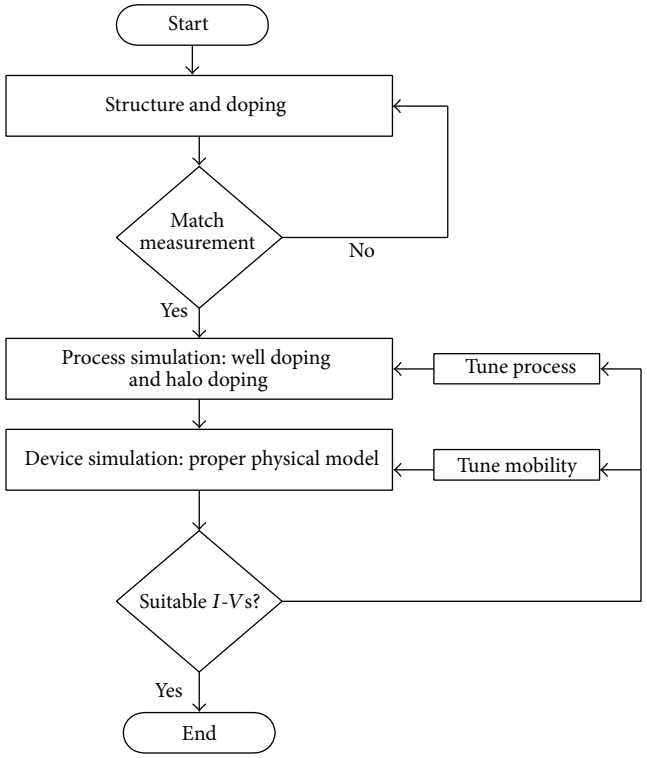


FIGURE 3: Flowchart for calibration methodology used in simulation [8].

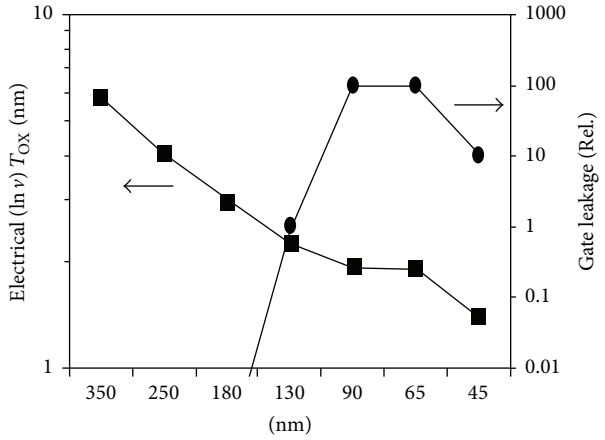


FIGURE 4: Effect of $T_{OX}$ scaling and gate leakage versus Intel technology [10].

the $T_{OX}$ [15]. Therefore, $T_{OX}$ scaling has been instrumental in controlling short channel effects as MOS gate dimensions have been reduced. This improves the control of the gate electrode over the channel, which enables both shorter channel lengths and higher performance. As $T_{OX}$ scales down, increase in gate leakage current becomes significant below 65 nm technology node as shown in Figure 4. In addition, gate capacitance also increases significantly with $T_{OX}$ scaling for superthreshold circuits. To reduce the increased gate leakage, a gate dielectric with higher dielectric constant is introduced below 45 nm [16]. However, due to lower $V_{DD}$,

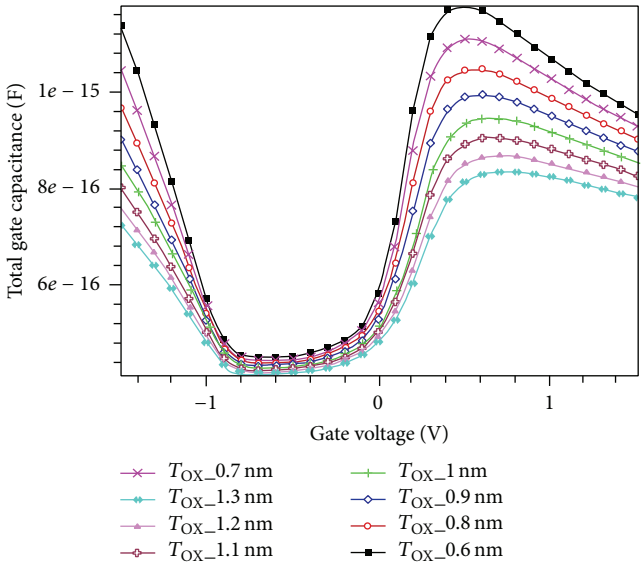


FIGURE 5: Gate capacitance as a function of $V_{GS}$ for 45 nm NMOS.

gate leakage component is negligible under subthreshold as compared to superthreshold conditions.

The effective gate capacitance $C_g$ of a transistor is dominated by intrinsic depletion and parasitic capacitances, which are strongly dependent on $T_{OX}$ [17]. In energy constraint subthreshold design, circuits are normally optimized to enhance the speed [18, 19]. To reduce these capacitances, higher value of $T_{OX}$ is preferred. However, it reduces the gate control over the channel; hence, it results in higher value of "S." Hence, for moderate speed application with some loss of energy, significant improvement in speed can be achieved. In addition, as shown in Figure 5, under subthreshold conditions ($V_{GS} < 0.3$), $T_{OX}$ scaling does not increase $C_g$ significantly contrary to superthreshold operating region. The effective channel length also determines subthreshold leakage current and $V_{th}$.

Therefore, this section examines the joint impact of $T_{OX}$ and $L_g$ scaling on the device performance. The calibrated NMOS structure, as shown in Figure 2, is simulated to investigate the effect of $L_g$ and $T_{OX}$ on the characteristics of NMOS device under subthreshold conditions at $V_{DD}$ = 150 mV. $L_g$ and $T_{OX}$ are varied from 30 nm to 50 nm and 0.6 nm to 1.3 nm respectively. The values of halo doping and substrate doping are kept constant at $1.6e+19/cm^3$ and $2.2e+18/cm^3$, respectively.

It is observed from Figure 6 that an increase in $L_g$ and a decrease in $T_{OX}$ reduce "S" significantly. Increasing $L_g$ from 35 to 50 nm reduces "S" by approximately 6 mV/decade for different values of $T_{OX}$. It is clear from Figure 7 that an increase in channel length has negligible effect on the gate capacitance. Therefore, longer channel length will result in lower power dissipation and better performance because of improved "S." Also, reducing $T_{OX}$ from 1 to 0.8 nm at $L_g$ = 35 nm reduces "S" by 2.3 mV/decade and increases $C_g$ by 12%. Therefore, careful selection of $T_{OX}$ is required so that the improvement in "S" will not be masked by the increase

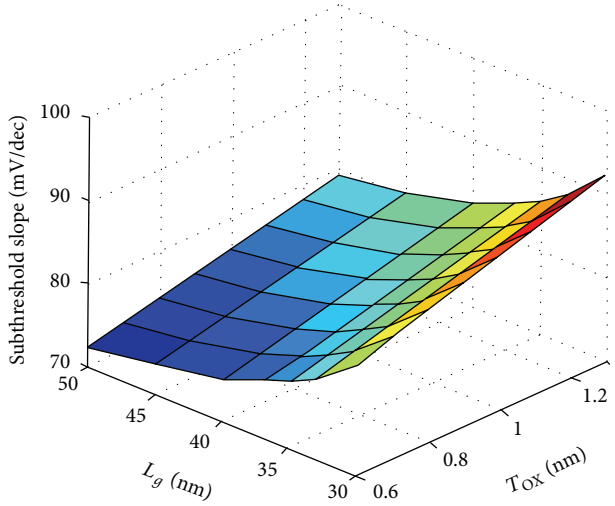


FIGURE 6: Subthreshold slope as a function of $L_g$ and $T_{OX}$ for 45 nm NMOS.

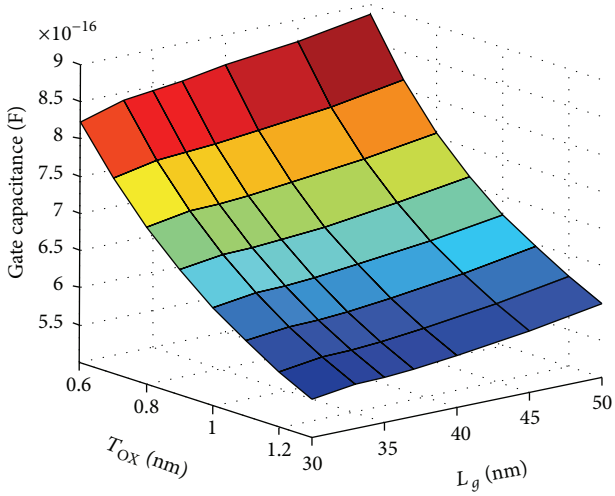


FIGURE 7: Gate capacitance as a function of $L_g$ and $T_{OX}$ for 45 nm NMOS.

in $C_g$ and hence the power dissipation ($C_g V_{DD}^2 f$). However, from Figure 7, it is evident that $T_{OX}$ is having large impact on $C_g$ as compared to $L_g$. In addition, it has been evident that the increase in $L_g$ reduces $I_{ON}$ and $I_{OFF}$ current by 14x and 22x, respectively, at $T_{OX}$ = 1 nm. Therefore, $I_{ON}/I_{OFF}$ ratio increases by 1.36x at $T_{OX}$=1 nm with the increase in $L_g$. This also reduces the power consumption. From Figure 8, optimum value of $L_g$ can be obtained for better values of "$S$" and $I_{ON}/I_{OFF}$ ratio for different values of $T_{OX}$.

From the above analysis, it can be concluded that, for energy efficient ULP circuits, larger value of $L_g$ can be used to reduce the energy consumption due to lower "$S$" and higher $I_{ON}/I_{OFF}$ ratio. However, for higher performance ULP circuits, increase in $L_g$ will significantly reduce the drive current and hence the speed. Therefore, higher value of $L_g$ is not suitable for high performance ULP applications.

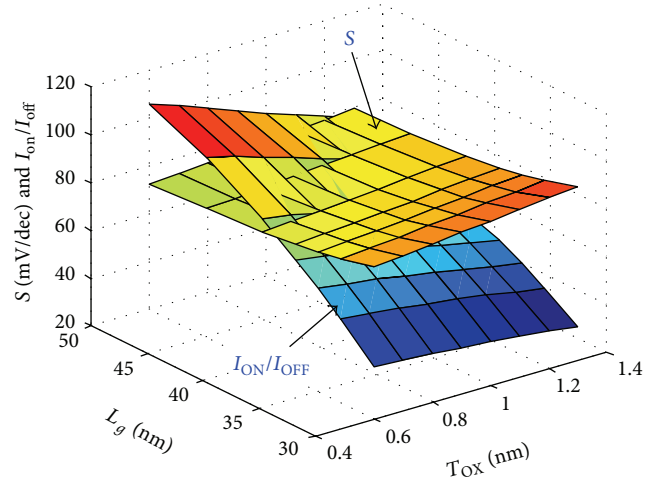


FIGURE 8: Subthreshold slope and $I_{ON}/I_{OFF}$ as a function of $L_g$ and $T_{OX}$ for 45 nm NMOS.

## 4. Effect of Doping Profile under Subthreshold Conditions

In scaled superthreshold transistors, halo and retrograde doping profiles are used to suppress short channel effects (SCE) like DIBL lowering and body punchthrough [20]. However, in subthreshold region, SCE plays a minor role as compared to superthreshold regime because of lower $V_{DD}$ [11]. Hence, it has been established that halo and retrograde doping are less effective under subthreshold conditions. Also low doping level can reduce the bottom junction capacitance. Therefore, it is important to investigate the effect of doping profile under subthreshold conditions in nanometer technology domain.

It is observed from Figure 9 that the reductions in substrate ($N_{sub}$) and halo doping increase the drain current ($I_{sub}$) significantly. The decrease in $N_{sub}$ doping concentration by 50% increases $I_{sub}$ by 3.5x. Also reducing $N_{halo}$ by 4x increases $I_{sub}$ by 2.25x. However, from Figure 10, it is observed that reducing $N_{sub}$ by 50% increases "$S$" by 0.7 mV/decade and $I_{OFF}$ by 3.88x. Therefore, a trade-off is involved in improving the drive current, "$S$," and $I_{OFF}$ on reducing $N_{sub}$ doping concentration. Similar performance trend is observed by changing the halo doping concentration. Figures 11 and 12 show the drive current and subthreshold slope as a function of halo and substrate doping.

## 5. Subthreshold Device Characterization

This section mainly targets improvement of the subthreshold slope so that energy consumption can be reduced [11]. The calibrated device is then tuned at optimum values of $L_g$, $T_{OX}$, $N_{sub}$, and $N_{halo}$ to achieve best subthreshold characteristics. Optimized device parameters from Section 4 are used to achieve better subthreshold slope under subthreshold conditions. Figure 13 shows the comparison of the subthreshold slope as a function of supply voltage for the conventional and the optimized device under subthreshold condition.

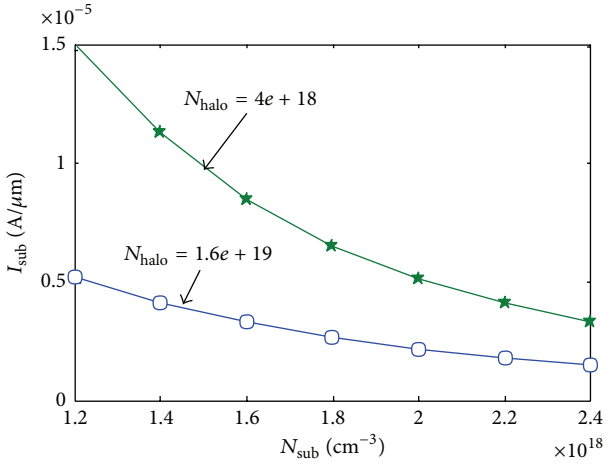


FIGURE 9: Drain current as a function of channel doping for different halo doping.

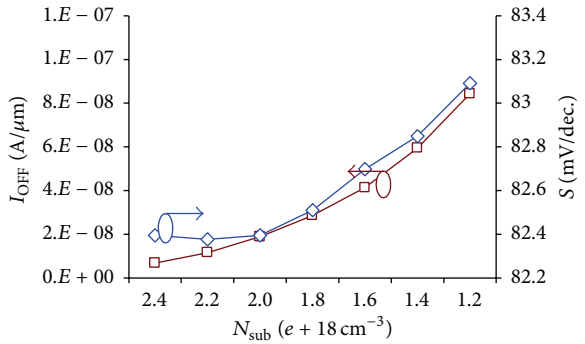


FIGURE 10: $I_{OFF}$ as function of channel doping.

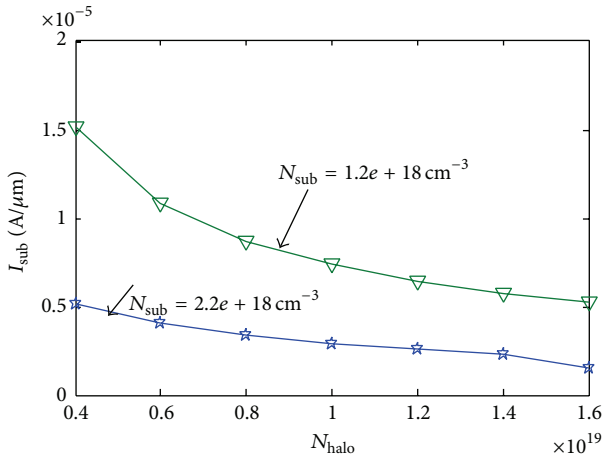


FIGURE 11: Drain current as a function of halo doping.

As shown in Figure 13, the optimized device shows 9.89% improvement in subthreshold slope over the conventional device operated in subthreshold region. Also, as shown in Table 3, $I_{ON}/I_{OFF}$ ratio increases by 34% in case of optimized device for the same drive current. Since effect of DIBL is very small under subthreshold conditions this work has not considered the DIBL during optimization.

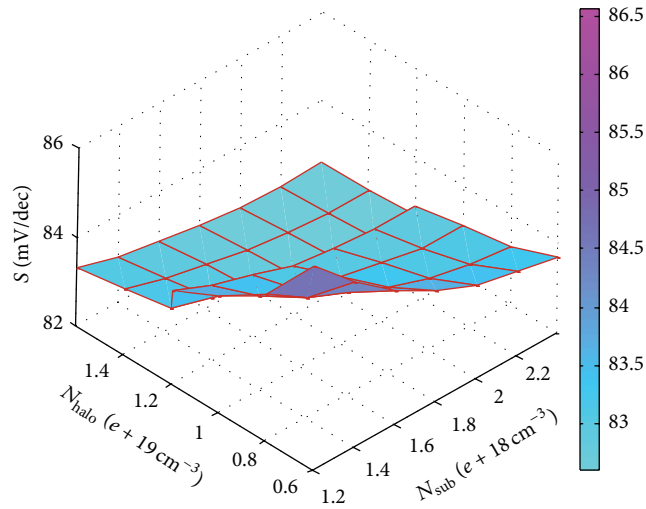


FIGURE 12: Subthreshold slope as a function of halo doping and channel doping.

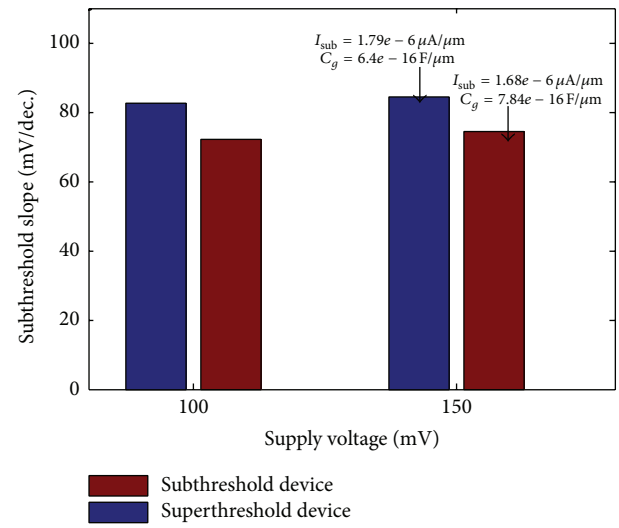


FIGURE 13: Subthreshold slope as a function of supply voltage.

TABLE 3: Comparison of performance parameters under subthreshold conditions.

| | Toshiba (experimental) | This work (simulation) |
|---|---|---|
| $I_{ON}$ (μA/μm) | 1.79 | 1.68 |
| $I_{OFF}$ (nA/μm) | 32 | 19.9 |
| SS (mV/dec) | 82.58 | 74.41 |

## 6. Conclusion

The device designed for superthreshold circuits is not suitable for optimum subthreshold operation. This paper proposed new device process parameters to improve the subthreshold slope and to enhance the speed of subthreshold circuits. It

has successfully concluded that optimizing the device for subthreshold region results in improvement in both the subthreshold slope and the $I_{ON}/I_{OFF}$ ratio. Hence, in order to obtain the better performance of device under subthreshold conditions, it is necessary to optimize the process and geometry parameters of Si-MOSFET at nanometer technology node due to relaxed constraint for different leakage currents and short channel effects.

## Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

## References


[1] A. Tajalli and Y. Leblebici, "Design trade-offs in ultra-low power digital nanoscale CMOS," *IEEE Transactions on Circuits and Systems-I*, vol. 58, no. 9, pp. 2189–2200, 2011.

[2] D. Bol, R. Ambroise, D. Flandre, and J.-D. Legat, "Interests and limitations of technology scaling for subthreshold logic," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 10, pp. 1508–1519, 2009.

[3] B. C. Paul and K. Roy, "Oxide thickness optimization for digital subthreshold operation," *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 685–688, 2008.

[4] J. Kwong and A. P. Chandrakasan, "Variation-driven device sizing for minimum energy subthreshold circuits," in *Proceedings of the International Symposium on Low Power Electronics Design (ISLPED '06)*, pp. 8–13, October 2006.

[5] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, 1998.

[6] J. M. Rabaey and M. Pedram, Eds., *Low Power Design Methodologies*, vol. 336 of *The Springer International Series in Engineering and Computer Science*, Kluwer Academic Publishers, Boston, Mass, USA, 1995.

[7] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, Cambridge, UK, 2nd edition, 2009.

[8] W. K. Henson, N. Yang, S. Kubicek et al., "Analysis of leakage currents and impact on off-state power consumption for CMOS technology in the 100-nm regime," *IEEE Transactions on Electron Devices*, vol. 47, no. 7, pp. 1393–1400, 2000.

[9] D. Lee, W. Kwong, D. Blaauw, and D. Sylvester, "Simultaneous subthreshold and gate-oxide tunneling leakage current analysis in nanometer CMOS design," in *Proceedings of the 4th International Symposium on Quality Electronic Design*, pp. 287–292, IEEE, San Jose, Calif, USA, March 2003.

[10] L. Wei, Z. Chen, K. Roy, M. C. Johnson, Y. Ye, and V. K. De, "Design and optimization of dual-threshold circuits for low-voltage low-power applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 7, no. 1, pp. 16–24, 1999.

[11] A. Wang, B. H. Calhoun, and A. P. Chandrakasan, *Sub-Threshold Design for Ultra Low-Power Systems*, Springer, New York, NY, USA, 1st edition, 2006.

[12] S. Thompson, M. Alavi, M. Hussein et al., "130 nm logic technology featuring 60 nm transistor, low-K diaelectrics, and Cu interconnects," *Intel Technology Journal*, vol. 6, no. 2, pp. 5–13, 2002.

[13] S. Inaba, K. Okano, S. Matsuda et al., "High performance 35 nm gate length CMOS with NO oxynitride gate dielectric and Ni salicide," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2263–2270, 2002.

[14] X. Wang, *Simulation study of scaling design, performance characterization, statistical variability and reliability of nanometer MOSFETs [Ph.D. thesis]*, University of Glasgow, Glasgow, UK, 2010.

[15] C. Auth, A. Cappellani, J. S. Chun et al., "45 nm high-k+ metal gate strain enhance transistor," *Intel Technology Journal*, vol. 12, no. 2, pp. 77–84, 2008.

[16] Y. Wang, X. Zhang, X. Liu, and R. Huang, "Novel devices and process for 32 nm CMOS technology and beyond," *Science in China Series F: Information Sciences*, vol. 51, no. 6, pp. 743–755, 2008.

[17] A. Khakifirooz and D. A. Antoniadis, "MOSFET performance scaling—part II: future directions," *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1401–1408, 2008.

[18] S. Hanson, M. Seok, D. Sylvester, and D. Blaauw, "Nanometer device scaling in subthreshold logic and SRAM," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 175–185, 2008.

[19] J. Kil, J. Gu, and C. H. Kim, "A high-speed variation-tolerant interconnect technique for sub-threshold circuits using capacitive boosting," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 16, no. 4, pp. 456–465, 2008.

[20] S. Thompson, P. Packan, and M. Bohr, "MOS scaling: transistor challenges for the 21st century," *Intel Technology Journal*, no. Q3, pp. 1–19, 1998.