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Research Article

Photovoltaic Energy Harvester with Power Management System

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We present a photovoltaic energy harvester, realized in 0.35-μm CMOS technology. The proposed system collects light energy from the environment, by means of 2-mm^2 on-chip integrated microsolar cells, and accumulates it in an external capacitor. While the capacitor is charging, the load is disconnected. When the energy in the external capacitor is enough to operate the load for a predefined time slot, the load is connected to the capacitor by a power management circuit. The choice of the value of the capacitance determines the operating time slot for the load. The proposed solution is suitable for discrete-time-regime applications, such as sensor network nodes, or, in general, systems that require power supply periodically for short time slots. The power management circuit includes a charge pump, a comparator, a level shifter, and a linear voltage regulator. The whole system has been extensively simulated, integrated, and experimentally characterized.

1. Introduction

Modern ultralow power integrated circuits have reached such a high level of complexity, that for many applications traditional batteries are no longer sufficient, since they cannot guarantee a long enough life time [1]. These applications, such as sensor nodes or lab-on-chip, often include very stressing computational algorithms and wireless communication systems. By harvesting energy from the environment, for example in the form of light, vibrations, or thermal gradients, such systems could work for nearly infinite time without the need of replacing batteries. Energy harvesting not only allows the improvement of the lifetime of the device and the reduction of its weight, but it also enables entirely new applications, that are otherwise not feasible, given the lifetime and size of the batteries. Despite the technology scaling, indeed, electrochemical batteries show a slow growth in terms of energy density and represent a bottleneck for weight and volume [2–4].

Light can be considered the most copious energy source in many environments. Photovoltaic energy scavengers can reach conversion efficiencies ranging from 20%, in standard monocrystalline silicon planar technology, to almost 50% [5, 6], in multimaterial planar wafers, considering an illumination of 1000 W/m^2 from the sun. Moreover the photoelectric phenomena [7] in doped silicon allows retrieving the highest amount of power with respect to any other types of harvesters. Moreover, photovoltaic cells are intrinsically compatible with standard integrated circuit technologies [8], thus making them particularly suitable for implementing energy-autonomous microsystems.

In this paper we present a photovoltaic energy harvesting power supply system for discrete-time-regime applications, realized in 0.35-μm CMOS technology. In particular, in the proposed system, a couple of integrated miniaturized solar cells are used as energy source and a power management circuit has been realized to handle the collected energy.

The block diagram of the proposed system is shown in Figure 1. A first solar cell provides the power supply to an oscillator and to eight parallel Dickson charge pumps. In order to simplify the schematic, we reported only one charge pump. The storage capacitor C_S is external, thus allowing us to choose the capacitance value, according to the operating time slot required by each application. The voltage across C_S (V_S) is monitored by a comparator followed by a level shifter. In particular, V_S is divided and compared with a fixed reference voltage, generated by the second (auxiliary) solar cell. When C_S is fully charged, the level shifter turns on the p-MOS switch M_S, thus connecting the load, and the capacitor delivers the accumulated energy. In order to provide to the load a stabilized power supply, we realized on-chip also a linear voltage regulator (LDO). The LDO is connected

between M_S and the load and, therefore, it is supplied only when the load is connected. In Section 2 we present the characterization of the photovoltaic energy harvesting element, while in Section 3 we describe the oscillator and the charge pump used to elevate the solar cell voltage to a usable value. Sections 4 and 5 discuss the power management system and the LDO, respectively. Finally, in Section 6 the simulation and experimental results are presented.

2. Photovoltaic Energy Harvesting Elements

The photovoltaic energy harvesting elements, implemented on-chip, are based on *p*-*n* junctions. Figure 2 shows the cross-section and the equivalent circuit of the integrated microsolar cell [9], whose area is 1 mm^2. The cell is realized with an *n*-well enclosing a *p*-diffusion, implemented with a particular geometry [10, 11], in order to optimize the active area density. This is useful to improve the photo-generated current per unit area. In Figure 2 it is possible to see also the equivalent circuit of the solar cell. Since each solar cell must be used as energy harvesting source for an integrated microsystem, realized on the same silicon substrate, it is not possible to exploit the photo-generated power of the deeper junction, since this would imply direct biasing of the junction between *n*-well and substrate, leading to a negative voltage at the *n*-well terminal with respect to the substrate. Furthermore, different cells cannot be connected in series, because they share the same substrate. Figure 3 shows the power curve of the realized cell, obtained with 300-W/m^2 illumination. As the substrate must be short-circuited with the *n*-well, the efficiency of the cell is, unfortunately, reduced by the recombination effect in the base of the parasitic *pnp* vertical transistor.

In order to perform reliable simulations of the whole system, we developed the equivalent electrical model of the microsolar cell, shown in Figure 4, where $I_{\text{ph}} = 12.28\,\mu$A, $A_D = 100\,\mu$m^2, $P_D = 40\,\mu$m, $R_{\text{sh}} = 40\,\text{k}\Omega$, and $R_s = 2.27\,\text{k}\Omega$.

3. Ring Oscillator and Charge Pump

The ring oscillator and the charge pump are shown in Figure 5. They represent the front-end block of the power management circuit. As the solar cell photo-generated voltage cannot exceed 500 mV, in order to obtain at least 4 V across the storage capacitor, a Dickson charge pump has been implemented. The circuit requires two nonoverlapping clock phases, Φ and $\overline{\Phi}$, with amplitude equal to the voltage produced by the microsolar cell V_{ph}. The charge pump operates by moving charges along the diode chain, charging the capacitors to increasing voltages. The charge pump has been designed to obtain a voltage of about 5 V, starting from $V_{\text{ph}} \cong 500$ mV, thus requiring 12 stages. A three stage ring oscillator provides the clock phases for the charge pump with a frequency equal to 29.5 kHz, which corresponds to the best trade-off between the time required to charge C_S and the charge transfer rate. The performance of the system is limited by the supply voltage, which is equal to the open-circuit voltage V_{ph} of the integrated microsolar cell, that forces all transistors to work in the subthreshold region. This circuit provides a very low current flow through each transistor, introducing an efficiency loss in terms of charge transfer and, hence, in terms of charging time. This efficiency loss, however, does not compromise the correct operation of the system, but just increases the charging time. In order to provide a constant voltage of 3.3 V to the load with a significant current for an established time slot, a storage capacitor is necessary. Therefore, the proposed system is only suitable for loads operated in discrete-time regime, such as sensor network nodes [12].

4. Power Management and Monitoring Circuit

The voltage across the storage capacitor C_S (V_S) is monitored with an hysteresis comparator, to verify the charging status. While the capacitor is charging and, hence, V_S is lower than the threshold voltage V_L, the load is disconnected. When V_S is higher than the threshold voltage V_H, the load is connected ($V_L < V_H$), until the capacitor is discharged. The schematic of the hysteresis comparator is shown in Figure 6.

Hysteresis is required to achieve a rising threshold (V_H) different from the falling threshold (V_L). The hysteresis value of this circuit is proportional to the ratio $\alpha = \beta_{M4}/\beta_{M3} = \beta_{M5}/\beta_{M6}$ between the geometries of transistors $M4$, $M3$, and $M5$, $M6$. Assume that initially the input voltage V_{in} is much lower than the reference voltage V_{ref}. In this case, all the current of $M12$ flows through $M2$ and $M5$ ($I_{M2} = I_{M5} = I_{M12}$), while $M1$, $M3$, and $M4$ are off ($I_{M1} = I_{M3} = I_{M4} = 0$) and, consequently, the output voltage V is high. Transistor $M6$ is also on, but no current is flowing in it ($I_{M6} = 0$). Initially, when V_{in} increases, nothing happens, until $V_{\text{in}} \cong V_{\text{ref}}$. At this point, some current starts to flow into $M1$ and $M6$, while the current in $M2$ starts to decrease. In these conditions, we can write

$$\begin{aligned} I_{M1} &= I_{M6} = \alpha I_{M5}, \\ I_{M1} + I_{M2} &= I_{M12}, \end{aligned} \tag{1}$$

and, hence,

$$I_{M2} + \alpha_r I_{M5} = I_{M12}. \tag{2}$$

If V_{in} increases further, $M1$ demands for more current, which can only come from $M6$. Since the current of $M5$ is decreasing and $I_{M6} = \alpha I_{M5}$, at a certain point I_{M5} cannot any longer satisfy (2). Therefore, $M4$ turns on, thus providing the current $M1$ is asking for. At this point, the output voltage of the comparator becomes low. The last value of V_{in} for which (2) is satisfied represents the threshold voltage V_H ($V_H > V_{\text{ref}}$). The value of V_H is controlled by parameter α: the larger is α, the longer (2) is satisfied, and the higher is V_H with respect to V_{ref}. The comparator shows the same behavior symmetrically when V_{in} decreases, leading to a threshold voltage $V_L < V_{\text{ref}}$, which also depends on α.

In order to drive properly the switch M_S, which connects and disconnects the load, a voltage level shifter has been implemented at the output of the comparator. When the voltage across the storage capacitor (V_S) reaches the desired

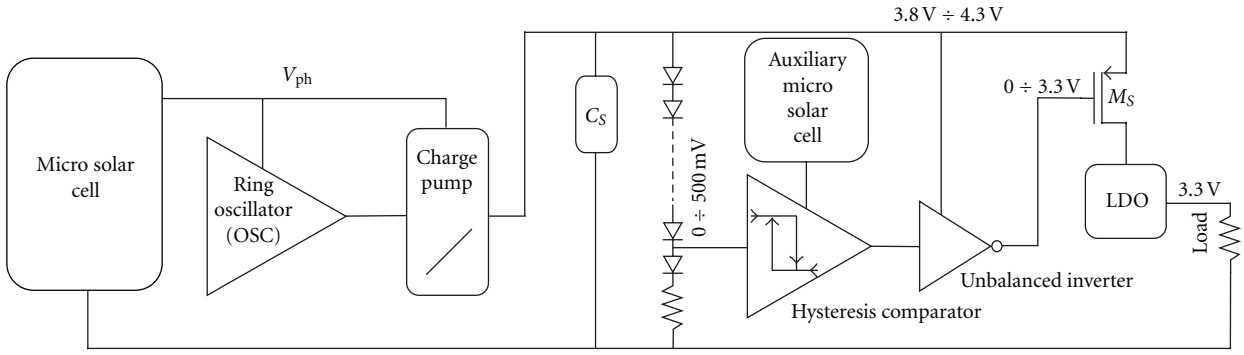

Figure 1: Block diagram of the proposed system.

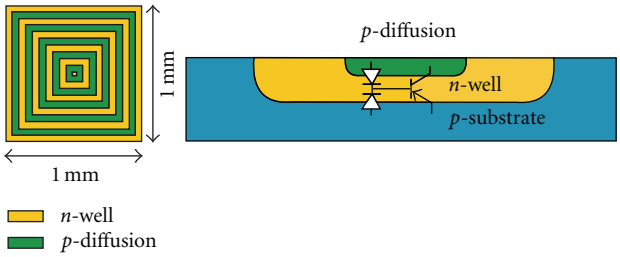

Figure 2: Cross-detection and equivalent circuit of the integrated photovoltaic energy harvesting element.

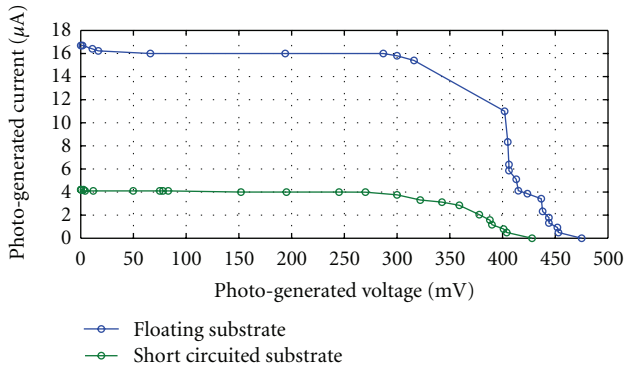

Figure 3: Output power curves of the integrated microsolar cell.

value, the level shifter has to turn on M_S, while, during the charging phase (V_S lower than the desired value), M_S has to be off, in order to disconnect the load and avoid the power consumption. The total power consumption of the power management system is about 500 pW, thus requiring, in principle, a small area for the auxiliary solar cell. The level shifter power consumption is negligible in steady state.

5. Voltage Regulator

In order to provide a fixed 3.3-V power supply to the actual load, a voltage regulator has been implemented. It consists of a bandgap circuit and an LDO circuit. The voltage regulator is supplied only when the voltage across the storage capacitor has reached the proper value. Figure 7 shows the schematic

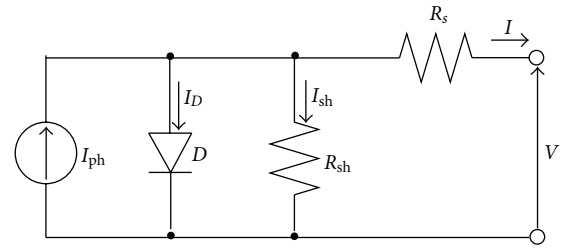

Figure 4: Equivalent circuit model of the integrated microsolar cell.

of the voltage regulator. The total current consumption of the circuit is less than 2 μA.

The bandgap circuit provides a voltage (V_{bg}), stable over temperature, as reference input of the LDO. It operates compensating the negative temperature coefficient of a p-n-junction voltage V_{be}, with the positive temperature coefficient of the thermal voltage V_T. The output voltage of the circuit is, hence,

$$V_{bg} = V_{be} + mV_T, \tag{3}$$

where $m \cong 25$. With the topology used, m is given by

$$m = \frac{R_2}{R_1} \ln\left[\frac{(W_{M1}/L_{M1})}{(W_{M2}/L_{M2})} \frac{A_{Q2}}{A_{Q1}}\right]. \tag{4}$$

Even if the supply voltage follows the discharge curve of the storage capacitor, V_{bg} remains constant.

The LDO provides a stable 3.3-V supply voltage with an input voltage ranging from 3.3 V to 4.8 V, allowing the actual load to operate properly. In particular, the output voltage is given by

$$V_{out} = V_{bg} \frac{R_4 + R_5}{R_4}. \tag{5}$$

Simulation results demonstrate that V_{out} achieves a maximum error of 0.3% over the whole input voltage range. In order to reduce the power dissipation, R_4 and R_5 are in the MΩ range. The total current consumption of the LDO is about 1 μA.

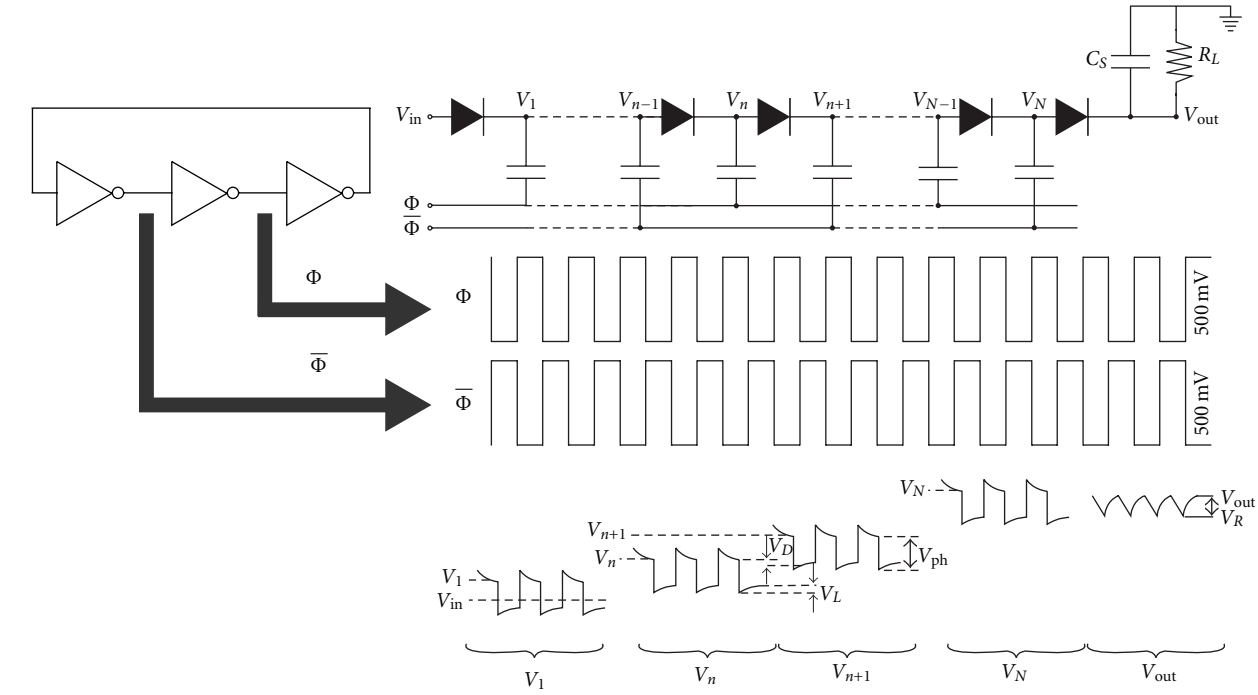

Figure 5: Schematic of the ring oscillator and of the charge pump.

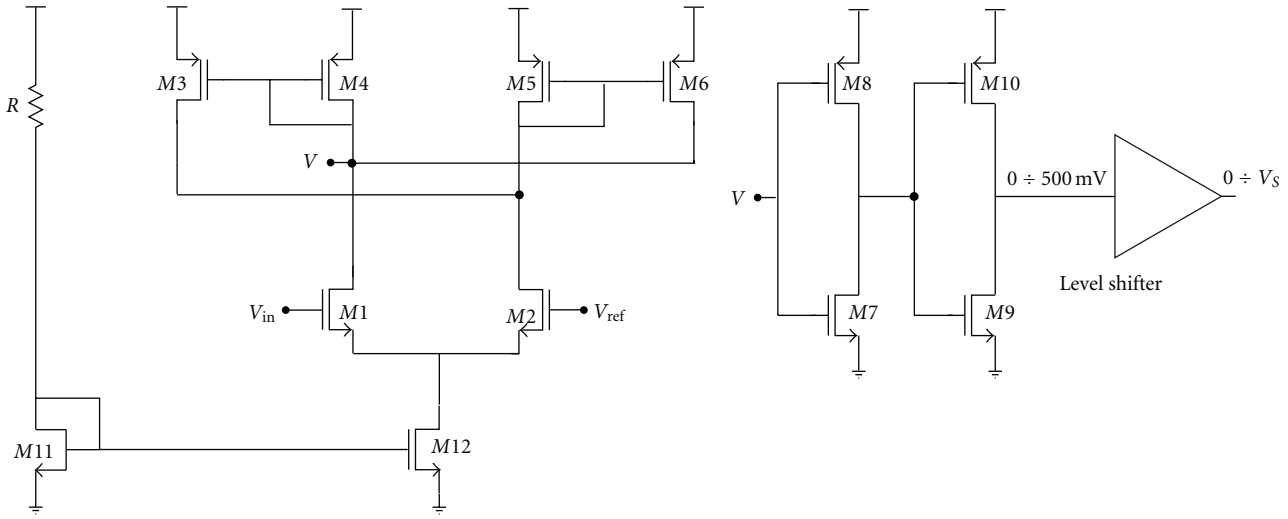

Figure 6: Schematic of the hysteresis comparator.

6. Simulation and Experimental Results

The storage capacitor is an external component, and, hence, its value can be chosen on the basis of the actual load power consumption. In particular, the charge transfer rate of the charge pump in the output voltage ranges from 3.8 V to 4.3 V is less than 10 nA. The charge pump efficiency is quite low, but this is not particularly important, because the system is able to store energy and provide it to the actual load only when it is enough to allow proper operation for an established time slot. Figure 8 shows a simulation of the storage capacitor voltage over a time slot of 7 s, obtained with a capacitance value of 10 nF.

Figure 9 shows the microphotograph of the chip. The chip area is 2.32 mm × 2.54 mm. The power management circuit is shielded from light with a layer of metal, in order to avoid unwanted generation of current in the *p*-*n* junctions of the circuit itself. Therefore, in Figure 9 we also reported the layout of the chip.

Figure 10 shows the measured voltage across the storage capacitor, acquired over a time slot of 15 s, obtained for different values of C_S (47 nF, 100 nF, and 147 nF). The system

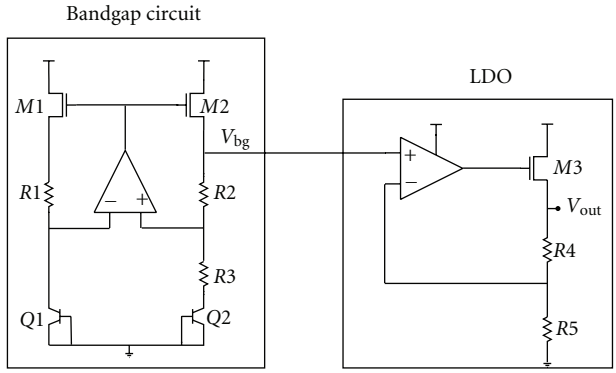

Figure 7: Schematic of the voltage regulator.

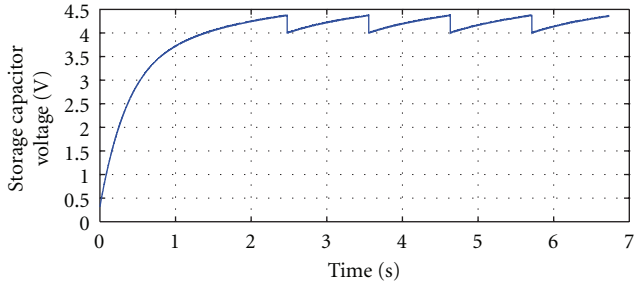

Figure 8: Simulation of the voltage across the storage capacitor with $C_S = 10$ nF.

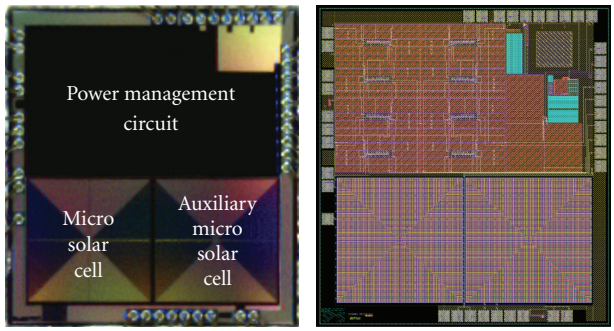

Figure 9: Microphotograph and layout of the realized chip.

is illuminated with a light source, delivering about 300 W/m^2 and the load is a 10-MΩ resistor (1-μW power at 3.3 V). The maximum value of the voltage V_S is adjustable by changing the value of the threshold voltage of the hysteresis comparator. The upper limit of the achievable voltage is a trade-off between the charge-pump transfer rate, the leakage current of the external capacitor, and the current that flows in the resistive string that provides the reference voltage to the comparator. The measurement results show that the system is actually more efficient than expected. Indeed, the time required to charge C_S in the measurement with $C_S = 47$ nF (Figure 10) should be about five times larger than in the simulation with $C_S = 10$ nF (Figure 8), while we obtain almost the same value in the two cases. Actually, in the measurement the voltage drop on the storage capacitor when

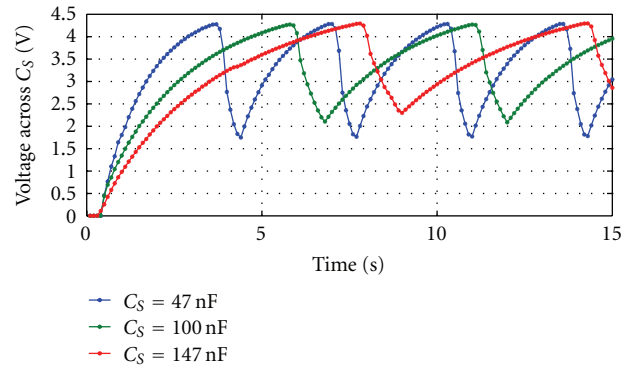

Figure 10: Measurement of the voltage across the storage capacitor with different values of C_S (47 nF, 100 nF, and 147 nF).

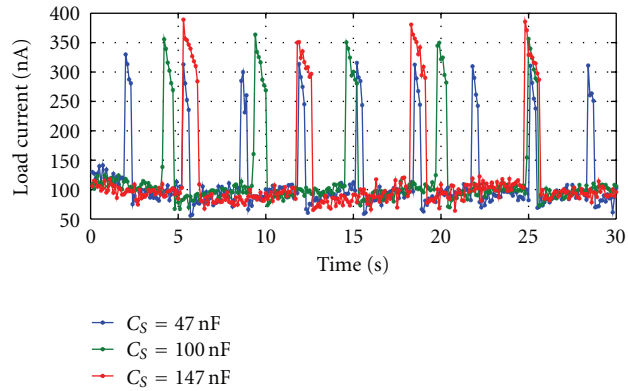

Figure 11: Measurement of the current through the 10-MΩ resistive load with different values of C_S (47 nF, 100 nF, and 147 nF).

the load is connected is larger than in simulation, since the comparator threshold voltage in the measurement is set to a different value than in the simulation.

Figure 11 shows the measured current through the 10-MΩ resistive load over a time slot of 30 s for different values of C_S (47 nF, 100 nF, and 147 nF). The different peak values of the curves are due to the measurement setup sampling frequency. Depending on the capacitance value, the energy available for the load and, hence, the operation duty-cycle changes. With $C_S = 147$ nF, for example, the system provides the same current value as with $C_S = 47$ nF, but for a longer time slot.

7. Conclusions

In this paper we presented an integrated photovoltaic energy harvester, including two 1-mm^2 microsolar cells and a power management circuit, consisting of a charge pump, a comparator, a level shifter, and a linear voltage regulator. The system accumulates energy in an external capacitor and delivers it to the load when the voltage across the capacitor is sufficiently high. The choice of the value of the capacitance determines the operating time slot of the

load. The proposed solution is suitable for discrete-time-regime applications. The experimental results, obtained from a prototype of the system, realized with a 0.35-μm CMOS technology, demonstrate the feasibility of a fully integrated photovoltaic energy harvester.

Acknowledgments

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References

[1] C. W. Seitz, "Industrial battery technologies and markets," *IEEE Aerospace and Electronic Systems Magazine*, vol. 9, no. 5, pp. 10–15, 1994.

[2] A. D. Joseph, "Energy harvesting projects," *IEEE Pervasive Computing*, vol. 4, no. 1, pp. 69–71, 2005.

[3] D. Niyato, M. M. Rashid, and V. K. Bhargava, "Wireless sensor networks with energy harvesting technologies: a game-theoretic approach to optimal energy management," *IEEE Wireless Communications*, vol. 14, no. 4, pp. 90–96, 2007.

[4] D. Brunelli, C. Moser, L. Thiele, and L. Benini, "Design of a solar-harvesting circuit for batteryless embedded systems," *IEEE Transactions on Circuits and Systems I*, vol. 56, no. 11, pp. 2519–2528, 2009.

[5] A. Barnett, C. Honsberg, D. Kirkpatrick et al., "50% efficient solar cell architectures and designs," in *Proceedings of the 4th IEEE World Conference on Photovoltaic Energy Conversion (WCPEC '06)*, vol. 2, pp. 2560–2564, May 2006.

[6] E. L. Ralph, "High efficiency solar cell arrays system trade-offs," in *Proceedings of the 24th IEEE Photovoltaic Specialists Conference*, vol. 2, pp. 1998–2001, Waikoloa, Hawaii, USA, December 1994.

[7] J. McGee, "Photoelectric cells—a review of progress," *IRE Transactions on Component Parts*, vol. 5, no. 1, pp. 2–23, 1958.

[8] N. J. Guilar, T. J. Kleeburg, A. Chen, D. R. Yankelevich, and R. Amirtharajah, "Integrated solar energy harvesting and storage," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 5, Article ID 4806116, pp. 627–637, 2009.

[9] J. Ohsawa, K. Shono, and Y. Hiei, "High-voltage micro solar cell arrays of GaAs with output voltage up to 100 V," in *Proceedings of IEEE/LEOS International Conference on Optical MEMS Conference Digest*, pp. 103–104, 2002.

[10] M. Ferri, D. Pinna, E. Dallago, and P. Malcovati, "Integrated micro-solar cell structures for harvesting supplied microsystems in 0.35-μm CMOS technology," in *Proceedings of IEEE International Conference on Sensors*, pp. 542–545, October 2009.

[11] M. Ferri, D. Pinna, D. Dallago, and P. Malcovati, "Active area density optimization technique for harvester photodiodes efficiency maximization," in *Sensors and Microsystems*, P. Malcovati, A. Baschirotto, A. D'Amico, and C. D. Natale, Eds., pp. 117–120, Springer, Dordrecht, The Netherlands, 2010.

[12] R. Rahul and R. K. A. Velu, "Power management in wireless sensor networks by enhancing the thermoelectric properties of their circuitries," in *Proceedings of the International Conference on Advanced Computer Theory and Engineering (ICACTE '08)*, pp. 817–821, December 2008.