Hindawi Publishing Corporation
Journal of Sensors
Volume 2010, Article ID 937301, 7 pages
doi:10.1155/2010/937301

Research Article

Experiments on the Release of CMOS-Micromachined Metal Layers

Daniel Fernández, Jordi Ricart, and Jordi Madrenas

Electronic Engineering Department, Technical University of Catalonia, UPC, C4 Building, Jordi Girona 1-3, 08034 Barcelona, Spain

Correspondence should be addressed to Daniel Fernández, dfernan@eel.upc.edu

Received 14 December 2009; Accepted 4 March 2010

Academic Editor: Maria Tenje

We present experimental results on the release of MEMS devices manufactured using the standard CMOS interconnection metal layers as structural elements and the insulating silicon dioxide as sacrificial layers. Experiments compare the release results of four different etching agents in a CMOS technology (hydrofluoric acid, ammonium fluoride, a mixture of acetic acid and ammonium fluoride, and hydrogen fluoride), describe various phenomena found during the etching process, and show the release results of multilayer structures.

1. Introduction

During the last decades, many efforts in microelectronics technology have been focused on miniaturization and cost reduction due to the ubiquitous use of electronic portable devices in modern life. New paradigms, as System on Chip (SoC), addressed those challenges by integrating as much electronics as possible in a single package. Later, as sensors begun to be part of many portable devices, the ultimate goal became the sensor integration in the same package together with the electronic circuits, in the so-called Sensing System on Chip (SSoC) [1].

There are many SSoC solutions based on a Multichip Module (MCM), where the sensor and circuit are packaged together but not monolithically; that is, they are in different dies that are electrically connected either with wire-bonding or flip-chip techniques. Monolithic integration, however, can substantially reduce the manufacturing costs and, at the same time, improve the performance of the sensing system as noise and parasitics are greatly reduced due to the shrinking of interconnection lengths.

Monolithic approaches for MEMS-CMOS can be classified [2] in three main categories:

(i) pre-CMOS: when the microsystem is manufactured before the CMOS circuitry [3, 4],

(ii) intra-CMOS: when the MEMS is manufactured between the regular fabrication steps of the CMOS circuit [5],

(iii) post-CMOS, when the microsystem is manufactured after the CMOS circuit.

There are two main variations of the post-CMOS approach. When the microsystem is fabricated by deposition of additional layers above the CMOS wafer, it is called MEMS on top [6, 7]; but if the CMOS layers themselves are used for manufacturing the microsystem, we refer to it as CMOS micromachining.

CMOS micromachining relies on using the own layers of the CMOS process as structural layers for the MEMS device, thereby obtaining an effective monolithic integration between sensor and its electronics. Three micromachining techniques have been proposed in the literature for MEMS release, Deep Reactive Ion Etching (DRIE) [8] (combined with anisotropic bulk etching), bulk micromachining [9, 10] (limited to piezoresistive devices), and the micromachining of the aluminum and polysilicon layers through silicon dioxide removal [10–13]. Among them, bulk and aluminum/polysilicon micromachining have the potential for lesser cost since they do not require sophisticated equipment. In both cases, no specific release mask is required, since for

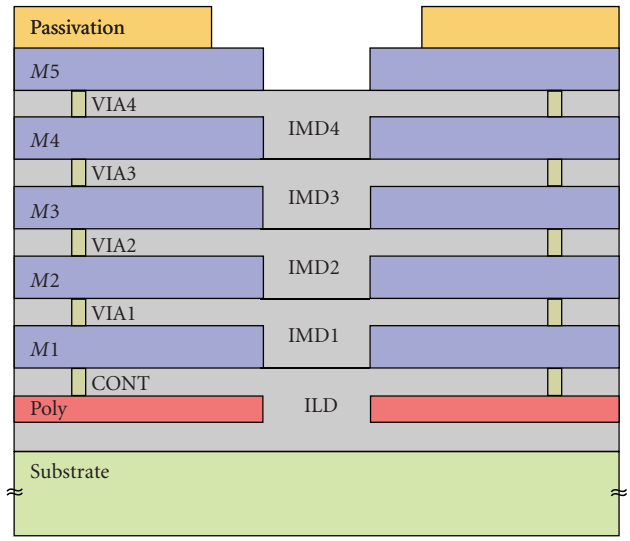

Figure 1: CMOS process cross-section. The etching agent dissolves the oxide (IMD and ILD) around the passivation openings.

bulk micromachining a stack of nonfilled via can usually expose the substrate (typically only with technologies above 0.7 μm of minimum feature size, where the conductive layers are used also as via material); and for aluminum/polysilicon micromachining the passivation layer can effectively be used to protect the structures not to be released.

Despite the fact that numerous devices have been manufactured using aluminum layer micromachining of a CMOS process (such as RF switches [11], resonators [14], RF filters and mixers [15], mass sensors [16], or micromirrors [17]), there is little work in the literature about the specific problems that the release of CMOS-micromachined structures may pose. This paper shows the results on the release of some CMOS-MEMS devices obtained from postprocessing of standard 0.35 μm CMOS-manufactured chips and a description of various phenomena found during the sacrificial material removal. The CMOS process used in the experiments is briefly described in Section 2, while the etching agents and the release results are described in Section 3 and the results with multilayer structures in Section 4.

2. The CMOS Process

The CMOS process used to test the release of the surface-micromachined structures was the *C035M-A* from AMI Semiconductor. It has a 0.35 μm minimum channel length and five metal layers are available for routing. Before each metal layer deposition, a chemical-mechanical polishing (CMP) of the wafer is performed so that the metal depositions are not conformal. Electrical connections between different metal layers are made with tungsten vias. The cross-section of the process layers is depicted in Figure 1.

Metal thickness changes from 630 nm for the bottom metal ($M1$) to 1020 nm for the top metal ($M5$). Each of the metal layers is composed by three sublayers, a first one of titanium and titanium nitride of 100 nm thickness (used to improve electromigration robustness and texture [18, 19]), a main conductor alloy composed of aluminum and copper, and another titanium and titanium nitride sublayer of 30 nm thickness working as an Antireflective Coating (ARC).

The process dielectric is used as a sacrificial material in the MEMS release procedure. Below $M1$ the Interlevel Dielectric (ILD) oxide is deposited, which is a sandwich of doped and nondoped thermally grown silicon dioxide. Above $M1$, the Intermetal Dielectric (IMD) oxide is deposited, which is composed of an 800 nm gap-filling oxide and a PECVD oxide. Passivation thickness is 1100 nm and it is composed of silicon nitride. As experiments show, those differences in metal and oxide compositions and structure have a significant impact on the release result.

3. Experiments on the Etching Process

During the course of our experiments, we have tested four different well-known etching agents and techniques to release the micromechanical devices. We focus first on wet-release solutions, since they provide more reduced cost and do not require sophisticated equipment. The etching agents we tested are hydrofluoric acid (HF), ammonium fluoride (NH_4F), and a mixture of acetic acid (CH_3COOH) and ammonium fluoride. Then, we examine the results with dry hydrogen fluoride (HF) etching.

3.1. Hydrofluoric Acid. Hydrofluoric acid (HF) is one of the most known etching agents for silicon dioxide. It dissolves the silicon dioxide (SiO_2), main compound of the dielectric CMOS process, with the following reactions:

$$\begin{aligned} SiO_2 + 4HF &\longrightarrow SiF_4 + 2H_2O, \\ SiO_2 + 6HF &\longrightarrow H_2SiF_6 + 2H_2O. \end{aligned} \tag{1}$$

When used in a wet release, the HF is dissolved in water, severely reducing its selectivity against aluminum. In our experiments, all releases with hydrofluoric acid ended with critical damage to the MEMS structure (see Figure 2). It has been proposed, however, that using isopropyl alcohol (IPA) instead of water enhances the aluminum selectivity [20], but this option has not been tested.

3.2. Ammonium Fluoride. Ammonium fluoride (NH_4F), also known as Buffered Oxide Etchant (BOE), is another well-known etching agent for silicon dioxide. The chemical reaction is described by

$$SiO_2 + 4HF + 2NH_4F \longrightarrow 2NH_4^+ + SiF_6^{2-} + 2H_2O. \tag{2}$$

As demonstrated by Figure 3, selectivity against aluminum is considerably higher than that of the hydrofluoric acid. However, detailed analysis revealed that the passivation layer is damaged to a point where small structures on top metal, belonging to the CMOS circuitry and covered with the passivation layer, were released.

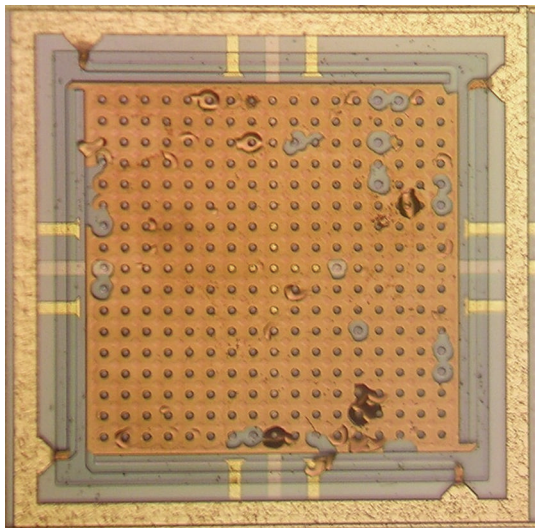

Figure 2: Microphotograph of a CMOS-MEMS membrane released with hydrofluoric acid (HF). Etching time was 6 min and 30 sec and HF concentration was 2.5%. The arms and part of the membrane disappeared, but only few nanometers of silicon dioxide were removed.

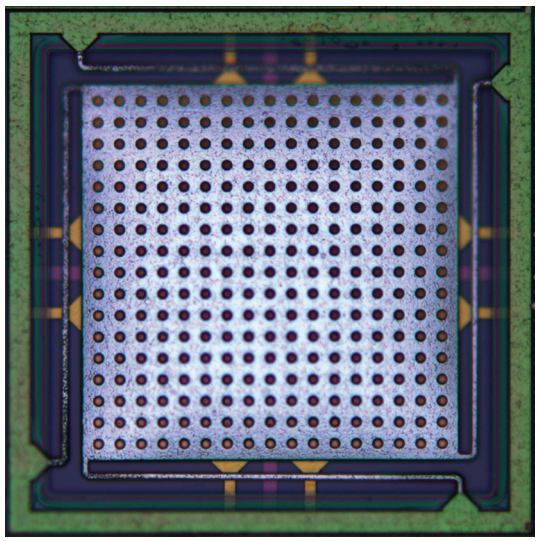

Figure 3: Microphotograph of a CMOS-MEMS membrane released with ammonium fluoride (NH_4F). Etching time was 40 minutes. The etching reached the substrate at 7.6 μm depth, but the passivation layer was damaged.

3.3. Acetic Acid and Ammonium Fluoride. The mixture of acetic acid (CH_3COOH) and ammonium fluoride (NH_4F) is known as a pad-etchant. The mixture dissociates as described by the following reaction:

$$CH_3COOH + NH_4F \longrightarrow (NH_4)^+CH_3COO^- + HF + H_2O, \quad (3)$$

producing water and hydrofluoric acid. However, the mixture has a high selectivity against aluminum, since a protective layer is formed during the first minutes of the etching process [21]. Preliminary results in our experiments also show that selectivity against the passivation layer was excellent even with long etching times, so detailed observations were made to assess the feasibility of this etching agent.

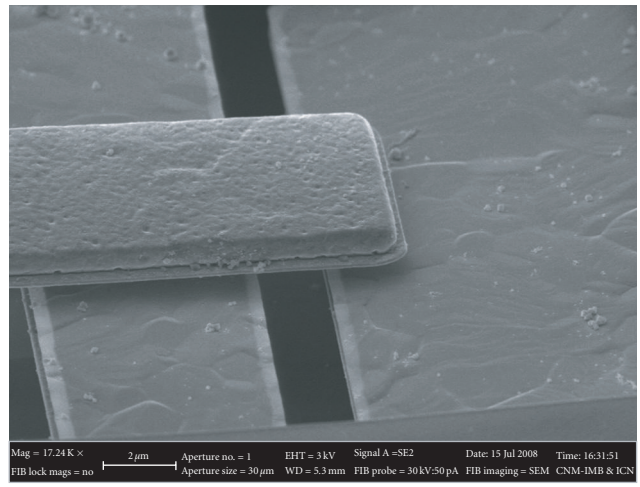

Figure 4: SEM image of a CMOS-MEMS SPST switch released with pad-etchant. Cantilever width is 5 μm and release time is 60 minutes.

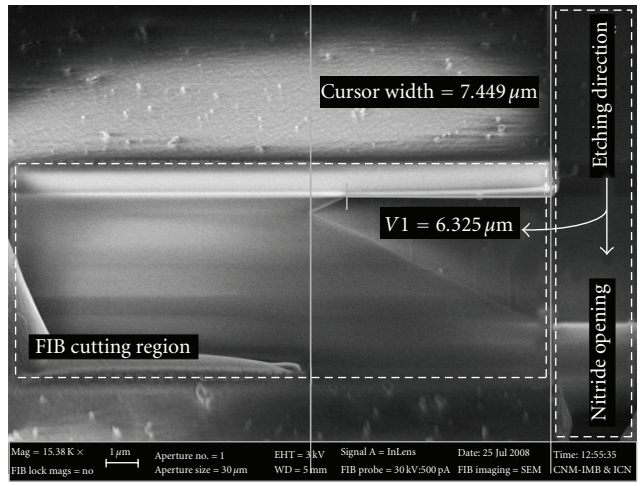

Figure 5: SEM image of a CMOS oxide removal with pad-etchant. Release time is 45 minutes.

Figure 4 shows an SPST (Single-Pole Single-Throw) cantilever-type switch. Note the presence of the ARC Ti/TiN layer below top metal, but not above it. This asymmetry on the layer composition of the structural material could lead to increased residual stress on the structures, causing curling, bending, and even fracture on membranes and cantilevers. It can also be noted that the etching dissolves the aluminum much faster than the ARC layer. Detailed measurements indicate that the ARC Ti/TiN layer is very resilient to the etching agent and is hardly damaged at all.

Figure 5 shows the result of etching through a passivation opening (on the right part of the image) and then performing a cut (in the center of the image) with a Focused Ion Beam

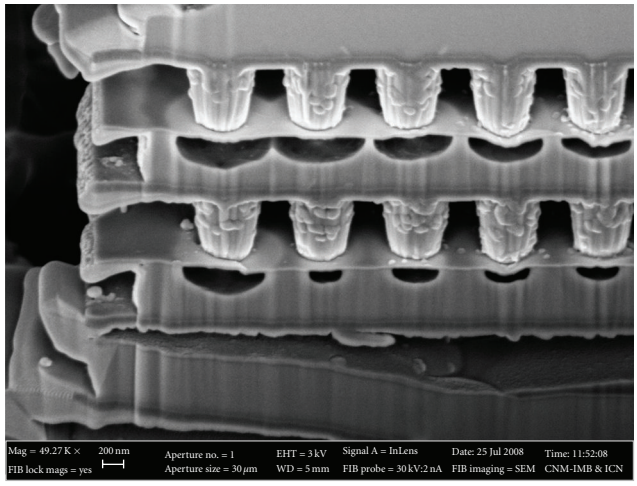

Figure 6: SEM image of a CMOS-MEMS via array released with pad-etchant and cut with FIB. Etching time was 45 minutes.

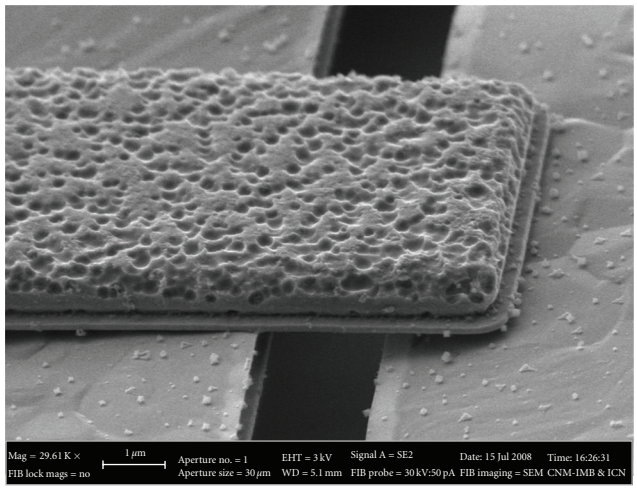

Figure 7: SEM image of a CMOS-MEMS cantilever released with pad-etchant and affected by pitting. Etching time was 45 minutes.

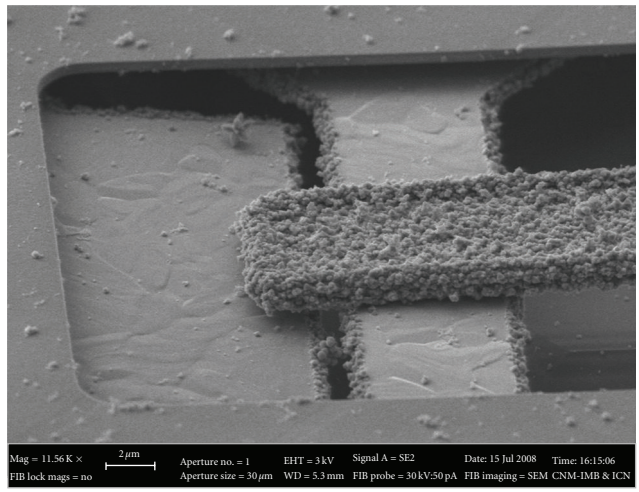

Figure 8: SEM image of a CMOS-MEMS cantilever released with pad-etchant and affected by crystalline contamination. Etching time was 75 minutes.

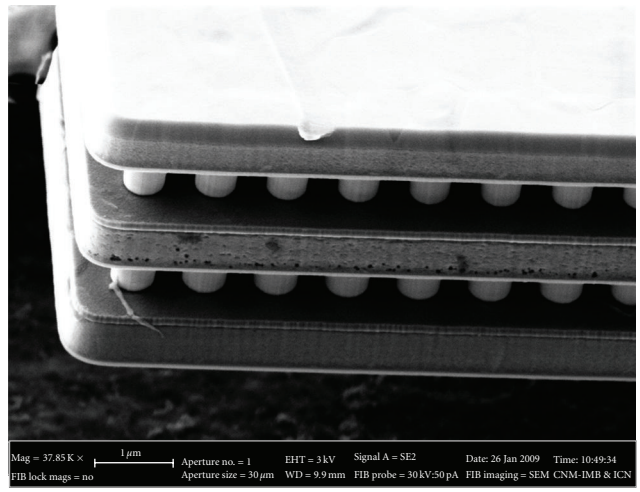

Figure 9: SEM image of a CMOS-MEMS cantilever released with hydrogen fluoride.

(FIB). As it can be seen, the etching agent has dissolved the oxide below the passivation, revealing differences in the etching speed as variations on the slope of the hole. Moreover, the oxide just below the passivation is etched slower than the rest, due either to a composition or structural change on the oxide. Also, the different oxide deposition steps (gap filling oxide and IMD) are revealed on the hole slope.

Despite those good results, more detailed analyses point to significant problems on the release procedure. For example, Figure 6 shows a via array released with pad-etchant after a FIB cut, revealing the internal structure of the aluminum layers. The etching agent enters into the structure from the left part of the image and then dissolves the oxide surrounding the tungsten via. Note, however, that the aluminum layer is also dissolved just below the tungsten via (leaving only the Ti/TiN layer), severely affecting the reliability of MEMS devices manufactured with stacked metal and via layers. Additional experiments also indicate that the oxide etching speed between the vias is 2.5 times higher than that of an oxide block alone (as in Figure 5), probably due to localized reactivity increase caused by the small flow of etching agent between the vias. Other problems found in some sparse samples after release are pitting [21] and crystalline contamination. Pitting phenomenon is shown in Figure 7. It is caused by the formation of low-pH cells that affect the formation of the protective layer around the aluminum and needs to be controlled by an adequate reflow of the etching agent. Crystalline contamination is shown in Figure 8 and affects only the aluminum. High-magnification SEM images reveal that the crystalline substance is octahedral in shape, but the exact chemical composition is unknown.

3.4. Hydrogen Fluoride. Hydrogen fluoride (HF) is the gaseous version of hydrofluoric acid. It dissolves the silicon dioxide through the same chemical reaction, but it is claimed

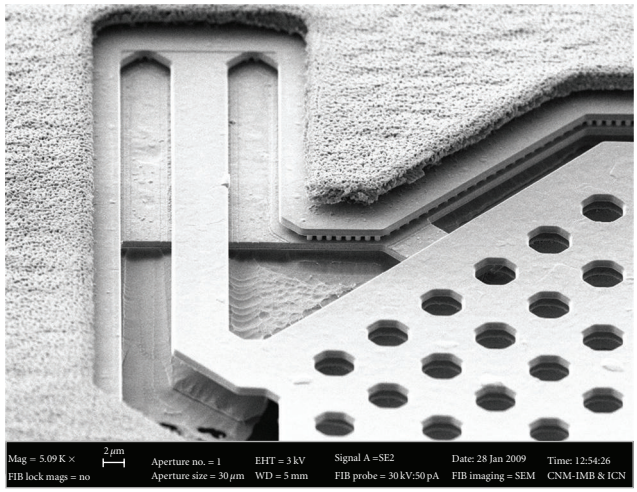

Figure 10: SEM image of a CMOS-MEMS membrane released with hydrogen fluoride. Note the anomalous texture of the passivation layer.

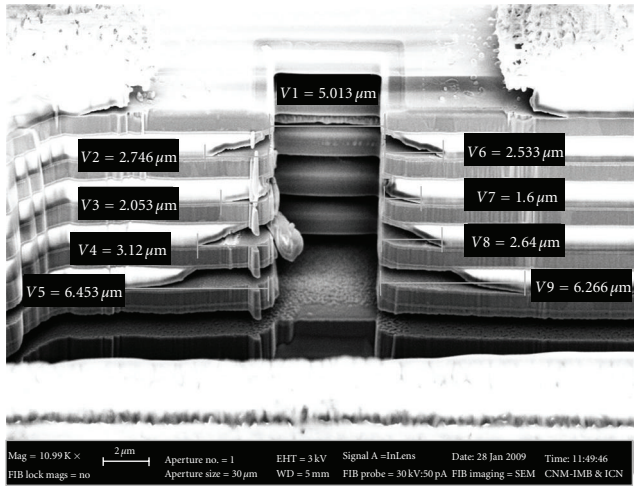

Figure 11: SEM image of a CMOS oxide removal with hydrogen fluoride through a 5 μm × 5 μm square hole on all metal and polysilicon layers.

to have a very high selectivity against aluminum. The releases we present here were performed at Memsstar [22] facilities with their specific equipment. In order to have a representative range of results, release times were varied in the range from 4 minutes to 12 minutes and gas pressure from 35 Torr to 90 Torr.

Figure 9 shows a CMOS-MEMS cantilever released with hydrogen fluoride. The cantilever is made of a stack of $M3$, $VIA3$, $M4$, $VIA4$, and $M5$. As it can be seen, there is no damage to the aluminum structure. Moreover, in contrast to Figure 6, FIB cuts along the via array do not show any internal damage to the structure.

A close view to the passivation layer after performing the release reveals that the silicon nitride is severely damaged during the process. As depicted in Figure 10, the passivation acquires a porous structure. FIB cuts on the nitride indicate that even with short release times almost half of the passivation thickness is damaged. Also, additional analyses reveal that for longer etching times the passivation breaks apart, exposing all circuitry to the etching agent. Note, however, that passivation is the last layer to be deposited over the CMOS wafer and its mask does not require high-resolution alignment, which means that it could be chemically modified to make it resilient to hydrogen fluoride without severely increasing cost. In fact, some foundries offer the possibility to end the process with polymide in addition to the silicon nitride passivation layer. This should work as a protective layer against hydrogen fluoride etchings.

A more severe problem is depicted in Figure 11. The figure shows a FIB cut after a hydrogen fluoride release on a 5 μm × 5 μm square hole on all five metal layers. Note the strange oxide etching profile between the metal layers. The release procedure has dissolved around 2.6 μm of the oxide between $M5$ and $M4$, 1.8 μm of the oxide between $M4$ and $M3$, 2.8 μm between $M3$ and $M2$, 6.3 μm between $M2$ and $M1$, and all oxide between $M1$ and the substrate. Additional SEM images indicate that the hydrogen fluoride also entered the chip laterally, from one side of the subdiced chip and dissolving more than 140 μm of ILD oxide (between $M1$ and the substrate) while only a few microns of IMD (between metal layers) are etched. This different etching speed between the ILD and the IMD can cause severe problems if the hydrogen fluoride reaches the ILD oxide, since it will be dissolved very fast and will cause structural weakness and damage to the CMOS circuitry. It is believed, although not confirmed, that the differences on the oxide structure or deposition techniques and the presence of different dopants on the oxide are the causes of those big differences in the etching speed.

4. Experiments with Multilayer Structures

Multilayer structures—which are composed of a stack of different metal layers connected with vias—can be an effective way to compensate for the high level of residual stress of the MEMS devices. Residual stress causes curling of the released mechanical structures, and, in some cases, may even cause breakage. Residual stress is reduced by applying a thermal treatment (annealing) to the deposited layers, but when CMOS surface micromachining is used on a standard or commercial CMOS process this is usually not an option since the manufacturing process is strictly optimized to maximize transistor performance and yield.

Despite the problems shown in Figure 6, various multilayer membranes were designed and released using a 60-minute etching with acetic acid and ammonium fluoride. As shown in Figure 12, they had an octagonal shape with a 50 μm apothem and almost all of them remained held together after the release despite the internal damage to the aluminum layers previously shown. A profile measurement taken with an interferometer for a single-layer membrane (manufactured with $M5$), for a 2-layer (manufactured with $M4$, $VIA4$, and $M5$), and for a 3-layer membrane (manufactured with $M3$, $VIA3$, $M4$, $VIA4$, and $M5$) is shown in Figure 13. Measured curling radius for the single-layer

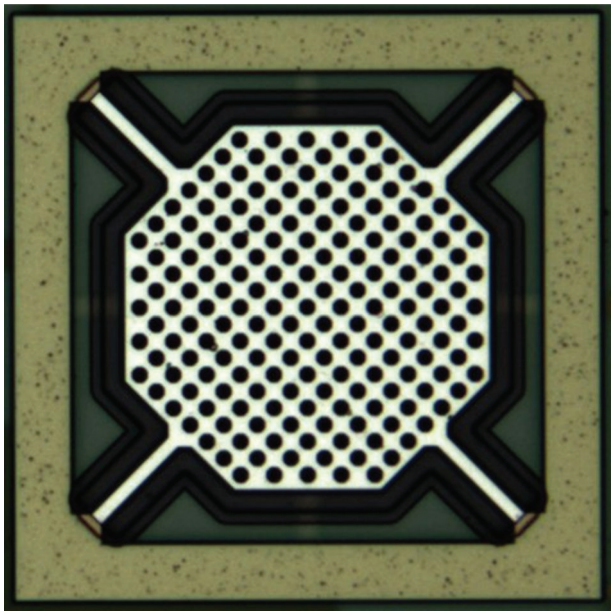

Figure 12: Microphotograph of one of the CMOS-MEMS membranes used in the profile measurements shown in Figure 13. Octagon apothem is 50 μm in length.

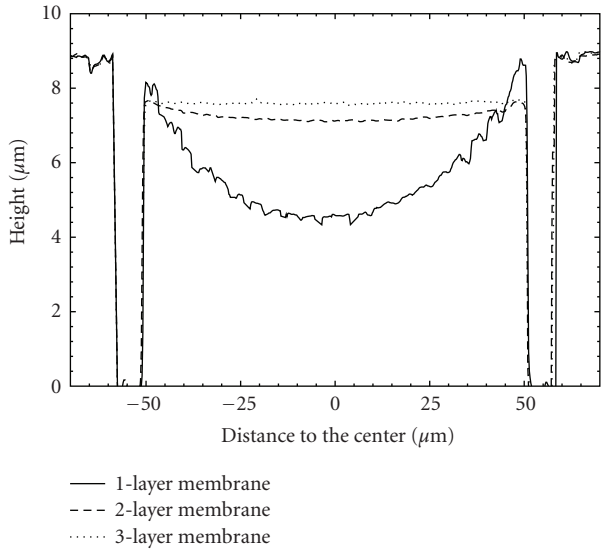

Figure 13: Profile measurement of different 100 μm CMOS-MEMS membranes composed of one, two and three metal layers. Passivation is around 9 μm height and substrate around 0 μm. The membranes were released with pad-etchant after 60 minutes.

membrane is around 0.39 mm, for the 2-layer is 3.72 mm, and for the 3-layer is 41.3 mm.

However, when releasing more complex structures (such as comb drivers), the yield or survival rate decreases dramatically because the different layers do not hold together. Figure 14 shows an interferometer view of a 3-layer comb-type MEMS device released under the same conditions. As it can be seen, some of the fingers are significantly more curled than the others, suggesting that with narrow and long

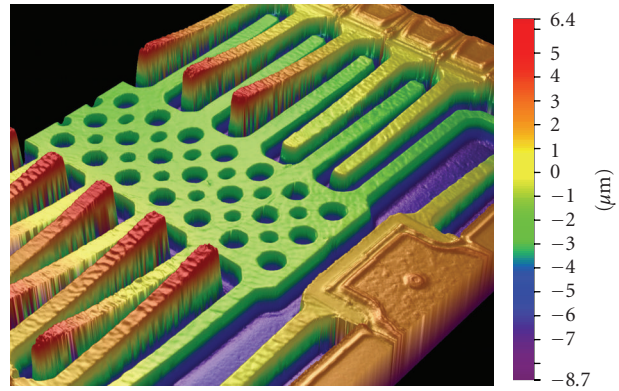

Figure 14: Interferometer view of a 3-layer comb-type CMOS-MEMS actuator after a release with pad-etchant, suggesting breakage between the different layers in some of the fingers. The structure was released with pad-etchant after 60 minutes.

structures the internal damage to the aluminum is so severe that the vias are not able to hold the layers together.

Another application of multilayer structures is to improve stiction robustness. Stiction causes the released micromechanical parts to become adhered together due to the surface attractive forces between them. For example, in case of membranes (which have high surface), a complete contact between the bottom fixed plate and the top free plate is likely to cause stiction if the restoring mechanical force is not high enough. In this case, for improving stiction robustness dimples can be used. Dimples are small bumps in the membrane surface that reduce the total contact area and, thus, the stiction force. They are widely used in commercial MEMS processes such as PolyMUMPs [23], and their effectiveness as a low-cost solution has been demonstrated over the years. In a CMOS-MEMS process, the same effect of dimples can be accomplished by the localized use of vias. In our case, a small 3×3 via matrix from $M5$ to $M4$ has proven to be a very effective dimple structure for a $M5$ membrane.

5. Conclusions

In this paper we have compared the release results with four different etching agents for surface micromachining of the aluminum layers in a standard CMOS technology (hydrofluoric acid, ammonium fluoride, a mixture of acetic acid and ammonium fluoride, and hydrogen fluoride), and we have pointed out some of the main problems and side effects, such as surface damage to the aluminum and passivation, internal damage to the structures, pitting, contamination and nonuniform etching speed. We have also shown the release results of multilayer structures designed with a stack of various metal layers and vias, revealing yield or survival rate problems in some of the designs.

Although each release agent has its limitations, in our opinion the pad-etchant provides the best overall results. Note, however, that hydrogen fluoride gives the best selectivity against the aluminum conductive layers and the tungsten

vias, but, unfortunately, the problems with the passivation and ILD oxide layers make it very difficult to use as a release agent for CMOS-MEMS designs. If those problems are solved (probably by introducing modifications to the CMOS process), hydrogen fluoride promises to become the best etching agent to CMOS-MEMS processes.

In conclusion, despite the interest of CMOS-MEMS devices, the release or etching process used to remove the oxide sacrificial material is not exempt from problems, mainly caused by the sophistication that the newer CMOS technology requires to attain high yield levels and submicron resolutions on the deposited layers. The particularity of each CMOS process and technological family make the release procedure entirely dependant on the manufacturing details of each CMOS foundry, and, in most cases, a close collaboration with the foundry or a technological change on the CMOS process may be required in order to get satisfactory results on an industrial-scale production.

Acknowledgments

This work was supported in part by the Spanish Ministry of Science and Innovation under Project TEC2008-06028/TEC and Ministry of Industry, Tourism and Commerce under Project TSI-020400-2008-121. The authors wish to thank Juan J. Valle and Laura Barrachina from Baolab Microsystems for their help taking the SEM images shown in this paper.

References

[1] O. Brand, "Microsensor integration into systems-on-chip," *Proceedings of the IEEE*, vol. 94, no. 6, pp. 1160–1176, 2006.

[2] H. Baltes, O. Brand, A. Hierlemann, D. Lange, and C. Hagleitner, "CMOS MEMS—present and future," in *Proceedings of the 15th IEEE International Conference on Micro Electro Mechanical Systems*, pp. 459–466, 2002.

[3] J. A. Yasaitis, M. Judy, T. Brosnihan, et al., "A modular process for integrating thick polysilicon MEMS devices with sub-micron CMOS," in *Micromachining and Microfabrication Process Technology VIII*, J. A. Yasaitis, M. A. Perez-Maher, and J. M. Karam, Eds., vol. 4979 of *Proceedings of SPIE*, pp. 145–154, San Jose, Calif, USA, January 2003.

[4] J. Smith, S. Montague, J. Sniegowski, J. Murray, and P. McWhorter, "Embedded micromechanical devices for the monolithic integration of MEMS with CMOS," in *Proceedings of the International Electron Devices Meeting*, pp. 609–612, 1995.

[5] T. Scheiter, H. Kapels, K.-G. Oppermann, et al., "Full integration of a pressure-sensor system into a standard BiCMOS process," *Sensors and Actuators A*, vol. 67, no. 1–3, pp. 211–214, 1998.

[6] A. Mehta, M. Gromova, C. Rusu, et al., "Novel high growth rate processes for depositing poly-SiGe structural layers at CMOS compatible temperatures," in *Proceedings of the 17th IEEE International Conference on Micro Electro Mechanical Systems (MEMS '04)*, pp. 721–724, 2004.

[7] A. Mehta, M. Gromova, P. Czarnecki, K. Baert, and A. Witvrouw, "Optimisation of PECVD poly-SiGe layers for MEMS postprocessing on top of CMOS," in *Proceedings of the 13th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS '05)*, vol. 2, pp. 1326–1329, 2005.

[8] H. Xie, L. Erdmann, X. Zhu, K. J. Gabriel, and G. K. Fedder, "Post-CMOS processing for high-aspect-ratio integrated silicon microstructures," *Journal of Microelectromechanical Systems*, vol. 11, no. 2, pp. 93–101, 2002.

[9] C.-L. Dai, J.-H. Chiou, and M. S.-C. Lu, "A maskless post-CMOS bulk micromachining process and its application," *Journal of Micromechanics and Microengineering*, vol. 15, no. 12, pp. 2366–2371, 2005.

[10] H. A. C. Tilmans, K. Baert, A. Verbist, and R. Puers, "CMOS foundry-based micromachining," *Journal of Micromechanics and Microengineering*, vol. 6, no. 1, pp. 122–127, 1996.

[11] C.-L. Dai, "A maskless wet etching silicon dioxide post-CMOS process and its application," *Microelectronic Engineering*, vol. 83, no. 11-12, pp. 2543–2550, 2006.

[12] A. Uranga, J. Teva, J. Verd, et al., "Fully CMOS integrated low voltage 100 MHz MEMS resonator," *Electronics Letters*, vol. 41, no. 24, pp. 1327–1328, 2005.

[13] J. Teva Meroño, *Integration of CMOS-MEMS resonators for radiofrequency applications in the VHF and UHF bands*, Ph.D. dissertation, Departament d'Enginyeria Electrònica, UAB, 2007.

[14] C.-L. Dai and W.-C. Yu, "A micromachined tunable resonator fabricated by the CMOS post-process of etching silicon dioxide," *Microsystem Technologies*, vol. 12, no. 8, pp. 766–772, 2006.

[15] A. Uranga, J. Verd, J. L. Lopez, et al., "Fully integrated MIXLER based on VHF CMOS-MEMS clamped-clamped beam resonator," *Electronics Letters*, vol. 43, no. 8, pp. 452–453, 2007.

[16] J. Verd, A. Uranga, G. Abadal, et al., "Monolithic mass sensor fabricated using a conventional technology with attogram resolution in air conditions," *Applied Physics Letters*, vol. 91, no. 1, Article ID 013501, 3 pages, 2007.

[17] Y.-C. Cheng, C.-L. Dai, C.-Y. Lee, P.-H. Chen, and P.-Z. Chang, "A circular micromirror array fabricated by a maskless post-CMOS process," *Microsystem Technologies*, vol. 11, no. 6, pp. 444–451, 2005.

[18] K. Rodbell, D. Knorr, and D. Tracy, "Texture effects on the electromigration behavior of layered Ti/AlCu/Ti films," in *Materials Research Society Symposium Proceedings*, pp. 107–113, Materials Research Society, 1993.

[19] D. P. Tracy, D. B. Knorr, and K. P. Rodbell, "Texture in multilayer metallization structures," *Journal of Applied Physics*, vol. 76, no. 5, pp. 2671–2680, 1994.

[20] P. Gennissen and P. French, "Sacrificial oxide etching compatible with aluminum metallization," in *Proceedings of the International Conference on Solid State Sensors and Actuators (TRANSDUCERS '97)*, vol. 1, pp. 225–228, Chicago, Ill, USA, 1997.

[21] J. Bühler, F.-P. Steiner, and H. Baltes, "Silicon dioxide sacrificial layer etching in surface micromachining," *Journal of Micromechanics and Microengineering*, vol. 7, no. 1, pp. R1–R13, 1997.

[22] Memsstar, http://www.memsstar.com.

[23] "MEMSCAP MUMPs processes," http://www.memscap.com/en_mumps.html.