

Research Article

Analysis on Structural Stress of 64×64 InSb IRFPAs with Temperature Dependent Elastic Underfill

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To improve the reliability of InSb IRFPAs, underfill has usually been filled between InSb chip and Si ROIC. Around the glass transition temperature, underfill shows viscoelasticity, yet, far below it, which shows apparently temperature dependent mechanical properties. Basing on the temperature dependent elastic model of underfill, firstly a small format array of 8×8 elements InSb IRFPAs is investigated by changing indium bump diameters and heights; simulated results show that the maximum stress in InSb chip has nothing to do with underfill height and is dependent on indium bump diameter; the varying tendency is just like the horizontally extended letter U. When indium bump diameter is set to $24 \mu\text{m}$ with height $21 \mu\text{m}$, the maximal stress in InSb chip reaches minimum. To learn the stress in 64×64 elements in short time, with the above optimal structure, InSb IRFPAs array scale is doubled once again from 8×8 to 64×64 elements. Simulation results show that the stress maximum in InSb chip is strongly determined by arrays format and increases with array scale; yet, the stress maximum in Si ROIC almost keeps constant and is independent on array sizes; besides, the largest stress locates in InSb chip, and the stress distribution in InSb chip is uniform.

1. Introduction

An indium antimonide (InSb) infrared focal plane arrays (IRFPAs) detector with cut-off wavelength of $5.5 \mu\text{m}$ at 77 K has been widely used in military guiding system and civilian optoelectronic equipment for higher quantum efficiency and good responsivity in the $3\text{--}5 \mu\text{m}$ spectral range [1]. In order to achieve better performance, InSb IRFPAs detector is usually fabricated by flip chip bonding technology; that is, the InSb chip and Si readout integrated circuit (ROIC) are fabricated on different substrates and, subsequently, indium bumps are formed firstly on both InSb chip and Si ROIC; then InSb chip and Si ROIC are aligned and force is applied to cause indium bumps to cold-weld together; after that, to improve the reliability of flip chip packaging, an epoxy-based material, called underfill encapsulant, is usually filled in the gap between InSb chip and Si ROIC substrate [2–8]. Hybrid InSb IRFPAs detector is back illuminated. For higher quantum efficiency, InSb substrate must be thinned to about $10 \mu\text{m}$. In order to achieve lower level of electronic noise to

the photon noise limit, it is necessary to cryogenically cool InSb IRFPAs to liquid nitrogen temperature (77 K); yet InSb IRFPAs detector is usually assembled and stored at room temperature (300 K). When the temperature rapidly reduces from 300 K to 77 K, here the temperature drop range is about 223 K; due to thermal mismatch of the different coefficients of thermal expansion (CTE) of Si ROIC circuit and InSb chip, the induced thermal stresses are the major causes of fracture in InSb chip, especially in larger format IRFPAs, which limits the finished product ratio. So it is necessary to analyze the induced thermal stress values and their distribution in InSb chip.

At present, the reliability of flip chip assemblies is usually assessed by finite element simulations in conjunction with experiment [9–14]. Therefore, finite element analysis plays an important role in optimization design of packaging. Within the approach, the selection of material models is very significant. Underfill encapsulant is usually described as linear and temperature independent, constant elastic material [15, 16], or described as viscoelastic material around its glass

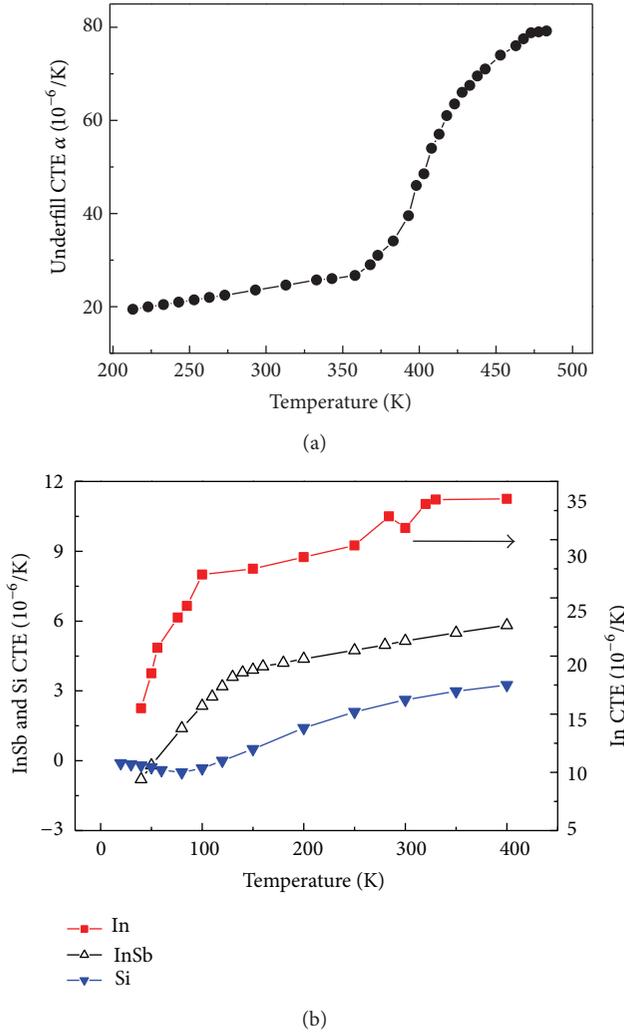


FIGURE 1: Evolution of CTE α with temperature for (a) underfill and (b) InSb, silicon, and indium.

transition temperature T_g [17]. InSb chip fracture usually happens in thermal shock from 300 K to 77 K, and during this temperature range the mechanical properties of underfill vary with temperature and show obvious temperature dependent elasticity [18, 19]. So, in this paper, the temperature dependent elastic model of underfill is adopted to analyze the structure stress of InSb IRFPAs. Besides, the temperature dependent mechanical properties of the other materials are also adopted.

Simulating large format InSb IRFPAs in three dimensions is very time and memory consuming. Here two-step method is used to research stress and its distribution in InSb chip [20]. Based on the temperature dependent CTE models of all materials, firstly, an 8×8 InSb IRFPAs detector is studied by varied indium bump diameters and height in a suitable range with fixed InSb thickness of $10 \mu m$; thus the optimum indium bump diameter and height are obtained. Then, the sizes of InSb IRFPAs are doubled once again to learn the stress value varying tendency with array scale; thus, the thermal stress dependence of indium bump locations and the thermal stress value versus the arrays format are studied, and the stress and

its distribution of 64×64 InSb IRFPAs are also obtained in a short time. All these are benefits to further optimally design and improve the reliability of hybrid InSb IRFPAs.

2. Materials Properties

Below glass transition temperature (T_g), underfill shows significant temperature dependent elasticity. Linear CTE of underfill is plotted in Figure 1(a) [18]. When the temperature approaches 398 K, the slope of curve increases rapidly, which is the signature of T_g . Below 363 K, the CTE α has a linear raising trend and increases from $19.4 \times 10^{-6} K^{-1}$ at 213 K to $26.7 \times 10^{-6} K^{-1}$ at 358 K, so it can be expressed as follows [18]:

$$\alpha(T) = 22.46 \times 10^{-6} + 5.04 \times 10^{-8}T \text{ (K}^{-1}\text{)}. \quad (1)$$

The dynamic mechanical properties of underfill are also acquired with dynamic mechanical thermal analysis (DMTA) [18]. The DMTA results show that the elastic modulus E at 223 K is approximately 9.5 GPa, as T increases and E

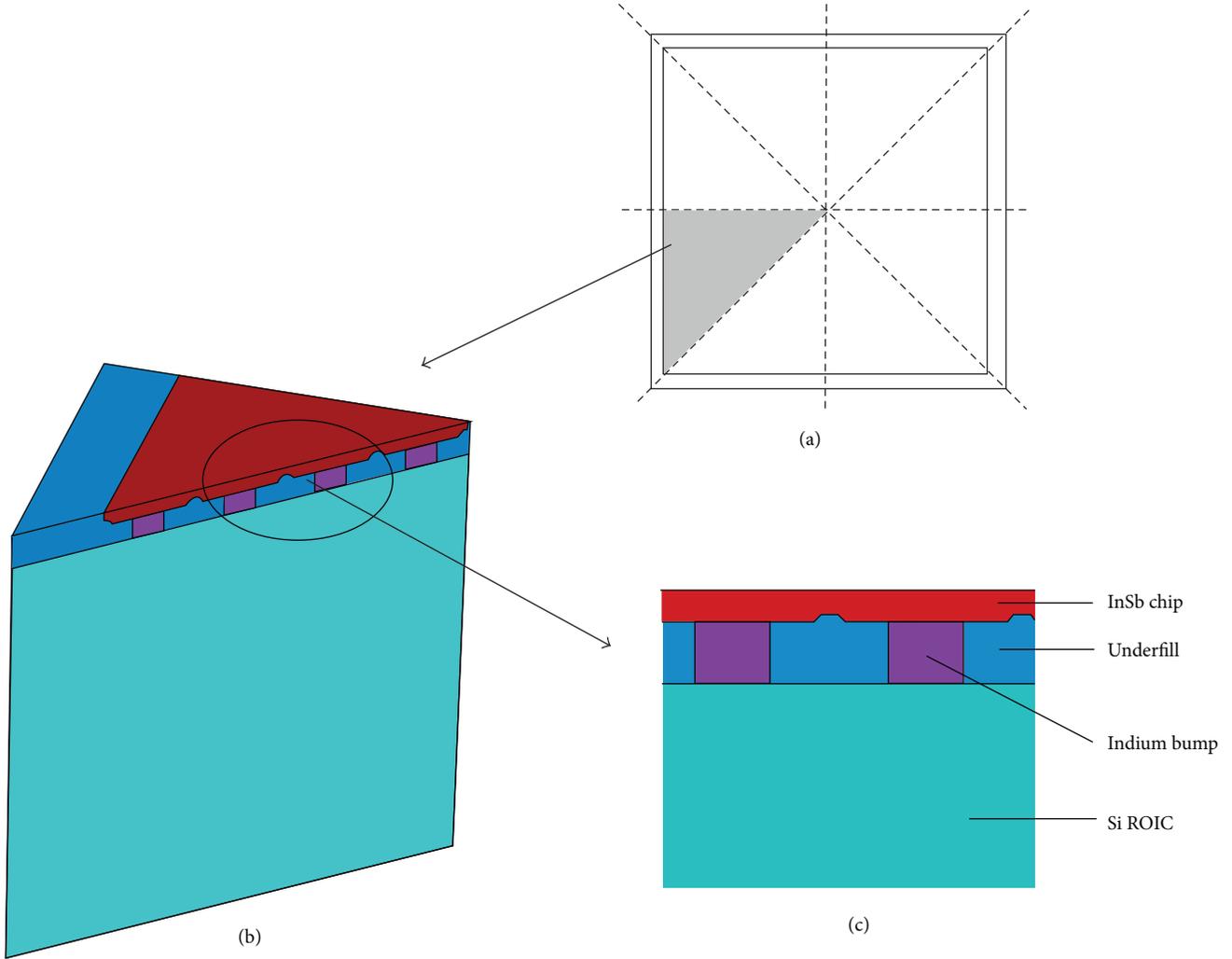


FIGURE 2: Schematic of three-dimensional model for InSb IRFPAs: (a) top-down view schematic drawing of the full model, (b) one-eighth finite element model due to symmetry, and (c) enlarged side view.

decreases gradually. At 298 K, E is about 8.2 GPa. When T approaches 398 K, E decreases rapidly. Based on the TMA and DMTA data, the stress index $\alpha(T) \cdot E(T)$ of this cured underfill is approximately a constant and, below the glass transition T_g , it is described as follows:

$$\alpha(T) \cdot E(T) \approx 0.2 \text{ MPa/K.} \quad (2)$$

Indium bump deformation is strongly temperature and time dependent, which is known to be viscoplastic. So, here Anand's viscoplastic model has been used to describe mechanics of constitutive relationship of indium bump, and the material parameters in Anand's model were acquired by Chang and McCluskey in 2009 [21]. The CTEs for indium as functions of temperature, implemented in the model, are given in Figure 1(b); InSb chip and Si ROIC are all considered to be linear elastic materials; the temperature dependence of CTEs for Si and InSb is also shown in Figure 1(b) [22, 23].

3. Model Creation and Parameters Selection

InSb IRFPAs detector is composed of InSb chip, indium bumps array, Si ROIC substrate, and underfill material. Here indium bump is assumed to be octagonal prism with no defects existing in the whole device. The thickness of InSb chip is set to $10 \mu\text{m}$. In 8×8 InSb IRFPAs, InSb chip dimensions are $400 \mu\text{m} \times 400 \mu\text{m} \times 10 \mu\text{m}$, Si ROIC substrate dimensions are $500 \mu\text{m} \times 500 \mu\text{m} \times 300 \mu\text{m}$, indium bump height is separately taken to $9 \mu\text{m}$, $15 \mu\text{m}$, and $21 \mu\text{m}$, and its diameter increases from $12 \mu\text{m}$ to $36 \mu\text{m}$ in step of $4 \mu\text{m}$. Using the geometrical symmetry, only one-eighth of the overall package is modeled, which is given in Figure 2. To describe the real mesa structure locating between neighboring detectors elements, the trapezoidal prisms are employed here.

In the whole model, symmetry boundary condition is utilized, meshing the whole model free. Flip chip process is completed at 370 K; after that, underfill is dispensed between InSb chip and Si ROIC substrate. The curing process is also

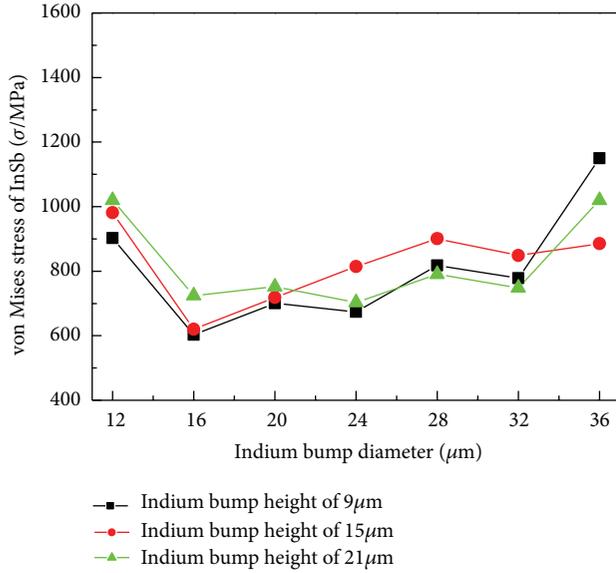


FIGURE 3: von Mises stress maximum values of InSb as a function of varied indium bump diameter with different indium bump heights.

TABLE 1: Material parameters.

Materials	Elastic modulus [E/MPa]	Poisson's ratio [μ]	CTE [$\alpha/(\times 10^{-6}/K)$]
Si ROIC	163000	0.28	See Figure 1(b)
InSb chip	409000	0.35	See Figure 1(b)
Indium bump	10600	0.45	See Figure 1(b)
Underfill	See (2)	0.3	See Figure 1(a)

operated at 370 K; at this temperature, no residual stress is assumed to exist within the package. In the simulation, the temperature is gradually reduced from 370 K to 77 K, no transient heat transfer is considered, and the temperature within the model is assumed to be uniform. Both InSb chip and Si ROIC substrate are considered to be linear elastic materials. The temperature dependent elastic model and Anand's viscoplastic model have separately been used to describe mechanics of constitutive relationship of underfill and indium bumps. All the employed parameters are listed in Table 1 [18, 21–23].

4. Simulation Results and Analysis

4.1. 8×8 InSb IRFPAs. To learn the effects from indium bump sizes to von Mises stress and its distribution in InSb chip, a small format array of 8×8 elements InSb IRFPAs model is selected, and the simulation results are given in Figure 3. In favor of comparison, for any structure, model meshing, constraints, and loading are all identical. Here indium bump diameter increases from 12 μm to 36 μm in step of 4 μm with fixed indium bump heights of 9 μm , 15 μm , and 21 μm . Apparently, when indium bump height is fixed at 21 μm , as indium bump diameters increase from 12 μm to 36 μm , the maximal von Mises stress in InSb chip firstly

decreases and then fluctuates slightly at 700 MPa from 16 μm to 32 μm ; once the diameters are over 32 μm , it increases sharply. The total varying tendency with increased diameters is just like the horizontal extended letter U, and the other heights have similar varying tendency. When indium bumps height increases from 9 μm to 21 μm , the stress values change little. This phenomenon is obviously different from that with the constant elastic underfill and viscoplastic underfill, where the maximal von Mises stress in InSb chip decreases with increasing underfill height [17]. It is worth noticing that as indium bump height is set to 21 μm , the maximum stress in InSb chip has a stable flat range. During the flat range, the maximum stress reaches the minimum with indium bump diameter of 24 μm . So, indium bump height of 21 μm and diameter of 24 μm as an optimum structure are selected.

The von Mises stress distribution of indium bumps is illustrated in Figure 4. Apparently the maximal von Mises stress appears on contact area between indium bumps and InSb chip, locating on the corner, which has the largest distance to neutral point. Besides, on top surface of indium bump, the stress shows apparent gradient distribution, which is amplified in the right part of Figure 4. For indium bumps, locating on diagonal, the stress reduced direction is along the diagonal line from far to the neutral point. For nondiagonal sites, the gradient direction is along the line from indium bumps position to the neutral point. So, the stress distribution on top surface shows circle structure from outside to inside. Besides, the maximal stress of indium bumps almost keeps at 16.2 MPa; compared with that of InSb chip, it is much smaller, almost 2.1%. The stress concentrating in InSb chip originates from the thinner InSb chip (10 μm), as the InSb chip becomes thinner and thinner by chemical mechanical polishing technology, its antideformation intensity becomes smaller and smaller, which makes the maximal stress redistribute and shift to InSb chip.

4.2. 64×64 InSb IRFPAs. For obtaining the von Mises stress and its distribution in 64×64 InSb IRFPAs in short time period, a typical structure with indium bump diameter of 24 μm and height of 21 μm is selected. As array scale increases from 8×8 to 64×64 , simulation results are shown in Figure 5. Apparently, von Mises stress maximum in InSb chip increases continually with array scale, as the array scale increases from 8×8 to 32×32 ; the maximal von Mises stress in InSb chip increases almost linearly and then increases faster after 32×32 . However von Mises stress maximum in Si ROIC almost keeps constant. Besides, compared with the maximal stress in InSb chip, the maximal stress in Si ROIC is almost 50% in 8×8 and about 26% in 64×64 , which means that von Mises stress in Si ROIC is much smaller than that in InSb chip; when array scale increases, the phenomenon comes from employed thinner InSb chip (10 μm), which tends to distortion compared with thicker 300 μm Si ROIC.

To learn von Mises stress dependence of indium bump locations, here some typical sites are selected; one group is located on diagonal; the others are situated in the middle column or row array parallel to the sides; their spacing is 0.28 mm and 0.20 mm. Simulation results are shown in

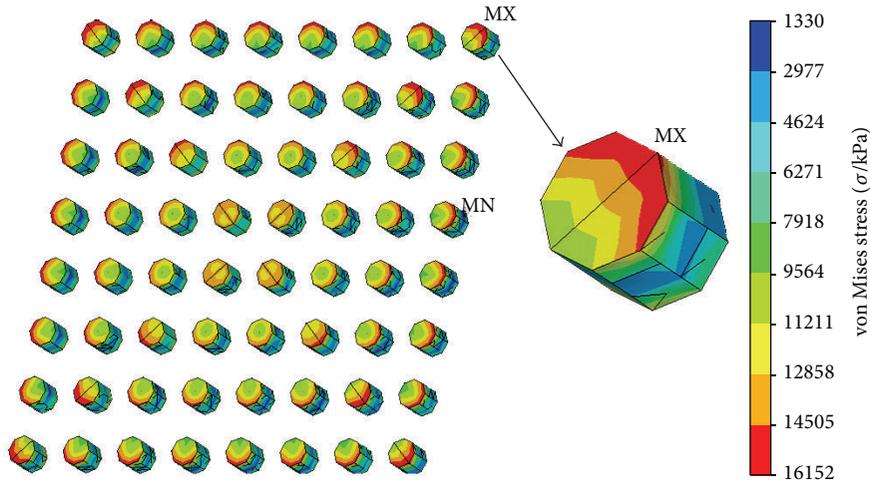


FIGURE 4: von Mises stress distribution of 3D indium bump array.

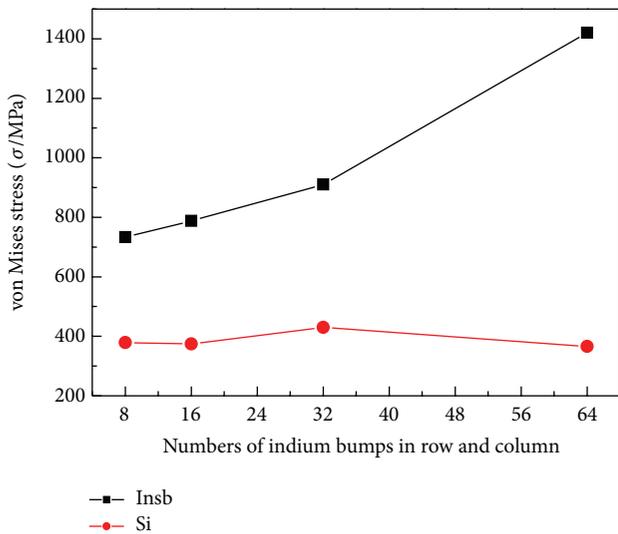


FIGURE 5: Mises stress maximum of InSb chip and Si ROIC VS numbers of indium bumps in row and column.

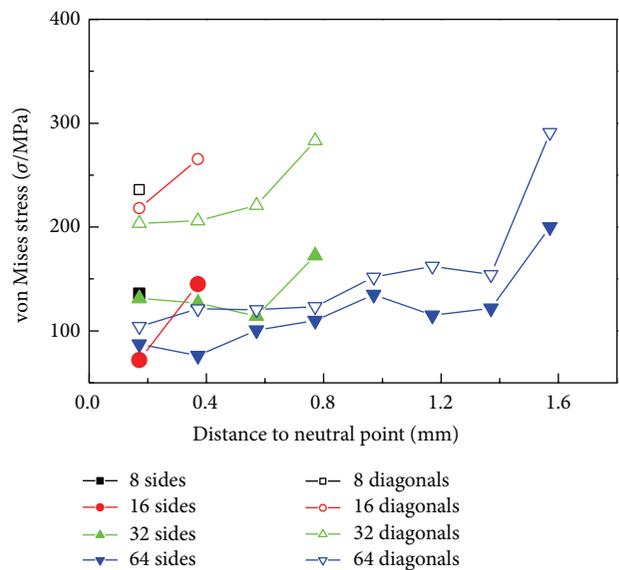


FIGURE 6: von Mises stress value of InSb chip versus distance to neutral point.

Figure 6. Apparently, the stress on diagonal is obviously larger than that situated on nondiagonal for all array scales. Besides, these sites on diagonal, their stress increase slowly with increasing distance to neutral point, but, for the sites with the largest distance to neutral point, where the stress values increase sharply. The stress values on nondiagonal almost have the similar shape; yet the values are smaller. It is noticed that stress values with the largest distance to neutral point for any scale detector arrays increase gradually with increased array scales, which means that, as the array scale is larger, the maximal von Mises stress value is also enlarged, and this phenomenon also agreed with that in Figure 5.

Figure 7(a) is von Mises stress distribution of InSb chip top surface with 64×64 arrays. Apparently, the maximal von Mises stress value 1420 MPa of InSb chip locates on the diagonal, which is far away from the neutral point.

The von Mises stress existing on those regions situated just over the contacting areas between InSb chip and indium bumps is smaller than the stress existing on its surrounding regions. This is contrary to InSb chip bottom surface stress distribution, which is also shown in Figure 7(b). Apparently, the stress existing on contact areas between InSb chip and indium bumps is concentrated and uniform; its stress value is about 475 MPa, larger than that of its surrounding areas. This phenomenon originates from the contacting areas which are glued together. This stress distribution of InSb chip for 64×64 arrays is distinctly different from the stress distribution in the structure without underfill, where the stress distribution of InSb chip is radiating, and the stress values decrease from inner to outer region [11].

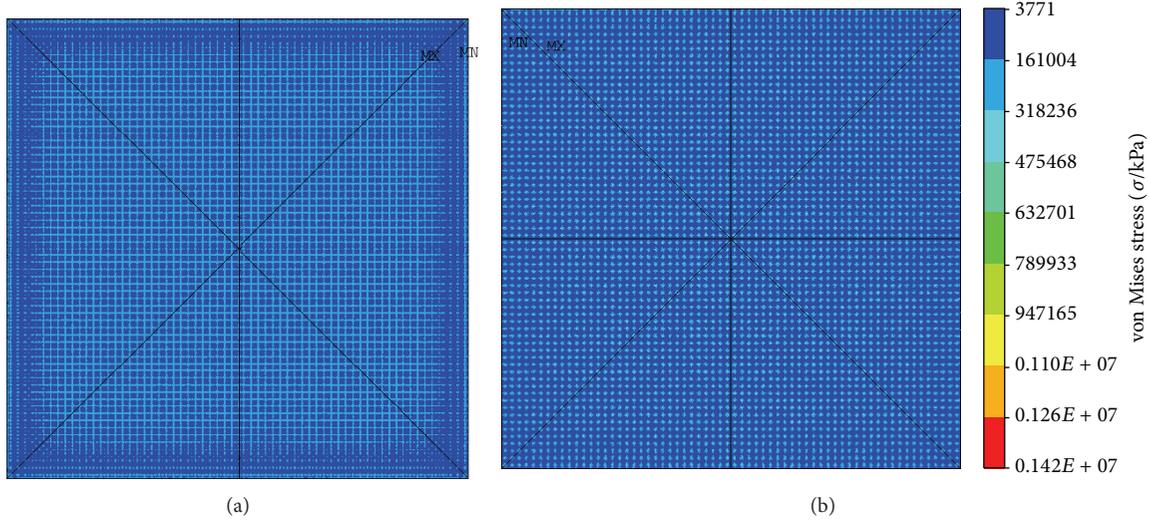


FIGURE 7: Mises stress distribution with 64×64 arrays for InSb chip: (a) top and (b) bottom surface.

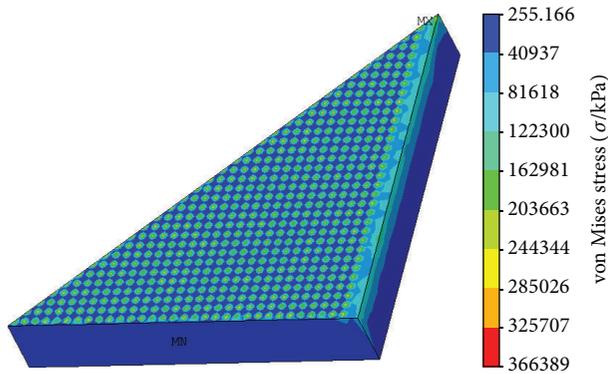


FIGURE 8: Mises stress distribution with 64×64 arrays for Si ROIC.

The von Mises stress distribution in Si ROIC is almost concentrated strongly on contacting areas between indium bumps and Si ROIC, and, around the contacting areas, the von Mises stress is so small that it is ignorable, just as shown in Figure 8. Besides, on the quadrilateral borders and sides of Si ROIC top surface, the von Mises stress is obviously larger than that on the noncontact areas. This phenomenon is distinctly different from the stress distribution of Si ROIC without underfill, where the stress on the quadrilateral borders and sides of Si ROIC top surface is ignorable [11].

5. Conclusions

Based on the temperature dependent elastic model of underfill and Anand's viscoplastic model of indium bumps, the thermal stress and its distribution in 64×64 InSb IRFPAs are systematically researched by employing finite element method. For 8×8 InSb IRFPAs, the thermal stress seems to have nothing to do with underfill height and is determined by indium bump diameters. Based on the above results, the stress in 64×64 InSb IRFPAs is obtained in a short time by

twice over the arrays format from 8×8 to 64×64 . Simulation results show that as the array scale is enlarged, the Von Mises stress value is also enlarged. The stress distribution for 64×64 arrays of InSb chip is uniform at contacting areas between InSb chip and indium bumps. These are favorable to reduce the crack happening in InSb chip and improve the final yield.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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