

## Research Article

# High Frequency InGaAs MOSFET with Nitride Sidewall Design for Low Power Application

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$\text{In}_x\text{Ga}_{1-x}\text{As}$  devices have been widely researched for low power high frequency applications due to the outstanding electron mobility and small bandgap of the materials. Regrown source/drain technology is highly appreciated in InGaAs MOSFET, since it is able to reduce the thermal budget induced by ion implantation, as well as reduce the source/drain resistance. However, regrown source/drain technology has problems such as high parasitic capacitance and high electric field at gate edge towards the drain side, which will lead to large drain leakage current and compromise the frequency performance. To alleviate the drain leakage current problem for low power applications and to improve the high frequency performance, a novel  $\text{Si}_3\text{N}_4$  sidewall structure was introduced to the InGaAs MOSFET. Device simulation was carried out with different newly proposed sidewall designs. The results showed that both the drain leakage current and the source/drain parasitic capacitance were reduced by applying  $\text{Si}_3\text{N}_4$  sidewall together with InP extended layer in InGaAs MOSFET. The simulation results also suggested that the newly created “recessed” sidewall was able to bring about the most frequency favorable characteristic with no current sacrifice.

## 1. Introduction

InGaAs MOSFET technology has been widely investigated for low power applications [1–7]. By using the regrown source/drain method, very low source/drain ohmic contact can be obtained [8–11] with highly doped material and reduced gate-source/gate-drain distance. However, high source/drain parasitic capacitance prohibits the InGaAs MOSFET from boosting the frequency performance due to the high- $k$  dielectric layer between the gate contact and the regrown source/drain contact. Besides, while high electron mobility is appreciated, III-V MOSFETs suffer from large drain leakage current when high electric field is applied [12–16]. To address these problems, a novel  $\text{Si}_3\text{N}_4$  sidewall was introduced between the gate contact and the regrown source/drain. It is able to reduce the parasitic capacitance and the drain leakage current under high electric field. Different  $\text{Si}_3\text{N}_4$  sidewall structures were proposed including one normal sidewall indicated as “spacer 1” and the other “recessed” sidewall together with InP extended layer, indicated as “spacer 2.” Device simulation was carried out using Atlas [17] to evaluate drain leakage current and frequency

performance. The “spacer 1” is able to effectively reduce the drain leakage current, while the “recessed spacer 2” can significantly decrease the parasitic capacitance without compromising the on-state performance.

## 2. Design Consideration and Motivation

In this paper, we proposed InGaAs MOSFET structures with  $\text{Si}_3\text{N}_4$  sidewall. Standard regrown source/drain MOSFETs only have one high- $k$  layer between the gate metal and the source/drain, which forms high parasitic capacitances  $C_{gs}$  and  $C_{gd}$  according to  $C = \epsilon_0\epsilon/t$ , prohibiting the device from attaining high frequency performance. To reduce the parasitic capacitance, we propose to insert a novel  $\text{Si}_3\text{N}_4$  sidewall layer between the gate metal and source/drain. The effective dielectric constant for the parasitic capacitance was therefore lowered and the dielectric thickness was increased, leading to smaller parasitic capacitance. Besides, InGaAs MOSFETs suffer from high drain leakage current [18–20], especially with the gate length scaling, due to the band-to-band tunneling effect caused by the high electric field at gate edge towards the drain side [21–23]. To deal with the

band-to-band tunneling problem, different solutions have been proposed, including adding larger bandgap material between the channel and regrown source/drain and lowering the doping level of the interfacial layer between the channel and the regrown source/drain. Here we propose a novel approach to solve the band-to-band tunneling problem by introducing a sidewall structure. With the insertion of the sidewall along the source/drain, the electric field would be modulated thus relieving the leakage problem. As a side effect, however, the insertion of the  $\text{Si}_3\text{N}_4$  would enlarge the gate-to-source and gate-to-drain distance and thus increase the source/drain access resistance. Another  $\text{Si}_3\text{N}_4$  sidewall structure “spacer 2” was then proposed to avoid the access resistance increase.

### 3. Simulation and Analysis

Device simulation without sidewall and with two different sidewalls was carried out using basic InGaAs MOSFET structure, and the three different structures were shown, respectively, in Figures 1(a), 1(b), and 1(c). The MOSFET structure consisted of a 10 nm  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  channel on top of a  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  buffer layer, grown on InP substrate. The regrown source/drain consisted of a thin InP layer and a 70 nm highly doped InGaAs layer. A 7 nm  $\text{HfO}_2$  layer was used as high- $k$  gate oxide as well as the insulating layer between the gate contact and the regrown source/drain contact. Two sidewall structures were studied: one is a normal sidewall along the InP/InGaAs side, which is indicated as “spacer 1” and shown in Figure 1(b), and the other is a novel “recessed” sidewall along the InGaAs side only, aligned to the extended InP head, which is indicated as “spacer 2” and shown in Figure 1(c). Basic simulation models such as “BGN” (Bandgap Narrowing model), “CVT” (Lombardi model including  $N$ ,  $T$ , and  $E$  effects), and “SRH” (Shockley-Read-Hall model) were used, and the sidewall processing damage was not considered during the simulation.

Electric field simulation results for devices without sidewall and with  $\text{Si}_3\text{N}_4$  sidewall were shown in Figures 2(a) and 2(b), respectively. The highest electric field was found at the gate edge towards the drain side. Comparing the two structures, the device with sidewall had a smaller electric field ( $4.4 \times 10^7$  V/cm) than the device without sidewall ( $4.8 \times 10^7$  V/cm), which is favorable for reducing drain leakage current. From the transfer characteristics shown in Figure 3, where the black curve represents the device without spacer, the blue curve represents the device with “spacer 1,” and the pink curve represents the device with “spacer 2”; the device with sidewall “spacer 1” reduced the drain leakage current by more than 2 orders than the one without sidewall from  $10^{-8}$  A to  $10^{-10}$  A, although the drain saturation current was compromised due to the increased access resistance  $R_{ac}$  induced by the sidewall, as indicated in the inserted illustration in Figure 1(a). Sidewall “spacer 2” showed almost the same transfer characteristic as that without sidewall, since  $\text{Si}_3\text{N}_4$  was on top of the extended InP drain layer, and its electric field modulation capability was screened by the InP layer. The parasitic capacitance simulation results were shown in Figure 4(b), where the set of solid curves represent the

$C_{gs}$  values and the set of open curves represent the  $C_{ds}$  values, showing that  $C_{gs}$  and  $C_{ds}$  were significantly reduced from  $3 \times 10^{-15}$  F/ $\mu\text{m}$  to  $1 \times 10^{-15}$  F/ $\mu\text{m}$  by the  $\text{Si}_3\text{N}_4$  sidewall according to  $C = \epsilon_0 \epsilon / t$ , where  $\epsilon$  is the dielectric constant of the sidewall, and  $t$  is the dielectric thickness. The dielectric constant of  $\text{Si}_3\text{N}_4$  is much smaller ( $k = 4-7$ ) than that of  $\text{HfO}_2$  ( $k = 16-22$ ), which increased the effective dielectric constant for parasitic capacitance. Besides, the insertion of 10 nm  $\text{Si}_3\text{N}_4$  added up to the total dielectric thickness and thus further reduced the parasitic capacitance. The sidewall “spacer 2” showed slightly higher parasitic capacitance than sidewall “spacer 1” since only the recessed part along the InGaAs source/drain side has sidewall, and there existed only high- $k$   $\text{HfO}_2$  between gate electrode and InP source/drain. Figure 4(a) showed the gain simulation results, where the set of solid curves represent the current gain  $H_{21}$  values and the set of open curves represent the unilateral power gain  $U$  values, from which the cut-off frequency  $f_t$  and the maximum oscillation frequency  $f_{max}$  can be extracted. While the current gain was smaller for device with sidewall “spacer 1” due to its higher access resistance and smaller transconductance ( $f_t = g_m / 2\pi(C_{gs} + C_{gd})$ ), the unilateral power gain for the device with sidewall “spacer 1” caught up with the one without sidewall due to reduced  $g_m$  and increased capacitance influence ( $f_{max} \approx (f_t / 8\pi R_g C_{gd})^{1/2}$ ). The device with sidewall “spacer 2” showed the highest current gain and unilateral power gain among the three structures since the recessed sidewall helped to decrease the parasitic capacitance effectively while it barely added up to the access resistance.

The influence of the thickness of both “spacer 1” and “spacer 2” sidewalls was studied, verified from 2 nm to 10 nm. The  $\log I_d - V_g$  characteristics for “spacer 1” were shown in Figure 5 for different  $\text{Si}_3\text{N}_4$  sidewall thickness, where the black curve represents the device with spacer 1 of 2 nm, the red curve represents the device with spacer 1 of 4 nm, the green curve represents the device with spacer 1 of 6 nm, the blue curve represents the device with spacer 1 of 8 nm, and the pink curve represents the device with spacer 1 of 10 nm. It is observed that the drain leakage current was improved from  $10^{-8}$  A,  $3 \times 10^{-10}$  A,  $1 \times 10^{-10}$  A, and  $7 \times 10^{-11}$  A to  $4 \times 10^{-11}$  A with increasing  $\text{Si}_3\text{N}_4$  thickness. This could be due to the effective electric field modulation at gate edge towards the drain side by the use of  $\text{Si}_3\text{N}_4$  sidewall. The current gain and unilateral power gain were shown in Figure 6(a). Both the current gain and the unilateral power gain decreased slightly with the increasing thickness of  $\text{Si}_3\text{N}_4$  sidewall. It can be explained that at increasing sidewall thickness from 2 nm to 10 nm, sidewall induced access resistance led to increased transconductance degradation, which overran the parasitic capacitance reduction from 2.2 fF/ $\mu\text{m}$ , 1.8 fF/ $\mu\text{m}$ , 1.6 fF/ $\mu\text{m}$ , and 1.4 fF/ $\mu\text{m}$  to 1.3 fF/ $\mu\text{m}$ , as shown in Figure 6(b).

The same thickness variation study was carried out on sidewall “spacer 2,” as shown in Figure 7, where the black curve represents the device with spacer 2 of 2 nm, the red curve represents the device with spacer 2 of 4 nm, the green curve represents the device with spacer 2 of 6 nm, the blue curve represents the device with spacer 2 of 8 nm,

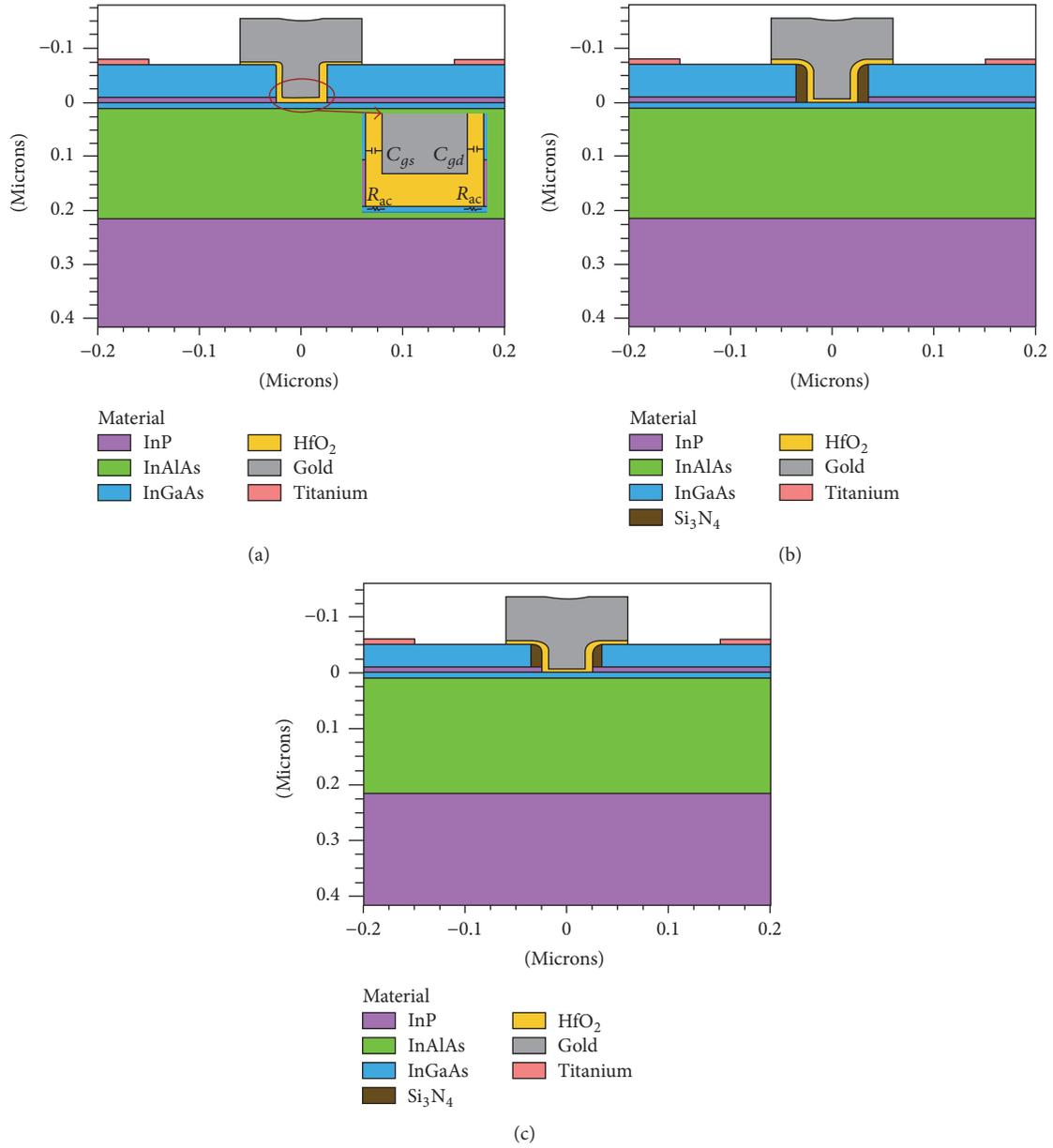


FIGURE 1: InGaAs MOSFET structures (a) without sidewall, (b) with sidewall “spacer 1,” and (c) with sidewall “spacer 2” for Atlas simulation.

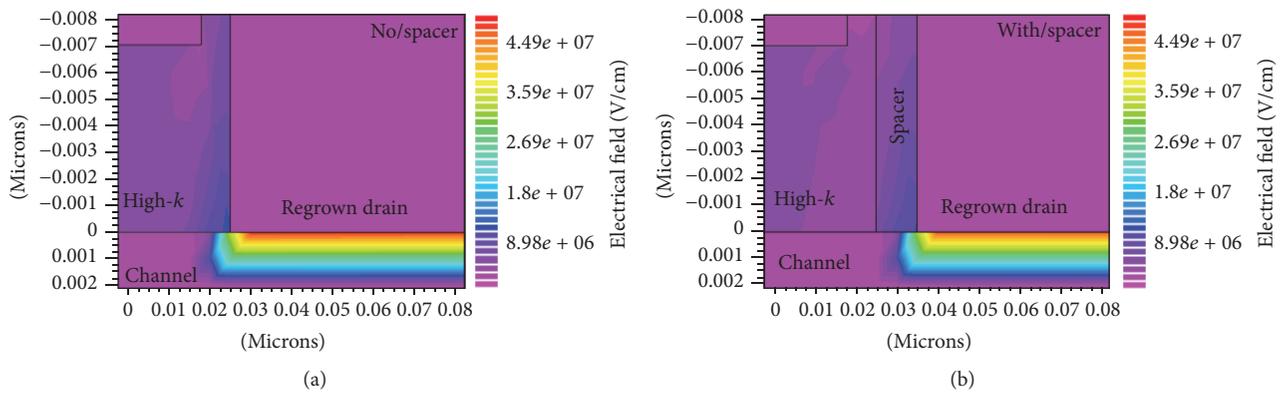


FIGURE 2: Electric field simulation of InGaAs MOSFET (a) without sidewall and (b) with sidewall “spacer 1.”

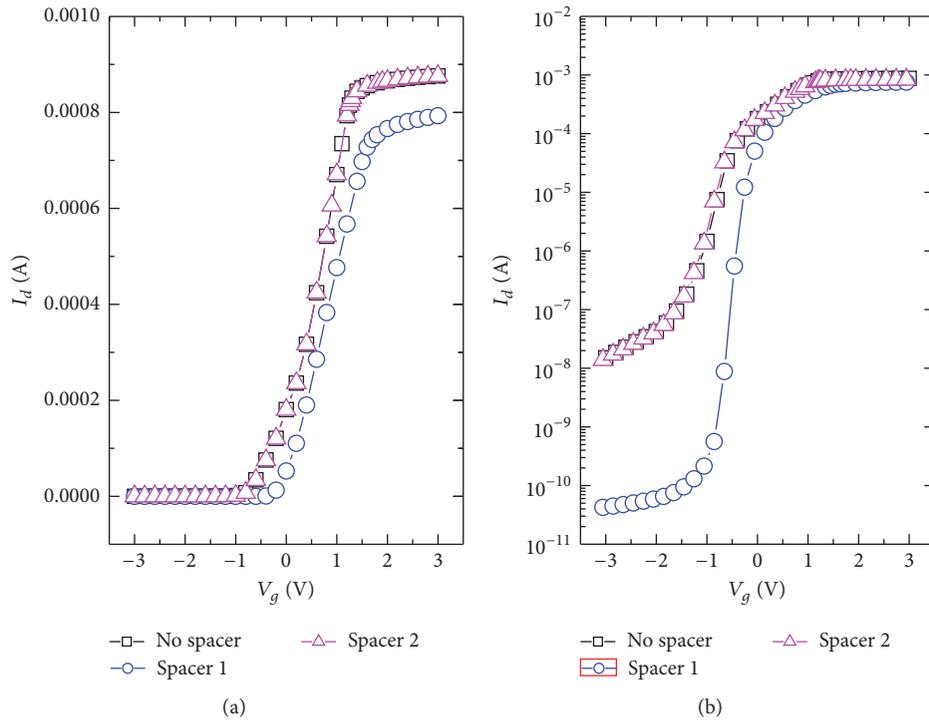


FIGURE 3: (a)  $I_d$ - $V_g$  and (b)  $\log I_d$ - $V_g$  characteristics of InGaAs MOSFET with sidewall "spacer 1," "spacer 2," and without sidewall.

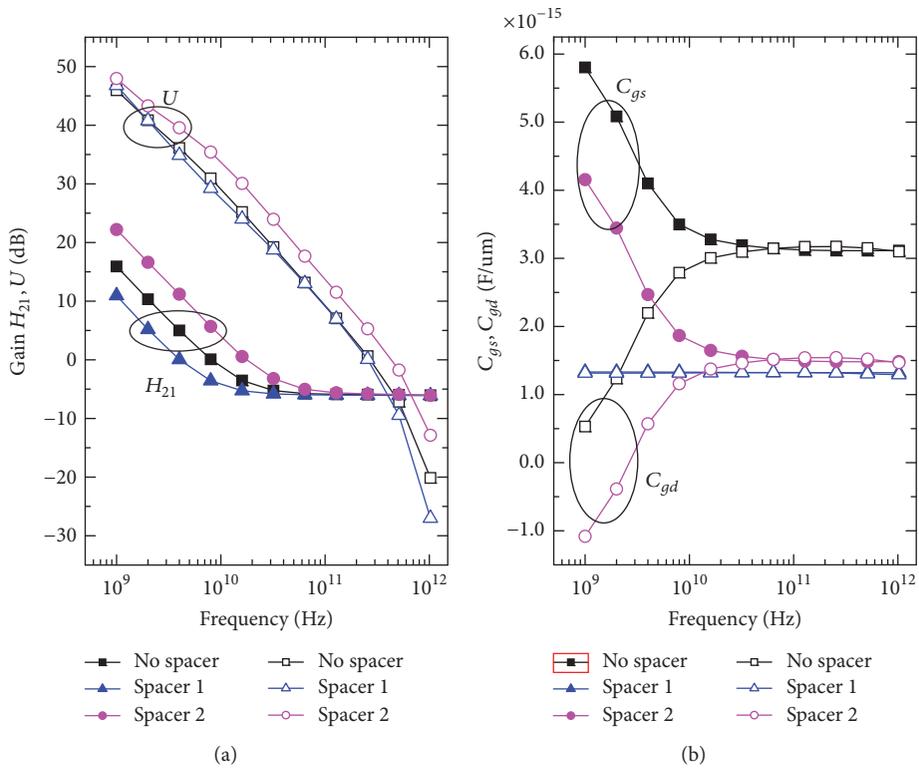


FIGURE 4: (a) Current gain, unilateral power gain versus frequency (solid: current gain  $H_{21}$ ; open: unilateral power gain  $U$ ), and (b) parasitic capacitances  $C_{gs}$  and  $C_{gd}$  versus frequency (solid:  $C_{gs}$ ; open:  $C_{gd}$ ) of InGaAs MOSFET with sidewall "spacer 1," "spacer 2," and without sidewall.

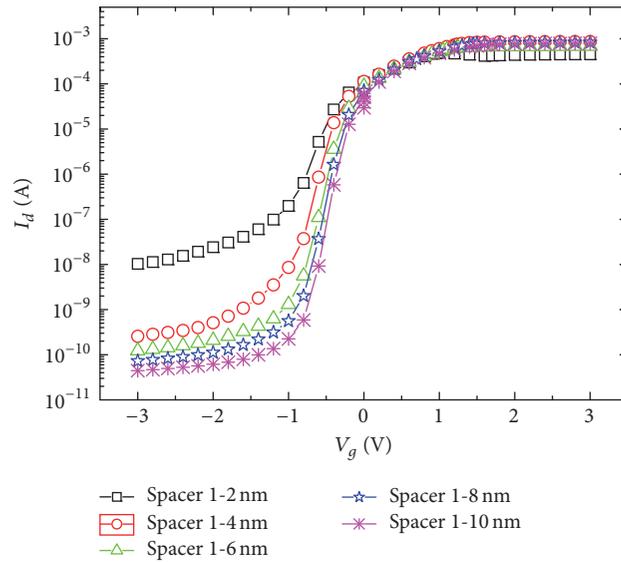


FIGURE 5:  $\log I_d$ - $V_g$  characteristics of InGaAs MOSFET with sidewall “spacer 1” thickness variation from 2 nm to 10 nm.

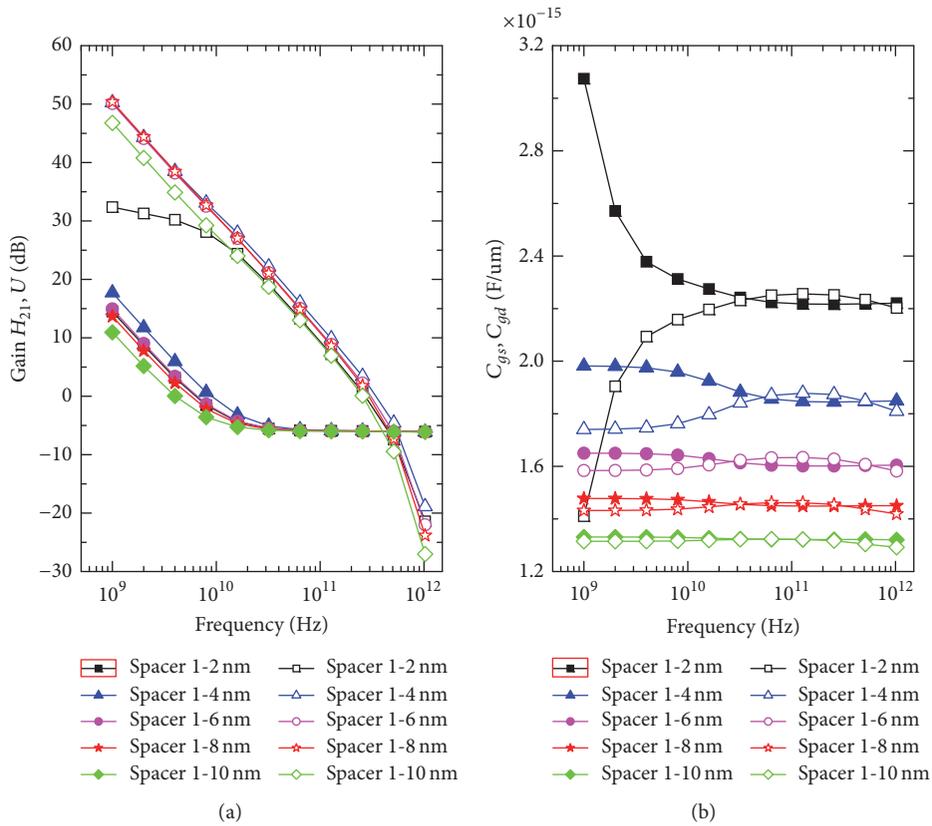


FIGURE 6: (a) Current gain, unilateral power gain versus frequency (solid: current gain  $H_{21}$ ; open: unilateral power gain  $U$ ), and (b) parasitic capacitances  $C_{gs}$  and  $C_{gd}$  versus frequency (solid:  $C_{gs}$ ; open:  $C_{gd}$ ) of InGaAs MOSFET with sidewall “spacer 1” thickness variation from 2 nm to 10 nm.

and the pink curve represents the device with spacer 2 of 10 nm. It is observed that, for “spacer 2,” the  $\text{Si}_3\text{N}_4$  sidewall thickness barely affected the drain leakage current, since the extended InP layer prevented the sidewall induced access resistances from increasing. As shown in shown in

Figure 8(a), the current gain and the unilateral power gain increased with the recessed sidewall thickness, which was mainly due to the parasitic capacitance reduction from  $2 \text{ fF}/\mu\text{m}$  to  $1.5 \text{ fF}/\mu\text{m}$  with constant transfer characteristics, shown in Figure 8(b).

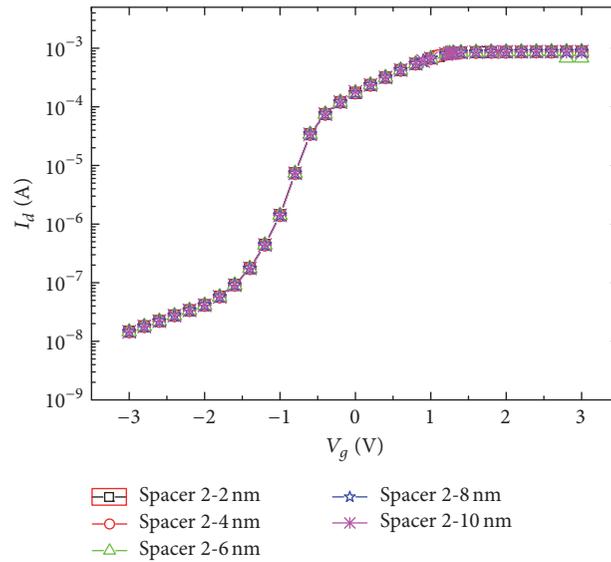


FIGURE 7:  $\log I_d$ - $V_g$  characteristics of InGaAs MOSFET with sidewall “spacer 2” thickness variation from 2 nm to 10 nm design.

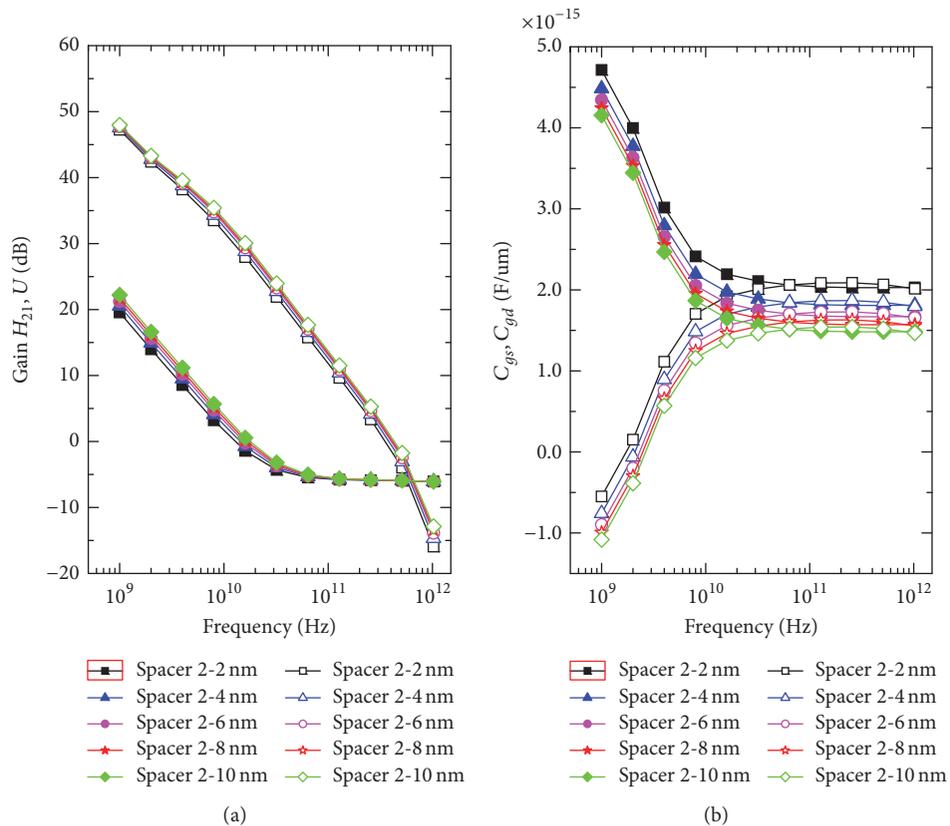


FIGURE 8: (a) Current gain, unilateral power gain versus frequency (solid: current gain  $H_{21}$ ; open: unilateral power gain  $U$ ), and (b) parasitic capacitances  $C_{gs}$  and  $C_{gd}$  versus frequency (solid:  $C_{gs}$ ; open:  $C_{gd}$ ) of InGaAs MOSFET with sidewall “spacer 2” thickness variation from 2 nm to 10 nm design.

#### 4. Proposed Device Processing

The proposed sidewall structures show promising electric characteristics according to the device simulation. The InGaAs MOSFET structures without  $\text{Si}_3\text{N}_4$  sidewall, with

$\text{Si}_3\text{N}_4$  sidewall “spacer 1,” and with  $\text{Si}_3\text{N}_4$  sidewall “spacer 2” can be fabricated using the main processing steps shown in Figure 9, which is compatible with normal device fabrication. The epitaxial layers were prepared by Molecular Beam Epitaxy (MBE) that consists of InP substrate, InAlAs

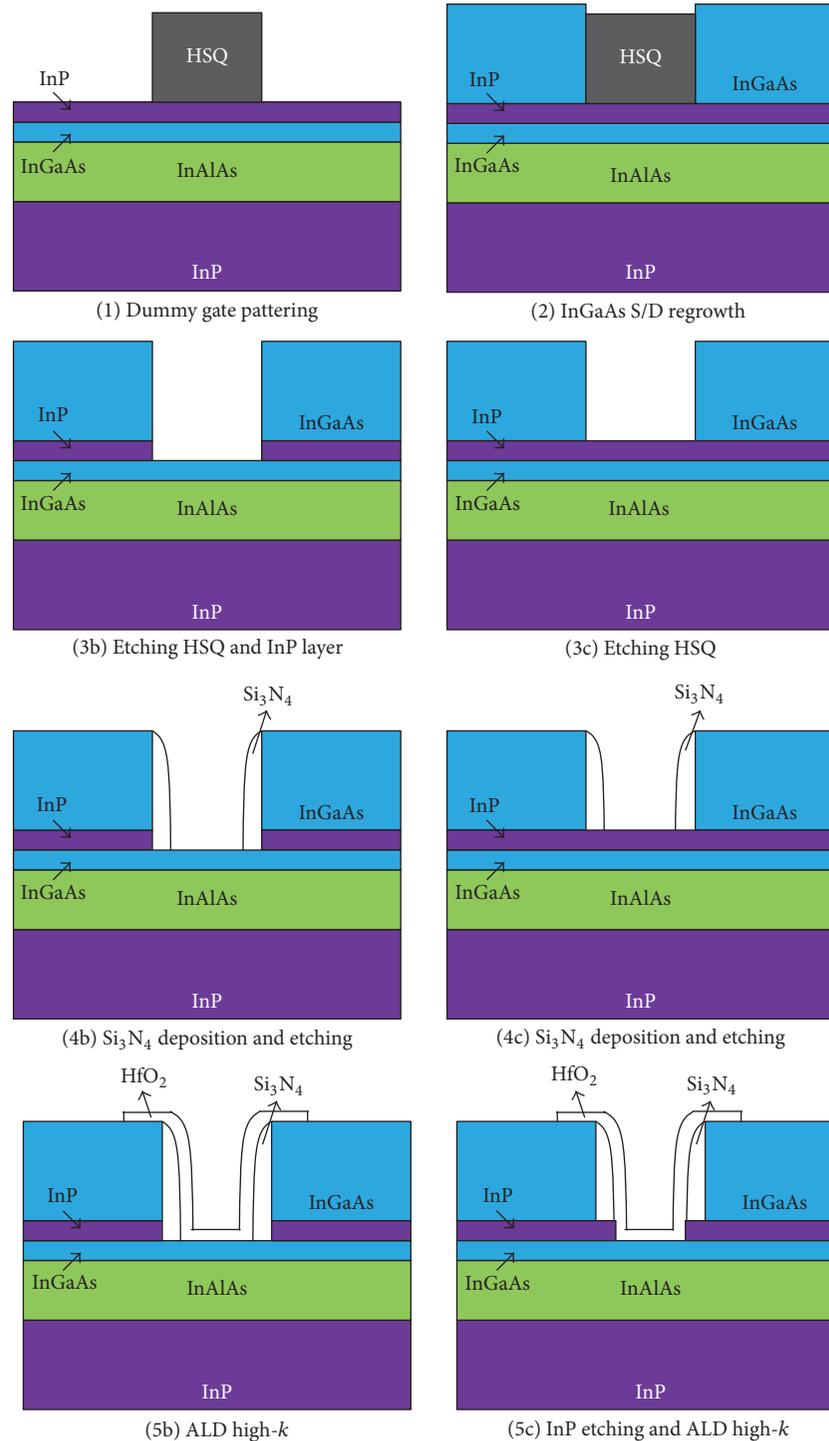


FIGURE 9: Proposed device fabrication steps for “spacer 1” and “spacer 2” structures (steps (1) and (2) are the common processing steps, steps (3b), (4b), and (5b) are the “spacer 1” processing steps, and steps (3c), (4c), and (5c) are the “spacer 2” processing steps).

buffer layer, InGaAs channel, and InP cap layer from the bottom to the top. Dummy gate using negative resist HSQ was patterned at first to define the gate length (step (1)); then, highly  $n^+$  doped InGaAs source/drain regrowth was carried out using Metal Organic Chemical Vapor Deposition (MOCVD) (step (2)). After that, HSQ was removed. For “spacer 1” structure, InP cap layer was etched right after

HSQ (step (3b)), while InP cap layer was kept for “spacer 2” structure (step (3c)). The etching selectivity between InP and InGaAs can be well controlled by using HCl based chemical solution, as shown in Figure 10, where an illustrative InP pattern was fabricated on the InGaAs surface by perfect wet etching.  $\text{Si}_3\text{N}_4$  was then deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) and etched using

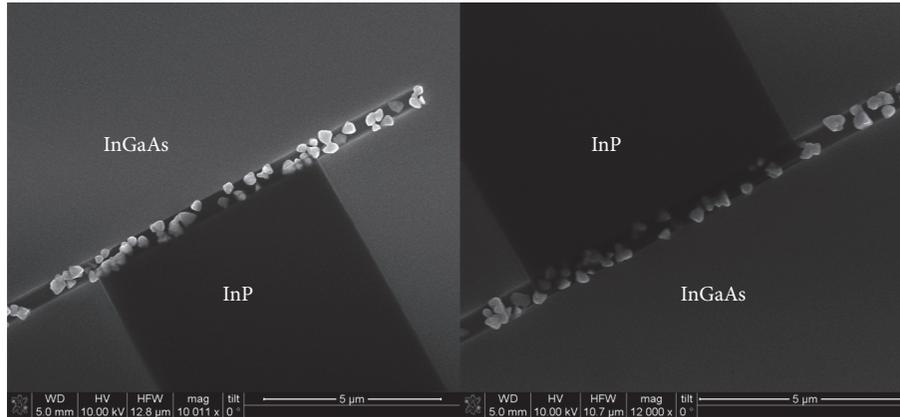


FIGURE 10: SEM image of selective InP etching on InGaAs surface.

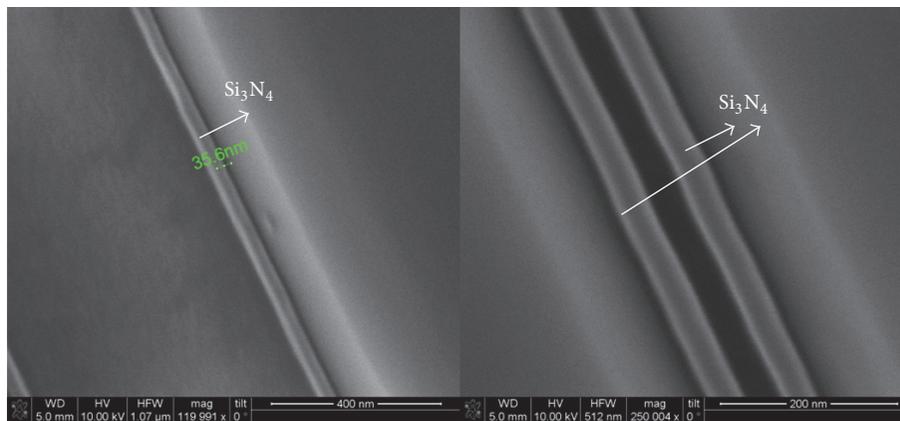


FIGURE 11: SEM image of  $\text{Si}_3\text{N}_4$  sidewall realized along the InGaAs side.

Reactive Ion Etching (RIE) to form the sidewall along the S/D for both structures (steps (4b) and (4c)). An experimental  $\text{Si}_3\text{N}_4$  sidewall is obtained using this technique, as shown in Figure 11, where a vertical  $\text{Si}_3\text{N}_4$  can be observed along the InGaAs side. After that, high- $k$  gate oxide was realized using Atomic Layer Deposition (ALD) after  $(\text{NH}_4)_2\text{S}$  surface treatment for “spacer 1” structure (step (5b)), while high- $k$  was deposited after InP cap etching for “spacer 2” structure (step (5c)). Gate metal was then carried out followed by source/drain metal patterning. Similar device processing can be found in papers [24, 25].

## 5. Conclusion

In this paper, a novel  $\text{Si}_3\text{N}_4$  sidewall structure was introduced to the regrown source/drain based InGaAs MOSFET technology. By relieving the electric field at gate edge towards the drain side, the new sidewall structures can reduce the drain leakage current to achieve low standby power consumption. It is also able to improve the potential frequency performance by reducing the parasitic source/drain capacitance. Different  $\text{Si}_3\text{N}_4$  sidewall structures including a normal sidewall and a “recessed” sidewall with extended InP layer were studied with varied  $\text{Si}_3\text{N}_4$  sidewall thickness. The normal sidewall

structure can effectively reduce the drain leakage current but may incur increased access resistance, compromising the frequency performance. As a compensation for this side effect, the novel “recessed” sidewall structure with extended InP layer plays a role in reducing the parasitic capacitance without sacrificing the on-state performance, which can further boost the frequency performance with the  $\text{Si}_3\text{N}_4$  thickness increase.

## Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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