

Research Article

Fabrication of a Piezoresistive Barometric Pressure Sensor by a Silicon-on-Nothing Technology

Jiale Su^{1,2}, Xinwei Zhang², Guoping Zhou², Jianjian Gu², Changfeng Xia², Zai-Fa Zhou¹, and Qing-An Huang¹ 

¹Key Laboratory of MEMS of the Ministry of Education, Southeast University, Nanjing 210096, China

²CSMC Semiconductor Co., Ltd., Wuxi 214061, China

Correspondence should be addressed to Qing-An Huang; hqa@seu.edu.cn

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This paper presents a piezoresistive barometric pressure sensor fabricated by using a Silicon-on-Nothing (SON) technology. Array of silicon trenches were annealed in hydrogen environment to form continuing crystalline silicon membrane over a vacuum cavity. Epitaxial growth on the silicon membrane is then completed for the desired thickness. All processes are CMOS compatible and performed on the front side of the silicon wafer. The piezoresistive barometric pressure sensor has been demonstrated with pressure hysteresis as low as 0.007%.

1. Introduction

MEMS pressure sensors find applications such as indoor and outdoor navigation, altimeter, and barometer. Recently, the shipping in the field of consumer electronics has rapidly increased. The consumer applications demand high-performance, low cost, and small size. A piezoresistive pressure sensor is a good candidate. The piezoresistive pressure sensors were first demonstrated by Tufte et al. in the 1960s [1] by using KOH etching. They may be made by bulk micromachining [2, 3] or surface micromachining [4, 5]. Also, wide-band gap semiconductors based piezoresistive pressure sensors have been proposed for hostile environments [6, 7]. However, double-side processing from bulk micromachining is not CMOS process friendly [2, 3]. For example, double-side alignment has the low photography accuracy and low throughput, and KOH etching has low efficiency and accuracy, resulting in high costs and high risk of batch process failure. Robert Bosch reported Advanced Porous Silicon Membrane (APSM) process for pressure sensors fabrication [8, 9]. However, such commercial piezoresistive pressure sensor through the APSM process demand dedicated tools to fabricate porous silicon which is not available in most of IC foundry. The Empty-Space-in-Silicon (ESS) process, a new

SON technology, was developed in 2000 [10, 11]. Array of silicon trenches were annealed in hydrogen environment to form continuing crystalline silicon membrane over a vacuum cavity. It has been used for capacitive pressure sensors [12] and other sensors [13]. This paper presents a process for a piezoresistive barometric pressure sensor by using the Silicon-on-Nothing (SON) technology.

2. SON Technology

The Empty-Space-in-Silicon (ESS) process includes the trench etching and annealing [10, 11]. In the first step, regular arrays of trenches are etched in (100) silicon wafers by reactive ion etching. The dimensions of the trenches depend on the annealing temperature and time. In the second step, the wafers are annealed in hydrogen environment. A heat treatment induces silicon to minimize the surface energy, leading silicon migration to widening of the void at the base and shrinking of the opening at the top.

The surface migration of silicon is governed by [10]

$$\mathbf{v} = -\frac{D}{kT}\nabla\mu \quad (1)$$

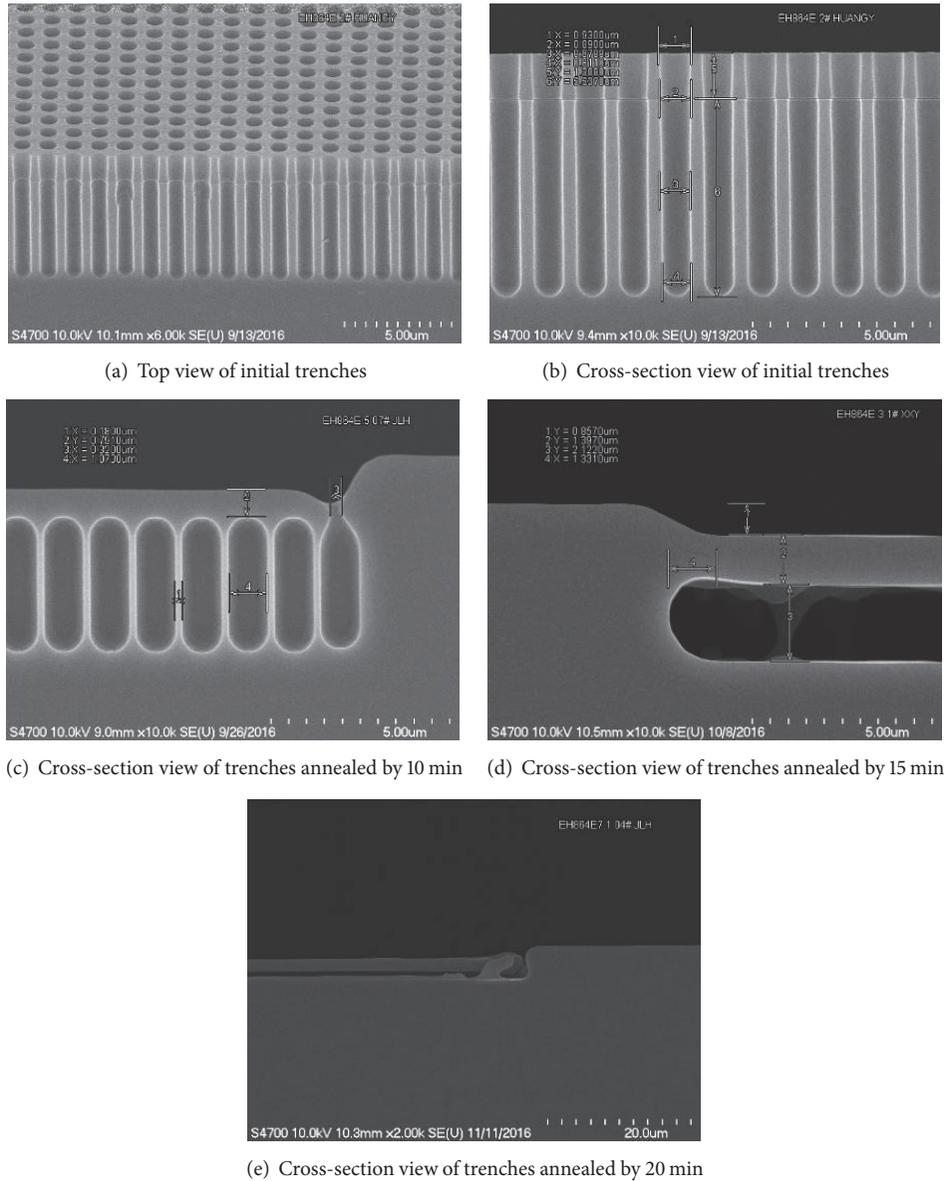


FIGURE 1: The SON process. (a) Top view of initial trenches, (b) cross-section view of initial trenches, (c) cross-section view after 10 min annealing, (d) cross-section view after 15 min annealing, and (e) cross-section view after 20 min annealing.

where v is the drift velocity of surface silicon atoms, D is the surface diffusion coefficient, k is the Boltzmann constant, and T is the process temperature. The chemical potential $\mu = K\gamma\Omega$, where K is the local mean curvature, γ is surface tension, and Ω is the molecular volume. The relationship between the processing temperature and silicon diffusion coefficient was described [10]. The diffusion coefficient at 1200°C is fourfold that at 1100°C . Thus, the annealing temperature and time, which will be optimized for ESS formation, depend on the size of the initial trenches. In our experiments, the trench with a diameter of $0.8\mu\text{m}$ was etched in (100) silicon wafers by reactive ion etching (RIE). As showed in Figure 1, the sizes of the trench on the top, middle, and bottom are $0.89\mu\text{m}$, $0.87\mu\text{m}$, and $0.81\mu\text{m}$, respectively. The

trenches can be transformed to ESS by the annealing at 1100°C for 10 min. Figures 1(b)–1(d) show the SEM cross-section pictures for our experiments at different annealing time.

When annealing for 10 min, as shown in Figure 1(c), the trenches were not completely merged as a whole. Thus, annealing for 10 min was not long enough to produce the membrane. When the annealing time was increased to 15 min, the desired cavity, as shown in Figure 1(d), was formed. However, when the annealing time was further increased to 20 min, the membrane was formed but cracked on the joint between the membrane and substrate. As a result, the formation process of the silicon membrane over a vacuum cavity depends on the annealing conditions. Usually, the trench diameter was controlled in the range of $0.5\text{--}1.2\mu\text{m}$.

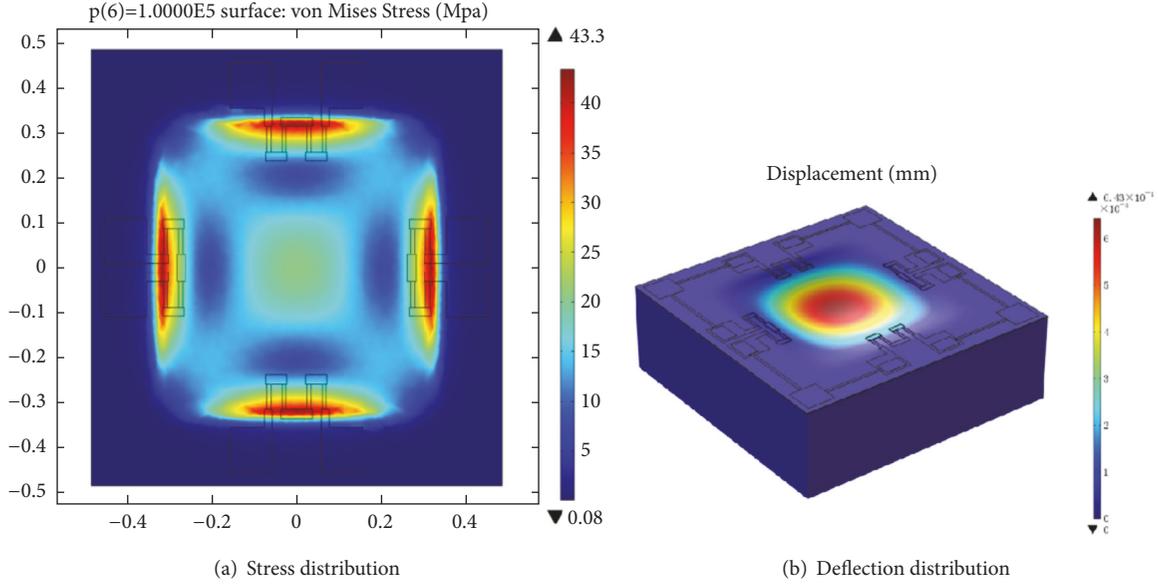


FIGURE 2: The simulation results of the stress and deflection of the diaphragm under 100 kPa.

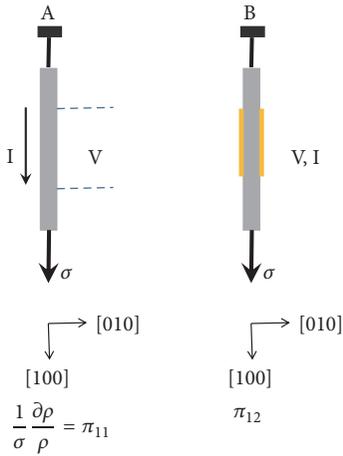


FIGURE 3: Definitions of longitudinal and transverse piezoresistive coefficients.

The spacing between the trenches was $0.5\text{-}1\mu\text{m}$, and the aspect ratio of the trench was defined in the range from 3 to 9.5.

3. Design and Fabrication

A piezoresistive pressure sensor was designed to measure 100 kPa absolute pressure. When the pressure was applied on the diaphragm, the strain (ϵ) or stress (σ) would bend the piezoresistors. Such a strain/stress can be measured by monitoring the resistance change of the sensor.

The resistivity (ρ) variation due to stress was written as [14]

$$\frac{\Delta\rho_\omega}{\rho} = \sum_{\lambda=1}^6 \pi_{\omega\lambda}\sigma_\lambda \quad (2)$$

where $\pi_{\omega\lambda}$ is the piezoresistive coefficients and σ_λ is the stress, in different orientations (λ), respectively.

According to Hooke's Law, it yields

$$\sigma = \epsilon E \quad (3)$$

where E is Young's Modulus.

3.1. Deflection Simulation. Figure 2 gives the simulation results of the stress and deflection of the diaphragm under 100 kPa. The diaphragm size is $600\mu\text{m} \times 600\mu\text{m}$ and its thickness is $13\mu\text{m}$. The maximum deflection in the center reaches $0.64\mu\text{m}$ and the stress concentrations occur in a $10\mu\text{m}$ wide rectangular area from the edge of diaphragm.

3.2. Piezoresistors. Single crystal silicon piezoresistive coefficients are showed below [3],

$$\pi = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & & & \\ \pi_{12} & \pi_{11} & \pi_{12} & & & \\ \pi_{12} & \pi_{12} & \pi_{11} & & & \\ & & & \pi_{44} & & \\ & & & & \pi_{44} & \\ & & & & & \pi_{44} \end{bmatrix} \quad (4)$$

where piezoresistive coefficients π are defined as in Figure 3 and Table 1.

When the direction of stress is the same as that of current, the corresponding longitudinal piezoresistive coefficient is π_{11} , and the resistor is along with $[100]$ direction. When the direction of stress is perpendicular to the current, the transverse piezoresistive coefficient is π_{12} .

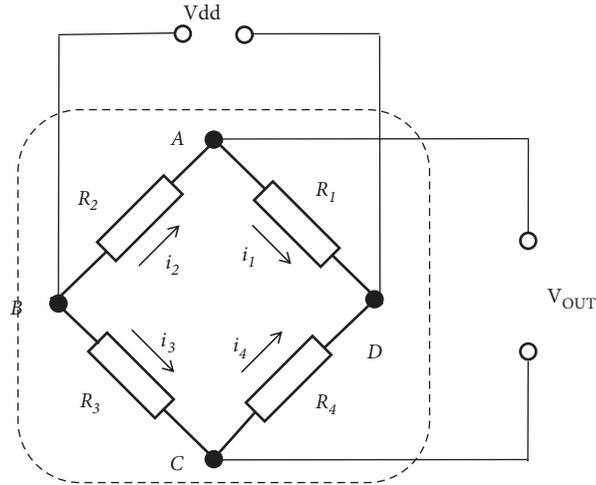


FIGURE 4: A circuit schematic of a Wheatstone bridge.

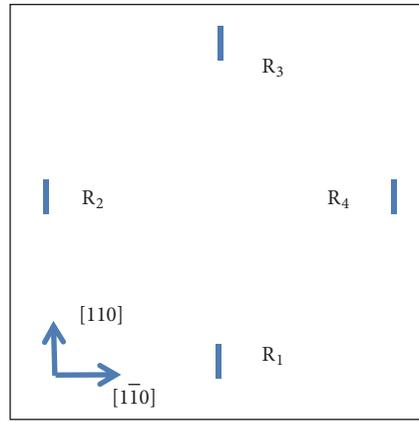


FIGURE 5: The schematic layout of piezoresistors.

3.3. Wheatstone Bridge. A Wheatstone bridge is widely used in the design of piezoresistive pressure sensors, as shown in Figure 4. V_{dd} stands for applied voltage across the node BD and V_{out} is the output voltage measured across the node AC. When pressure is applied, the resistances of R_1 and R_3 vary due to the longitudinal piezoresistive effect, while the resistances of R_2 and R_4 change due to transverse piezoresistive effect.

$$V_{out} = \left(\frac{R_1}{R_1 + R_2} - \frac{R_3}{R_3 + R_4} \right) V_{dd}. \quad (5)$$

A particular design, the full-bridge with four identical piezoresistors, that is, $R_1 = R_2 = R_3 = R_4 = R$, yields

$$\Delta V_{out} = \frac{\Delta R_1 - \Delta R_2 + \Delta R_3 - \Delta R_4}{4R} V_{dd}. \quad (6)$$

All piezoresistors are fabricated on N-type $\langle 100 \rangle$ silicon wafer and aligned with $[110]$ direction because of a large piezoresistive coefficient.

According to the simulation in Figure 2, the four piezoresistors were aligned in the middle of the edge of diaphragm,

showed in Figure 5. The cross-section and overview of the devices are shown in Figure 6. Four piezoresistors were implanted and connected via aluminum as a Wheatstone bridge. P^+ stands for a boron heavily doped region, P^- stands for a boron lightly doped region, and TEOS is abbreviated by Tetraethyl Orthosilicate. ANSYS was used here to simulate stress distribution and deflection so that the size of the membrane over the cavity can be optimized.

Moreover, piezoresistors were related to temperature variation; the piezoresistance factor $P(N, T)$ for p-Si was a function of doping concentration and temperature [3]. As shown in Figure 7, the temperature coefficient of resistance (TCR) was around 2200 ppm/ $^{\circ}\text{C}$.

With the TCR values illustrated in Figure 7, Figure 8 shows the calculated bridge voltage output as a function of pressure at different temperatures, 0°C , 40°C , and 80°C .

3.4. Fabrication. The fabrication process of a piezoresistive barometric pressure sensor was shown in Figure 9. In the first step (a), a regular array of $0.8\mu\text{m}$ trenches were etched in N-type $\langle 100 \rangle$ silicon wafer with $1\sim 10\Omega\text{cm}$ by deep reactive

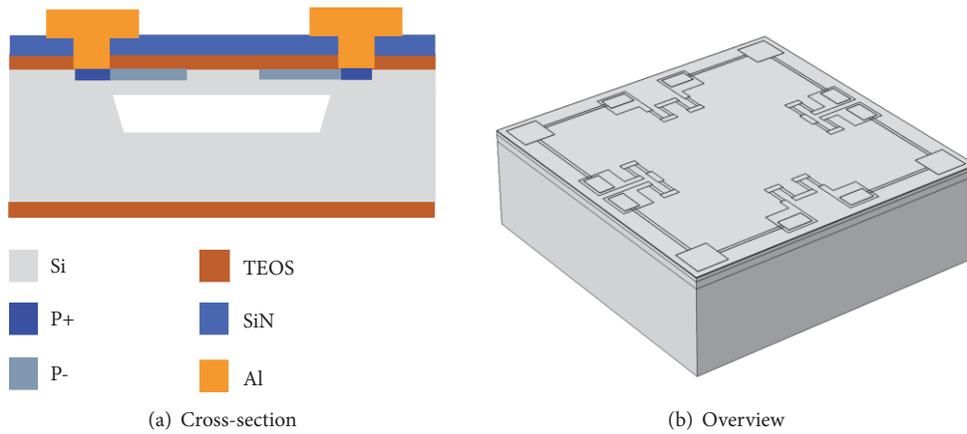


FIGURE 6: Schematic diagram of a piezoresistive pressure sensor.

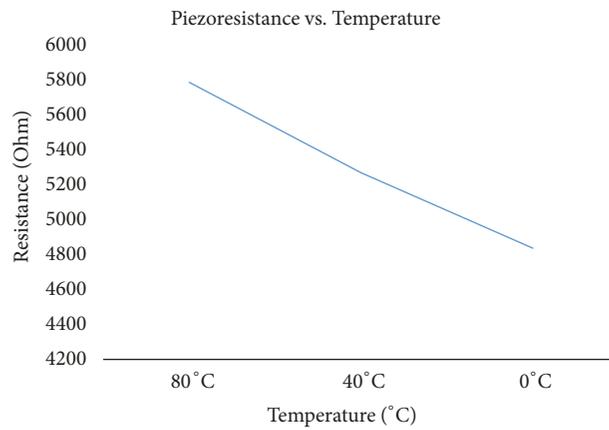


FIGURE 7: Piezoresistance versus temperature.

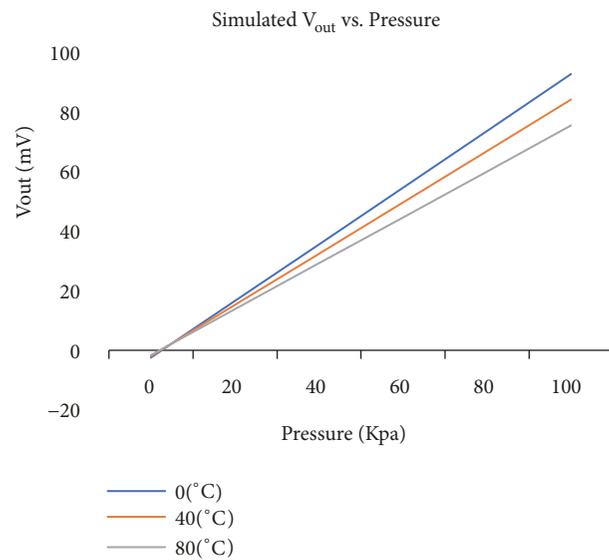


FIGURE 8: Simulated voltage output versus pressure.

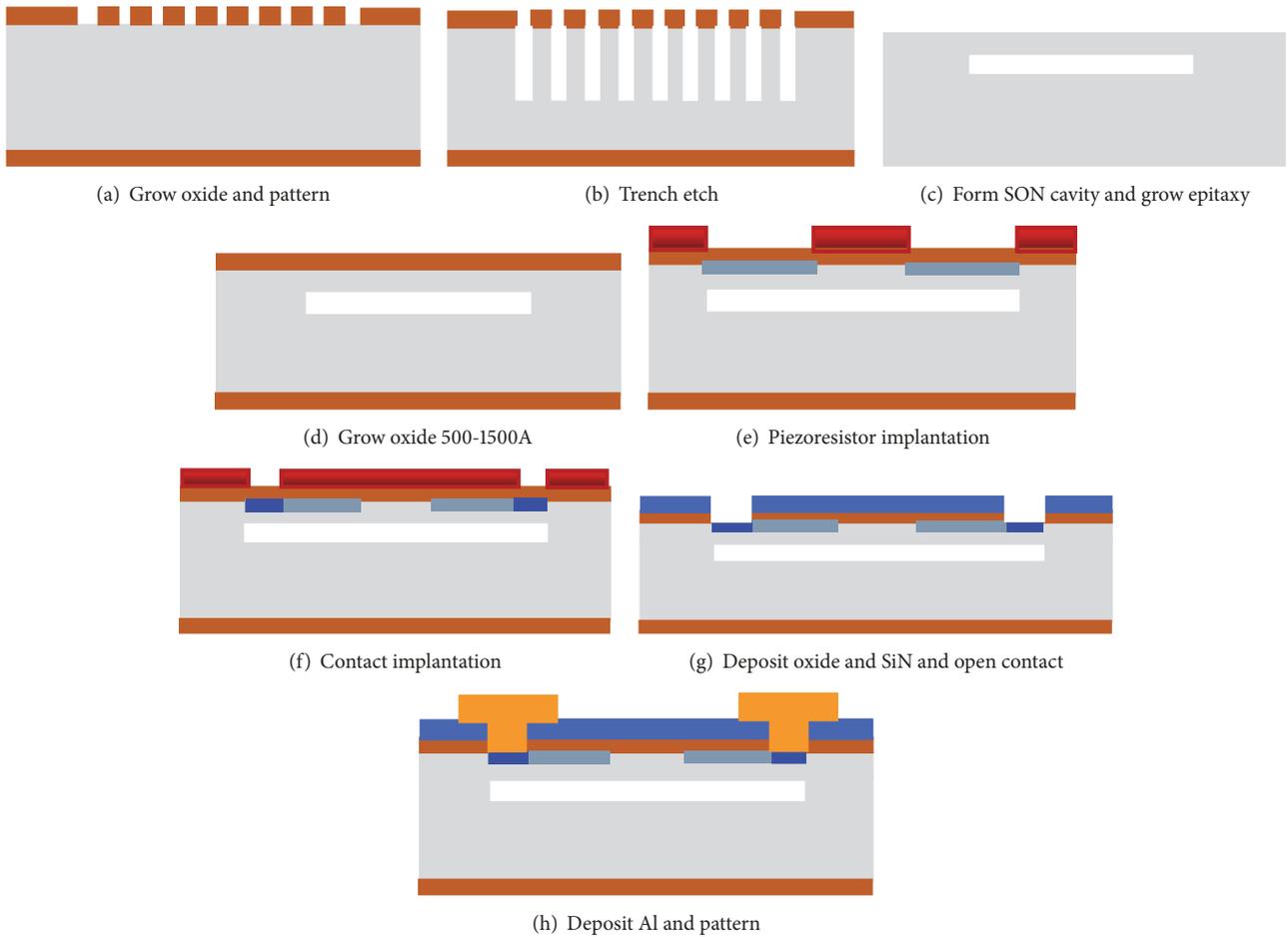


FIGURE 9: Fabrication process of a piezoresistive barometric pressure sensor.

TABLE 1: Longitudinal and transverse piezoresistive coefficients in different directions [3].

| Direction of Stress | Direction of Current | Type | Piezoresistive Coefficient |
|-----------------------|-----------------------------------|--------------|---|
| $\langle 100 \rangle$ | $\langle 100 \rangle$ | Longitudinal | π_{11} |
| $\langle 100 \rangle$ | $\langle 010 \rangle$ | Transverse | π_{12} |
| $\langle 110 \rangle$ | $\langle 110 \rangle$ | Longitudinal | $\frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44})$ |
| $\langle 110 \rangle$ | $\langle \bar{1}\bar{1}0 \rangle$ | Transverse | $\frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44})$ |
| $\langle 111 \rangle$ | $\langle 111 \rangle$ | Longitudinal | $\frac{1}{2}(\pi_{11} + 2\pi_{12} + 2\pi_{44})$ |

ion etching. In the second step (b), the wafers were annealed in hydrogen environment at 1100°C for 15 min. Then, 12 μm epitaxial growth of the silicon membranes was carried out. Together with 1 μm silicon membrane after annealing, the total thickness reached 13 μm , which meet the design demand for 100Kpa silicon pressure sensor. In the third step (c), light boron was implanted to form piezoresistors with the resistance of 200~500 Ω /sq. Though 12 μm thick epitaxy film, the alignment can still be processed by the ASML stepper, and the piezoresistors were aligned and exposed. Silicon oxide and silicon nitride were deposited on the membrane and the

contact holes were etched. Aluminum was finally deposited and patterned to form connects (d). Figure 10 shows the SEM cross-section pictures of the silicon membrane over the sealed vacuum cavity.

4. Measurement and Results

Sensors were measured in a Model-GY-600 test chamber connected to pressure control equipment, shown in Figure 11. The sensor was put into the chamber and connected to the electrodes outside the chamber through an electrical

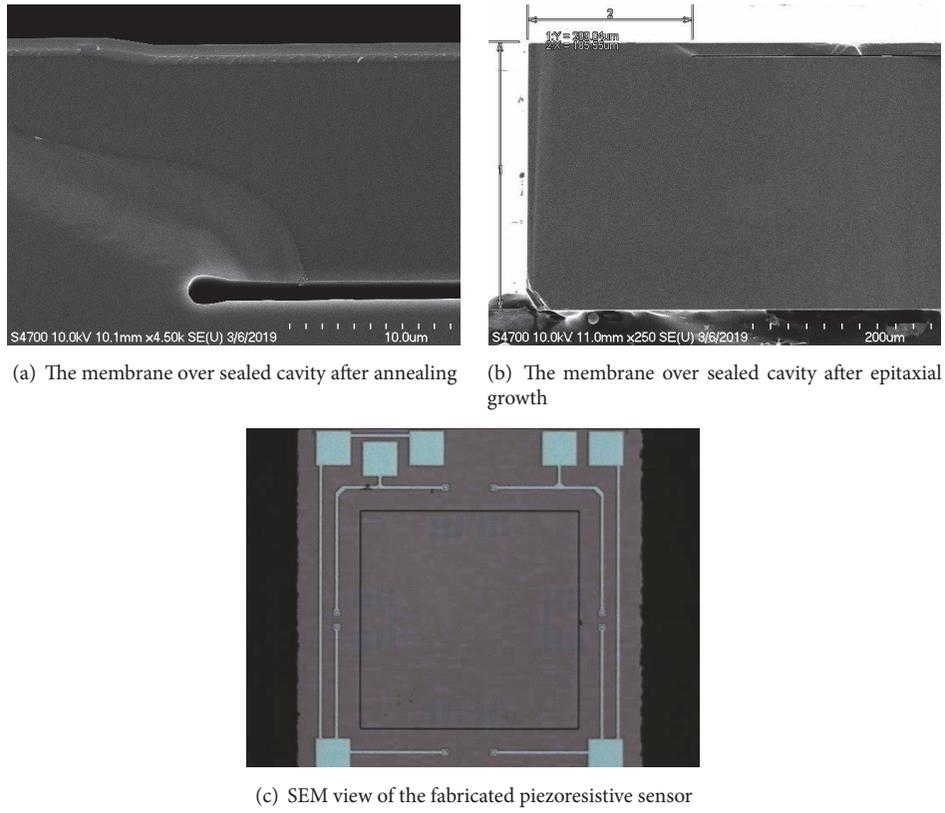


FIGURE 10: SEM picture of the process. (a) The cross-section of the silicon membrane, (b) the sealed vacuum cavity, and (c) the piezoresistive sensor.

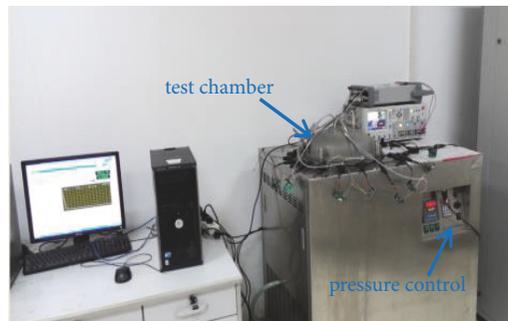


FIGURE 11: The test setup for a barometric pressure sensor.

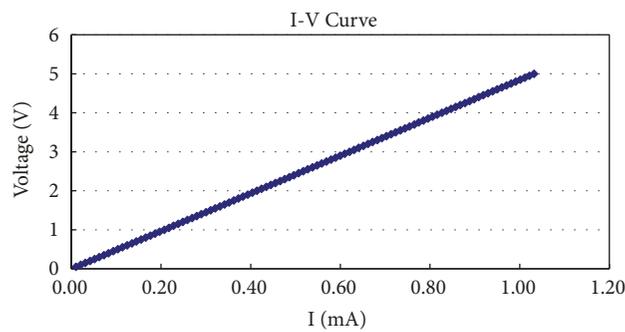


FIGURE 12: The I-V property of a piezoresistor at room temperature.

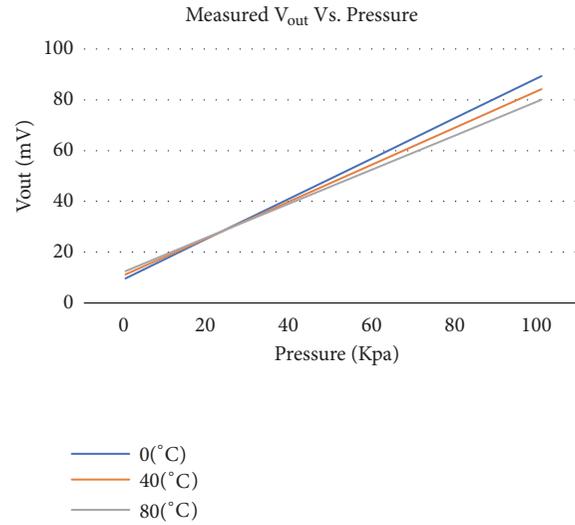


FIGURE 13: The measured bridge output of the pressure sensor as a function of pressure at different temperature (0°C, 40°C, and 80°C).

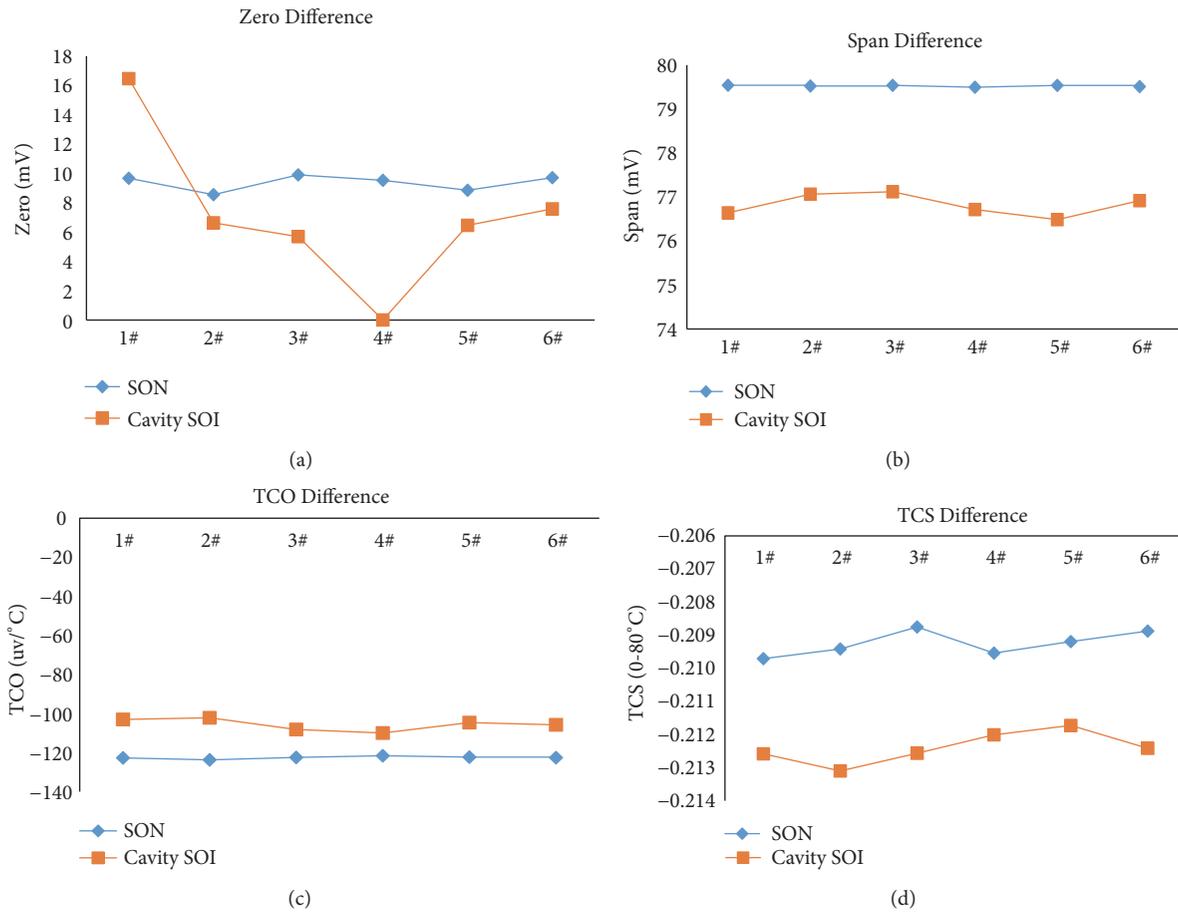


FIGURE 14: Comparison between SON and Cavity-SOI. (a) Zero-point output, (b) span, (c) TCO, and (d) TCS.

TABLE 2: Parameters of piezoresistive pressure sensors.

| | |
|----------------------------|-----------|
| Range(Kpa) | 0-100 |
| Span(mV) | 70-80 |
| Sensitivity(mV/kPa) | 0.7-0.8 |
| Non-Linearity(%FS) | 0.02 |
| Pressure hysteresis(%FS) | 0.007 |
| Temperature hysteresis(mV) | <0.1 |
| TCO($\mu V/^{\circ}C$) | ≤ 40 |
| TCS(%FS) | -0.202 |

interface. With the pressure controller, the pressure in the chamber was monitored while measurement.

Figure 12 shows voltage-current property of a fabricated piezoresistor at room temperature. It is clear that the resistance of the piezoresistor is measured to be 5.03k Ω .

Figure 13 shows the measured bridge output of the pressure sensor as a function of pressure with respect to different temperatures. Compared with the simulated data in Figure 8, the measured value, in Figure 13, was closed to calculated one. The offset is around 10 mV and the max span of 0 $^{\circ}C$ is close to 80 mV.

The sensitivity was measured to be 0.79, 0.72, and 0.67mV/kPa for 0 $^{\circ}C$, 40 $^{\circ}C$, and 80 $^{\circ}C$, respectively.

The nonlinearity was measured to be 0.02, 0.01, and -0.01%FS for 0 $^{\circ}C$, 40 $^{\circ}C$, and 80 $^{\circ}C$, respectively.

The pressure hysteresis was measured to be 0.007, 0.005, and 0.002%FS for 0 $^{\circ}C$, 40 $^{\circ}C$, and 80 $^{\circ}C$, respectively.

The temperature hysteresis was measured to be 0.056mV for 25 $^{\circ}C$.

The temperature coefficient of offset (TCO) was measured to be 29.80 $\mu V/^{\circ}C$.

The temperature coefficient of span (TCS) was measured to be -0.202%FS.

In order to study processing variations, different samples were measured. Table 2 shows a list of features of four different pressure sensors.

It shows that the pressure hysteresis is lower than 0.007%.

To compare with SON technology, the same design was fabricated by the Cavity-SOI technology [15], in which silicon membrane on the vacuum cavity was formed by anodic bonding or fusion bonding technology. Four regular parameters including zero-point output, span, TCO, and TCS were measured and showed in Figure 14. The membrane thickness of the SON devices has less variation than that of the Cavity-SOI, because the Cavity-SOI requires grinding the top wafer to desired values with a variation of $\pm 1\mu m$, while the SON by using epitaxy is less than $\pm 0.2\mu m$. Moreover, the Cavity-SOI has a lower throughput due to process steps including etching cavities/double-side lithography, bonding, and grinding, while the SON process takes less process steps. Thus, the SON devices are better in characteristic and throughput.

5. Conclusions

A process for a piezoresistive barometric pressure sensor is proposed and demonstrated by using a Silicon-on-Nothing

technology. All fabrication processes have been performed on the front side of the silicon wafer, and they avoid the use of double-side processing and wet bulk silicon micromachining, resulting in high production efficiency. The continuing monocrystalline silicon membranes and self-closed vacuum cavity assure the low hysteresis. And the SON devices demonstrated here are better than those fabricated by the Cavity-SOI.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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