Hindawi
Journal of Sensors
Volume 2021, Article ID 6618206, 5 pages
https://doi.org/10.1155/2021/6618206

Research Article

Design of a CMOS Lineal Hall Sensor Front-End Working in Current Mode with Programmable Gain Stage for Power Specific Chip

Peng Li,[1] Wei Xi,[1] Xianggen Yin,[2] Hao Yao,[1] and Huafeng Chen [3]

[1]*Digital Grid Research Institute, Artificial Intelligence and Chip Application Research Department, CSG, Guangzhou 510670, China*
[2]*State Key Laboratory of Advanced Electromagnetic Engineering and Technology, Huazhong University of Science and Technology, Wuhan 430074, China*
[3]*College of Electronics and Information Engineering, Zhejiang University of Media and Communications, Hangzhou 310018, China*

Correspondence should be addressed to Huafeng Chen; walfen@126.com

Received 28 November 2020; Revised 22 December 2020; Accepted 20 January 2021; Published 2 February 2021

Academic Editor: Kai Huang

With the continuous intelligentization of power systems, the demand for the integration of digital chips and sensor chips such as the Internet of Things is also increasing. A CMOS lineal magnetic Hall sensor front-end working in current mode with programmable gain stage is designed and implemented with SMIC 55 nm standard CMOS technology. By using a spinning-current technique, chopper technique, and digital calibration technique to eliminate the offset voltage and nonlinearity, this magnetic Hall sensor can be easily integrated into digital systems like SoCs. This work has already finished the circuit simulation and layout design, and all simulation indicators basically reach the expected value. The maximum gain of proposed sensor systems can be up to 33.9 dB. The total power is less than 4 mW. And the total area is less than 0.113 μm^2. The magnetic Hall sensor can be easily integrated into chips such as the power Internet of Things to form a single-chip-level SoC design, which is mainly used in applications such as circuit breakers and electric energy measurement.

1. Introduction

With the rapid development of very large-scale integrated circuits, various new types of equipment and various digital chips used in power grids and related digital-analog hybrid sensor chips are also emerging. Commonly used special control chips for power Internet of Things generally have an integration level only to the digital-analog/analog-to-digital converter level, and the corresponding sensor part still needs to be connected to an off-chip chip. Considering the realization of the overall function of the system and the realization of sufficient performance at a relatively low cost, SoC (System on Chip) design has gradually become the mainstream. On the premise of meeting standard CMOS silicon process manufacturing, many of the off-chip sensor circuit parts have already been integrated into the SoC to form a single-chip-level design. Hall sensor is one of which is easy to integrate with standard CMOS process. As a part of the special chip for the power Internet of Things, it can measure the current inside the line without contact by measuring the magnetic induction near the power line, which can be applied to various occasions such as circuit breakers and energy measurement.

Hall sensors are widely used in automotive and industrial applications such as current measurement, angle detection, and position detection. Hall sensors are preferred because of their low cost, low power, wide range, high sensitiveness, and great compatibility to standard CMOS. As the sensors are not fabricated in dedicated technology, they also suffer from sensitivity drift and offset in Hall plate. Usually, offset can be eliminated by spinning-current and chopper techniques. The sensitivity drift can be compensated by a look-up table, analog compensation technique, or digital calibration technique. The look-up table is the simplest way for sensitivity drift compensation, but the performance is poor. The analog compensation technique can have better performance

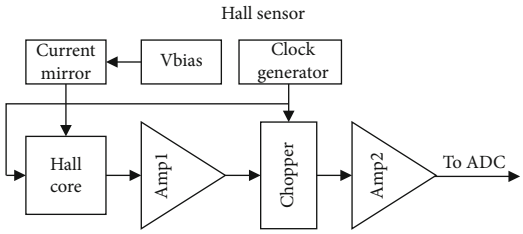


Figure 1: Main structure of Hall sensor front-end.

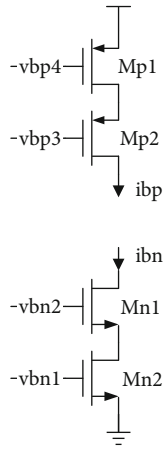


Figure 2: A pair of wide swing cascade current mirrors.

but leads to higher complexity and implementation cost. The digital calibration technique is preferred because it outperforms the look-up table and it is easy to implement in a digital domain with an elaborately designed calibration algorithm.

2. Materials and Methods

The main structure of the proposed Hall sensor system is presented in Figure 1. It consists of a Hall core, a current mirror and its bias, two stages of a differential amplifier, a chopper circuit, and a clock generator.

In this design, the Hall device is biased by a pair of current mirrors to produce a pair of differential Hall voltage. The differential Hall voltage is amplified by a differential amplifier Amp1 with constant gain. Then, the output of Amp1 goes through the chopper circuit to eliminate the offset voltage of the Hall plate. After the amplification of Amp2 with programmable gain, the final output is sampled and measured by a 16-bit 1MSps ADC, then processed in a digital domain. The clock generator produces different clocks for the Hall core to realize the spinning-current technique and for chopper to reduce Hall offset voltage. The detail of each block will be discussed below.

2.1. Current Mirror and Vbias. The Hall core is biased with 100 μA constant current to produce a stable Hall voltage. To get lower common-mode voltage of Hall voltage, a pair of current mirrors is implemented separately by PMOS and NMOS using a wide swing cascade structure. Figure 2 shows

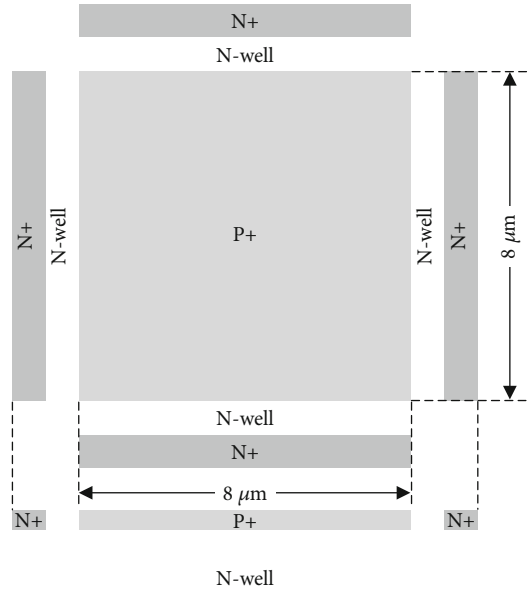


Figure 3: An N-well Hall device with geometry of 8 μm.

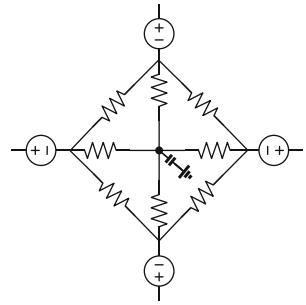


Figure 4: Simulation model of Hall device.

the details of current mirrors where nodes vbp4 to vbn1 come from Vbias circuit.

The Vbias circuit provides nodes from vbp4 to vnb1 for current mirrors. That is, it is basically a constant-Gm structure which can provide satisfying immunity to power supply [1].

2.2. Hall Core. The Hall core consists of a Hall device or so-called Hall plate and 8 switches. The Hall device is implemented with an N-type semiconductor, to be more explicit, the N-well region. Figure 3 demonstrates the typical geometry of the Hall device. Common types of Hall plate include rectangle, bridge, and cross. In this design, a cross type is chosen, and a P+ region is added on the top of N-well to get rid of the effect from the upper circuit.

Figure 4 shows a Hall plate model for circuit simulation. And its basic framework still adopts the most basic Wheatstone bridge structure [2, 3]. The four resistors on the arm represent the N-well diffusion resistance of the four interdigital regions. The four resistors in the middle represent the resistance in the central region of the Hall plate. The capacitor serves as the parasitic capacitance at the contact hole to simulate the transient response of the Hall plate. And the

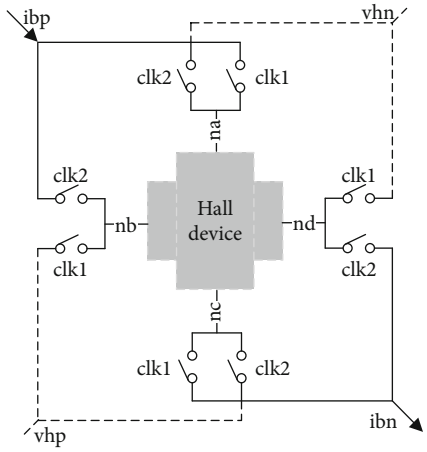


Figure 5: Structure of Hall core using spinning-current.

four current controlled voltage sources are used to simulate the Hall effect and controlled by the current flowing through the contact hole. The output voltage of this model varies from magnetic field intensity dynamically. For example, it can produce a pair of 84 μV differential Hall voltage, accompanied with 96 μV offset voltage under 10 mT@20 kHz. The circuit of this model is shown.

To eliminate the Hall offset voltage introduced by geometry asymmetry, we employ the spinning-current technique in the Hall core circuit by using 8 switches [4–8]. Figure 5 presents the basic structure. The clocks of 8 switches are 50% duty cycle square wave and can be up to 50 MHz. The phase between clk1 and clk2 is 180°. The current direction is from ibp to ibn. It works in 2 different phases.

In the first phase, the bias current flows from node na to node nc; thus, differential Hall voltage V_{sensor} is generated from node nb and node nd:

$$V_{\text{sensor}[1]} = V_{\text{Hall}[1]} + V_{\text{off}[1]}. \quad (1)$$

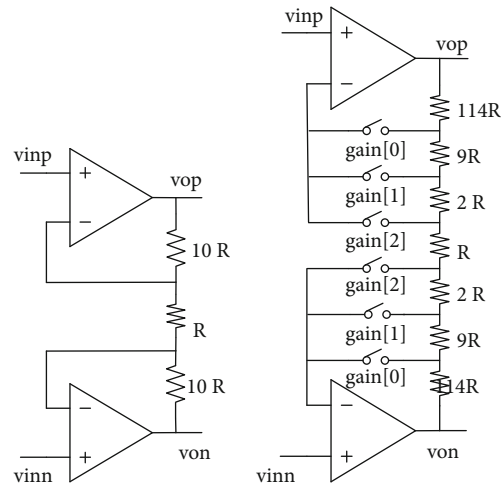
In the second phase, the bias current flows from node nb to node nd; thus, differential Hall voltage V_{sensor} is generated from node nc and node na:

$$V_{\text{sensor}[2]} = V_{\text{Hall}[2]} - V_{\text{off}[2]}. \quad (2)$$

If the switching frequency of the current direction is far greater than the change frequency of the magnetic field, then the magnetic field is approximately unchanged in these two phases. By subtracting the voltage obtained from these two phases, the differential Hall voltage becomes

$$V_{\text{sensor}} = V_{\text{sensor}[1]} + V_{\text{sensor}[2]} = 2V_{\text{Hall}} + \Delta V_{\text{off}}. \quad (3)$$

Using the rotating current technology with n ports and n phases can further reduce the offset voltage, but it will increase the complexity of the system and limit the working speed of the system. It is necessary to coordinate the relationship between the system speed and the offset voltage.



(a) Structure of Amp1 (b) Structure of Amp2

Figure 6: The structure of adopted differential amplifier.

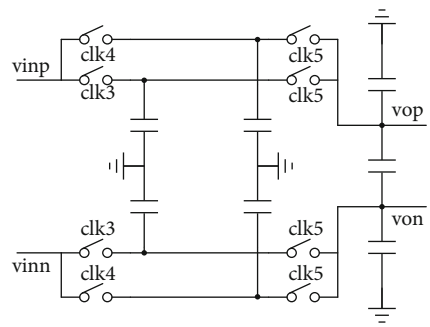


Figure 7: Chopper circuit structure.

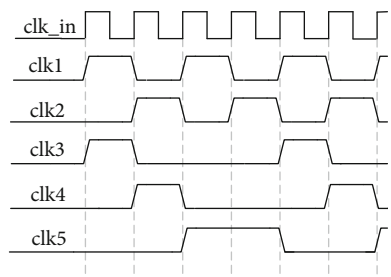


Figure 8: Phase diagram of the clock generator.

2.3. Differential Amplifier. The Hall effect is very weak. And the output Hall voltage of the modulation module is very small, which is in the order of μV~mV. Therefore, it must be amplified before demodulation. The differential amplifier consists of two single-ended operational amplifiers and several resistances. Since the output signal of the Hall disk is weak, the first stage of the gain adjustable amplifier needs low noise and high input impedance. For Amp1, a two-stage folded-cascode optional amplifier with Miller compensated is used in this design. For Amp2, three switches are used to obtain programmable gain. The detailed structure of Amp1 and Amp2 is shown in Figures 6(a) and 6(b). With such implementation,

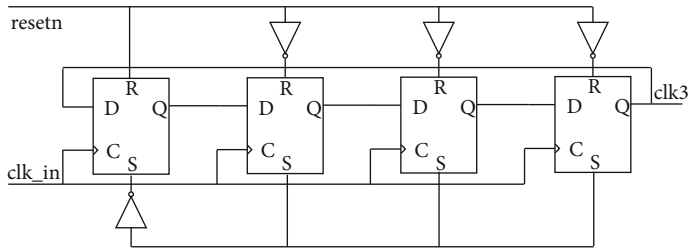


Figure 9: Ring D flip-flop structure.

Table 1: Parameters of 5 clocks.

	T_{rise}/ps	T_{fall}/ps	Duty	T (min)/ns
clk1	27.1	28.9	50 ± 0.1%	20 ± 0.02
clk2	27.9	28.8	50 ± 0.1%	20 ± 0.02
clk3	24.8	27.1	25 ± 0.1%	40 ± 0.04
clk4	24.5	27.2	25 ± 0.1%	40 ± 0.04
clk5	27.4	28.8	50 ± 0.1%	40 ± 0.04

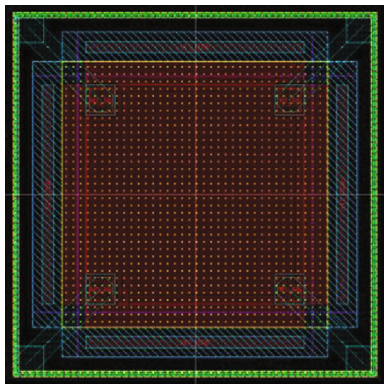


Figure 10: Layout design of Hall device.

Amp1 can provide a gain of 20, and Amp2 can provide a gain of 250/49.2/9.1 when gain[2]/gain[1]/gain[0] are enabled separately. The power supply of the operational amplifier implemented is 2.5 V, and the static power consumption is 370 μA. The open-loop gain is up to 80 dB. And the open-loop cutoff frequency is 200 MHz [9–11].

2.4. Chopper. The chopper circuit is designed between Amp1 and Amp2 to reduce the offset voltage of the Hall device by integrating Hall voltage vhp and vhn in two clock phases [12]. The chopper circuit is implemented with several capacitors. The detailed structure is shown in Figure 7. And clocks clk3 to clk5 are also generated by the clock generator. In the clk3 phase, $V_{sensor[1]}$ is stored on the capacitor. Then, in the clk4 phase, $V_{sensor[2]}$ is stored on the capacitor. In the clk5 phase, $V_{sensor[1]}$ and $V_{sensor[2]}$ are integrated on the output capacitor. As long as the ratio of input capacitance and output capacitance is controlled to be 2 : 1, the value of output capacitance is V_{Hall}.

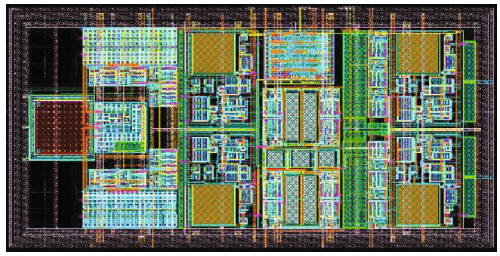


Figure 11: Layout design of the proposed Hall sensor system.

2.5. Clock Generator. The clock generator generates 5 clocks for the Hall core and chopper circuit [13]. The phase diagram of these clocks is presented in Figure 8. The parameters of these clocks are of vital importance. Thus, with ring D flip-flop structure and digital synthesis technique, these parameters can be strictly precise. Figure 9 shows the ring D flip-flop structure of the clock generator (for example, clk3), and Table 1 lists the parameters of these clocks.

3. Results and Discussion

This work has already finished the circuit simulation and layout design. The layout design of the proposed Hall plate is shown in Figure 10. And the layout design of the entire system is shown in Figure 11. The simulation results show that the proposed Hall sensor system can amplify a 168 μv (Vpp) Hall voltage (with 96 μv offset) to 414 mv (with -27 mv offset). By using the proposed Hall sensor system, the Hall voltage is amplified by 2460 times.

The performance summary is given in Table 2 (*The sensitivity is related to the Hall device model).

4. Conclusions

The simulation results show that the Hall sensor system front-end is capable of amplifying Hall voltage and reducing offset voltage. While integrated with ADC, the Hall voltage data can be easily processed with CPU or DSP. At the same time, since the design of the sensor system is based on the standard SMIC 55 nm process, with the necessary digital control logic and ADC part, the design is easy to integrate into the corresponding power specific SoC chips. The advantage of our Hall sensor system is small area consumption and easily integrated with SoC chips. And due to very high frequency spinning current technique, this Hall sensor system

Table 2: Main parameter compared with related work.

	This	[14]	[15]	[16]	Unit
Tech	55	180	350	180	nm
Plate size	8 × 8	8 × 8	/	/	μm^2
Num of plates	1	2	4	4	
Spinning frequency	50M	250k	20k	1k	Hz
Area	0.113	1.16	11.55	/	μm^2
Power	4	0.12	3.3	1.6	mW
Sensitivity	4.14 V/m*	1.6 V/A/T	50 mA/T	50 mV/T	
Nonlinearity	*	0.2%	0.8%	/	%
Offset	65 μT	50 μT	40 μT	25 μT	μT

can process up to 100 kHz alternating magnetic field with no more than -3 dB attenuation.

In this paper, a lot of work has been carried out on CMOS Hall device design optimization, offset elimination, and signal amplification circuit technology, as well as Hall device simulation modeling and other aspects. Though we have obtained some meaningful results, there are still some deficiencies. The future plan involves the following directions.

We have mainly adopted the dynamic offset elimination technology of two-phase spinning-current. However, the residual offset is still high, which is due to the sensitivity of the Hall device to the fluctuation of the manufacturing process and junction field effect. We will use the four-phase spinning-current technology combined with the fully symmetrical structure of the Hall device design to improve the ability of eliminating the Hall device offset and obtaining lower residual offset. In addition, the negative feedback technology will be applied to the signal conditioning circuit to reduce the residual offset caused by the signal conditioning circuit itself. The mechanical stress compensation technology in a chip will also be explored to eliminate offset caused by mechanical stress after packaging.

Data Availability

The raw/processed data required to reproduce the results obtained in this study cannot be shared at this time because they are used in an ongoing study.

Conflicts of Interest

The authors declare no conflict of interest.

References

[1] Y. Shen and R. Zhang, "Constant-gm bias circuit without off-chip components," in *13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Hangzhou, China, 2016.

[2] Y. Xu and H. Huang, "An accurate simulation model for cross-shaped CMOS Hall sensors," *Journal of Functional Materials and Devices*, vol. 20, no. 1, 2014.

[3] Q. He, Y. Xu, and F. Zhao, "Simplified simulation model for cross-shaped CMOS integrated hall sensor," *Instrument Technique and Sensor*, vol. 10, pp. 13–15, 2011.

[4] J. Jiang and K. A. Makinwa, "A multi-path CMOS Hall sensor with integrated ripple reduction loops," *IEEE Asian Solid-State Circuits Conference*, pp. 53–56, 2015.

[5] A. Ajbl, M. Pastre, and M. Kayal, "A Hall sensor microsystem with integrated voltage and current references for continuous sensitivity calibration," in *IEEE International Conference on Circuits and Systems (ICCAS)*, Kuala Lumpur, Malaysia, 2012.

[6] S. Zhang, S. Liu, C. Yuan, and N. Duan, "Design of the CMOS switching hall sensor circuit," in *International Conference on Sensors Networks and Signal Processing (SNSP)*, Xi'an, China, 2018.

[7] L. Wang, H. Pan, S. He, M. Zhao, and L. Li, "Optimization of integrated hall sensor," *Electron IC Measurement Technology*, vol. 34, no. 5, 2011.

[8] X. Zhang and R. Wei, "Design of the read-out IC for linear hall sensor," *China Integrated Circuit*, vol. 6, pp. 33–37, 2019.

[9] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, 1994.

[10] K.-J. de Langen and J. H. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, 1998.

[11] L. Moldovan and H. H. Li, "A rail-to-rail, constant gain, buffered op-amp for real time video applications," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 2, pp. 169–176, 1997.

[12] L. Jiang, W. Xu, and Y. Yu, "Design of CMOS integrated temperature sensor based on chopping and dynamic element matching," *Journal of Electronic Measurement and Instrument*, vol. 2009, no. 8, pp. 20–26, 2009.

[13] H. Huang, D. Wang, and Y. Yu, "Design of CMOS integrated 2D vertical Hall sensor circuit," *Journal of Electronic Measurement and Instrument*, vol. 29, no. 9, 2015.

[14] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A CMOS current-mode magnetic hall sensor with integrated front-end," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 62, no. 5, pp. 1270–1278, 2015.

[15] A. Ajbl, M. Pastre, and M. Kayal, "A fully integrated hall sensor microsystem for contactless current measurement," *IEEE Sensors Journal*, vol. 13, no. 6, pp. 2271–2278, 2013.

[16] J. Jiang, W. J. Kindt, and K. A. A. Makinwa, "A continuous-time ripple reduction technique for spinning-current hall sensors," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 7, pp. 1525–1534, 2014.