Hindawi
Journal of Sensors
Volume 2021, Article ID 6630100, 8 pages
https://doi.org/10.1155/2021/6630100

Research Article

A Small-Area, Low-Power Delta-Sigma DAC Applied to a Power-Specific Chip

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Received 3 December 2020; Revised 31 December 2020; Accepted 6 May 2021; Published 25 May 2021

Academic Editor: Harith Ahmad

This paper introduces a small-area, low-power delta-sigma DAC that can support power line carrier communication. In order to achieve the oversampling ratio of 128, a three-stage cascaded half-band filter is utilized. An optimized sturdy MASH $\Delta\Sigma$ modulator was used to avoid instability caused by high-order shaping and reduce the area at the same time. The postanalog reconstruction includes a switched-capacitor DAC (SC DAC) and a 4-tap FIR/IIR hybrid filter, which not only meets the requirements of low power but also promotes the out-of-band SNR. The final chip is fabricated in a 55 nm CMOS process, occupies 0.08 mm^2, and consumes 1.5 mW of analog power at 2.5 V supply. The simulation results show that the dynamic range is 85.7 dB, while the out-of-band SNR is 40.5 dB.

1. Introduction

The smart grid is a new type of grid based on the physical grid, combined with modern advanced computer technology, information technology, sensor measurement, and other technologies. Different from the traditional power grids in the past, today's power grids are not limited to one-way collection and have their own networking function, which can realize the interconnection of everything and the smart life of smart electricity. For example, in power line carrier communication (PLC) technology, wires can be used to distribute power to consumers and transmit data. In the PLC analog front-end transmitter, the digital-to-analog converter (DAC) is responsible for converting the digital baseband signal into an analog signal and loading it into the power grid. Low power and high resolution are required for DAC in PLC.

While increasing the function and reducing the size, extending the service life of the battery has been the focus of smart device design engineers for many years [1]. Low power consumption, small area, and high integration are the keys to the design of Very Large Scale Integration (VLSI). $\Delta\Sigma$ DAC is widely used in portable devices and smart grid equipment because of its low-speed, high-precision, high-integration, and low-cost characteristics.

The delta-sigma DAC introduced in this article has made a comprehensive consideration of performance, power consumption, and area in the digital and analog design. In the digital difference filter part, a three-stage half-band filter (HBF) cascade is used to reduce the number of filter stages. At the same time, an optimized sturdy MASH $\Delta\Sigma$ modulator is used to achieve the same signal-to-noise ratio while avoiding redundant matching circuits and further reducing the area. In addition, in the subsequent analog reconstruction part, the SC DAC is used to integrate the 4-tap FIR/IIR hybrid filter structure, which not only meets the requirements of low power consumption but also improves the out-of-band signal-to-noise ratio [2].

2. Materials and Methods

2.1. Proposed $\Delta\Sigma$ DAC Architecture. The $\Delta\Sigma$ DAC is composed of a digital front-end module and an analog reconstruction one. The digital front-end module includes a 128x interpolation filter, sturdy MASH 2-1 delta-sigma modulator

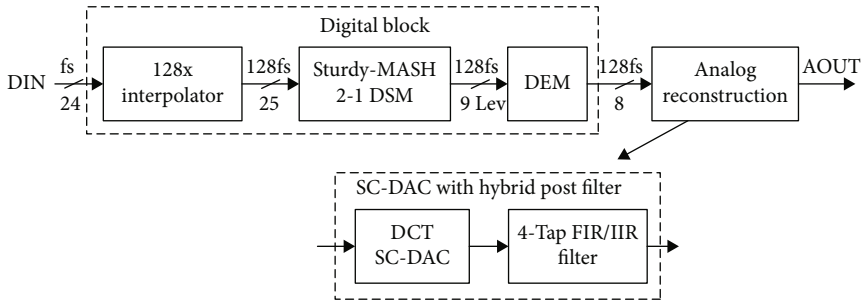

Figure 1: Delta-sigma DAC diagram.

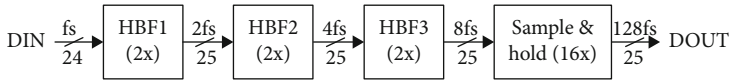

Figure 2: Interpolation filter diagram.

(DSM), and dynamic element matching (DEM); the analog reconstruction module includes a SC DAC and a 4-tap FIR-IIR hybrid postfilter. Figure 1 is the architecture diagram of the $\Delta\Sigma$ DAC. The input is a 24-bit PCM digital signal, and its sampling frequency is fs = 44.1 kHz. First, the signal is oversampled by using an interpolation filter by 128 times; then, an optimized MASH 2-1 DSM performs noise shaping on the signal, pushing the noise to high frequency and at the same time converting the high-bit digital stream into low-bit (4-bit) 9th-order digital flow; then, the DEM algorithm disrupts its thermometer coding bits to reduce the unit capacitance mismatch of the subsequent SC DAC; finally, the SC DAC realizes the digital-to-analog function, and the subsequent filter filters out-of-band noise.

2.1.1. Interpolation Filter. Considering the linear phase, a finite impulse response (FIR) filter is utilized instead of an infinite impulse response (IIR) filter [3]. The former has the virtues of simplicity and high feasibility. In order to further shrink the area, this design uses a half-band filter (HBF), a type of FIR, which has the characteristics of small filter coefficient multiplication and coefficient symmetry, and half of the coefficient is 0.

Figure 2 shows the diagram of the interpolation filter. The interpolation filter adopts a three-stage HBF cascade structure. The first two stages achieve the OSR (oversampling ratio) of 8, and the last stage is a sample-and-hold circuit, which increases the oversampling rate to 128 times. Table 1 summarizes the technical indicators of the three-level HBF.

2.1.2. Sturdy MASH Delta-Sigma Modulator. This design adopts sturdy MASH DSM. The input is 25 bits, while the output is the 9th order. Generally speaking, it is an effective way to improve the signal-to-noise ratio (SNR) with high-order loop filters in DSM. However, the higher the order, the worse the stability and the more difficult the engineering realization [4]. The authors [5] proposed the Multistage Noise Shaping Modulator (MASH DSM). It eliminates the stability problem of high-order modulators through measurement and subtraction between multiple levels. However, in terms of $\Delta\Sigma$ ADC, the MASH structure has a matching problem between analog and digital parts [6]. Considering $\Delta\Sigma$ DAC, there is also a trade-off between the accuracy and area. To solve the aforementioned shortcomings, scholars have successively proposed and studied the sturdy MASH $\Delta\Sigma$ modulator [6–9]. In short, compared with the single-stage structure, sturdy MASH DSM is more stable and suitable for multibit quantization. Furthermore, compared with the MASH structure, the output of the second stage is coupled back into the first loop without additional cancellation logic, thereby reducing the area.

Table 1: Technical indicators of the three-level HBF.

	Orders	Passband frequency (normalized)	Passband ripples (dB)
HBF1	70	0.4535	0.02
HBF2	10	0.2268	0.016
HBF3	6	0.1134	0.01

Figure 3 shows the architecture of sturdy MASH 2-1 DSM. As the name implies, the DSM is divided into two stages. The loop filter of the first stage adopts a second-order cascade-of-resonators feedback form (CRFB) and optimizes the in-band zero to produce two complex zeros located at 20 kHz [2], which further improves SNR; the second stage is a first-order function. The signal transfer function (STF) and noise transfer function (NTF) of the first stage are as follows:

$$\mathrm{STF}_1 = \frac{z^{-1}}{1 + g \bullet z^{-1}}, \tag{1}$$

$$\mathrm{NTF}_1 = \frac{1 + (g-2) \bullet z^{-1} + z^{-2}}{1 + g \bullet z^{-1}}. \tag{2}$$

The STF and NTF of the second stage are as follows:

$$\mathrm{STF}_2 = 1, \tag{3}$$

$$\mathrm{NTF}_2 = 1 + z^{-1}. \tag{4}$$

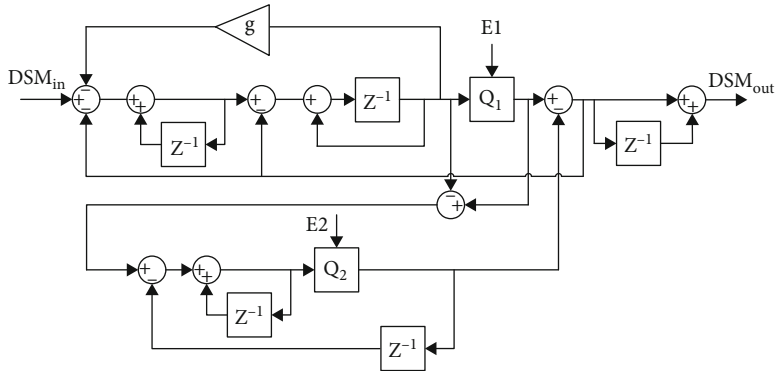

Figure 3: Sturdy MASH 2-1 DSM architecture.

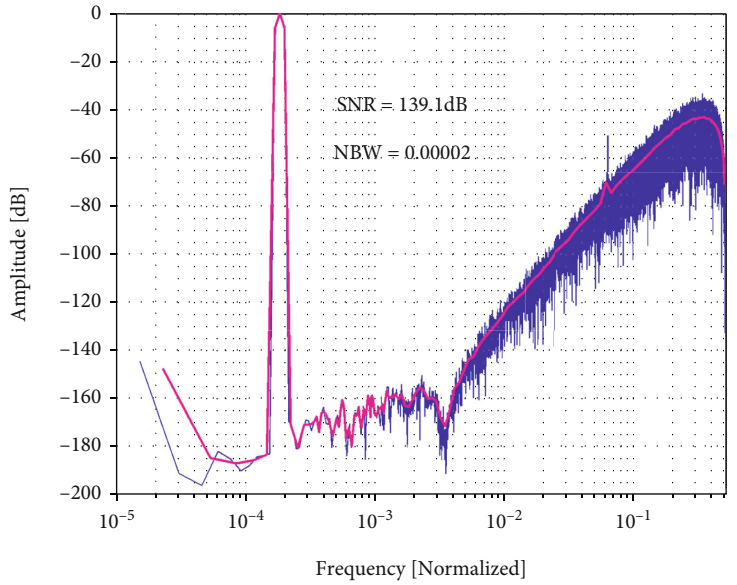

Figure 4: DSM simulation spectrum.

The equation of the overall DSM is as follows:

$$\mathrm{DSM_{out}} = \mathrm{DSM_{in}}\bullet\mathrm{STF_1} + E_1\bullet\mathrm{NTF_1}\bullet(1-\mathrm{STF_2}) - E_2\bullet\mathrm{NTF_1}\bullet\mathrm{NTF_2}. \tag{5}$$

$\mathrm{DSM_{in}}$ and $\mathrm{DSM_{out}}$ are the input and the output of DSM, respectively. STF_i, NTF_i, and E_i are the STF, NTF, and quantization error of the i-th stage, respectively, and g is the feedback coefficient in the first stage (the actual value is 2^{-11}).

By incorporating Equations (1)–(4) into Equation (5), the first-level quantization noise (E1) can be eliminated, leaving only the second-level quantization noise (E2), so that the overall DSM STF and NTF formulas are as follows:

$$\begin{aligned}\mathrm{STF_{top}} &= \frac{z^{-1}}{1+g\bullet z^{-1}},\\ \mathrm{NTF_{top}} &= \frac{\left(1-z^{-1}\right)\bullet\left[1+(g-2)\bullet z^{-1}+z^{-2}\right)]}{1+g\bullet z^{-1}}.\end{aligned} \tag{6}$$

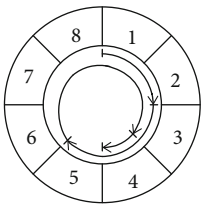

Figure 5: DWA algorithm diagram $\{2, 3, 6, 1\}$.

The last module of DSM, i.e., $1 + z^{-1}$, induces a pole at fs/2 to attenuate high-frequency noise and idle sounds [10]. MATLAB's SIMULINK tool was used to simulate DSM, and the input signal is 1 kHz, which was sampled at 128×44.1 kHz. Figure 4 shows the DSM simulation spectrum.

It shows that there is a notch at fs/2 (normalized = 1) and 20 kHz (normalized = $3.543e^{-3}$). The former is due to the function of $(1 + z^{-1})$ followed by DSM, while the latter is caused by the zero optimization of the first stage in DSM. The simulation results are consistent with the previous theory.

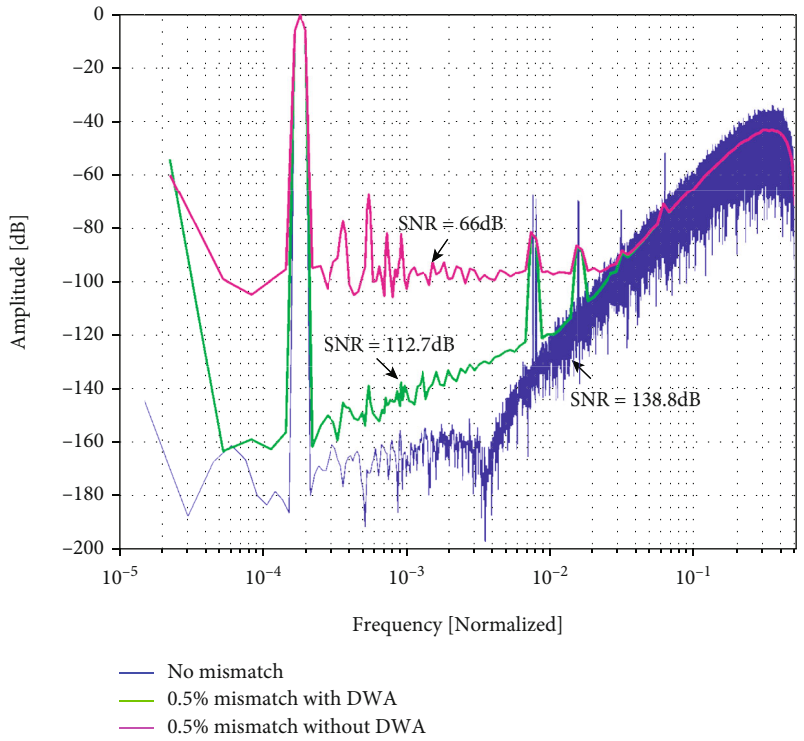

Figure 6: Digital front-end output spectrum, with no mismatch, 0.5% mismatch without DWA, and 0.5% mismatch with DWA.

2.1.3. DEM. Since the DSM uses multibit quantization, a subsequent multibit DAC is required for digital-to-analog conversion. Due to process limitations, the unit capacitance cannot be perfectly matched; that is, there are inevitable nonlinear problems. In addition to factory calibration (such as laser fine-tuning) and analog calibration [4], a more cost-effective way is digital correction. The DEM algorithm is commonly applied in digital correction. DEM uses a random selection algorithm to make unit devices as equally probable as possible and converts mismatch errors into white noise [11]. Data Weighted Average (DWA) is the first-order error shaping algorithm of DEM, and its working mechanism is rotation selection.

An example of the 8-element DWA algorithm is illustrated in Figure 5. Assume that the selection sequence is 2, 3, 6, 1, and each element is selected cyclically. Under the high-frequency clock, the cumulative average of the error is close to 0. That is, the low-frequency adaptation error is pushed to the high frequency. In addition to the first-order error shaping algorithm, many researchers have proposed second-order or even higher-order shaping algorithms, such as vector-based error shaping [12–14] and tree structure-based error high-order shaping [15]. Owing to its complicated circuit structure and stability issues, high-order shaping is not taken into our consideration, although it has a better noise shaping performance than the first-order one.

The digital front-end output spectrum, with no mismatch, 0.5% mismatch without DWA, and 0.5% mismatch with DWA, is shown in Figure 6. The simulation tool is MATLAB SIMULINK. In order to better distinguish between different curves, the 0.5% mismatched curve has been processed by a log smooth function to average the power and reduce the variance [4]. Under a 0.5% mismatch, SNR is 65 dB without DWA, while SNR with DWA is only 20 dB lower than the ideal SNR, which meets the design requirements.

2.1.4. Analog Reconstruction Module. As mentioned earlier, the final output of the DSM is a 9th-order bit stream; therefore, a low-bit DAC is needed to realize the digital-to-analog function. At the same time, because DSM introduces a lot of high-frequency noise, a poststage filter is included to purify the signal. The main purpose of this design is low power consumption and small area, so the direct charge transfer switch capacitor DAC (DCT-SC DAC) is adopted [11, 16]. Compared with current steering DAC, DCT-SC DAC is more insensitive to clock jitter and has lower power consumption. Furthermore, this structure allows hybrid filtering of FIR and IIR, which can significantly reduce out-of-band noise. In order to obtain a larger out-of-band SNR (SNR_{out}), the authors in [2] extended the FIR tap on the basis of [16]. The analog reconstruction module of this design is SCT-SC DAC, integrating a 4-tap FIR/IIR hybrid filtering function.

Figure 7 is a block diagram of the analog reconstruction module. There are 4 groups of different unit capacitor arrays. The input is the thermometer code after DEM scrambled a total of 16 bits (of which 8 bits are logical NOT), controlling different switches (SW). The input code is sequentially delayed by a unit clock, controlling the switches of different

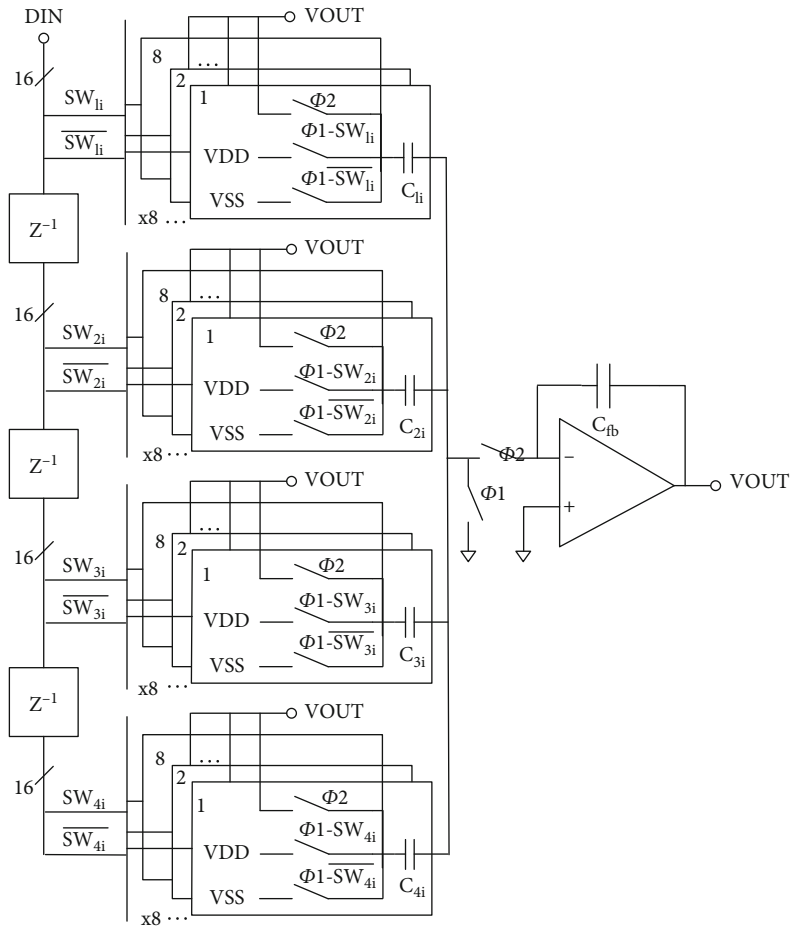

Figure 7: Block diagram of the analog reconstruction module.

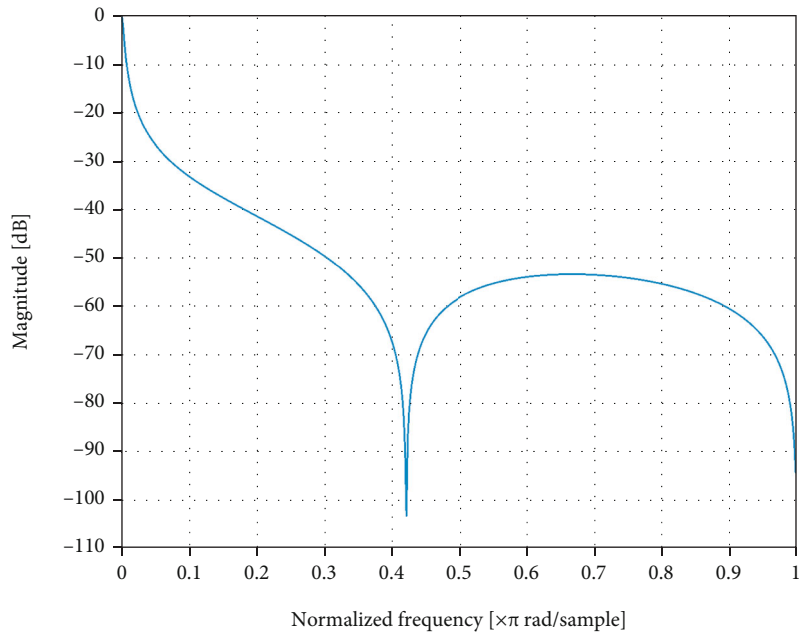

Figure 8: 4-tap FIR/IIR frequency response curve.

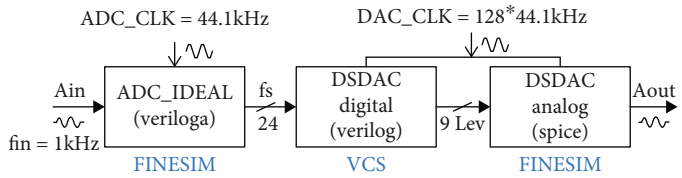

Figure 9: DSDAC hybrid simulation structure.

groups to function the 4-tap FIR filtering [2]. During phase 1 ($\Phi 1$), all unit capacitors (C_{1i}, C_{2i}, C_{3i}, and C_{4i}) are sampled (charged or discharged). During phase 2 ($\Phi 2$), all potential capacitors are connected in parallel with C_{fb} and direct charge transfer occurs. Since the amplifier does not provide driving current, the power consumption is greatly reduced, and the design of the amplifier will not be tricky. An operational amplifier with fully differential input and single-ended output is used for the sake of the small area. The transmission equation of the hybrid 4-tap FIR/IIR is as follows:

$$H\left(z^{-1}\right) = \frac{C_1 + C_2 \bullet z^{-1} + C_3 \bullet z^{-2} + C_4 \bullet z^{-4}}{C_{\text{fb}} + C_1 + C_2 + C_3 + C_4 - C_{\text{fb}} \bullet z^{-1}},$$
$$C_1 = \sum_{i=1}^{8} C_{1i}, C_2 = \sum_{i=1}^{8} C_{2i}, C_3 = \sum_{i=1}^{8} C_{3i}, C_4 = \sum_{i=1}^{8} C_{4i}. \quad (7)$$

In this design, $C_{\text{fb}} = 16$ pF, $C_{1i} = 40$ fF, $C_{2i} = 20$fF, $C_{3i} = 20$ fF, and $C_{4i} = 40$ fF. With MATLAB simulation, the frequency response curve of the hybrid 4-tap FIR/IIR transfer function is shown in Figure 8. It can be seen from the figure that the curve has notches at fs/2 and $0.42 \cdot$ fs/2, and its cut-off frequency is about $0.018 \cdot$ fs/2 = 50 kHz, which greatly reduces SNR_{out} while not compromising the in-band signal.

2.2. Simulation and Results. This design adopts a simulation method called digital-analog hybrid simulation, with VCS (digital front-end part) and FINESIM (ideal ADC and analog part) tools, verifying and analyzing the entire DAC system. A block diagram of the DSDAC hybrid simulation structure is shown in Figure 9. The input analog signal frequency is 1.03359 kHz (the number of FFT points is 216, and the signal frequency is perfectly located at one of the bins of the FFT, which can effectively avoid spectrum leakage [4]), and the sampling frequency is 44.1 kHz. We use the Verilog language to construct an ideal 24-bit ADC to assist simulation. The synthesizable behavioral Verilog is used as a simulation model for the digital front-end part, and the XRC Spice netlist is used as the analog simulation model.

The data of the transient simulation is output to a file at 1/fs time interval. Then, we import the file into MATLAB for spectrum analysis, with the number of FFT points being 216. Figure 10 presents an in-band output spectrum of 1 kHz full amplitude input signal. And the SNR is 63.2 dB. An in-band output spectrum of 1 kHz -6 dB input signal

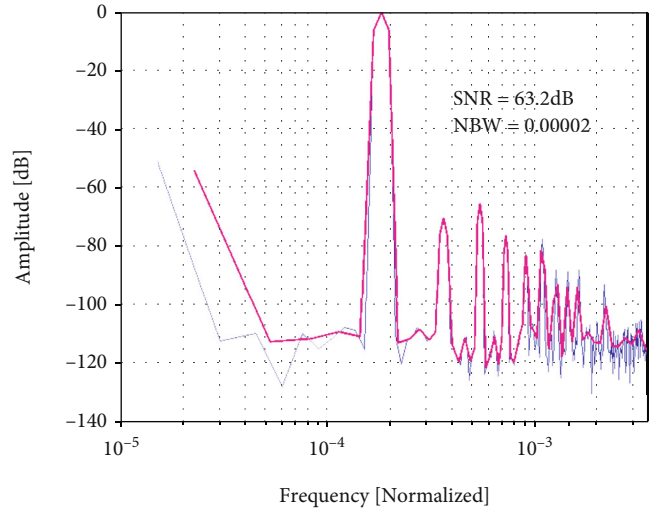

Figure 10: In-band output spectrum of 1 kHz 0 dBFS input signal.

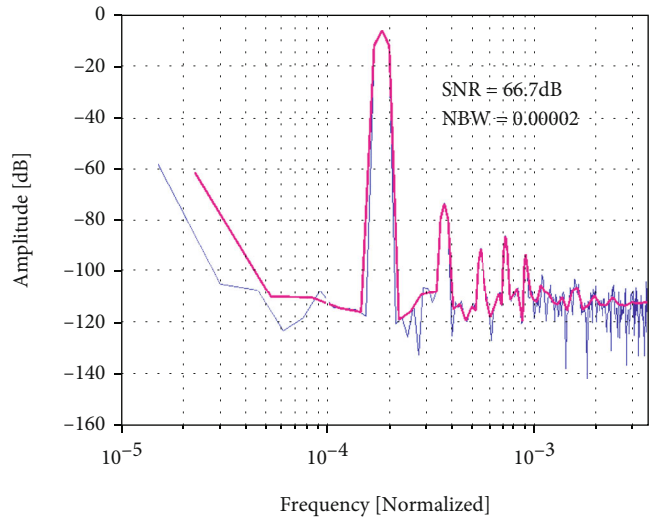

Figure 11: In-band output spectrum of 1 kHz -6 dBFS input signal.

(-6 dBFS) is shown in Figure 11, and the SNR is 66.7 dB. Figure 12 is an in-band output spectrum of 1 kHz -60 dBFS input signal, and the SNR is 25.7 dB. For audio equipment, the dynamic range (DR) is usually calculated as SNR of 1 kHz at -60 dBFS [16]. Therefore, the dynamic range is

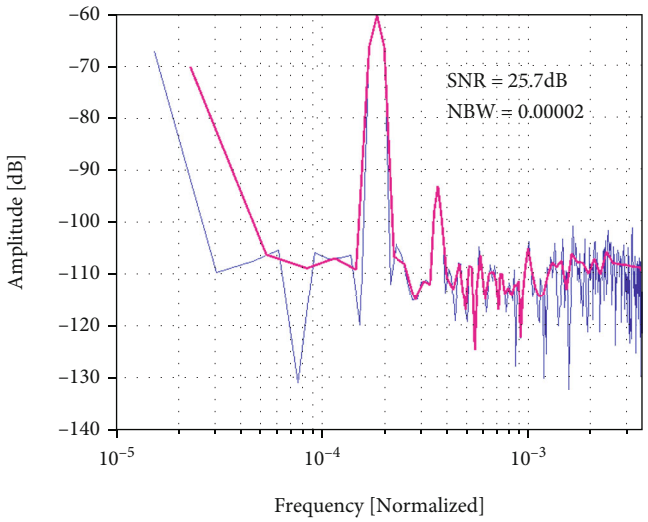

Figure 12: In-band output spectrum of 1 kHz -60 dBFS input signal.

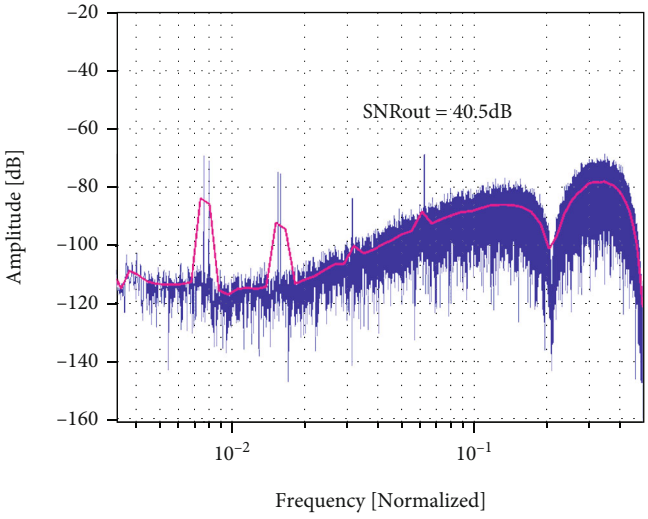

Figure 13: Out-of-band output spectrum of 1 kHz 0 dBFS input signal.

85.7 dB. Figure 13 shows the out-of-band output spectrum when the input signal is 1 kHz with 0 dBFS. It can be seen from the figure that the SNR_{out} is 40.5 dB. And the signal has two notches probably at fs/2 and 0.21 fs, which is consistent with the previous 4-tap FIR/IIR hybrid filter transfer function spectrum response results.

Table 2 summarizes the simulation performance of DSDAC. Due to the limitation of harmonics, the performance of the actual peak SNR is not ideal. A jitter can be added to DSM to avoid the interference of idle tones in subsequent experiments [2, 3].

The chip is based on 55 nm CMOS technology. The digital and analog parts are powered by 1.2 V and 2.5 V, respectively. Finally, DSDAC is integrated into SoC (System on Chip), and the AXI-Lite bus is used for interactive control.

Table 2: DSDAC performance summary.

	This work	[2]	[3]
Types of results	Postlayout simulation	Experiment	Experiment
Process	55 nm	0.13 μm	0.35 μm
Supply (V)	1.2*/2.5**	1.2*/3.3**	0.8
Power (mW)	1.5**	14.5	2.6
Output swing	0.48 Vpp	0.9 Vrms	0.56 Vpp
SNR (dB)	66.7	88	69
DR (dB)	85.7	97	88
SNR_{out} (dB)	40.5	39	—
Area (mm^2)	0.05*/0.03**	0.44	3.52***

*Digital part; **analog part; ***including a headphone driver.

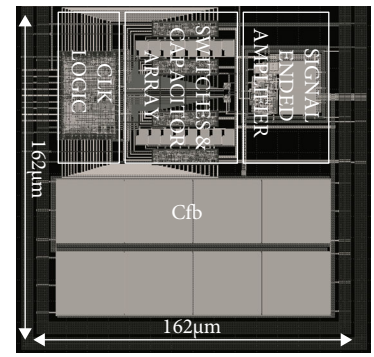

Figure 14: Analog part layout.

Figure 14 shows the layout of the analog part. The total area of the analog part is 160 μm × 160 μm.

3. Conclusions

Considering the endurance and integration of applications such as smart grids and portable electronic devices, this article designs and implements a small-area, low-power $\Delta\Sigma$ DAC. In terms of small area, we focus on the digital front-end part, using a three-level cascade HBF and an optimized sturdy MASH structure for the DSM; in terms of low power consumption, the main optimization of the analog reconstruction part is to use SC DAC and 4-tap FIR/IIR hybrid postfiltering. It not only improves the SNR_{out} but also reduces power consumption. The analog area is only 0.08 mm^2 in the 55 nm CMOS process. Circuit simulation shows that DR is 85.7 dB, the SNR_{out} is 40.5 dB, and the analog power consumption is 1.5 mW. It is suitable for high-efficiency and low-cost information transmission systems in the power field.

Data Availability

The raw/processed data required to reproduce the results obtained in this study cannot be shared at this time because they are used in an ongoing study.

Conflicts of Interest

The authors declare no conflict of interest.

Acknowledgments

This work is supported by the National Key R&D Program of China (2020YFB0906000, 2020YFB0906001).

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