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Research Article

Multipurpose Drivers for MEMS Devices Based on a Single ASIC Implemented in a Low-Cost HV CMOS Process without a Triple Well

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This paper presents a novel topology for multipurpose drivers for MEMS sensors and actuators, suitable for integration in low-cost high-voltage (HV) CMOS processes, without a triple well. The driver output voltage, V_{MEMS}, can be programmed over a wide, symmetrical range of positive and negative values, with the maximum output voltage being limited only by the maximum drain-source voltage that the HV transistors can handle. The driver is also able to short its output to the ground line and to leave it floating. It comprises generators for large positive and negative voltages followed by an LDO for each polarity that ensures that V_{MEMS} has a well-controlled level and a very low ripple. The LDOs also help implement the grounded- and floating-output operating modes. Most of the required circuitry is integrated within a HV CMOS ASIC: the drivers for the large voltage generators, the error amplifiers of the LDOs, the DAC used to program the V_{MEMS} level, and their support circuits. Thus, only the power stages of the large voltage generators, the pass transistors of the LDOs and two resistors for the LDO feedback network are discrete. A suitable configuration was devised for the latter that allows for the external resistor network to be shared by the two LDOs and prevents negative voltages from developing at the ASIC pins. Two circuit implementations of the proposed topology, designed in a low-cost 0.18 μm HV CMOS process, are presented in some detail. Simulation results demonstrate that they realize the required operating modes and provide V_{MEMS} voltages programmable with steps of 100 mV or 200 mV, between -20 V and +20 V or between −45 V and +45 V, respectively. The output voltage ripple is relatively small, just 3.4 mVpkpk for the first implementation and 17 mVpkpk for the second. Therefore, both circuits are suitable for biasing and controlling a wide range of MEMS devices, including MEMS mirrors used in applications such as endoscopic optical coherence tomography.

1. Introduction

Microelectromechanical system (MEMS) devices are ubiquitous in technologies nowadays, from inkjet printers to smartphones and cars, from health monitoring to medical diagnosis and microsurgery tools, and from environmental monitors to microphones and loudspeakers, to name just a few applications [1]. MEMS devices have been developed based on thermoelastic, piezoelectric, and magnetic forces, but the electrostatic force remains the most employed by far. In general, electrostatic-driven MEMS devices require low-power biasing and control while providing fast responses to control voltages; also, their design and implementations are straightforward and they are well suited to silicon integration in single-chip systems that include the support and signal processing circuitry [2]. This paper focuses on electrostatic-driven MEMS sensors and actuators, particularly on the circuits used to generate the required high-voltage potentials.

The designer of an electrostatic-driven MEMS device must balance contradictory requirements regarding the area, response time, and value of the actuation voltage. In general, the actuation voltage is inversely proportional to the actuation area while the response time is inversely proportional to the

mechanical resonance frequency. Therefore, the actuation electrodes must be large enough to keep the required actuation voltage reasonably low. But a large area usually results in a longer response time. To improve the response time, one may use a higher spring constant—but this means a larger electrostatic force, so a higher actuation voltage—or to reduce the mass of the actuation area—but this often means decreasing the actuation area, which again means a larger actuation voltage. Decreasing the spring constant is not a valid option, either: it leads to a low restoring force, making the moveable part prone to sticking and to a large response/restore time.

A typical compromise is to design MEMS device components of hundreds of micrometres in length and width, driven by voltages in the range of tens of volts and with response times in the range of a few to tens of microseconds [3, 4].

An unwanted side effect of using high actuation voltage levels is the dielectric charging or charge trapping between MEMS electrodes, which reduces the lifetime of the device [5]. The typical solution is to toggle periodically the body potential between a positive and a negative level [5–7]. In [8, 9], the body of a capacitive RF MEMS switch was periodically connected to the ground line; then, it was left floating. A charging-floating-discharging sequence of the body terminal can be even more effective.

Therefore, a driver for MEMS devices should provide at its output positive and negative voltages with relatively large values—typically several times larger than its unipolar supply voltage; it should also be able to ground the output or to leave it floating so that it presents a high output impedance.

Besides DC biasing, MEMS sensors often require accurate control voltages, as well. A DC voltage programmable between 5 V and 45 V was used in [10] to control the tilting angle of micromirrors between 0.24° and 2.55°; in [11], DC voltages up to 30 V were applied to the top or middle membranes of capacitive mass-based MEMS sensors, to enhance their operational properties, particularly their sensitivity. MEMS varicaps have similar requirements: the voltage levels used in [12] varied from 10 V to 22 V, while in [13], the range was from 0 to 20 V.

Few drivers capable of implementing at least some of these requirements have been reported so far. They are usually implemented in expensive technologies able to handle negative voltages, lower than the substrate potential of the integrated circuit: silicon on insulator (SOI) [14], silicon on sapphire (SOS) [7], or triple-well CMOS processes [15–17]. These technologies simplify the circuit design, as standard implementations of DC-DC converters and analog multiplexers can be integrated.

However, the continuous quest for size and cost reduction demands MEMS devices to work in conjunction with integrated circuits manufactured in low-cost CMOS processes and even to be realized on the same CMOS substrate—the CMOS MEMS monolithic integration [18]. Complex MEMS devices can be integrated alongside electronic circuitry in a standard CMOS process, with only mask-less post-CMOS processing [10].

The cheapest HV CMOS processes provide neither a triple well nor a floating well. Often, they are derived from CMOS-based processes by adding a few more masks for the thick gate oxide and drain extensions required to implement HV transistors. ASICs developed in such processes cannot handle negative voltages (lower than the substrate potential) and cannot integrate floating diodes [19]. The maximum current that these HV devices can handle is limited to a few hundred mA, and the maximum operating voltages are typically no larger than 50 V, with rare exceptions going up to 100 V—see [20–22].

These limitations require that new topologies and circuit solutions are developed for MEMS drivers that can be implemented in such low-cost HV CMOS technologies. Additional design challenges are brought in by the applications envisaged here: low-cost single-ASIC drivers for MEMS mirrors used in endoscopic optical coherence tomography (OCT) [23] and similar precision applications [10]. An extended review of such devices was presented in [23]: it showed that large voltage levels (16 V to 300 V) are required to obtain large tilting/scan angles (±2° to ±20°) and also that voltage levels need to be precisely controlled and programmable in fine steps and should exhibit a very low-voltage ripple. Of course, a driver able to meet these requirements can also be used to control a variety of MEMS sensors, as well as to bias the body of MEMS switches.

Of the very few solutions proposed so far in the open literature, the single-ASIC driver for MEMS body biasing reported in [19] comes closest to fitting the requirements listed above. That driver consists of two high-voltage generators that provide the large positive and negative voltages required by the system, called V_{POS} and V_{NEG}, followed by an external multiplexer that conveys one of these voltages to the output. The controlling device and the driver operate from the same, low-voltage supply, and they have a common ground line. The drivers for the high-voltage generators and the control circuitry for the multiplexer are integrated in an ASIC implemented in a low-cost HV CMOS process, without a triple well. Thus, only the power stages of the high-voltage generators and the high-voltage transistors that implement the voltage multiplexer are not integrated. However, as the one-ASIC driver reported in [19] was designed for MEMS body biasing, it is not suitable for accurate control of MEMS sensors on at least three counts: (i) there should be a narrow and discontinuous output voltage range (−20 V to −10 V and +10 V to +20 V, respectively), (ii) there should be a large output voltage ripple (60 mV_{pkpk} for V_{MEMS} = +20 V and 160 mV_{pkpk} for V_{MEMS} = −20 V), and (iii) the output cannot be grounded.

This paper proposes a novel circuit topology for implementing low-cost and high-performance multipurpose drivers suitable for the precise control of a large variety of MEMS sensors. To reduce the production costs, most circuitry is integrated within an ASIC, which can be implemented by using low-cost HV CMOS technologies. These drivers provide an accurate voltage level programmable over a wide-range, low-voltage ripple and are able to short their output to the ground line or to leave it floating. Of course, they can also be used for biasing the body of MEMS switches.

Two proof-of-concept circuit implementations are presented. Thus, the proposed topology is validated by simulations run on circuits designed in a low-cost 0.18 μm HV CMOS process without a triple well, but with HV transistors able to withstand drain-source voltages of up to 50 V.

The requirements set for these drivers are listed in Section 2, which also describes the novel driver topology. Section 3 and Section 4 present the two circuit implementations. The first one employs only charge pumps while the second uses an effective, compact implementation of an inductor-based boost converter and inverting charge pump ensemble. Section 5 summarizes the key points and contributions and compares the drivers presented here against the state-of-the-art.

2. System-Level Requirements and Limitations of Existing Solutions and the Proposed Topology

2.1. Main Requirements for the Envisaged Driver and Limitations of Existing Solutions. The typical application envisaged for the drivers presented here is the MEMS mirrors used in endoscopic OCT [23]. Besides the general requirements for MEMS drivers listed in the Section 1 (ability to generate large positive and negative voltages, ground the output, or leave it floating), for such precision-sensitive application, the positive and negative voltages outputted by the driver should be precisely controlled and programmable in fine steps over a range as wide as possible, while maintaining a reduced voltage ripple [23]. Moreover, the size of the MEMS device and its driver is important; also, routing a high-voltage potential into an endoscopic probe is to be avoided. These problems can be solved by (a) integrating as much of the driver circuitry as possible into one ASIC and (b) MEMS-CMOS monolithic integration, whereby the MEMS devices are built on top of the silicon die that the driver is integrated in, and (c) having the ASIC realized using low-cost HV CMOS processes, for a cost-effective solution.

The multipurpose drivers for MEMS devices envisaged in this paper are designed to meet the following real-life set of requirements:

(i) The supply voltage, V_{IN}, varies between 4.5 V and 5.5 V

(ii) In the operation modes called hereafter "POS" and "NEG", the driver supplies a positive ("POS" mode) and a negative ("NEG" mode) output voltage, V_{MEMS}, programmable between (0 V and 20 V, then −20 V to 0 V), with a resolution of 100 mV or between (−45 V to +45 V), with a resolution of 200 mV

(iii) In all cases, the voltage ripple of V_{MEMS} is kept below 10 mV_{pkpk}

(iv) When transitioning from a positive to a negative value, V_{MEMS} reaches 95% of its programmed value, within 100 μs; when transitioning between two values with the same polarity but 1 V apart, V_{MEMS} settles in less than 2 μs. At startup, V_{MEMS} can reach its maximum value within 10 ms

(v) Mostly nowadays, MEMS require the driver to source/sink currents in the hundreds of μA–mA range. To ensure enough margin and be a future proof, a target of 2 mA was set for the maximum current that the driver, discussed here, should handle while providing the voltage V_{MEMS}

(vi) In the "ZERO" operating mode, the driver shorts its output to the ground line, by a resistance no larger than 20 kΩ

(vii) In the "OPEN" operation mode, the driver output is left floating, with no DC path to the ground or supply lines

(viii) The number, cost, and complexity of components (the bill of materials (BoM)) should be minimized. For this, most of the circuitry should be integrated into one ASIC, designed in a low-cost 0.18 μm HV CMOS process, without triple-well and floating diodes, but with drain-extended transistors able to withstand a maximum drain-source voltage of 50 V

(ix) Low power consumption and high efficiency are general targets for the driver

To the authors' best knowledge, no such driver has been reported in the open literature so far. The requirement to only use one ASIC implemented in a low-cost HV CMOS process is the main challenge and differentiator. The shortcomings of the published solution that comes closest to meeting these requirements—the driver for MEMS body biasing reported in [19], which uses one ASIC—were described in the previous section. Their root cause is the use of external HV transistors only as multiplexers that convey to the driver output the voltages V_{POS} or V_{NEG} provided by the positive and negative high-voltage generators. Thus, the V_{MEMS} there inherits the limited range and large voltage ripple of V_{POS} and V_{NEG}. The way around these shortcomings indicated in [19] was to replace the external analog multiplexer with digitally controlled amplifiers supplied by V_{POS} and V_{NEG}, implemented by other ASICs. But that approach yielded two-ASIC solutions, outside the requirements set here.

2.2. The Proposed Topology. Figure 1 shows the topology of the multipurpose driver for MEMS devices envisaged here, able to meet all requirements set in Section 2.1. The high-value positive and negative voltages, V_{POS} and V_{NEG}, provided by the respective generators, are not applied directly to the MEMS device; instead, they feed two linear voltage regulators which provide stable, precisely controlled voltage levels for V_{MEMS}, with low ripple. The ASIC comprises most of the required circuitry, so that only the power stages of the positive and negative voltage generators—depicted in Figure 1 by dashed-line and dotted-line rectangles, respectively—and the pass transistors and the feedback network of the two linear regulators—illustrated by dash-dot rectangles—need to be implemented by external components.

One notices that no operation mode requires that both regulators are active at the same time. This means that it is possible for the regulators to share the external feedback network.

The regulators allow for a simple and effective implementation of the required four modes of operation:

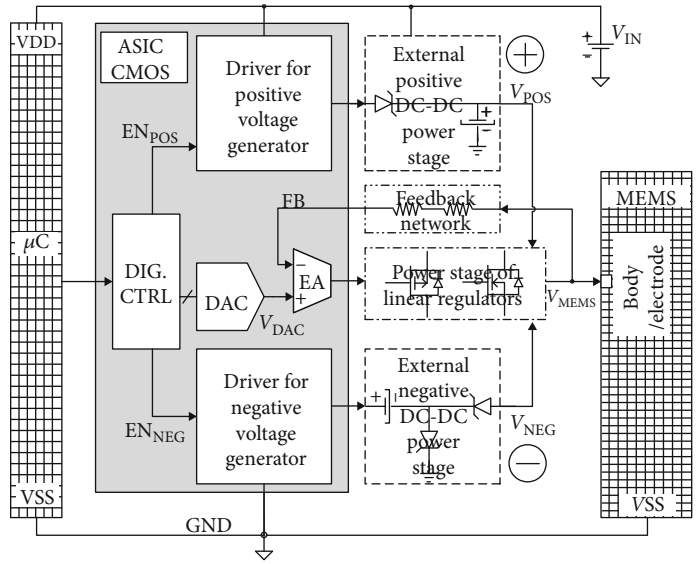

Figure 1: Proposed topology for a multipurpose driver for MEMS sensors and actuators, based on one ASIC implemented in a low-cost HV CMOS technology, without a triple well.

(1) Changing the polarity of V_{MEMS} can be achieved by simply turning on the voltage regulator that corresponds to the wanted polarity while turning off the other regulator, so that it presents a high output impedance

(2) The driver output can be left floating by disabling both regulators and by disconnecting the feedback network

(3) The driver output can be shorted to ground by turning off both regulators and by connecting the feedback network to the GND line

Another advantage of this topology is that accurate values for voltages V_{POS} and V_{NEG} are not required. Thus, the switched-mode voltage generators which provide them can be simpler than those in [19].

The ASIC shown in Figure 1 within the shadowed rectangle is to be implemented in a CMOS technology without a triple well, so it cannot handle negative voltage levels at its pins. Therefore, it comprises only the drivers for the positive and negative voltage generators that provide V_{POS} and V_{NEG}. The EA that handles V_{NEG} can be integrated, as well, if set to operate in the inverting configuration. The ASIC also comprises a DAC and support and auxiliary circuitry such as a reference voltage and biasing and a digital interface that takes in signals from the microcontroller—denoted as μC in Figure 1—and provides digital controls to the entire ASIC.

The microcontroller enables the driver and sets its operating mode; also, it programs the actual values of V_{MEMS} via a control word applied to the DAC driver. The entire system is supplied from the low-voltage supply V_{IN}, referenced to the GND line, common to the μC and the driver and the MEMS device.

3. The Single-ASIC Multipurpose MEMS Driver with External Open-Loop Charge Pumps

3.1. The Block Diagram and Functional Description. Figure 2 presents the first solution proposed here for implementing the driver depicted in Figure 1. It consists of an CMOS ASIC, highlighted by the shadowed rectangle in the center and three external sections:

(i) The output stage of a Dickson charge pump—encompassed by the dashed-line rectangle in the top-right corner—and the inverting charge pump within the dotted-line rectangle in the bottom-right corner that generates the main positive and negative voltages, V_{POS} and V_{NEG}, respectively. V_{POS} drives the high-voltage supply line of the ASIC, V_{DDH}

(ii) The pass transistors, M_P and M_N, of the two linear regulators and the feedback network that they share, R_{FB1} and R_{FB2}, encompassed by the dash-dot rectangle

The μC that controls the driver is also shown in Figure 2, as well as a simple model for the MEMS device: an $R_M \| C_M$ network in series with an alternative-current voltage source V_{OPEN}. The source V_{OPEN} allows us to demonstrate the implementation of the "OPEN" operation mode, when the driver output should be left floating.

The main blocks integrated within the HV CMOS *ASIC1* delimited by the shadowed rectangle in Figure 2 are as follows:

(i) The block denoted as "Driver POS" includes the power switches and the drivers that provide the switching phases CX1 and CX2 to the Dickson

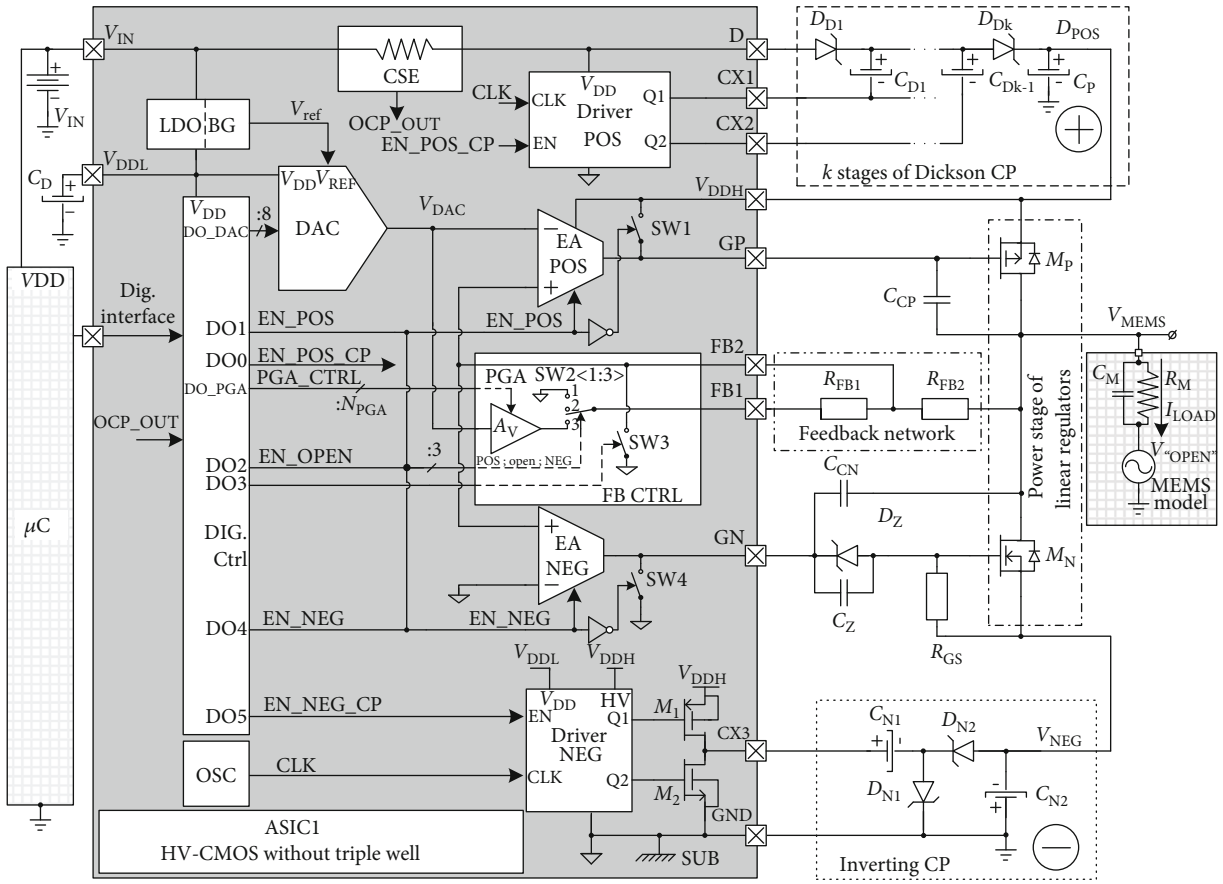

Figure 2: Proposed multipurpose driver for MEMS devices, with the main voltage generator implemented by a Dickson charge pump. It uses one ASIC implemented in low-cost HV CMOS, with the block diagram encompassed by the shadowed rectangle. The three external sections are indicated by the same types of rectangles used in Figure 1: dashed-line and dotted line for the power stages of the V_{POS} and V_{NEG} generators and dash-dot line for the M_P and M_N pass transistors of the LDOs and their common feedback network.

charge pump. Note that the Dickson charge pump operates without a control loop

(ii) The block denoted as "Driver NEG" includes the power switches and the drivers that provides the switching phases CX3 for the inverting charge pump (ICP). This charge pump operates without a control loop, as well

(iii) A digital-to-analog converter (DAC) that provides a programmable control voltage, V_{DAC}, to both voltage regulators, thus setting the value of V_{MEMS} in both POS and NEG operating modes

(iv) The error amplifiers for the positive and negative voltage regulators, EA_POS and EA_NEG, which drive the gates of the external PMOS and NMOS pass transistors, M_P and M_N, respectively

(v) The feedback control block—denoted as "FB_CTRL" in Figure 2—comprises switches SW2 and SW3 and a programmable gain amplifier (PGA). The switches connect the chip side terminals of the external feedback network, R_{FB1} and R_{FB2}, to specific levels, depending on the wanted operation mode as follows:

(1) *"POS" mode*: only the EA_POS is enabled and set to work in a noninverting configuration, with the input voltage V_{DAC}. SW3 is turned *off*, while SW2 connects the FB1 terminal of the feedback network to GND:

$$V_{MEMS} = \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \cdot V_{DAC} \quad (1)$$

(2) *"NEG" mode*: SW3 remains *off*, but this time, the EA_NEG is enabled and set to work in an inverting configuration, with the input voltage provided by the PGA. The PGA gain is set to a larger-than-unity value, to compensate for the gain difference between the noninverting and inverting configurations. Thus, negative values are obtained for V_{MEMS}, equal in module to the ones obtained in the POS mode for the same V_{DAC}:

$$V_{MEMS} = \left(-\frac{R_{FB2}}{R_{FB1}}\right) A_{V\_PGA} \cdot V_{DAC} \quad (2)$$

Note that in both the "POS" and "NEG" modes, the voltage levels at the chip terminals FB1 and FB2 are positive, close to either V_{DAC} or the

GND level. The largest voltage that the ASIC needs to handle is V_{POS}, which is applied to pin V_{DDH}. It follows that V_{MEMS} can take values close to the maximum breakdown voltage of the CMOS process that the ASIC is integrated in.

(3) *"OPEN" mode*: both EAs are disabled, as well as the PGA; SW3 remains *off* while SW2 is set to position 2, leaving the FB1 terminal floating. When EA_POS is disabled, the switch SW1 turns *on*, pulling terminal GP to V_{DDH}, thus ensuring that the M_P pass transistor is off, too. Similarly, when EA_NEG is disabled, the terminal GN is connected to GND by the switch SW4. The Zener voltage is larger than V_{NEG}; therefore, the M_N pass transistor is off even if the inverting charge pump remains enabled. With both pass transistors turned *off* and the feedback network left open, there is no DC path between the driver output and either supply lines. However, if the output terminal is driven by an external source to negative voltage levels, the substrate diodes associated with the feedback pins get forward biased. In this case, the impedance seen between the output and the GND line is R_{FB2}. Therefore, if V_{MEMS} could drift to negative values while the driver operates in the "OPEN" mode, the value of R_{FB2} should be chosen in the range of tens or even hundreds of kΩ

(4) *"ZERO" mode*: it has the same settings as for the OPEN mode, except for SW3 which is turned *on*. Thus, resistor R_{FB2} connects the driver output to the GND line

ASIC1 also comprises the following auxiliary blocks:

(i) A bandgap reference (BG) that provides the reference voltage, V_{REF}, to the DAC and to a low dropout regulator (LDO) that ensures a constant voltage level on the internal supply line denoted as V_{DDL}. The external decoupling capacitor, C_D, connected to that line helps increase the PSRR of the internal LDO

(ii) A current sensor, denoted as CSE, which feeds the overcurrent protection of the entire driver

(iii) A digital interface that conveys instructions from the external controlling device to the block denoted as "DIG Ctrl" which provides corresponding digital controls to the entire *ASIC1*

(iv) An internal oscillator "OSC" that provides clock signals for the POS and NEG drivers

It should be noted that this topology allows the end user, the application engineer, to choose and size the external components that best suit their application.

Presenting in detail the transistor-level implementation of the proposed driver is beyond the scope of this paper, which focuses on driver topology, with only proof-of-concept circuit implementation required to validate it. Moreover, most functional blocks depicted in Figure 2 can be implemented by using well-known approaches, such as those presented in [24].

Therefore, only the blocks with particular requirements set by the proposed topology will be discussed here.

3.2. Voltage Generators for V_{POS} and V_{NEG}. The supply voltage provided by the positive and negative voltage generators must be higher than the maximum V_{MEMS} value, to provide enough headroom for the pass transistors M_P and M_N. Besides this, there is no need to control accurately the voltage levels on the V_{POS} and V_{NEG} lines. This feature allows for simpler implementations of the V_{POS} and V_{NEG} voltage generators, with unregulated outputs.

3.2.1. The Positive Voltage Generator. The positive voltage generator encompassed by the dashed-line rectangle in the top-right corner of Figure 2 was implemented by cascaded switched-capacitor Dickson cells, called the Dickson charge pump [25]. Each cell yields at its output a voltage equal to the sum of the input voltage and the peak value of the clocking signal—delivered here by the block called "Driver POS", supplied directly by V_{IN}—less the voltage drop across the cell diode, D_D. The positive voltage generator is enabled during all four modes of operation by setting the EN_POS_CP = '1' ; the V_{POS} yielded by the Dickson CP can be written as

$$V_{POS} = k_{DICKSON} \cdot (V_{IN} - V_{Dk}) \tag{3}$$

,where $k_{DICKSON}$ is the number of cells within the chain and V_{Dk} is the voltage drop across diode $D_{D,k}$. The minimum number of Dickson cells results from the condition that V_{POS} is large enough to ensure sufficient headroom to the linear regulator

$$K_{Dickson} \geq \frac{V_{MEMS}}{V_{IN} - V_{Dk}} + V_{LDO\_DROPOUT} \tag{4}$$

,where $V_{LDO\_DROPOUT}$ represents the minimum voltage drop across the pass transistor M_P necessary to keep it in saturation. Its value is usually between 100 mV and 200 mV.

A Dickson charge pump with six stages provides approximately 23.4 V on the V_{POS} line even for the minimum level of the supply voltage, 4.5 V, and for the maximum load current, 2 mA.

3.2.2. The Negative Voltage Generator. The negative voltage V_{NEG} is provided by the inverting charge pump (ICP) encompassed by the dotted-line rectangle in the bottom-right corner of Figure 2. The ICP is supplied by the V_{POS} line, fed by the Dickson charge pump back to the ASIC through the pin V_{DDH}. Thus, the maximum negative voltage that the ICP can generate at its output is

$$V_{NEG} = -V_{POS} + V_{DN1} + V_{DN2} \tag{5}$$

,where $V_{DN1,2}$ are the forward voltages of the external diodes, D_{N1} and D_{N2}. It follows that the minimum value of V_{POS} should be set considering equation (5) and the minimum

drop voltage on the pass transistor M_N. In our case, V_{POS} is close to 25 V so the value of V_{NEG} gets over 23 V, a level more than sufficient for the negative voltage regulator.

The internal oscillator "OSC" provides the clock signal CLK to the "Driver NEG" block, which drives the gates of complementary switches M_1 and M_2. These switches are active as long as the control EN_NEG_CP is high; thus, the charge is transferred from the V_{DDH} supply line to V_{NEG}, via the external ICP components $C_{N1} - C_{N2}$ and $D_{N1} - D_{N2}$.

The voltage generators, V_{POS} and V_{NEG}, are not conveyed directly to the driver output but used to supply linear voltage regulators described in the following sections.

3.3. Positive and Negative Voltage Regulators

3.3.1. Positive Voltage Regulator LDO_POS. Figure 3 details the schematic of the positive voltage regulator, called here as LDO_POS. The pass transistor M_P and the feedback networks R_{FB1} and R_{FB2} are external, while the error amplifier EA_POS is integrated within *ASIC1*. It is activated during the POS mode, to provide precisely controlled voltage levels for V_{MEMS}, with low ripple.

The value of V_{MEMS} is set by V_{DAC}, as indicated in equation (6). As the DAC output voltage range is [0 V, 2 V], the ratio R_{FB2}/R_{FB1} was set to 9:

$$\left.\begin{aligned} k_P &= \frac{R_{FB2}}{R_{FB1}} = 9 \\ V_{DAC} &\in [0\,\text{V}, 2\,\text{V}] \end{aligned}\right\} \Rightarrow \begin{cases} V_{MEMS} = 10 \cdot V_{DAC} \\ V_{MEMS} \in [0\,\text{V}, +20\,\text{V}] \end{cases} \quad (6)$$

Note that the output voltage range is not limited by the topology. In fact, an 8-bit DAC can provide a voltage level up to $256 \times V_{LSB}$, which translates into $V_{MEMS} = 25.6$ V for a 100 mV output referred as V_{LSB}. However, the V_{MEMS} is limited by the maximum voltage that the CMOS process can handle—which is 50 V in this case—and by the maximum drain-to-source voltage that the external pass transistor, M_P, can withstand:

$$V_{DSmax\_M_P} > V_{POS} - V_{NEG} \quad (7)$$

Therefore, this circuit can be used to supply larger V_{MEMS} values by simply choosing a suitable external transistor and by resizing the feedback network. A Dickson charge pump with a larger voltage gain needs to be used as well. This is the reason that the frequency compensation was implemented by the external capacitor C_{CP}: the user can adjust its value for optimum overall performance, considering the other external components and the capacitive load presented by the MEMS device.

Besides stability and precision, the LDO_POS should have a good power supply rejection over a wide frequency range, including the switching frequency. For this, the folded cascode transconductor presented in Figure 3 within the dotted-line rectangle was chosen to implement the positive error amplifier, EA_POS.

The LDO_POS is disabled by pulling down the control EN_POS. Then, the switch M_{SW1} pulls the gate of transistor M_P up to V_{POS}, turning off the transistor. The drain-extended HV transistors available in this process withstand drain-source voltages of up to 50 V, but no more than 7 V of gate-source voltage. Therefore, the digital control EN_POS is applied to the gate of M_{SW1} through a level-shifter block (LVS). Besides the switch, only transistors M_0, M_7, and M_8 have to handle large drain-source voltages; therefore, smaller and faster low-voltage transistors can be used to implement most of the signal path in Figure 3.

3.3.2. Negative Voltage Regulator LDO_NEG. Figure 4 presents the schematic of the negative voltage regulator, called here as LDO_NEG. There are some similarities with the LDO_POS described on the previous section: the pass transistor M_N and the feedback networks R_{FB1} and R_{FB2} are external, while the error amplifier EA_NEG is integrated within *ASIC1*. The feedback resistors are, in fact, precisely the same one used by LDO_POS. Also, the frequency compensation is implemented by the external capacitor C_{CN}; the user can set the C_{CN} value considering the other external components and the capacitive load of the LDO. Finally, a similar folded cascode topology was used for the error amplifier. However, the signal current mirror at the EA_NEG output is implemented on the low side of the cascode stage—thus with NMOS transistors. This helps reduce the systematic offset of the LDO_NEG.

There are more important differences between LDO_POS and LDO_NEG: the error amplifier operates as an inverting summing amplifier, with the inverting input (−) connected directly to the GND line, while the noninverting input (+) was connected to the midpoint of two series resistors placed between V_{NEG} and a positive voltage reference provided by the PGA at the FB1 pin. This way, the error amplifier and M_N pass transistor are enclosed in a negative feedback loop that will force equal potential at the error amplifier inputs. Thus, the voltage at feedback pin FB2 is forced to the GND potential, preventing the large negative voltage V_{MEMS} to drag the pin voltage below zero. Now, the value of V_{MEMS} is set by V_{DAC} and A_{V_PGA} as indicated in equation (2). However, the negative V_{MEMS} value provided by LDO_NEG can be made equal in module to the positive V_{MEMS} yielded by the LDO_POS for the same V_{DAC} by setting the PGA gain appropriately:

$$A_{V\_PGA} \cdot \frac{R_{FB2}}{R_{FB1}} = \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \Rightarrow A_{V\_PGA} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad (8)$$

The DAC output voltage range is [0 V, 2 V]; therefore, the ratio R_{FB2}/R_{FB1} was set to 9:

$$\left.\begin{aligned} A_{V\_PGA} &\cong 1.111 \\ V_{DAC} &\in [0\,\text{V}, 2\,\text{V}] \end{aligned}\right\} \Rightarrow \begin{cases} V_{MEMS} \cong -10 \cdot V_{DAC} \\ V_{MEMS} \in [-20\,\text{V}, 0\,\text{V}] \end{cases} \quad (9)$$

A fixed-gain amplifier is enough to meet the requirements set here. However, a PGA was integrated in order to

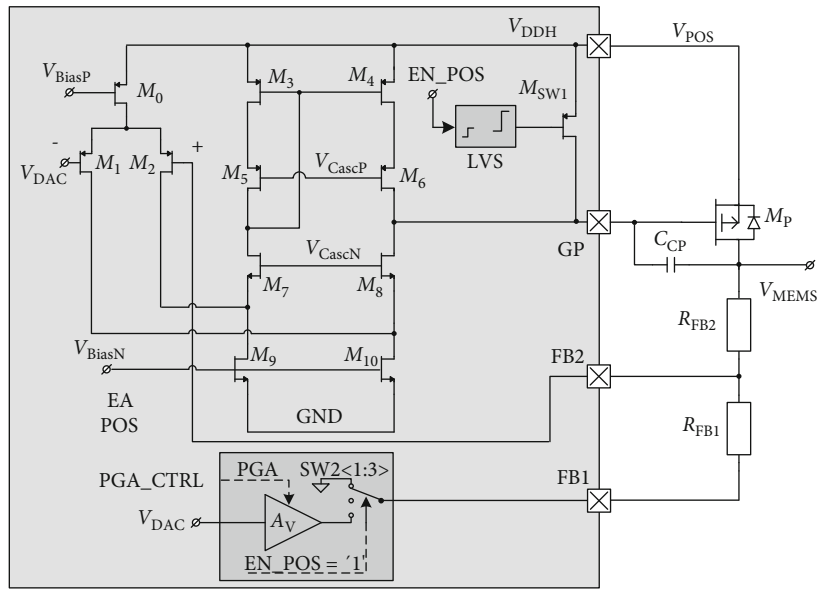

Figure 3: Schematic of the positive voltage regulator. The error amplifier depicted within the shadowed rectangle corresponds to the block EA_POS within *ASIC1* shown in Figure 2.

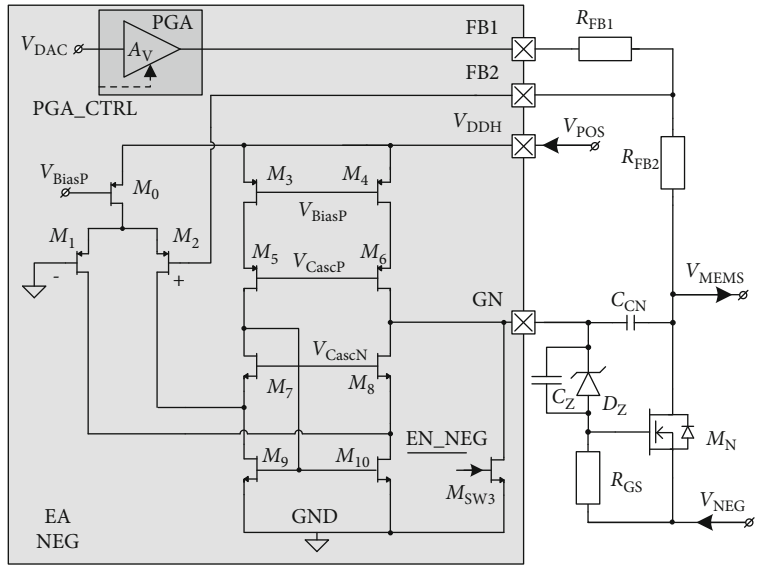

Figure 4: Schematic of the negative LDO. The error amplifier integrated in *ASIC1* that it depicted within the shadowed rectangle. It corresponds to EA_NEG in Figure 2.

allow the user to obtain symmetrical V_{MEMS} values irrespective of the output voltage range. To change the V_{MEMS} range the user only needs to resize the external feedback network and the pass transistors, then to set the PGA gain to the value indicated in equation (8).

The substrate of *ASIC1* is connected to the common GND line, so a negative voltage applied to the pins would result in the forward biasing of the intrinsic bulk diode. This is avoided by employing the inverting error amplifier EA_NEG shown in Figure 4: although the feedback networks R_{FB1} and R_{FB2} is connected to V_{MEMS}—which takes negative values in this case—the potentials at pins FB1 and FB2 never drop below GND:

$$V_{FB1} = V_{DAC} \cdot A_{V\_PGA}$$
$$V_{FB2} = \text{GND} \tag{10}$$

Another key difference is the presence of the external Zener diode D_Z: it ensures that the voltage on the ASIC pin GN is shifted up from the gate of M_N, which can go to voltage levels as low as V_{NEG}. Therefore, the breakdown voltage of

the Zener diode (BV_{D_z}) must be higher than the maximum absolute voltage of V_{NEG}:

$$BV_{D_z} \geq |V_{NEG}| \quad (11)$$

Equation (5) shows that the negative voltage rail V_{NEG} depends on the value of V_{POS} that in turns depends on the value of V_{IN}. The input voltage range is 5 V ± 10% and the forward voltage of the external diodes is approximately 0.6 V. It follows that the positive output voltage, V_{POS}, can take values between 23.4 V and 29.4 V, while the negative output voltage range is slightly narrower, $V_{NEG} \in [-22.2\,V, -28.2\,V]$.

A gate-to-source resistor R_{GS} is required to ensure a DC path for the bias current of the Zener diode. It also converts the control current, provided by the EA_NEG transconductor, into a control voltage at the gate of M_N. When the LDO_NEG is disabled, this resistor shorts the gate of M_N to its source, ensuring that it is turned *off*.

A shunt capacitor, *Cz*, was placed around the Zener diode to reduce the charge injection effect due to gate-to-drain parasitic capacitance M_N and the external compensation capacitor C_{CN}. This is necessary to prevent false turning *on* of M_N that can otherwise occur when V_{MEMS} transitions from negative to positive voltage levels.

Note that the idea of using an operational amplifier (OpAmp) in the inverting configuration, to avoid handling of negative voltages within a CMOS ASIC, was also employed in [26, 27]. However, the OpAmp was used there to implement an inverting summing amplifier: the noninverting input of the OpAmp was connected directly to the GND line, while the inverting input was connected to the midpoint of two series resistors placed between V_{NEG} and a positive voltage. Therefore, the current flowing through the feedback network had to be sunk by a buffer driven by the reference voltage source. The topology proposed here, shown in Figure 2, has two important advantages over the ones presented in [26, 27]:

(1) There is no need to buffer the V_{DAC} reference, as all blocks connected to that line (EA_POS, PGA) have high input impedances and

(2) The external feedback network requires only 2 pins, instead of 4

3.4. Simulation Results. ASIC1 shown in Figure 2 was designed in a low-cost 0.18 μm HV CMOS technology, without a triple well but with drain-extended transistors able to withstand drain-source voltages of up to 50 V.

Following the approach introduced in Section 3.1, detailed simulations are presented for the entire driver, while block-level simulation results are presented for the positive and negative LDOs shown in Figures 3 and 4. The load presented to the driver by the MEMS device was modelled by an $R_M \| C_M$ network, with $R_M = 10\,k\Omega$ and $C_M = 100$ pF.

Figure 5 presents the loop gains of the positive and negative voltage regulators shown in Figures 3 and 4, respectively. The module and phase frequency characteristics were obtained for the extreme values of the output voltages: +10 V and +20 V for LDO_POS and −20 V and −10 V for LDO_NEG. The quiescent current of both error amplifiers was set to 300 μA.

Figure 6 presents the frequency characteristics of the power supply rejection (PSR) at the V_{MEMS} output of the driver, driven by the two LDOs in the POS and NEG operating modes. The markers highlight the PSR values at the switching frequency of the charge pumps, 50 kHz.

The performance of the entire driver is determined to a large extent by its external components, which are difficult to model in the Cadence Virtuoso environment used to design *ASIC1*. Therefore, LTspice was used for system-level simulations, with *ASIC1* being represented by a SPICE-compatible model and transistor level representations of the error amplifiers.

The frequency of the clock signal was set to $F_{CLK} = 50$ kHz. The external components were chosen with the aim of minimizing the ripple on the V_{MEMS} by reducing the ripple on the V_{POS} and V_{NEG} supply lines. The following values resulted for the passive components: $C_{D1} - C_{Dk-1} = 100$ nF, $C_P = 1\,\mu$F, $C_{N1} = 100$ nF, and $C_{N2} = 1\,\mu$F. All capacitor models included a 50 mΩ·s ESR. The diode RB706W-40 (double series diodes in one pack) was chosen to implement all diodes within the Dickson and the inverting charge pumps, while BZX84B27VL was for the Zener diode. The SPICE models of BSS84 and RJU002N06 were used for the pass transistors M_P and M_N. Finally, the feedback resistors R_{FB2} and R_{FB1} were set to 180 kΩ and 20 kΩ, according to equation (6). The output ripple was reduced by using Schottky diodes with low parasitic capacitance (4 pF) and large ESR (10 Ω) and MOS transistors with low gate-source capacitance (20 pF).

Figure 7 presents the output voltage, V_{MEMS}, when the driver operates in the "POS' and "NEG" modes. The DAC voltage is ramped up in 100 mV steps, across its full range, 0 to 2 V. The resulting V_{MEMS} varies continuously between −20 V and +20 V, as required. Also, after each DAC step, it settles well within the 2 μs limit.

Figure 8 presents the main signals within the MEMS driver shown in Figure 2, while going through all its four operation modes and the startup phase. Note that the driver was loaded by the 10 k$\Omega \| 100$ pF model of the MEMS device described before; also, the voltage source V_{OPEN} was placed is series with this model, to highlight the cases when the driver does not set the V_{MEMS} voltage.

In all system-level simulations presented here, the DC level of V_{OPEN} was set to 2 V, its amplitude to 1 V, and its frequency to 1 kHz.

The driver is powered up at the start of the simulation, in the "ZERO" mode; in 4 ms, V_{POS} and V_{NEG} reach levels large enough to allow for normal operation. After this point, the operating mode is changed at every 2 ms, to present all modes of operations and the transition between them.

At $t = 4$ ms, the driver is set to operate in the "POS" mode, with V_{DAC} set to 1 V (so the target V_{MEMS} level is 10 V). Next, at 6 ms, the driver is reconfigured for the "NEG" operating mode, while the DAC voltage is maintained at 1 V; this forces the V_{MEMS} level to drop from 10 V to −10 V,

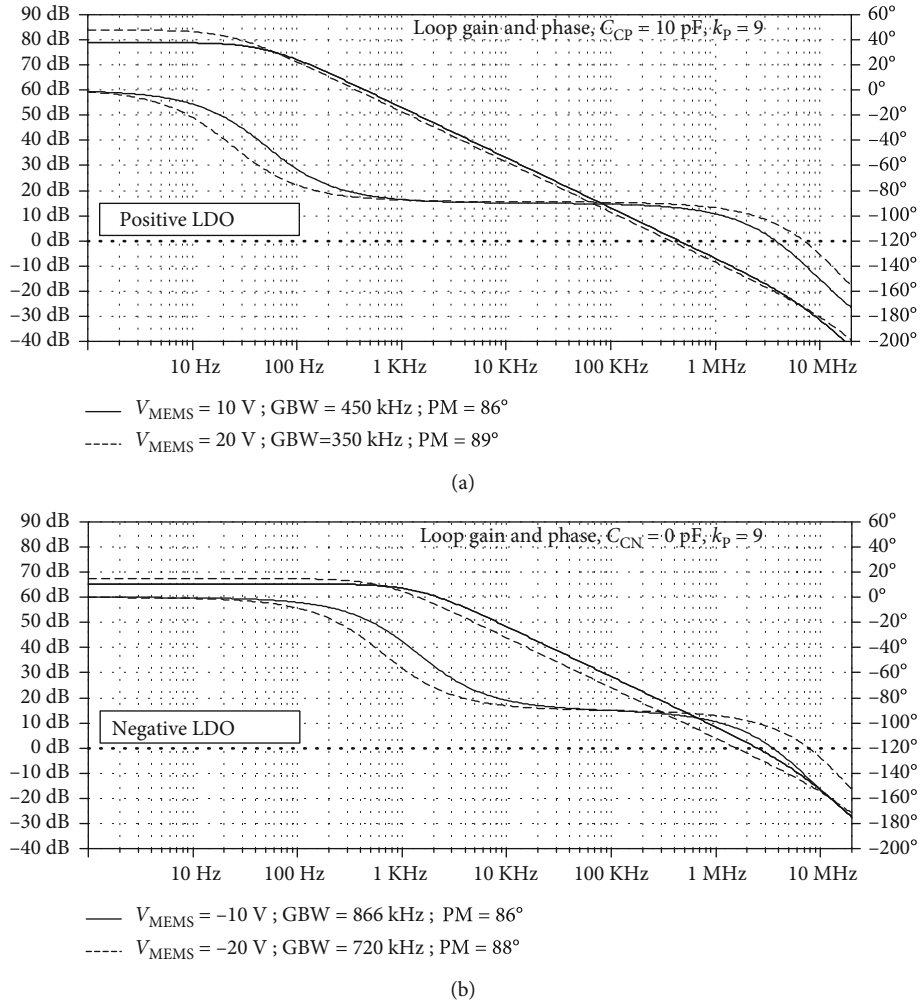

Figure 5: Loop gain frequency characteristics of the LDOs: (a) the positive LDO shown in Figure 3 and (b) the negative LDO illustrated in Figure 4.

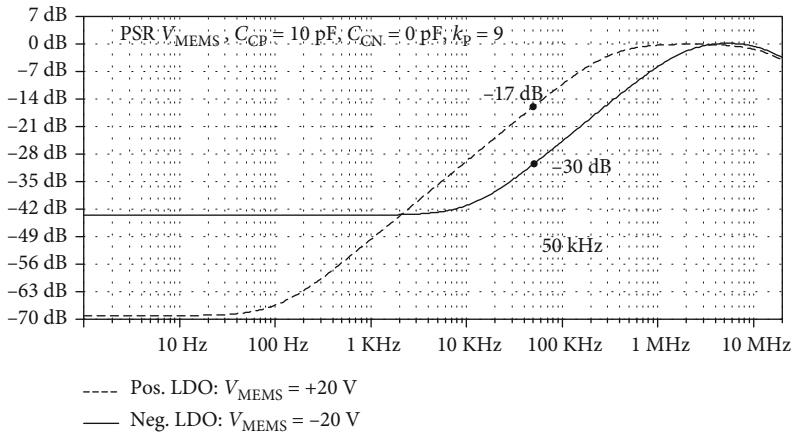

Figure 6: PSR frequency characteristics of the LDOs: dashed line: the positive LDO presented in Figure 3 and continuous line: the negative LDO shown in Figure 4.

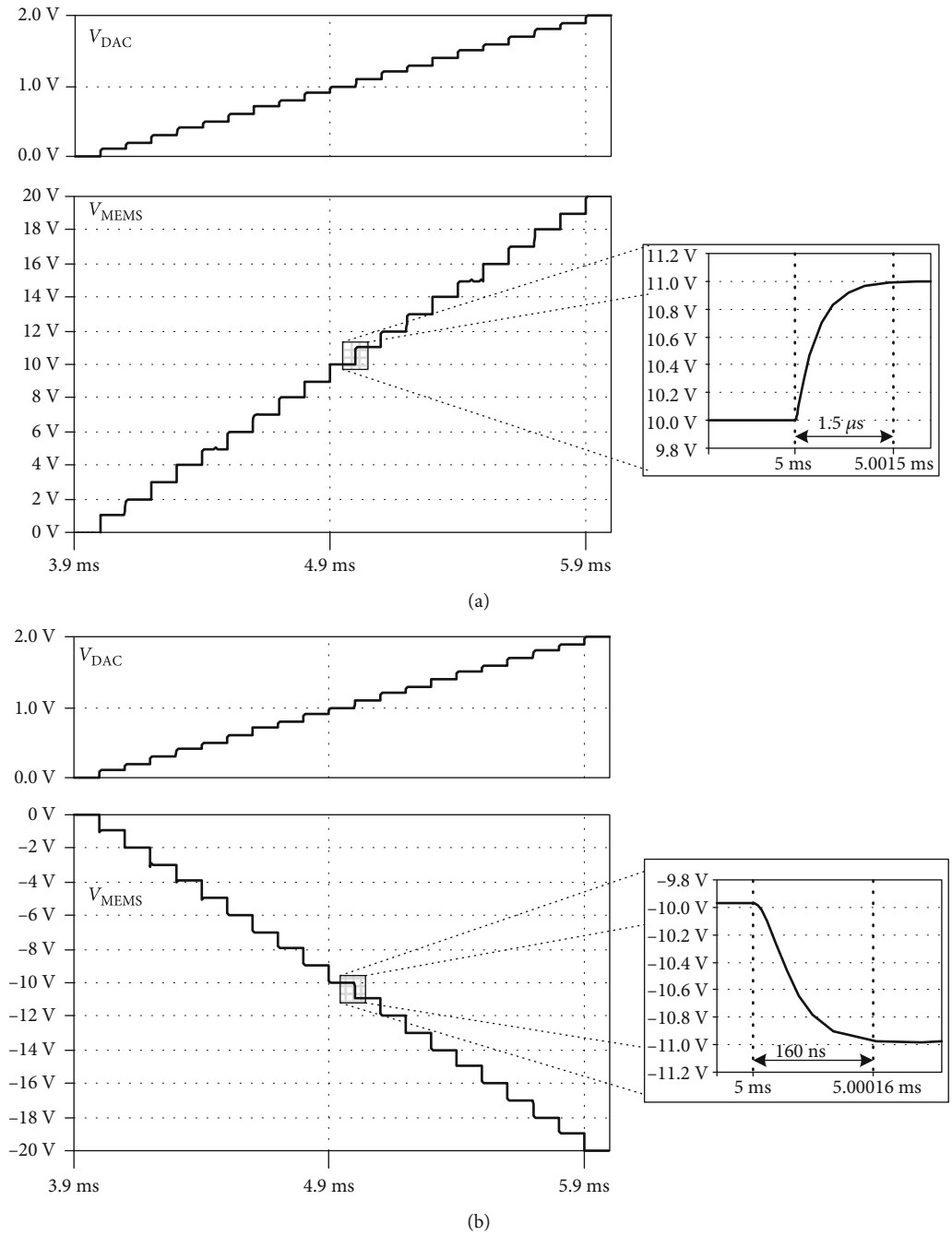

Figure 7: The driver output in the (a) "POS" operating mode and in the (b) "NEG" mode when V_{DAC} steps up by 100 mV every 100 μs, along its range, 0 to 2 V.

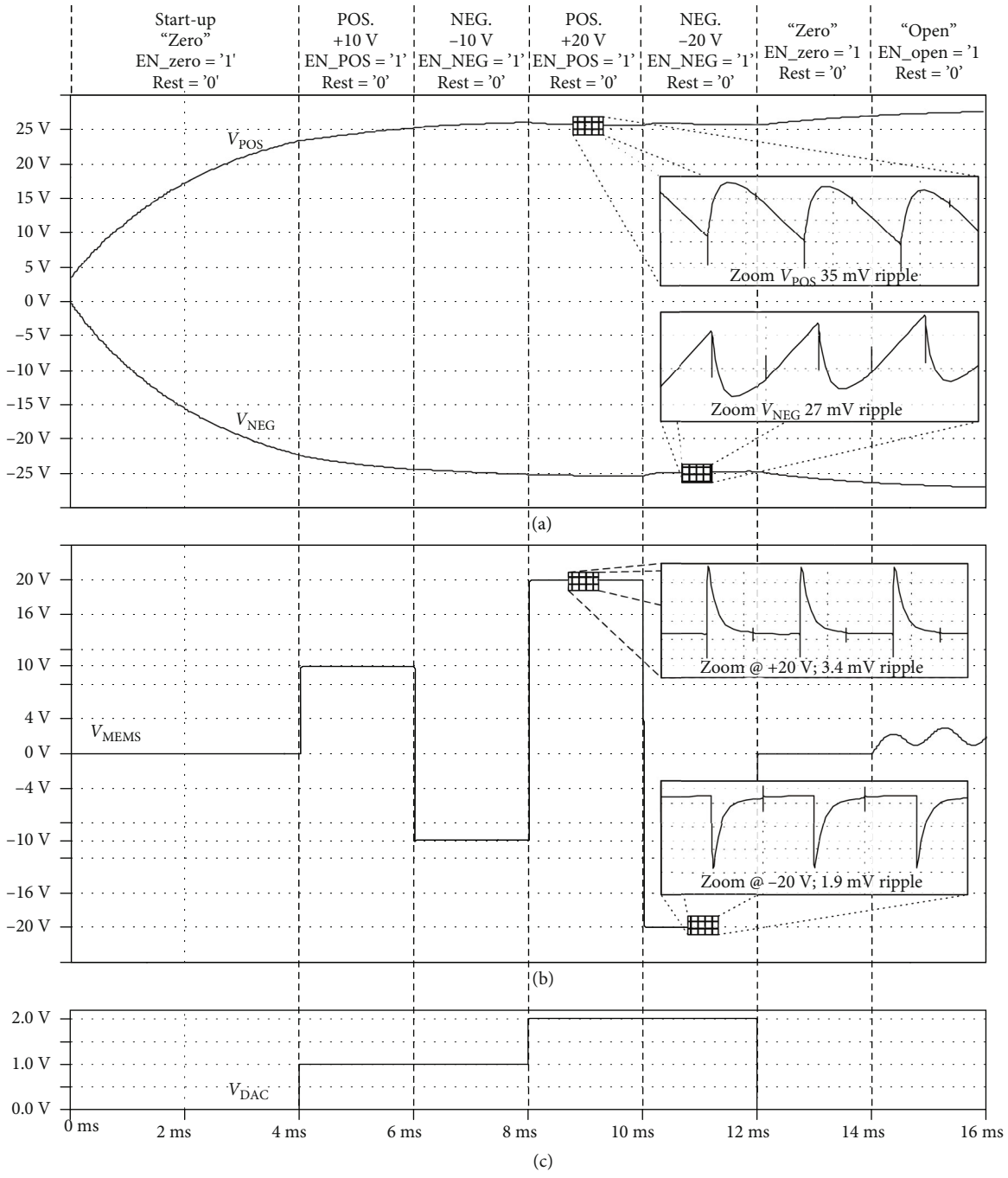

FIGURE 8: System level simulation results with *ASIC1*: (a) V_{POS} and V_{NEG} with a zoom-in view for the ripple, (b) V_{MEMS} with a zoom-in for the ripples in POS and NEG operation modes, and (c) $V_{DAC} = 0$ V, 1 V, and 2 V.

with a slope of −23 V/μs. At 8 ms, the driver is set again to the "POS" operating mode while the DAC voltage is increased to 2 V; this forces V_{MEMS} to jump from −10 V to +20 V, with a slope of 17 V/μs. At 10 ms, the driver is reconfigured for the NEG operation mode while maintaining the DAC voltage, thus forcing V_{MEMS} to drop from +20 V to −20 V.

The zoom-in views of the V_{POS}, V_{NEG}, and V_{MEMS} waveforms confirm that their voltage ripple values are relatively small: 35 mV, 27 mV, and 3.4 mV and 1.9 mV, respectively.

At 12 ms, the driver is configured in the "ZERO" operation mode, where both the positive and negative voltage regulators are turned *off* and the output voltage is quickly pulled down to ground by the feedback resistor R_{FB2}. One notices that at $t = 12$ ms, the V_{POS} and V_{NEG} voltages increase slightly. This appears because the current provided by the Dickson charge pump and ICP decreases because of load current drops in "ZERO" and "OPEN" operation modes, resulting in smaller voltage drops across the diodes.

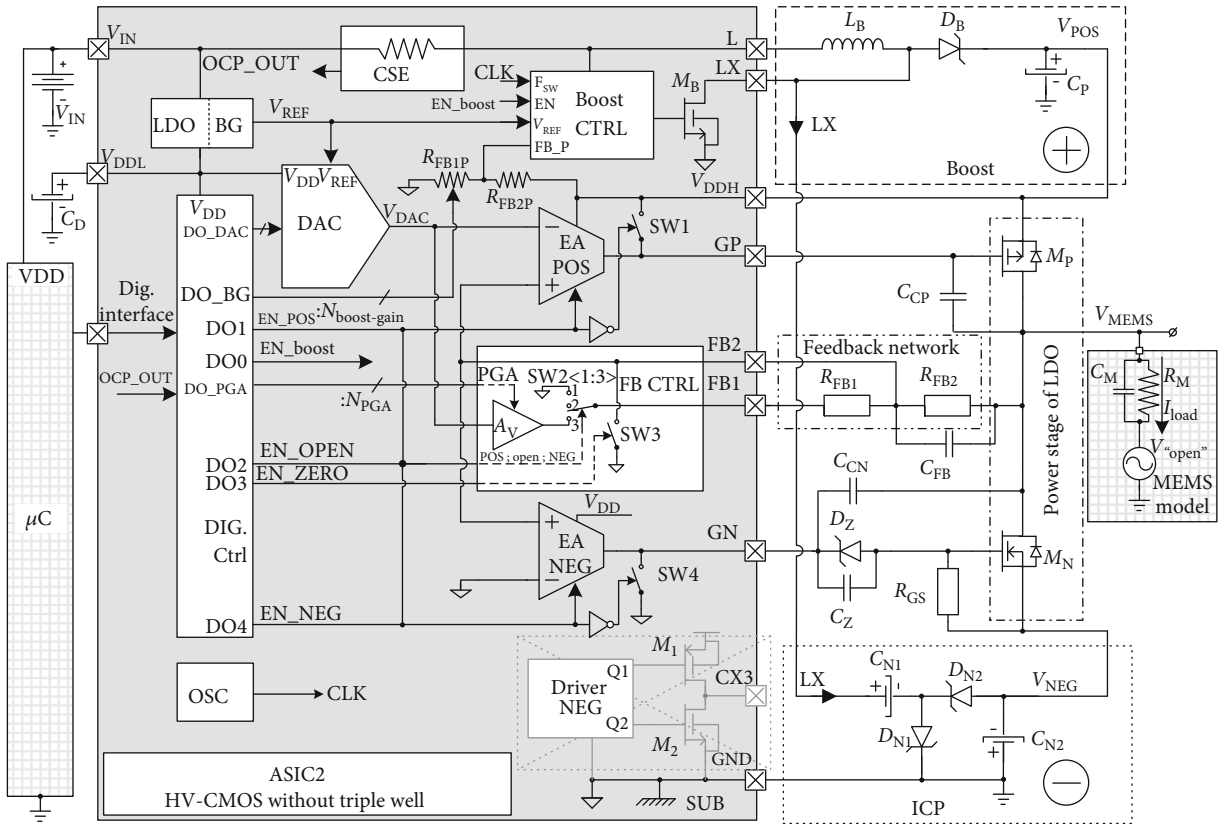

FIGURE 9: Multipurpose driver for MEMS devices based on a compact voltage generator for V_{POS} and V_{NEG}. It employs one ASIC implemented in low-voltage HV CMOS, with the block diagram depicted within the dashed-line rectangle.

Finally, at 14 ms, the driver goes into the "OPEN" operating mode, where the driver output is left floating. This state is proven by the fact that a sinusoidal voltage with a 1 V amplitude, 2 V DC level, and 1 kHz frequency appears on V_{MEMS}, which is precisely the voltage provided by the external source V_{OPEN}.

It should be noted that the transition times between operating modes are very small, in the order of a few μs.

4. The Single-ASIC Multipurpose MEMS Driver with a Compact External Boost Converter and Inverting Charge Pump

4.1. Description of the Proposed System. Figure 9 presents the second solution proposed here for implementing the driver depicted in Figure 1. The aim was to reduce the BOM and to improve the power efficiency, while increasing the range of the V_{MEMS} voltage. The two main ideas for achieving it were (i) to implement the positive voltage generator by using an inductor-based boost converter instead of the Dickson charge pump and (ii) to use one integrated power switching transistor, M_B, for both the boost converter and the inverting charge pump that implement the negative voltage generator. These ideas eliminate the multiple-stage external Dickson charge pump and the integrated ICP driver, thus reducing the BOM. Also, they allow for a simpler ASIC and improve the power efficiency of the driver.

The block diagram of the ASIC required by this solution is presented in Figure 9 within the dashed-line rectangle. It is very similar to the *ASIC1* block diagram shown in Figure 2, except for the Driver_POS and Driver_NEG blocks: the former is replaced by Boost_CTRL block and the power switch, M_B, while the latter is no longer necessary. It will be called hereafter *ASIC2*, to distinguish it from *ASIC1*.

Besides these changes, the driver shown in Figure 9 is quite similar to, and has the same modes of operation as, the driver described in Section 3.1. Therefore, equations (1), (2), (7)–(10) are valid for this driver, as well.

A hysteretic/burst control similar with the one presented in [19] was used for the boost converter, as it provides good efficiency at light loads. The power switch, M_B, also serves as the switching transistor for the inverting charge pump, ICP. This arrangement is somewhat similar to the solution proposed in [28], but we took full advantage of the fact that here, V_{NEG} needs not to be set to a precise value; it only needs to track V_{POS}. The ICP does not have its own voltage control loop; therefore, the switches M_{n1} and M_{n2} from [28] were replaced by M_B and D_{N1}, respectively. This way, C_{N1} is charged through the diode D_{N1} and the difference between the resulting absolute values of V_{NEG} and V_{POS} are automatically maintained within the voltage drop across a forward-biased diode. Similar to the driver shown in Figure 2, the supply voltage provided by the positive and negative voltage generators must be higher than the maximum V_{MEMS} value and they do not need to be precisely controlled. However, the

voltage generators shown in Figure 9 can generate more efficiently large voltage levels. The maximum V_{POS} level is limited only by the breakdown voltage (BV) of the HV CMOS process that *ASIC2* is implemented in and the voltage capability of the external transistors.

This compact and power-efficient implementation of the positive and negative voltage generators comes at a price: larger voltage ripple on both V_{POS} and V_{NEG}. This means that the positive and negative voltage regulators should have better PSR than those described in Section 3 to maintain a reduced level of ripple.

4.2. Circuit Implementation. This section is the *ASIC2* counterpart of Section 3.2 and Section 3.3: it details the circuit-level implementation of the voltage generators and the linear voltage regulators.

4.2.1. The Positive Voltage Generator: a Boost DC-DC Converter with Hysteretic/Burst Control. Figure 10 presents the inductor-based boost DC-DC converter with hysteretic control that implements the positive voltage generator. A fixed frequency clock drives the burst logic block that controls the gate of the power switch, M_B. The clock is passed on to the M_B gate only when the comparator output, V_{COMP}, goes high. The hysteresis comparator takes in a fraction of the V_{POS} output voltage and compares it with the reference voltage V_{REF}.

As a result, the output voltage will toggle between two levels, set by the trip points of the comparator amplified by the gain of the feedback network, $1 + R_{FB2P}/R_{FB1P}$.

The V_{POS} output voltage provided by this boost converter has the following expression:

$$V_{POS} = \left(1 + \frac{R_{FB2P}}{R_{FB1P}}\right) \cdot (V_{REF} \pm V_{HYST})$$

$$V_{POS\_average} = (1 + k_B) \cdot V_{REF}, \quad k_B = \frac{R_{FB2P}}{R_{FB1P}} \tag{12}$$

,where the factor k_B is the ratio of the feedback resistors.

The voltage ripple at the output of the converter is

$$V_{POS\_ripple\_pkpk} = (1 + k_B) \cdot V_{HYST} \tag{13}$$

,where V_{HYST} is the hysteresis width of the comparator.

A detailed description of this type of boost converter can be found in [19].

As discussed in the previous section, the power switch M_B also drives the ICP that yields the negative voltage:

$$V_{NEG\_average} = -V_{POS\_average} + V_{D_{N1}} + V_{D_{N2}} - V_{D_B}$$
$$V_{NEG\_average} \cong -V_{POS\_average} + V_{DN2} \tag{14}$$

Thus, the value of V_{NEG} closely follows the V_{POS} voltage—the only difference is the voltage drop V_D across the transfer diode D_{N2} within the ICP. Therefore, the ICP does not need an own voltage control loop.

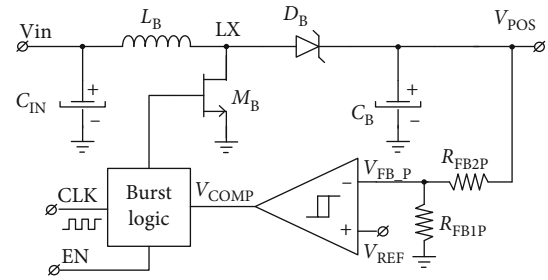

Figure 10: Block diagram of the positive voltage generator: a boost DC-DC converter with hysteretic burst control, similar to [19].

Equations (11) and (12) indicate that, if the factor k_B is made programmable, the values of V_{POS} and V_{NEG} can be easily pushed up to the maximum voltage that *ASIC2* can handle at pins V_{DDH} and LX. The HV low-cost CMOS process used here has a maximum 50 V operating voltage. The resulted maximum V_{POS} value that the driver here should provide is

$$V_{POS\_MAX} = V_{HV\_CMOS\_MAX} - V_{D_{BOOST}} \cong 49\,V \tag{15}$$

Considering the minimum voltage drop across the pass transistors M_P and M_N of the positive and negative LDOs, $V_{LDO\_DROP\_MIN}$, the maximum regulated voltage that this driver can provide for V_{MEMS} results as follows:

$$V_{MEMS\_MAX} = V_{POS\_MAX} - V_{LDO\_DROP\_MAX} \cong 48.8\,V \tag{16}$$

Besides adjusting the value of k_B, one needs to choose appropriately the external components, as well.

For example, by setting $k_B = 18.2$ and $V_{REF} = 2.5$ V and assuming a nominal value for V_{FD}, 0.6 V, one obtains

$$V_{POS\_average} = 48\,V$$
$$V_{NEG\_average} = -47.4\,V \tag{17}$$

But the V_{POS} voltage ripple takes rather large values, as well: for $k_B = 18.2$ and $V_{HYST} = 6$ mV, equation (12) yields a value of 115 mVpkpk, almost three times larger than the ripple seen in Figure 8. The ripple on the positive rail V_{POS} is conveyed to the negative rail, V_{NEG}.

One also notices that the ripple generated by the charge pump used by the first proposed driver, shown in Figure 8(a), has a rectified sinus shape. This yields a cleaner spectrum (fewer harmonics and with smaller amplitudes) than the typical saw tooth-shaped ripple generated by a boost DC-DC converter. Therefore, in this case, the LDOs should provide a far better PSR than the ones shown in Figure 6, especially at high frequency.

4.2.2. Positive and Negative LDOs. It is somewhat similar to the one shown in Figure 3, but three important changes were introduced to improve its PSR:

(1) The C_{FB} capacitor was placed in parallel with the feedback resistor R_{FB2}. This compensation technique

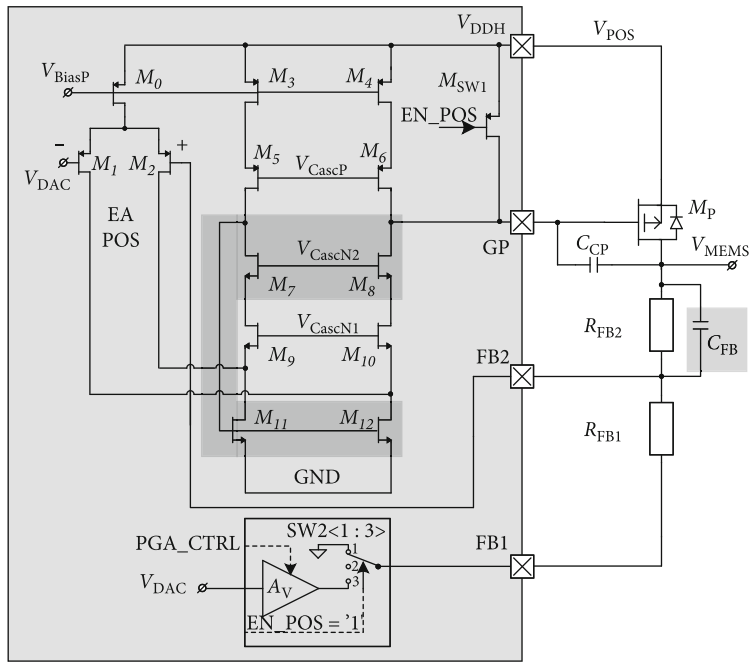

FIGURE 11: Schematic of the positive LDO. Differences with respect to Figure 3 are highlighted in gray: C_{FB} in parallel with R_{FB2}; NMOS signal current mirror, $M_{11} - M_{12}$, with a second level of NMOS cascodes, $M_7 - M_8$. The same error amplifier was used for the negative LDO.

impacts significantly the LDO PSR and stability [29]. The C_{FB} introduces a zero and a pole into the LDO loop gain frequency characteristics. Usually, the additional zero is placed near the unity-gain frequency in order to improve the LDO phase margin. Here, the Miller frequency compensation introduced by C_{CP} is sufficient to ensure stability. Therefore, the zero introduced by C_{FB} is placed below the switching frequency, to boost the loop gain value at the frequency where a large PSR is needed the most. Moreover, at higher frequencies, R_{FB2} is effectively shorted by C_{FB}, so the closed-loop gain of the LDO decreases dramatically and so does the noise gain

(2) The signal current mirror at the EA_POS output is implemented on the low side of the cascode stage, by the NMOS transistors $M_9 - M_{10}$. This helps improve the PSR, but a large systematic offset could appear if the cascodes $M_{11} - M_{12}$ ended up having very different drain to source V_{DS} voltages

(3) This was prevented by introducing a second level of cascodes, implemented by transistors M_7 and M_8

Figure 11 presents the schematic of the modified positive LDO proposed for the driver shown in Figure 9.

Similar with the first proposal, the value of V_{MEMS} is set by V_{DAC}, as indicated in equation (18). As the DAC output voltage range is [0 V, 2.25 V], the ratio R_{FB2}/R_{FB1} was set to 19:

$$\left.\begin{aligned} k_P &= \frac{R_{FB2}}{R_{FB1}} = 19 \\ V_{DAC} &\in [0\,V, 2.25\,V] \end{aligned}\right\} \Rightarrow \begin{cases} V_{MEMS} = 20 \cdot V_{DAC} \\ V_{MEMS} \in [0\,V, +45\,V] \end{cases} \quad (18)$$

4.3. Simulation Results. *ASIC2* depicted in Figure 9 was designed in the same low-cost HV CMOS technology used to validate the *ASIC1* proposal, described in Section 3. Furthermore, it was designed to meet the same set of requirements—detailed in Section 2.1—except for the V_{MEMS} range. This time, the upper limit of V_{MEMS} was pushed close to the process limit of 50 V and the range was enlarged: [−45 V to 0 V] for negative values and [0 V to +45 V] for positive values of V_{MEMS}. The switching frequency was set to 50 kHz, as before.

The hysteresis of the comparator shown in Figure 10 was set to $V_{HYST} = 6$ mV and the external feedback resistors R_{FB2} and R_{FB1} were set to 380 kΩ and 20 kΩ, for a feedback gain k_P of 19. The external components of the boost converter and the ICP were chosen with the aim of minimizing the ripples on V_{POS} and V_{NEG}: $L_B = 60\,\mu$H, $C_B = 2\,\mu$F, D_B = BAT54, $C_{N1} = 1\,\mu$F, $C_{N2} = 1\,\mu$F. The diodes RB706W-40 were used for the ICP and 1N5371B 60 V for the Zener, while transistors BSS145 and QS8M51_P, able to handle V_{DS} voltages of up to 100 V, were chosen to implement M_P and M_N.

For a direct comparison, this section presents results yielded by the *ASIC2* solution for the same set of simulations, run under the same conditions, as those presented in Section 3.4 for the solution based on *ASIC1*. The MEMS bias terminal was modeled by an $R_M \| C_M$ network, with $R_M = 22.5$ kΩ and $C_M = 100$ pF, so that the load current had the same value as in the simulations shown in Section 3, 2 mA. The models of all external capacitors included a 50 mΩ ESR. This allows for a fair and direct comparison between the two proposals.

Figure 12 presents the loop gains of the positive and negative voltage regulators designed for this proposal.

Both use the error amplifier shown in Figure 11, which was sized for the same quiescent current used by the first proposal, 300 μA. The module and phase frequency

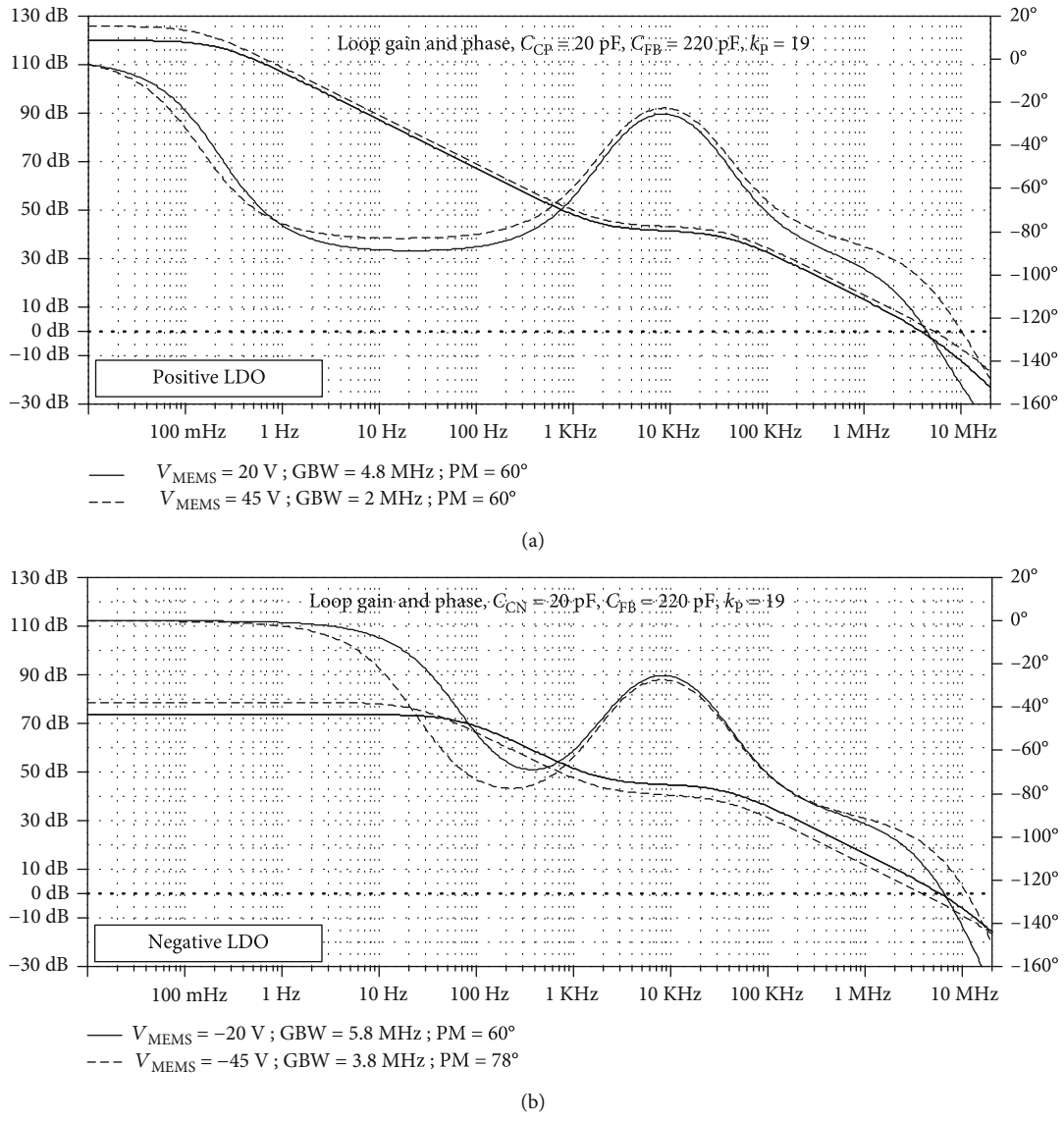

Figure 12: Loop gain frequency characteristics for the (a) positive LDO illustrated in Figure 11 and (b) the negative LDO with the improvements from positive LDO.

characteristics were obtained for the mid and extreme values of the output voltages: +20 V and +45 V for LDO_POS and −45 V and −20 V for LDO_NEG. One notices the gain boost caused by the zero introduced by placing the capacitor $C_{FB} = 220$ pF, in parallel with the feedback resistor R_{FB2}.

By comparing these results with the ones shown in Figure 5, one concludes that the unity-gain frequency, denoted as GBW in Figure 12, was increased by almost a full decade, from 350–850 kHz to 2–5.8 MHz. The phase margin decreased but remained above 60°, ensuring that both LDOs are stable.

Stability will be further verified by analyzing the LDO transient responses to changes caused by switching between operation modes.

Figure 13 presents the frequency characteristics of the PSR at the V_{MEMS} output of the driver, driven by the two LDOs in the "POS" and "NEG" operating modes.

The markers highlight the PSR values at the switching frequency, 50 kHz. They are far better than those for the LDOs described in Section 3.3: −32 dB instead of −17 dB read from Figure 6 for LDO_POS and −36 dB instead of −30 dB, for LDO_NEG.

Figure 14 presents the main waveforms within the MEMS driver shown in Figure 9, while going through a test scenario identical—except for the target V_{MEMS} levels—to the one presented in Section 3.4 (see Figure 8):

(i) The driver is powered up at the start of the simulation, in the "ZERO" mode; voltages V_{POS} and V_{NEG} increase rapidly, reaching levels large enough to allow for normal operation by $t = 4$ ms

(ii) At $t = 4$ ms, the operating mode is set to "POS" while the DAC voltage is set to 1 V, thus setting the target for V_{MEMS} to 20 V (see Figures 14(b) and 14(c))

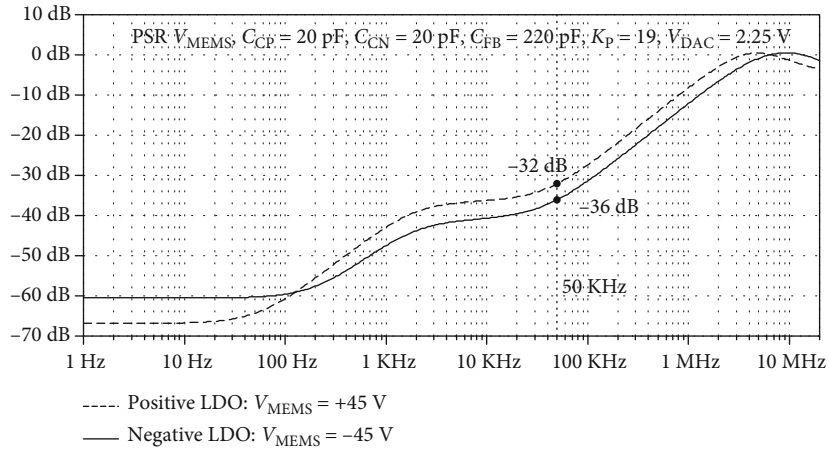

Figure 13: PSR characteristics for both LDOs implemented with EA from Figure 11: dotted line for the LDO_POS; continuous line for the LDO_NEG.

(iii) At $t = 6$ ms, the operating mode is set to "NEG", while maintaining $V_{DAC} = 1$ V; therefore, the target for V_{MEMS} is −20 V

(iv) The operating mode is changed at every 2 ms and the V_{DAC} at every 4 ms: at $t = 8$ ms, it goes up to 2.25 V and then drops back to 0 V at $t = 12$ ms. This way, the driver goes through all modes of operations. In the "POS" and "NEG" modes, it was set to reach the extreme values of V_{MEMS}, ±45 V

By comparing Figure 14 with Figure 8, one notices two main differences:

(1) The transition time between the operating modes is longer due to the C_{FB} frequency compensation, 100 μs instead of 5 μs, but still meets the requirements

(2) Although the voltage ripple on the V_{POS} and V_{NEG} is much larger in this case (120 mV instead of 35 mV on V_{POS} and 100 mV instead of 50 mV on V_{NEG}), the ripple on the V_{MEMS} is relatively small: around 17 mV in the "POS" operating mode and 10 mV in the "NEG" mode

Simulation results shown in Figures 12–14 validate the design, proving that it meets the wanted extended voltage range for V_{MEMS}, as well as the requirements set for the output voltage ripple and the transition time between operating modes.

4.4. Comparison between the Drivers Proposed in This Work, Based on ASIC1 and ASIC2. The multipurpose driver for MEMS sensors and actuators presented in Figure 9 has important advantages over the one proposed in Figure 2. First, it is easier for the user to set the V_{MEMS} range that best suits their application: one only needs to choose appropriately the external components and to set the PGA gain via the digital interface, instead of modifying the number of stages for the Dickson charge pump shown in Figure 2. Second, it uses power more efficiently, as the level of voltage V_{POS} is regulated and there is no need for a driver dedicated for the ICP. The latter feature also makes *ASIC2* significantly less complex than *ASIC1*, with only 11 pins required. Finally, the BoM for the entire driver comprises 19 devices, including *ASIC2*, compared to the 26 needed to implement the driver based on the Dickson charge pump.

These advantages are balanced, for some applications such as automotive, by the drawbacks associated with the use of an inductor: an expensive component that requires special design techniques for the printed circuit board. Also, an inductor-based DC-DC converter can be a major source of EMI radiations, especially when operating in a discontinuous current conduction (DCM) mode. However, this is not a major concern here due to the low power level required to drive the MEMS devices.

The burst-mode control specific to light loads used here can drive the switching frequency of the boost converter close to the audio range. Also, it results in a large voltage ripple on both the V_{POS} and V_{NEG} lines; this was compensated for by increasing the PSR of the LDOs which supply the V_{MEMS}. But the PSR improvement was partially obtained by employing the C_{FB} frequency compensation technique, which in turn resulted in longer transition times between the operating modes.

5. Summary and Conclusions

5.1. Summary and Main Contributions. Two novel CMOS ASIC-based solutions for generating voltages suitable to bias and control a wide range of electrostatic-driven MEMS sensors and actuators were presented. Both drivers proposed in this paper, shown in Figures 2 and 9, provide positive or negative programmable voltage, with maximum levels several times larger than their low-voltage (minimum 4.5 V) supply—the operation modes called here as "POS" and "NEG", respectively; also, they can short their output terminal to the ground line or leave it floating, when operating in the "ZERO" the "OPEN" modes, respectively. The two drivers are based on a novel topology that comprises generators for large positive and negative voltages followed by LDOs with external pass transistors. The LDOs share an external

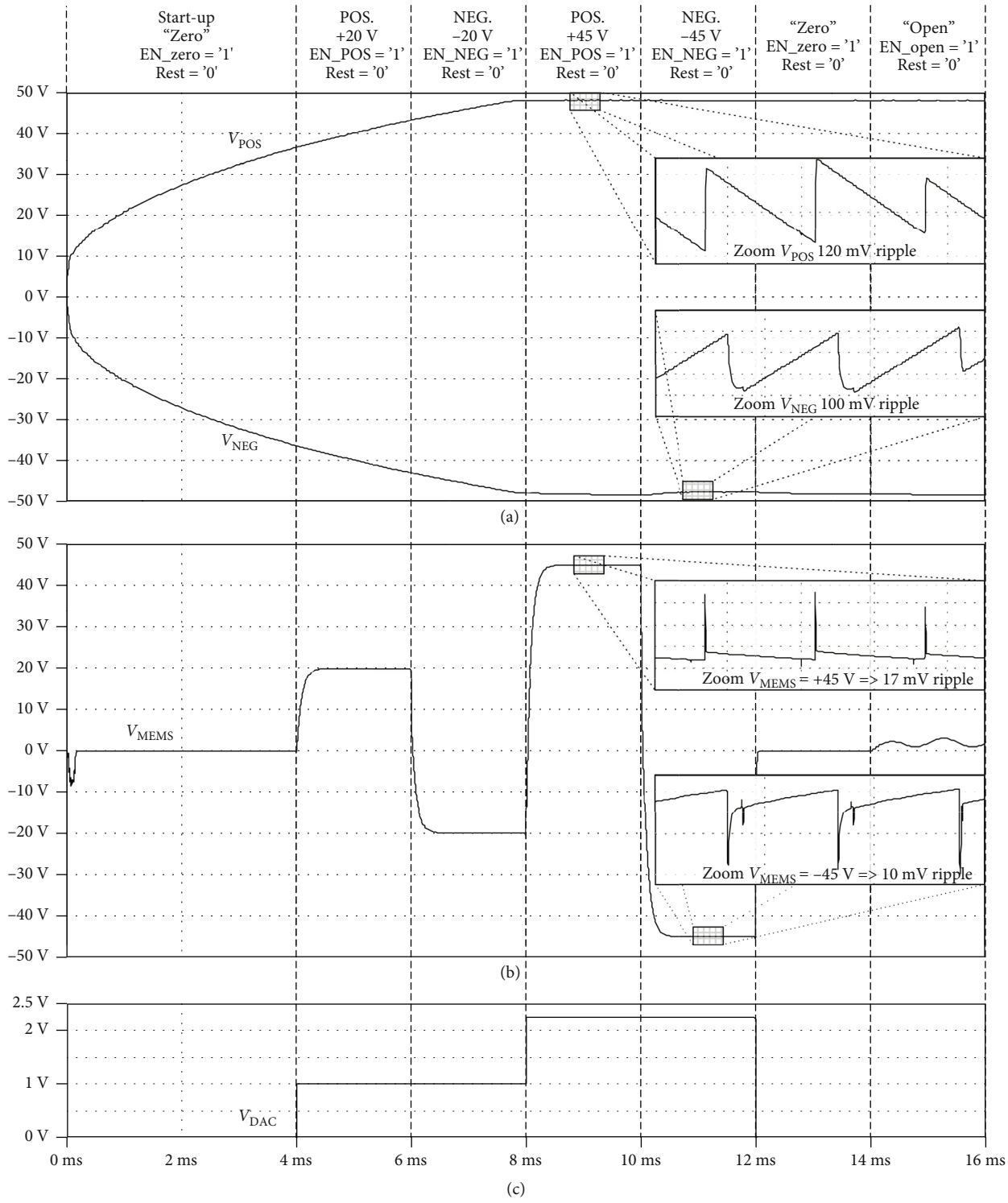

Figure 14: Simulation results for the driver shown in Figure 9. The control sequence is described on the top row: (a) V_{POS} and V_{NEG} with a zoom-in view for the ripple, (b) V_{MEMS} with a zoom-in view for the ripples in POS and NEG operation mode, and (c) V_{DAC} changes every 4 ms: 0 V, 1 V, 2.25 V, and 0 V.

feedback network. They provide well-controlled, programmable voltage levels with a low ripple to the V_{MEMS} output in "POS" and "NEG" operating modes and help implement the "ZERO" and the "OPEN" modes.

The driver described in Section 3 uses open-loop charge pumps to implement both the positive and negative voltage generators, based on which two LDOs provide V_{MEMS} voltage levels programable between [−20 V and +20 V]. Drivers for both charge pumps are integrated within an ASIC—called *ASIC1*—as well as the error amplifiers for the positive and negative voltage regulators that the DAC used to program the V_{MEMS} level and the support and auxiliary circuitry. The diodes and capacitors for both charge pumps are external, and so are the pass transistors of both LDOs.

An inductor-based boost converter with hysteretic burst control suitable for light loads is used to implement the positive voltage generator for the driver described in Section 4. The power switch of the boost converter also serves as the switching transistor for the inverting charge pump that implements the negative voltage generator. This arrangement results in a compact, more power-effective circuit solution for these generators than the one proposed in Section 3.

The major drawback of this solution is the larger output voltage ripple of these generators, which was compensated for by increasing the PSR of the LDOs. This was achieved in two steps: first, the PSR of the integrated error amplifiers was improved and second, a capacitor was placed in parallel with one of the two external resistors which form the feedback network common to the positive and negative LDOs. Note that the C_{FB} size was optimized for best PSR, rather than the usual approach, focused on LDO stability. The ASIC used by this driver—called *ASIC2*—is similar to, but somewhat simpler than, *ASIC1*: besides the two LDO error amplifiers, the DAC, and the support and auxiliary circuitry, it only integrates one power switching transistor and its driver, which is shared by the positive and negative voltage generators.

Both *ASIC1* and *ASIC2* were designed so that they can be implemented in low-cost HV CMOS technologies, without a triple well. Their substrate is connected to the GND line, the common reference of the system; therefore, no negative voltage could be applied to their pins. This was ensured by a suitable design of the negative LDO: first, a level shifter based on a Zener diode was placed between the output of the integrated error amplifier and the gate of the pass transistor which could go down to the largest negative voltage level within the system and second, the error amplifier was set to work in an inverting configuration, with the input voltage provided by a programmable gain amplifier driven by the DAC voltage, V_{DAC}. The PGA gain can be set so that the voltage provided by the negative LDO is equal in module with the voltage provided by the positive LDO, for the same value of V_{DAC}. Note that error amplifier of the positive LDO operates in the usual noninverting configuration, driven directly by V_{DAC}, and that the two LDOs share the external resistive feedback network.

This arrangement allows the user to set the range that the V_{MEMS} voltage can be programmed within, by appropriately choosing the external components and by programming the PGA gain. The driver described in Section 4 is more effective in this respect than the one described in Section 3: the number of external components required by the former does not depend on the V_{MEMS} range, as it is the case for the Dickson charge pump used by the latter. This feature was demonstrated by a design example that required the driver based on a boost converter to cover a wider V_{MEMS} range than the first one, [−45 V to +45 V].

To validate the topology and the circuit solutions proposed here, the ASICs for both drivers were designed in a low-cost 0.18 μm HV CMOS technology without a triple well, but with drain-extended transistors able to withstand drain-source voltages of up to 50 V. Circuit implementation of blocks with particular requirements set by the proposed topology was presented in some detail. Simulation performed on schematic representations of the entire drivers, including the external components, proved that the proposed drivers meet all requirements set for them.

5.2. Comparison with a State-of-the-Art. The main parameters of the two drivers proposed here are presented in Table 1, along with eight similar drivers reported in the literature. All these drivers provide positive and negative voltages with values several times larger than the supply voltage, by using only one ASIC along with external components.

First, one notices that only the two drivers proposed here implement all four operating modes required by a multipurpose driver for MEMS sensors and actuators. Second, the solutions proposed in [17, 28, 30] do not include an output voltage multiplexer; therefore, they provide their positive and negative voltages at two distinct output pins. Furthermore, the existing solutions—with the sole exception of [19]—do not allow for the output voltage value to be controlled digitally; instead, it can be changed only by adjusting some external resistors.

Four of the previously reported solutions were implemented in CMOS technologies, but only two of them—[19, 27]—did not use a triple well process. The range of voltage levels that these two provide is like the one covered by the driver described in Section 3, [±20 V], but the amplitudes of their voltage ripple are far larger. Our driver needs 26 components, including the ASIC: fewer than the one reported in [27] but almost double the number required by [19]. However, one notices that the solution proposed in [19] does not implement the "ZERO" operating mode and the V_{MEMS} ripple is up to 60 times larger.

The driver described in Section 4 provides the largest output voltage value listed in Table 1, from −45 V to +45 V. The drivers reported in [7, 30] are close, with ±40 V, but they were implemented in special processes, silicon on sapphire and BiCMOS, respectively. Also, the amplitudes of their voltage ripple are larger than the 17 mV–10 mV yielded by our driver, which requires fewer components to implement.

Table 1 indicates that the two multipurpose drivers for MEMS sensors and actuators proposed in this paper have major advantages over the similar drivers reported in the literature. The main one is flexibility: by choosing external components, the user sets the range that the V_{MEMS} voltage can be programmed within, while the operating mode and the actual value of V_{MEMS} are set through digital controls.

Table 1: Main parameters of the two multipurpose MEMS drivers proposed in Figures 2 and 9, compared against eight single-ASIC drivers reported previously.

Reference	Technology	BOM*	Vin range	V_{MEMS} "NEG"	V_{MEMS} "POS"	V_{OUT} ripple POS/NEG	V_{OUT} programmability	Operating modes
[7]	0.5 μm CMOS Si-on-sapphire	N/A	N/A	−40 V	+40 V	>1 V	Only by changing an external voltage	POS, NEG, OPEN
[15]	0.18 μm CMOS deep Nwell	N/A	1.8 V to 3 V	−9 V	9 V	N/A	N/A	POS, NEG
[16]	0.13 μm triple-well CMOS	N/A	1.2	−16.1 V	16.5	N/A	No	POS, NEG
[17]	0.5 μm 30 V deep Nwell CMOS	14	2.8 V to 5.5 V	−15 V to −10 V	+10 V to +20 V	−16 dB PSR	Only by changing the external resistors	POS, NEG
[19]; Figure 3	0.18 μm CMOS, without a triple well	14	4.75 V to 10 V	−20 V to −10 V	+10 V to +20 V	POS: 60 mV; NEG: 120 mV	Digitally controlled, 100 mV resolution.	POS, NEG, OPEN
[27]	Standard CMOS	>30	2.5 V to 6 V	−18 V	Vin to 30 V	≈10 mV	Only by changing the external resistors	POS, NEG
[28]	0.5 μm BiCMOS	12	2.7 V to 4.5 V	−8 V to −5 V	4.6 V to 6 V	POS: 5 mV; NEG: 15 mV	Only by changing the external resistors	POS, NEG
[30]	BiCMOS	>30	2.7 V to 5.5 V	−40 V	+40 V	POS: 20 mV; NEG: 10 mV	Only by changing the external resistors	POS, NEG
This work; Figure 2	0.18 μm CMOS, no triple well	26**	4.5 V to 5.5 V	−20 V to 0 V	0 V to +20 V	POS: 1.9 mV; NEG: 3.4 mV	Digitally controlled, 100 mV resolution	POS, NEG, OPEN, ZERO
This work; Figure 9	0.18 μm CMOS, no triple well	19	4.5 V to 5.5 V	−45 V to 0 V	0 V to +45 V	POS: 10 mV; NEG: 17 mV	Digitally controlled, 200 mV resolution	POS, NEG, OPEN, ZERO

*The ASICs are counted in, along with the external components; **assumes a complete discrete Dickon charge pump with individual diodes and capacitors.

To conclude, this paper introduced a novel topology for implementing multipurpose drivers for MEMS sensors and actuators, suitable for integration in low-cost HV CMOS processes, without a triple well. Two circuit embodiments designed in such a 0.18 μm process were presented and validated through simulations. They realize the required operating modes and provide accurate voltages programmable in fine steps over wide bipolar ranges, with very low-voltage ripples. Therefore, they are suitable for biasing and controlling a wide range of MEMS devices, including MEMS mirrors used in applications such as endoscopic optical coherence tomography.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

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