

Retraction

Retracted: Development and Implementation of a Low-Cost Test Solution for High-Precision ADC Chips Based on Intelligent Sensor Networks

Journal of Sensors

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This article has been retracted by Hindawi following an investigation undertaken by the publisher [1]. This investigation has uncovered evidence of one or more of the following indicators of systematic manipulation of the publication process:

- (1) Discrepancies in scope
- (2) Discrepancies in the description of the research reported
- (3) Discrepancies between the availability of data and the research described
- (4) Inappropriate citations
- (5) Incoherent, meaningless and/or irrelevant content included in the article
- (6) Manipulated or compromised peer review

The presence of these indicators undermines our confidence in the integrity of the article's content and we cannot, therefore, vouch for its reliability. Please note that this notice is intended solely to alert readers that the content of this article is unreliable. We have not investigated whether authors were aware of or involved in the systematic manipulation of the publication process.

Wiley and Hindawi regrets that the usual quality checks did not identify these issues before publication and have since put additional measures in place to safeguard research integrity.

We wish to credit our own Research Integrity and Research Publishing teams and anonymous and named external researchers and research integrity experts for contributing to this investigation.

The corresponding author, as the representative of all authors, has been given the opportunity to register their agreement or disagreement to this retraction. We have kept a record of any response received.

References

- [1] X. Liu and J. Sun, "Development and Implementation of a Low-Cost Test Solution for High-Precision ADC Chips Based on Intelligent Sensor Networks," *Journal of Sensors*, vol. 2022, Article ID 3453468, 12 pages, 2022.

Research Article

Development and Implementation of a Low-Cost Test Solution for High-Precision ADC Chips Based on Intelligent Sensor Networks

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Analog-to-digital converters (ADCs) are moving toward high speed and high resolution for low-cost testing. Based on the theory of intelligent sensor network, this paper designs a low-cost test solution for high-precision ADC chips, which solves the problems related to signal integrity. It mainly includes the following: designing an appropriate circuit connection scheme, planning an appropriate PCB stack-up structure, formulating detailed layout and wiring constraints, etc., and building a high-speed ADC test platform to obtain static and dynamic performance; based on the existing instruments in the laboratory, the effects of different signal sources, different input powers, and the presence or absence of filters on the dynamic performance of high-speed ADCs are studied. In the simulation process, the HyperLynx simulation platform is used to design and simulate the signal integrity of the high-speed acquisition board. Combined with the relevant theoretical knowledge of the signal integrity of high-speed digital circuits, the signal integrity analysis and simulation of the ADC module circuit and the DDR3 high-speed memory circuit are carried out, respectively. The results show that, taking the histogram method as a reference, when the optimal 30 windows are selected, the integral nonlinearity (INL) error of the proposed method is 0.12 LSB, the highest sampling frequency is up to 5GSps, and 61440 sampling points are required. The time is reduced by about 30% compared with the excitation error identification and removal (SEIR) method, which effectively improves the low-cost test effect of the ADC chip.

1. Introduction

With the rapid development of ultralarge-scale integrated circuits, the functions of chips are becoming more complex and diversified, and the performance requirements for automatic test machines in large-scale production testing are also getting higher and higher [1]. This makes ATE more complex and requires testing capabilities of digital circuits, analog circuits, and memory circuits at the same time, and the SoC test system emerges as the times require [2]. Because the trace is too long, the rising edge of the clock signal received by the CPU chip is no longer monotonic [3–5]. For a circuit that triggers collection by the rising edge, the clock signal may collect the same data twice; for a high-speed circuit board, due to the dense layout and wiring, it

is inevitable to make some wires close to other wires, and mutual coupling may occur between the wires [6], and the energy is coupled from one wire to another wire, distorting the signal waveform. When propagating on a discontinuous transmission line, reflections occur, which cause signal ringing, which is the recurring overshoot and undershoot. In practical engineering design, these signal integrity problems can be seen everywhere [7].

There are existing ADC standard test methods that can accurately test general-purpose ADCs, but in the field of high-resolution ADCs, this method has limitations such as high signal source accuracy and too many sampling points [8–10]. Therefore, research on fast and accurate test methods for high-resolution ADCs has become one of the focuses in the field of ADC testing. Although high-speed

digital circuits have real-time and high-speed data processing capabilities, they also bring some problems that do not appear in traditional circuits [11], especially signal integrity problems. With the continuous increase of chip functions, the complexity of chip functions requires automatic test equipment to provide various test resources [12]. This requires that in the test, not only the automatic test equipment can provide digital signals and analog signals of various frequencies, such as sine waves with high and intermediate frequencies and analog signals with modulation information, but also can analyze the signal output by the chip [13]. For example, it can judge the logic state of the digital output pin and can correctly sample the analog signal, Fourier transform, spectrum analysis, etc. [14].

This paper proposes a piecewise polynomial fitting method for testing high-resolution ADCs based on low-precision signal sources. The method first uses a low-precision DAC and a DC bias circuit to generate multiple correlated sinusoidal signals with different offsets. After analyzing the signal error, each correlated sinusoid is used as the input of the ADC (DUT) under test. In order to separate the low-precision sinusoidal excitation and the nonlinear characteristics of the DUT, the method uses a set of Fourier series with unknown coefficients to represent the transfer function of the DUT and then combines the known output code of the DUT and the transfer function expression to establish a relationship between the analog conversion level equations, use the least 2 multiplication method to fit a set of optimal Fourier coefficients, and then solve the transfer function of the DUT. Compared with the histogram method, the proposed method greatly reduces the number of required sampling points, but too few points will lead to lower test accuracy. In order to reduce or eliminate this effect, this paper further uses a rectangular window to divide the full-scale input range of the DUT into multiple segments and ensures that the overlap between adjacent segments is not less than 3%. Firstly, according to the technical specifications of the chip, a reasonable test scheme is designed to realize the parallel test of four devices under test. The main technology is to use a signal generator to divide the signal into 4 channels through the splitter and input them into 4 tuners, respectively, to generate intermediate frequency signals to 4 DUTs, including quantization error, offset error, static indicators such as nonlinear error, gain error, and nonlinear error, and dynamic indicators such as equivalent input reference noise, signal-to-noise ratio, signal-to-noise-distortion ratio, and spurious-free dynamic range. In addition, the commonly used test methods for static and dynamic indicators are also given. The downside is that an expensive external signal source is still required. In addition, the stability of the test is difficult to control due to the complexity of the test scheme and synchronization problems.

2. Related Work

At present, various ATE equipment at home and abroad has gradually transformed from the previous functional subdivision to functional integration: the previous ATE will be mainly divided into digital signal IC special testing machine,

analog signal IC special testing machine, and storage IC special testing machine. The current situation is that more and more test functions are concentrated on one or several ATEs. For example, the current mainstream SoC ATE includes digital signal IC, analog signal IC, digital-analog mixed signal IC test, and even many other types of IC test functions [15].

The signal integrity issues are further improved at a later stage of the design, so that the designed circuit has good signal integrity. Xie and Liu [16] insisted on using the method based on signal integrity analysis and simulation in the design of high-speed digital circuits, focusing on the analysis and simulation of sensitive signals, finding and solving signal integrity problems, so as to avoid signal integrity problems on the circuit. Many circuit design companies in foreign countries design circuits according to this design method and process, and this design method based on signal integrity analysis and simulation will gradually become more standardized.

Huan et al. [17] estimated the transfer function of the DUT based on the harmonic power combined with the Chebyshev polynomial rank and then solved the static parameters of the ADC under test. Since only the dynamic parameters need to be tested, this kind of method can realize the test of the DUT with less sampling points under the condition of satisfying the Nyquist sampling theorem. But it is not difficult to understand that the accuracy of the measured dynamic parameters will directly determine the reliability of the estimation in this method. In order to improve the test accuracy of dynamic parameters, Yang et al. [18] introduced a method to calculate the spectral characteristics of the DUT by means of interpolation DFT and based on the fast Fourier transform method to test the INL value of the DUT and then used the 16 to 20-bit ADC as the test subjects experimentally. On this basis, Coulby et al. [19] further use various window functions to process the sampled data to reduce or eliminate the problem of spectral leakage in actual testing. In addition, Cao et al. [20] also analyzed the influence of spurious components at nonharmonics on the estimation accuracy. However, because the dynamic parameter test is usually carried out under the condition of high frequency input signal, this method does not consider the monotonicity of the ADC under test. In addition, due to the inability to achieve accurate coherent sampling, spectral leakage and noise still exist at the harmonic points [21]. However, the DUT transfer function described by the Chebyshev polynomial will not be able to reflect the local nonlinear abrupt change [22]. Therefore, the method of estimating static characteristics based on dynamic parameters is only suitable for fast testing occasions that do not require very high accuracy of static parameters [23].

3. Construction of a Low-Cost Test Model for High-Precision ADC Chips Based on Smart Sensor Networks

3.1. Intelligent Sensor Network Structure. The digital-analog hybrid SoC chip test is usually a method of submodule

testing for intelligent sensor networks. The circuit function of the digital part is tested first, and then, the analog part is tested. This is because the test principle of the digital module is relatively simple, the requirements for test resources are low, and the test time is relatively short; the test of the analog module requires more complex test methods and test equipment, and the test time is relatively long. During the debugging process, the failure data is collected and processed, and the test items with higher failure probability are ranked first, which reduces the test time of the failed chip and reduces the test cost.

$$\text{que}(x, y) = \begin{cases} \sqrt{\text{vin}(x) - x} * x, \\ \sqrt{\text{vin}(y) - y} * y, \end{cases} \quad (1)$$

$$\sqrt{\text{per}(x) - x(t)} + \sqrt{\text{per}(y) - y(t)} = \begin{cases} \text{per}(x) - x(t), \\ \text{per}(y) - y(t). \end{cases} \quad (2)$$

In order to facilitate theoretical analysis, the transmission line model should be simplified as much as possible, so that the electrical characteristics of the medium remain unchanged, and the cross-sectional area of the transmission line also maintains a fixed value, that is, the transmission line is uniform. Transmission lines have distributed parameter electrical properties of capacitance, inductance, resistance, and conductance, especially when high-frequency signals are transmitted; these electrical properties are more pronounced.

$$\text{sue}(x, y) = \begin{cases} \int \text{vin}(x) - x dx * x, \\ \int \text{vin}(y) - y dy * y, \end{cases} \quad (3)$$

$$\left[\frac{\sqrt{\text{per}(y) - y(t)}}{\sqrt{\text{per}(x) - x(t)}} \right] = \left[\frac{\text{per}(x) dx - x(t) dt}{\text{per}(y) dy - y(t) dt} \right]. \quad (4)$$

During the transmission of digital signals, signal reflection will occur due to impedance mismatch. The reflection coefficient is used to characterize the amount of reflection. From the expression of reflection coefficient, it can be known that the terminal load ZL of the transmission line and the characteristic impedance Z together determine the size of the reflection coefficient. In high-speed digital circuits, signal reflection will cause SI problems such as overshoot, undershoot, signal delay, and ringing, and the mismatch of transmission line impedance is the most fundamental cause of signal reflection problems.

The method of realizing differential input is generally to convert single-ended signals into differential signals by transformers or differential op amps. Generally speaking, transformers have higher operating frequencies, and the linearity of differential op amps is generally better than that of transformers at low frequencies, so transformers are often used for AC coupling, and op amps are not limited by cou-

pling in bandwidth.

$$\frac{\text{per}(x, \text{snr}(x)) - x(t)}{\text{per}(y, \text{snr}(y)) + x(y)} - 1 = \frac{x - y}{\text{snr}(y)}, \quad (5)$$

$$\begin{cases} \text{snr}(x, y) < x - y, \\ \log \frac{\text{snr}(y) - \text{snr}(x)}{y - x} < \text{ref}[\text{snr}(y), \text{snr}(x)]. \end{cases} \quad (6)$$

SNR is usually defined as the ratio of signal power to noise power. For an ideal ADC, the noise mainly comes from quantization error. As mentioned above, different quantization methods have different corresponding minimum quantization errors. This article uses the rounding method for analysis. The rms value of quantization noise can be obtained by taking the square root of the mean of the squares of the quantization errors.

$$a * w_i^j(t) - t + b^{\wedge}2 * \sqrt{w_i^j(t) - t} + c^{\wedge}3 * \sqrt[3]{w_i^j(t) - t} + \dots + n = 1, \quad (7)$$

$$\left\{ \frac{i}{i+j}, \frac{j}{i+j} \right\} \in [-1 - \text{ref}(t) * t + n, 1 - \text{ref}(t) * t - n]. \quad (8)$$

Signal-to-Noise Distortion Ratio SINAD is the ratio of input signal power to all output signal distortion power (including noise and harmonic components, but excluding DC). Figure 1 measures all transfer function nonlinearities of the output signal plus all system noise. SINAD is a parameter that reflects the real performance of the ADC; usually SINAD can be expressed as above.

The effective number of bits refers to an ADC with a resolution of n , whose performance is equivalent to the number of bits of an ideal ADC due to interference from various noise and distortion. ENOB is calculated based on the ADC device signal-to-noise ratio, which converts the transmitted signal quality to the equivalent bit resolution. Here, resistors R13, R14, and capacitors C58-C60 form a differential two-way RC filter structure, where C60 = 20 pF is much larger than the input capacitance value of the ADC. Considering that the differential op amp AD8138 needs a positive and negative 3.3 V power supply, the switched capacitor voltage converter chip LM2644 of TI company is selected for implementation.

3.2. ADC Chip Design Indicators. In high-speed digital systems, many transmission lines are used for interconnection between ADC chip design devices, and the lengths are different. The delay of the signal passing through the transmission line cannot be ignored relative to the transition time of the signal itself. Digital signals are transmitted at the speed of electromagnetic waves on the signal line. At this time, the signal line is a network with parameters such as impedance, capacitive reactance, and inductive reactance, which can only be approximated by a distributed parameter system, that is, the transmission line model. Because the digital

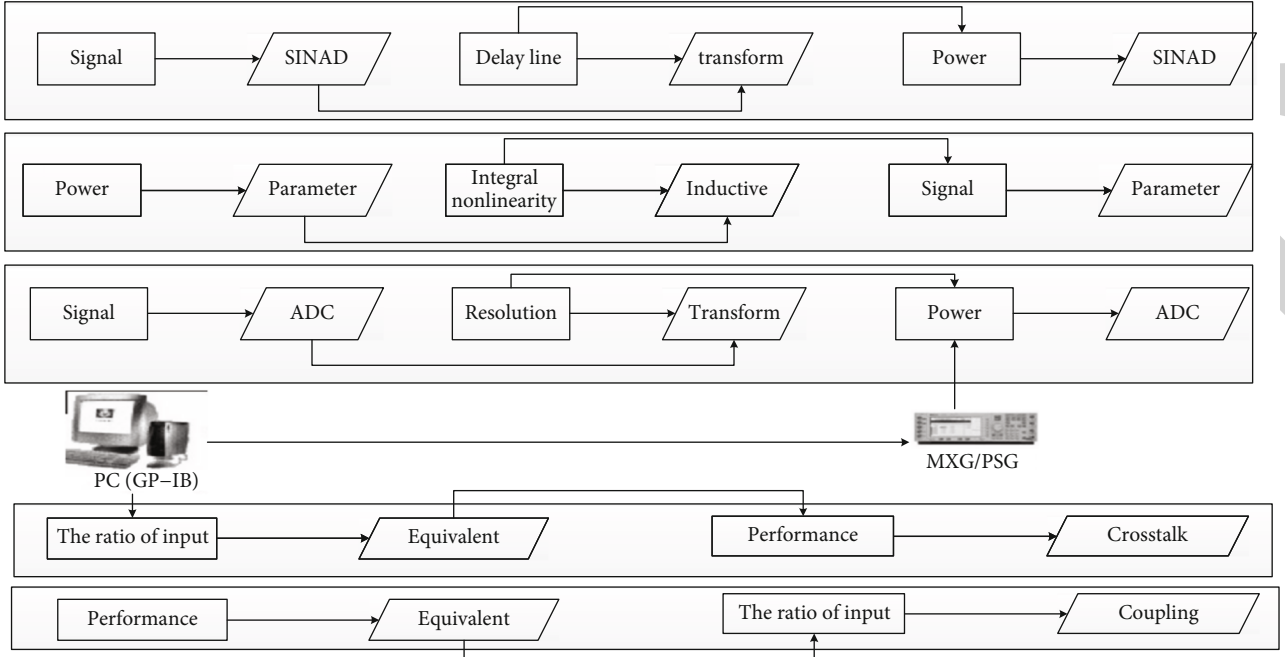


FIGURE 1: Smart sensor network topology.

signal will have a certain delay on the transmission line, it is also called a delay line.

$$[F_i(i) + F_i(j)], [F_i(i) - F_i(j)], [F_i(x) + F_i(y)], [F_i(x) - F_i(y)] = v_{ref}(x, y), \quad (9)$$

$$\prod (x + y) dx dy = \left[\frac{c_i(x)}{c_i(x) + c_i(y)}, \frac{c_i(y)}{c_i(x) + c_i(y)} \right]. \quad (10)$$

When two signal lines form a closed loop, mutual inductive coupling occurs between the signal lines. Signal changes on the attacker's network will affect the victim network through mutual inductive coupling, and the crosstalk caused by this coupling is inductive crosstalk.

$$\begin{cases} \frac{v(a) - v(b)}{v(a) + v(b)} < \frac{v(a) - v(b)}{v(a) - v(b)}, \\ \sqrt{a - b - 1 - a - b} < v(a) - v(b), \end{cases} \quad (11)$$

$$\left\langle \frac{omg(x, y)}{-omg(x, y)} \middle| x \right\rangle \subseteq \left\langle \frac{omg(x) - omg(y)}{-omg(x) - omg(y)} \middle| 1 \right\rangle. \quad (12)$$

When analyzing integral nonlinearity, sometimes due to offset or gain errors, the end of the conversion range may be shifted from the ideal value. Therefore, there are two methods to determine this end-point connection in practical applications: "best straight line method" and "endpoint method." The best straight line method is defined as the straight line that mathematically best fits the actual conversion curve of the ADC; the end point method is defined as the line connecting the first and last points in the conversion

curve.

$$\begin{bmatrix} miu(x_{1-a-b}^{a-b}, y_{a-b}^{1-a-b}) \\ miu(x - dx_{1-a-b}^{a-b}, y - dy_{a-b}^{1-a-b}) \end{bmatrix} \in \begin{bmatrix} v(\text{in}) \\ v(\text{out}) \end{bmatrix}, \quad (13)$$

$$\left\langle miu(x_{1-a-b}^{a-b}, y_{a-b}^{1-a-b}) \middle| x \right\rangle + \left\langle miu(x_{1-a-b}^{a-b}, y_{a-b}^{1-a-b}) \middle| y \right\rangle = x - y. \quad (14)$$

The offset error is the deviation between the actual analog input value and the ideal analog input when the output code transitions for the first time from the least significant bit. The gain error is the difference between the actual analog input and the ideal analog input corresponding to the highest two codes. The static performance of the ADC can be described by the input-output transfer curve. Ideally, the input and output characteristics show a highly uniform step in the entire dynamic range, but due to factors such as manufacturing process and working environment, the actual relationship between the level and the code word deviates from the ideal situation to a certain extent.

$$\sum \frac{1 - \partial(x - y) - \partial(x + y)}{\partial(x - y)} + \sum \frac{\partial(x + y)\partial(x - y)}{\partial(x, y)} = \sum \partial(1 - x - y). \quad (15)$$

Although according to Nyquist sampling law, such sampling will cause spectral aliasing and cause distortion, but if the input is a band-limited signal, effective sampling quantization can also be performed by using undersampling technology. Typically used for quantization of narrowband signals, new RF and IF sampling structures can be designed

TABLE 1: Design algorithm of sensor network signal source.

Design algorithm code	Sensor network signal data
Vector<vector<double>> neighbors;	Based on the method $\partial F_i(a)$
For(int i=0;i < k;i++){	Proposed in this paper $\partial(x, y)$
Neighbors.push_back();	Among the $v(a) - v(b)$
Distances[i].first	To the window function $1 - a - b$
Return neighbors;	The peak-to-peak $x - y$
For(auto vote : classvotes){	The transfer function corresponding
If(vote.second > maxvote){	Value of one group of data is $[F_i(i) + F_i(j)]$
Maxvote = vote.second;	$1 - \partial(x - y) - \partial(x + y)$
Res = vote.first;	Equal to the input range of $1 - x$
Or(int i=0;i < testset.size();i++){	In the last window function
If(testset[i][4] == predictions[i]){	Two groups of data $c_i(x) + c_i(y)$

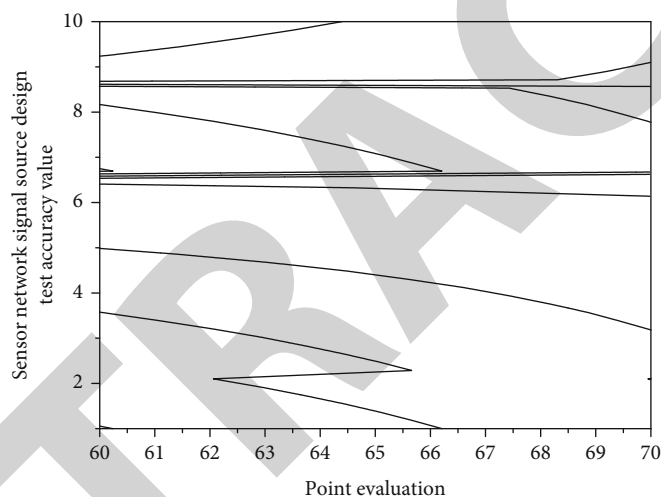


FIGURE 2: Design and test accuracy of sensor network signal source.

using undersampling techniques. Since all comparator branches are triggered by the same clock pulse, the fully parallel ADC only needs one clock cycle for each data conversion, so it has the fastest speed.

3.3. Signal Source Design of Sensor Network. In the high-speed acquisition board of the sensor network signal source, the analog-to-digital conversion chip is an important factor to determine whether the indicators of the entire board meet the requirements. In order to obtain higher accuracy and more stable performance, this paper chooses a high-speed chip that is widely used in the capture board and is produced by E2V Company; the model is EV10AQ190. This chip adopts time cross-sampling technology and realizes the purpose of high ADC sampling rate based on the working principle of multichannel analog-to-digital conversion core phase shifting. The input signal used to verify SEIR and the proposed method is generated by the superposition of a 10-bit Maxim 5183 DAC and a DC bias circuit, while the input signal used for the traditional histogram test method

is generated by a 16-bit Agilent E33522a. In addition, an additional channel of the instrument will be used to generate the DUT's clock signal. An Agilent 16702B logic analyzer will be used to generate the control signal for the DUT and the input signal for the DAC. The reference signal is a built-in 1 V voltage, and an external reference signal interface is reserved. The total power supply of the ADC under test is provided by Agilent N6705, and after passing through the combined structure of different LDOs and ferrite beads in the test board, it supplies power to the corresponding modules, respectively. For the digital output of the ADC to be tested, this paper chooses to use the NI PXle 6556 high-speed digital acquisition card in Table 1 to collect.

In addition, based on the method proposed in this paper, among the two groups of data in the last window function, the peak-to-peak value of one group of data is equal to the input range of the transfer function corresponding to the window function, while the other group has superimposed DC offset. Therefore, a full "1" output code will appear due to partial cut-off distortion. At this time, the INL value at

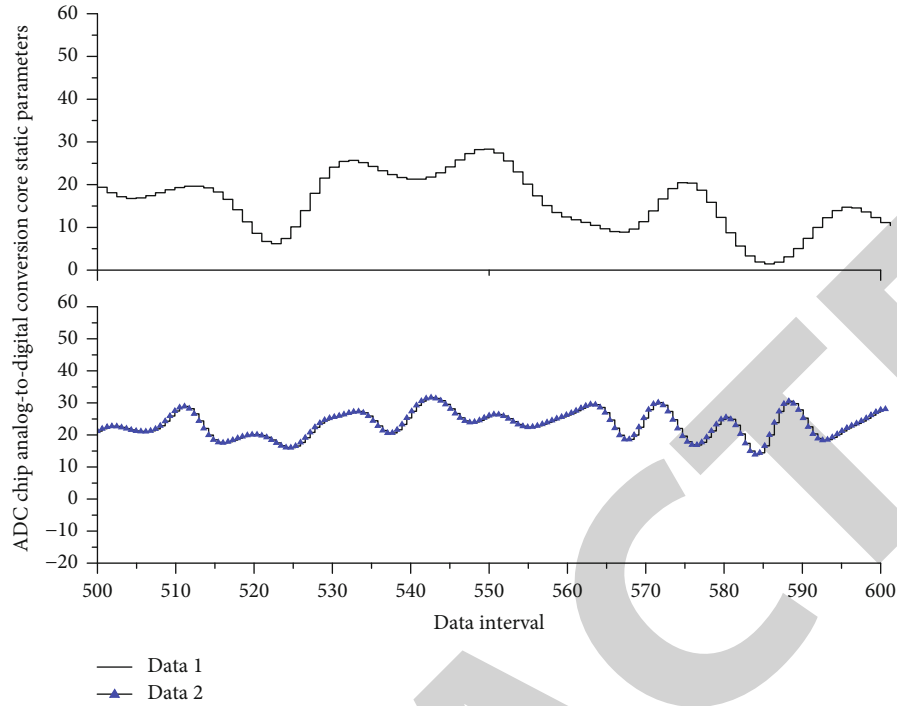


FIGURE 3: ADC chip analog-to-digital conversion core static parameters.

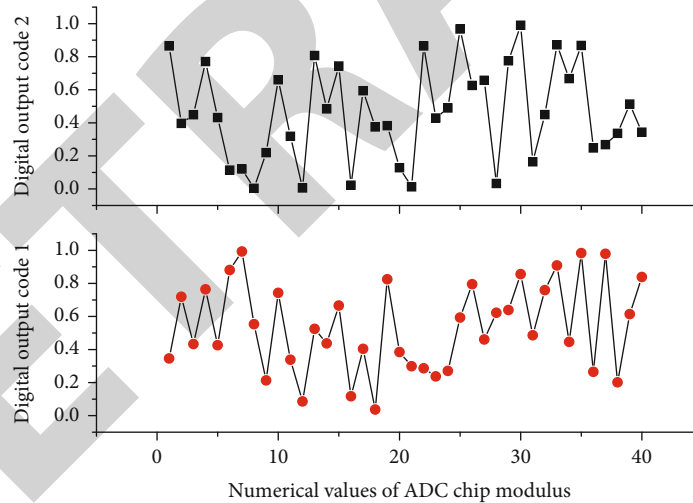


FIGURE 4: Digital output code value of ADC chip modulus.

the sequence corresponding to the full partial code in the window function will not be solved due to lack of real data. The number of code values for which an exact solution cannot be obtained should be equal to the number of all “1” codes. To reduce this effect, the offset should be as small as possible. In this paper, the offset between the two sets of data in the same segment is selected to be 10LSB.

Compared with the histogram method, the main difficulty of the proposed method lies in the accurate identification and removal of low-precision signal source errors. In the actual test process, in addition to the factors described above that will affect the test accuracy, the accuracy of the

selected signal source will directly affect the test accuracy. For example, when the resolution of the selected signal source is more than 3 bits higher than that of the ADC under test, the test error will not be lower than that of the histogram method. As the accuracy of the signal source of Figure 2 decreases, the test error of the proposed method will also change.

In the middle of the test, by stopping the CDR, the frequency register and the phase register are manually operated, so that the comparison edge is at the position of points 1, 2, 3, 4, and 5. At the same time as the test, the width of the eye diagram is tested by adding a bias voltage. Under

TABLE 2: Intelligent sensor network data.

Sensor node	Network bit	Network kHz	Network mW	Network ratio
ADC1	22.65	86.53	0.55	0.35
ADC2	28.02	39.65	0.21	0.64
ADC3	10.50	44.90	0.74	0.56
ADC4	14.00	77.04	0.34	0.30
ADC5	23.43	43.14	0.09	0.41
ADC6	25.12	11.34	0.52	0.67

the condition that the performance index of the instrument does not meet the requirements of chip test, various solutions including sampling test and multichannel multilevel test are proposed, and the effectiveness of these methods is verified in the actual test. The actual test result of the 2GSps 6-bit ultrahigh-speed ADC shows that the ADC's maximum conversion speed can reach 2.2GSps, the minimum quantization accuracy is 10 nV, the maximum effective bit can reach 5.7 bits at the highest conversion speed, and the total power consumption of the circuit is 310 mW.

The whole test head is divided into 8 groups, each group has a corresponding clock board (clock board), a control board (control board), 4 DC/DC conversion boards for power supply to the board, 1A power board (Power s knock Ply board) powered by a chip, and a maximum of 8 digital channel boards, analog modules, or RF modules. Above the test head is the test chip interface (OUT interface). The chip or wafer will be interfaced with the test chip through the test carrier board. The former is the difference between the time midpoint of the positive signal and the midpoint of the negative signal time. The latter is to select two single-ended signals that are not in the same group, and measure the time deviation between the time midpoints of the two signals. All tests should include both low-to-high and high-to-low variations.

3.4. ADC Chip Static Parameters. The construction goal of the acquisition board is as follows: under the control of FPGA, DDR3 can stably and effectively cache the static parameter data of the high-speed ADC chip sampled by the high-speed ADC, can read it out in real time, and send the data to the data through optical fiber or VPX backplane. High-speed clock generation module: it is mainly composed of a high-frequency clock chip ADF4360, a 10 MHz active crystal oscillator, a clock buffer chip CDCVF2310, and a set of SMA interfaces. Main control module: it is mainly composed of a Xilinx V6 series FPGA, which is matched with two XCF32P configuration chips and a JTAG interface. Computing module: it is mainly composed of a piece of TS201, which is matched with a FLASH chip for chip configuration and the corresponding JTAG interface. Cache module: it is mainly composed of two DDR3 chips, which can realize ping-pong operation. The chip is produced by Samsung, and the model is K4B2G1646C. Clock module: it is mainly composed of three active crystal oscillators of 50 MHz, 125 MHz, and 200 MHz and three corresponding clock buffer chips CDCVF2310.

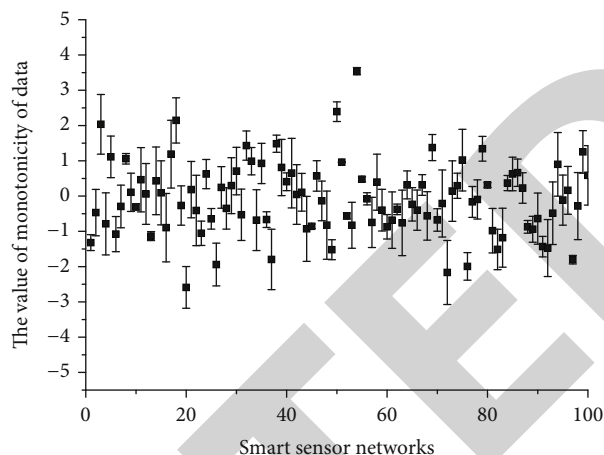


FIGURE 5: Data monotonicity of smart sensor network.

There are four analog-to-digital conversion cores inside the chip, which are marked as A, B, C, and D, respectively. The four analog-to-digital conversion cores in Figure 3 can cooperate with each other to make the chip work in four-channel mode, two-channel mode, or single-channel mode. All four ADC cores are controlled by the same external input clock signal and the same set of SPI buses. The chip needs to receive a pair of external differential clocks, the maximum clock frequency can reach 2.5 GHz, and the clock should be a sinusoidal signal with a peak-to-peak value of 500 mV and low jitter. There is a clock module inside the chip, which divides the external 2.5 GHz clock signal by two to generate a 1.25 GHz internal sampling clock. Different working modes handle the 1.25 GHz sampling clock differently. The best straight line method is defined as the straight line that mathematically best fits the actual conversion curve of the ADC; the endpoint method is defined as the connecting line between the first point and the last point in the conversion curve. Comparing the two methods, the best straight line method contains information about offset and gain errors, so the "best straight line method" is usually the first choice.

In order to achieve the test of Figure 4, a ramp or sinusoidal signal with a peak-to-peak value slightly larger than the full-scale input range of the DUT and a very low frequency can be selected as the input to the ADC. The square wave is used as the clock signal of the ADC to ensure that each digital output code value of the ADC is sampled at least 10 times. Use the logic analyzer and other instruments to collect the corresponding output codes, and transmit the data to the PC based on the LAN port, and finally process the data based on the histogram principle.

Due to the existence of various noise and nonlinear components, the number of occurrences of each code value is different. Since the peak-to-peak value of the input signal is slightly larger than the full-scale input range of the ADC under test, the maximum and minimum code values obtained by statistics cannot truly reflect the linearity of the ADC at the lowest and highest code values. Therefore, these two points should not be considered when doing statistical analysis of data.

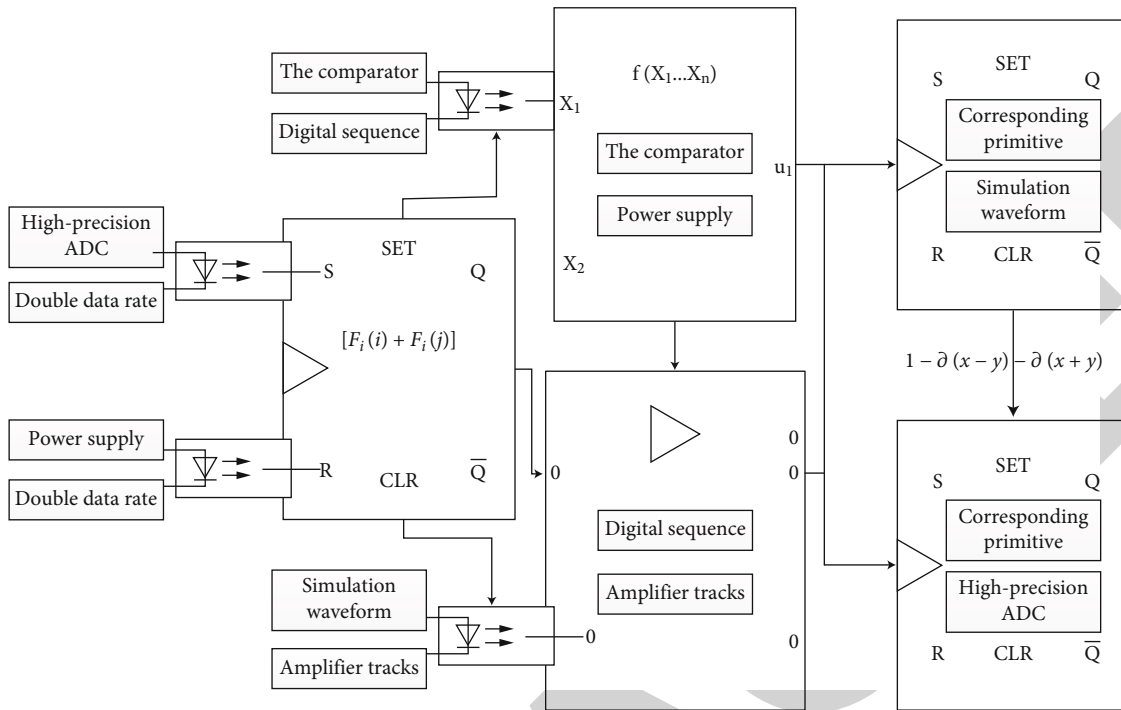


FIGURE 6: ADC chip low-cost test module.

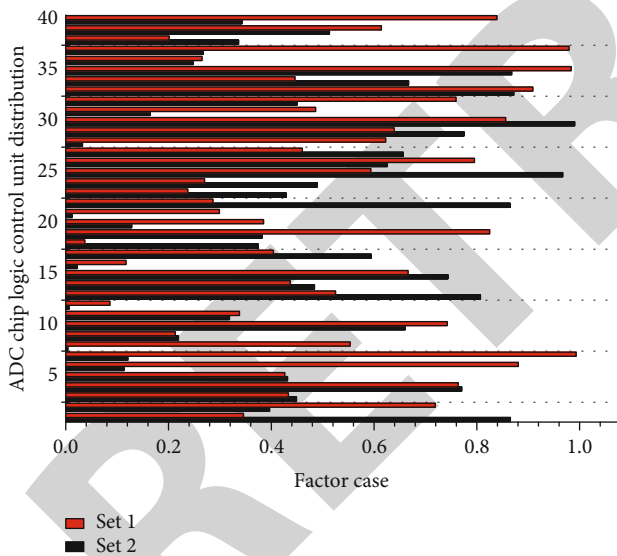


FIGURE 7: ADC chip logic control unit distribution.

4. Application and Analysis of Low-Cost Test Model of High-Precision ADC Chip Based on Intelligent Sensor Network

4.1. Intelligent Sensor Network Data Preprocessing. In the experiment, an intelligent sensor network data test platform was built, and the high-speed digital circuit and the improved circuit with signal integrity problems were tested, respectively, and the improvement effect of the signal integrity problem was verified. By comparing the simulation waveforms, it is shown that the high-speed digital circuit

with signal integrity problems cannot work normally, but all parts of the improved circuit can work normally, which ensures the correctness of the circuit design. First, import the IBIS (input/output device information) simulation model, perform signal integrity analysis and interactive simulation of individual key signals, find signal integrity problems such as crosstalk and reflection of key signals, and modify the design of the corresponding parts. Second, use the global fast simulation to verify the signal integrity design of the high-speed acquisition board, and modify the PCB design until all hidden dangers that may cause signal integrity problems are eliminated.

In the actual test process, the method in Table 2 selects two low-precision DACs to generate a sine signal and a DC offset, respectively. After the two are superimposed, the scaling circuit is used to make the scaled signal equal to the full-scale input range of the specific window function, and use the scaled signal as the input to the ADC under test.

On this basis, this paper selects a set of Fourier series to establish the transfer function expression in this segment and uses the relationship between the analog offsets corresponding to the two groups of sampled data in the same segment to be fixed to establish the relationship between equation to simulate the input signal. Finally, the proposed method uses the least squares method to solve the optimal coefficient and transfer function expression and superimposes the same DC offset on the first two sets of signals, so that the signals completely fall into other window functions, and then use the same method to solve others. A complete expression of the DUT transfer function can be obtained by successively processing the transfer function curves of adjacent functions.

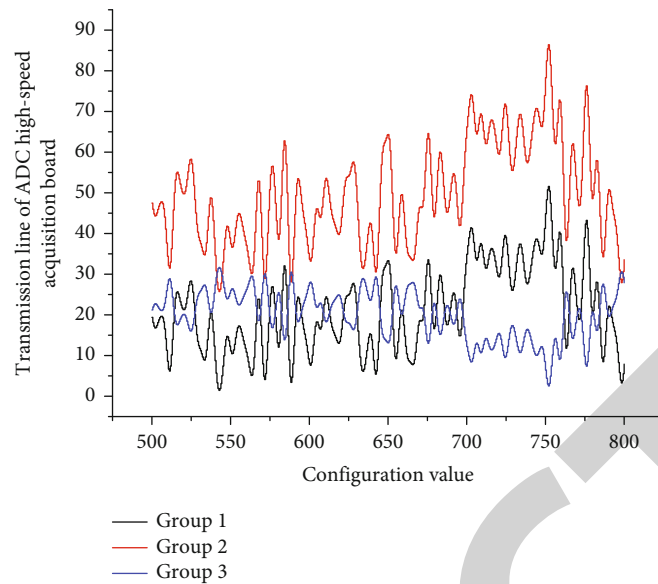


FIGURE 8: Transmission line configuration of ADC high-speed acquisition board.

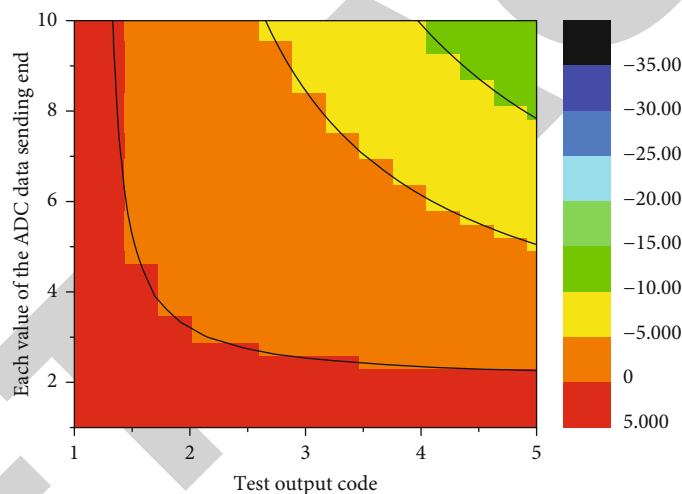


FIGURE 9: Each output code value of the ADC data transmission end.

Monotonicity refers to the variation law of the output digital code of the ADC with the increase of the input signal in Figure 5. For a monotonic ADC, when the input analog quantity increases continuously, the output code value of the latter should be greater than or equal to the output code value of the former. When the input signal rate is high, the ADC will operate in a monotonic state due to the limitation of the comparator conversion time. In the actual testing process, the probability that the code value width is $1/10\text{LSB}$ is very small, so the missing code is usually defined as the corresponding code value whose width is less than $1/10\text{LSB}$.

4.2. Low-Cost Test Simulation of High-Precision ADC Chips.

It can use verilog to write high-precision ADC chip test module simulation test, convert the value of D0-D1l from hexadecimal 0000 to binary, and input signal V_i from 5. For 0 V, the reference voltage V_r is 2.5 V. Under the control

of the clock signal, V_{out} increases from 0 V to 2.5 V in steps of $610\ \mu\text{V}$. The test conditions are the power supply voltage $V_{cc} = 3.3\ \text{V}$, the temperature $T = 270^\circ\text{C}$, and the digital-analog hybrid simulation is carried out. The digital sequence during the simulation is realized by verilog, and the simulation waveform is shown in the figure. The off-capacitor comparator uses the combination J1: off-capacitor and no-bad comparator. Its advantage is that the differential signal can be compared with a single-ended circuit, and it can be automatically zeroed for J1: the DC offset of the ring comparator. In the latch stage, the amplifier is turned off and the latch works, so the instantaneous output of the preamplifier is amplified by the memory into a logical “1” or “0.”

The primitives in Figure 6 are used to complete the double data rate (DDR) input function, and there are corresponding primitives, which can be instantiated when used. The IDDR primitive signal pins are shown as it. Q1 and

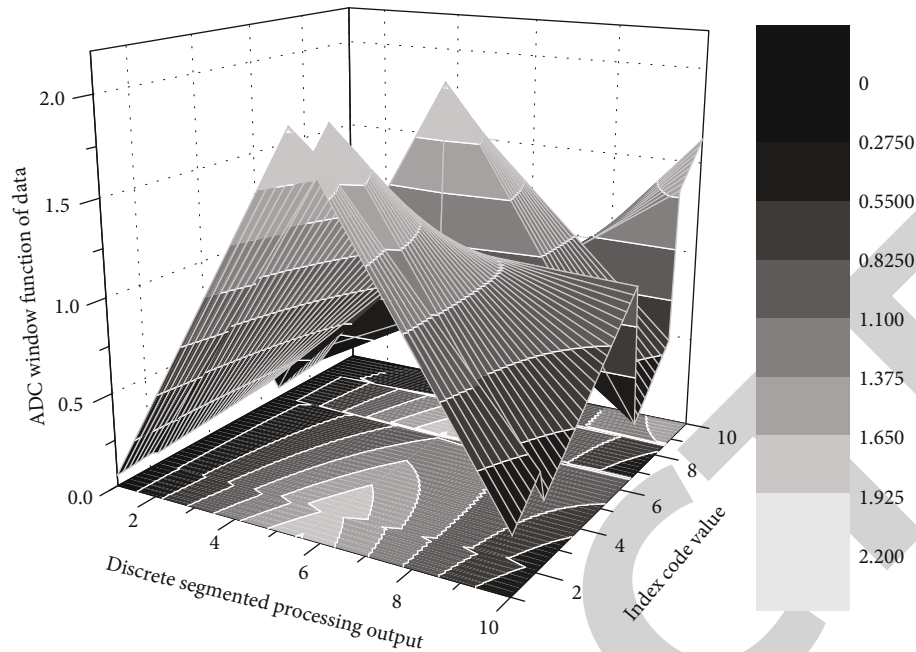


FIGURE 10: ADC window function segmented processing output code value changes.

Q2 are the data output of the IDDR register, C is the clock input port, CE is the clock enable port, and this enable port affects the data loading of the DDR flip-flop.

The sample-and-hold circuit controlled by the high-speed clock is the core part of the whole circuit, and its speed and accuracy directly determine the speed and accuracy of the entire conversion circuit, so in some designs, the sample-and-hold circuit will be individually designed using a more advanced process. When set to logic 0, clock changes are ignored and no new data is loaded into the DDR flip-flops. CE must be a logic 1 to load new data into the DDR flip-flop. D is the IDDR register input from the IOB. R is the synchronous/asynchronous reset pin. S is the sync/async setup pin.

In the actual working process, the logic control unit of Figure 7 first generates a logic digital code whose highest bit is 1 and other bits are 0 and adds it to the DAC input end. The output of this DAC will generate an analog reference signal of 0.5 and serve as the reference input of the comparator. When adding an analog signal to the input end of the ADC, the analog signal will be compared with the 0.5% time through the comparator. If the comparator output is a high level, the MSB is set to 1; otherwise, the MSB is 0. The output of the corresponding DAC is compared with the analog input signal at the input of the comparator to determine the actual logic value of the second most significant bit, which is stored in the output register. Repeat the above steps until all bits of the ADC are determined.

4.3. Example Application and Analysis. Virtex-6 series FPGA devices also include input serial-to-parallel conversion logic resources (ISERDES). The ISERDES unit is used to imple-

ment serial-to-parallel conversion, including clock and logic control functions, to assist in high-speed source-synchronous applications. The functions of the ISERDES unit include deserializer, serializer, and Bit-slip subunit. The high-speed data transmission can be completed through the ISERDES module, and the transmission rate cannot match the operating frequency in the FPGA. The high-speed serial sampling result data is input to the SelectIO module in the FPGA at the LVDS-DDR (differential level double-edge latched data transmission mode) level.

The data sending end is FPGA, the receiving end is the DDR3 data interface shown in Figure 8, and the IBIS simulation model of the driving source FPGA is Virtex-6, obtained from the Xilinx technical support website. Since the ADC conversion system is not completely linear, distortion occurs in the digital spectrum. Harmonic distortion is numerically equal to the ratio of the signal to the rms value of each harmonic component. Harmonic distortion only considers the second to tenth harmonics; harmonics above the tenth are usually assumed to be negligible.

In addition, based on the basic definition of the INL test, first analyze the analog input voltage value in Figure 9 corresponding to the change of each output code value of the ADC. This converts the ADC's many-to-one input-output relationship into a one-to-one transfer function.

Aiming at the overall circuit test of the 6-bit 2GSps ADC in this design, the TEKTRON-11LA7012 logic analyzer is used to directly sample the output of NC. This logic analyzer is the best logic analyzer currently available. It has an analog bandwidth of 3 GHz, and the highest data rate that the probe can reach is 1.4 Gbps. It is currently the only logic analyzer that can meet the test requirements of this ADC. Although the fitting result can improve fitting accuracy due to the

shorter transfer function contained in each segment, the test waste caused by repeated sampling is increasing. When the critical point is reached, the test efficiency becomes low.

When the number of window functions in Figure 10 is small, using the window function to process data in segments can significantly improve the test accuracy, and the number of sampling points required is less. When the number of window functions is greater than 100, the error of the test result does not decrease significantly, but the number of required sampling points will increase sharply. The test time caused by the number of sampling points will be extended accordingly. After adding a BPF with a center frequency of 1 MHz, although the noise floor of the signal is reduced, the second and third harmonics become larger. The main reason is that the designed filter attenuates only more than 60 dB at 2 MHz, and when the output power of the signal source is a 1 MHz sine of 0 dBm, its second harmonic is close to -71 dBm. At this time, the BPF is not suitable as an impedance at the ADC input. The real-time signal processor requires the high-speed ADC sampling module to be as close as possible to the antenna end, and the digital signal converted by the ADC of the RF signal is sent to the digital signal processing part, so as to obtain as much useful information as possible. The circuit design also optimizes the coupling capacity between the DAC stages according to the parasitic capacitance value, which improves the accuracy of the ADC. The comparator adopts the independent capacitor comparator of self-elimination and loss of power, which improves the comparison accuracy.

5. Conclusion

This article describes in detail the design and implementation of 12-bit 125 kHz sampling rate SAR ADC for touch screen controller chip designed in 35 gm CMOS process. In order to reduce power consumption, an ADC circuit that adopts two working modes is designed. When there is a touch event, the ADC will wake up without delay. If it is not turned on, the device will be in a state of drooping. At the same time, it is ensured that the ADC and the internal reference voltage source are turned off during the analog-to-digital conversion period. The test results show that under 60 MHz sampling and 20 MHz analog input, its SFDR is as high as 75 dB, and the effective number of bits is 10.6 bits. The paper also discusses the dynamic performance at different amplitudes and with and without filters on the analog input. Finally, combined with the actual test situation, the factors that lead to the unsatisfactory performance of AD9238 under low frequency input are verified and analyzed. According to the parasitic capacitance value, the circuit design optimizes the DAC-level state coupling capacitor, which improves the accuracy of the ADC. The function test of the high-speed interface and the DC parameter test are realized in a loopback way, so as to achieve the goal of greatly reducing the test cost of the integrated chip. Through the research of this subject, it is shown that the test scheme is an economical and effective high-speed interface circuit chip test scheme and has a practical reference value.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

- [1] N. Navabian, S. Beskhyroun, and J. Matulich, "Development of wireless smart sensor network for vibration-based structural health monitoring of civil structures," *Structure and Infrastructure Engineering*, vol. 18, no. 3, pp. 345–361, 2022.
- [2] A. Elango and R. Landry Jr., "FPGA-based autonomous GPS-disciplined oscillators for wireless sensor network nodes," *Sensors*, vol. 22, no. 9, p. 3135, 2022.
- [3] S. Gao, X. Zhang, C. Du et al., "A multichannel low-power wide-area network with high-accuracy synchronization ability for machine vibration monitoring," *IEEE Internet of Things Journal*, vol. 6, no. 3, pp. 5040–5047, 2019.
- [4] L. Mezzera, M. Carminati, M. Di Mauro, A. Turolla, M. Tizzoni, and M. Antonelli, "A 7-parameter platform for smart and wireless networks monitoring on-line water quality," in *Electronics, Circuits and Systems (ICECS) IEEE*, pp. 709–712, Bordeaux, France, 2018.
- [5] M. Abdulkarem, K. Samsudin, F. Z. Rokhani, and M. F. A. Rasid, "Wireless sensor network for structural health monitoring: a contemporary review of technologies, challenges, and future direction," *Structural Health Monitoring*, vol. 19, no. 3, pp. 693–735, 2020.
- [6] M. Rohani, M. Isa, M. Syahril, C. C. Yii, A. S. Rosmi, and B. Ismail, "Sigma-delta ADC topology implementation based on partial discharge detection using rogowski coil sensor," *Journal of Physics: Conference Series. IOP Publishing*, vol. 1019, no. 1, p. 12031, 2018.
- [7] G. Zhang, "A wearable device for health management detection of multiple physiological parameters based on ZigBee wireless networks," *Measurement*, vol. 165, p. 108168, 2020.
- [8] D. Laurijssen, W. Saeys, S. Truijien, W. Daems, and J. Steckel, "Synchronous wireless body sensor network enabling human body pose estimation," *IEEE Access*, vol. 7, pp. 49341–49351, 2019.
- [9] J. Picaut, A. Can, N. Fortin, J. Ardouin, and M. Lagrange, "Low-cost sensors for urban noise monitoring networks—a literature review," *Sensors*, vol. 20, no. 8, p. 2256, 2020.

- [10] S. Prager, M. S. Haynes, and M. Moghaddam, "Wireless sub-nanosecond RF synchronization for distributed ultrawideband software-defined radar networks," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 11, pp. 4787–4804, 2020.
- [11] T. Polonelli, D. Brunelli, M. Guermandi, and L. Benini, "An accurate low-cost Crackmeter with LoRaWAN communication and energy harvesting capability," *Emerging technologies and factory automation (ETFA) IEEE*, vol. 1, pp. 671–676, 2018.
- [12] M. P. Goswami, S. Hazarika, D. Bora, and U. Sarma, "WSN based embedded system for field parameter monitoring inside a low-cost polyhouse," *International Journal of Sensors Wireless Communications and Control*, vol. 10, no. 3, pp. 354–367, 2020.
- [13] H. B. Li, S. N. Qi, and C. M. Wu, "Forest fire positioning monitoring system based on wireless sensor networks," *J. Inf. Hiding Multim. Signal Process*, vol. 9, no. 4, pp. 970–976, 2018.
- [14] Y. Liao, N. Yu, D. Tian, C. Wang, S. Li, and Z. Li, "An intelligent low-power low-cost mobile lab-on-Chip yeast cell culture platform," *IEEE Access*, vol. 8, pp. 70733–70745, 2020.
- [15] N. Gunawardena, E. R. Pardyjak, R. Stoll, and A. Khadka, "Development and evaluation of an open-source, low-cost distributed sensor network for environmental monitoring applications," *Measurement Science and Technology*, vol. 29, no. 2, article 024008, 2018.
- [16] H. Xie and J. Liu, "Design of multi-parameter real-time acquisition system of human movement based on nanosensor," *Measurement*, vol. 194, p. 111056, 2022.
- [17] J. Huan, H. Li, F. Wu, and W. Cao, "Design of water quality monitoring system for aquaculture ponds based on NB-IoT," *Aquacultural Engineering*, vol. 90, p. 102088, 2020.
- [18] C. Yang, P. Cronin, A. Agambayev, S. Ozev, A. E. Cetin, and A. Orailoglu, "A crowd-based explosive detection system with two-level feedback sensor calibration," in *Proceedings of the 39th International Conference on Computer-Aided Design*, pp. 6–9, New York, 2020.
- [19] G. Coulby, A. K. Clear, O. Jones, and A. Godfrey, "Low-cost, multimodal environmental monitoring based on the Internet of Things," *Building and Environment*, vol. 203, p. 108014, 2021.
- [20] C. Cao, L. Zhou, Y. Wang et al., "Design and implementation of wireless motion sensor node," in *Electronic Information Technology and Smart Agriculture (ICEITSA)*, pp. 43–47, Huaihua, China, 2021.
- [21] B. C. Renner, J. Heitmann, and F. Steinmetz, "ahoi: inexpensive, low-power communication and localization for underwater sensor networks and μ AUVs," *ACM Transactions on Sensor Networks (TOSN)*, vol. 16, no. 2, pp. 1–46, 2020.
- [22] S. Sun, W. Yang, and W. Wang, "Power-saving design of radio frequency identification sensor networks in bus seatbelt monitoring systems," *Sensors*, vol. 20, no. 20, p. 5882, 2020.
- [23] S. Hou and G. Wu, "A low-cost IoT-based wireless sensor system for bridge displacement monitoring," *Smart Materials and Structures*, vol. 28, no. 8, article 85047, 2019.