Retraction

Retracted: Optimization of Voltage Dynamic Performance at Inverter Output with Machine Learning and Intelligent Virtual Impedance

Mobile Information Systems

This article has been retracted by Hindawi following an investigation undertaken by the publisher [1]. This investigation has uncovered evidence of one or more of the following indicators of systematic manipulation of the publication process:

(1) Discrepancies in scope

(2) Discrepancies in the description of the research reported

(3) Discrepancies between the availability of data and the research described

(4) Inappropriate citations

(5) Incoherent, meaningless and/or irrelevant content included in the article

(6) Peer-review manipulation

The presence of these indicators undermines our confidence in the integrity of the article's content and we cannot, therefore, vouch for its reliability. Please note that this notice is intended solely to alert readers that the content of this article is unreliable. We have not investigated whether authors were aware of or involved in the systematic manipulation of the publication process.

Wiley and Hindawi regrets that the usual quality checks did not identify these issues before publication and have since put additional measures in place to safeguard research integrity.

We wish to credit our own Research Integrity and Research Publishing teams and anonymous and named external researchers and research integrity experts for contributing to this investigation.

The corresponding author, as the representative of all authors, has been given the opportunity to register their agreement or disagreement to this retraction. We have kept a record of any response received.

References

[1] L. Wang, "Optimization of Voltage Dynamic Performance at Inverter Output with Machine Learning and Intelligent Virtual Impedance," *Mobile Information Systems*, vol. 2022, Article ID 5488103, 13 pages, 2022.

Research Article

Optimization of Voltage Dynamic Performance at Inverter Output with Machine Learning and Intelligent Virtual Impedance

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With the continuous improvement of industrial production and manufacturing level, all kinds of equipment are developing in the direction of refinement and precision, especially the equipment manufacturing industry such as automobile manufacturing, equipment, integrated circuits, chip manufacturing, and other semiconductor industries. An intelligent virtual resistance control strategy based on machine research is proposed for rational power distribution and cycle suppression when multiple inverters are operated in parallel in low-voltage microgrids. Based on this, the control strategy of temporary power reduction of inverters is improved to improve the parallel inverter power distribution accuracy and ensure the reliable dynamic response of the constrained current in the circuit between parallel inverters. Finally, a multi-inverter parallel system model is established to verify the correctness and effectiveness of the proposed control strategy. The voltage waveform under nonlinear load conditions is improved and high-frequency harmonics are suppressed, which has obvious advantages compared with the general virtual impedance design method.

1. Introduction

A large number of precision equipment with CPU, PLC, and other cores, these modern precision instruments, production equipment, etc. have very high requirements for power quality [1], sometimes just a momentary voltage dip may lead to very serious consequences, such as causing interruptions in the production process or equipment failure, thus causing enterprises to suffer huge economic losses, as shown in Figure 1 for a variety of high-end manufacturing equipment characteristics and the impact of power quality [2, 3]. These power quality problems can directly or indirectly cause serious economic losses to the national economy and seriously affect the safe, stable, and efficient operation of electric power.

IEEE standard 22 coordinating committee pointed out that the main power quality problems include voltage unbalance overvoltage, undervoltage, voltage dips, voltage surges, power supply interruptions, flicker current harmonics, or ground fault. Among them, voltage dip refers to the phenomenon that the square root mean value of frequency voltage suddenly drops to 90%~10% of the rated value at a certain moment, with a duration of 10 ms~1 min, and then rises back to near the rated value. Through a large number of survey data, it is found that the grid voltage dip is the most probable and serious power quality problem.

Voltage dips in the power grid have caused very serious effects on the normal operation of equipment [4, 5]. Siemens, Germany, has studied the voltage sensitivity of power electronics widely used in daily life and has given the effects of voltage dips on some important power electronics, as listed in Table 1. Many devices are affected by voltage dips, and the impact is so great that it seriously affects the safe and stable operation of the equipment. Therefore, it is of great practical significance to carry out comprehensive management of voltage dips [6].

For the voltage dips in the power grid, the existing main governance solutions are mainly divided into two aspects: active governance and passive governance. Active management is to optimize the system operation by changing the system structure and connection, such as transformer tap regulator, magnetic resonant transformer CVT, and static switch switching STS. However, this kind of management can
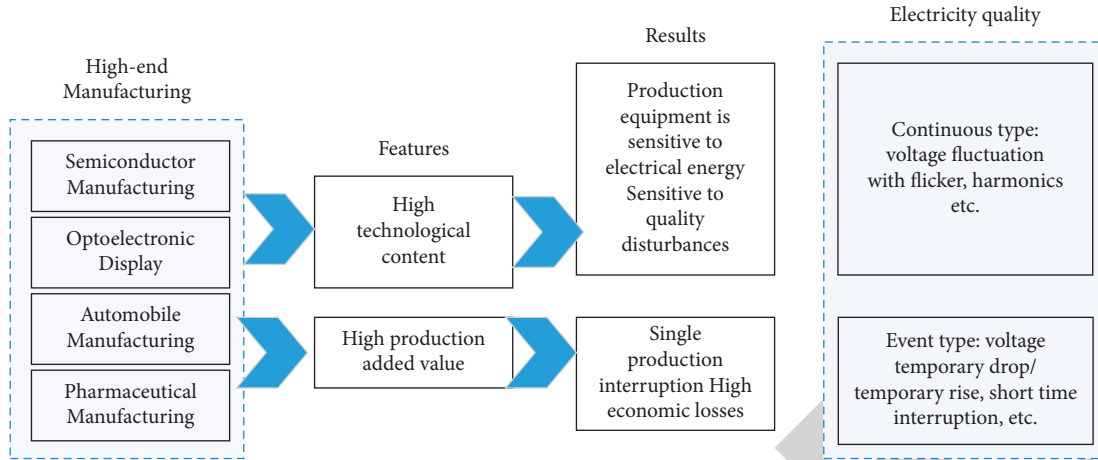
FIGURE 1: High-end manufacturing industry is affected by the power quality map.

TABLE 1: Effect of voltage dips on some equipment (rated at 100%).

Device name	Effects caused by voltage dips
Programmable controller	The PLC will stop when the voltage is less than 50%
Precision machine tools	It will be tripped when there are 2 to 3 cycles of voltage value below the threshold value
DC motor	Tripped when the voltage is less than 80%
Computer	If the voltage is less than 60% and lasts for more than 12 cycles, data loss will occur
Speed control motor	If the voltage is less than 70% and lasts for more than 6 cycles, the speed control motor will be cut off

TABLE 2: Treatment effect of different power quality treatment devices.

Name of governance device	Problems that can be governed	Treatment effect
STATCOM	Transient problems, voltage fluctuations, voltage flicker, power oscillation damping	Good
APF	Harmonics, reactive power, unbalance	Good
UPQC	Voltage dips/surges, voltage flicker, voltage unbalance, harmonics, power factor, load harmonic current, load unbalance	Good
UPS	Transient power interruption	Not good
DVR	Voltage dip/sudden rise	Good

only mitigate the impact of voltage dips to a certain extent, and the cost is high and not universal. With the development of power electronics technology, the passive governance method has been widely developed and applied. Table 2 compares and analyzes the treatment effects of the above power quality management devices. Among them, DVR is a series-type power quality controller, which ensures the voltage on the sensitive load side to maintain stability by injecting a compensating voltage with adjustable amplitude and phase in series between the system and the load [3, 7]. It not only can economically and effectively solve the power quality problems caused by voltage dips [8] but also can manage a variety of power quality problems through reasonable design and control, which has very good application prospects and is one of the most effective and economical devices recognized to solve the voltage dips of the power grid [9].

2. Related Work

The conventional DVR topology mainly consists of a DC-side energy storage unit, an inverter unit, an LC filter unit, a series-coupled transformer, and a bypass switch [10]. When the grid voltage does not dip, the DVR works in standby mode, when the DVR has no effect on the system and the losses are low. When a dip in the grid voltage is detected, the DVR is quickly connected to the system in series, and the DC-side voltage is passed through the voltage source inverter to produce a compensating voltage U_{dvr}, and the compensating voltage vector U_{dvr} is superimposed on the system voltage U_S to keep the load-side voltage U_L balanced and stable.

When the DVR detection module detects a grid voltage dip fault on the system side or a voltage dip fault on other lines at the bus due to a fault on a nearby line, the control module subtracts the load voltage reference value from the grid voltage value after the fault to obtain the voltage vector to be compensated by the device and then controls the inverter to output the compensation voltage with the required amplitude and phase through the corresponding control strategy. The DVR can output the compensated voltage in a very short time and thus has a fast compensation speed and good dynamic performance [11].

Table 3: Some development history of DVR.

Year	Capacity class	Country of development	Number of inverter levels	Series transformer
1999	12.47 kV 2 MVA	United States	2	Yes
2001	10 KVA 100 V	UK	2	Yes
2002	250 KVA 220 V	Netherlands	Multilevel	None
2003	220 V	Taiwan	2	Yes
2004	1 KVA 200 V	Singapore	2	None
2005	200 KVA 10 KV	Denmark Australia	2	Yes
2006	50 V	United States Canada	Multilevel	Yes
2007	10 KV	Singapore Denmark	2	Yes
2008	5 KVA 110 V	China	Multilevel	None

Inverters with virtual impedance have been well developed because of their good dynamic performance and cost advantages [12]. Following the installation of the world's first DVR device by Westinghouse in 1996, a series of in-depth analysis and research works on DVRs have been carried out by universities, research institutes, and companies in many countries one after another. The IGBT-based DVR device was announced to be developed by ABB in 1998 and attracted a lot of discussions. Since then, ABB has further upgraded the DVR products step by step, significantly increasing the capacity of the DVR and making it possible for the DVR products to obtain the required energy from the DC side directly from the grid [13]. In addition, research institutions such as Wisconsin and Cutler-Hammer have also researched and developed DVR devices and applied them to various research areas. These research institutions have not only achieved fruitful research results in the theoretical study of DVR but also have several devices that have been put into use and have achieved better operational results and experience. Some development history of DVR is listed in Table 3.

At present, 10 kVA/380 V DVR experimental prototype has been successfully developed by Tsinghua University, while the Chinese Academy of Sciences, Hunan University and other research institutions and universities have also concentrated their research efforts on DVR devices to carry out in-depth research, and has made many research results [14]. But whether from the capacity, voltage level, or engineering applications, there is still a large gap between the domestic development results on DVR compared to foreign countries [15].

As can be seen from the development history of DVRs, the inverters used in DVRs are mostly two-level structures with simple circuit structures and control methods, but the equivalent switching frequency is low and the inverter output harmonics are large. Multilevel converters are widely used in the prestage structure of DVRs because of their large capacity, easy expansion, and good output voltage harmonic

characteristics. There are three main basic circuit topologies of multilevel converters: (1) diode-clamped type, (2) fly-across capacitor type, and (3) cascaded H-bridge type. Among them, the cascaded H-bridge type multilevel converter has similar multiswitch combinations as the fly-span capacitor type structure compared to the first two structures, flexible control, easy-to-realize multilevel output, simple structure, easy modularization, and relatively independent DC power supply; therefore, it is widely used in DVRs to constitute a cascaded H-bridge type virtual impedance inverter (cascaded H-bridge-dynamic voltage restorer, CHB-DVR).

The topology, control strategy, and modulation strategy of the CHB-DVR have been studied in depth as follows:

(1) *Topology*. Literature [16–19] proposed a cascaded H-bridge converter topology for high system voltage and power in medium and high voltage systems, which was applied to DVR and effectively extended the capacity of DVR compensation device; literature [20] eliminated the expensive series transformer for CHB-DVR structure; literature [21] made a detailed analysis and introduction for different topology characteristics of DVR. Literature [22] provides a detailed analysis and introduction of different topologies of DVRs.

(2) *Control*. The overall control strategy of CHB-DVR is divided into two aspects: compensation strategy and control strategy. The commonly used DVR compensation strategies are as follows: in-phase compensation, complete compensation, and minimum energy compensation, and the compensation capacity and compensation effect of the three compensation strategies are compared in Table 4. Literature [23] proposes a DVR control strategy based on minimum energy compensation, which can greatly reduce the active injection of DVR and extend the compensation time of DVR; literature [24] proposes a control

TABLE 4: Comparison table of DVR compensation strategies.

Compensation strategy	Compensating voltage amplitude	Phase angle jump	Output active power
Same phase compensation	Min.	Larger	Larger
Fully compensated	Large	Min.	Larger
Minimum energy compensation	Large	Large	Min.

strategy that can manage the harmonics of the grid system based on the original DVR control strategy for the harmonic problem in the grid.

3. Method

The system consists of two resonance inductors that are receiving coil and transmission coil, which are denoted as Rx and Tx respectively, according to Figure 2.

The system is denoted by the circuit component, which is lumped (L, C, and R), according to the Figure 3.

A common topology of inverter is shown in Figure 3. This inverter supplies a three-phase resistive load consisting of a series inductor L_o, a resistor R_o, and a counter-electromotive force e_o, and the three-phase output current is i_o.

From Figure 4, it can be observed that the WPT may exist multiple resonant frequencies. The Resonance frequency is randomly tracked by using the traditional frequency-tracking method.

The gating signal $g_2 = |i_{o\alpha}^*(k+1) - i_{o\alpha}(k+1)| + |i_{o\beta}^*(k+1) - i_o(k+1)|$, $(i_{oa}, i_{ob}, i_{oc}) = 10\,A$, $R_{oa} = R_{ob} = R_{oc} = 0.1\Omega$, $L_{oa} = L_{ob} = L_{oc} = 20\,mHT_s = 50\mu s10i_o^*(k-1) - 20i_o^*(k-2) + 15i_o^*(k-3) - 4i_o^*(k-4)_\circ$ determines the switching state of the converter.

$$S_y = \begin{cases} 1, & \text{Switch closed,} \\ 0, & \text{Switch open,} \end{cases} \tag{1}$$

where $Y = a, b, c$. It can be expressed in vector form as follows:

$$S_y = \frac{2}{3}\left(S_a + aS_b, a^2S_c\right), \tag{2}$$

where $a = e^{-j2\pi/3}$, S_g are the switching state vectors.

The load voltage vector generated by the inverter is defined as follows:

$$U_O = \frac{2}{3}\left(U_{aN} + aU_bN, a^2U_{cN}\right), \tag{3}$$

where U_{aN}, U_bN, U_{cN} are the voltages between each phase of the inverter and the neutral point N.

The relationship between the load voltage vector U_O and the switching state vector S_g is as follows:

$$U_O = U_{dc}S_g, \tag{4}$$

where U_{dc} is the DC bus voltage.

Substituting equation (3) into equation (4), we get that the relationship between the switching state variable (S_a, S_b, S_c) and the load voltage vector U_O as follows:

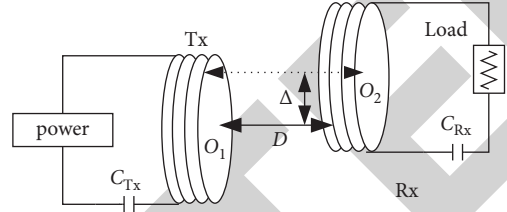$$U_O = \frac{2}{3}U_{dc}\left(S_a, aS_b, a^2S_c\right). \tag{5}$$

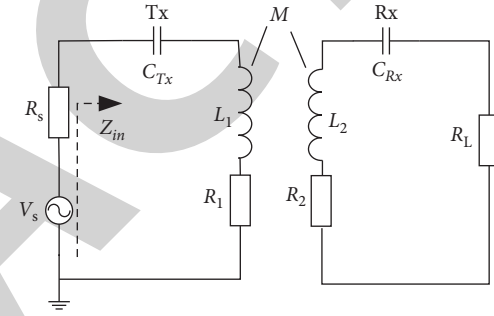FIGURE 2: Concise diagram of system on basis of magnetically coupled resonators.

FIGURE 3: The circuit equivalent for system. Each coil is considered as a train of resonators in the modeling.
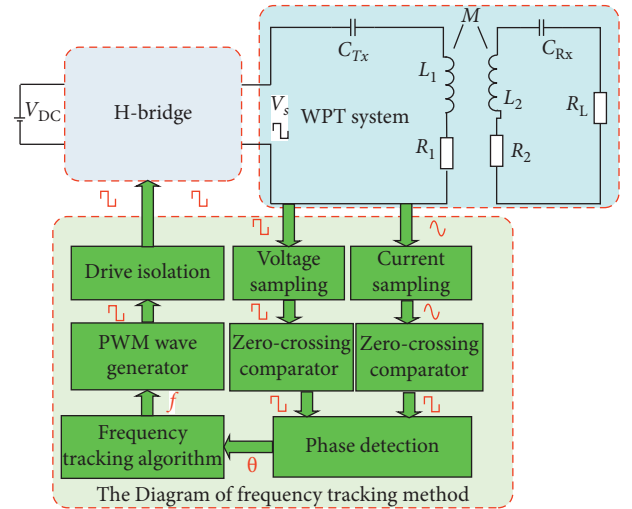

FIGURE 4: The frequency-tracking method.

According to the different combinations of (S_a, S_b, S_c), the inverter output voltage space vector is shown in Figure 5.

When multiple inverters are operated in parallel, the multiinverter parallel system is first analyzed, as shown in Figure 6.

In general, the switching frequency of the inverter is so high that the instantaneous values of the variables can be
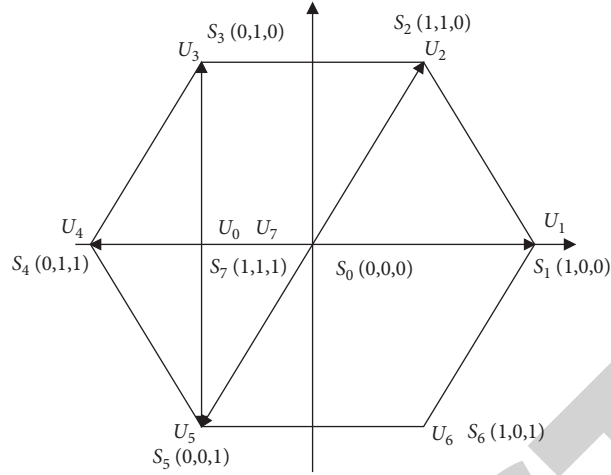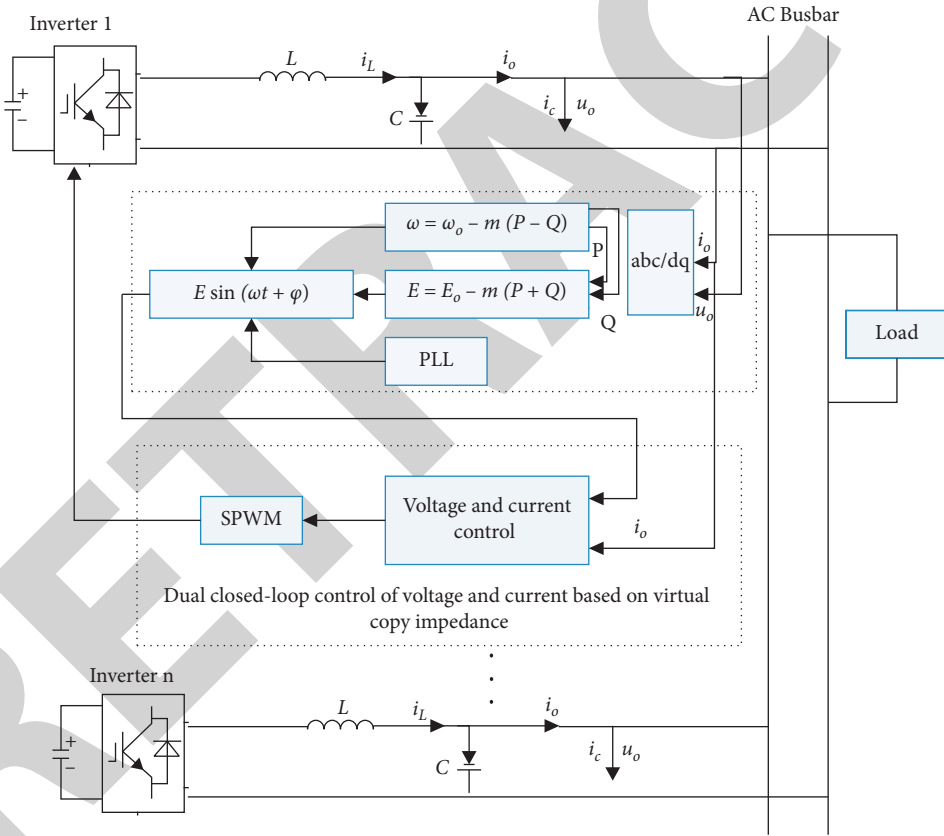
Figure 5: Inverter output voltage space vector.

Figure 6: Block diagram of parallel inverter output characteristics control.

considered to be equal to their average values in one switching cycle. For the control of the inverter, the virtual impedance-based v method is used, and its specific control block diagram is shown in Figure 7.

The U_0 can be expressed as follows:

$$u_0 = u_{0\text{ref}}(s)G_{\text{Inv}}(s) - \left(Z_{\text{Inv}}(s) + \frac{L_v s}{T_f s + 1}G_{\text{Inv}}(s)\right),$$

$$i_0(s)\,u_{0\text{ref}}(s)G_{\text{Inv}}(s) - Z_{\text{InvE}}(s)i_0(s). \tag{6}$$

$G_{\text{Inv}}(s), Z_{\text{Inv}}(s)$ are based on capacitor-current feedback control; $Z_{\text{InvE}}(s)$ is obtained by the following equation:

$$Z_{\text{InvE}}(s) = Z_{\text{Inv}}(s) + \frac{L_v s}{T_f s + 1}G_{\text{Inv}}(s). \tag{7}$$

They are reduced by R after introducing a certain virtual inductance L_v, so that the fundamental frequency output impedance Z_{InvE} is approximately purely inductive. Therefore, the system inductance can be designed by changing L_v,
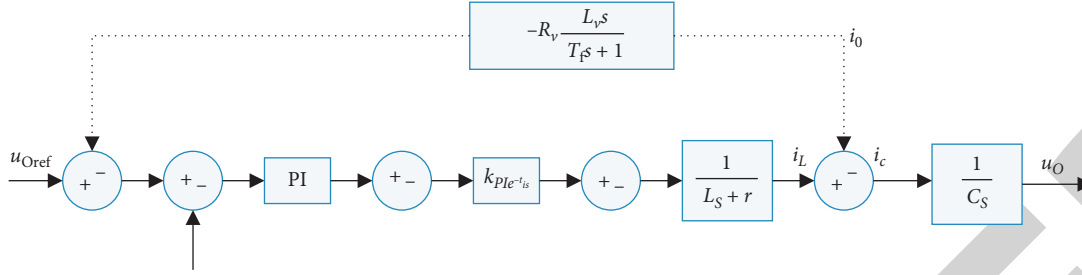
Figure 7: Block diagram of virtual impedance-based control.

and then, the system impedance of each parallel inverter unit can be matched.

Low-voltage lines generally exist L_{Line} much larger than R_{Line}, and it is assumed that the low-voltage line impedance Z_{Line} is as follows:

$$Z_{\text{Line}} = R_{\text{Line}} + sL_{\text{Line}}. \tag{8}$$

The fundamental system impedance Z_{Line} of the parallel inverter is as follows:

$$Z = Z_{\text{In}vE} + Z_{\text{Line}} = R_s + jL_s. \tag{9}$$

$Z_{\text{In}vE}$ is approximately purely inductive, and Z_{Line} is purely resistive, which is easy to cause power coupling and output voltage landing when the size of R_s and L_s is comparable. In this regard, by introducing virtual negative resistance to reduce the resistive component of the system impedance, the coupling degree between the output power is reduced, and the virtual negative impedance is obtained as follows:

$$Z_v(s) = -R_v + \frac{L_v s}{T_f s + 1}. \tag{10}$$

The system impedance can be expressed as follows:

$$Z(s) = Z_{\text{In}v}(s) + \left(\frac{L_v s}{T_f s + 1} - R_v\right) G_{\text{In}v}(s) + R_{\text{Line}} + sL_{\text{Line}}$$

$$= R + jX. \tag{11}$$

A suitable virtual negative resistance R_v is chosen to meet the impedance matching requirement. Considering that the power decoupling makes the system impedance at the fundamental frequency $R = X$, the filtering time constant T_f is very small and can be neglected, $G_{\text{In}v}(s) = 1, Z_{\text{In}v}(s) = 0$, and thus, the total system impedance can be simplified as follows:

$$Z(s) = R_{\text{Line}} - R_v + s(L_{\text{Line}} + L_v). \tag{12}$$

From equation (12), it can be seen that only $R_v = R_{\text{Line}}$ needs to be satisfied under the condition of fundamental impedance to achieve completely independent decoupling from the inverter. The ideology of segmentation frequency-tracking algorithm is shown in Figure 8.

CNNs have been widely used in classification problems for power system stability analysis, but their applications in
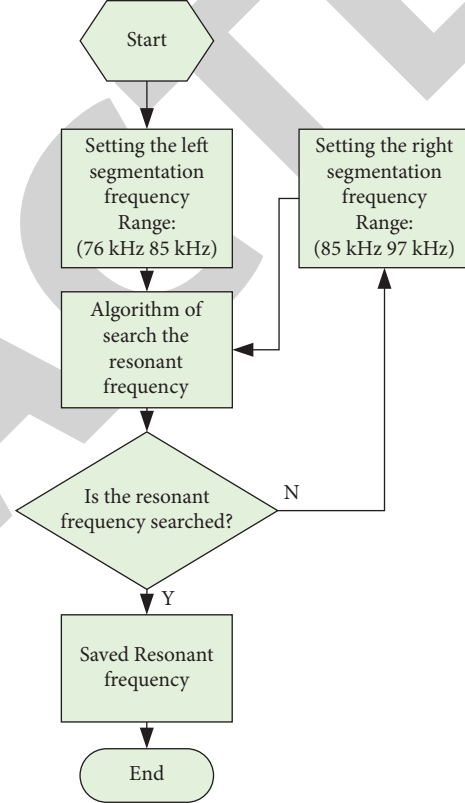

Figure 8: Flowchart of segmentation frequency-tracking algorithm.

regression problems are rarely explored. In this section, the advantages of CNN in classification and regression problems are fully utilized to develop the inverter output-time voltage dynamic performance of virtual impedance and quantitative risk classification. First, the traditional stability classification result is replaced by a binary combination of stability classification result and plausibility metric as the output of the classification model, so that the plausibility of the classification result can be grasped intuitively. Then, by setting the confidence threshold, the stability prediction results of the samples are divided into four sets: stable set, unstable set, missed unstable set, and misclassified unstable set. For the misclassified destabilization set and the stable set, the voltage stability margin at output is quickly predicted by the CNN regression model; for the missed destabilization set and the destabilization set, the stability margin is set to −1 according to the constructed voltage stability margin at
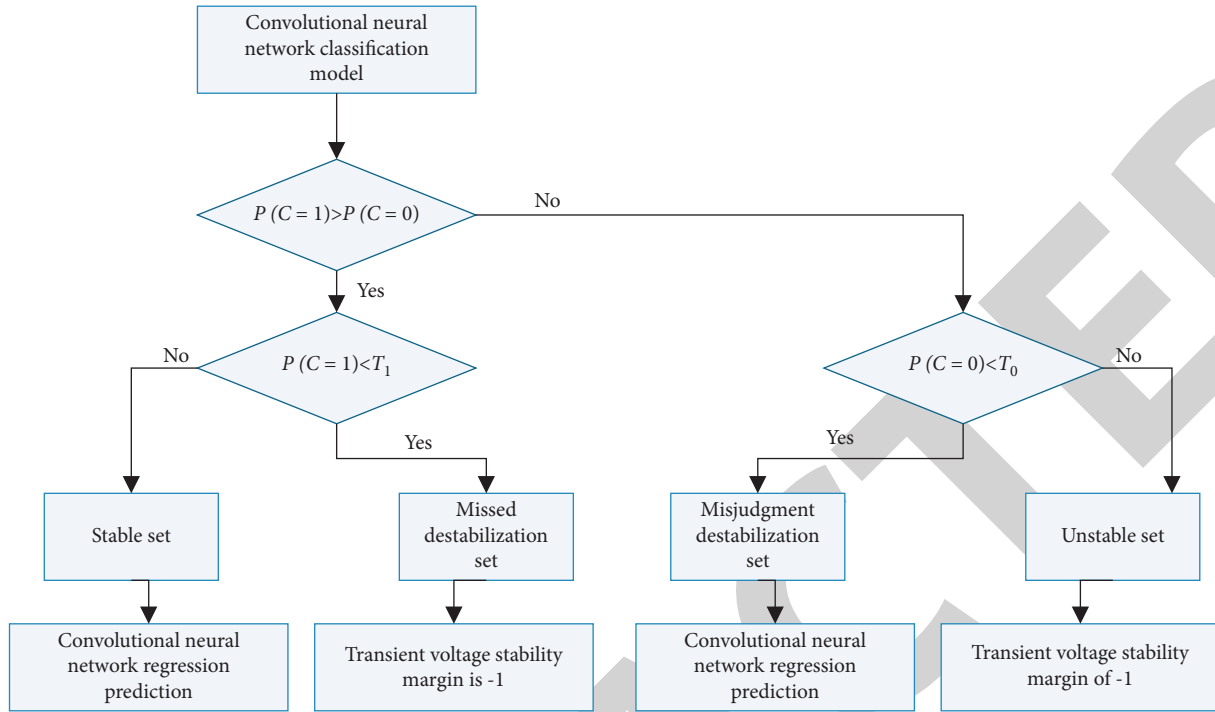
FIGURE 9: The process of analyzing the dynamic performance and confidence with virtual impedance.

output index, and the specific analysis process is shown in Figure 9. The method improves the confidence of the inverter output-time voltage dynamic performance of virtual impedance, solves the problem of mishandling the omission/misjudgment cases, and realizes a reasonable quantitative evaluation of the output-time voltage stability, which is fully applicable to practical rapid evaluation applications [25, 26].

After softmax processing, for each test sample, the predicted result of the CNN classification model corresponds to a probabilistic output [27]. In this section, the above two are combined to obtain a binary indicator to replace the traditional single classification result indicator, whose expression is as follows:

$$y = (C, P). \tag{13}$$

C is the stability discriminant result, and the value of C is 0 for destabilization and 1 for stability; P is the probability corresponding to the stability discriminant result.

The confidence threshold can be set by an iterative search of the training samples T_1, T_0. In the training phase, the confidence threshold is determined based on the samples obtained from the system historical data or time domain simulation results T_1, T_0; in the evaluation phase, the set of prediction results of the samples is divided using the confidence threshold determined in the phase, and the set is updated immediately if there is an error in the set division due to the possible difference in the confidence threshold corresponding to the training samples and the test data. In this stage, the confidence threshold T_1, T_0 is readjusted by analyzing the cases of division errors so that it can be correctly divided for the test data set. Through the update learning process of CNN, the confidence thresholds can

perform better on unknown data and substantially improve the generalization ability.

As shown in Figure 9, the probability of judging as stable is expressed by $P(C = 1)$, and the probability of judging as unstable. If $P(C = 1) > T_1$, the prediction result is considered credible and classified into the stable set; on the contrary, the prediction result is not credible and classified into the unstable set. On the contrary, if $P(C = 1) < P(C = 0)$, the prediction result is initially judged as unstable. If $P(C = 0) > T_0$, the prediction result is considered credible and is classified into the unstable set; on the contrary, the prediction result is considered untrustworthy and is classified into the misjudged unstable set.

Based on the above principles, the prediction results are classified into stable set, unstable set, missed unstable set, and misjudged unstable set. For the unstable set and the missed unstable set, they are directly fed back to the dispatching operators for early warning; while for the stable set and the misjudged unstable set, the CNN regression model-based method proposed in the next section is used to predict the voltage stability margin at output to achieve quantitative and graded risk assessment of voltage stability at output [28, 29].

4. Experiments

For the intention of checking the validity of the approach, we have built a prototype model for the system. It contains a DC voltage source, an H-bridge inverter, a transfer resonant coil, a receiving resonant coil, and a load. For the voltage source of DC, its value is 30 V. The H-bridge inverter is arranged to realize AC excitation, which is presented in Figure 10(b). It
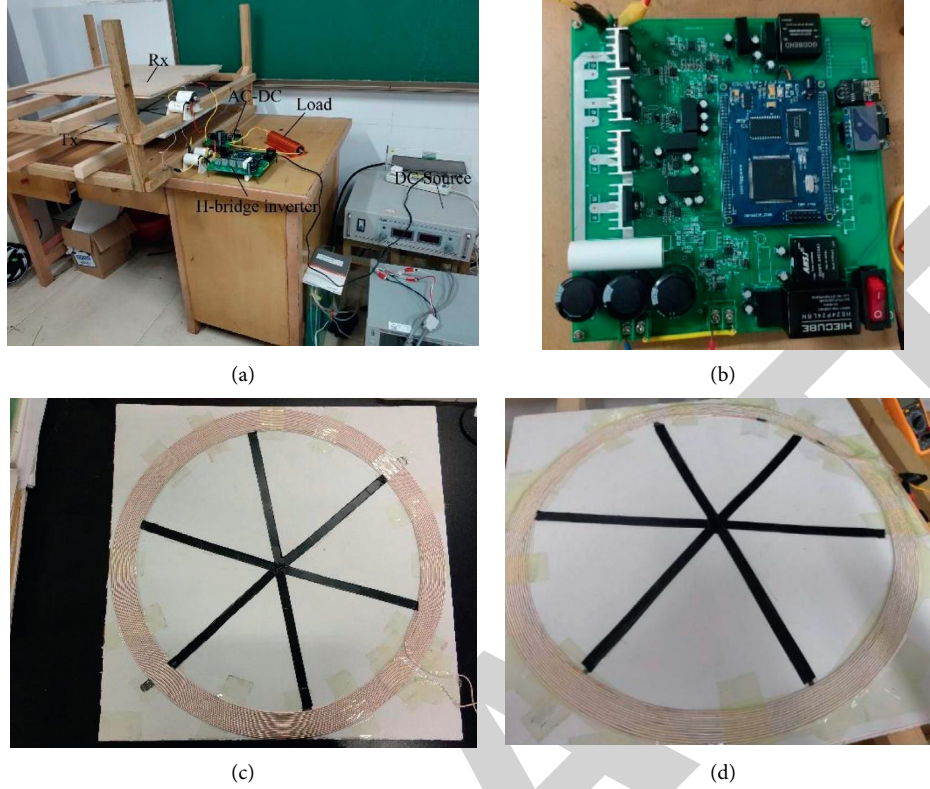
(a)

(b)

(c)

(d)

Figure 10: Experimental setup. (a) Setup. (b) H-bridge inverter. (c) Tx. (d) Rx.

consists of four Si C MOSFETs (C2M0080120D). Figure 10(c) shows the transmission resonant coil. Its outer diameter is 60 cm with a pitch of 0 cm for 17 turns. Figure 10(d) shows the receiving resonant coil. Its outer diameter is 55 cm with a pitch of 0 cm for 13 turns. The circuit of phase detection is displayed in Figure 10. Through the circuit, the input electric tension and the input current are converted to signal of square wave. Then, we can work out the value of θ by comparing the two values, that is, the forward position for the square wave signal of input voltage, and the forward position for the square wave signal of input current, with the aid of DSP28335 ECAP. Every coil is made of AWG 38Litz-wire with 300 strands. The parameters of every coil range from 20 to 22. Their parameters can be calculated [19–21]. We can compute the parameters in equations (2) and (1) by adopting the impedance analyzer. We set the primary resonant frequency as 85.0 kHz and the resistance of load as 15.8Ω. The distance of transmission equals 15 cm. Table 5 lists the resonant coils and their parameters. The receiver's travelling direction is denoted as Y axis. We simulated the mutual induction between Rx and Tx by ANSYS Maxwell and measured it by adopting an impedance analyzer. The simulated and calculated results of mutual induction are presented in Figure 9. It is easy to see that the mutual induction changes from 66.2 μH to 29.6 μH, while the misalignment is varied from 0 cm to 25 cm.

The start frequency is set as 76 kHz. Meanwhile, the WPT system works in a nonresonant condition as shown in Figure 11(a). However, when using this frequency-tracking algorithm, the system is in a resonance condition. It is found

Table 5: Detailed parameters of every coil.

Symbol	Value
L_1 (μH)	353.68
L_2 (μH)	216.02
C_1 (nF)	9.86
C_2 (nF)	16.09
R_1 (Ω)	0.438
R_2 (Ω)	0.281
f_0 (kHz)	85.0

that the input voltage has same phase with the input current, as presented in Figure 11(b). According to Figure 11b, we see that the resonant frequency is 77.56 kHz.

Figure 12 presents the output power as well as the DC-DC efficiency measured versus misalignments. From Figure 12(a), we can see that the efficiency is changed from 82.0% to 81.2% with frequency-tracking; whereas, the efficiency is changed from 81.0% to 75.4% with fixed frequency. The efficiency with frequency-tracking is nearly the same as that with fixed frequency when $\Delta = 25$ cm because the frequency at the highest efficiency point is equal to 85.298 kHz, which is close to 85 kHz. From Figure 12(b), we can see that the output power ranges from 33.2 W to 25.6 W when there is frequency tracking; the output power ranges from 33.2 W to 6.7 W when the frequency is fixed. Apparently, the efficiency of frequency tracking is greater than that of fixed frequency tracking. Meanwhile, the output power of frequency tracking is larger than that of fixed frequency. Interestingly, output power and efficiency in frequency-
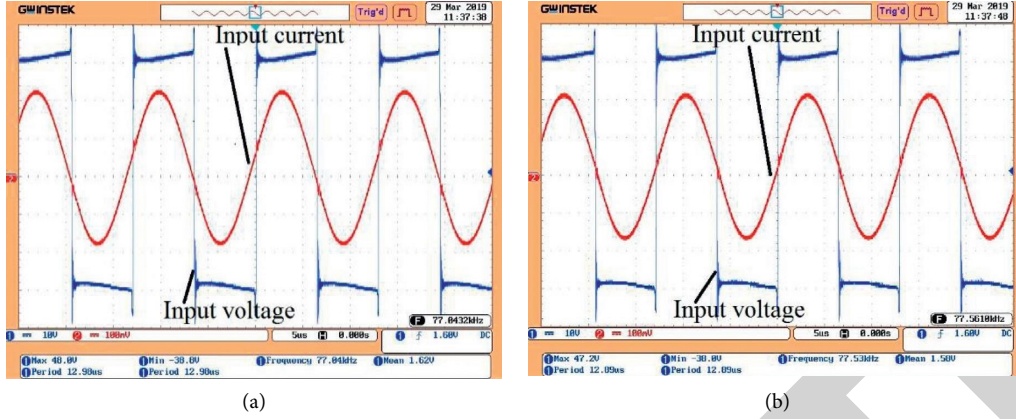
(a)

(b)

FIGURE 11: Input voltage and Input current with $\Delta = 0$ cm. (a) Input voltage and current without frequency-tracking algorithm. (b) Input voltage and current with frequency-tracking algorithm.
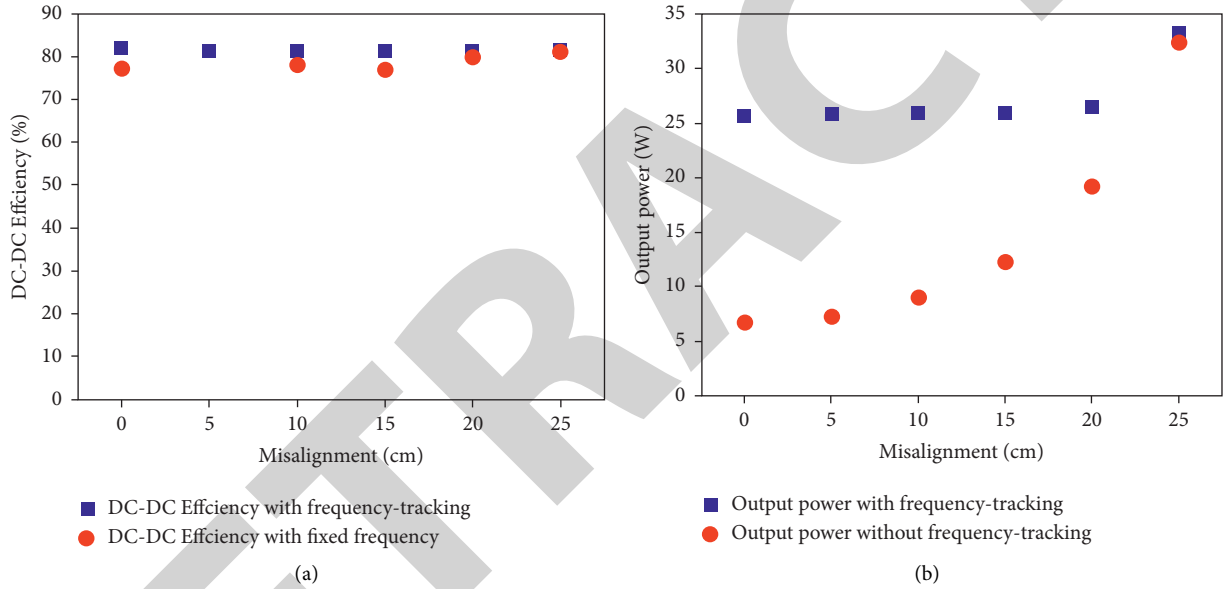

(a)

(b)

FIGURE 12: Measured efficiency and output power versus misalignment. (a) Measured DC-DC efficiency versus misalignment. (b) Measured output power versus misalignment.$V_{ref.}$

tracking method remain almost invariable as the misalignment changes from 0 to 20 cm. But in the presence of fixed frequency approach, output power varies greatly under the circumstance that the misalignment changes from 5 to 25 cm.

The reference voltage V_{ref} is given by the following equation:

$$\frac{V_{fil}}{V_{ref}} = G_v(s) = \frac{L_{sp}Ts^2 + (L_{sp} + TR_i)s + R_o}{L_{sp}Ts^2 + (L_{sp} + T + R_iT)s + R_o}$$

$$= 1 - \frac{Ts}{L_{sp}Ts^2 + (L_{sp} + T + R_iT)s + R_o}. \quad (14)$$

It is known that the magnitude of the virtual resistance and virtual inductance changes the pole distribution of the output transfer function, i.e., the adjustment of the virtual impedance. The output gain $G_{inv} = 1$ can be obtained and the inverter control parameters in the steady-state condition, but only determined by the reference voltage, so the output voltage can maintain good stability when the load condition is changed. Table 6 gives the virtual impedance parameters of resistive, inductive, and resistive inductance respectively in the industrial frequency state, according to which the step signal response can be obtained with the parameter.

To check the accuracy of results obtained by equations (7) and (12), the simulation is conducted. The result of simulation is presented in Figure 13. Figure 13(a) presents the characteristic angle of input impedance versus ω/ω_0 when the lateral misalignments are varied.

To verify the effectiveness of the algorithm, a system model of the voltage inverter FCS-MPC is built in this study, as listed in Table 7.

TABLE 6: Control parameters of different virtual impedances.

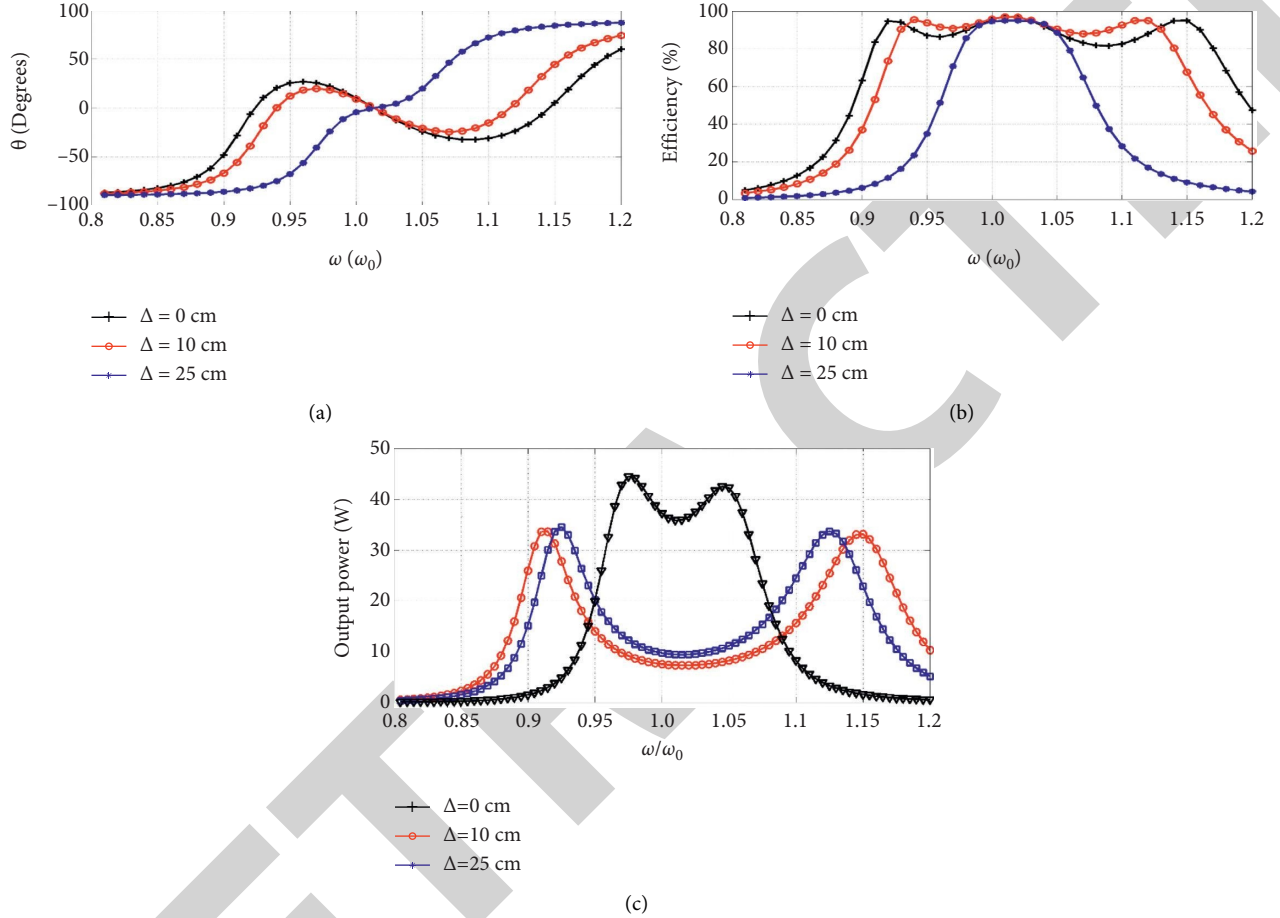| Output impedance	α	β	λ	T/ms	R_i/Ω	L_i/mH
Purely inductive	0.2	0.96	1.01	0.635	10	6.35
Purely resistive	1.26	−0.5	1.01	15.8	0.4	6.35
Resistive inductive	1	0.96	1.01	3.19	2	6.35

(a)

(b)

(c)

FIGURE 13: Input impedance characteristic angle, efficiency, and output power. (a) Characteristic angle of input impedance versus ω/ω_0. (b) Efficiency versus ω/ω_0. (c) Output power versus ω/ω_0.

TABLE 7: Model prediction controller parameters table.

Parameter name	Parameter value
DC voltage U_{dc}/V	520
Load counter-electromotive force e_o/V	100
Sampling time $T_s/\mu s$	50
Reference current i_o*/A	10/10-20
Load resistance R_o/Ω	0.1
Load inductance L_o/mH	20

The simulation results of the model predictive control system considering different scenarios for the steady state and transient cases at sampling time $T_s = 50\mu s$ are shown below. With delay time and compensation case, the objective function is $g_2 = |i_{o\alpha}^* (k+1) - i_{o\alpha}(k+1)| + |i_{o\beta}^*(k+1) - i_o(k+1)|$, $(i_{oa}, i_{ob}, i_{oc}) = 10\,A$, $R_{oa} = R_{ob} = R_{oc} = 0.1\Omega$, $L_{oa} = L_{ob} = L_{oc} = 20mH$, sampling time $T_s = 25\mu s$.

The CNN-based output-time voltage stability evaluation process can be divided into two phases, training and evaluation, as shown in Figure 14.

The training phase includes the following steps:

(1) Fully consider the key factors, develop a reasonable equivalence scheme, and scale down the studied AC-DC large system significantly with the same transient response characteristics to obtain the equivalence postsystem.

(2) A two-stage partitioning method based on the system structure and output-time voltage similarity is used to partition the AC-DC equivalent system, and each partition is subsequently evaluated separately for output-time voltage stability.

(3) Set different operation modes and fault scenarios, simulate the equivalent system in time domain to
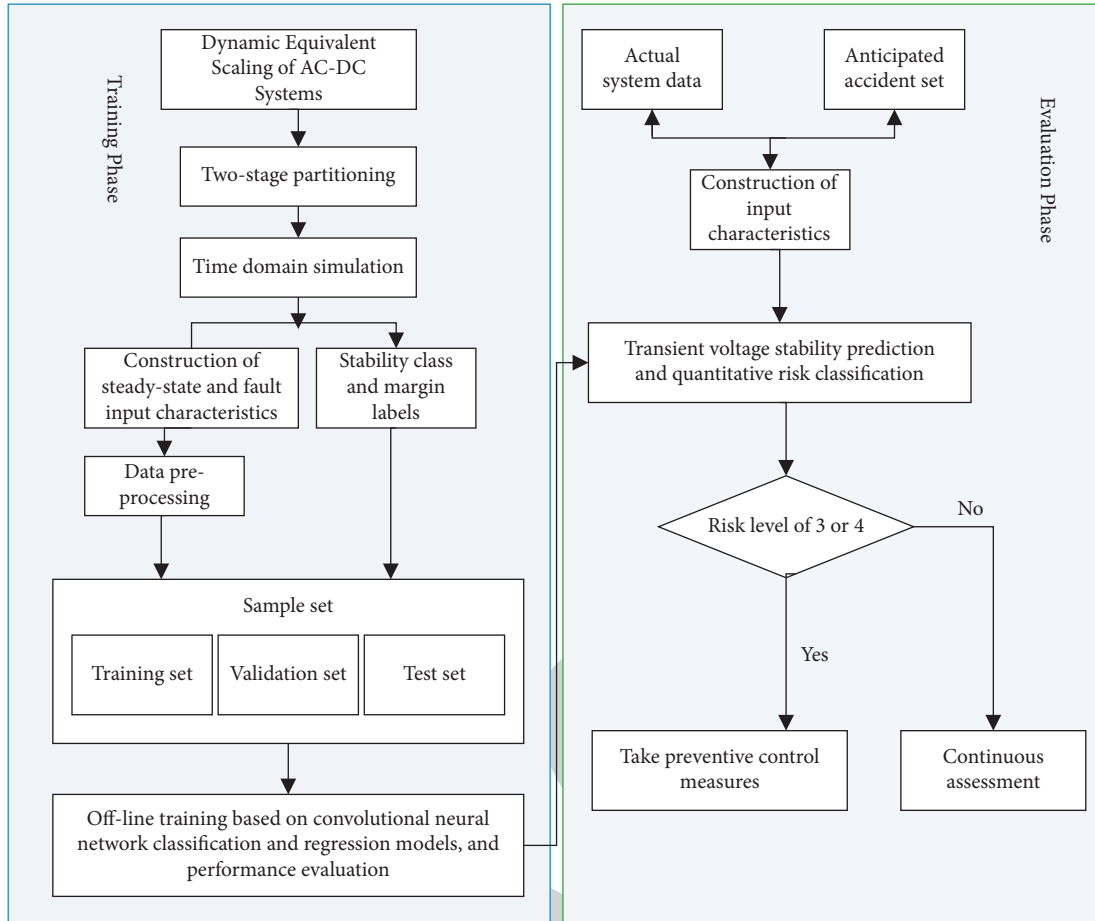
Figure 14: Voltage stability evaluation flow at output.

Table 8: Comparison of compensation voltage FFT and H-bridge equivalent switching frequency.

Modulation strategy	CPS-SPWM modulation	HPWM modulation
Compensation voltage THD (%)	0.43	1.33
Switching frequency	$3 \times 2k$	$2 \times 50 + 2k$

obtain the sample set, construct the input feature set based on the steady-state features and fault features, and carry out data normalization preprocessing; according to the basis for judging the voltage stability at output and the calculation results of the voltage stability margin at output, label the samples one by one to form two kinds of labels of stability category and margin.

(4) Generate CNN classification model and regression model corresponding to each partition, classify and predict the voltage stability at output and quantitative risk classification for the input samples, test the evaluation effect according to the evaluation index, and apply it to the evaluation if it meets the requirements.

Evaluation Stage. Steady-state features are obtained from actual system data, while a number of expected accident sets are generated to obtain fault features, which together constitute the input feature set and are fed into the CNN model of each partition obtained from training for output-time voltage stability prediction and quantitative risk grading evaluation. If the risk levels are 3 and 4, the scheduling and operation personnel are required to take preventive control measures in time to avoid serious damage to the system caused by voltage instability at output.

The equivalent switching frequencies of the compensated voltage FFT and H-bridge under CPS-SPWM modulation and HPWM modulation are compared in Table 8.

The load voltage can be stabilized at the target value after CHB-DVR compensation in the case of 30% drop in grid voltage within 0.2 to 0.4 s time.

5. Conclusion

The control strategy of CHB-DVR is a method for the design of the control loop as well as the steady-state and dynamic performance analysis, which is mainly responsible for the improvement of the response speed and compensation

accuracy of the DVR. In order to make the DVR device achieve the ideal compensation effect, its detection module should be sensitive and accurate enough to have a faster voltage tracking capability. The corresponding compensation strategy can be used to obtain a more accurate and appropriate compensation reference signal. The tracking performance of the DVR device for the compensation reference signal is determined by the control strategy adopted by the DVR, so the selection of a suitable control strategy can make the DVR device have a better compensation effect. The virtual impedance output voltage performance optimization method proposed in this study not only ensures the dynamic and steady-state characteristics but also improves the voltage waveform under nonlinear load conditions and suppresses high-frequency harmonics, which has obvious advantages over the general virtual impedance design method.

Data Availability

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

Conflicts of Interest

The author declares that there are no conflicts of interest.

Acknowledgments

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