Hindawi
Mobile Information Systems
Volume 2022, Article ID 8323322, 8 pages
https://doi.org/10.1155/2022/8323322

Research Article

Design and Performance Analysis of W-Band Low Noise Amplifier for RFIC-5G Mobile Systems

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Received 19 November 2021; Revised 31 May 2022; Accepted 7 July 2022; Published 21 August 2022

Academic Editor: Adrian Kliks

This paper presents a new approach of the design of a W-band low noise amplifier (LNA) in a 0.13 μm CMOS technology for narrowband and wideband applications. The proposed LNA utilizes input matching bandwidth extensions based on the source degeneration topology, and it is designed and optimized at a center frequency of 94 GHz and a supply voltage of 1.2 V. The obtained results exhibit a noise figure of 3 dB, a power gain of 32 dB, and a VSWR of 1.1. The design technique of this LNA is based on an agreeable tradeoff between the available gain of 30 dB and the noise figure of 3 dB, which leads to good bilateral stability and high linearity described by an input third-order intercept point of -17 dBm. A detailed performance analysis is presented and discussed along this paper. With the aim of a complete and robust integration, all lumped elements and transmission lines are integrated on a silicon PCB having $\varepsilon_r = 11.7$ and a dielectric loss $\text{Tan}\Delta = 0.001$ for low manufacturing costs. The prominent results of this LNA indicate that it is suitable for 94 GHz-image-radar and RFIC-5G mobile systems.

1. Introduction

During the past years, massive efforts have been made to obtain optimally designed radio-frequency integrated circuits (RFIC) operating at millimeter-wave bands, addressed to the wide range of 5G use cases and applications. The obtained results have motivated researchers to develop diverse 5G integrated-circuits with limited supply voltages (1-2 V) and ultra-low power consumption [1, 2]. In this context, the low noise amplifier (LNA) is a very important component in RFIC. This is the first block in a receiver whose primary function is to provide enough gain to overcome noise from subsequent blocks (such as the filter and the mixer), but not too much so as not to overload the mixer. In addition, LNA based on CMOS technologies should provide good linearity as demonstrated in [3, 4]. It should have also a specific impedance, conventionally 50 Ω, at the input source and at the output load. Moreover, LNA should provide low-power consumption especially for portable systems and 5G-enabled IoT devices [5, 6]. As W-band LNA applications, Li et al. [7] and Xue et al. [8] proposed various LNA structures for automotive radars.

For CMOS technologies [9], these new RFIC potentialities must be added to a series of useful RFICs on insulating silicon substrates despite the high permittivity of silicon ($\varepsilon_r \approx 11.7$ @ 94 GHz). Among these advantages, we can cite much lower substrate drain and substrate source diffusion capacities, better integration density, strong reduction in junction surfaces, and possibility of using high-resistive substrates to obtain passive devices (inductors) of high-quality factor. Moreover, the frequency performances and characteristics of CMOS devices have been continuously enhancing, and several RFIC/MMIC results using the CMOS technology operating in E/W-band have been published [10–14]. These prior LNAs have achieved acceptable performances but have been modest in terms of tradeoff between the gain and the noise figure (NF), as presented in [11], where $G = 14.2$ dB and NF = 6.3 dB. In our work, LNA is proposed with miniaturized RF inductors followed by microstrip-transmission-line input/output matching networks, as shown in the block diagram of Figure 1. The LNA core is composed of a cascode topology with a drain/source DC bias and stability circuits. The put/output matching networks are represented as a bandpass topology.

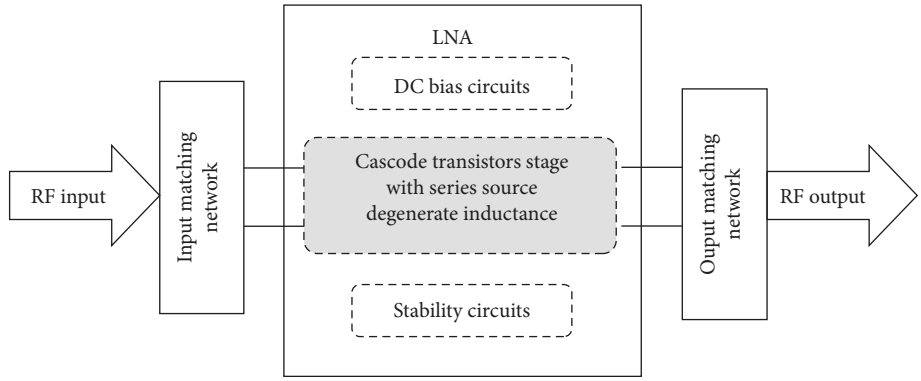

Figure 1: Block diagram of proposed W-band LNA.

The studied block is that LNA is the first element of the RF reception chain. In this context, the main aim of our work is to optimize the suggested model for low-power consumption with low-cost RF components for 94 GHz anti-collision radar. The application of the proposed LNA model is not limited only for 94 GHz systems but it is compatible to diverse applications over the W-band such as millimeter-wave radar [15] and radar targeting [16] search used for civilian [17, 18] and military purposes [19, 20], satellite communications [21, 22], and various military and civilian geo-tracking applications [23]. To improve these previous applications, the suggested LNA has advantages in terms of power consumption and gain with the NF cost. Moreover, this work gives a good tradeoff between the gain and NF with relatively high LNA linearity, like the results obtained by Li et al. in [24]. Besides, the input/output matching networks, device parameters, LC components, and biasing points have been designed to get the effective results. Thus, the proposed amplifier is designed with standard microelectronic procedures for low cost, all with the aim of achieving a good performance compared to prior research exposed in [3, 4, 11, 13, 14, 24, 25], as summarized in Subsection 5.4 of this manuscript.

This paper is structured as follows: Section 2 deals with the suggested LNA modeling and its design parameters. Section 3 gives polarization circuits with a DC/RF stopper and the corresponding LNA matching networks. Section 4 concludes the modeling and design techniques with the performance analysis of the proposed LNA. Section 5 exposes the obtained results and the discussion. Section 6 draws the conclusions presented as opportunities for research. Finally, all results are performed by Cadence and advanced design systems (ADS) simulators.

2. Proposed LNA Design

The most important step in designing LNA with the desired performances is the choice of the transistor. Various transistor topologies are available for LNA applications. In this context, the suitable transistor should be designated for a good tradeoff between the high gain (G) and the low NF. In practice, the operation frequency is crucial to limit the number of transistors. Figure 2 shows the electronic circuit of the integrated amplifier. The configuration used is a common source (T1) structure with inductive degeneration.

Before going to the presented analysis and techniques of the suggested LNA, it will be useful to first investigate the topology of the source degeneration cascode LNA, as explored in detail in [26, 27]. In general, the source degeneration LNA, represented by the series source inductor «L_s» of Figure 2, ensures bilateral stability, good input matching, and a low NF by utilizing L_s degeneration to realize 50-Ω input impedance, but without inducing resistive thermal noise.

This configuration presents a good compromise between NF, the gain, and the stability of LNA. The output load is by convention resistive 50 Ω tuned to the working frequency 94 GHz. The addition of a cascode stage (T2) guarantees the isolation between the output and the input of the stage, and it prevents any problem of instability at a high frequency. The input power adaptation is carried out thanks to inductors $L6$ and $L8$ which cancel the capacitive part Cin of the input impedance Z_{in} and adjust the real part of Z_{in} to the value of 50 Ω at the pulse working ω_0. At the output, the adaptation on a resistive load of 50 Ω is carried out by the capacitive divider C10–C13. The C8 and C10 capacitors prevent the stopper of the DC signal from dissipating in the RF generator. The role of the $L7$ inductor is to isolate the RF signal from DC. Inductors L_i ($i = 1, 2, 3, 4, 5, 10$) model, the interconnecting conductors; transmission lines (TL_i) ($i = 1, 2, 3, 4, 5, 6$) model, the package effect; and these lines are made up of distributed RLC elements where, $R = 0.880\,\text{n}\Omega$, $L = 1\,\text{nH}$ and $C = 1.6\,\text{pF}$. Resistors R_i ($i = 3, 4, 5$) are used to bias the NMOS transistors T1 and T2 and ensure the stability of the amplifier at the operating frequency. However, it should be noted that the power adaptation is necessary to ensure the maximum transfer of power from the source to the load. The supply voltage is fixed at 1 V.

There are several steps to follow the design of the RF amplifier [28]. First, choose the point of polarization without forgetting to isolate the DC signal and the RF signal from each other. Then, study the input/output stability of the transistor and stabilize it. If it is not already unconditionally stable, it must then choose a tradeoff between the available gain (G_a) and NF and find the input and output

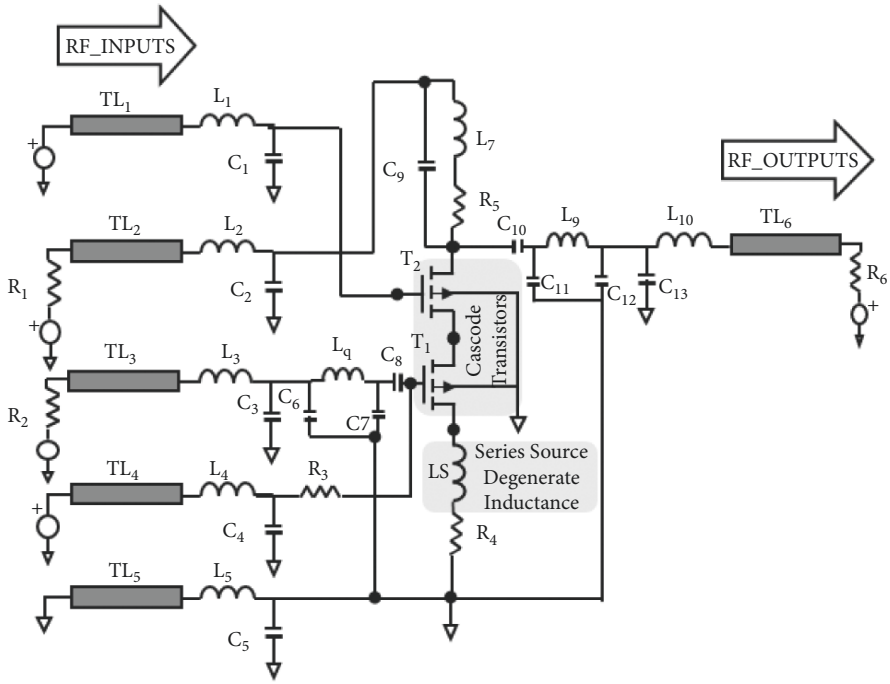

Figure 2: Topology of proposed LNA.

matching circuits that will achieve the desired performance. These steps lead to obtaining a mask for the final circuit.

3. Polarization and DC/RF Signal-Stopper Circuits

3.1. DC Bias and the Polarization Point. The problem of polarization is quite simple [28]. It is just to find Vgs which gives the transistor a bias current of 1.374 mA with VDS = 1.2 V. We use the complete electrical model of the transistor illustrated in Figure 3 for this DC simulation. Voltage Vgs is then 0.581 V.

3.2. RF/DC Signal Stopper. To avoid any loss of power of the RF signal, it must prevent this signal from going to dissipate in the polarization resistors of the gate and the drain. For this, we use $\lambda/4$ microstrip TL terminated by capacitors which must behave like a closed circuit at the operating frequency, as depicted in Figure 3.

The end of this TL will be seen as an open circuit at the input of $\lambda/4$ – TL. This TL must have a very large characteristic impedance compared to the impedance of the capacitor. By optimization, the width of this TL is equal to 152.4 μm and the capacitance is equal to 0.1 pF. According to the obtained results of the reflection coefficient S_{11} listed in Table 1, LNA is properly polarized at 94 GHz without lossless power.

4. Analysis and Design of Proposed LNA

4.1. Input Impedance. To facilitate the analysis of the LNA circuit, we take the assembly of Figure 4(a). This stage presents a common source amplifier with L_s inductance

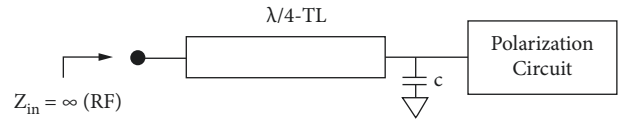

Figure 3: RF-signal stopper and DS-signal stopper.

Table 1: Reflection coefficient S_{11} at input of polarization circuits of the gate and the drain.

Frequency (GHz)	S_{11}, gate	S_{11}, drain
94	0.988/0.0008	0.993/0.0009

around of 1 nH, inserted between the source and the ground to control the real part of the input impedance. From Figure 4(b), we can extract all physical parameters related to the input impedance (Z_{in}) as follows:

$$\dot{V}x = \frac{\dot{I}x}{j\omega C_{gs}} + j\omega L_s\left(\dot{I}x + g_m\dot{V}gs\right). \tag{1}$$

From equation (1), the input impedance (Z_{in}) can be demonstrated as

$$\begin{aligned}\frac{\dot{V}x}{\dot{I}x} &= Z(j\omega)\\ &= \frac{1}{j\omega C_{gs}} + j\omega L_s + g_m\frac{L_s}{C_{gs}}.\end{aligned} \tag{2}$$

This impedance which is a series RLC-network is proportional to the value of the inductance LS. It is important to consider that this L_s inductor does not bring thermal noise back to the amplifier circuit because a pure reactance is noise

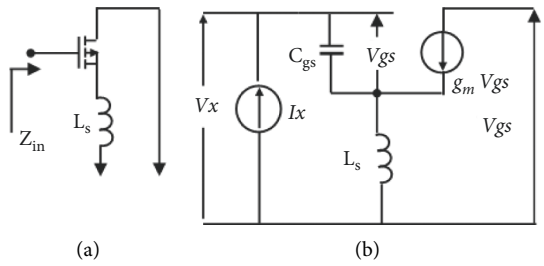

Figure 4: (a) A circuit with inductor (LS) at the LNA-Source, (b) an equivalent electronic model.

free. This impedance is then purely resistive at a single frequency (at resonance). However, this method can be used in circuits operating at a narrow band.

4.2. Input Matching Network. In order to maximize the performance of the circuit and ensure a maximum power transfer from the input-source to load (ZL), it is necessary to design a matching network to match the output impedance of the source-RF-generator (Z_g) to the input impedance (Z_{in}) of LNA, where $Z_g = Z_{\text{in}}^*$ and $Z_g = R_s$. To achieve this task: (i) we create an impedance of 50 Ω, and (ii) design a resonant circuit with inductance L_s and capacitance C_{gs} at the resonant frequency 94 GHz. It is often difficult to obtain resonance with these two elements. For this, we add inductance L_g, as shown in Figure 5.

To obtain an impedance of 50 Ω, a fine tuning can be introduced on inductance L_g.

Let us now consider the circuit presented by Figure 6 with the presence of source V. Therefore, we can write as

$$v = v_{gs} + g_m v_{gs} Z. \tag{3}$$

That gives

$$v_{gs} = \frac{v}{1 + g_m Z}, \tag{4}$$

$$\begin{aligned} i_{\text{out}} &= g_m v_{gs} \\ &= \frac{g_m}{1 + g_m Z} v. \end{aligned} \tag{5}$$

Using expression equation (2) and Figure 6(b), we can write as

$$Z_{in} = \frac{1}{C_{gs} \cdot j\omega} + j\omega L_s + \omega_T L_s, \tag{6}$$

where $\omega_T = g_m / C_{gs}$.

Suppose now that the resonance is completed by L_g and L_s, then we get

$$1 - \omega_0^2 \left(L_g + L_s\right) C_{gs} \approx 1 - L_g C_{gs} \omega_0^2 = 0, \tag{7}$$

$$\omega_0 \approx \frac{1}{\sqrt{\left(L_g + L_s\right) C_{gs}}}. \tag{8}$$

We can neglect term $-L_g C_{gs} \omega_0^2$, so we directly obtain the gain of the LNA circuit:

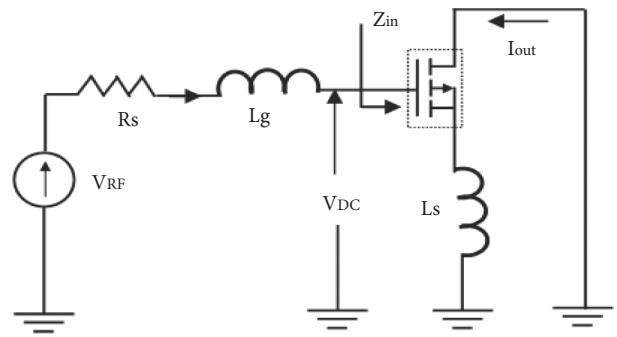

Figure 5: Input matching network.

$$G_m(j\omega_0) = \frac{g_m}{j\omega_0 C_{gs}\left(R_s + \omega_T L_s\right)}. \tag{9}$$

4.3. NF Analysis. After ensuring the maximum transfer of power from the source-RF-generator to the load, it is essential to evaluate the NF of the circuit. To calculate this parameter, it must evaluate the current at the output of the circuit, while assuming that there is a short circuit at the output of LNA. To achieve this, it must determine the transfer function (transconductance) from the input to the output of the circuit at the resonant frequency which is set at 94 GHz in the spectral (frequency) domain. From equation (9), we can define the function of the spectral density function (SDF). For the resistance ($R_s = Z_g$) and in terms of voltage, the spectral density is

$$\frac{\overline{v}_s^2}{\Delta f} = 4k\text{TR}_s. \tag{10}$$

By multiplying this expression (SDF) by the squared transconductance, we obtain the first component of the SDF in terms of output-current such that we get

$$\frac{\overline{i}_{o1}^2}{\Delta f} = \frac{4kT}{R_s}\left(\frac{\omega_T}{\omega_0}\right)^2 \frac{1}{\left(1 + \omega_T L_s / R_s\right)^2}. \tag{11}$$

Gate-current (io1) can be analyzed using Figures 6(a)–6(b). Then, gate-current (io1) can be expressed as

$$\frac{\overline{i}_{o1}^2}{\Delta f} = 4kT\delta g_g\left(1 - |c|^2\right). \tag{12}$$

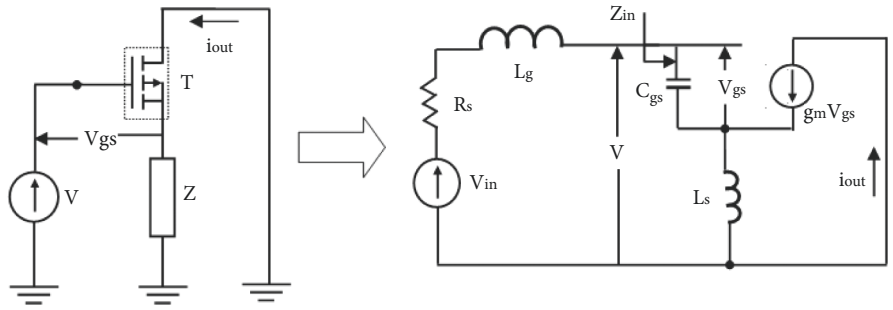

Figure 6: Analytical circuits of the matching network.

This expression shows us that there is a relation between the output-current component (io2) and the gate-current (i_g), which can be written as follows:

$$io2\left\{1+\frac{gmL_s(j\omega)}{C_{cs}(j\omega)\left[R_s+(j\omega)\left(L_g+L_s\right)\right]}\right\} = i_{gu}\frac{g_m}{(j\omega)C_{gs}}\frac{R_s+(j\omega)\left(L_g+L_s\right)}{R_s+(j\omega)\left(L_g+L_s\right)+1/(j\omega)C_{gs}}. \tag{13}$$

From this equality, the spectral density of the current at output (io2) can be expressed as follows:

$$\frac{\overline{i}_{o2}^2}{\Delta f}=\frac{\overline{i}_{gu}^2}{\Delta f}\frac{1}{\left(1+\omega_T L_s/R_s\right)^2}\left(\frac{\omega_T}{\omega_0}\right)\left(1+Q_L^2\right), \tag{14}$$

with $\mathrm{QL}=(L_g+L_s)\omega_0/R_s=1/\omega_0 R_s C_{gs}$ and $g_g=\omega_0^2 C_{gs}^2/5g_{d0}$.

Using the circuit illustrated by Figure 7, we can determine the noise which accompanies the current of drain (id) with SDF using equation (10):

$$\frac{\overline{i}_d^2}{\Delta f}=4kT\gamma g_{d0}. \tag{15}$$

The current at output (io2) of the transistor can be expressed as follows:

$$\frac{i_{ot}^2}{\Delta f}=\frac{4kT\eta\gamma g_{do}}{\left(1+\omega_T L_s/R_s\right)^2}, \tag{16}$$

where

$$\begin{aligned}\eta &= \kappa+\xi\\ &= 1+2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}+\frac{\delta\alpha^2}{5\gamma}\left(1+Q_L^2\right),\\ \kappa &= \frac{\delta\alpha^2}{5\gamma}|c|^2+\left(1+|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right)^2,\\ \xi &= \frac{\delta\alpha^2}{5\gamma}\left(1-|c|^2\right)\left(1+Q_L^2\right),\\ \alpha &= \frac{g_m}{g_{do}}.\end{aligned} \tag{17}$$

Finally, the NF of the proposed LNA circuit can be expressed as

$$\mathrm{NF}=1+\eta\gamma g_{do}R_s\left(\frac{\omega_o}{\omega_T}\right)^2. \tag{18}$$

5. Results and Discussion

5.1. S-Parameters and Gains. LNA is characterized by its S-parameters [29, 30], such that S_{11} and S_{22} give us the amounts of signals reflected at the input/output port. S_{21} indicates the signal transmission coefficient from the input to the output of the LNA amplifier. It also represents the gain of the amplifier at the operating frequency, after adaptation. S_{12} indicates the signal transmission coefficient from the output to the input of the LNA amplifier, and is also considered as inverse gain (S_{12}). Figure 8 shows the simulation results of the S parameters. The reflection at input S_{11} is −14.75 dB, the reflection at output S_{22} is −19 dB, and the inverse gain (S_{12}) is −34 dB and the forward gain (S_{21}) is 32 dB at 94 GHz.

These S-parameter results are rigorous enough to achieve the desired performance of LNA and confirm well that the proposed LNA is bilaterally stable and matched at frequencies between 90 and 100 GHz. However, the value of S_{22} can be improved by making a fine tuning to the value of the load (ZL) at the output of LNA.

5.2. NF. NF varies as a function of the RF-generator impedances ($R_s = Z_g$) and has a minimum NF min for an admittance called optimal (Y_{opt} or G_{opt}). Figure 9 illustrates the NF of the suggested LNA and that for a frequency range from 90 GHz to 100 GHz, with an operating frequency of 94 GHz, where NF = 3 dB.

5.3. Third-Order Input Intercept Point. The third-order input intercept point (IIP3) is a very important parameter to evaluate the performance of LNA. It also determines the non-linearity of the amplifier. Figure 10 shows that the value of IIP3 at a 94-GHz operating frequency is −16.78 dB.

5.4. Comparison Results. The performance summary and the comparison results with other state of the art W-band LNA in silicon-based technologies are shown in Table 2. It can be

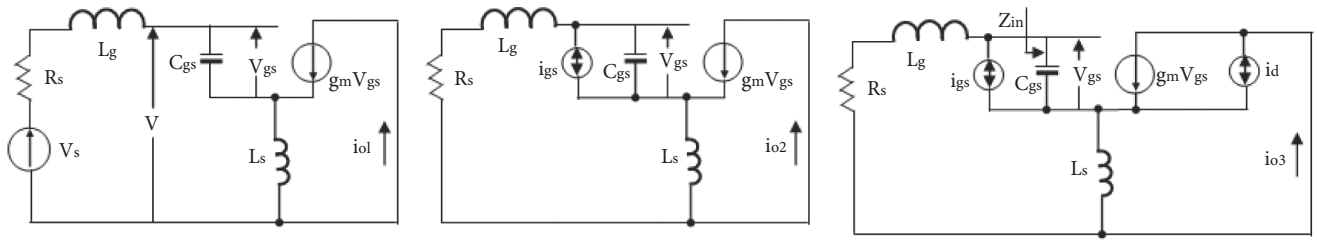

Figure 7: Analytical circuits of NF evaluation.

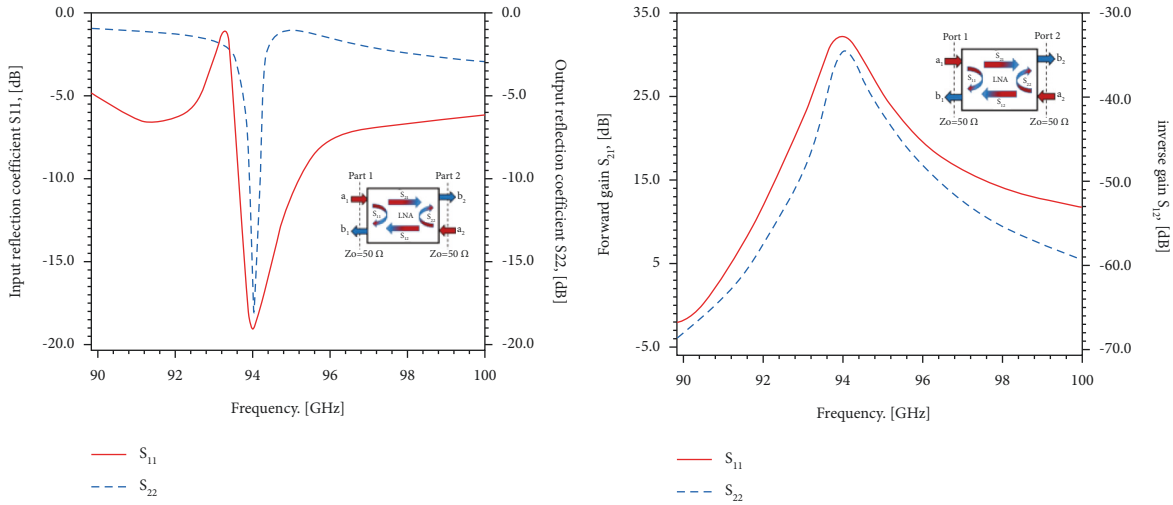

Figure 8: S-parameters of proposed LNA, (a) input/output reflection coefficients (S_{11} and S_{22}), (b) forward gain (S_{21}) and inverse gain (S_{12}).

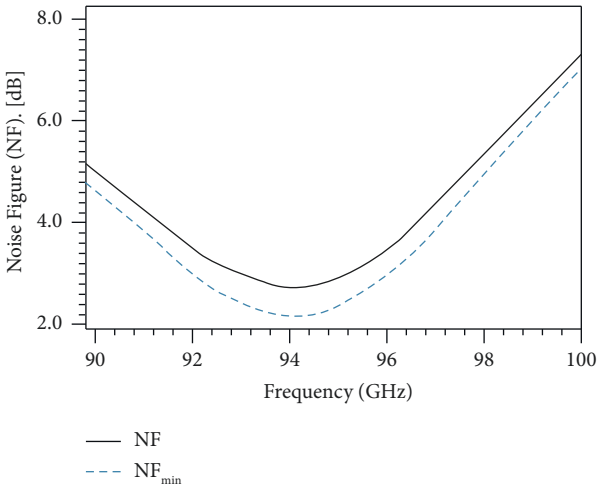

Figure 9: NF simulation.

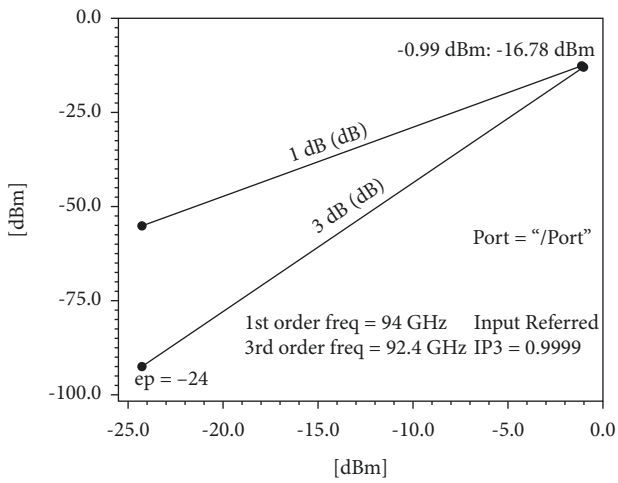

Figure 10: Third-order input intercept point (IIP3).

seen that our work accomplishes a high gain, a required NF, and a competitive linearity at the same time. The figure of merit (FoM) is calculated and simulated as mentioned by equation (3) [3]. Moreover, the obtained results are very promising for active RF devices over the W-band (from 75 GHz to 300 GHz) where ultra-large bands are needed.

Table 2: Performance comparison of proposed LNA with existing LNAs operating in silicon-based technologies (post-simulation results).

Ref.	[24] 2021	[25] 2021	[3] 2020	[11] 2019	[4] 2018	[13] 2017	[14] 2016	This work
F_0 (GHz)	78	77	92	77	73.5	77.5	78	94
Gain (dB)	21.3	32	18.2	14.2	20	18.5	15	32
NF (dB)	5.5	11.8	5.8	6.3	4	5.5	7.4	3
IIP3 (dBm)	-14.5	-8	-27.4	-10	-22.8	-15	-30	-16.7
P_{DC} (mW)	52	32.4	16	33.5	10.8	27	7.2	19
FoM	-	-	15	0.14	16.1	11.3	1.88	7.3

6. Conclusion

A new approach of modeling and designing W-band LNA in silicon-based technologies has been presented in this paper. The suggested LNA design provides good performances and results compared with the existing work. Biasing point, stability, and matching network components have been designed to obtain better results at a 94-GHz frequency. A tradeoff between the gain and NF have been improved as 32 dB and 3 dB, respectively. Input/output return losses (S_{11} and S_{22}) are less than −13 dB. Thus, this LNA exhibits a high linearity of −16.78 dBm at 94 GHz and good stability. In future work, power consumption can be reduced. The proposed model can be a good candidate for 5G-RFIC mobile systems.

Data Availability

The data that support the findings of this study are available from the author upon reasonable request.

Conflicts of Interest

The author declares that there are no conflicts of interest.

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