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Research Article

Modeling and Simulation of Ultra-Wideband Communication Receiver Based on Balanced Sampling and Integrating Circuit

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In order to solve the problem of extracting signals from impulse radio ultra-wideband (IR-UWB) receivers in a low signal-to-noise ratio (SNR) environment, this paper uses circuit transient analysis to establish a mathematical model of an ultra-wideband wireless communication receiver based on a balanced sampling and integration circuit (BSIC). The effect of receiver circuit component parameters on the output signal is simulated and tested, and the optimization of circuit component parameters for UWB wireless communication receivers is achieved. The sampling capacitance in the receiver circuit ranges from 1 pF to 6 pF, depending on the 200 ps pulse width. The output signal amplitude increases as the sampling capacitance increases. The range of integral capacitance is from 2.5 pF to 25 pF, which is based on a 100 ns interval between two pulses. The output signal amplitude decreases as the integration capacitance increases and the signal waveform becomes better as the integration capacitance increases. The effect of SNR from 0 to −30 dB on the receiver output is simulated, and the results show that the Bit Error Ratio (BER) of the receiver is less than 10^{-3} when the SNR is greater than −15 dB. The simulation and test results show that the model developed in this paper is useful as a guide for optimizing the receiver parameters at low SNR.

1. Introduction

Impulse radio ultra-wideband (IR-UWB) has high application value in the Internet of Things (IoT) and wireless communications [1–3], and IR-UWB technology has been widely used in short-range communications, positioning, and radars [4, 5].

Receiver is the basis for the realization of IR-UWB technology. At present, there are many types of IR-UWB signal receiver. In [6–9], there are incoherent energy detection receivers for the additive Gaussian white noise channel environment and matched filter receivers for correlated reception. In [10, 11], there are RAKE receivers consisting of multiple parallel correlators for complex multipath channel environments and transmission reference (TR) receivers [12–15], which do not require complex channel estimation compared to RAKE receivers. In [16–21], the structure of the low-noise amplifier (LAN) is optimized to improve the gain of the LAN and reduce the noise so as to improve the data speed of the receiver and reduce the bit error rate (BER). In [22–25], the algorithm of analog-to-digital converter (ADC) is optimized to reduce the bit error rate of the receiver. These improvements can effectively reduce the BER of UWB receiver, and the data speed can reach 100 Mbps to 1 Gbps. And in [10, 12, 13, 20, 24], the effect of the environment on UWB receivers has been studied. However, most of these studies are carried out in high signal-to-noise ratio (SNR) environment, which has poor antinoise ability.

The balanced sampling and integration circuit (BSIC) [26] is a simple and low-complexity circuit for recovering rapidly changing weak signals that are drowning in noise. The difference between this receiver and other receivers is the different position of the amplifier. In other receivers, the received signal is first processed by LNA and then by energy detection or correlator. In contrast, sampling and integration receivers process the received signal before amplification by an amplifier, which reduces the amplifier requirements.

In order to enhance the anti-interference ability of UWB receiver, the circuit in [26] is improved by adding two resistors, so it is necessary to establish a new model of the receiving circuit. This article mainly adopts the circuit

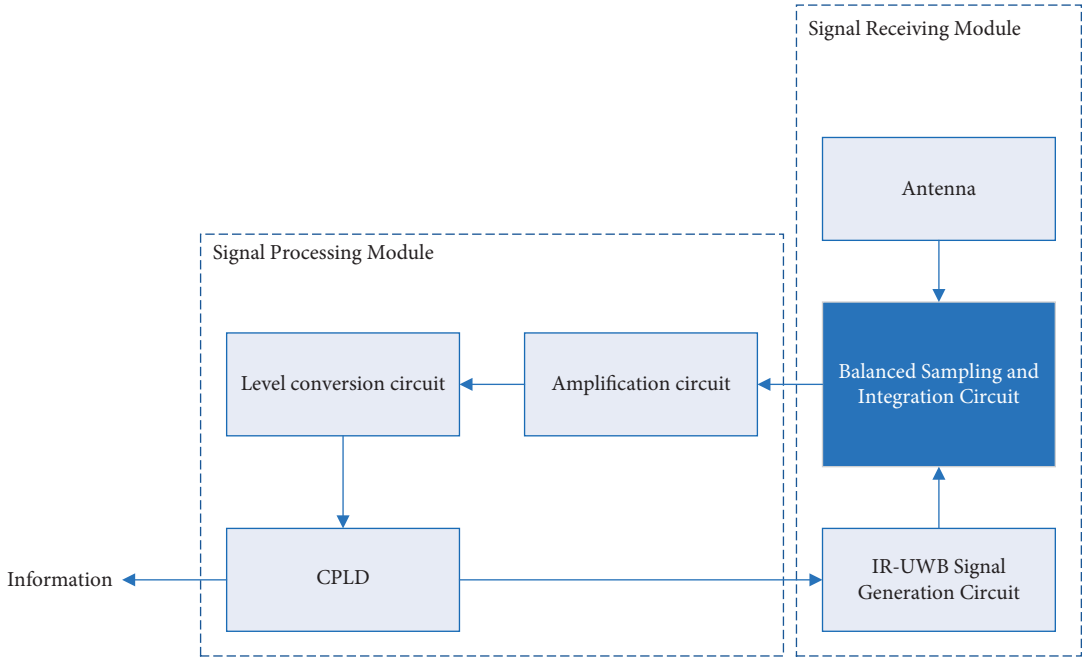


Figure 1: Block diagram of the IR-UWB receiver.

transient analysis method to establish the mathematical model of the UWB wireless communication receiver and obtain the receiver output signal expression through Laplace transform. The influence of receiver circuit component parameters on the output signal is studied, and the circuit component parameters of IR-UWB wireless communication receiver are optimized. The influence of different SNR on the output signal of receiver is studied by simulation.

The paper is structured in the following sections: Section 2 establishes the receiver model. Section 3 introduces simulation and measurement methods. Section 4 presents and discusses simulation and measured results. Section 5 describes the summary and future work of this article.

2. IR-UWB Receiver Modeling

In this section, an IR-UWB wireless communication receiver using a BSIC to achieve correlation calculations between sampling pulses and received signals is studied. The IR-UWB receiver block diagram is shown in Figure 1. The receiver consists of two parts, the signal receiving module and the signal processing module. The signal receiving module consists of an antenna, a BSIC, and an IR-UWB signal generation circuit. The signal processing module consists of an amplifier circuit, a level conversion circuit and a CPLD. Signal capture and decoding are performed on the CPLD.

The BSIC in IR-UWB wireless communication receiver is shown in Figure 2, which is composed of three parts: a sampling circuit, an integration circuit, and a high-pass filter circuit. The circuit in Figure 2 is an improvement on [26]. Resistors R_2 and R_3 in Figure 2 have been added to increase the anti-interference capability of the circuit.

The sampling circuit is composed of sampling capacitors C_1, C_2, diodes D_1, D_2, and resistance R_1, and the sampling pulse is U_p. The exponential integrating circuit is composed of integrating capacitors C_3, C_4 and resistors R_4, R_5. The high-pass filter circuit is composed of filter capacitors C_5, C_6 and resistors R_6, R_7. The input signal of the IR-UWB wireless communication receiver is the signal received by the antenna. Diode conduction is controlled by sampling pulse, and input signal is sampled by the sampling capacitor. The sampling values are integrated by capacitors C_3 and C_4 after the diodes are cut off. The low-frequency part of the integrated signal is filtered out by capacitors C_5 and C_6, and the signal is input to the differential amplifier. After multiple sampling periods, the output signal of the IR-UWB wireless communication receiver can be obtained.

2.1. Circuit Model of Sampling Process of IR-UWB Communication Receiver. According to the two different working states of IR-UWB communication receiver, the sampling process and the integration process, the mathematical models of the two working stages are established in one signal period.

The sampling process is the process in which IR-UWB wireless communication receiving circuit samples the input signal after the sampling pulse conducting the diodes D_1 and D_2. The resistors R_1, R_2, and R_3 are connected in parallel with an equivalent resistance of R_q when the diode is conducting. The circuit in the sampling process is shown in Figure 3. And ignore the effect of conduction diode resistors, because the resistors value of diode conduction is much smaller than R_1, R_2, and R_3.

R_q in the figure is

$$R_q = R_1//R_2//R_3 = \frac{R_1R_2R_3}{R_2R_3 + R_1R_3 + R_1R_2}. \quad (1)$$

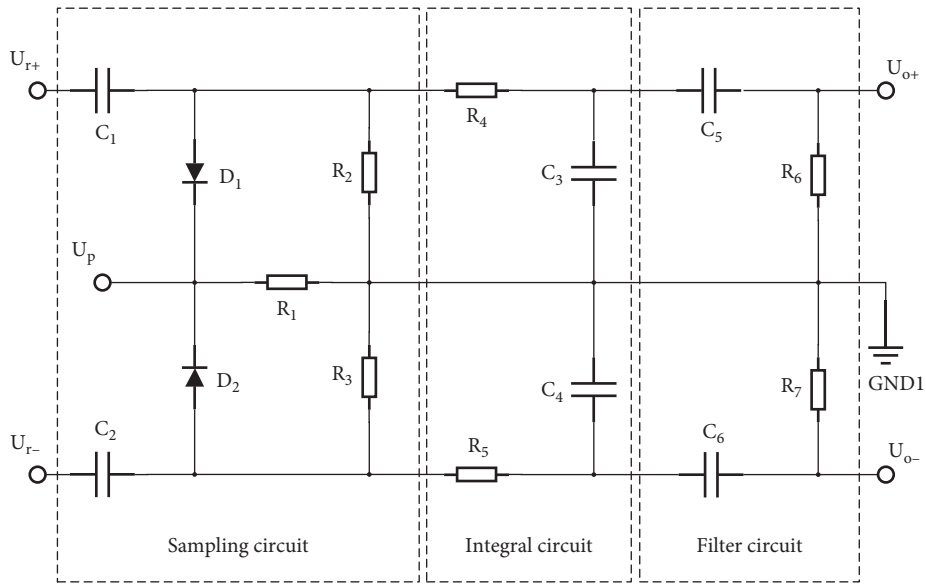


Figure 2: IR-UWB receiver circuit schematic diagram.

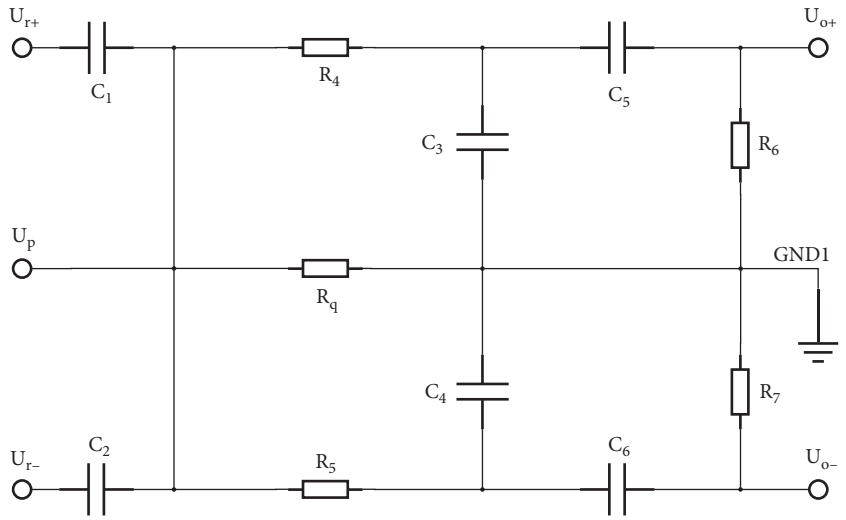


Figure 3: Equivalent circuit diagram of sampling process.

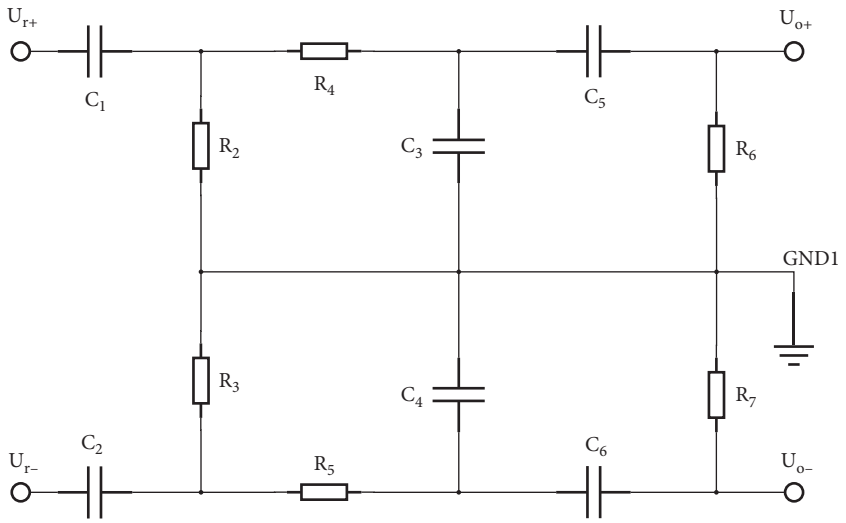


Figure 4: Equivalent circuit diagram of integration process.

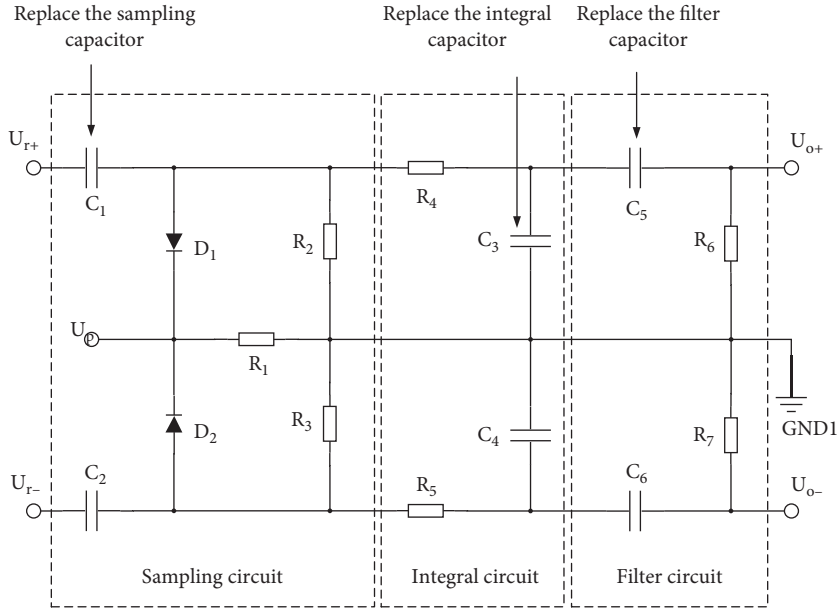


Figure 5: Circuit simulation and measurement principle block diagram.

Since the upper and lower parts of the BSIC have the same circuit principles, this article only elaborates on the derivation process of the upper part of the circuit model.

In the nth period, the initial states of C_1, C_3, and C_5 are assumed to be u_{n1}, u_{n3}, and u_{n5}, respectively, when the diode is conduction. According to Kirchhoff's voltage law, the simplified circuit model from Figure 3 is shown below.

$$\begin{cases} u_{r+} = u_1 + R_q\left(C_1\dfrac{du_1}{dt} - C_3\dfrac{du_3}{dt} - C_5\dfrac{du_5}{dt}\right) + u_p, \\ u_{r+} = u_1 + R_4\left(C_3\dfrac{du_3}{dt} + C_5\dfrac{du_5}{dt}\right) + u_3, \\ u_3 = u_5 + R_6C_5\dfrac{du_5}{dt}. \end{cases} \tag{2}$$

Because the frequency of the received UWB signal is on the order of GB, the parameters of the upper part of the circuit in Figure 3 satisfy $R_6 \gg R_4 \gg R_q$, $[R_4 + (R_6 + 1/j\omega C_5)//1/j\omega C_3] \gg R_q$, and $R_6 + 1/j\omega C_5 \gg 1/j\omega C_3$. So $i_{C_1} \gg i_{C_3} \gg i_{C_5}$; then, the system of equations (2) can be simplified to

$$\begin{cases} u_{r+} = u_1 + R_qC_1\dfrac{du_1}{dt} + u_p, \\ u_{r+} = u_1 + R_4C_3\dfrac{du_3}{dt} + u_3, \\ u_3 = u_5 + R_6C_5\dfrac{du_5}{dt}. \end{cases} \tag{3}$$

Perform Laplace transform on the system of equations (3), and perform inverse Laplace transform on the equations to get $u_1(t)$, $u_3(t)$, and $u_5(t)$ as follows:

$$\begin{aligned} u_1(t) &= \left(u_{n1} - u_{r+} + u_p\right)e^{-\left(t/R_qC_1\right)} + u_{r+} - u_p, \\ u_3(t) &= u_{n3}e^{-\left(t/R_4C_3\right)} + u_p\left(1 - e^{-\left(t/R_4C_3\right)}\right) \\ &\quad - \frac{R_qC_1}{R_qC_1 - R_4C_3}\left(u_{n1} - u_{r-} + u_p\right)\left(e^{-\left(t/R_qC_1\right)} - e^{-\left(t/R_4C_3\right)}\right), \\ u_5(t) &= u_{n5}e^{-\left(t/R_6C_5\right)} - \frac{u_{n3}R_4C_3}{R_4C_3 - R_6C_5}\left(e^{-\left(t/R_4C_3\right)} - e^{-\left(t/R_6C_5\right)}\right), \\ &\quad + u_p\left(1 - e^{-\left(t/R_6C_5\right)}\right) - \frac{u_pR_4C_3}{R_4C_3 - R_6C_5}\left(e^{-\left(t/R_4C_3\right)} - e^{-\left(t/R_6C_5\right)}\right), \\ &\quad - \frac{R_qC_1}{R_qC_1 - R_4C_3}\left(u_{n1} - u_{r+} + u_p\right) \\ &\quad \cdot \left[\frac{R_qC_1}{R_qC_1 - R_6C_5}\left(e^{-\left(t/R_qC_1\right)} - e^{-\left(t/R_6C_5\right)}\right)\right. \\ &\quad \left. - \frac{R_4C_3}{R_4C_3 - R_6C_5}\left(e^{-\left(t/R_4C_3\right)} - e^{-\left(t/R_6C_5\right)}\right)\right]. \end{aligned} \tag{4}$$

As shown in Figure 3, the upper part and the lower part of the BSIC are symmetrical. Assume that the initial states of the capacitors C_2, C_4, and C_6 during diode conduction are u_{n2}, u_{n4}, and u_{n6}, respectively. Similarly, the solutions of $u_2(t)$, $u_4(t)$, and $u_6(t)$ can be obtained as follows:

$$
\begin{aligned}
u_2(t) &= \left(u_{n2} - u_{r-} + u_p\right)e^{-\left(t/R_qC_2\right)} + u_{r-} - u_p,\\
u_4(t) &= u_{n4}e^{-\left(t/R_5C_4\right)} + u_p\left(1 - e^{-\left(t/R_5C_4\right)}\right),\\
&\quad - \frac{R_qC_2}{R_qC_2 - R_5C_4}\left(u_{n2} - u_{r-} + u_p\right)\left(e^{-\left(t/R_qC_2\right)} - e^{-\left(t/R_5C_4\right)}\right),\\
u_6(t) &= u_{n5}e^{-\left(t/R_7C_6\right)} - \frac{u_{n4}R_5C_4}{R_5C_4 - R_7C_6}\left(e^{-\left(t/R_5C_4\right)} - e^{-\left(t/R_7C_6\right)}\right)\\
&\quad + u_p\left(1 - e^{-\left(t/R_7C_6\right)}\right),\\
&\quad - \frac{u_pR_5C_4}{R_5C_4 - R_7C_6}\left(e^{-\left(t/R_5C_4\right)} - e^{-\left(t/R_7C_6\right)}\right)\\
&\quad - \frac{R_qC_2}{R_qC_2 - R_5C_4}\left(u_{n2} - u_{r-} + u_p\right),\\
&\quad \cdot \left[\frac{R_qC_2}{R_qC_2 - R_7C_6}\left(e^{-\left(t/R_qC_2\right)} - e^{-\left(t/R_7C_6\right)}\right)\right.\\
&\quad \left. - \frac{R_5C_4}{R_5C_4 - R_7C_6}\left(e^{-\left(t/R_5C_4\right)} - e^{-\left(t/R_7C_6\right)}\right)\right].
\end{aligned}
\tag{5}
$$

2.2. Circuit Model of Integration Process of IR-UWB Communication Receiver. At the interval between two sampling pulses, diodes D_1 and D_2 are cut off, and the input signal of the receiving circuit sampled by the sampling capacitors C_1 and C_2 is transferred to the integrating capacitors C_3 and C_4. After multiple sampling cycles, the integration process of the input signal of the receiving circuit is completed, and the low-frequency part of the signal is filtered out by the high-pass filter circuit. The equivalent circuit diagram is shown in Figure 4.

When the diode is cut off in the nth cycle, the initial states of the capacitors C_1, C_3, and C_5 in the upper half of the circuit are u_{n1}', u_{n3}', and u_{n5}', respectively. The equations can be obtained from the equivalent circuit diagram in Figure 4.

$$
\begin{cases}
u_{r+} = u_1 + R_2\left(C_1\dfrac{du_1}{dt} - C_3\dfrac{du_3}{dt} - C_5\dfrac{du_5}{dt}\right),\\
u_{r+} = u_1 + R_4\left(C_3\dfrac{du_3}{dt} + C_5\dfrac{du_5}{dt}\right) + u_3,\\
u_3 = u_5 + R_6C_5\dfrac{du_5}{dt}.
\end{cases}
\tag{6}
$$

For $i_{C_3} \gg i_{C_5}$, therefore, C_5du_5/dt in the first two equations can be ignored. So, the solution of the equation system can be simplified to

$$
\begin{aligned}
u_1(s) &= \frac{C_3R_4C_1R_2s^2u_{n1}' + C_3R_2\left(u_{r+} - u_{n3}'\right)s + u_{r+}}{\left(C_1R_4C_3R_2s^2 + C_3R_2s + 1\right)s},\\
u_3(s) &= \frac{C_3R_2u_{n3}'\left(R_4C_1s + 1\right) + C_1R_2u_{r+}}{C_3R_4R_2C_1s^2 + C_3R_2s + 1},\\
u_5(s) &= \frac{C_5R_6u_{n5}'\left(C_1R_2C_3R_4s^2 + C_3R_2s + 1\right)}{\left(C_5R_6s + 1\right)\left(C_3R_4C_1R_2s^2 + C_3R_2s + 1\right)}.
\end{aligned}
\tag{7}
$$

The result of the inverse Laplace transforms of the simplified $u_1(t)$, $u_3(t)$, and $u_5(t)$ can be obtained as follows:

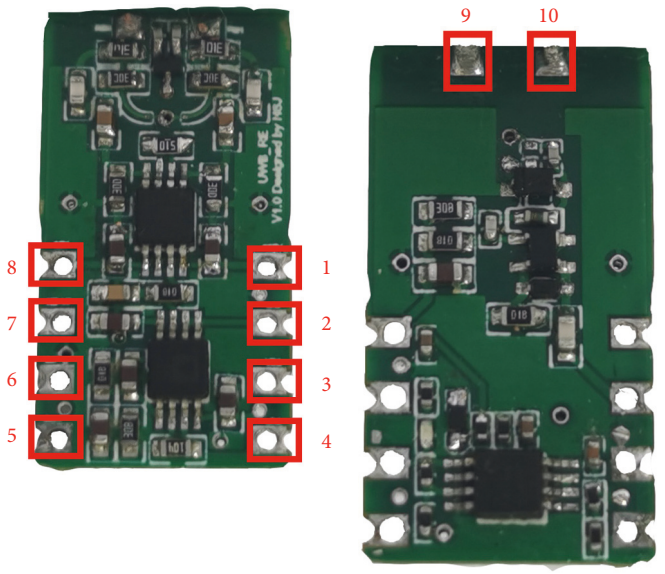
$$
\begin{aligned}
u_1(t) &= u_{r+} + e^{-\left(t/2R_4C_1\right)}\left[\left(u_{n1}' - u_{r+}\right)\cosh\left(\frac{\alpha}{R_4C_1}t\right)\right.\\
&\quad \left. - \frac{2}{\alpha}\left(u_{n3}' + u_{n1}' - u_{r+}\right)\sinh\left(\frac{\alpha}{R_4C_1}t\right)\right],\\
u_3(t) &= u_{r+} + \left(u_{n3}' - u_{r+}\right)e^{-\left(t/2R_4C_1\right)}\\
&\quad \cdot \left[\cosh\left(\frac{\alpha}{R_4C_1}t\right) + \frac{1}{2\alpha}\sinh\left(\frac{\alpha}{R_4C_1}t\right)\right],\\
u_5(t) &= u_{n5}'e^{-\left(t/R_6C_5\right)}.
\end{aligned}
\tag{8}
$$

where $\alpha = \sqrt{(R_2C_3 - 4R_4C_1)/4R_2C_3}$.

As shown in the equivalent circuit diagram of the integration process of the receiving circuit in Figure 3, the upper and lower parts of the circuit are symmetrical during the integration process of the BSIC. In the same way, suppose the initial states of the capacitors C_2, C_4, and C_6 are u_{n2}', u_{n4}', and u_{n6}', respectively, and the results of $u_2(t)$, $u_4(t)$, and $u_6(t)$ can be obtained as

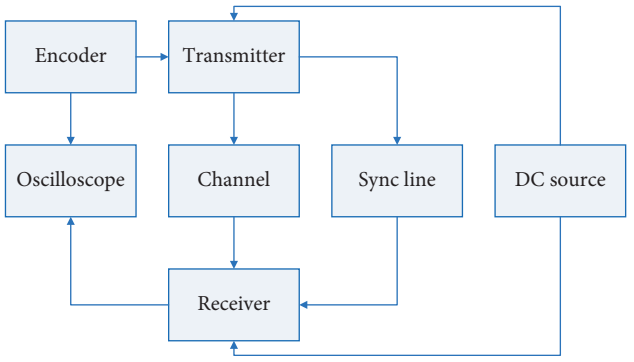
$$
\begin{aligned}
u_2(t) &= u_{r-} + e^{-\left(t/2R_5C_2\right)}\left[\left(u_{n2}' - u_{r-}\right)\cosh\left(\frac{\beta}{R_5C_2}t\right)\right.\\
&\quad \left. - \frac{2}{\beta}\left(u_{n4}' + u_{n2}' - u_{r-}\right)\sinh\left(\frac{\beta}{R_5C_2}t\right)\right],\\
u_4(t) &= u_{r-} + \left(u_{n4}' - u_{r-}\right)e^{-\left(t/2R_5C_2\right)}\left[\cosh\left(\frac{\beta}{R_5C_2}t\right)\right.\\
&\quad \left. + \frac{1}{2\beta}\sinh\left(\frac{\beta}{R_5C_2}t\right)\right],\\
u_6(t) &= u_{n6}'e^{-\left(t/2R_7C_6\right)}.
\end{aligned}
\tag{9}
$$

where $\beta = \sqrt{(R_3C_4 - 4R_5C_2)/4R_3C_4}$.

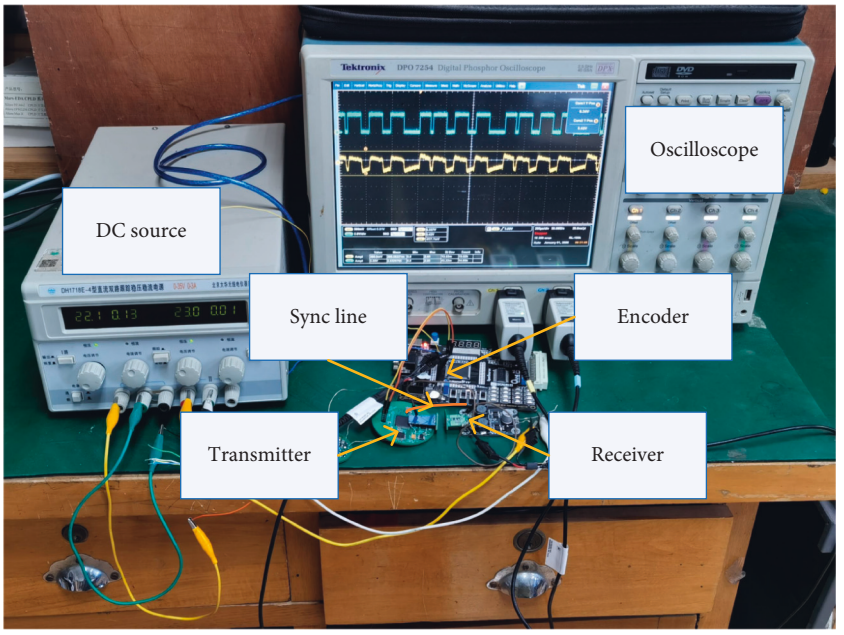


(a) (b)

Figure 6: The measured receiver. (a) Front of the receiver. (b) Back of the receiver.



(a)



(b)

Figure 7: Block diagram and measurement photo. (a) Block diagram of the measurement receiver. (b) Photo of measurement receiver.

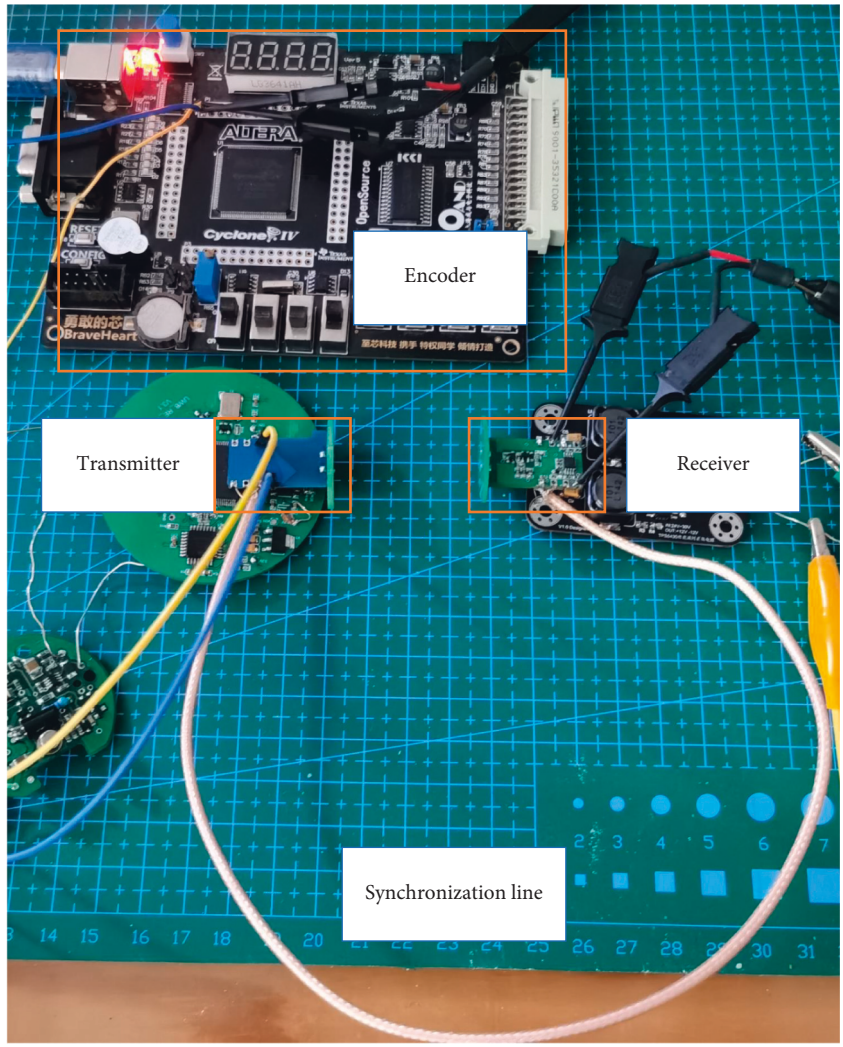


Figure 8: Photo of encoder, transmitter, receiver, and synchronization line.

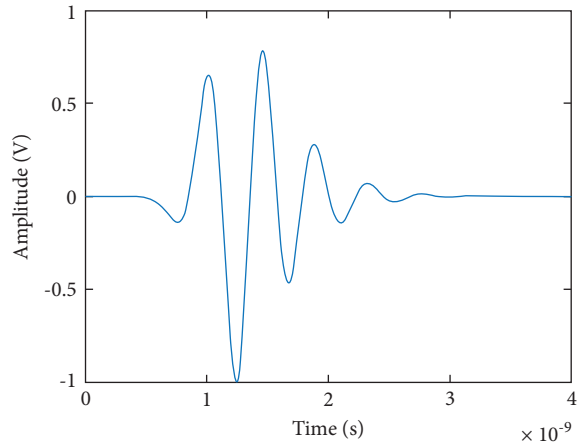


Figure 9: Single narrow pulse signal received by the receiving circuit.

In the process of circuit model calculation, the received UWB signal is iterated through equations (8) and (9), according to the initial states u_{n1}, u_{n3}, and u_{n5} of the three capacitors in the upper part of the circuit during diode conduction, and the final state values of u_{n1}', u_{n3}', and u_{n5}' of the capacitors C_1, C_3, and C_5 in the circuit sampling process

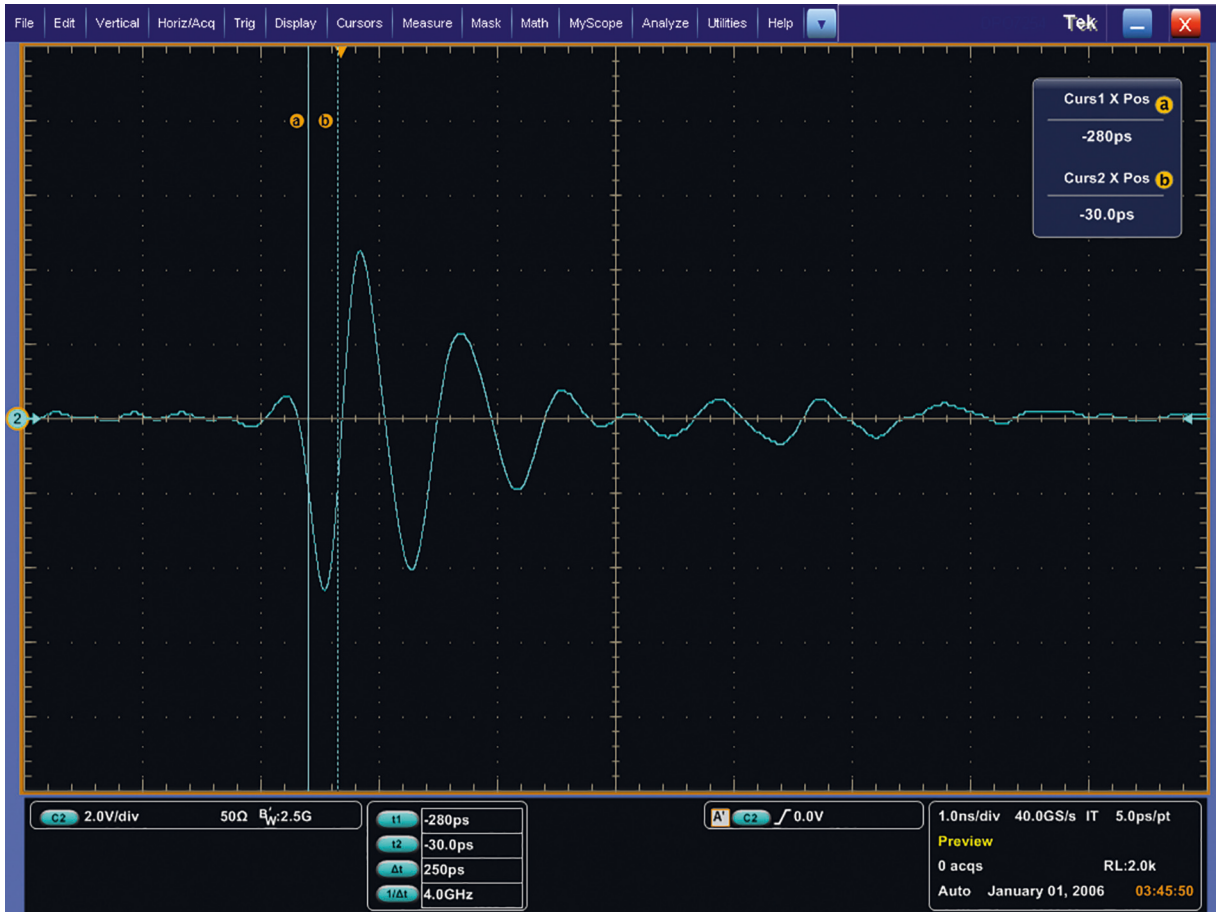


Figure 10: Single narrow pulse signal transmitted by the transmitter.

are obtained. u_{n1}', u_{n3}', and u_{n5}' are the initial state values of capacitors C_1, C_3, and C_5 in the circuit integration process at diode cutoff. Through the iterative operation of equations (8), the final state values of the three capacitors in the upper half of the nth cycle circuit can be obtained. $u_{(n+1)1}$, $u_{(n+1)3}$, and $u_{(n+1)5}$ are the initial states of the three capacitors during diode conduction in the next period.

The output signal of the upper part of the BSIC can be obtained by iterative calculation with the above method. In the same way, the output signal of the lower half of the BSIC can be obtained. The BSIC is connected to the differential amplifier, and $u_2 - u_3 - u_5 + u_6$ is taken as the output result of the whole circuit.

$$\begin{aligned} u_{\mathrm{OUT}} = {} & u_{r+} + (u_{n3}' - u_{r+}) e^{-(t/2R_4C_1)} \left[\cosh\left(\frac{\alpha}{R_4C_1}t\right) \right. \\ & \left. + \frac{1}{2\alpha}\sinh\left(\frac{\alpha}{R_4C_1}t\right) \right] - u_{n5}' e^{-(t/R_6C_5)}, \\ & - u_{r-} - (u_{n4}' - u_{r-}) e^{-(t/2R_5C_2)} \left[\cosh\left(\frac{\beta}{R_5C_2}t\right) \right. \\ & \left. + \frac{1}{2\beta}\sinh\left(\frac{\beta}{R_5C_2}t\right) \right] + u_{n6}' e^{-(t/R_7C_6)}, \end{aligned} \tag{10}$$

where $\alpha = \sqrt{(R_2C_3 - 4R_4C_1)/4R_2C_3}$, $\beta = \sqrt{(R_3C_4 - 4R_5C_2)/4R_3C_4}$.

3. Simulation and Test

3.1. Simulation and Test Methods. In this paper, the mathematical model of equation (10) BSIC is simulated, and the output signal of the actual circuit is measured to study the influence of circuit element parameters on the output signal so as to determine the parameters. The schematic block diagram of circuit parameter simulation and measurement is shown in Figure 5.

As shown in Figure 5, a modulated received signal is generated, and the received signal is input into a receiving circuit that has replaced different capacitance values. The capacitance values of the sampling capacitor, the integrating capacitor, and the high-pass filter capacitor in the circuit have been replaced, respectively. The influence of sampling capacitance, integrating capacitance and high-pass filter capacitance on the output signal of receiver, is studied through the waveform of output signal of receiving circuit.

The measured receiving circuit is shown in Figure 6.

In Figure 6, on the front side of the receiver (Figure 6(a)) are the BSIC and the amplification circuit. On the back of the receiver (Figure 6(b)) is the IR-UWB signal generation circuit. The BSIC, shown in Figure 5, is above the first black

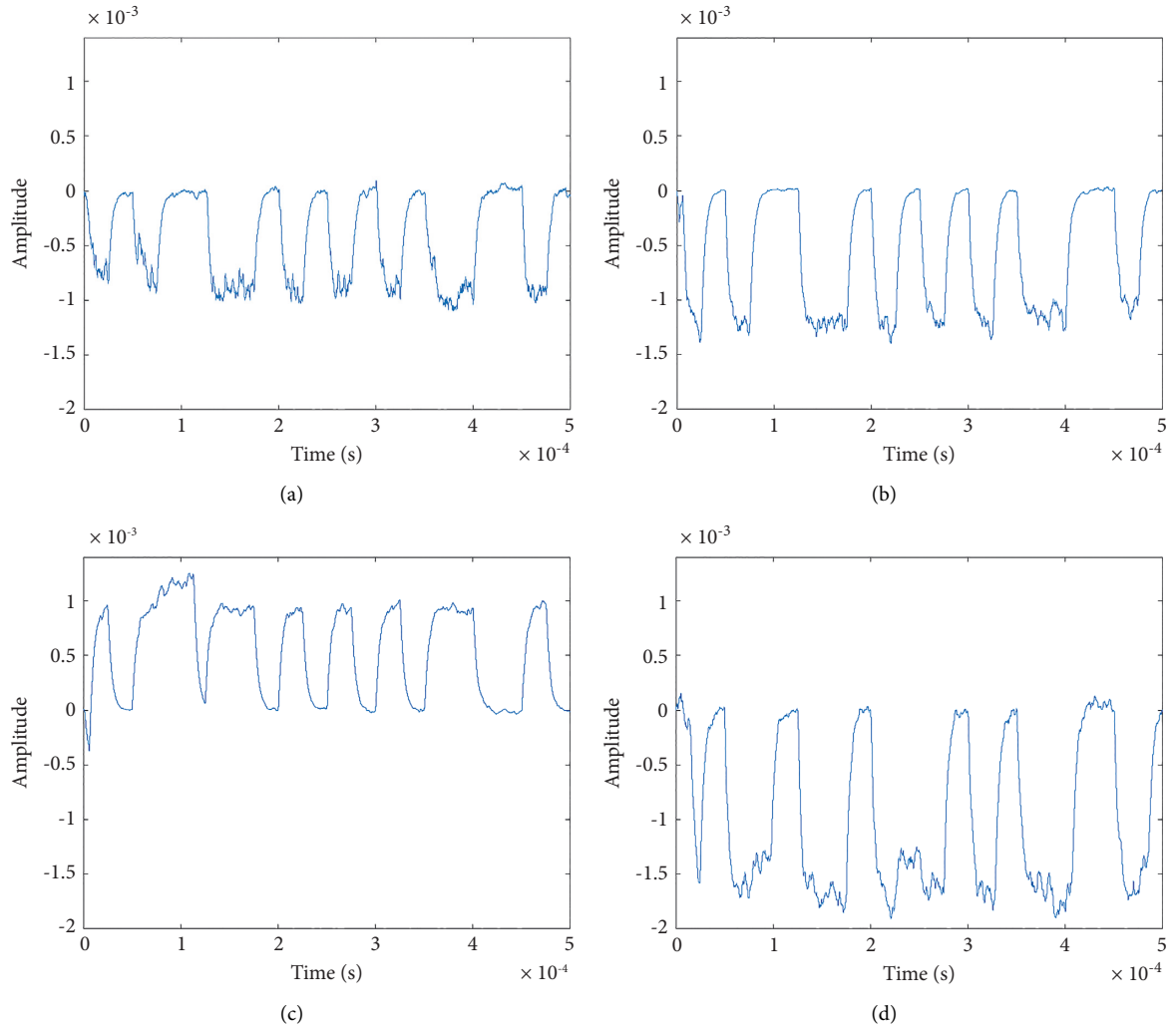


Figure 11: Simulation output waveforms of receiving circuit models with different sampling capacitors. (a) Sampling capacitance is 1 pF, (b) sampling capacitance is 2 pF, (c) sampling capacitance is 4 pF, and (d) sampling capacitance is 6 pF.

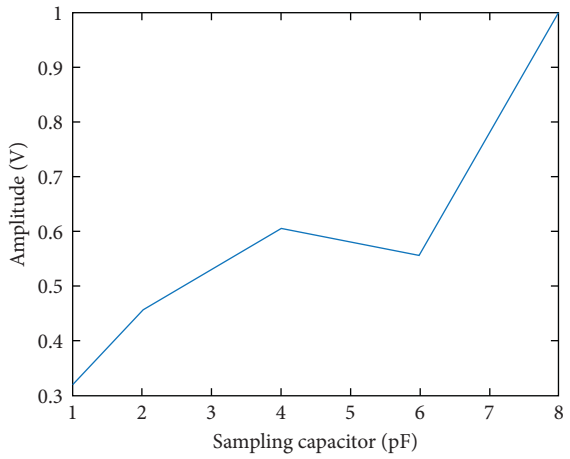


Figure 12: The relationship between the sampling capacitor and the normalized amplitude of the output signal of the receiving circuit simulated by equation (10).

Table 1: Output signal amplitude of BSIC with different sampling capacitors.

Sampling capacitance value (pF)	Circuit output signal amplitude (mV)
1	80
2	160
4	380

package amplifier in Figure 6(a). And ports 1 and 8 are 12 V and −12 V power supply. Port 2 is the output of differential amplifier. Port 3 is the output of comparator. Port 4 is the output of amplifier. Ports 5 and 6 connected to ground. Port 7 is the input signal, which controls the sampling switch. Ports 9 and 10 are connected to IR-UWB symmetrical dipole antennas.

The measured principle block diagram of the output signal of IR-UWB wireless communication receiver is shown in Figure 7, which is mainly composed of a transmitter, a

(a)

(b)

Figure 13: Continued.

(c)

Figure 13: The influence of different sampling capacitors on the output signal of the BSIC. (a) Sampling capacitance is 1 pF. (b) Sampling capacitance is 2 pF. (c) Sampling capacitance is 4 pF.

receiver, an encoder, a DC stabilized power supply, an oscilloscope, and a synchronization line.

Equipment models are as follows. Encoder: ALTERA Cyclone IV EP4CE6E22C8N. DC stabilized power supply: DH1718E-4. Oscilloscope: Tektronix DPO 7254 2.5 GHz 40 GS/s. Synchronization line: Coaxial line. The transmitter and receiver are made by ourselves.

As shown in Figures 7 and 8, the encoded signal generated by the encoder is modulated and then emitted by the transmitter, and the signal reaches the receiver through the wireless channel. At the same time, the transmitter sends the synchronous signal to the receiver through the synchronous line. Power supply for UWB wireless communication transmitter and receiver by DC stabilized power supply. The oscilloscope tests the output signal of receiver and the encoded signal of transmitter in different channels. The mathematical model of the receiver proposed in this paper is verified by measuring the output signal of the receiver, which has replaced the values of sampling capacitance, integrating capacitance and high-pass filter capacitance in the receiver.

When the parameters of the receiver are determined, a channel simulation module is added between the modulation signal and the receiver to simulate the channel noise, and the noise category is Gaussian white noise. The SNR is changed during simulation to test the receiver's antinoise ability.

3.2. Simulation and Test Setup. The single narrow pulse signal received by the receiver in the simulation is an ultra-wideband signal with a narrow pulse width of 200 ps. The normalized waveform is shown in Figure 9.

The signal in Figure 9 is obtained from a Gaussian second-order derivative by simulation of the antenna model in the CST software.

The OOK modulated binary code is used in the simulation, the narrow pulse repetition period is 50 ns, and the unit code length is 25 μs. The resistance R_1 is 51 Ω, R_2 and R_3 are 1 MΩ, R_4 and R_5 are 10 kΩ, R_6 R6 and R_7 are 200 kΩ, the capacitors C_1 and C_2 are 4 pF, C_3 and C_4 are 25 nF, and C_5, C_6 are 19.5 nF.

The narrow pulse signal transmitted by the transmitter during the test is shown in Figure 10, and the pulse width is about 250 ps.

The OOK modulated binary code is used in the simulation, the narrow pulse repetition period is about 52 ns, and the unit code length is 25 μs. The resistance R_1 is 51 Ω, R_2 and

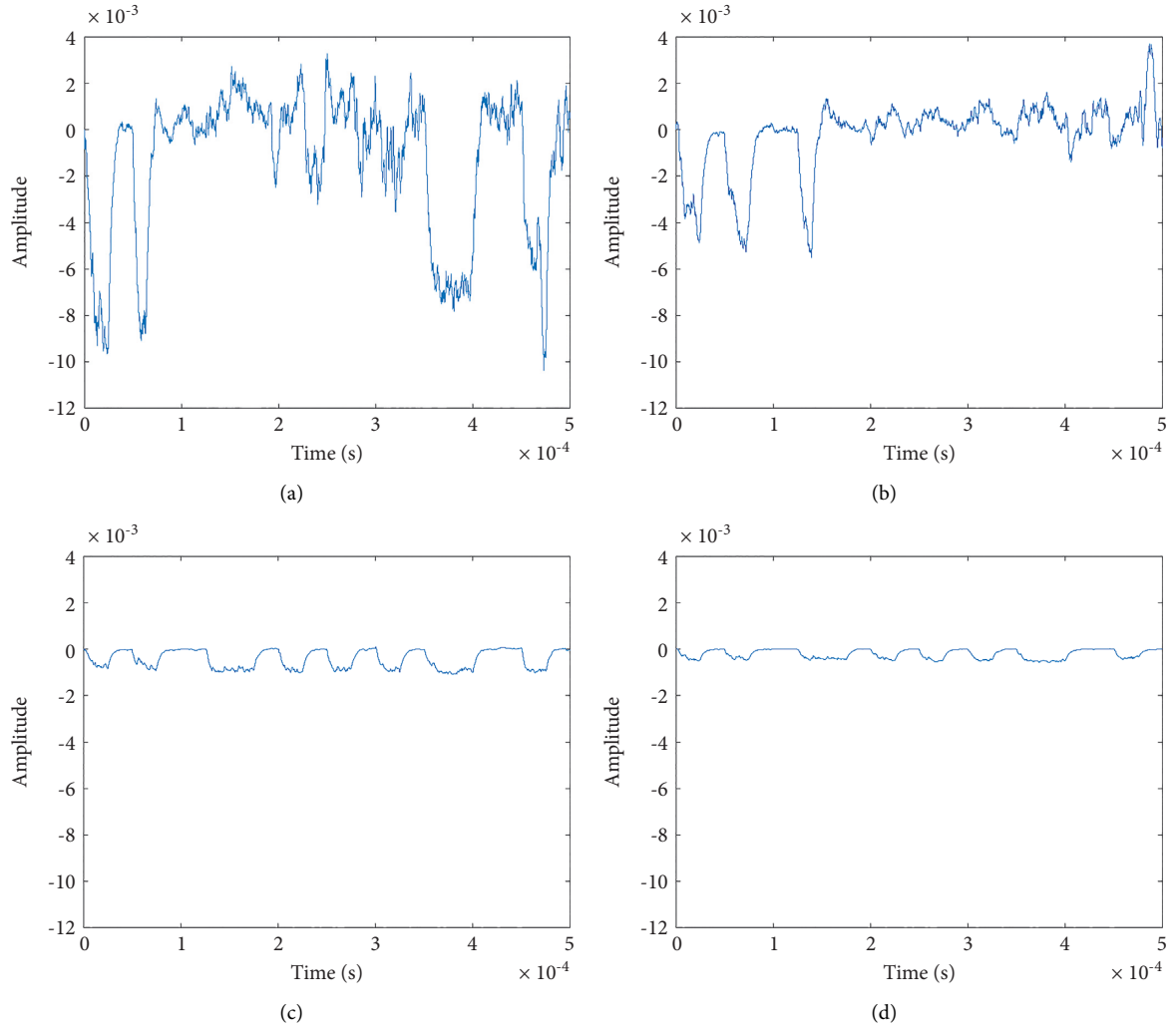


Figure 14: The simulation output waveform of the mathematical model of the receiving circuit with different integrating capacitors. (a) Integral capacitance is 2.5 nF. (b) Integral capacitance is 5 nF. (c) Integral capacitance is 25 nF. (d) Integral capacitance is 50 nF.

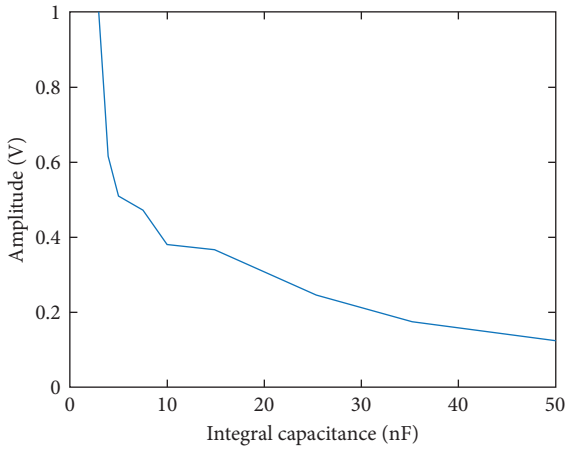


Figure 15: The relationship between the integrating capacitance and the output signal amplitude simulated by equation (10).

R_3 are 1 MΩ, R_4 and R_5 are 10 kΩ, R_6 and R_7 are 200 kΩ, the capacitors C_1 and C_2 are 4 pF, C_3 and C_4 are 22 nF, and C_5, C_6 are 18 nF.

4. Results and Discussion

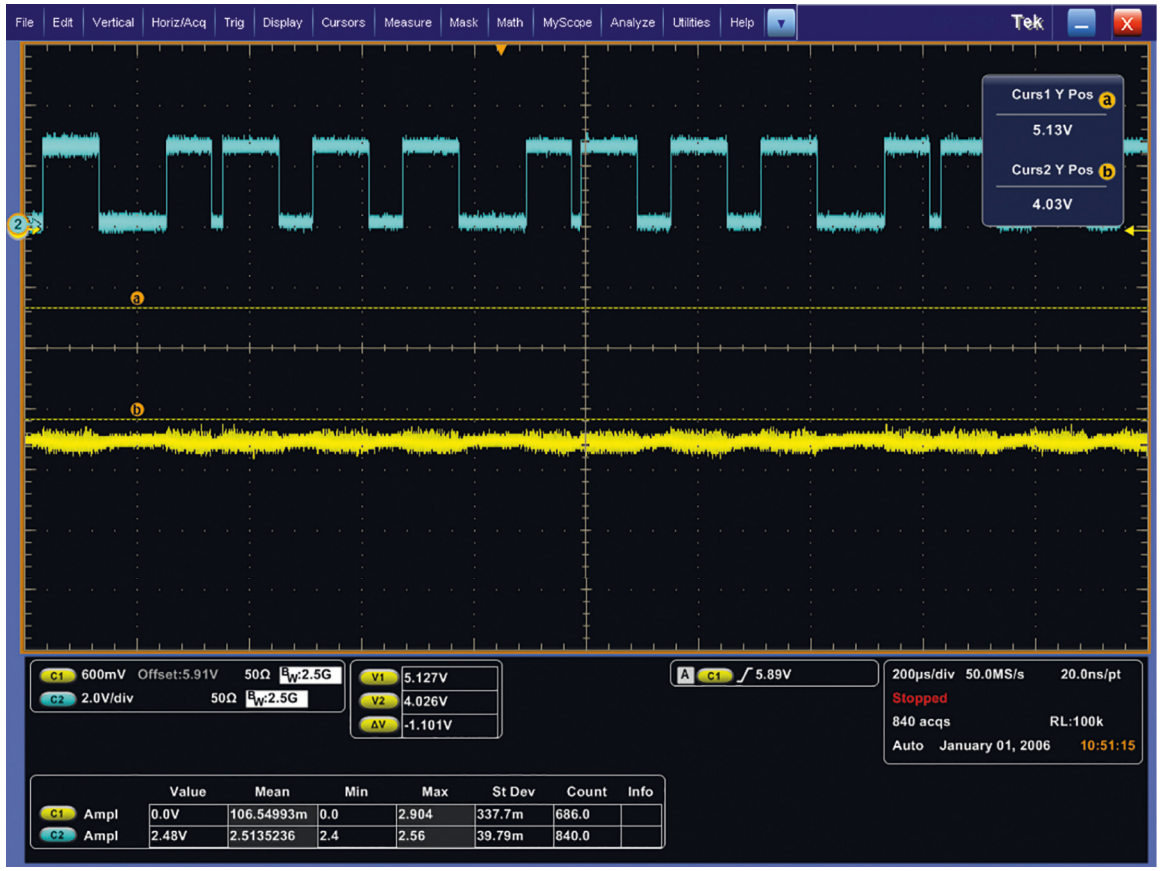
4.1. Receiver Output Signal with Different Sampling Capacitors. The value of the sampling capacitor depends on the pulse width of the received UWB signal. The approximate value range of the sampling capacitor can be calculated by the principle of capacitor charging.

$$u_{C_1}(t) = u_{r_+}\left(1 - e^{-\left(t/R_qC_1\right)}\right), \tag{11}$$

where u_{r_+} is the receive voltage, u_{C_1} is the voltage of sampling capacitor, and R_qC_1 is the time constant τ.

For the UWB signal pulse width is 200 ps, τ can be 50 ps, 100 ps, 200 ps, and 300 ps. The corresponding sampling capacitors C_1 and C_2 are, respectively, 1 pF, 2 pF, 4 pF, and 6 pF; the output signal of the receiving circuit can be obtained through the simulation of (10) as shown in Figure 11.

The relationship between the value of sampling capacitance C_1, C_2 and the output waveform amplitude obtained by simulation of the receiving circuit through equation (10) is shown in Figure 12.



(a)

(b)

Figure 16: Continued.

(c)

Figure 16: The influence of different integral capacitance on the output signal of the balanced sampling integral receiver circuit. (a) Integrating capacitance is 22 pF. (b) Integrating capacitance is 4.7 nF. (c) Integrating capacitance is 22 nF.

It can be clearly seen from Figures 11 and 12 that when the sampling capacitance C_1 and C_2 is changed, the output waveform amplitude of the BSIC changes significantly. The output signal of the receiving circuit increases with the increase of the sampling capacitance. When the sampling capacitance is 6 pF, the output signal amplitude of the receiving circuit decreases slightly.

When the sampling capacitors C_1 and C_2 are, respectively, 1 pF, 2 pF, and 4 pF, the output signal waveform of the BSIC is shown in Figure 13.

The influence of different sampling capacitors on the output signal amplitude of the BSIC is shown in Table 1.

As shown in Figure 13 and Table 1, the amplitude of the output signal of the BSIC increases with the increase of the sampling capacitance, and the trend is the same as the simulation result, when the sampling capacitance does not exceed 8 pF.

4.2. Receiver Output Signal with Different Integral Capacitance. The value of the integrating capacitor is determined by the interval between two narrow pulses. The charging process of the integrating capacitor C_3 is the same as the discharge process of the sampling capacitor C_1. The discharge time constant for the sampling capacitor is as follows:

$$\tau = \frac{C_1 C_3}{C_1 + C_3} R_4. \tag{12}$$

Table 2: Output signal amplitude of different integral capacitor BSIC.

Integrating capacitance value (pF)	Circuit output signal amplitude (mV)
22	—
4700	648
22000	640

Because the interval between two narrow pulses is 100 ns, the integrating capacitors C_3 and C_4 are 2.5 nF, 5 nF, 25 nF, and 50 nF, respectively, the output signal of the receiving circuit can be obtained through the simulation of (10), as shown in Figure 14.

Figure 15 shows the relationship between the integrating capacitors C_3, C_4 and the receiving circuit through the simulation of equation (10).

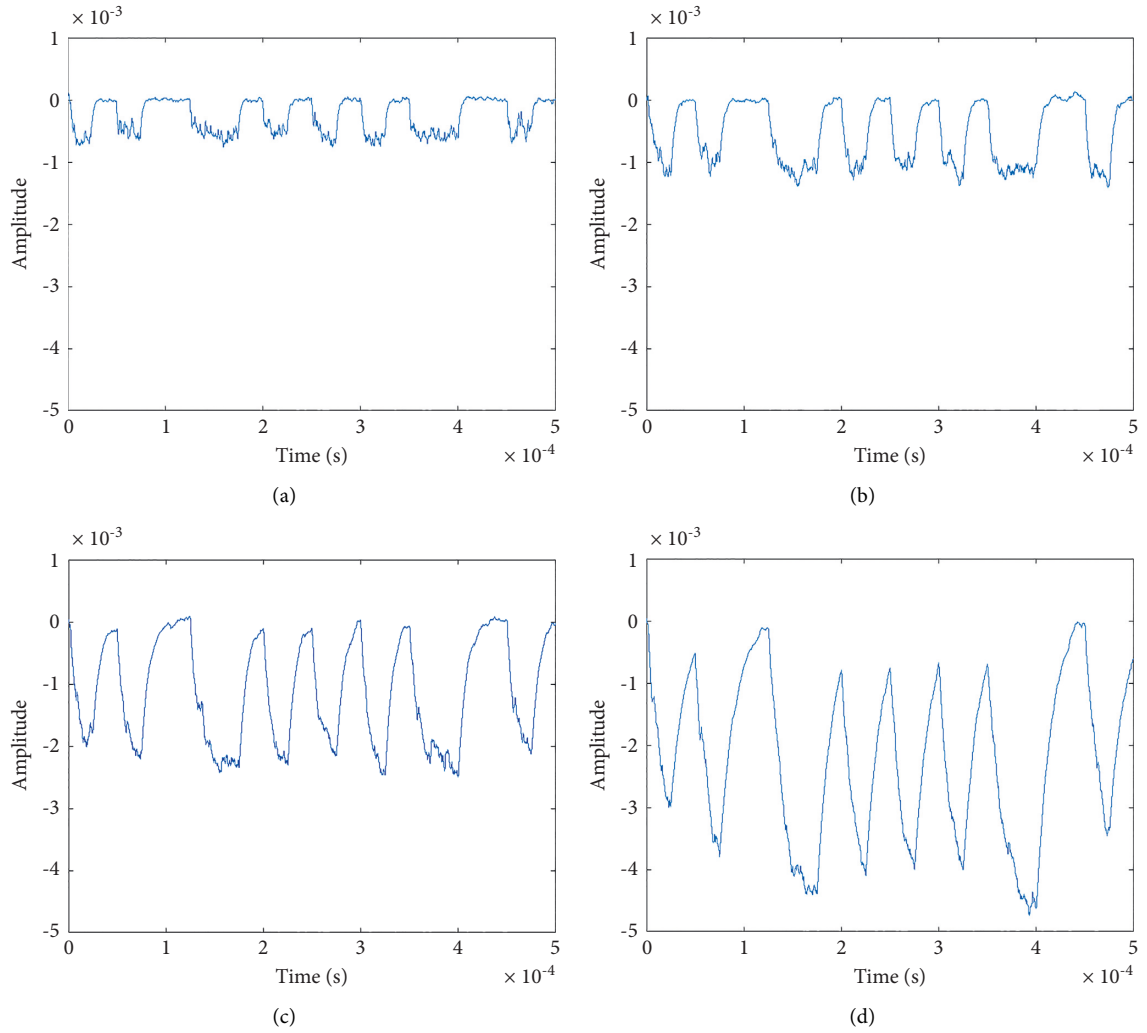


Figure 17: The simulation output waveform of the mathematical model of the receiving circuit with different filter capacitors. (a) Filter capacitance is 9.75 nF. (b) Filter capacitance is 19.5 nF. (c) Filter capacitance is 39 nF. (d) Filter capacitance is 78 nF.

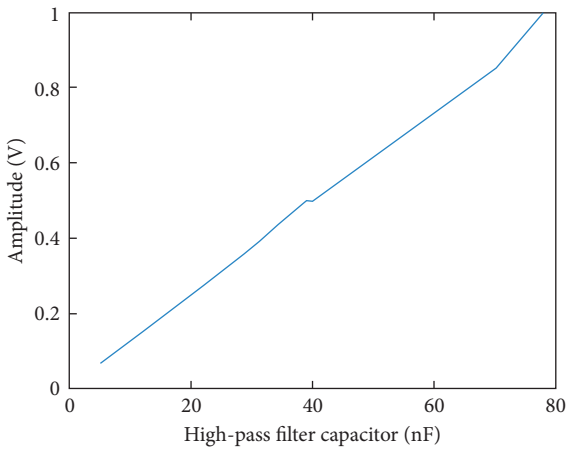


Figure 18: The relationship between the high-pass filter capacitance and the output signal amplitude simulated by equation (10).

As shown in Figures 14 and 15, the amplitude of the output signal of the receiving circuit decreases as the integral capacitance C_3 and C_4 increase. When the integrating capacitance increases to 5 nF, the output signal amplitude of the receiving circuit decreases rapidly. When the integrating capacitance increases from 5 nF to 50 nF, the output signal amplitude of the receiving circuit decreases gradually.

When the integrating capacitors C_3 and C_4 are, respectively, 22pF, 4.7 nF, and 22 nF, the output signal waveform of the BSIC is shown in Figure 16.

The influence of different integrating capacitors on the output signal amplitude of the BSIC is shown in Table 2.

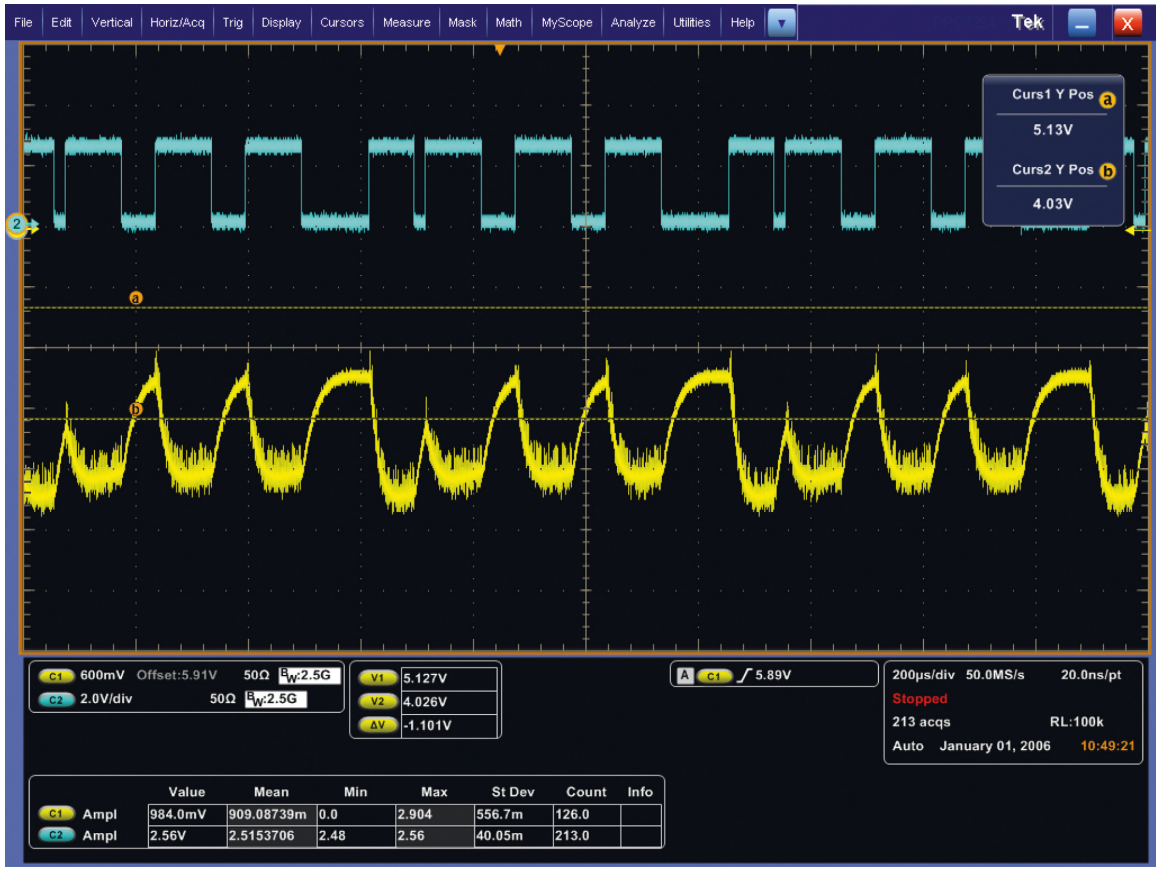
As shown in Figure 16 and Table 2, when the integrating capacitor is 22 pF, there is no obvious waveform amplitude as a DC voltage. When the integrating capacitor is 4.7 nF, part of the waveform amplitude can be seen to be 648 mV. When the integrating capacitor is 22 nF, obvious waveforms can be seen, with an amplitude of 640 mV.

The simulated and measured results are the same in that the output waveform becomes better when the integrating capacitor is around 22 nF. The difference is in the output waveform when the integration capacitance is less than 22 nF.

(a)

(b)

Figure 19: Continued.



(c)

Figure 19: The influence of different high-pass filter capacitors on the output signal of the balanced sampling and integrating receiver circuit. (a) Filter capacitance is 10 nF. (b) Filter capacitance is 18 nF. (c) Filter capacitance is 39 nF.

4.3. Receiver Output Signal with Different Filter Capacitance. When the filter capacitors C_5 and C_6 are, respectively, 9.75 nF, 19.5 nF, 39 nF, and 78 nF, the output signal of the receiving circuit obtained by the simulation based on equation (10) is shown in Figure 17.

The amplitude relationship between different filter capacitors C_5, C_6 and the output signal of the receiving circuit simulated through equation (10) is shown in Figure 18.

It can be seen from Figures 17 and 18 that the amplitude of the output signal of the receiving circuit increases with the increase of the filter capacitors C_5 and C_6.

When the filter capacitors C_5 and C_6 are 10 nF, 18 nF, and 39 nF, respectively, the output signal waveform of the BSIC is shown in Figure 19.

The influence of different high-pass filter capacitors on the output signal amplitude of the BSIC is shown in Table 3.

As shown in Figure 19 and Table 3, the output signal amplitude of the BSIC increases with the increase of the high-pass filter capacitor value, but the waveform is obviously distorted when the waveform reaches 39 nF. The measured result trend is the same as the model simulation result.

Table 3: Output signal amplitude of different filter capacitor BSIC.

Filter capacitance value (nF)	Circuit output signal amplitude (mV)
10	300
18	920
39	984

4.4. Simulation Results of Received Signals under Different SNR. When SNR is −30 dB, the time-domain waveform diagram of the received signal and the receiver output signal is shown in Figure 20.

To show the differences between all receiver output signals, the receiver output SNR and BER of receiver output signal is provided in Figure 21. The input SNR is the ratio of signal to noise in the channel. The output SNR is the ratio of the receiver output signal to the output noise. The BER is obtained by dividing the number of error bits by the total number of bits transmitted. The number of erroneous bits is obtained by statistical method.

The receiver output SNR decreases as the SNR decreases in Figure 21, and the BER also increases as the SNR decreases. Figure 21 shows that the BER of the receiver output signal is less than 10–3 when the input SNR is greater than −15 dB.

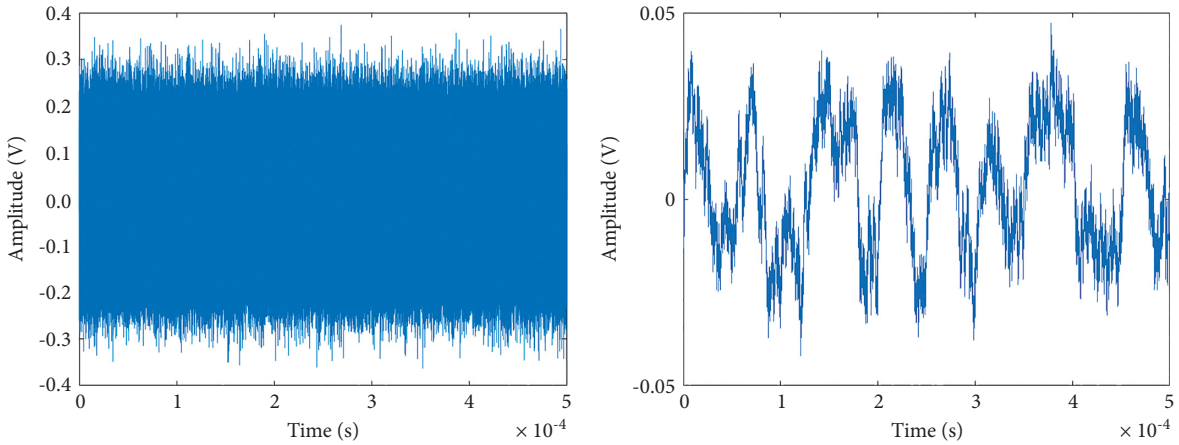


Figure 20: The time-domain waveform of the received signal and output signal of the receiver when SNR is −30 dB. (a) Receive signal. (b) Receiver output signal.

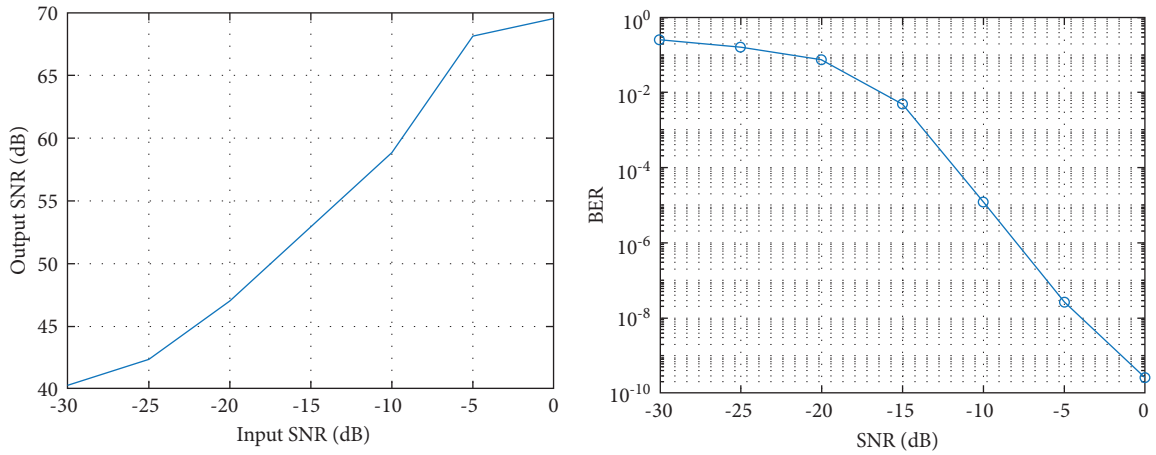


Figure 21: Receiver performance in low SNR environments. (a) Receiver output SNR. (b) BER of receiver output signal.

Table 4: Comparing with other published works.

	This work	Ref. [10]	Ref. [12]	Ref. [13]	Ref. [22]	Ref. [20]
Pulse width (ns)	0.20	—	Less 33	0.85	0.80	0.22
SNR of max. BER (dB)	−30	0	8	0	9	1
Maximum BER	10–1	10–1	10–1	10–1	10–1	10–1
SNR of min. BER (dB)	0	20	18	20	30	14
Minimum BER	10–9	10–8	10–4	10–5	10–5	10–5

The antinoise performance of the receivers in this paper is compared with other receivers in Table 4. The operating environment, BER, and pulse width of the receivers are compared in Table 4. It can be seen from the table that the UWB signal pulse width used in this paper is the narrowest. When BER is the highest, it is in the same order of magnitude as other receivers, but its corresponding SNR is the lowest, which is −30 dB. The receiver proposed in this paper is 1 to 4 orders of magnitude lower than other receivers at the minimum BER, and its corresponding SNR is also the lowest. This indicates that the receiver's antinoise ability is stronger than other receivers operating in high SNR environments.

5. Discussion

Through the simulation and measured results in Sections 4.1 to 4.3, it can be seen that the BSIC model established in this paper is consistent with the real circuit. However, in order to simplify the calculation, some parameters in the model are

ignored, which leads to a little difference between the calculated results using the model and the measured results.

In Section 4.4, the simulation results of the model in different SNR environments are compared with the results of some articles. The comparison results show that the anti-interference ability of BSIC receiver is stronger than other compared receivers. However, due to the characteristics of capacitor charging and discharging, the upper limit of data rate of BSIC receiver is lower than receivers with other structures. Therefore, the BSIC receiver can be mainly used in areas with relatively bad channel environment.

6. Conclusions

The IR-UWB receiver based on BSIC is improved to enhance its anti-interference ability. The mathematical model of the improved BSIC is established by using the circuit transient analysis method, and the expression of the output signal of the UWB wireless communication receiver is obtained by Laplace transform. The receiver parameters are studied and optimized based on BSIC model. The results of the study show that the integration capacitance in the receiver circuit has the greatest impact on the received signal waveform at an interval of 100 ns with a width of 200 ps; the smaller the integration capacitance, the worse the received signal waveform, in the range of 2.5 pF to 25 pF. This is basically the same as the test results. Simulation and test results show that the receiver model developed in this paper can serve as a guide for optimizing the receiver circuit parameters. The effect of noise on the output signal of the receiver was investigated and compared, and the results showed that the BER of the receiver is less than 0.005 when the SNR is greater than −15 dB. The comparison results show that the anti-interference ability of the improved BSIC receiver is stronger than that of other receivers. This improvement is effective. The next step is to increase the data transmission rate of this receiver.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

References

[1] S. Sharma and Y. Hong, "UWB receiver via deep learning in MUI and ISI scenarios," *IEEE Transactions on Vehicular Technology*, vol. 69, no. 3, pp. 3496–3499, 2020.

[2] S. Sharma, A. Gupta, and V. Bhatia, "IR-UWB sensor network using massive MIMO decision fusion: design and performance analysis," *IEEE Sensors Journal*, vol. 18, no. 15, pp. 6290–6302, 2018.

[3] J. Zhang, P. V. Orlik, Z. Sahinoglu, A. F. Molisch, and P. Kinney, "UWB systems for wireless sensor networks," *Proceedings of the IEEE*, vol. 97, no. 2, pp. 313–331, 2009.

[4] J. Ren, T. Zhang, J. Li, L. H. Nguyen, and P. Stoica, "RFI mitigation for UWB radar via hyperparameter-free sparse SPICE methods," *IEEE Transactions on Geoscience and Remote Sensing*, vol. 57, no. 6, pp. 3105–3118, 2019.

[5] T. Wan, K. Jiang, H. Ji, and B. Tang, "Deep Learning-Based LPI Radar Signals Analysis and Identification Using a Nyquist Folding Receiver Architecture," *Defence Technology*, 2021.

[6] M. Crepaldi, G. N. Angotzi, and L. Berdondini, "A 0.34 mm^2 1 Gb/s non-coherent UWB receiver architecture with pulse enhancement and double PLL clock/data packet recovery," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 7, pp. 2735–2748, 2019.

[7] Xi Qin, Y. Huang, and Z. Hong, "A 6-7 GHz, 40 dB receiver RF front-end with 4.5 dB minimum noise figure in 0.13μm CMOS for IR-UWB applications," *Journal of Semiconductors*, vol. 34, no. 3, Article ID 035006, 2013.

[8] L. Cai, L. Huang, Z. Fu, J. Yang, and W. Wang, "An energy detection receiver for non-coherent IR-UWB," *Journal of Semiconductors*, vol. 32, no. 6, Article ID 065006, 2011.

[9] D. C. Daly, P. P. Mercier, M. Bhardwaj et al., "A pulsed UWB receiver SoC for insect motion control," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 153–166, 2010.

[10] M. A. Rahman, S. Sasaki, Z. Jie, S. Muramatsu, and H. Kikuchi, "Evaluation of selective RAKE receiver in direct sequence ultra wideband communications in the presence of interference," *Ieice T Fund Electr*, vol. E87-A7 pages, 2004.

[11] R. Price and P. Green, "A communication technique for multipath channels," *Proceedings of the Ire*, vol. 46, no. 3, pp. 555–570, 1958.

[12] H. Khani, "Iterative Algorithms to Compensate for Quantization Noise in Monobit Transmitted-Reference Receivers," in *Proceedings of the 2014 IEEE International Conference on Ultra-WideBand (ICUWB)*, September 2014.

[13] H. Gharaee and A. Nabavi, "Baseband implementation of OTR-UWB receiver using FPGA," *AEUE - International Journal of Electronics and Communications*, vol. 64, no. 3, 2010.

[14] D. D. Wentzloff, F. S. Lee, D. C. Da Ly, M. Bhardwaj, and A. P. Chandrakasan, "Energy Efficient Pulsed-UWB CMOS Circuits and Systems," in *Proceedings of the IEEE International Conference on Ultra-wideband*, Singapore, September 2007.

[15] T. Quek and M. Z. Win, "Analysis of UWB transmitted-reference communication systems in dense multipath channels," *IEEE Journal on Selected Areas in Communications*, vol. 23, no. 9, 2005.

[16] M. Javadi, H. Miar-Naimi, and S. M. Hosseini Andargoli, "A UWB receiver with modified CS-CG LNTA: noise and nonlinearity analysis," *International Journal of Circuit Theory and Applications*, vol. 47, no. 5, pp. 654–665, 2019.

[17] D. Elsheakh, H. Shawkey, and S. Saleh, "A 9 - 10.6 GHz microstrip antenna—UWB low noise amplifier with differential noise canceling technique for IoT applications," *International Journal of Communications, Network and System Sciences*, vol. 12, no. 11, pp. 189–197, 2019.

[18] S. Arshad, R. Ramzan, and Q. U. Wahab, "50-830 MHz noise and distortion canceling CMOS low noise amplifier," *Integration, the VLSI Journal*, vol. 60, 2017.

[19] P. Jamshidi, "An Ultra Wideband Low-Power Low-Noise Amplifier Using Coupled Inductors," in *Proceedings of the Iranian Conference on Electrical Engineering*, Tehran, Iran, May 2015.

[20] Y. Shim, C. W. Kim, J. Lee, and S. G. Lee, "Design of Full Band UWB Common-Gate LNA," *Ieee Microw Wirel Co*, vol. 17, no. 10, 2007.

[21] C. F. Liao and S. I. Liu, "A Broadband Noise-Canceling CMOS LNA for 3.1-10.6-GHz UWB Receiver," *Custom Integrated Circuits Conference*, vol. 42, no. 2, 2005.

[22] S. Sharma, V. Bhatia, K. Deka, and A. Gupta, "Sparsity-based monobit UWB receiver under impulse noise environments," *IEEE Wireless Communications Letters*, vol. 8, no. 3, pp. 849–852, 2019.

[23] F. Sun, H. Yin, and W. Wang, "Finite-Resolution digital receiver for UWB TOA estimation," *IEEE Communications Letters*, vol. 16, no. 1, pp. 76–79, 2012.

[24] H. Yin, Z. Wang, L. Ke, and J. Wang, "Monobit digital receivers: design, performance, and application to impulse radio," *IEEE Transactions on Communications*, vol. 58, no. 6, pp. 1695–1704, 2010.

[25] L. Ke, H. Yin, W. Gong, and Z. Wang, "Finite-resolution digital receiver design for impulse radio ultra-wideband communication," *IEEE Transactions on Wireless Communications*, vol. 7, no. 12, pp. 5108–5117, 2008.

[26] Y. Yan, H. Zhonghua, and C. Zhanzhong, "Influence of sampling pulse on balanced sampling integral differential circuit performance," *Journal of Data Acquisition & Processing*, vol. 26, no. 2, 2011.