Hindawi Publishing Corporation
Mathematical Problems in Engineering
Volume 2016, Article ID 6086497, 10 pages
http://dx.doi.org/10.1155/2016/6086497

*Research Article*

# Carrier-Based PWM Method to Reduce Common-Mode Voltage of Three-to-Five-Phase Indirect Matrix Converter

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Received 11 July 2016; Revised 9 October 2016; Accepted 20 October 2016

Academic Editor: Stefan Balint



In order to reduce the common-mode voltage (CMV) for three-to-five-phase indirect matrix converter (IMC), the CMV with the conventional modulation strategy is analyzed. A novel carrier-based PWM (CBPWM) method is proposed in this paper. The zero vectors in the inverter stage are assigned to the rectifier stage, equivalently, which are not considered in the inverter stage. The zero vectors are selected appropriately to ensure that the dc-link is connected to an input phase with the minimum absolute value, so that the larger CMV can be avoided. Then, the modulation signals are derived by the duty ratios, which are used to compare with the only one carrier signal and generate the gate pulses of switches. With the proposed method, the CMV is reduced effectively compared with the conventional modulation strategy. This method is analyzed and researched with a simulation model established by Matlab/Simulink. Simulation results are provided in detail to verify the feasibility and validity of the proposed method.

## 1. Introduction

With the rapid development of the power electronic converter, the drive system gradually gets rid of the bound of the phase number. Multiphase drive system has received more and more attention [1–5], so that the multiphase matrix converter (MC) has been widely studied [6–11]. The three-to-five-phase direct matrix converter (DMC) was proposed in [7], and there are fifteen bidirectional switches connected in series; each output phase can connect with each input phase. However, this topology requires many power switches, multistep commutation, and complicated overvoltage protection circuits [12]. To avoid the above problems, a three-to-five-phase indirect matrix converter (IMC) topology, illustrated in Figure 1, has been researched to implement the AC-AC power converter. The benefits of three-to-five-phase IMC are similar to those of a three-to-five-phase DMC, such as no required large energy storage components, compact structure, bidirectional energy flow, unrestricted output frequency, a controllable input power factor, and a maximum voltage transfer ratio (VTR) of 0.7886 [7]. Moreover, it has additional advantages such as zero current safer commutation and less switching losses in the rectifier stage and less total number of power switches [11].

However, the CMV between the motor neutral point and the ground is caused inevitably when the SVPWM strategy is applied to MC. Due to the switches operating at high switching frequencies, the CMV, with a high value of $du/dt$, will produce a strong impact action on the motor drive system. Meanwhile, it will excite stray capacitance and parasitic coupling capacitance to generate high-frequency leakage current. This leakage current will produce a strong electromagnetic interference (EMI) [13–15]. Meanwhile, the CMV may cause shaft voltage between the shaft and the bearing seat through the distributed capacitance existing in the gap between stator, rotor, air, and ground, so that the normal operation of motor devices will be affected. Therefore, it is particularly important to reduce the negative effects of CMV.

At present, the research on control strategy to reduce CMV of the three-to-three-phase MC is relatively mature [14, 16–19], which is based on the mechanism of CMV. According

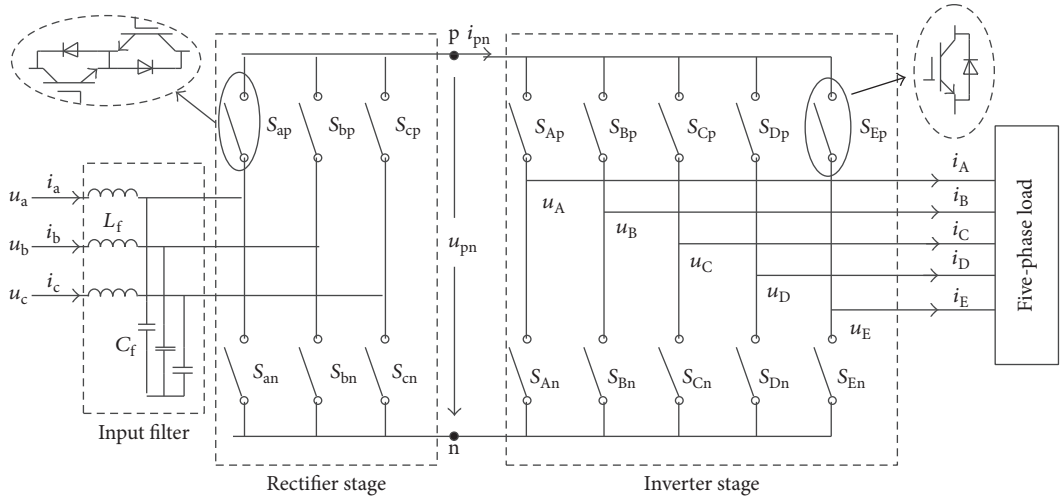



Figure 1: The topology of three-to-five-phase IMC.

to the amplitude-frequency characteristic of CMV, the low-pass filter with much smaller cut-off frequency than the switching frequency is applied in [16], so that the CMV is reduced. The high value of $du/dt$ is suppressed in [17] by improving the topology of matrix converter, and the output voltage is not mutation. Instead of zero vectors, a pair of opposing active vectors is chosen in [18] to reduce CMV. The two smaller line voltages are selected in [14] to synthesize the dc-link voltage. The CMV and switching losses of IMC are both reduced, but the maximum VTR is limited to 0.5. Using three active vectors to synthesize the desired output voltage vector is proposed in [19]. Although the CMV of IMC is reduced, the maximum VTR is only 0.577.

However, the research on CMV of the multiphase MC is relatively few. The zero vectors in the inverter stage are reselected based on SVPWM strategy in [20]. But it requires a complex sector combination and lookup tables.

In view of the above problems, a carrier-based PWM (CBPWM) method is proposed in this paper to reduce the CMV of three-to-five-phase IMC. This method focuses on the reasonable distribution of the zero vectors in both stages, so that the value of CMV is reduced. And the switching losses of the inverter stage are decreased.

## 2. Topology and Modulation Principles of Three-to-Five-Phase IMC

*2.1. Topology of Three-to-Five-Phase IMC.* The topology of three-to-five-phase IMC is shown in Figure 1. It consists of a rectifier stage with six bidirectional switches and a five-leg inverter stage with ten unidirectional switches. $u_a$, $u_b$, and $u_c$ and $i_a$, $i_b$, and $i_c$ are three-phase input voltages and input currents, respectively; $u_A$, $u_B$, $u_C$, $u_D$, and $u_E$ and $i_A$, $i_B$, $i_C$, $i_D$, and $i_E$ are five-phase output voltages and currents respectively. $u_{pn}$ and $i_{pn}$ are the dc-link voltage and current, respectively. $L_f$ and $C_f$ are inductor and capacitor of input filter. The switches of the rectifier stage are denoted by using $S_{kw}$ ($k \in \{a, b, c\}$; $w \in \{p, n\}$), and those of the inverter stage are denoted by using $S_{jw}$ ($j \in \{A, B, C, D, E\}$).

*2.2. The Basic Principle of Conventional Modulation Strategy.* For the rectifier stage, suppose the three input voltages are described by

$$\begin{aligned} u_a &= U_{im} \cos(\omega_i t) \\ u_b &= U_{im} \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ u_c &= U_{im} \cos\left(\omega_i t + \frac{2\pi}{3}\right), \end{aligned} \tag{1}$$

where $U_{im}$ and $\omega_i$ are the amplitude and angular frequency of the input phase voltage, respectively. One period of input phase voltages is divided into twelve segments, as shown in Figure 2.

In each segment, to obtain the maximum dc-link voltage $u_{pn}$, only two larger and positive line voltages are selected to synthesize $u_{pn}$ [21]. Taking the input voltages in segment 1 as an example, then, the voltages $u_{ab}$ and $u_{ac}$ are selected, as shown in Figure 2(b). Thus, the average value of the dc-link voltage $U_{pn}$ can be expressed as

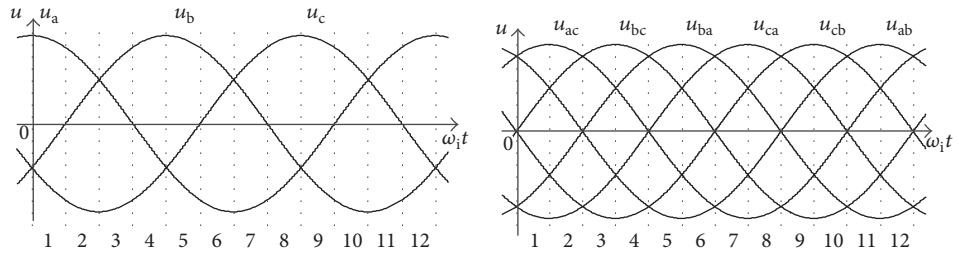
$$U_{pn} = d_\delta \cdot u_{ab} + d_\gamma \cdot u_{ac}, \tag{2}$$

where $d_\delta$ and $d_\gamma$ are duty ratios of voltages $u_{ab}$ and $u_{ac}$, respectively, and satisfy the following constraints:

$$d_\delta + d_\gamma = 1 \quad 0 \le d_\delta \le 1 \; 0 \le d_\gamma \le 1. \tag{3}$$

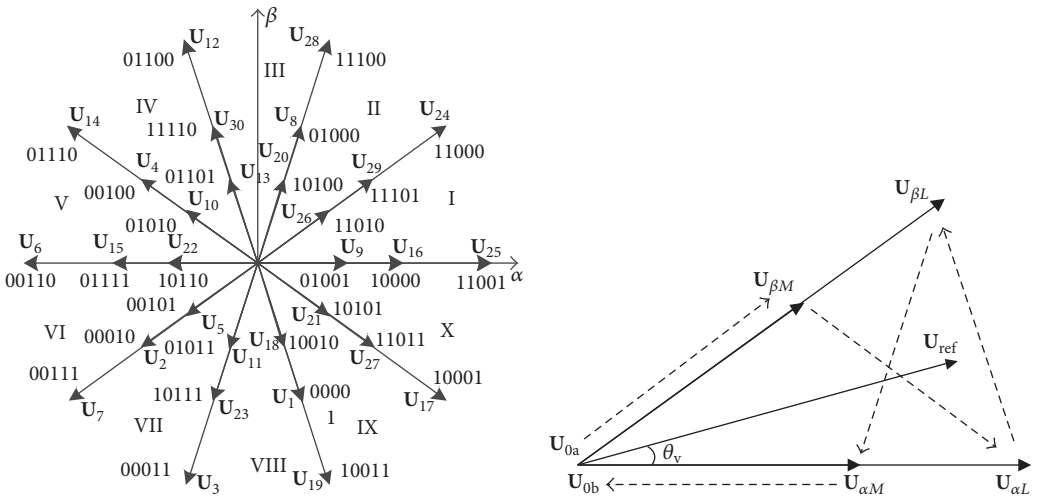
The local-averaged input currents are expressed as

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} d_\delta + d_\gamma \\ -d_\delta \\ -d_\gamma \end{bmatrix} I_{pn}, \tag{4}$$




(a) Input three-phase voltages (b) Input three line voltages

Figure 2: Segment partition for input voltages.




(a) Distribution of output voltage space vector (b) Generation of output reference voltage

Figure 3: Distribution and Generation of output voltage space vector.

where $I_{pn}$ is the local-averaged dc-link current of $i_{pn}$. Combining (2), (3), and (4) with the condition of unit input power factor, the duty ratios are obtained by

$$d_\delta = \frac{T_\delta}{T_s} = -\frac{u_b}{u_a}$$
$$d_\gamma = \frac{T_\gamma}{T_s} = -\frac{u_c}{u_a}, \tag{5}$$

where $T_s$ is the sampling period. $T_\delta$ and $T_\gamma$ are action times of voltages $u_{ab}$ and $u_{ac}$.

Combining (2) and (5), the average value of the dc-link voltage is

$$U_{pn} = \frac{3U_{im}^2}{2u_a}. \tag{6}$$

Thus, $U_{pn}$ varies in each input segment. The respective minimum and maximum values of the average dc-link voltage are

$$U_{pn}\big|_{min} = 1.5U_{im}$$
$$U_{pn}\big|_{max} = \sqrt{3}U_{im}. \tag{7}$$

According to the above analysis, the switching states in each segment and the corresponding duty ratios are shown in Table 1.

For the five-leg inverter stage, assume the expected output voltages are described by

$$u_A = U_{om}\cos(\omega_o t)$$
$$u_B = U_{om}\cos\left(\omega_o t - \frac{2\pi}{5}\right)$$
$$u_C = U_{om}\cos\left(\omega_o t - \frac{4\pi}{5}\right)$$
$$u_D = U_{om}\cos\left(\omega_o t - \frac{6\pi}{5}\right)$$
$$u_E = U_{om}\cos\left(\omega_o t - \frac{8\pi}{5}\right), \tag{8}$$

where $U_{om}$ and $\omega_o$ are the amplitude and angular frequency of the output phase voltage, respectively.

The distribution of output voltage space vector is shown in Figure 3(a), which includes thirty active vectors and two zero vectors ($\mathbf{U}_0$(00000) and $\mathbf{U}_{31}$(11111), not shown in

Table 1: The switching state and corresponding duty ratio in each segment.

| Segment | ON switch | Modulated switches and duty ratios | | | |
|---|---|---|---|---|---|
| | | $d_\delta$ | | $d_\gamma$ | |
| 1, 12 | $S_{ap}$ | $S_{bn}$ | $-u_b/u_a$ | $S_{cn}$ | $-u_c/u_a$ |
| 2, 3 | $S_{cn}$ | $S_{bp}$ | $-u_b/u_c$ | $S_{ap}$ | $-u_a/u_c$ |
| 4, 5 | $S_{bp}$ | $S_{an}$ | $-u_a/u_b$ | $S_{cn}$ | $-u_c/u_b$ |
| 6, 7 | $S_{an}$ | $S_{cp}$ | $-u_c/u_a$ | $S_{bp}$ | $-u_b/u_a$ |
| 8, 9 | $S_{cp}$ | $S_{bn}$ | $-u_b/u_c$ | $S_{an}$ | $-u_a/u_c$ |
| 10, 11 | $S_{bn}$ | $S_{ap}$ | $-u_a/u_b$ | $S_{cp}$ | $-u_c/u_b$ |

Figure 3(a)). Each vector is represented by the set ($S_A$, $S_B$, $S_C$, $S_D$, and $S_E$), where $S_k$ ($k$ = A, B, C, D, E) is defined as

$$S_k = \begin{cases} 1, & \text{the upper switch of leg } k \text{ is ON state} \\ 0, & \text{the lower switch of leg } k \text{ is ON state.} \end{cases} \tag{9}$$

There are six adjacent vectors in each sector that can be used to synthesize the reference output voltage vector. However, in order to obtain the maximum output reference voltage, only two adjacent maximum vectors $\mathbf{U}_{\alpha L}$ and $\mathbf{U}_{\beta L}$, and two medium vectors $\mathbf{U}_{\alpha M}$ and $\mathbf{U}_{\beta M}$, and zero vector $\mathbf{U}_0$ are selected [22], as shown in Figure 3(b).

The reference output voltage vector $\mathbf{U}_{\text{ref}}$ can be described by

$$\begin{aligned} \mathbf{U}_{\text{ref}} = {} & d_{\alpha L}\mathbf{U}_{\alpha L} + d_{\alpha M}\mathbf{U}_{\alpha M} + d_{\beta L}\mathbf{U}_{\beta L} + d_{\beta M}\mathbf{U}_{\beta M} \\ & + d_0\mathbf{U}_0, \end{aligned} \tag{10}$$

where

$$\begin{aligned} d_{\alpha L} &= \frac{T_{\alpha L}}{T_s} = \frac{1}{\sin(4\pi/5)} \frac{m_{\text{inv}}}{\eta \cdot M + L} \sin\left(\frac{\pi}{5} - \theta_v\right) \\ d_{\alpha M} &= \frac{T_{\alpha M}}{T_s} = \eta \cdot d_{\alpha L} \\ d_{\beta L} &= \frac{T_{\beta L}}{T_s} = \frac{1}{\sin(4\pi/5)} \frac{m_{\text{inv}}}{\eta \cdot M + L} \sin(\theta_v) \\ d_{\beta M} &= \frac{T_{\beta M}}{T_s} = \eta \cdot d_{\beta L} \\ d_{0v} &= \frac{T_{0v}}{T_s} = 1 - \left(d_{\alpha L} + d_{\alpha M} + d_{\beta L} + d_{\beta M}\right), \end{aligned} \tag{11}$$

where $m_{\text{inv}}$ is the modulation index of the five-leg inverter stage, $m_{\text{inv}} = U_{\text{om}}/U_{\text{pn}}$. $\theta_v$ is the angle between the vector $\mathbf{U}_{\text{ref}}$ and the vector $\mathbf{U}_{\alpha L}$. $M = 0.4$. $L = 0.8\cos(\pi/5)$. $T_{\alpha L}$, $T_{\alpha M}$, $T_{\beta L}$, and $T_{\beta M}$ and $d_{\alpha L}$, $d_{\alpha M}$, $d_{\beta L}$, and $d_{\beta M}$ are action times and duty ratios of corresponding vector. $\eta$ is the ratio of the medium and maximum vector in the same direction. In order to ensure the output voltage is sinusoidal waveform, the value of $\eta$ should be equal to $1/(2\cos(\pi/5))$.

Suppose the output voltage is in sector I ($\theta_v = \omega_o t$, $0 \le \theta_v \le \pi/5$), from (11), the sum of the duty ratios of the active vectors must be satisfied

$$d_{\alpha L} + d_{\alpha M} + d_{\beta L} + d_{\beta M} \le 1. \tag{12}$$

From (11) and (12), the following inequality can be obtained:

$$\frac{2\sin(2/5)\pi \cdot U_{\text{om}} \cdot \cos\left(\omega_o t - \pi/10\right)}{U_{\text{pn}}} \le 1. \tag{13}$$

On the left of (13), when the numerator takes the maximum value and the denominator takes the minimum value, (13) should also be established. That is,

$$\frac{2\sin(2/5)\pi \cdot U_{\text{om}}}{U_{\text{pn}}\big|_{\min}} \le 1. \tag{14}$$

From (7) and (14), the voltage transfer ratio (VTR) of the three-to-five-phase IMC is calculated as

$$\text{VTR} = \frac{U_{\text{om}}}{U_{\text{im}}} \le 0.7886. \tag{15}$$

To obtain the sinusoidal input and output waveforms, the switching pattern should produce an effective combination of the rectifier and inverter switching states. The input voltages in segment 1 and output voltages in sector I are taken as an example; the duty ratios of switching states within one sampling period are obtained by (5) and (11):

$$\begin{aligned} d_{\delta\alpha M} &= d_\delta \cdot d_{\alpha M}; \\ d_{\delta\alpha L} &= d_\delta \cdot d_{\alpha L} \\ d_{\delta\beta M} &= d_\delta \cdot d_{\beta M}; \\ d_{\delta\beta L} &= d_\delta \cdot d_{\beta L} \\ d_{\delta 0v} &= d_\delta \cdot d_{0v} \\ d_{\gamma\alpha M} &= d_\gamma \cdot d_{\alpha M}; \\ d_{\gamma\alpha L} &= d_\gamma \cdot d_{\alpha L} \\ d_{\gamma\beta M} &= d_\gamma \cdot d_{\beta M}; \\ d_{\gamma\beta L} &= d_\gamma \cdot d_{\beta L} \\ d_{\gamma 0v} &= d_\gamma \cdot d_{0v}. \end{aligned} \tag{16}$$

According to Figure 3(b), for the first half of the switching period, the vectors of the five-leg inverter stage are switched by $\mathbf{U}_{0a} \to \mathbf{U}_{\beta M} \to \mathbf{U}_{\alpha L} \to \mathbf{U}_{\beta L} \to \mathbf{U}_{\alpha M} \to \mathbf{U}_{0b}$, and in reverse for the second half for the symmetrical scheme. The switching sequence of the two stages is shown in Figure 4. The selection principle of zero vectors, $\mathbf{U}_{0a}$ and $\mathbf{U}_{0b}$, is to ensure the least switching number in each sampling period. $\mathbf{U}_{0a}, \mathbf{U}_{0b} \in \{\mathbf{U}_0, \mathbf{U}_{31}\}$. According to (16), the action time of each switching state is $t_{01} = 0.25 d_{\delta 0v} T_s$, $t_1 = 0.5 d_{\delta\beta M} T_s$, $t_2 = 0.5 d_{\delta\alpha L} T_s$, $t_3 = 0.5 d_{\delta\beta L} T_s$, $t_4 = 0.5 d_{\delta\alpha M} T_s$, $t_{02} =$

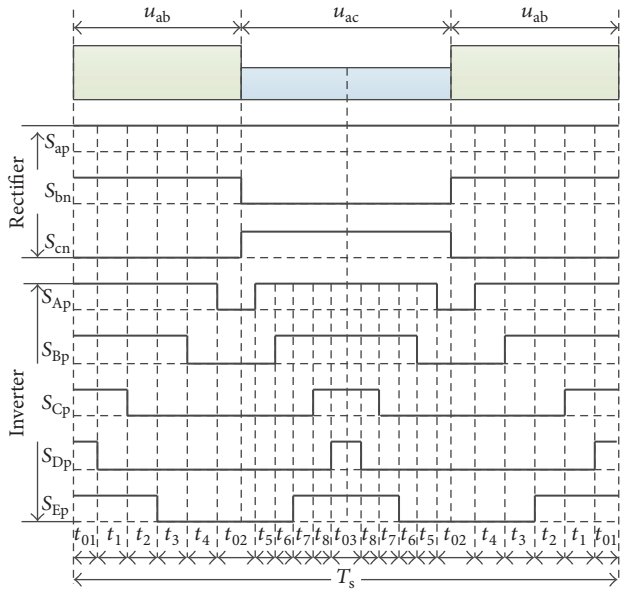



Figure 4: The switching sequence of conventional modulation strategy.

$0.25d_{0v}T_s$, $t_5 = 0.5d_{\gamma\alpha M}T_s$, $t_6 = 0.5d_{\gamma\beta L}T_s$, $t_7 = 0.5d_{\delta\alpha L}T_s$, $t_8 = 0.5d_{\gamma\beta M}T_s$, and $t_{03} = 0.5d_{\gamma 0v}T_s$. From Figure 4, the zero dc-link current commutation is achieved in the rectifier stage [21].

*2.3. Sector Transition Problem.* The principle of the transition from one segment to the other adjacent segment is to ensure the least switching number.

In the rectifier stage, The states of six switches in rectifier stage are represented by the set ($S_{ap}$, $S_{an}$, $S_{bp}$, $S_{bn}$, $S_{cp}$, and $S_{cn}$), and $S_{kw} = 1$ denotes that the switch $S_{kw}$ is ON state, and $S_{kw} = 0$ denotes that the switch $S_{kw}$ is OFF state, where $k \in \{a, b, c\}$; $w \in \{p, n\}$. The switching sequence in segment 1 is $u_{ab}(100100) \rightarrow u_{ac}(100001) \rightarrow u_{ab}(100100)$. In case of transit to segment 2, the switching sequence is $u_{ac}(100001) \rightarrow u_{bc}(001001) \rightarrow u_{ac}(100001)$. So, during the transition, the switch switches only once. From Figure 2(b), in case of transit from segment 2 to segment 3, the switch state remains unchanged. It is similar in other segments.

In the inverter stage, the switching sequence in sector I is $\mathbf{U}_{31}(11111) \rightarrow \mathbf{U}_{29}(11101) \rightarrow \mathbf{U}_{25}(11001) \rightarrow \mathbf{U}_{24}(11000) \rightarrow \mathbf{U}_{16}(10000) \rightarrow \mathbf{U}_0(00000) \rightarrow \mathbf{U}_{16}(10000) \rightarrow \mathbf{U}_{24}(11000) \rightarrow \mathbf{U}_{25}(11001) \rightarrow \mathbf{U}_{29}(11101) \rightarrow \mathbf{U}_{31}(11111)$. In case of the transit to the sector II, the switching sequence is $\mathbf{U}_{31}(11111) \rightarrow \mathbf{U}_{29}(11101) \rightarrow \mathbf{U}_{28}(11100) \rightarrow \mathbf{U}_{24}(11000) \rightarrow \mathbf{U}_8(01000) \rightarrow \mathbf{U}_0(00000) \rightarrow \mathbf{U}_8(01000) \rightarrow \mathbf{U}_{24}(11000) \rightarrow \mathbf{U}_{28}(11100) \rightarrow \mathbf{U}_{29}(11101) \rightarrow \mathbf{U}_{31}(11111)$. The switching sequence in other sectors is similar to that described above.

## 3. CMV Analysis in Three-to-Five-Phase IMC

The principle of CMV when a five-phase AC motor is driven by the three-to-five-phase IMC is shown in Figure 5. $Z_{NO}$ is the leakage impedance between the load neutral point and the ground. The paths of CMV and leakage current

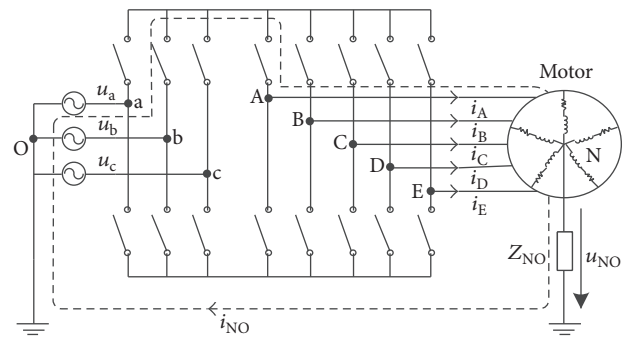



Figure 5: Generation of CMV and leakage current.

are represented by the dashed line in Figure 5. Then, the equations can be obtained by KVL:

$$\begin{aligned} u_{AO} - u_{NO} &= Ri_A + Ldi_A/dt \\ u_{BO} - u_{NO} &= Ri_B + Ldi_B/dt \\ u_{CO} - u_{NO} &= Ri_C + Ldi_C/dt \\ u_{DO} - u_{NO} &= Ri_D + Ldi_D/dt \\ u_{EO} - u_{NO} &= Ri_E + Ldi_E/dt, \end{aligned} \tag{17}$$

where $u_{AO}$, $u_{BO}$, $u_{CO}$, $u_{DO}$, and $u_{EO}$ are voltages between output phases and the ground. $R$ and $L$ are the equivalent resistance and inductance of the AC motor. Under the condition of sinusoidal and symmetrical output waveforms, the sum of output currents is equal to zero $i_A + i_B + i_C + i_D + i_E = 0$. From (17), The CMV $u_{NO}$ can be expressed as

$$u_{NO} = \frac{u_{AO} + u_{BO} + u_{CO} + u_{DO} + u_{EO}}{5}. \tag{18}$$

According to the above analysis, it can be seen that the CMV is generated inevitably between the motor neutral point and the ground, when the motor is driven by five-phase converter. Different peak value of CMV is generated due to the different switching combinations, when the conventional modulation strategies in [11, 22] are applied. According to the basic principle of the conventional modulation strategy, taking the input voltage in segment 1 and the reference output voltage vector in sector I as an example, when the dc-link voltage is $u_{ab}$ and the vector $\mathbf{U}_{25}(11001)$ is used in the five-leg inverter stage, the output phases "A," "B," and "E" are connected to "p" pole of dc-side (input phase "a"); "C" and "D" are connected to "n" pole of dc-side (input phase "b"). Combining (18), The CMV generated at this time is calculated by $u_{NO} = (3u_a + 2u_b)/5$, the value range of which is $[\sqrt{3}U_{im}/10, 3\sqrt{3}U_{im}/10]$. Thus, the peak value of CMV is $3\sqrt{3}/10$ times of the amplitude of input phase voltage. Other cases are similar to the above. The distribution of CMV at each switching combination is shown in Table 2. Similarly, the same method can be used to analyze the CMV of other sector combinations.

From Table 2, the peak value of CMV is the amplitude of input phase voltage when the zero vector $\mathbf{U}_{31}$ is used in the

Table 2: Distribution and variation of the CMV.

| $u_{dc}$ | Vector | $u_{NO}$ | Ranges | Peak value of $u_{NO}$ |
|---|---|---|---|---|
| $u_{ab}$ | $\mathbf{U}_0$(00000) | $u_b$ | $[-\sqrt{3}U_{im}/2, 0]$ | $\sqrt{3}U_{im}/2$ |
| | $\mathbf{U}_{16}$(10000) | $(u_a + 4u_b)/5$ | $[-3\sqrt{3}U_{im}/10, \sqrt{3}U_{im}/10]$ | $3\sqrt{3}U_{im}/10$ |
| | $\mathbf{U}_{24}$(11000) | $(2u_a + 3u_b)/5$ | $[-\sqrt{3}U_{im}/10, \sqrt{3}U_{im}/5]$ | $\sqrt{3}U_{im}/5$ |
| | $\mathbf{U}_{25}$(11001) | $(3u_a + 2u_b)/5$ | $[\sqrt{3}U_{im}/10, 3\sqrt{3}U_{im}/10]$ | $3\sqrt{3}U_{im}/10$ |
| | $\mathbf{U}_{29}$(11101) | $(4u_a + u_b)/5$ | $[3\sqrt{3}U_{im}/10, \sqrt{13}U_{im}/5]$ | $\sqrt{13}U_{im}/5$ |
| | $\mathbf{U}_{31}$(11111) | $u_a$ | $[\sqrt{3}U_{im}/2, U_{im}]$ | $U_{im}$ |
| $u_{ac}$ | $\mathbf{U}_0$(00000) | $u_c$ | $[-\sqrt{3}U_{im}/2, 0]$ | $\sqrt{3}U_{im}/2$ |
| | $\mathbf{U}_{16}$(10000) | $(u_a + 4u_c)/5$ | $[-3\sqrt{3}U_{im}/10, \sqrt{3}U_{im}/10]$ | $3\sqrt{3}U_{im}/10$ |
| | $\mathbf{U}_{24}$(11000) | $(2u_a + 3u_c)/5$ | $[-\sqrt{3}U_{im}/10, \sqrt{3}U_{im}/5]$ | $\sqrt{3}U_{im}/5$ |
| | $\mathbf{U}_{25}$(11001) | $(3u_a + 2u_c)/5$ | $[\sqrt{3}U_{im}/10, 3\sqrt{3}U_{im}/10]$ | $3\sqrt{3}U_{im}/10$ |
| | $\mathbf{U}_{29}$(11101) | $(4u_a + u_c)/5$ | $[3\sqrt{3}U_{im}/10, \sqrt{13}U_{im}/5]$ | $\sqrt{13}U_{im}/5$ |
| | $\mathbf{U}_{31}$(11111) | $u_a$ | $[\sqrt{3}U_{im}/2, U_{im}]$ | $U_{im}$ |

five-leg inverter stage. Then, the dc-link is connected to an input phase with the maximum absolute value. The CMV, the peak value of which is equal to $U_{im}$, is generated.

## 4. The CBPWM Method with CMV Reduction

By analyzing the switching sequence in Figure 4, the zero vectors in the inverter stage are assigned to the rectifier stage, equivalently, which are not considered in the inverter stage. Thus, the dc-link voltage is synthesized by two larger line voltages and a zero voltage, which can be selected according to the absolute value of the input phase voltage. When the input voltage is in segments 1, 2, 7, and 8, the zero voltage $u_{bb}$ is selected; the voltage $u_{aa}$ is used in segments 3, 4, 9, and 10; and in segments 5, 6, 11, and 12, $u_{cc}$ is used. The input voltage in segment 1 and the reference output voltage vector in sector I are taken as an example; the switching sequence is shown in Figures 6(a) and 6(b).

In terms of the change rate of CMV, the CMV is changed 16 times within one sampling period by using the improved modulation strategy. While it is 22 times and 18 times when using two zero vectors and one zero vector, respectively, under conventional modulation strategies.

According to (16), the action time of each switching state in Figure 6 is $t_1 = 0.5d_{\delta\beta M}T_s$, $t_2 = 0.5d_{\delta\alpha L}T_s$, $t_3 = 0.5d_{\delta\beta L}T_s$, $t_4 = 0.5d_{\delta\alpha M}T_s$, $t_5 = 0.5d_{\gamma\alpha M}T_s$, $t_6 = 0.5d_{\gamma\beta L}T_s$, $t_7 = 0.5d_{\gamma\alpha L}T_s$, $t_8 = 0.5d_{\gamma\beta M}T_s$, and $t_0 = 0.5d_{0v}T_s$.

In the rectifier stage, when the switching states are switched, the active vectors are used in the inverter stage. Thus, the commutation mode should be applied appropriately to ensure the safe commutation of switches in the rectifier stage.

According to the above analysis and Table 2, the peak value of CMV is not more than $\sqrt{13}U_{im}/5$, so that it can be reduced to $\sqrt{13}/5$ of the amplitude of the input phase voltage.

The modulation strategy is realized by complex division and combination of sectors, which is similar to the SVPWM strategy. In order to simplify the process, only one

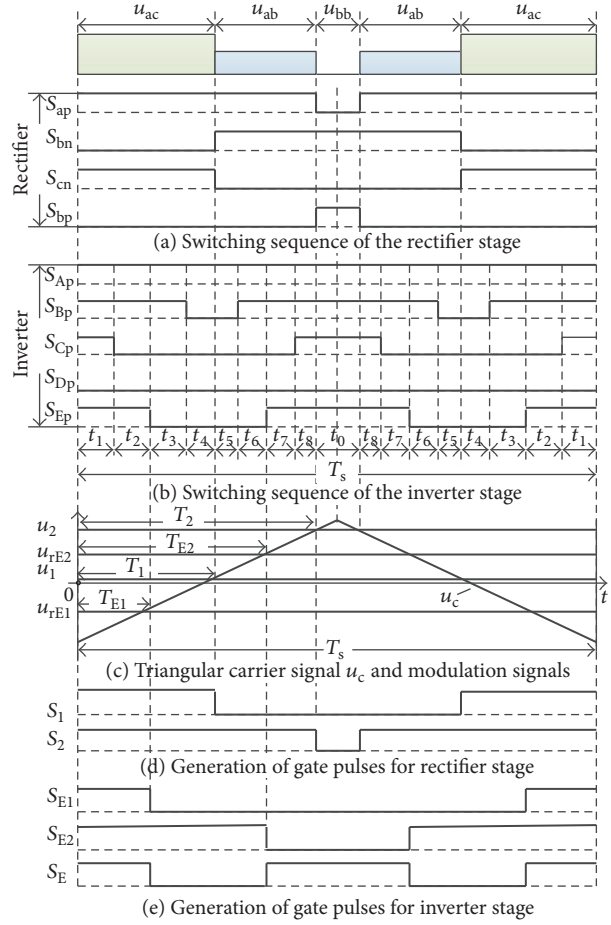



Figure 6: The switching sequence and generation of gate pulses by using the improved modulation strategy.

symmetrical triangular carrier signal is applied in this paper, which is described as

$$u_c = \frac{4}{T_s}t - 1, \quad 0 \le t \le \frac{T_s}{2}, \tag{19}$$

where $u_c$ is the instantaneous value of the carrier signal.

*4.1. Rectifier Stage Control.* Figure 6(d) shows the principle to generate gate pulses for the rectifier stage. The two modulation signals $u_1$ and $u_2$ in Figure 6(c) are used to generate the gate pulses for rectifier stage. The two pulses $S_1$ and $S_2$ in Figure 6(d) are obtained by comparing two modulation signals to the carrier signal. The gate pulses for switches $S_{ap}$, $S_{bp}$, $S_{bn}$, and $S_{cn}$ are calculated by

$$\begin{aligned} S_{ap} &= S_2 \\ S_{bp} &= \overline{S}_2 \\ S_{bn} &= \overline{S}_1 \\ S_{cn} &= S_1. \end{aligned} \tag{20}$$

The gate pulses for other switches are $S_{an} = 0$ and $S_{cp} = 0$. The switching sequence for the rectifier stage, shown in Figure 6(a), is obtained by (20) and Figure 6(d).

From Figures 6(a) and 6(c), the durations $T_1$ and $T_2$ can be derived as

$$\begin{aligned} T_1 &= \left(d_{\alpha M} + d_{\beta L} + d_{\alpha L} + d_{\beta M}\right) \cdot d_\delta \cdot \frac{T_s}{2} \\ T_2 &= \left(d_{\alpha M} + d_{\beta L} + d_{\alpha L} + d_{\beta M}\right) \cdot \frac{T_s}{2}. \end{aligned} \tag{21}$$

Combining (19) and (21), two modulation signals are obtained by

$$\begin{aligned} u_1 &= 2d_\delta \frac{u_A - u_D}{U_{pn}} - 1 \\ u_2 &= 2\frac{u_A - u_D}{U_{pn}} - 1. \end{aligned} \tag{22}$$

In other segments, the two modulation signals are similar to (22). In different input segments, they can be written as

$$\begin{aligned} u_{r1} &= 2d_\delta \frac{u_{max} - u_{min}}{U_{pn}} - 1 \\ u_{r2} &= 2\frac{u_{max} - u_{min}}{U_{pn}} - 1, \end{aligned} \tag{23}$$

where $u_{r1}$ and $u_{r2}$ are two modulation signals for the rectifier stage. $u_{max} = \max(u_A, u_B, u_C, u_D, u_E)$ and $u_{min} = \min(u_A, u_B, u_C, u_D, u_E)$.

*4.2. Inverter Stage Control.* In Figure 6(b), because the zero vectors are not considered in the inverter stage, the switches $S_{Ap}$ and $S_{Dn}$ keep ON state, while $S_{An}$ and $S_{Dp}$ keep OFF state within each sampling period in sector I, so that the switches of phases "B," "C," and "E" are modulated. In order to generate the gate pulse for the upper switch of each phase, two modulation signals are needed. Figure 6(e) shows the principle to generate the gate pulse for switch $S_E$ when the CBPWM method is used in the inverter stage. The two modulation signals, $u_{rE1}$ and $u_{rE2}$, are used to generate the gate pulse for the upper switch of phase "E," which is shown in Figure 6(c). The pulses $S_{E1}$ and $S_{E2}$ are obtained by comparing two modulation signals, $u_{rE1}$ and $u_{rE2}$, respectively, with the symmetrical triangular signal $u_c$. Then, the pulse $S_E$ for switch $S_{Ep}$ is shown in Figure 6(e). It is obtained by XOR function:

$$S_E = S_{E1} \cdot S_{E2} + \overline{S}_{E1} \cdot \overline{S}_{E2}. \tag{24}$$

The switching sequence for output phase "E" is obtained by (24) and Figure 6(e).

From Figures 6(b) and 6(c), the durations $T_{E1}$ and $T_{E2}$ can be derived as

$$\begin{aligned} T_{E1} &= \left(d_{\beta M} + d_{\alpha L}\right) \cdot d_\delta \cdot \frac{T_s}{2} \\ T_{E2} &= \left[\left(d_{\beta M} + d_{\alpha L} + d_{\beta L} + d_{\alpha M}\right) \cdot d_\delta + \left(d_{\alpha M} + d_{\beta L}\right)\right. \\ &\quad \left. \cdot d_\gamma\right] \cdot \frac{T_s}{2}. \end{aligned} \tag{25}$$

Combining (19) and (25), two modulation signals are obtained by

$$\begin{aligned} u_{rE1} &= 2d_\delta \frac{u_E - u_D}{U_{pn}} - 1 \\ u_{rE2} &= 2\left(\frac{u_A - u_D}{U_{pn}} - \frac{u_E - u_D}{U_{pn}} d_\gamma\right) - 1. \end{aligned} \tag{26}$$

The two modulation signals of other phases are similar to (22) as well as in other sectors. Generally, the double modulation signals to generate gate pulse for the upper switch of phase "$X$" ($X \in \{A, B, C, D, E\}$) in the inverter stage are given by

$$\begin{aligned} u_{rX1} &= 2d_\delta \frac{u_X - u_{min}}{U_{pn}} - 1 \\ u_{rX2} &= 2\left(\frac{u_{max} - u_{min}}{U_{pn}} - \frac{u_X - u_{min}}{U_{pn}} d_\gamma\right) - 1, \end{aligned} \tag{27}$$

where $u_{rX1}$ and $u_{rX2}$ are two modulation signals of phase "$X$" and $u_X$ is output voltage of phase "$X$".

In the inverter stage, the gate pulse of the lower switch of each phase has a complementary relationship with that of the upper switch. However, in the different sectors, the switches which keep ON state or OFF state continuously are different. Thus, the different modulation signals are needed, as shown in Table 3.

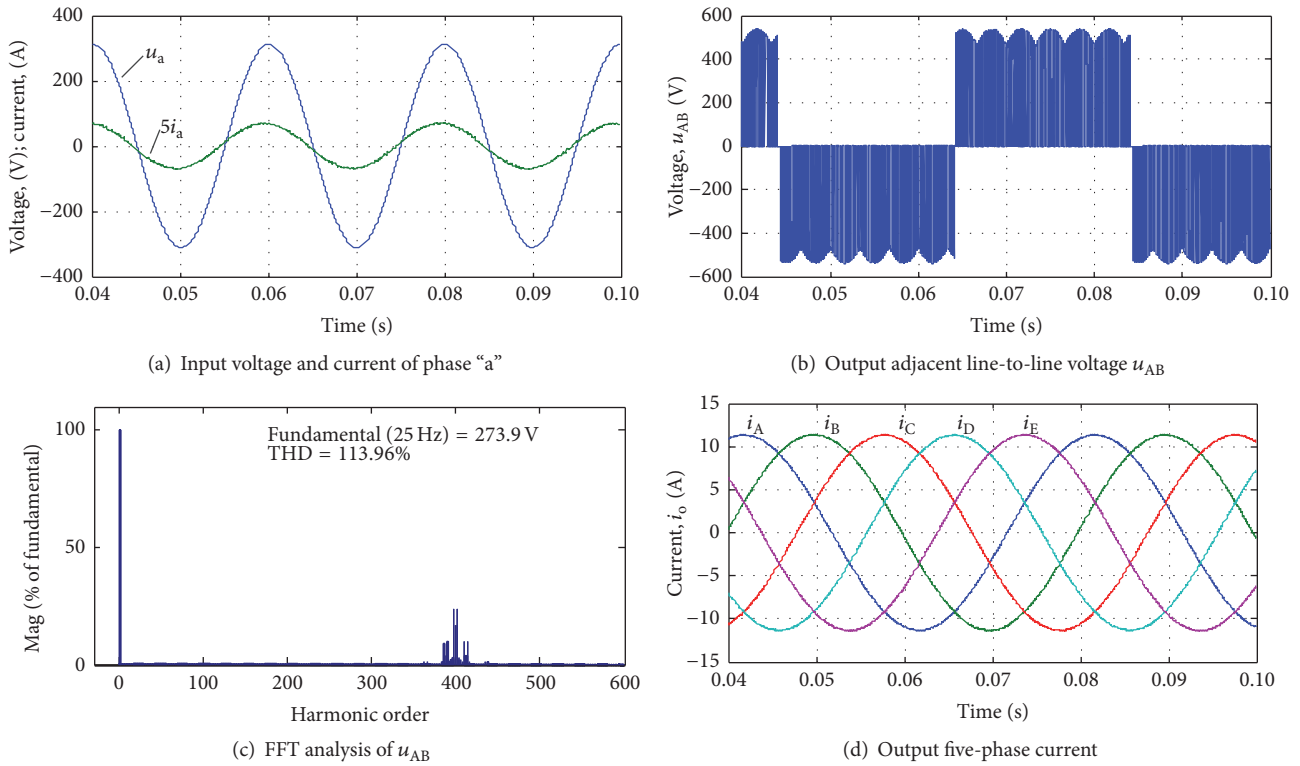
## 5. Simulation Results

In order to verify the feasibility of the proposed CBPWM method, the simulation model of three-to-five-phase IMC is established based on Matlab/Simulink. The parameters of the simulation model are shown in Table 4. The simulation results are shown in Figures 7 and 8.

Figure 7 contains the simulation waveforms of the input voltage $u_a$ and input current $i_a$, output line-to-line voltage $u_{AB}$, FFT analysis of $u_{AB}$, and five-phase output current. From Figure 7(a), the input current $i_a$ becomes almost sinusoidal waveform due to the *LC* filter. However, the *LC* filter causes

Table 3: Switching states and modulation signals in each sector.

| Sector | ON state switches | OFF state switches | Modulation signals |
|---|---|---|---|
| I | $S_{Ap}, S_{Dn}$ | $S_{An}, S_{Dp}$ | $u_{B1}, u_{B2}, u_{C1}, u_{C2}, u_{E1}, u_{E2}$ |
| II | $S_{Bp}, S_{Dn}$ | $S_{Bn}, S_{Dp}$ | $u_{A1}, u_{A2}, u_{C1}, u_{C2}, u_{E1}, u_{E2}$ |
| III | $S_{Bp}, S_{En}$ | $S_{Bn}, S_{Ep}$ | $u_{A1}, u_{A2}, u_{C1}, u_{C2}, u_{D1}, u_{D2}$ |
| IV | $S_{Cp}, S_{En}$ | $S_{Cn}, S_{Ep}$ | $u_{A1}, u_{A2}, u_{B1}, u_{B2}, u_{D1}, u_{D2}$ |
| V | $S_{Cp}, S_{An}$ | $S_{Cn}, S_{Ap}$ | $u_{B1}, u_{B2}, u_{D1}, u_{D2}, u_{E1}, u_{E2}$ |
| VI | $S_{Dp}, S_{An}$ | $S_{Dn}, S_{Ap}$ | $u_{B1}, u_{B2}, u_{C1}, u_{C2}, u_{E1}, u_{E2}$ |
| VII | $S_{Dp}, S_{Bn}$ | $S_{Dn}, S_{Bp}$ | $u_{A1}, u_{A2}, u_{C1}, u_{C2}, u_{E1}, u_{E2}$ |
| VIII | $S_{Ep}, S_{Bn}$ | $S_{En}, S_{Bp}$ | $u_{A1}, u_{A2}, u_{C1}, u_{C2}, u_{D1}, u_{D2}$ |
| IX | $S_{Ep}, S_{Cn}$ | $S_{En}, S_{Cp}$ | $u_{A1}, u_{A2}, u_{B1}, u_{B2}, u_{D1}, u_{D2}$ |
| X | $S_{Ap}, S_{Cn}$ | $S_{An}, S_{Cp}$ | $u_{B1}, u_{B2}, u_{D1}, u_{D2}, u_{E1}, u_{E2}$ |



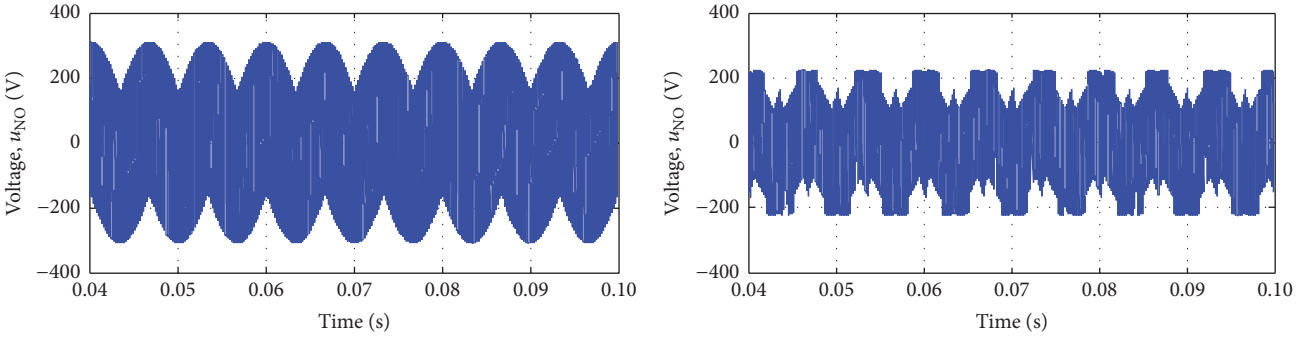

(a) Input voltage and current of phase "a"

(b) Output adjacent line-to-line voltage $u_{AB}$

(c) FFT analysis of $u_{AB}$

(d) Output five-phase current

Figure 7: Input and output waveforms and FFT analysis.




(a) The CMV of conventional modulation strategy

(b) The CMV of the proposed CBPWM method

Figure 8: Waveforms of CMV.

Table 4: The simulation parameters for the simulation model.

| Parameters | Value |
|---|---|
| Input voltage (line-to-line RMS) | $220\sqrt{3}$ V |
| Input frequency | 50 Hz |
| Input filter | $R_f = 0.2\,\Omega$, $L_f = 0.2$ mH, $C_f = 30\,\mu$F |
| Switching frequency | 10 kHz ($T_s = 1 \times 10^{-4}$ s) |
| Output frequency | 25 Hz |
| Voltage transfer ratio | VTR = 0.75 |
| Five-phase *R-L* load | $R = 20\,\Omega$, $L = 30$ mH |

the displacement angle between the input voltage and current at the power supply. From Figures 7(b) and 7(c), the output line-to-line voltage does not contain the low-order harmonic, and the output currents are sinusoidal waveforms in Figure 7(d). It can be confirmed that the sinusoidal output voltages and input currents are obtained by using proposed CBPWM method.

Figure 8 shows the CMV waveforms with the conventional modulation strategies, proposed in [11, 22], and the proposed CBPWM method, respectively. Obviously, the peak value of CMV in Figure 8(a) is 311 V which is equal to the amplitude of input phase voltage. And the peak value of CMV in Figure 8(b) is equal to about 224 V, which is 72% (about $\sqrt{13}/5$) of the amplitude of input phase voltage. In other words, by using the proposed CBPWM method, the CMV is reduced by 28%. It is consistent with the theoretic analysis above.

## 6. Conclusion

In this paper, a CBPWM method to reduce CMV of three-to-five-phase IMC is proposed. To ensure the dc-link is connected to an input phase with the minimum absolute value, the zero vectors are selected and arranged reasonably. Thus, the peak value of CMV can be reduced effectively, which is $\sqrt{13}/5$ times of the amplitude of input phase voltage. The method is implemented by using only one symmetrical triangular carrier signal, which is simple and avoids the complexity of sector combination and lookup tables. Due to the zero vector is assigned to the rectifier stage, the switching times as well as the switching losses are reduced. The correctness of the theoretical analysis is verified by simulation.

## Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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