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Research Article

An Improved Memristive Diode Bridge-Based Band Pass Filter Chaotic Circuit

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By replacing a series resistor in active band pass filter (BPF) with an improved memristive diode bridge emulator, a third-order memristive BPF chaotic circuit is presented. The improved memristive diode bridge emulator without grounded limitation is equivalently achieved by a diode bridge cascaded with only one inductor, whose fingerprints of pinched hysteresis loop are examined by numerical simulations and hardware experiments. The memristive BPF chaotic circuit has only one zero unstable saddle point but causes complex dynamical behaviors including period, chaos, period doubling bifurcation, and coexisting bifurcation modes. Specially, it should be highly significant that two kinds of bifurcation routes are displayed under different initial conditions and the coexistence of three different topological attractors is found in a narrow parameter range. Moreover, hardware circuit using discrete components is fabricated and experimental measurements are performed, upon which the numerical simulations are validated. Notably, the proposed memristive BPF chaotic circuit is only third-order and has simple topological structure.

1. Introduction

Due to the unique nonlinear characteristics of memristors [1], an explosive growth study of memristor based circuits has been boosted up in the past years [2–16]. Unfortunately, induced by technical handicaps in fabricating nanoscale memristor, the commercial memristor is not expected to be available in the near future. Thus, various kinds of physically implementable equivalent circuits which can manifest the three fingerprints of memristors [17] have attracted much attention [2, 6–18]. Popularly, the circuits implemented by operational amplifiers and analog multipliers [7–12] as well as the circuits consisting of diode bridge cascaded with RC [13–15], LC [16], and RLC [18] filters have been used for experimental measurements in memristor based circuits. The most significant feature of the memristive diode bridge emulators is ungrounded limitation, which makes it as a serial expandable and flexible element in designing memristor based circuit [19]. Focusing on simplifying the mathematical model, an improved memristive diode bridge emulator achieved by a diode bridge cascaded with only one inductor will be illustrated in this paper. The newly proposed memristor emulator has simpler structures but more practical application in memristor based circuit.

Numerous memristive dynamical circuits have been reported by introducing memristor into classical linear or nonlinear dynamical circuits [4, 5, 9, 13, 14, 16, 20–23], from which complex dynamical behaviors, such as chaotic behaviors [4, 5, 20, 21], coexisting multiple attractors [9, 13], self-excited and hidden attractors [14, 22, 23], and chaotic and periodic bursting [16], have been revealed and analyzed by theoretical analyses, numerical simulations, and experimental measurements. It is worth noting that the stability depends on the memristor initial condition in a memristive dynamical circuit, leading to the occurrence of coexisting multiple attractors [9, 13]. The coexistence of different kinds of attractors, called multistability, reveals a rich diversity of stable states in nonlinear dynamical systems [12, 24–32] and makes the system offer great flexibility, which can be used for image processing or taken as an additional source of randomness used for many information engineering applications [32–37]. Therefore, it is very attractive to seek for a simple memristive chaotic circuit that has the striking dynamical behavior of coexisting multiple attractors.

In [13, 19], two memristive Chua's circuits are proposed by bridging ungrounded limitation generalized memristors. Meanwhile, a simplest third-order memristive BPF chaotic

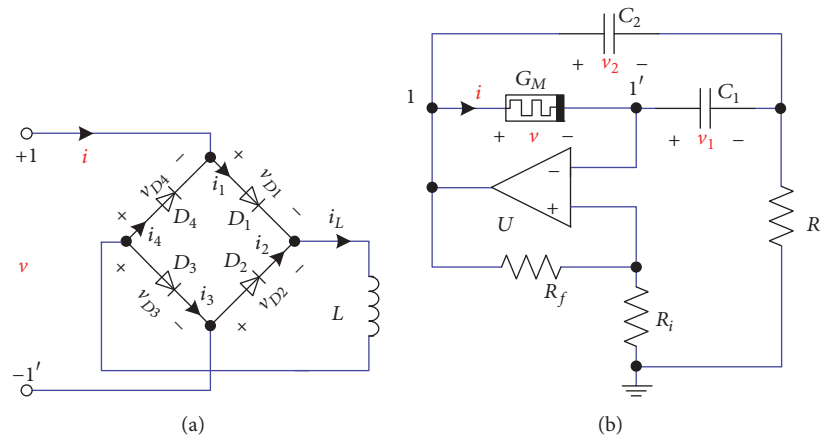


FIGURE 1: Circuit scheme of the memristor emulator and its chaotic circuit. (a) Improved memristive diode bridge emulator; (b) third-order memristive BPF chaotic circuit.

circuit is realized by replacing the parallel resistor in classical BPF with a grounded limitation memristor in [38]. Inspired by the advantages of those methodologies in building chaotic circuit, a novel and simple memristive BPF chaotic circuit with complex dynamical behaviors is constructed from a second-order active BPF by replacing a series resistor with our proposed memristive diode bridge emulator. The newly proposed circuit has extremely simple circuit realization, and the dimension is only three. It is significant that the memristive BPF chaotic circuit has only one determined unstable saddle point and can generate complex dynamical behaviors. Particularly, the new finding of coexisting multiple attractors in such a simple memristive BPF circuit has not been previously reported.

The rest of the paper is organized as follows. In Section 2, the realization and mathematical model of the improved memristive diode bridge emulator is given and its fingerprints by adding sinusoidal voltage stimuli are illustrated. The schematic structure of the memristive BPF circuit and dimensionless state equations are introduced, and stability of the equilibrium point is investigated in Section 3. Complex dynamical behaviors are revealed numerically in Section 4. Coexisting multiple attractors are performed in Section 5. Some hardware experiments are performed to validate the correctness of the theoretical analyses and numerical simulations in Section 6. Finally, the conclusions are drawn in Section 7.

2. Improved Memristive Diode Bridge Emulator

Different from the diode bridge-based memristor emulators reported in [16, 18, 39], an improved memristive diode bridge emulator with much simpler circuit realization is designed as shown in Figure 1(a), where v and i represent the voltage and current at the input port $11'$, respectively, and v_L and i_L stand for the voltage and current across the inductor L.

Consider that the diode bridge is implemented by four unified diodes, where v_{Dk} and i_k represent the voltage across and the current through the diode D_k ($k = 1, 2, 3, 4$), respectively. The voltage and current relation for D_k can be written as

$$i_k = I_S\left(e^{2\rho v_{Dk}} - 1\right), \tag{1}$$

where $\rho = 1/(2nV_T)$ and I_S, n, and V_T are the model parameters of D_k, which stand for the reverse saturation current, emission coefficient, and thermal voltage of the diode, respectively.

According to [39], there are two relations of $v_{D1} = v_{D3}$ and $v_{D2} = v_{D4}$. By applying Kirchhoff's laws, two node current equations are obtained as

$$i = i_1 - i_2, \tag{2}$$

$$i_L = i_1 + i_2 \tag{3}$$

and two loop voltage equations are yielded as

$$v_{D2} = v_{D1} - v, \tag{4}$$

$$2v_{D1} = v - v_L. \tag{5}$$

By substituting (1) and (3) into (4), the voltage across D_1 can be solved as

$$v_{D1} = \frac{1}{2\rho}\ln\left[\frac{(2I_S + i_L)\exp(\rho v)}{2I_S\cosh(\rho v)}\right]. \tag{6}$$

Then, by combining (1), (2), and (4) with (6), the voltage and current relation at the input port $11'$ can be expressed as

$$i = (2I_S + i_L)\tanh(\rho v). \tag{7}$$

By leading (6) into (5) and using $v_L = L\mathrm{d}i_L/\mathrm{d}t$, the state equation of inductor L is modeled as

$$L\frac{\mathrm{d}i_L}{\mathrm{d}t} = v - \frac{1}{\rho}\ln\left[\frac{(2I_S + i_L)\exp(\rho v)}{2I_S\cosh(\rho v)}\right]. \tag{8}$$

The mathematical models (7) and (8) are used to characterize the voltage and current relation of the improved memristive

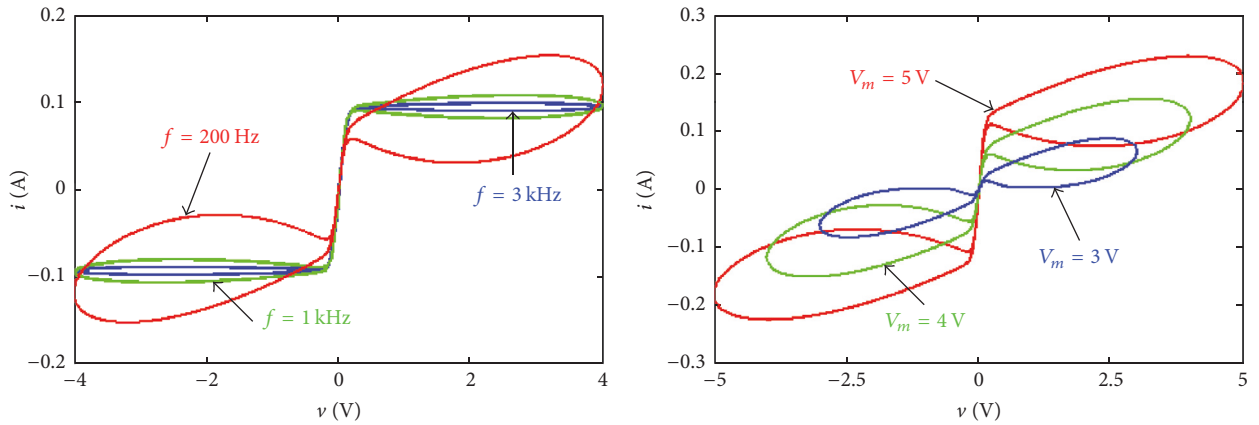


FIGURE 2: Pinched hysteresis loops of the improved memristive diode bridge emulator in the v-i plane. (a) $V_m = 4$ V with different frequencies; (b) $f = 200$ Hz with different amplitudes.

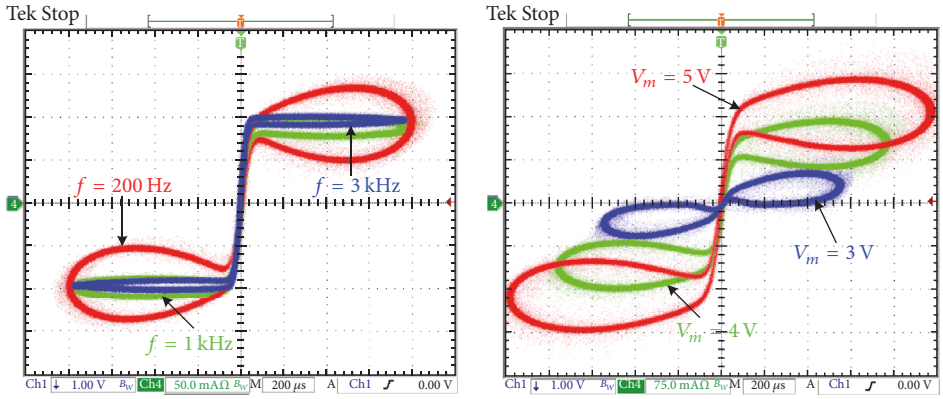


FIGURE 3: Experimentally measured pinched hysteresis loops of the improved memristive diode bridge emulator. (a) $V_m = 4$ V with different stimulus frequencies; (b) $f = 200$ Hz with different stimulus amplitudes.

diode bridge emulator, which accords with the defining equations of the class of generalized memristors [4] and it can be implemented by inexpensive off-the-shelf discrete components easily.

In order to illustrate the frequency-dependent pinched hysteresis loops of the improved memristive diode bridge emulator, the circuit element parameters $L = 10$ mH and four 1N4148 diodes with $I_S = 5.84$ nA, $n = 1.94$, and $V_T = 25$ mV are selected, and a sinusoidal voltage source is considered as $v = V_m \sin(2\pi f t)$, where V_m and f are the stimulus amplitude and frequency, respectively.

When $V_m = 4$ V is fixed and f is set to 200 Hz, to 1 kHz, and to 3 kHz, respectively, the v-i curves are displayed in Figure 2(a), from which it can be seen that the hysteresis loops are pinched at the origin, and the lobe area decreases with the increase of the frequency, while when $f = 200$ Hz is fixed and V_m is set to 3 V, to 4 V, and to 5 V, respectively, the v-i curves are plotted in Figure 2(b), which explains that the pinched hysteresis loop is regardless of the stimulus amplitude. The simulation results in Figure 2 show that the improved memristive diode bridge emulator can exhibit three fingerprints for identifying memristors [17].

Also, a hardware level on a breadboard is fabricated and Tektronix AFG 3102C is used to generate a sinusoidal voltage. The experimental results, as shown in Figure 3, are captured by Tektronix TDS 3034C to validate three fingerprints of the memristor emulator, from which the results from hardware circuit are unanimous to those revealed by numerical simulations. It is emphasized that the minor deviations are caused by small difference between numerical simulations and experimental measurements of the inductor L parameter.

3. Third-Order Memristive BPF Chaotic Circuit

A second-order active BPF circuit has a simple circuit topology, which contains only one amplifier, two capacitors, and four resistors [40]. In this paper, by replacing a series resistor with the proposed memristive diode bridge emulator, a third-order memristive BPF circuit is proposed, as shown

in Figure 1(b). Therefore, the proposed memristive chaotic circuit is much simpler and more intuitive in practical realization than other memristive chaotic circuits reported in [13–16].

3.1. Mathematical Model. The proposed circuit has three dynamic elements of capacitor C_1, capacitor C_2, and memristor G_M, respectively, corresponding to three state variables of v_1, v_2, and i_L. According to Kirchhoff's circuit laws and constitutive relationships of basic circuit elements, a state equation set is written as

$$\begin{aligned} C_1\frac{dv_1}{dt} &= (2I_S + i_L)\tanh(\rho v),\\ C_2\frac{dv_2}{dt} &= \frac{kv_2 - (k+1)v_1}{R} - (2I_S + i_L)\tanh(\rho v),\\ L\frac{di_L}{dt} &= v - \frac{1}{\rho}\ln\left[\frac{(2I_S + i_L)\exp(\rho v)}{2I_S\cosh(\rho v)}\right], \end{aligned} \tag{9}$$

where $v = v_2 - v_1$ and $k = R_i/R_f$.

Denote

$$\begin{aligned} x &= \rho v_1,\\ y &= \rho v_2,\\ z &= \rho R i_L,\\ C_1 &= C_2 = C,\\ \tau &= \frac{t}{RC},\\ a &= \frac{R^2C}{L},\\ c &= 2\rho R I_S,\\ \dot{u} &= \frac{du}{d\tau}, \quad (u \equiv x, y, z). \end{aligned} \tag{10}$$

Equation (9) can be rewritten in a dimensionless form as

$$\begin{aligned} \dot{x} &= (c+z)\tanh(y-x),\\ \dot{y} &= ky - (k+1)x - (c+z)\tanh(y-x),\\ \dot{z} &= a\ln[c\cosh(y-x)] - a\ln(c+z). \end{aligned} \tag{11}$$

Thus the parameter amount of the dimensionless equation (11) will decrease to three.

The circuit parameters shown in Figure 1 are selected as $C_1 = C_2 = 20$ nF, $L = 10$ mH, $R = 50\ \Omega$, $R_i = 50\ \Omega$, $R_f = 1$ kΩ, and four 1N4148 diodes with $I_S = 5.84$ nA, $n = 1.94$, $V_T = 25$ mV, which are used as typical circuit parameters. Therefore, the normalized parameters are calculated by (10) as

$$\begin{aligned} a &= 5\times10^{-3},\\ c &= 6.02\times10^{-6},\\ k &= 0.05. \end{aligned} \tag{12}$$

In our following work, the parameters given in (12) will be taken as typical system parameters to reveal dynamical behaviors in the third-order memristive BPF circuit.

3.2. Stability Analysis. Obviously, system (11) has only one zero equilibrium point $\mathbf{S}(0,0,0)$. By linearizing (11) around the equilibrium point $\mathbf{S}$ and keeping $k = 0.05$ unchanged, the Jacobian matrix is obtained as

$$\mathbf{J} = \begin{bmatrix} -c & c & 0\\ c - 1.05 & 0.05 - c & 0\\ 0 & 0 & -\dfrac{a}{c} \end{bmatrix}. \tag{13}$$

Thus, the eigenvalues at equilibrium point $\mathbf{S}$ are yielded by solving the following characteristic equation:

$$\det(\mathbf{1}\lambda - \mathbf{J}) = \left(\lambda + \frac{a}{c}\right)\left[\lambda^2 + (2c - 0.05)\lambda + c\right] = 0. \tag{14}$$

Correspondingly, the eigenvalues at equilibrium point $\mathbf{S}$ are expressed as

$$\begin{aligned} \lambda_{1,2} &= 0.025 - c \pm \sqrt{(c-0.025)^2 - c},\\ \lambda_3 &= -\frac{a}{c}. \end{aligned} \tag{15}$$

It is notable that the values of $\lambda_{1,2}$ and the symbol of λ_3 at $\mathbf{S}$ are considered to remain unchanged with $c = 6.02\times10^{-6}$ and positive a. For the typical system parameters, the eigenvalues at $\mathbf{S}$ are calculated as

$$\begin{aligned} \lambda_1 &= 0.0499,\\ \lambda_2 &= 0.0001,\\ \lambda_3 &= -830.5648 \end{aligned} \tag{16}$$

which implies that $\mathbf{S}$ is always an unstable saddle.

3.3. Typical Chaotic Attractor. For the typical system parameters of (12) and the initial conditions of $(0, 0.01, 0)$, phase portraits of the typical chaotic attractor in three different planes are numerically simulated by solving system (11) and shown in Figures 4(a), 4(b), and 4(c), respectively, and Poincaré mapping on $y = 0$ section is depicted in Figure 4(d). It is noted that the proposed third-order memristive BPF circuit can generate chaos indeed.

4. Dynamical Behaviors in Memristive BPF Chaotic Circuit

Consider that the parameter a increases from 0.001 to 0.1 and the other parameters are selected as given in (12). Bifurcation diagrams of the system variable x and first two Lyapunov exponents calculated by Wolf's method [41] are presented as shown in Figure 5. Two sets of initial states, positive initial conditions $(0, 0.01, 0)$ colored in red and negative initial conditions $(0, -0.01, 0)$ colored in blue, are utilized in Figure 5(a). From Figure 5, striking dynamical behaviors including period, chaos, period doubling bifurcation, and coexisting bifurcation modes are observed. Different transitions to chaotic states, such as forward period doubling and crisis scenario are also discovered. The dynamical behaviors

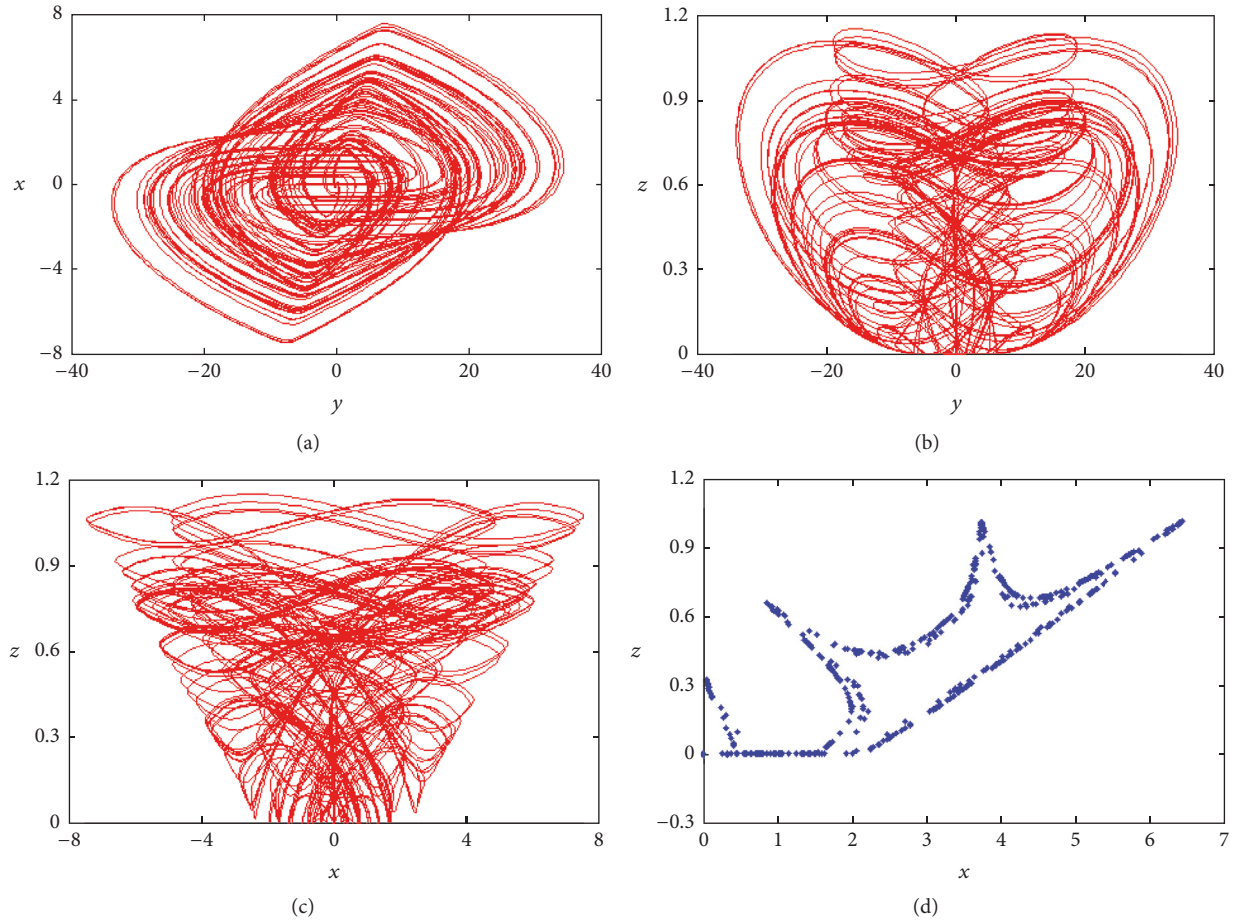


FIGURE 4: Numerically simulated chaotic attractor under typical system parameters. (a) Phase portrait in the y-x plane; (b) phase portrait in the y-z plane; (c) phase portrait in the x-z plane; (d) Poincaré mapping in the x-z plane.

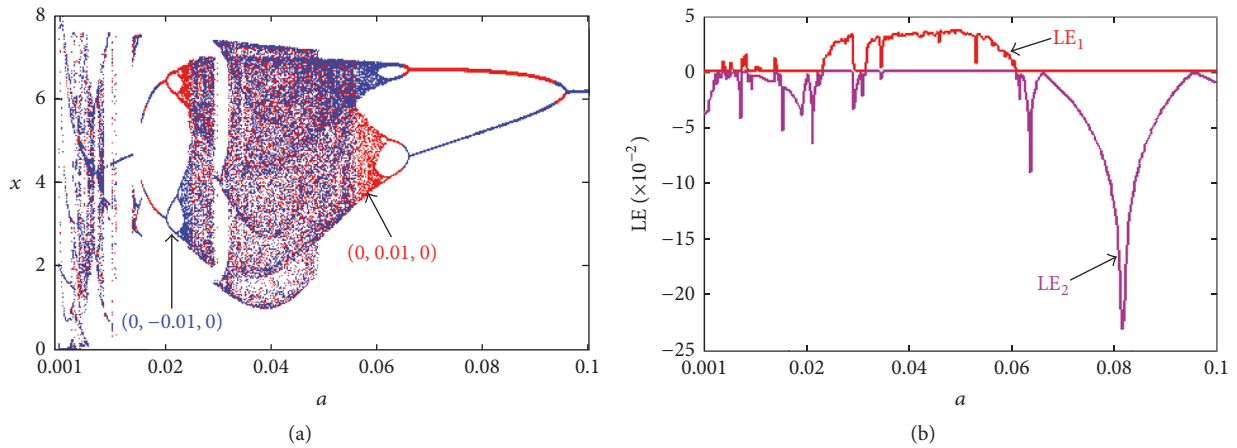


FIGURE 5: Dynamics with a increasing in the memristive BPF chaotic circuit. (a) Bifurcation diagrams of x; (b) first two Lyapunov exponents.

determined by the Lyapunov exponents are consistent well with those revealed by the bifurcation diagrams. Note that the bifurcation diagrams in the narrow region of $0.0145 < a < 0.017$ have imperfect bifurcation structures, that is, without bifurcation route from period to chaos. Therefore, there must exist an attractive basin with special initial conditions to be located [9]. Under these special initial conditions, a period doubling bifurcation route can be found in system (11), which leads to the coexistence of multiple attractors.

When $0.001 \leq a \leq 0.004$, system (11) shows periodic behavior, while when $0.004 < a \leq 0.015$, the first Lyapunov exponent is zero or positive alternately, which indicates the occurrences of periodic and chaotic behaviors. With the intervals of a in $0.015 < a \leq 0.025$ and $0.056 \leq a \leq 0.096$, the

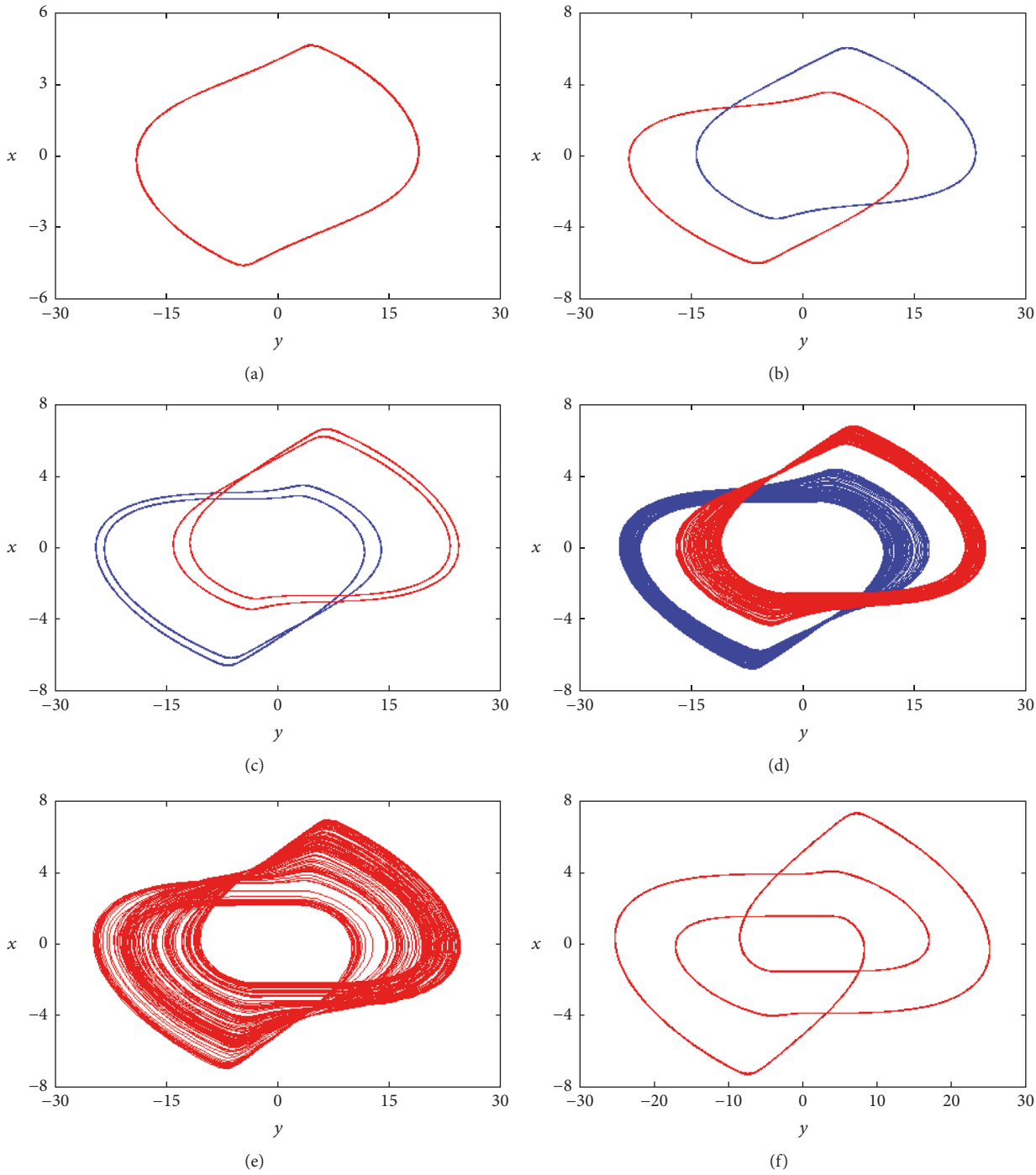


Figure 6: Numerically simulated phase portraits with different a in the y-x plane. (a) Period-1 limit cycle at $a = 0.014$; (b) coexisting period-1 limit cycles at $a = 0.018$; (c) coexisting period-2 limit cycles at $a = 0.022$; (d) coexisting chaotic attractors at $a = 0.025$; (e) chaotic attractor at $a = 0.028$; (f) period-3 limit cycle at $a = 0.031$.

occurrences of period doubling bifurcation, reverse period doubling, and coexisting bifurcation modes are discovered. In $0.025 < a < 0.056$, system (11) locates in the region of chaos with a larger periodic windows near $a = 0.03$.

For different values of a, phase portraits of system (11) in the y-x plane are numerically simulated, as shown in Figure 6, where the initial conditions of the red and blue trajectories are the same as those used in Figure 5(a). These results just emulate the dynamical behaviors of period, chaos, period doubling bifurcation, and coexisting bifurcation modes emerging from system (11). Note that the chaotic attractor in Figure 6(e) is spiral structure, similar to that revealed in the delay system [42].

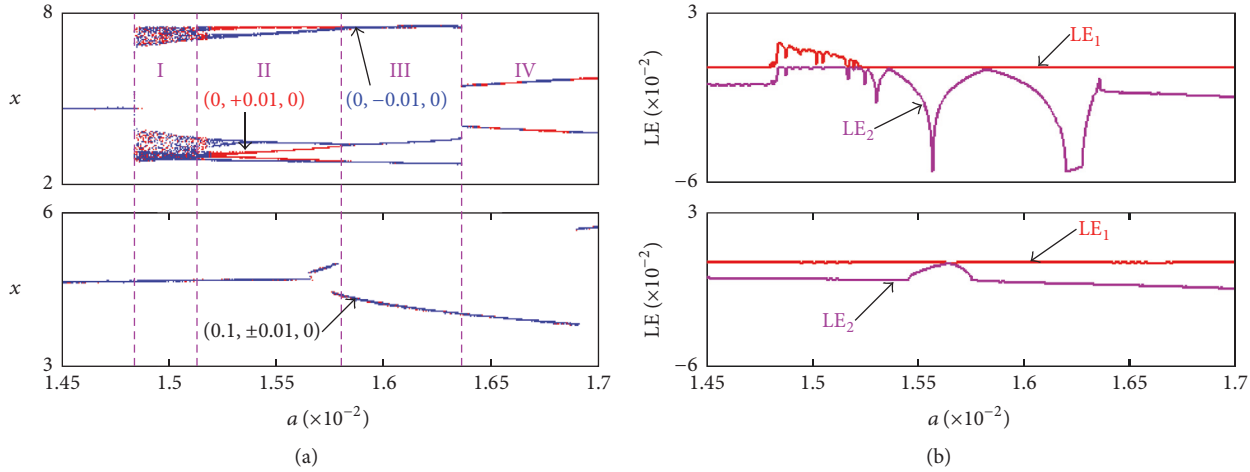


Figure 7: Bifurcation routes in the region of $0.0145 \le a \le 0.017$ with different initial states. (a) Bifurcation diagrams of x under $(0, \pm 0.01, 0)$ and $(0.1, \pm 0.01, 0)$; (b) first two Lyapunov exponents under $(0, \pm 0.01, 0)$ and $(0.1, \pm 0.01, 0)$.

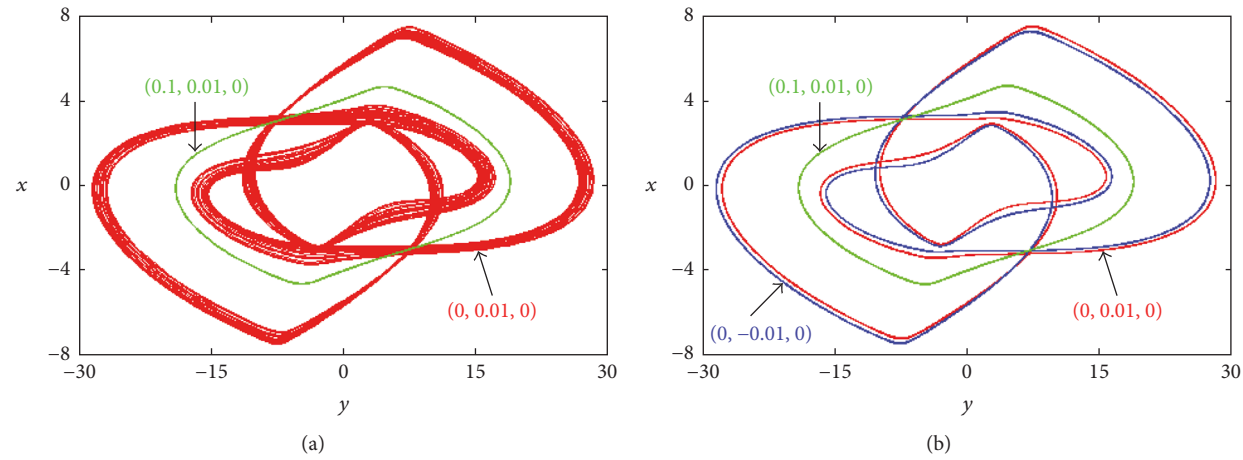


Figure 8: Simulated multiple attractors. (a) Coexisting chaotic attractor and limit cycle with $a = 0.015$; (b) coexisting twin limit cycles and limit cycle with $a = 0.0155$.

5. Multiple Attractors Depending on the Initial Conditions

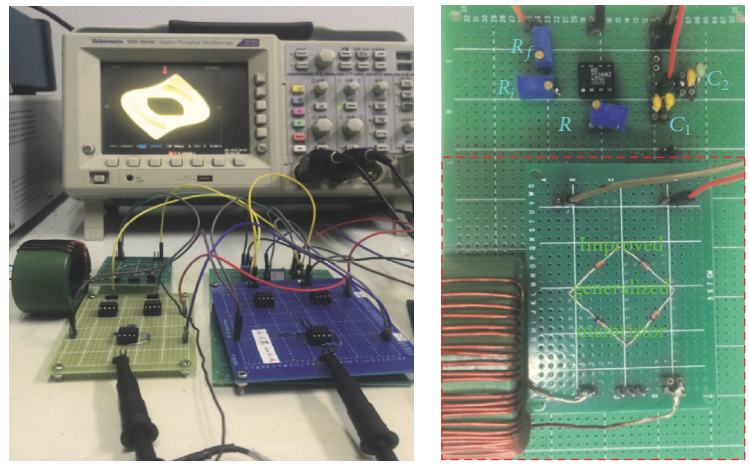
In this section, the special phenomenon of coexisting multiple attractors in system (11) is mainly concerned. The bifurcation diagrams of x and Lyapunov exponents in the region of $0.0145 \le a \le 0.017$ under different initial conditions are presented in Figure 7 to highlight the phenomenon of multiple attractors. The initial conditions are specified as $(0, \pm 0.01, 0)$ and $(0.01, \pm 0.01, 0)$ and the color settings are marked in Figure 7(a), respectively. Note that there exists different bifurcation route in concerned parameter region for different initial conditions, which leads to the existence of multiple attractors.

In Figure 7(a), the narrow parameter range of a can be divided into four different regions of I, II, III, and IV. In region I, two kinds of coexisting attractors, including chaotic attractor and limit cycle, are revealed. Coexisting limit cycles with different periods are given in region III, while, in regions II and IV, coexisting twin limit cycles and limit cycle are observed. Within two regions, phase portraits of coexisting multiple attractor with different topological structures are plotted in Figure 8.

6. Experimental Verifications

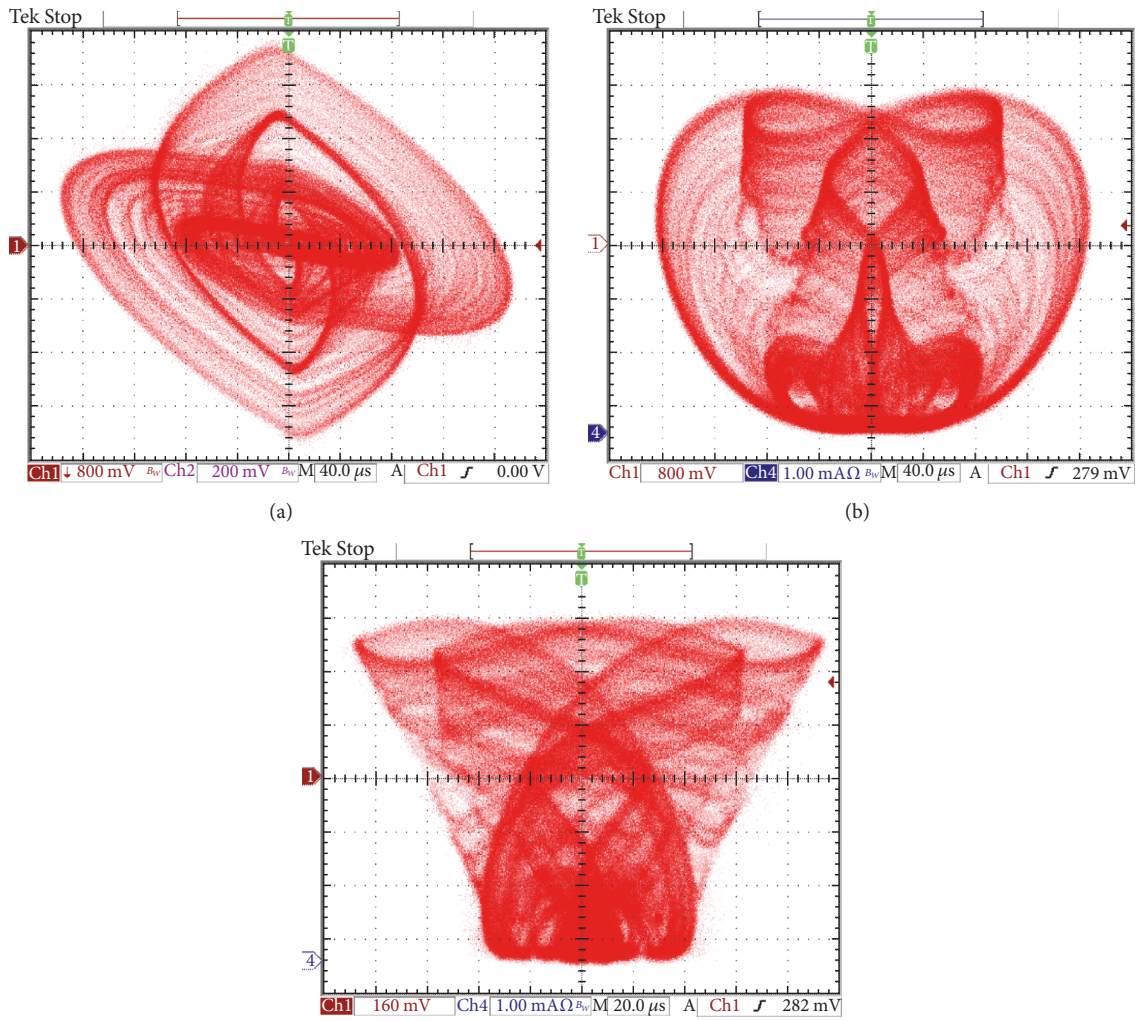
A hardware level on a breadboard is fabricated to validate the complex dynamics of the proposed memristive BPF chaotic circuit. The experimental prototype for the memristive BPF chaotic circuit is photographed and shown in Figure 9, where the passive elements of precision potentiometer and monolithic ceramic capacitor and manually winding inductor as well as the active devices of operational amplifier AD711KN with ±15 V DC power supplies are chosen in our experiment. Note that two auxiliary gadget circuits are hired in experimental measurements to obtain the terminal voltages of capacitors C_1 and C_2. Additionally, the experimental results are captured by a Tektronix TDS 3034C digital oscilloscope in XY mode.

Phase portraits in different planes under typical circuit parameters are easily observed, as shown in Figure 10. For



(a) (b)

FIGURE 9: Photograph of the experimental prototype for the memristive BPF chaotic circuit: (a) is a global graph of digital oscilloscope connecting with hardware circuit breadboard, whereas (b) is an enlarged view of proposed hardware circuit breadboard.



(a) (b)

(c)

FIGURE 10: Experimentally measured phase portraits under typical circuit parameters in different planes, where $R = 50\,\Omega$, $R_i = 50\,\Omega$, $R_f = 1\,\text{k}\Omega$, $L = 10\,\text{mH}$, and $C_1 = C_2 = 20\,\text{nF}$. (a) Phase portrait in the v_2-v_1 plane; (b) phase portrait in the v_2-i_L plane; (c) phase portrait in the v_1-i_L plane.

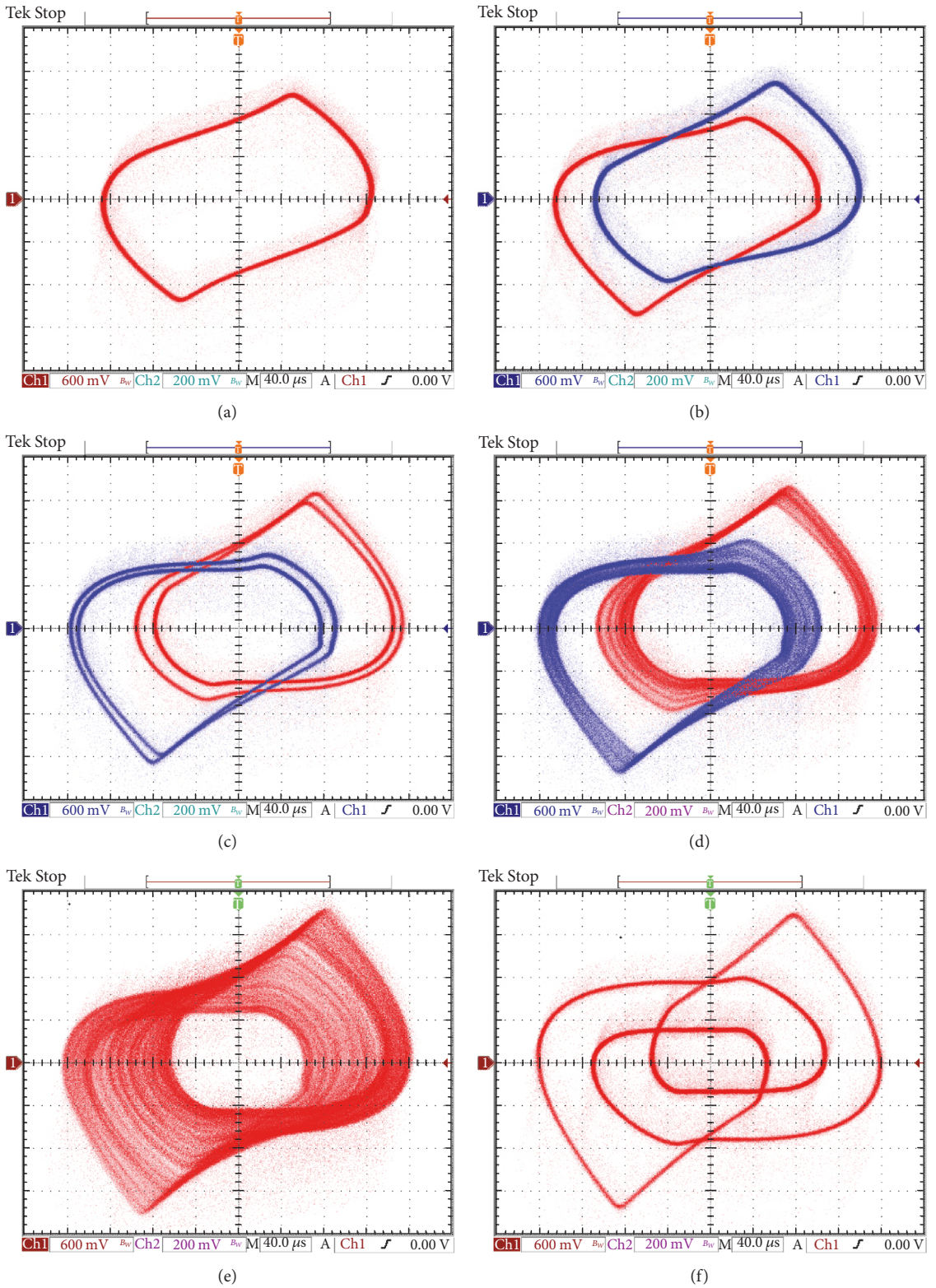


FIGURE 11: Experimentally measured phase portraits in the v_2-v_1 plane with different C_1 and C_2, where $R = 50\,\Omega$, $R_i = 50\,\Omega$, $R_f = 1\,\text{k}\Omega$, and $L = 10\,\text{mH}$. (a) Period-1 limit cycle at $C_1 = C_2 = 56\,\text{nF}$; (b) coexisting period-1 limit cycles at $C_1 = C_2 = 72\,\text{nF}$; (c) coexisting period-2 limit cycles at $C_1 = C_2 = 94\,\text{nF}$; (d) coexisting chaotic attractors at $C_1 = C_2 = 105\,\text{nF}$; (e) chaotic attractor at $C_1 = C_2 = 115\,\text{nF}$; (f) period-3 limit cycle at $C_1 = C_2 = 126\,\text{nF}$.

convenience, the two capacitors C_1 and C_2 are adjusted to meet the variation of dimensionless parameter a in our experimental measurements. When the two capacitors C_1 and C_2 turned as six different values, phase portraits in the v_2-v_1 plane are measured, as shown in Figure 11, where the phase portraits of coexisting attractors in Figures 11(b)–11(d) are captured separately and handed with after-treatment. It is emphasized that the desired different initial capacitor voltages and inductor current are difficult to assign in hardware circuit, which are randomly sensed through turning on the hardware circuit power supplies again [9, 13]. Ignoring the minor deviations caused by parasitic parameters, the experimental results shown in Figures 10 and 11 match well with the results of numerical simulations in Figures 4 and 6.

7. Conclusion

In this paper, a third-order memristive BPF chaotic circuit is presented, which is constructed by replacing a resistor in second-order active BPF with an improved memristive diode bridge emulator. Numerical simulations of the mathematical model and the corresponding hardware experiments are performed, which show that the memristive BPF chaotic circuit has only one zero unstable saddle and generates complex dynamical behaviors of period, chaos, period doubling bifurcation, and coexisting bifurcation modes. The most significant feature of the proposed memristive chaotic circuit is that the stability depends on the initial conditions of dynamic elements, thereby leading to the occurrence of coexisting multiple attractors. Besides, the proposed memristor is much simpler in practical circuit realization and the constructing memristive BPF chaotic circuit is realized with less discrete components.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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