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Research Article

Virtual Space Vector Pulse Width Modulation for Asymmetric *T*-Type Neutral Point Clamped 3-Level Inverter

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This paper proposes a novel 3-phase asymmetric 3-level *T*-type NPC inverter and studies its PWM performance using a virtual space vector pulse width modulation control strategy. Firstly, the mathematical model and characteristics of this economical topology are described. Then, a virtual space vector approach is proposed to build a space vector diagram for designing SVPWM control. Similar to the conventional 3-level NPC inverter, the asymmetric inverter can also work with the neutral point voltage self-balancing in a fundamental period, which enables employment of this topology in various applications. Finally, simulation and experiment results under different load conditions have shown good output performance of the asymmetric 3-level topology. Similar tests are also performed on both conventional 2-level and 3-level inverters for comparison. For an almost similar number of different voltage vectors in the space vector diagram, the asymmetric 3-level topology can compete with conventional 3-level inverters for low-cost applications. The obvious benefit of the asymmetric 3-level inverter is a smaller number of switches devices while it can achieve output performance similar to that of the conventional 3-level. The comparative investigation also shows that the total loss given by SVPWM for the asymmetric 3-level configuration is lower than that of the traditional 3-level inverter.

1. Introduction

Three-level converters have been widely used in industrial applications, which includes high-power motor drivers [1], grid connection for renewable energy systems [2, 9], and electric vehicles [3]. In particular, in high-power and medium-voltage applications, it has outstanding advantages compared with 2-level converters, such as better total harmonic distortion (THD), lower switching losses, and reduced voltage stress dv/dt across the power devices [4–6]. These most common topologies are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) types. In fact, NPC converters are being widely used. Among them, the *T*-type NPC was shown to be more efficient than the traditional NPC up to the medium switching frequency range [7–13]. This topology does not use clamping diodes, and the number of power switches is the same as the NPC converters.

For overall good performances in relation to loss distribution, high efficiency compared with conventional 3L-NPC, *T*-type NPC legs have been commercialized by many manufacturers such as Semikron, Infineon, Mitsubishi, and Fuji [14, 15]. Many modified T-NPC structures have been introduced to satisfy different purposes. For example, an advanced *T*-NPC (AT-NPC) structure using a reverse blocking IGBT (RB-IGBT) instead of two conventional IGBTs at the T-leg connected to the neutral point has been studied [16–18]. This structure reduces the conduction voltage drop and related device loss when the neutral point is connected to outputs. Another topology named combined AT-NPC and quasi-Z source impedance converter presents an attractive and economic solution for renewable energy

applications with low DC input voltage [19]. Recently, numerous research studies on utilizing wide band gap devices for T-type converters also draw much intention from researchers [20, 21]. One of the major trends in modern power converters is to design higher multilevel converters for high-power and high-voltage applications. Because there are no topologies from NPC, FLC and cascaded inverters can meet various demands in practice and many hybrid multilevel topologies were designed and shown as good solutions for industry. For this aim, several five-level hybrid T-type NPC inverters were presented in the recent literature [22–25].

Although 3-level NPC inverters have many advantages compared with 2-level inverters, as mentioned above, they have some disadvantages, such as an increased system volume, higher cost, and reduced reliability due to more switches. Many recent studies focus on developing reduced switched topologies [26–32] to improve system reliability, reducing size and cost. In [26–29], the diode NPC 3-level 2-leg topology was proposed in which the required number of switches is reduced from 12 IGBTs and 6 diodes to 8 IGBTs and 4 diodes. A similar structure for the T-type has been proposed to eliminate the diodes [32]. These topologies only need two legs for a three-phase 3-level inverter, so the number of components is reduced by one-third, as shown in Figure 1(a). However, a drawback is that the linear output voltage is limited to half, as shown in Figure 1(b).

This paper proposes a so-called asymmetric 3-level T-type NPC inverter by adding a half-bridge leg to the 2-leg 3-level NPC inverter. This new configuration, as shown in Figure 2, enables twice the output voltage range compared with Figure 1. In order to evaluate and compare the PWM performance of the novel topology with conventional 2-level and 3-level inverters, virtual space vectors and the related virtual space vector pulse width modulation (VSVPWM) control will be proposed and designed. Simulations and experiments are performed to demonstrate the effectiveness and feasibility of the asymmetric T-type NPC 3-level inverter.

2. Circuit Analysis and Mathematical Model

The asymmetric inverter topology is illustrated in Figure 2. The phase leg B is a half-bridge; phases A and C are 3-level T-type legs. The DC-bus voltage is supplied via two DC-link capacitors (c_1, c_2) in series. Three-phase load R-L is connected to the output terminals of the converter.

Under the condition of balanced DC-link capacitor voltages, the voltage from the output terminal to the negative of the DC-bus can be expressed as follows:

$$v_{XN} = S_X \frac{V_{\mathrm{dc}}}{2}, \tag{1}$$

where $X \in \{A, B, C\}$ and S_X is the switching state and defined in terms of the IGBT states per phase legs. For 3-level leg phases A and C, S_X can be 0, 1, and 2. For 2-level leg phase B, S_X can be 0, 2. The switching states of the three phases A, B, and C are described in Table 1.

The Clarke formula transforms the voltage vector in the abc to $\alpha\beta$ coordinate system as follows:

$$\vec{V}_k = \frac{2}{3}\left(v_{AN} + e^{j2\pi/3} v_{BN} + e^{j4\pi/3} v_{CN}\right), \tag{2}$$

where $\vec{V}_k$ is the output voltage vector of the inverter in the $\alpha\beta$ coordinate system and k is denoted as the vector index.

The converter generates 18 voltage vectors, including 2 redundant zero voltage vectors (ZV), 6 small voltage vectors (SV), 4 medium-voltage vectors (MV), and 6 large voltage vectors (LV) illustrated in Figure 3. Compared with 7 and 19 difference vectors used in 2-level and 3-level NPC inverters, respectively, the number of difference vectors in the asymmetric NPC is 17, nearly identical to the NPC. So, it is expected that the performance of the asymmetric PWM control will be as good as the 3-level NPC inverter.

Form (1), the line voltage between two terminal legs is rewritten and deduced as follows:

$$\begin{cases} v_{AB} = v_{AN} - v_{BN} = \dfrac{1}{2} V_{\mathrm{dc}} \left(S_A - S_B\right), \\ v_{BC} = v_{BN} - v_{CN} = \dfrac{1}{2} V_{\mathrm{dc}} \left(S_B - S_C\right), \\ v_{CA} = v_{CN} - v_{AN} = \dfrac{1}{2} V_{\mathrm{dc}} \left(S_C - S_A\right). \end{cases} \tag{3}$$

With the switching state S_X as defined in Table 1, applying the above analysis for the 2-level and 3-level conventional converters, the specific characteristics of each type are compared with the asymmetric configuration reported in Table 2. The asymmetric converter generates line voltages at 5 voltage levels $\pm V_{\mathrm{dc}}$, $\pm (1/2) V_{\mathrm{dc}}$, and 0, similar to traditional 3-level converters.

3. Virtual SVPWM for Asymmetric Inverter

The reference voltage vector $\vec{V}_{\mathrm{ref}}$ can be synthesized in relation with the switching states S_X on the phase legs, with $X \in \{A, B, C\}$, as follows:

$$\vec{V}_{\mathrm{ref}} = \left(S_A + S_B e^{j2\pi/3} + S_C e^{j4\pi/3}\right) \frac{V_{\mathrm{dc}}}{3}. \tag{4}$$

We define $V_{(1)\max}$ as the maximum amplitude of the reference vector in the linear modulation range, corresponding to the radius of the largest circle inscribed in the hexagon. The modulation index is defined as follows:

$$m_a = \frac{V_{(1)\max}}{\left(V_{\mathrm{dc}}/\sqrt{3}\right)}. \tag{5}$$

It can be seen that the maximum amplitude of $V_{(1)\max} = V_{\mathrm{dc}}/\sqrt{3}$, and asymmetric 3-level achieves the same maximum voltage as traditional symmetric configurations.

The space vector diagram of the asymmetric inverter in Figure 3 lacks two medium-voltage vectors, $\vec{V}_{210}$ and $\vec{V}_{012}$,

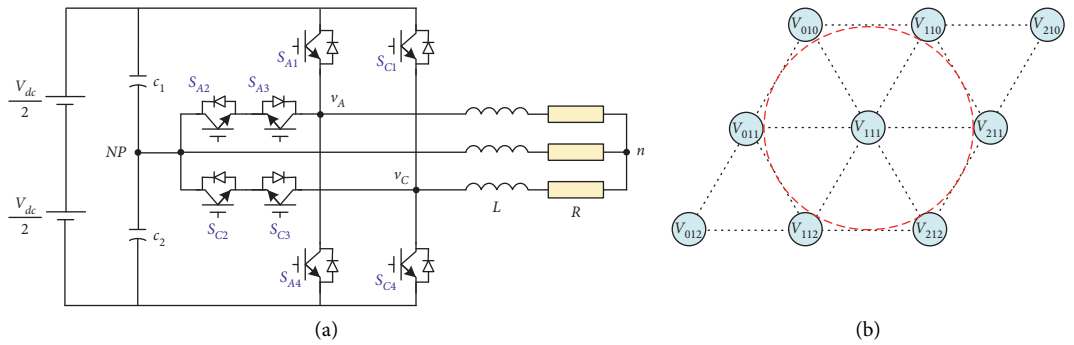

FIGURE 1: Structure of the two legs T-type 3-level inverter: (a) the topology of the two legs T-type 3-level inverter; (b) space vector diagram of the two legs T-type 3-level inverter.

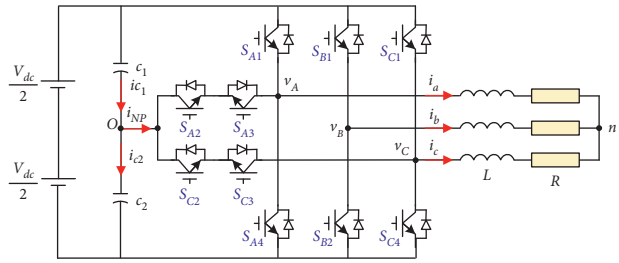

FIGURE 2: Structure of the asymmetric inverter.

TABLE 1: Switching states and output voltages of the asymmetric inverter.

For phase X with $X \in \{A, C\}$						For phase B			
Switching state	Device state				Output voltage	Switching state	Device state		Output voltage
S_X	S_{X1}	S_{X2}	S_{X3}	S_{X4}	v_{XN}	S_B	S_{B1}	S_{B2}	v_{BN}
2	1	1	0	0	V_{dc}	2	1	0	V_{dc}
1	0	1	1	0	$(1/2)V_{\mathrm{dc}}$	—	—	—	—
0	0	0	1	1	0	0	0	1	0

in sectors I and IV, respectively. To apply the SVPWM technique of the traditional 3-level into asymmetric topology, two virtual vectors are proposed and added to the space vector diagram as illustrated in Figure 4, defined as follows:

$$\begin{cases} \overrightarrow{V}_{210}^{\mathrm{vir}} = \dfrac{1}{2}\overrightarrow{V}_{200} + \dfrac{1}{2}\overrightarrow{V}_{220}, \\ \overrightarrow{V}_{012}^{\mathrm{vir}} = \dfrac{1}{2}\overrightarrow{V}_{002} + \dfrac{1}{2}\overrightarrow{V}_{022}. \end{cases} \tag{6}$$

3.1. Identify Region of Sectors. As in Figure 4, each sector is divided into 4 regions numbered 1 to 4. The SVPWM technique for $\overrightarrow{V}_{\mathrm{ref}}$ will be solved for sector I, and these results will be properly deduced for other sectors.

The reference voltage vector synthesized by the three nearest voltage vectors, which are determined through the region where the reference vector is located, is as follows [33]:

$$\begin{cases} d_1 = m_a \sin\left(\dfrac{\pi}{3} - \theta_I\right), \\ d_2 = m_a \sin\left(\theta_I\right). \end{cases} \tag{7}$$

The region identification is related to d_1 and d_2 as follows:

If $(d_1 + d_2) \le 0.5$, then region 1

If $d_1 > 0.5$, then region 3

I $d_2 > 0.5$, then region 4

Else region 2

The remaining sectors will be converted to sector I. Therefore, the reference vector will be calibrated so that the modified angle θ_I falls between 0 and $\pi/3$, that is,

$$\theta_I = \theta_k - (k-1)\frac{\pi}{3}, \tag{8}$$

where $k = 2, \ldots, 6$ for sectors II, ..., VI, respectively.

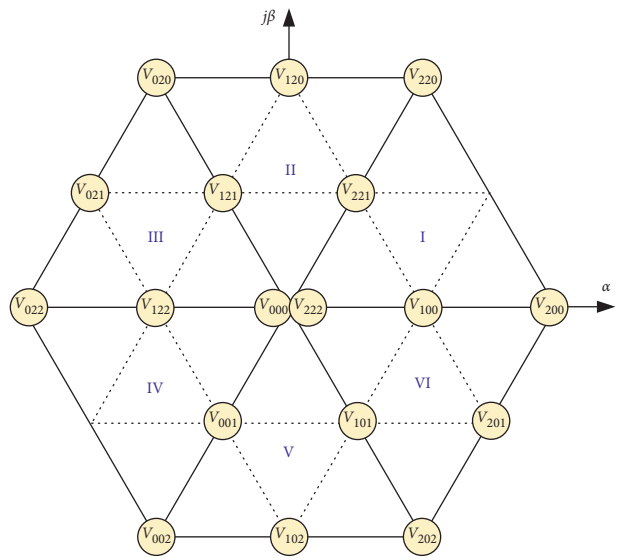

Figure 3: Space vector diagram of asymmetric T-type 3-level NPC inverter.

3.2. Duty Cycle Calculation. The duty cycle for the voltage vector at the vertices of the triangle where the reference vector is placed essentially represents the dwell time of the selected switching states during the sampling interval T_s. For example, the reference vector in region 3 of sector I, as shown in Figure 5, is synthesized by voltage vectors $\vec{V}_{100}$, $\vec{V}_{210}^{\text{vir}}$, and $\vec{V}_{200}$ over a sampling period, defined by the following.

$$\begin{cases} d_a \vec{V}_{100} + d_b \vec{V}_{210}^{\text{vir}} + d_c \vec{V}_{200} = \vec{V}_{\text{ref}}, \\ d_a + d_b + d_c = 1, \end{cases} \tag{9}$$

where d_a, d_b, and d_c are the duty ratios for the vectors $\vec{V}_{100}$, $\vec{V}_{210}^{\text{vir}}$, and $\vec{V}_{200}$, respectively.

Substituting the values of the voltage vectors into (9) and separating the real and imaginary parts give

$$\begin{vmatrix} \frac{1}{3}V_{\text{dc}} & \frac{1}{2}V_{\text{dc}} & \frac{2}{3}V_{\text{dc}} \\ 0 & \frac{1}{2\sqrt{3}}V_{\text{dc}} & 0 \\ 1 & 1 & 1 \end{vmatrix} \begin{vmatrix} d_a \\ d_b \\ d_c \end{vmatrix} = \begin{vmatrix} V_r \cos(\theta_I) \\ V_r \sin(\theta_I) \\ 1 \end{vmatrix}. \tag{10}$$

Solving (10), the results are as follows:

$$\begin{vmatrix} d_a \\ d_b \\ d_c \end{vmatrix} = \begin{vmatrix} 2 - 2(d_1 + d_2) \\ 2d_2 \\ 2d_1 - 1 \end{vmatrix}, \tag{11}$$

where d_1 and d_2 are defined as in (7).

Calculating similarly for the remaining regions, the relationship between the $\vec{V}_{\text{ref}}$ location and duty factors is summarized in Table 3.

In regions 2, 3, and 4 of sectors I and IV, the reference voltage vector is synthesized with the participation of the virtual vector. For example, $\vec{V}_{\text{ref}}$ in region 3 of sector I is synthesized by 3 voltage vectors $\vec{V}_{100}$, $\vec{V}_{200}$, and $\vec{V}_{210}^{\text{vir}}$ with duty coefficients d_a, d_c, and d_b, respectively, in which $\vec{V}_{210}^{\text{vir}}$ is performed by $\vec{V}_{200}$ and $\vec{V}_{220}$, as defined in (6), with duty $d_b/2$ for each. The duty factors for available vectors $\vec{V}_{100}$, $\vec{V}_{220}$, and $\vec{V}_{200}$ are adjusted to d_a, $d_b/2$, and $((d_b/2) + d_c)$, rewritten as $2 - 2(d_1 + d_2)$, d_2, and $2d_1 + d_2 - 1$, respectively. All the adjusted duty coefficients of the voltage vectors of sectors I and IV are detailed in Table 4.

3.3. Switching Sequence. After calculating the duty for the selected voltage vectors to synthesize into the reference vector, the next step is to arrange the switching sequence. In this section, the switching sequence for $\vec{V}_{\text{ref}}$ is designed to minimize the switching frequency according to required criteria is as follows. ① The transition between switching states involves only two switches in the same phase leg. It is satisfied if there is no switching from state 0 to state 2 or vice versa in phase leg A and C. ② When the reference vector $\vec{V}_{\text{ref}}$ moves from one sector (or region) to the next, the transition requires no or a minimum number of switching. ③ The switching sequence is arranged in a half-wave symmetrical pattern to eliminate even-order harmonics on the output line voltages.

For example, $\vec{V}_{\text{ref}}$ is located in region 2 of sector I. A typical seven-segment switching sequence and output line-voltage waveforms are presented in Figure 6(a). It can be seen that

requirement ① is satisfied. The starting and ending point is state 100, so the switching sequence in the remaining regions of sector I must also start from state 100 or 200 to satisfy requirement ②. For the requirement ③ to be also satisfied, then region 2 of sector IV must be arranged in the opposite order of sector I, as shown in Figure 6(b).

The typical switching sequence for the asymmetric *T*-type NPC inverter is shown in Figure 7.

3.4. The Self-Balancing Mechanism. The relation between the DC-link capacitor voltages (V_{c1}, V_{c2}) and DC-link capacitor currents (i_{c1}, i_{c1}) is provided as follows [34–38]:

$$\begin{cases} V_{c1} = V_{c1}^{o} + \dfrac{1}{C}\displaystyle\int_{o}^{t} i_{c1}\mathrm{d}t, \\ \\ V_{c2} = V_{c2}^{o} + \dfrac{1}{C}\displaystyle\int_{o}^{t} i_{c2}\mathrm{d}t, \end{cases} \tag{12}$$

where V_{c1}^{o} and V_{c2}^{o} are the initial values of c_1 and c_2 capacitors and supposing their capacitance $C_1 = C_2 = \mathrm{C}$.

Kirchhoff's current law is applied at the neutral point as follows:

$$i_{\mathrm{NP}} = i_{c1} - i_{c2}. \tag{13}$$

Assuming $V_{c1}^{o} = V_{c2}^{o}$, the difference between V_{c1} and V_{c2} voltages per fundamental cycle is calculated as follows:

$$\Delta V_c = V_{c1} - V_{c2} = \frac{1}{C}\int_{o}^{2\pi} i_{\mathrm{NP}}\mathrm{d}t. \tag{14}$$

When a zero or large vector is applied, as shown in Figures 8(a)and 8(d), the difference voltage ΔV_c is not affected because of $i_{\mathrm{NP}} = 0$. In contrast, small and medium vectors can contribute to the variation of ΔV_c, as shown in Figures 8(b) and 8(c), in which the polarity and magnitude of ΔV_c are determined by the load current generated by the switching state.

For the selected switching sequence, as in Figure 7, the voltage difference ΔV_c generated by the switching states at the low modulation index $(m_a \le 0.5)$ in one fundamental period is presented in Figure 9. For example, when the reference vector moves in region 1 of sector I, the switching states 100, 221, and 222 are applied to synthesize the reference vector. The voltage difference caused by the switching states is calculated as follows:

$$\begin{aligned} \Delta V_{cI} &= \frac{1}{C}\left[\int_{0}^{t_a/2} i_A\mathrm{d}t + \int_{(t_a/2)}^{(t_a/2)+(t_c/2)} i_C\mathrm{d}t + \int_{(t_a/2)+(t_c/2)+t_b}^{(t_a/2)+t_c+t_b} i_C\mathrm{d}t + \int_{(t_a/2)+t_c+t_b}^{\pi/3} i_A\mathrm{d}t\right] \\ &= \Delta V_{cI}^{①} + \Delta V_{cI}^{②} + \Delta V_{cI}^{③} + \Delta V_{cI}^{④}. \end{aligned} \tag{15}$$

Similarly for region 1 of sector IV,

$$\begin{aligned} \Delta V_{cIV} &= \frac{1}{C}\left[\int_{\pi}^{\pi+(t_a/2)} i_A\mathrm{d}t + \int_{\pi+(t_a/2)}^{\pi+(t_a/2)+(t_c/2)} i_C\mathrm{d}t + \int_{\pi+(t_a/2)+(t_c/2)+t_b}^{\pi+(t_a/2)+t_c+t_b} i_C\mathrm{d}t + \int_{\pi+(t_a/2)+t_c+t_b}^{4\pi/3} i_A\mathrm{d}t\right] \\ &= \Delta V_{cIV}^{①} + \Delta V_{cIV}^{②} + \Delta V_{cIV}^{③} + \Delta V_{cIV}^{④}. \end{aligned} \tag{16}$$

The general equation of the load currents is as follows:

$$\begin{cases} i_A = I_{Am}\sin(\omega t + \varphi_A), \\ \\ i_B = I_{Bm}\sin\left(\omega t - \dfrac{2\pi}{3} + \varphi_B\right), \\ \\ i_C = I_{Cm}\sin\left(\omega t + \dfrac{2\pi}{3} + \varphi_C\right), \end{cases} \tag{17}$$

where I_{Xm} is the max amplitude of the phase load current and φ_X is the load power factor angle; $X \in \{A, B, C\}$.

Substitute (17) into (15) and (16), the definite integrals $\Delta V_{cI}^{①}$ and $\Delta V_{cIV}^{②}$ are calculated as follows:

$$\begin{cases} V_{cI}^{①} = \dfrac{I_{Am}}{\omega C}\left[\cos(\varphi_A) - \cos\left(\omega\dfrac{t_a}{2} + \varphi_A\right)\right], \\ \\ V_{cIV}^{①} = \dfrac{I_{Am}}{\omega C}\left[-\cos(\varphi_A) + \cos\left(\omega\dfrac{t_a}{2} + \varphi_A\right)\right]. \end{cases} \tag{18}$$

Expression (18) and Figure 9 show that when applying the switching state 100, it causes a capacitor imbalance, by the red area marked ① in sector I. Meanwhile, the switching state 122 in sector IV makes the capacitor unbalanced by an amount equal to that caused by switching state 100 but a different sign (area marker ① in sector IV). Similarly, with the remaining definite integrals, we have

$$\begin{array}{rccccc} & \Delta V_{cI} = \Delta V_{cI}^{①} + \Delta V_{cI}^{②} + \Delta V_{cI}^{③} + \Delta V_{cI}^{④} & & & & \\ + & \Delta V_{cIV} = \Delta V_{cIV}^{①} + \Delta V_{cIV}^{②} + \Delta V_{cIV}^{③} + \Delta V_{cIV}^{④} & & & & \\ \hline & 0 & 0 & 0 & 0 & 0 \end{array} \tag{19}$$

Table 2: Comparing typical properties of inverters.

Characteristic	2-level	Asymmetric 3-level	3-level
Structure	+ Symmetric + using 6 IGBTs	+ Asymmetric + using 10 IGBTs	+ Symmetric + using 12 IGBTs
Switching states	8	18	27
Different voltage vectors	7	17	19
Line-voltage levels	$\pm V_{dc}$; 0	$\pm V_{dc}$; $\pm$ (1/2)V_{dc}; 0	$\pm V_{dc}$; $\pm$ (1/2)V_{dc}; 0

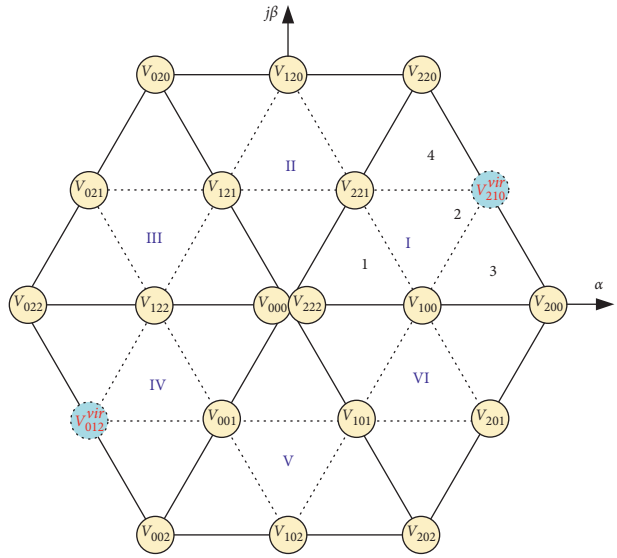

Figure 4: Virtual space vector diagram.

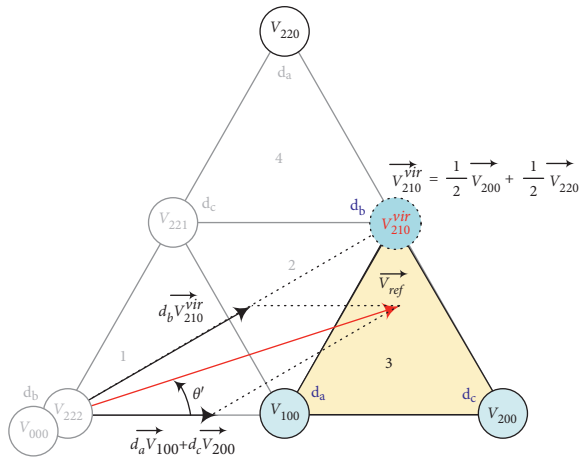

Figure 5: $\vec{V}_{ref}$ is located in region 3 of sector I.

Table 3: Duty ratio calculation in conventional 3-level NPC.

$\vec{V}_{ref}$ location	Duty ratio		
	d_a	d_b	d_c
1	$2d_1$	$1-2(d_1+d_2)$	$2d_2$
2	$1-2d_2$	$2(d_1+d_2)-1$	$1-2d_1$
3	$2-2(d_1+d_2)$	$2d_2$	$2d_1-1$
4	$2d_2-1$	$2d_1$	$2-2(d_1+d_2)$

Table 4: Adjusted duty ratio for voltage vectors in sectors I and IV.

Region	Voltage vector		Adjusted duty ratio
	Sector I	Sector IV	
2	$\vec{V}_{100}$	$\vec{V}_{122}$	$1-2d_2$
	$\vec{V}_{200}$	$\vec{V}_{022}$	$d_1+d_2-0.5$
	$\vec{V}_{220}$	$\vec{V}_{002}$	$d_1+d_2-0.5$
	$\vec{V}_{221}$	$\vec{V}_{001}$	$1-2d_1$
3	$\vec{V}_{100}$	$\vec{V}_{122}$	$2-2(d_1+d_2)$
	$\vec{V}_{200}$	$\vec{V}_{022}$	$2d_1+d_2-1$
	$\vec{V}_{220}$	$\vec{V}_{002}$	d_2
4	$\vec{V}_{200}$	$\vec{V}_{022}$	d_1
	$\vec{V}_{220}$	$\vec{V}_{002}$	d_1+2d_2-1
	$\vec{V}_{221}$	$\vec{V}_{001}$	$2-2(d_1+d_2)$

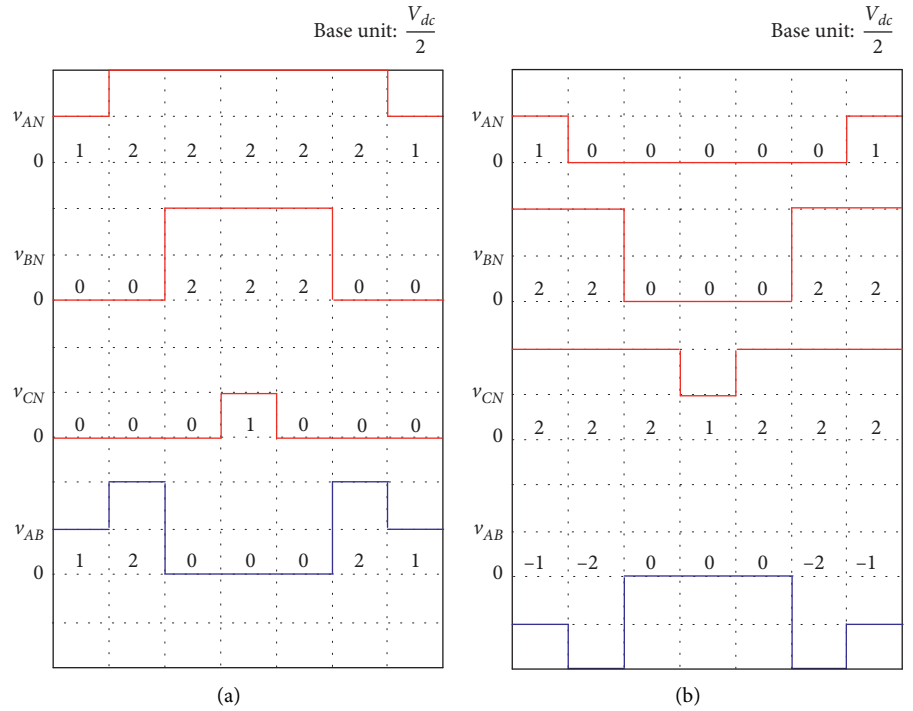

Figure 6: Switching sequence for region 2: (a) sector I; (b) sector IV.

In one fundamental cycle, the switching state in the first half causes an imbalance. However, it quickly returns to balance in the next half-cycle by switching states on the opposite side, which have the same neutral current characteristics but a different sign, so

$$\underbrace{\Delta V_{cI}+\Delta V_{cIV}}_{0}+\underbrace{\Delta V_{cII}+\Delta V_{cV}}_{0}+\underbrace{\Delta V_{cIII}+\Delta V_{cVI}}_{0}=0, \tag{20}$$

where ΔV_{ci} is the difference voltage caused by the switching states in sector i; $i \in \{\mathrm{I}, \mathrm{II}, \mathrm{III}, \mathrm{IV}, \mathrm{V}, \mathrm{VI}\}$.

The self-balancing mechanism for the high modulation index ($m_a > 0.5$) also occurs similarly, as presented in Figure 10.

3.5. Harmonic Distortion. The harmonic distortion performance of SVPWM strategies is evaluated by the THD of the load current and voltage output as follows [39]:

$$\begin{aligned}\mathrm{THD}_I &= \frac{1}{\mathrm{Im}}\sqrt{\sum_{n=2}^{\infty} I_n^2},\\ \mathrm{THD}_V &= \frac{1}{Vm}\sqrt{\sum_{n=2}^{\infty} V_n^2},\end{aligned} \tag{21}$$

where I_m and I_n are the fundamental magnitude and the n^{th} harmonic magnitude of phase current output, respectively.

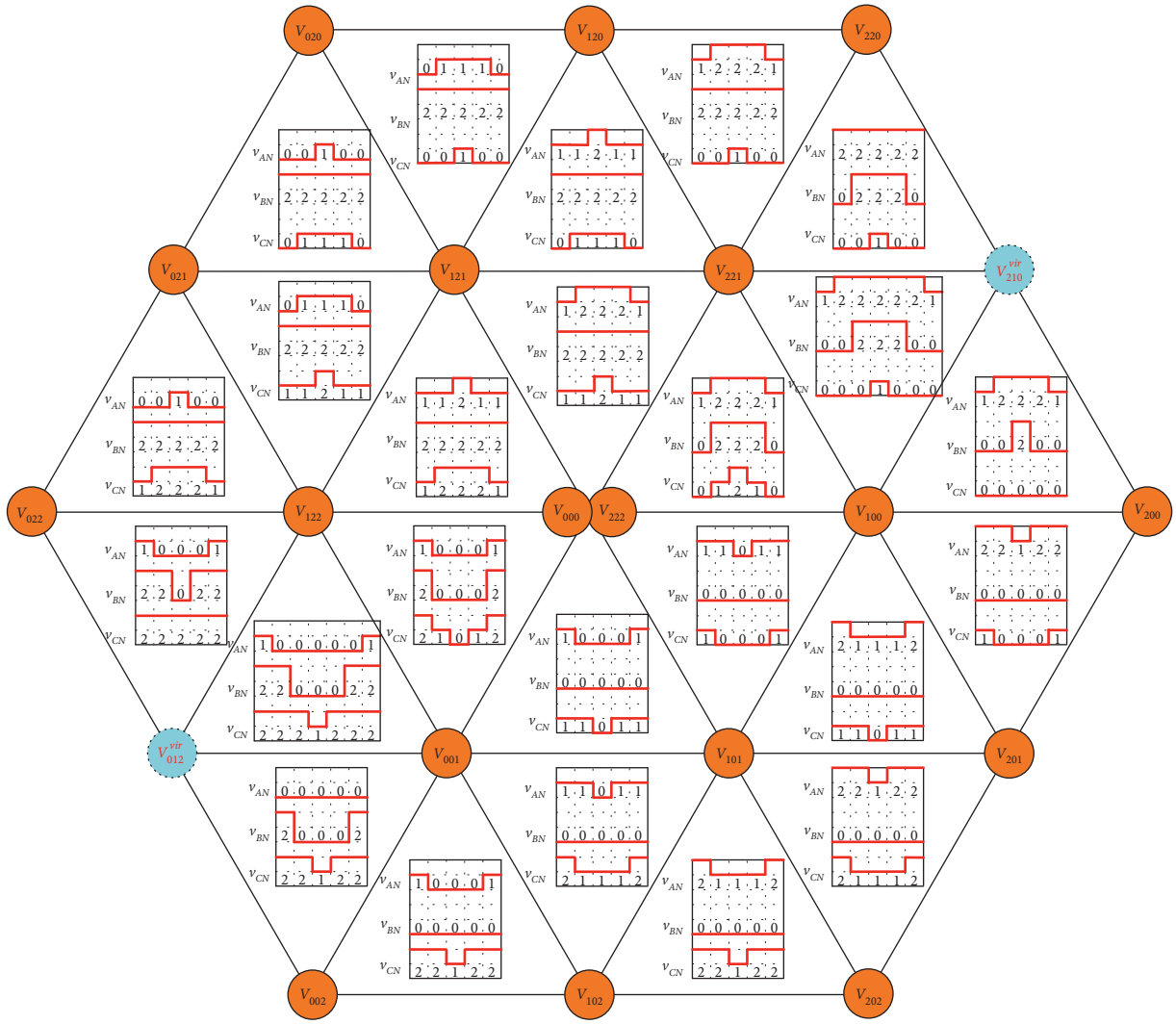

Figure 7: Switching sequence for asymmetric T-type NPC inverter.

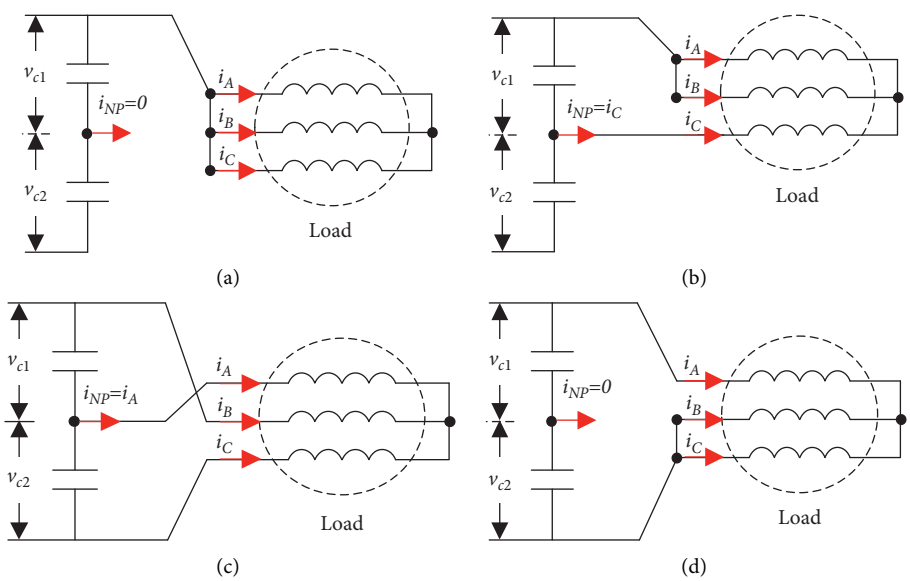

Figure 8: The effect of switching vectors on dc-link capacitors: (a) ZV; (b) SV; (c) MV; (d) LV.

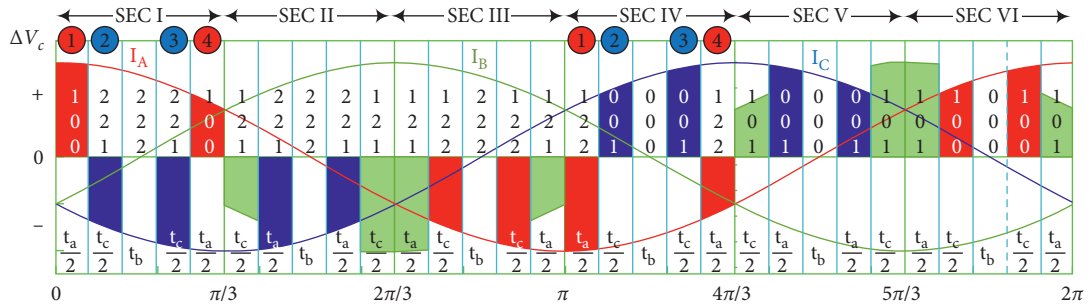

Figure 9: The difference voltage generated by the switching states at $m_a \leq 0.5$.

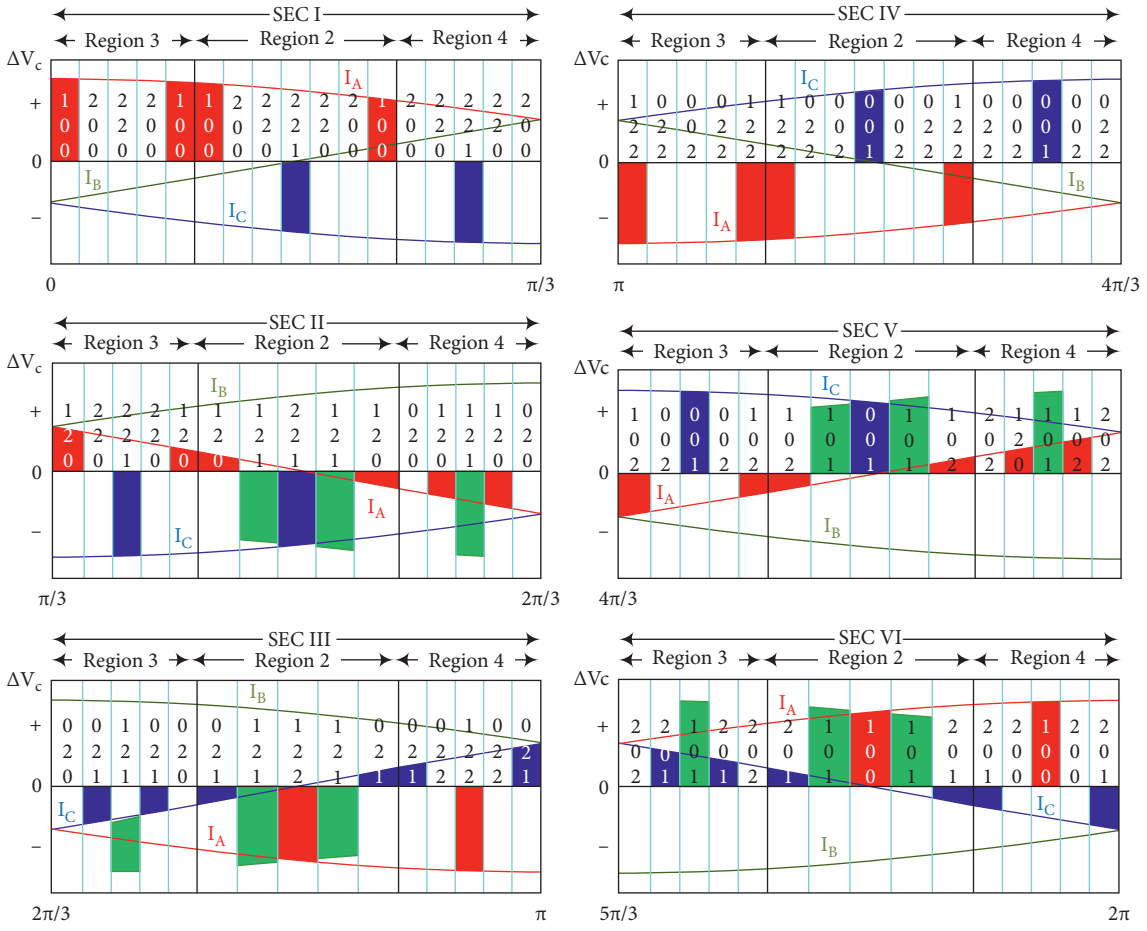

Figure 10: The difference voltage generated by the switching states at $m_a > 0.5$.

V_m and V_n are the fundamental magnitude and the n^{th} harmonic magnitude of line-voltage output, respectively. In this paper, the THD spectrum of load current and output voltage is calculated to the 1000^{th} harmonic.

4. Simulation and Experimental Results

4.1. Simulation Results. To validate the asymmetric 3-level *T*-type NPC inverter, simulations were performed using MATLAB/Simulink software version 2018a, as shown in Figure 11. The system parameters are shown in Table 5.

Figure 12 shows the steady-state of the VSVPWM method for the asymmetric 3-level inverter with $m_a = 0.9$. The load current and the balance of DC-link capacitor voltages are depicted in Figures 12(c) and 12(d). Let V_{32} be a line voltage between outputs of 3-level and 2-level legs and V_{33} be a line voltage between outputs of two 3-level legs. The waveforms of V_{32} and V_{33} are illustrated in Figures 12(a) and 12(b) with THD_V of about 44.4% and 32.8%, respectively.

In order to evaluate the dynamic response performance, a step change in modulation index from 0.4 to 0.8 is examined in this study. The diagram of the load current is shown in Figure 13(c). The voltage of the capacitors is

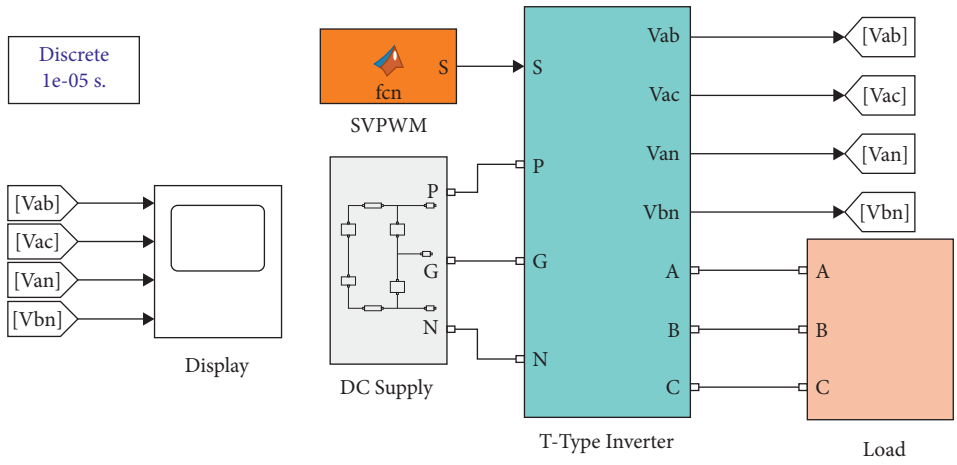

Figure 11: Simulation model in Matlab/Simulink.

Table 5: System parameters for simulation.

Description	Parameter	Value
DC voltage	V_{dc}	600 V
Load resistor	R	12 Ω
Load inductor	L	20 mH
DC-link capacitor	C_1, C_2	1200 μF
Switching frequency	f_{sw}	2.4 kHz
Frequency	f	50 Hz

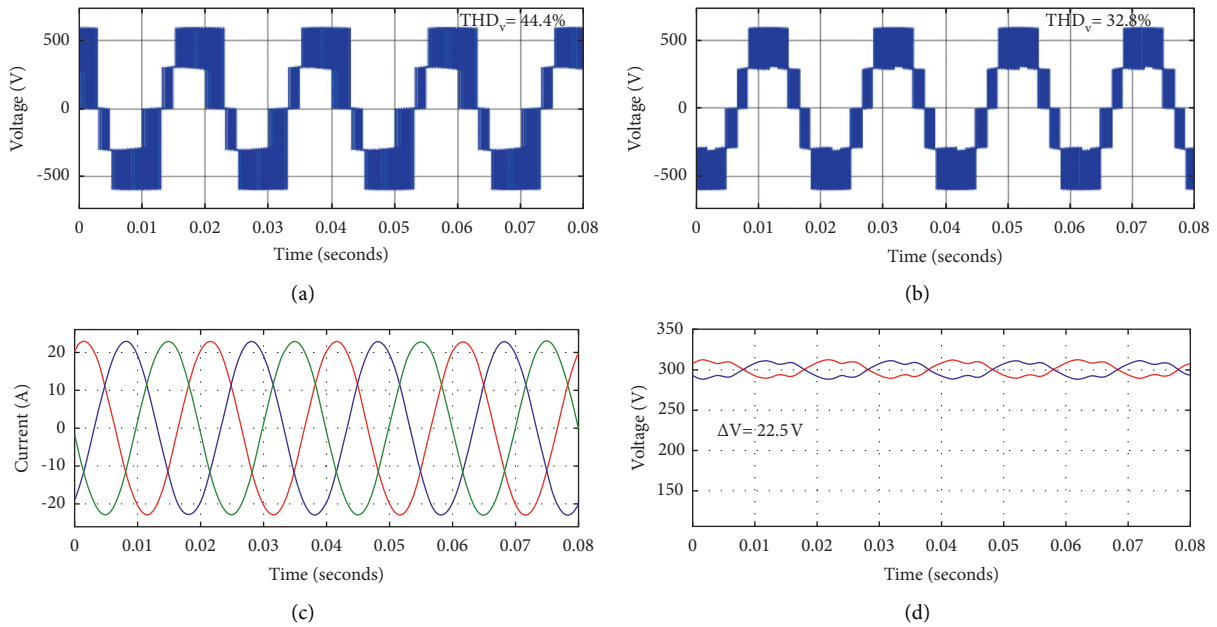

Figure 12: Steady-state response of VSVPWM for the asymmetric 3-level inverter at $m_a = 0.9$: (a) output voltage V_{32}; (b) output voltage V_{33}; (c) load current; (d) capacitor voltages.

maintained in balance with ΔV_c around 20 V and 32 V for the modulation index of 0.4 and 0.8, respectively, as shown in Figure 13(d). For $m_a = 0.4$, the line-voltage quality V_{32} and V_{33} are almost the same, with THD$_V$ about 76%; for $m_a = 0.8$, THD$_V$ of V_{33} is about 38% while that of V_{32} is 49.3%, as illustrated in Figures 13(a) and 13(b).

THD$_V$ of the asymmetric 3-level inverter for different modulation indices is described in Table 6. For $m_a \leq 0.5$,

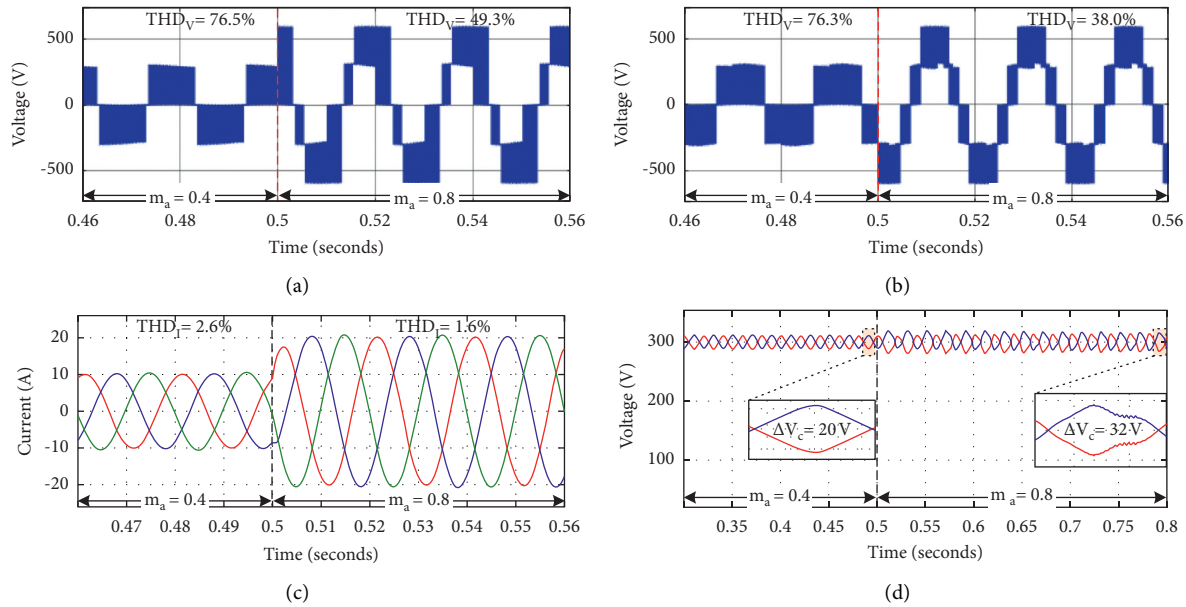

FIGURE 13: The dynamic response of the asymmetric 3-level inverter for step change m_a from 0.4 to 0.8: (a) output voltage V_{32}; (b) output voltage V_{33}; (c) load current; (d) capacitor voltages.

TABLE 6: THD_V for different modulation indices.

	Total harmonic distortion (%)									
m_a	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
V_{32}	230.7	145.8	104.9	76.5	52.4	50.9	52.4	49.3	44.4	39.0
V_{33}	229.2	147.3	105.8	76.3	52.1	44.5	41.3	38.0	32.8	26.5

THD_V on both V_{32} and V_{33} is almost the same. For $m_a > 0.5$, when the reference voltage vector appears in regions 2, 3, and 4, THD_V of V_{32} is higher than V_{33}. For example, at $m_a = 0.9$, THD_V of V_{32} and V_{33} is 44.4% and 32.8%, respectively.

The behavior of the system is also examined under a sudden change of the load at $m_a = 0.9$, as presented in Figure 14(a). In the initial state, the system operates with the load parameters $R = 12\,\Omega$ and $L = 20$ mH; then, another resistor $R' = 12\,\Omega$ is connected parallel with R at $t = 0.5$ s. This results in a load current change from 23 A to 36 A with THD_I about 1.32% to 0.98%, respectively, as shown in Figure 14(b). As depicted in Figure 14(c), the capacitor voltages are maintained to be well balanced with ΔV_c around 22 V and 37 V. The output voltage quality of the asymmetric T-type NPC inverter is not influenced by the load parameters with THD_V maintained about 44% and 32% for V_{32} and V_{33}, as shown in Figure 14(d).

To evaluate the influence of the load power factor on ΔV_c, simulation is examined with a fixed load impedance $Z = 13.55\,\Omega$ and a variable power factor between 0.4 and 0.95 for the different modulation indexes. The results in Figure 15 show that the neutral point voltage maintains a relatively good balance at different load power factors and modulation indices. The region with $m_a \le 0.4$ gives a small capacitor voltage difference in the range $\Delta V_c \le 4\%$, i.e., $\Delta V_{c\,\max}$ is about 24 V, with all load power factors. For $0.4 < m_a \le 0.8$, the capacitor voltage difference gradually increases with the modulation index and load power factor and ΔV_c ranges from 3%–7% and reaches the maximum value of about 43 V at (m_a; cos φ) = (0.6; 0.95). In the remaining region with $m_a > 0.8$, ΔV_c tends to decrease in the range of 3%–5% when the power factor increases. For example, at $m_a = 1$, $\Delta V_c = 30$ V for power factor 0.55 and $\Delta V_c = 16$ V for power factor 0.95.

A test with unbalanced load parameters depicted in Figure 16(a) is also performed in this study. Figures 16(b) and 16(c) show that even though the 3-phase load currents are unbalanced, the capacitor voltages are maintained balanced with ΔV_c about 28 V.

To verify the behavior of the self-balancing mechanism of neutral point voltage, the simulation is performed at $m_a = 0.9$, and capacitor c_2 is discharged during $t = 0.5$ – 0.56 s by connected a resistor connected in parallel, as shown in Figure 17(a). The difference of capacitor voltages at $t = 0.56$ s is about 300 V. Under the proposed VSVPWM, it rapidly decreases and attains a steady-state value at 24 V after 0.3 s, as shown in Figure 17(b).

The graph in Figure 18 compares voltage THD characteristics of the asymmetric T-type NPC, 3-level, and 2-level inverter. As observed, for $m_a \le 0.5$, the THD characteristic of the asymmetric T-type NPC topology is similar to that of the conventional 3-level. For $m_a > 0.5$, the THDV characteristic of the voltage V_{32} is higher than that of 3-level inverter, while the THDV characteristic of the voltage V_{33} is similar to that of 3-level inverter. THD_V of the asymmetric

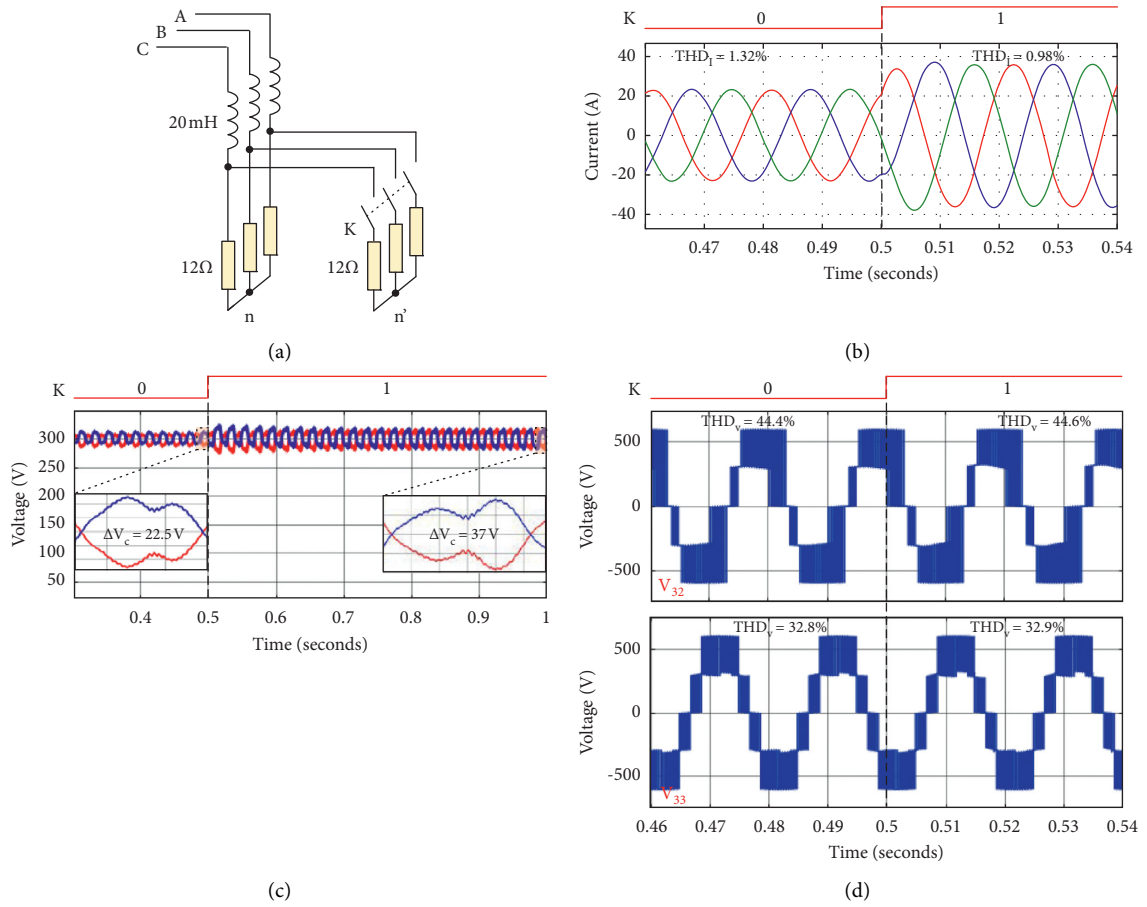

Figure 14: System response at the module index $m_a = 0.9$ under variable load parameters: (a) change load parameters; (b) load current; (c) capacitor voltages; (d) output voltages.

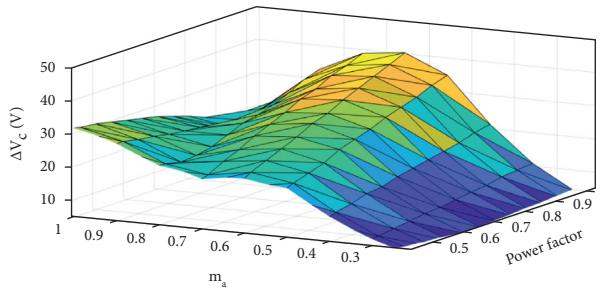

Figure 15: Plot of voltage difference for various load power factors and modulation indices.

T-type NPC inverter is significantly better than that of the 2-level inverter for all modulation indices.

Another benefit of the asymmetric inverter can be demonstrated in loss comparison. The total loss is calculated as the sum of conduction loss and switching losses of all IGBTs and diodes, whose device datasheets are given in Table 7. The principle of power loss calculation is explained in detail in [40]. The calculation is realized with the use of SimPowerSystems and Simscape in Matlab, with parameters $V_{dc} = 300$ V, $m_a = 0.9$, and load $R = 1.5\,\Omega$, $L = 3$ mH.

The comparison chart of conduction loss, switching loss, and total loss between the asymmetrical 3-level inverter and the conventional 3-level inverter is shown in Figures 19–21, respectively. The conduction loss is almost unchanged at various switching frequencies, about 284 W for the conventional 3-level inverter and 277 W for the asymmetric 3-level inverter, as shown in Figure 19.

The switching loss of the asymmetric 3-level inverter is shown to be smaller than that of the conventional 3-level inverter, as shown in Figure 20. At $f_{sw} = 15$ kHz, the switching loss of the asymmetric inverter is 73.1 W

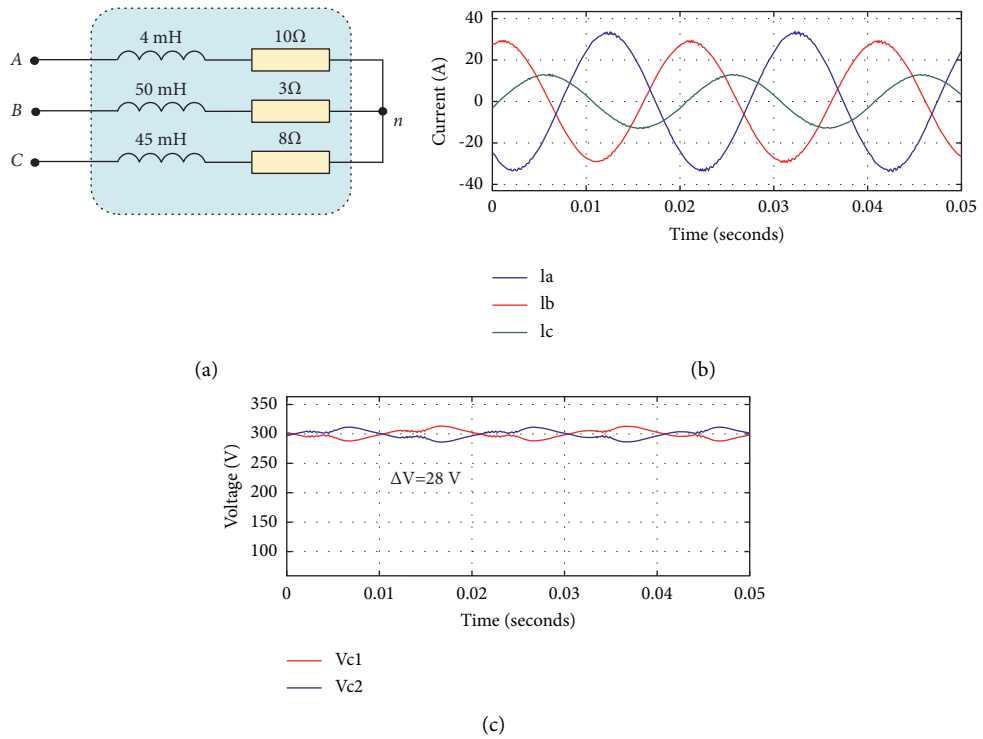

Figure 16: The responses of VSVPWM for asymmetric 3-level inverter under unbalanced load at $m_a = 0.9$: (a) the unbalanced load; (b) load current; (c) capacitor voltages.

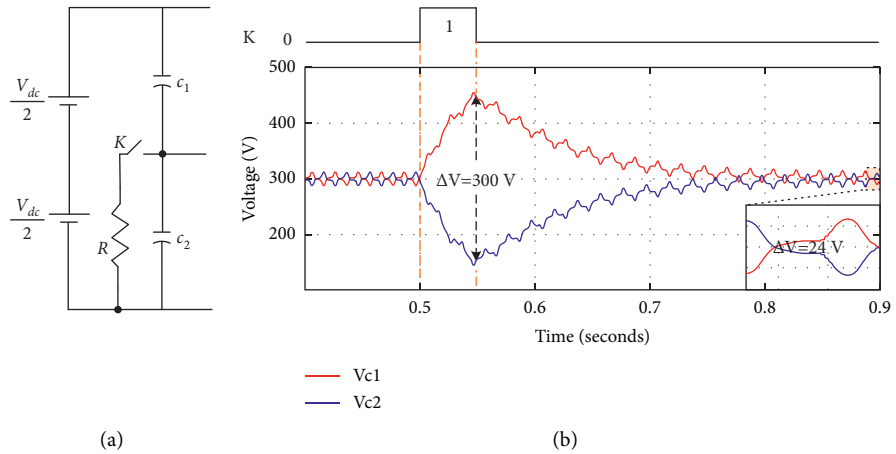

Figure 17: The self-balancing mechanism of VSVPWM for the asymmetric 3-level inverter after setting a large imbalance: (a) forced imbalance with $v_{c1} > v_{c2}$; (b) capacitor voltages.

compared with the 104.4 W of the conventional 3-level inverter. It gives a reduction of about 30% switching loss. Similar results are also obtained for other switching frequencies.

As demonstrated in Figure 21, the total loss of the asymmetric inverter is lower than that of a conventional 3-level inverter. For example, at f_{sw} = 10 kHz, the total losses of the asymmetric 3-level inverter and conventional 3-level inverter are 326.1 W and 353.8 W, respectively. Likewise, at f_{sw} = 20 kHz, the total loss is 374.4 W for the asymmetric inverter and 424.2 W for the conventional 3-level inverter. This translates to a more than 12% improvement in power loss.

4.2. Experimental Results. To verify the effectiveness of the presented topology, the experiments were carried out on an asymmetric *T*-type NPC, 2-level, and 3-level configuration under both transient and steady-state conditions. A laboratory model is built as shown in Figure 22, including ① a digital signal processor TMS320F28379D to perform algorithms built-in Matlab/Simulink environment with

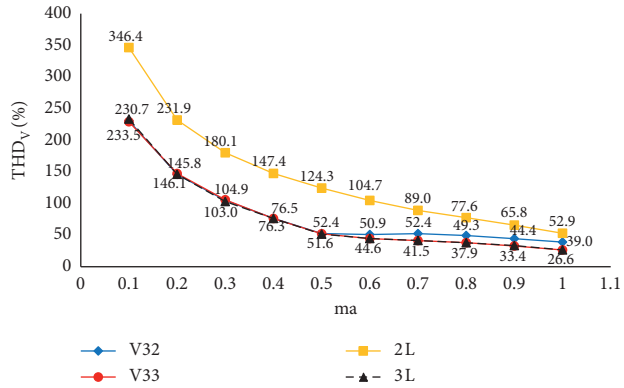

Figure 18: Graph of THD_V comparison of asymmetric 3-level, conventional 3-level, and 2-level inverter.

Table 7: Power device parameters.

IGBT module 2MBI150U2A-060				
Item		Symbol	Rating	Unit
Collector-emitter voltage		V_{CES}	600	V
Gate-emitter voltage		V_{GES}	±20	V
Collector current		I_C	150	A
		I_{CP}	300	
Collector power dissipation		P_C	500	W
Turn-on time		t_{on}	0.40	μs
Turn-off time		t_{off}	0.48	
Thermal resistance	IGBT	$R_{th(j\text{-}c)}$	0.25	°C/W
	FWD	$R_{th(j\text{-}c)}$	0.46	
Contact thermal resistance		$R_{th(c\text{-}f)}$	0.05	

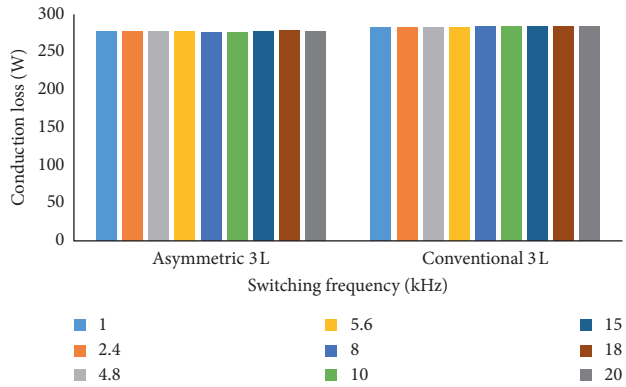

Figure 19: Graph of conduction loss comparison for different switching frequencies.

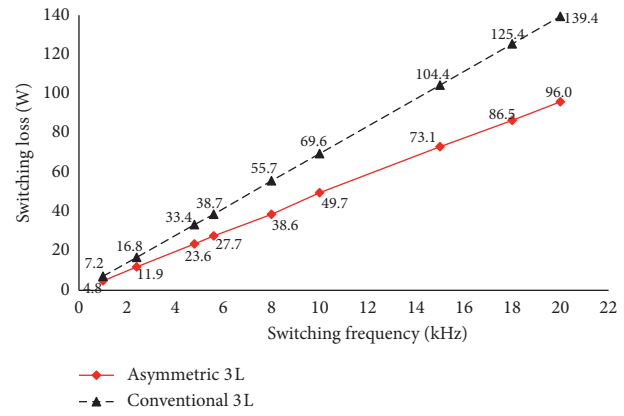

Figure 20: Graph of switching loss comparison for different switching frequencies.

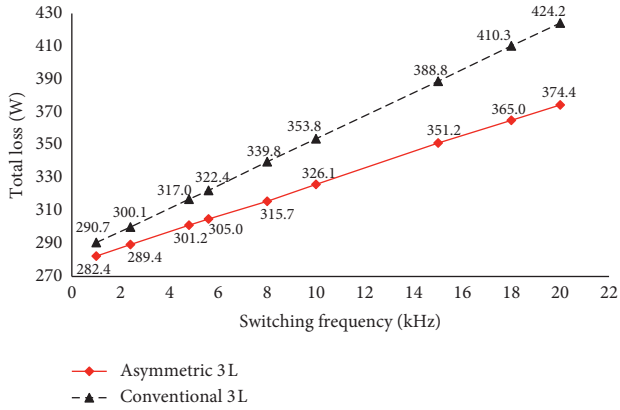

Figure 21: Graph of total loss comparison for different switching frequencies.

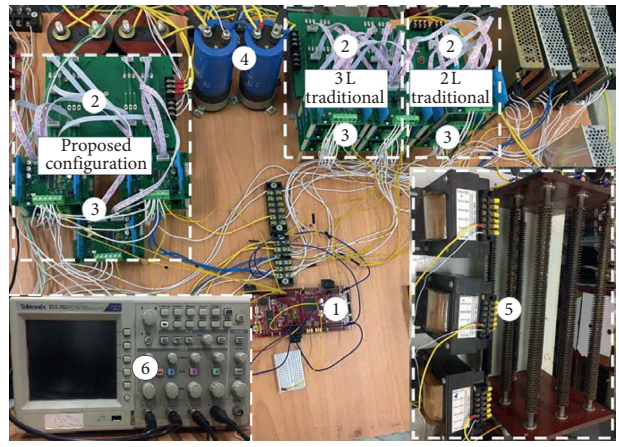

Figure 22: Experimental model in the laboratory.

Embedded Coder Support Package for TI C2000 Processors; ② the inverter made from TOSHIBA's IGBT GT50J325-type; ③ IGBT driver circuit which uses QP12W08S-37 type; ④ DC-link capacitors; ⑤ R-L load; and ⑥ Tektronix TDS2024C oscilloscope. The experimental parameters are listed in Table 8.

The first test is performed with the modulation index stepped from 0.4 to 0.9. The results illustrated in Figure 23 show that the DC-link capacitor voltages are maintained balanced at both modulation indices. The output voltage qualities V_{32} and V_{33} are similar at modulation index m_a = 0.4, THD_V about 76%. For modulation index m_a = 0.9, the voltages V_{32} and V_{33} are distinguished with THD_V about 45.32% and 33.85%.

The second experiment is performed to evaluate the system's response under a step change in load parameters at m_a = 0.9. Initially, load 1 is with parameters R_1 = 35 Ω and L_1 = 45 mH; then, another resistor R_2 = 25 Ω is connected parallel with R_1, as shown in Figure 24(a). The results from Figure 24(b) show that the capacitor voltage is kept balanced for both load parameters. The load current changes from 2.7 A to 5.1 A. The quality of the output voltage is unchanged, THD_V about 45% and 33% for V_{32} and V_{33}.

The test with an unbalanced load is also performed with the load parameters as in Figure 25 at m_a = 0.9. The results shown in Figure 26 show that the capacitor voltages are kept balanced, and the output line-voltage qualities are similar to the above-balanced load test case, THD_V about 45% and 33% for V_{32} and V_{33}.

The experiment results of the self-balancing mechanism using VSVPWM strategy for asymmetric 3-level inverter under the unbalanced capacitor voltage condition at m_a = 0.9 are presented in Figure 27. In the initial state in Figure 27(a), switch K is closed, resulting in capacitor c_2 discharging and ΔV_c attains about 25 V. Then, K is opened, and ΔV_c rapidly decreases and obtains balancing, as shown in Figure 27(b).

Figure 28 shows the graph of the THD_V comparison of the VSVPWM algorithm for the asymmetric 3-level inverter and the SVPWM technique for conventional 2-level and 3-level inverters. The diagram shows that the experimental results are similar to the simulation results obtained in Figure 18.

Table 8: Experimental parameters.

Description	Parameter	Value
DC voltage	V_{dc}	200 V
Load resistor	R	14.5 Ω
Load inductor	L	45 mH
DC-link capacitor	C_1, C_2	1200 μF
Switching frequency	f_{sw}	2.4 kHz
Frequency	f	50 Hz

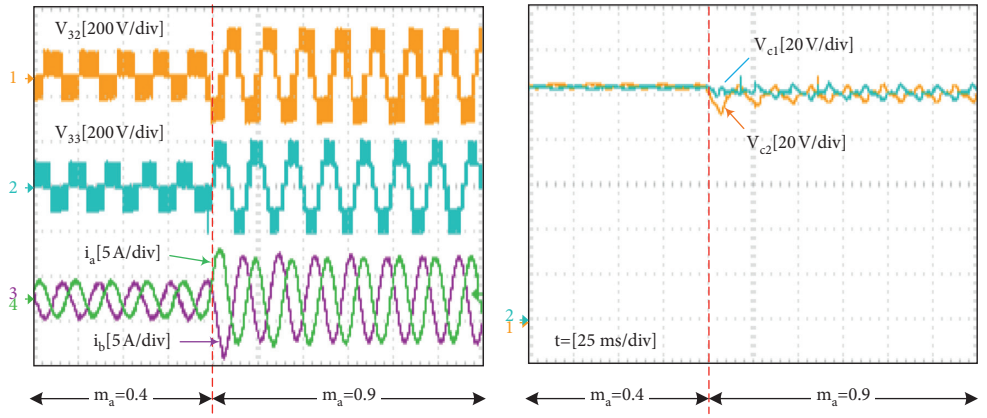

Figure 23: System response under step change in the modulation index.

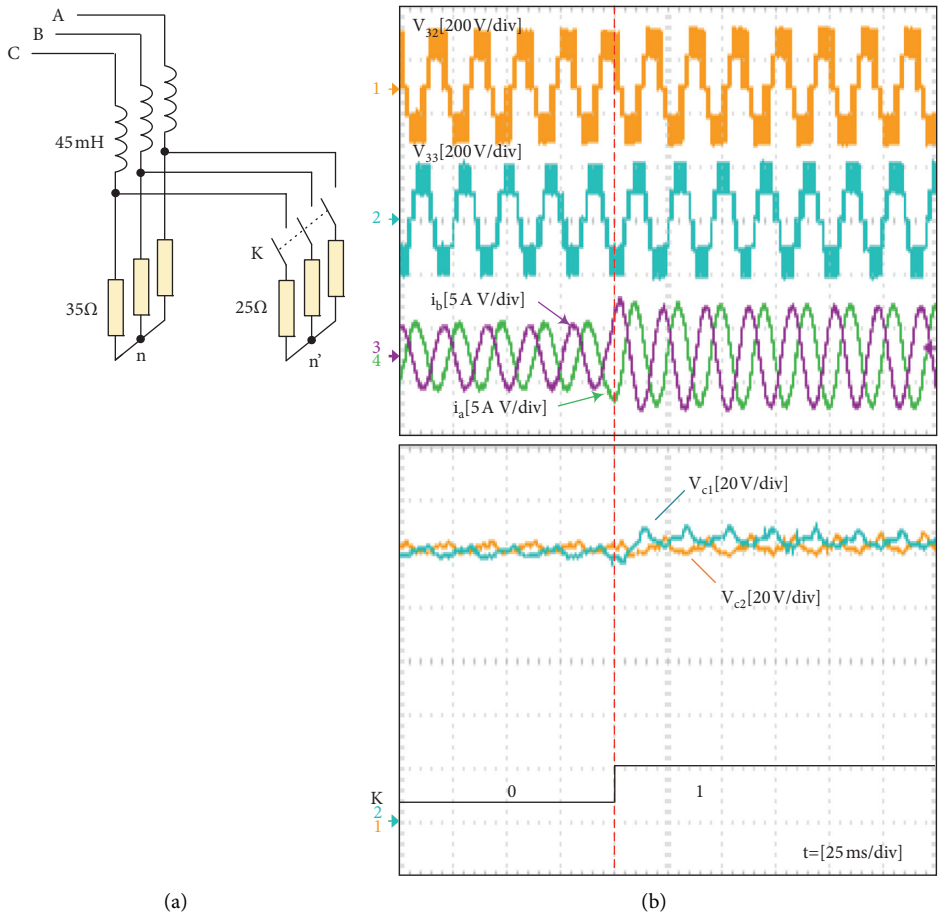

Figure 24: System response under step change in load parameters: (a) change load parameters; (b) system response.

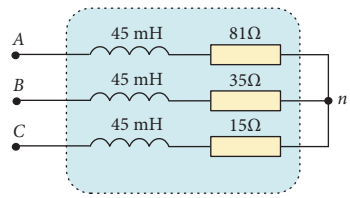

Figure 25: Unbalanced load parameters used in experiment.

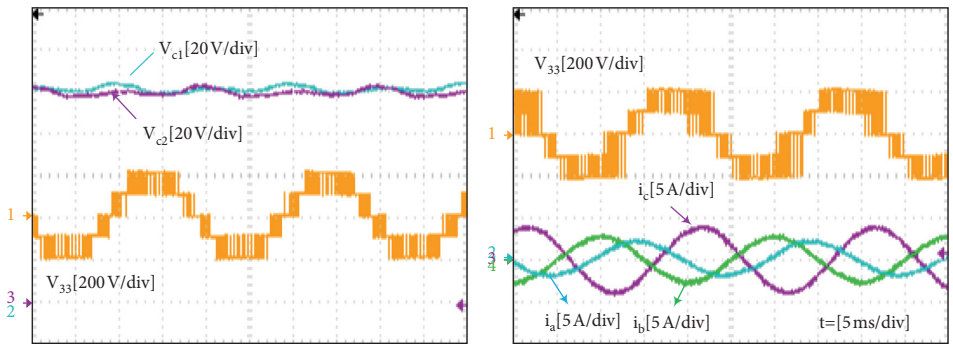

Figure 26: System response under unbalanced load conditions.

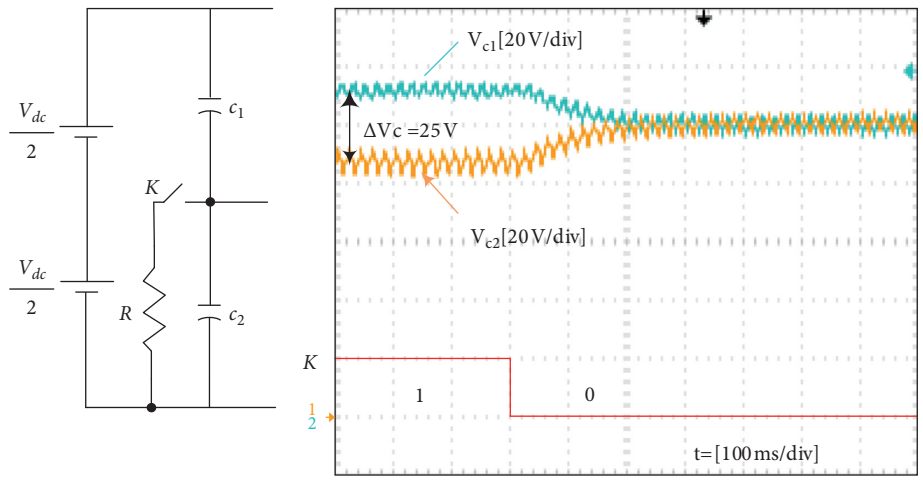

Figure 27: The self-balancing mechanism of VSVPWM for asymmetric 3-level inverter under unbalanced capacitor condition: (a) forced imbalance with $v_{c1} > v_{c2}$; (b) capacitor voltages.

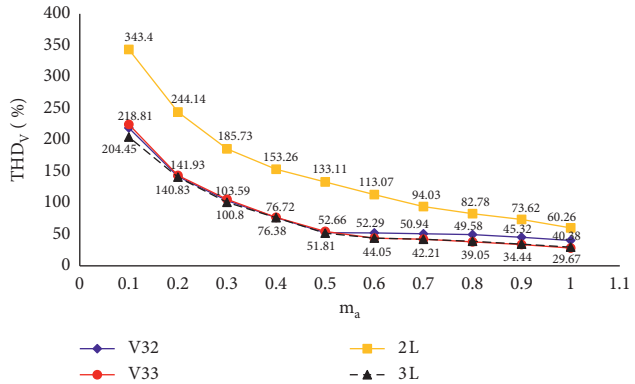

Figure 28: Experimental results of THD_V comparison between asymmetric 3-level, conventional 3-level, and 2-level inverter.

5. Conclusions

This paper presents virtual SVPWM control for the asymmetric *T*-type NPC 3-level inverter topology. A modified space vector diagram is built with the help of the virtual vector. Then, the conventional SVPWM algorithm of the three nearest vectors is implemented. The switching sequence has been designed to reduce the amount of switching. A comparative evaluation between asymmetric *T*-type, 2-level, and 3-level inverters was performed. Simulation and experiment results show that the output voltage quality of the asymmetric *T*-type NPC inverter is much improved compared with that of the conventional 2-level inverter and almost similar to that of the conventional 3-level inverter. Besides, the capacitor voltages are also maintained in a good balance. The asymmetric inverter is attractive for applications that require lower cost but own similar output performances of a three-level inverter such as full output voltage range and low harmonic distortion. In another application, the proposed VSVPWM control can be applied for a conventional 3-level *T*-type NPC in a faulty condition while one T-leg connected to the neutral point is defectively open.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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