Research Article

Design and Optimization of 2.1 mW ULP Doherty Power Amplifier with Interstage Capacitances Using 65 nm CMOS Technology

Muhammad Ovais Akhter and Najam Muhammad Amin

Department of Electrical Engineering, Bahria University, Karachi Campus, Karachi, Pakistan

Correspondence should be addressed to Muhammad Ovais Akhter; ovaisakhter1@gmail.com

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This research proposed the design and calculations of ultra-low power (ULP) Doherty power amplifier (PA) using 65 nm CMOS technology. Both the main and the peaking amplifiers are designed and optimized using equivalent lumped parameters and power combiner models. The operation has been performed in RF-nMOS subthreshold or triode region to achieve ultra-low power (ULP) and to improve the linearity of the overall power amplifier (PA). The novel design consumes a DC power of 2.1 mW, power-added efficiency (PAE) of 29.8%, operating at 2.4 GHz band, and output referred 1 dB compression point at 4.1 dBm. The simulation results show a very good capability of drive current, high gain, and very low input and output insertion losses.

1. Introduction

We are living in a modern world where everyone has lesser time to recharge their handy devices along with usage of a larger number of applications including healthcare, smart offices, and homes [1]. Demand for long-lasting battery life is one of the major requirements these days. When we talk about transmitter components, the power amplifier is considered as the power-hungry block [2] and is the most challenging building block in RF transceiver chip [3]. While designing a power amplifier, efficiency and linearity become a trade-off with each other [4]. Achieving both at the same time along with a low power becomes a challenge. This research simulates the idea of designing an ultra-low power (ULP) power amplifier with 65 nm CMOS technology. The calculations have been shown in a very simple manner, making it easier to understand for a designer. Numerous methods are available in past research studies where equivalent lumped parameters have been designed using bipolar devices, but CMOS designs are still preferred as these are relatively cheap as compared to bipolar transistors [5–7].

The Doherty power amplifier consists of two amplifiers: the carrier or main amplifier and the peaking amplifier [8]. These are usually prematched by a free scale. The two amplifiers operate at 90° out of phase. This is achieved by 90-degree output splitter such as a hybrid splitter or Wilkinson power divider [9]. Of course, the two signals have to be combined again after they are amplified. This is done by use of 90-degree transmission line at output of main amplifier [10]. The main amplifier is biased in class B (theoretically), but in practice we choose class AB to bias. The peaking amplifier is biased in class C [11]. When the signal level of the Doherty amplifier is slow (backoff mode), the peaking amplifier is off and only the main amplifier is operating, which means that the biasing point of class C is further slightly lower than the pinch-off point. This is the secret sauce to improve the efficiency of the Doherty amplifier. Another important component of the Doherty amplifier is the Doherty combiner or the power combiner circuit [12], which is implemented by another 90-degree transmission line which usually has a characteristic impedance of 50 ohms divided by a square root of 2. The function of the Doherty combiner is to transfer the impedance of 50 ohms load

impedance to 25 ohms impedance at the Doherty combining node, which then connects the Doherty node to the main amplifier, which has an impedance of 100 ohms. The impedance level stays constant as long as the amplifier stays off. Another important thing is that the peaking amplifier represents a very high impedance to its combining nodes. If you consider that the signal level increases at the input of the main amplifier, the peaking amplifier starts to produce power, but on the other hand, it also increases the impedance at the output of the main amplifier, which is known as effect of load modulation [13].

2. Proposed Doherty Power Amplifier Model Using 65 nm TSMCTM CMOS Technology

The four sections of the power amplifier are separated with red dotted lines in Figure 1. These include the power divider circuit, the main amplifier, the peaking amplifier, and power combiner circuit.

2.1. Wilkinson Power Divider Equivalent Model. Since a single band with power divider has been used, a perfect impedance matching is required. Both the main amplifier and the peaking amplifier are supposed to load Z_o . Various designs have been proposed earlier where both equal and unequal power divider techniques were used to calculate the input impedance of transmission lines. Both symmetric and asymmetric lumped element power divider techniques were observed in [14–16]. Since the equal power divider model has been implemented for both main and peaking amplifiers. If we match the ports of Wilkinson power divider, it becomes a lossless model [17]. Using the same approach, an equivalent circuit is designed using this technology. The 90-degree phase shift at one of the ports is accomplished by p-network. Previously, this work was done on BiCMOS technology [18]. Power divider in Figure 1 shows an equivalent lumped circuit as a p-network to achieve 90-degree phase.

Setting $Z_o = 50 \Omega$ for perfect matching, the distributed realization can be seen with parameters C , L , and R and a tuned frequency of 2.4 GHz as $R = 2Z_o = 100 \Omega$, $L = 50(\sqrt{2})/2\pi(2.4 \text{ GHz}) = 4.689 \text{ nH}$, and $C = 1/2\pi[50(\sqrt{2})](2.4 \text{ GHz}) = 937.8 \text{ fF}$.

Figure 2 shows a very low $S_{11} = -87.8 \text{ dB}$, $S_{22} = S_{33} = -96.1 \text{ dB}$ shows an almost perfect match, and $S_{12} = -3.01 \text{ dB}$ is an equal split of power divider. In addition, the following is valid for the insertion loss of nearly to ideal value of -3 dB .

$$\text{Insertion loss} = 10 \log_{10} \left(\frac{\text{input power}}{\text{output power}} \right) = 10 \log_{10} \left(\frac{1}{2} \right). \quad (1)$$

For our case, where we need to perfectly match at 50Ω , the transmission line is $\lambda/4 = \sqrt{2}Z_o = \sqrt{2}(100) = 70.71 \Omega$. Since this is a narrow band circuit, it avoided more cascading with factor <1 as seen in the traditional method [14]. The impedance of two ports can be calculated by first applying the transmission line theory (theoretical analysis), but using equal power division. As the admittance of transmission

lines is equal, the overall admittance of Z_1 and Z_2 can be rewritten as Y_1 and Y_2 , respectively [15]. It gives

$$Y_1 = Y_2 = Y_A \cot \theta \frac{Y_0 + Y_A \tan \theta}{Y_A \cot \theta + jY_0}. \quad (2)$$

To match the input, the condition will be $Y_0 = Y_2 + Y_3$. Under the condition of both input matching, the new condition becomes $Y_1 + Y_2 = Y_0$. Remember Z_0 as 50Ω , which is the port characteristic impedance for the calculation of input impedance. Reflection coefficient is maximum at 2.4 GHz center frequency. By using the value of S_{11} in Figure 3 and $\theta = \pi/2$, we can find the value of Γ [19], as $S_{11} = 20 \log \Gamma$ or $Z_{in} = Z_0(1 + \Gamma/1 - \Gamma)$.

As an alternative and to make it precise, we will observe the impedances on the Smith chart. With an operational frequency of 2.4 GHz, a frequency span of 0 MHz, and a characteristic impedance of 50Ω , the measured results can be observed in Figure 3 which are perfectly matched.

Due to symmetry, $S_{11} = S_{22}$, $S_{21} = S_{12}$, and $S_{13} = S_{31}$. Figure 4 shows the parameters achieved using the tuned scale, which are perfectly matched.

3. The Proposed Main and Peaking Power Amplifier Models with Interstage Capacitance

3.1. Input and Output Impedance Matching and Small Signal Model. Looking through the source path for the input impedance of the main power amplifier in Figure 4,

$$Z_{in1} = \left(\left(\frac{2}{g_{m1}} \right) \parallel Z_{C8} \right) + Z_{C6} + (Z_{L3} \parallel Z_{C5}) + Z_{C4}. \quad (3)$$

Similarly, for the peaking amplifier,

$$Z_{in2} = \left(\left(\frac{1}{g_{m2}} \right) \parallel Z_{C15} \right) + Z_{C13} + (Z_{L5} \parallel Z_{C12}) + Z_{C11}. \quad (4)$$

Looking through the output of the main amplifier, the overall output impedance can be calculated as

$$Z_{Out2} = Z_{C10} \parallel (Z_{L4} \parallel (r_{O1} \parallel Z_{C9} \parallel \left(\frac{1}{g_{m1}} \parallel Z_{C7} \right))). \quad (5)$$

Similarly, for the peaking amplifier,

$$Z_{Out2} = Z_{C19} \parallel ((Z_{C18} + Z_{L7} + Z_{C17}) \parallel (Z_{L6} \parallel r_{O2} \parallel Z_{C16} \parallel \left(\frac{1}{g_{m2}} \parallel Z_{C14} \right))), \quad (6)$$

where Z_{in1} and Z_{in2} are the input impedances of the main amplifier and peaking amplifier, respectively, observed from their source to the power divider circuit. Z_{out1} and Z_{out2} are the output impedances of main amplifier and peaking amplifier, respectively, observed from the divider end to their drain. The impedances towards PA are measured to 50Ω for perfect matching.

$C4$ and $C11$ are placed in interstage capacitors between the divider of the main amplifier and peaking amplifier circuits to improve the PAE [20]. The before and after

FIGURE 1: Schematic of the Doherty power amplifier using 65 nm CMOS technology.

FIGURE 2: Input return loss (S11), insertion loss (S12), and output return loss (S22) for power divider circuit.

interstage capacitor effect can be seen in Figure 5. Similarly, $L3||C5$ and $L5||L12$ are placed to match and tune the fundamental frequency of 2.4 GHz. $C6$ and $C13$ block the DC bias ($+V_{b1}$ and $+V_{b2}$). $M1$ and $M2$ are operating in sub-threshold region with gate-to-source voltage of 280 mV and 290 mV, respectively. $C7$, $C8$, $C9$, $C14$, $C15$, and $C16$ are placed to accommodate the unwanted parasitic capacitances.

The impedance parameter values and very small variation in source impedance vary the result from the theoretical values. The design has fixed interstage capacitances unlike [21], where variable interstage capacitance has been observed due to broadband. Fixed interstage capacitances with perfect matching shows novel research contribution along with optimization.

FIGURE 3: (a) Impedance matching through the Smith chart for power combiner lumped parameters and (b) power divider lumped parameters. (c) Wilkinson power divider and (d) power combiner using equivalent RLC model.

3.2. Subthreshold Operation in Triode Region. Figure 6 shows the input operation for V_{GS} operating at much lower pinch-off point. The output observed at the drain of the main amplifier M1 varies as the input varies from -20 dBm to -7 dBm. The input is applied at the gate of the main amplifier and the output is sensed at its drain. The g_m/I_d technique is used to relate the normalized drain current to the transconductance drain current, and the results are further optimized to achieve the power gain.

4. Simulation Findings Using 65 nm CMOS Technology

A few of the simulation findings have already been shown in the figures in previous sections. For standard $V_{DD} = 1.2$ V and defined $V_{TH} = 450$ m and M1 operating as main amplifier at subthreshold value of $V_{GS1} = V_{b1} = 280$ mV, the

simulation findings observed are as follows: $I_{d1} = 547.5$ μ A, $g_{m1} = 10.78$ m, $g_{m1}/I_{d1} = 19.74$, and $P_{DC1} = 985.1$ μ W. For M2 operating as the peaking amplifier at subthreshold value of $V_{GS2} = V_{b2} = 290$ mV, the simulation findings observed are as follows: $I_{d2} = 663.5$ μ A, $g_{m2} = 12.64$ m, $g_{m2}/I_{d2} = 19.1$, and $P_{DC2} = 1.194$ mW (see Figure 6 for subthreshold operations).

4.1. Scheme for Linearization. V_{b1} and V_{b2} (gate-to-source voltages) are set to the levels observed in Figures 6(a) and 6(b) to reduce the strong nonlinear behavior. The Taylor expansion [22] expresses the maximum linearity in the circuit design to optimize the proper bias voltage for both amplifiers. If I_{ds1} and I_{ds2} represent the nonlinear drain-to-source currents in the main and power amplifier, respectively, the expansion is as follows:

FIGURE 4: Small signal model for (a) main power amplifier and (b) peaking power amplifier operating in subthreshold region.

FIGURE 5: (a) The transient state before the interstage capacitor and (b) the transient state after the interstage capacitor of the main amplifier. (c) The result before the interstage state of the peaking amplifier and (d) its effect after the interstage capacitor as input power reaches -7 dBm.

FIGURE 6: (a) Subthreshold operation of the main amplifier and (b) the peaking amplifier with distinctive g_m values, operating much lower than the pinch-off point. (c) The transient output voltage (red dotted line) and the transient output current (brown dotted line) at -20 dBm input voltage. (d) The same simulation results as seen in (c) for -7 dBm inputs.

$$I_{ds1} = g_{m-1} \cdot V_{b1} + \frac{g_{m-1}}{2!} V_{b1}^2 + \frac{g_{m-3}}{3!} V_{b1}^3 + \dots, \quad (7)$$

$$I_{ds2} = g_{m-1} \cdot V_{b2} + \frac{g_{m-1}}{2!} V_{b2}^2 + \frac{g_{m-3}}{3!} V_{b2}^3 + \dots, \quad (8)$$

where the second and third harmonics are g_{m-2} and g_{m-3} , respectively, which are further expressed as

$$I_{ds\ 1.2w2-w1} = \frac{3}{4} g_{m-3} V_{b1,w2}^2 \cdot V_{b1,w1}, \quad (9)$$

where g_{m-3} generates the third-order intermodulation which is almost neglected and considered nearly equal to zero.

5. Power Consumption Trade-Offs for Amplifiers

The bandwidth of WLAN application-based devices operates between 2.4 GHz and 2.48 GHz [23]. Figure 7 shows the thermal noise which can be observed between this range using the relation for drain thermal noise which is expressed as

$$i_{dn}^2 = 4kT_o \Delta f \gamma G_{do}, \quad (10)$$

where k is Boltzmann's constant in joules per kelvin, T_o is temperature in kelvin, Δf is the bandwidth in Hz, and γ is an enhancement factor [24]. The above equation can be written as

$$\frac{v^2}{R} = 4kT_o \Delta f \gamma G_{do}, \quad (11)$$

FIGURE 7: Comparative change in input vs. output noise in $nV/\sqrt{Hz}$ from 2.3 GHz to 2.6 GHz range.

or

$$v = \sqrt{4kT_o \Delta f \gamma G_{do} R}, \quad (12)$$

hence the difference between the output noise and input noise. Figure 8 shows the maximum levels of noise for both input and output ports. A change of $0.3 nV/\sqrt{Hz}$ of noise levels was observed at the output port with respect to the input port.

FIGURE 8: (a) The comparison of PAE to the input power and (b) the comparison of PAE to the output power. (c) Proof of the DC power consumption at a maximum level of 2.1 mW.

FIGURE 9: Continued.

FIGURE 9: (a) The input return loss (S11). (b) The 1 dB compression point. (c) The DC power consumption of M1 equals 985.1 uW when the input-referred drain current equals 547.5 uA. (d) The DC power consumption of M2 equals 1.194 mW when the input-referred drain current equals 663.5 uA.

6. DC Power Dissipation, Power-Added Efficiency (PAE), and Gate Biasing for Enhanced Power Backoff Efficiency

The DC power exponentially increases as the drain voltage increases. Figure 8(a) shows the maximum value of 2.1 mW

as the overall DC power consumption when V_{DD} reaches its maximum value of 1.2 volts. Both M1 and M2 are operating in a triode with even low subthreshold values for DC operating current of I_D [25]. The DC power consumption from both M1 and M2 can be summed up using the following equation:

$$P_{dc} = (\mu_n C_{ox})^2 \left[\left(\frac{W_1}{L_1} \right)^2 \{ (V_{b1} - V_{TH1}) V_{out1} - V_{out1}^2 \}^2 Z_{L4} + \left(\frac{W_2}{L_2} \right)^2 \{ (V_{b2} - V_{TH2}) V_{out2} - V_{out2}^2 \}^2 Z_{L6} \right], \quad (13)$$

where few of the individual parameters' findings using simulation tool are already shown under the heading

"Simulation findings using 65 nm CMOS technology." Also, $V_{out1} = V_{out2} = V_{DD}$ as no voltage drop is observed across

FIGURE 10: (a) The input return loss (S11), insertion loss (S12), and output return loss (S22) power-divider circuit. (b) The input-referred 1 dB compression point. (c) The input reflection loss (S11). (d) The output gain (S21). (e) The power-added efficiency (PAE). (f) Validated software results with yellow line showing input noise and red showing the output noise. (g) Harmonic content and power contours.

TABLE 1: Performance comparison of the proposed PA.

Specification	This work	[28]	[29]	[30]	[31]	[32]
Technology	65 nm	130 nm	40 nm	65 nm	180 nm	90 nm
Year	2021	2020	2019	2018	2017	2013
IEEE standard	802.15.4	802.15.4	802.15.6	802.15.4	802.15.1	802.15.4
Frequency	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
DC power consumption	2.1 mW	4.7 mW	1.5 mW	1.9 mW	10 mW	
DC current consumption	1.22 mA	—	—			9.2 mA
Supply voltages	1.2 volts	1.2 volts	0.9 volts	1 volt		1.2 volts
IIP3		−12 dBm				
Output power	2 dBm	0 dBm	−3.3 dBm	−3 dBm	5 dBm	0 dBm–4 dBm
1 dB compression point	4.1 dBm	−1.36 dBm	—	—	—	—
Input return loss (S11)	−13.1 dB	−10.3 dB	—	—	—	—
Gain (S21)	10.3 dB	—	—	—	8 dB	—
General class of PA	Doherty PA with fixed interstage capacitances	Class AB with current re-use	Switched capacitor digital PA (SCDPA) All digital scaling	PA-ADPLL all digital scaling	—	Load push-pull
Efficiency	29.85%	27%	39%	—	16%	—

L4 and L6. The length $L_1 = L_2 = 60$ nm is a default set value for TSMC 65 nm technology. The width to adjust the DC can be found using the equation above. The transistor is turned on, and keeping fixed gate voltage and fixed threshold voltage values, the area under the curve will be estimated for the perfect width to achieve this DC power consumption [26]. For our case, $W_1/L_1 = W_2/L_2 = 30 \mu\text{m}/60$ nm, showing the number of fingers equal to 5 and width per finger equal to $6 \mu\text{m}$. Each width can be theoretically estimated using the following equations:

$$\begin{aligned}
 W_1 &= \int_{V_{\text{off}}}^{V_{\text{on}}} I_{D1} dV_{\text{out } 1}, \\
 W_2 &= \int_{V_{\text{off}}}^{V_{\text{on}}} I_{D2} dV_{\text{out } 2}, \\
 W_1 &= (\mu_n C_{\text{ox}}) \left[(V_{b1} - V_{TH1}) \int_{V_{\text{off}}}^{V_{\text{on}}} V_{\text{out } 1} dV_{\text{out } 1} \right. \\
 &\quad \left. - \int_{V_{\text{off}}}^{V_{\text{on}}} V_{\text{out } 1}^2 dV_{\text{out } 1} \right], \\
 W_2 &= (\mu_n C_{\text{ox}}) \left[(V_{b2} - V_{TH2}) \int_{V_{\text{off}}}^{V_{\text{on}}} V_{\text{out } 2} dV_{\text{out } 2} \right. \\
 &\quad \left. - \int_{V_{\text{off}}}^{V_{\text{on}}} V_{\text{out } 2}^2 dV_{\text{out } 2} \right].
 \end{aligned} \tag{14}$$

The power-added efficiency (PAE) of the proposed HPA is 29.8%, which can be easily understood by $\eta = (P_{\text{out}} - P_{\text{in}})/P_{\text{dc}} \times 100$, where P_{in} and P_{out} represent the input power and output power, respectively. Theoretically, only class F power amplifier has the ability to achieve 100% of PAE [27], which is not possible for the case of Doherty due to different classes of PA. However, both biasing voltages at subthreshold regions are optimized at perfect matching to achieve the backoff level at 29.8% PAE. This PAE can be found at 4 dB backoff point.

7. The Overall Input Return Loss and Gain

The input return loss (S11) and output gain (S21) can be observed in Figure 9. The PA has a maximum gain (S21) of 10.3 dB with an input reflection loss (S11) of −13.4 dB observed at 2.4 GHz. The input referred 1 dB compression point is equal to 4.1 dBm. The total power of PA is 2.1 mW.

Using interstage capacitances through the path of lumped parameters to main and auxiliary amplifiers, less than 10 dB of input power has been reflected to the Wilkinson divider path which shows perfect impedance matching towards the input end. Gate-to-drain insulation for both $M1$ and $M2$ creates a negative conduction in reverse path. Similar perfect matching at the output enhances the gain even higher to 10 dB.

Major simulation results can be observed in Figure 10.

8. Performance Parameters of 2.4 GHz RF ULP Power Amplifier

Table 1 summarizes the performance of the proposed ULP-PA in comparison with other current state-of-the-art CMOS PAs. The parameter comparison does not include the post-layout design results.

9. Conclusion

In this study, the design and calculation of a ULP Doherty power amplifier using 65 nm CMOS technology were presented. The proposed method mentions equivalent lumped parameters for Wilkinson power divider and power combiner circuit along with interstage capacitances used before the main and peaking power amplifiers. The PA shows the peaking output power of 2 dBm with −7 dBm input. The measurement results are summarized in Table 1. The design consumes significantly low power by consuming as low as 2.1 mW DC power on overall main and peaking amplifiers.

10. Future Enhancement

The TSMC technology is a well-developed library based on 65 nm CMOS IC design which is cheaper to manufacture on mass-level production. The future project includes fabricating and manufacturing the simulated design. The contribution in research will lead to production of PAs for short-range WPAN sensing and data transfer devices under the umbrella of IEEE 802.15.x standard.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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