

Research Article

Design Methodology for Interfacing DERs to Power Systems through VSC

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This paper presents a methodology to connect distributed energy resources via an 84-pulse voltage source converter to three-phase system grid or load of standard or nonstandard voltage values. Transfer function blocks are included to illustrate interfacing among converters. The main input-output values to be considered in the application are detailed and the system can be modified to be included in other systems without loss of generality. The definition of the reactive component for supporting grid or load variations without degrading the overall performance is carried by for the DC-DC converter. A control variable for reducing the DC gain is used to improve the settling time. Our proposal defines the capacitive and inductive component values for an operating point and gives the option to reduce them when adding smoothed variations and adaptive controllers.

1. Introduction

Voltage source converters (VSC) have been used for many years to adapt DC voltage to three-phase AC voltage load or interfacing to grid for improving power quality by reducing the conducted low-frequency phenomena described in [1]. They are encouraged to follow the attributes of the steadystate phenomena listed in [2]. In recent years, VSCs have been used to add compatibility for the interoperability between utility electric power systems (EPSs) and distributed energy resources (DERs) [3]. Topologies used for VSC vary from multilevel, pulse width modulation (PWM), and multipulse, and each one has some advantages over the others depending on the application. Because of that, combinations of topologies have been used for improving the response in particular applications, such as that described in [4] for sag, swell, three-phase failure, and motor startup and in [5] for large induction motor control. DC-link capacitor or battery energy storage systems (BESS) are

needed for an optimal operation of the system based on VSC [6, 7]. Low ripple or almost constant DC-link signals require bulky components leading to slow dynamic response of the system while maintaining the DC voltage under established parameters. Complex control routines or switching strategies for reducing these components are needed [8]. Maintaining the voltage level on the capacitor is another field of research, as we can get the energy from AC or DC sources and with different amplitudes. When high DC gain is required, quadratic converters can be used [9, 10], but low modifications on the DC input voltage can bring to large AC output voltage variations, which might require complex control strategies to operate [11]. Practical engineering applications require the system to work with the least amount of measurements possible, but the controllers have to be robust enough to parametric variation, nonmodeled dynamics, and disturbances, so, the system becomes high complex to model, even in a specific application [12, 13]. One of the hardest tasks for the power systems' designer is to

develop a set of component values for interfacing standard or nonstandard nominal system voltages of low and medium voltages with distributed energy resource connection [14, 15]. This paper defines a methodology for connecting an 84-pulse VSC to the grid or load specifying the needed DC voltage for it. As this voltage can be obtained from different sources, we are using the grid with standard or nonstandard values to build the AC-DC converter. The configuration is complemented by a simple buck-boost converter with a limited gain to avoid big voltage variations in the load. The VSC's output is defined by transformers' output and DC input, but we can select the transformers' ratio gain "n" to limit DC gain. Capacitive and inductive component values are chosen to limit the ripple, but by using programmed trajectories for smoothed transitions, the reduction of these components and settling time is granted. DER can be connected as the AC source when its output is AC or as the input to the buck-boost converter when its output is DC without changing the method. Simulations for a big load are included to verify the appropriateness of the proposal.

2. Methodology

This section deals with the voltage characteristics of the three-phase system to be converted to a DC signal using a noncontrolled three-phase full-wave rectifier. After that, the DC signal might need to be adapted in magnitude; for this, we use a buck-boost converter. Then, the DC signal is converted again to a three-phase quasi-sinusoidal signal using an 84-pulse voltage source converter. Lastly, this signal will be connected to the grid if the system is used as a StatCom or to the load if this works in an isolated system. This scheme is presented in Figure 1. This scheme illustrates the kind of converter required to adapt the power signals for feeding a load or give the energy back to the grid. The starting point would be associated to the type of distributed energy resource output voltage available.

In many cases, a single AC-AC converter is preferred over this three part cascaded converter, but the harmonic distortion obtained can be very high, and controlling it might be a hard task, reducing its capacity of use to a specific application. For the sake of simplicity, the variable names used on this section are detailed in Table 1.

2.1. Input AC-DC Converter. On this study, a balanced threephase system with $v_{3\phi}$ of nominal RMS line voltage is used. For rectifying, it is needed to have a neutral point, so the phase peak voltage can be obtained by $V_m = v_{3\phi} \sqrt{2/3}$. Then, the phase voltage system is described by

$$v_{a} = V_{m} \sin(\omega t),$$

$$v_{b} = V_{m} \sin\left(\omega t - \frac{2\pi}{3}\right),$$

$$v_{c} = V_{m} \sin\left(\omega t + \frac{2\pi}{3}\right).$$
(1)

When this system is feeding a three-phase full wave rectifier for obtaining a DC signal, the average value V_{mean} and the root mean square V_{RMS} can be calculated by

$$V_{\text{mean}} = \frac{6}{\pi} \int_{0}^{\pi/6} (v_c - v_b) dt,$$
 (2)

$$V_{\rm RMS} = \sqrt{\left(\frac{6}{\pi} \int_{0}^{\pi/6} (v_c - v_b)^2 dt\right)}.$$
 (3)

With these two values, it is possible to know the ripple factor (RF) on the rectified signal. This is a measure of how far is a DC signal from a constant value. This is obtained by

$$RF = \frac{\sqrt{V_{RMS}^2 - V_{mean}^2}}{V_{mean}}.$$
 (4)

The lower RF on the output would bring better results in the DC-DC conversion, or it can be used to calculate a passive input filter.

When we manage control tasks for alternating currents, the usage of nonvarying signals reduces the computational effort, so it is important to use signals that are pure DC, and we can utilize the module of the three signals, defined by (5), as the reference:

$$V_{\text{module}} = \sqrt{v_a^2 + v_b^2 + v_c^2}.$$
 (5)

Consider a balanced system, $V_{\text{module}} = V_m \sqrt{3/2}$, which is equal to the value of line voltage $v_{3\phi}$.

2.2. Output DC-AC Converter. When using an 84-pulse voltage source converter for obtaining the AC signal from the DC signal, we get the peak value of the three-phase staircase sinusoidal \bar{V}_m when the YY converter is at its maximum value, but Y Δ is at its minimum on the diagram of Figure 2.

Considering the converter structure defined in [5] and references therein,

$$\dot{\overline{V}}_{m} = \frac{2n}{3} \left[2V_{DC} + a \left(3V_{DC} \right) \right] + \frac{n}{\sqrt{3}} \left[2V_{DC} - a \left(3V_{DC} \right) \right].$$
(6)

This equation shows (2n/3) as the gain of the six pulses *YY* transformers, $(n/\sqrt{3})$ as the gain of the $Y\Delta$ transformers, $(3V_{DC})$ as the amplitude of the seven-level inverter, $2V_{DC}$ is the central point or offset for the seven-level inverter, and *a* is the reinjection transformer ratio. The factor *n* is included in the case; we need to change the voltage output level in a fixed amount on the output transformers or add a coupling transformer with an integer transformer ratio. The factor *a* = 0.5609 is the optimized value to minimize the voltage THD, being according to IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems [16]. A strict reinjection transformer turns' ratio *a* is not obligated, as this factor can have 12.5% of variation to have a



FIGURE 1: Block diagram of the proposal with variable names.

TABLE 1: Acronyms and abbreviations.

Parameters	Description	Unit
$v_{3\phi}$	Input grid RMS line to line voltage	V
Vm	Input grid phase voltage amplitude	V
v _{a.b.c}	Input grid phase voltage	V
V _{mean}	Full wave rectified average voltage	V
V _{BMS}	Full wave rectified RMS voltage	V
RF	Ripple on the rectified DC output	%
V _{module}	DC equivalent of a three-phase input voltage	V
V _{DC}	DC capacitor voltage for 7-level inverter	V
V	Capacitor chain voltage $(4V_{\rm DC})$	V
\overline{V}_m	Output VSC phase peak voltage amplitude	V
$\frac{1}{v_{3\phi}}$	Output VSC RMS line to line voltage	V
a	Optimized reinjection transformer ratio	None
п	Integer factor for adjusting output transformers ratio	None
$v_{\mu\nu\mu}$	Output VSC phase voltage	V
$v_{\mu,\nu,\mu}$	Output VSC fundamental frequency phase voltage	V
$\delta^{\alpha_1,\alpha_1,\alpha_1}$	Phase shift among $v_{3\phi}$ and $v_{3\phi}^{0.0}$	rad
THD	Per phase output voltage total harmonic distortion	%



FIGURE 2: 84-pulse voltage source converter.

maximum THD lower than 3% when DC sources are used for the staircase signal generation [4].

The VSC phase voltage v_u can be calculated using the Fourier series of the staircase signal obtained at the VSC's

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output [4], which is related to the VSC phase peak voltage amplitude \bar{V}_m by the following expression:

$$v_{u} = \sum_{m=1}^{N} V_{u_{(2m-1)}} \sin\left((2m-1)\omega t\right),$$

$$V_{u_{(2m-1)}} = \frac{4\bar{V}_{m}}{3\pi(2m-1)} \left(A_{(2m-1)} + aB_{(2m-1)}\right),$$

$$A_{(2m-1)} = 2 + 2\cos\left(\frac{1}{3}\pi(2m-1)\right) + 2\sqrt{3}\cos\left(\frac{1}{6}\pi(2m-1)\right),$$

$$B_{(2m-1)} = \sum_{i=0}^{20} C_{i}\cos\left(\frac{i}{42}\pi(2m-1)\right),$$

$$C_{i} = \begin{cases} -3, & 1, & 1, & 1, & 1, & 1, & 1, \dots \\ -3\sqrt{3}, & \sqrt{3} - 1, \dots \\ -3, & -\sqrt{3} + 2, \end{cases}$$

$$(7)$$

In a similar way, v_v and v_w are obtained with a phase shift of $-2\pi/3$ rad and $2\pi/3$ rad, respectively. Figure 3 depicts the 84-pulse output used with this strategy.

The expected RMS line voltage for the VSC staircase signal to be connected to the point of common coupling (PCC) is

$$\dot{V}_{3\phi} = \frac{2\sqrt{2}nV_{\rm DC}\sqrt{-3\sqrt{3}a^2 + 6a^2 + 3\sqrt{3} + 6}}{3},\qquad(8)$$

where V_{DC} is the DC voltage of one capacitor or source of the ones connected in chain on the 7-level inverter, that is, the first part of the 84-pulse converter of Figure 2, and can be obtained with the next expression:

$$V_{\rm DC} = \frac{\overline{v}_{3\phi}}{2\sqrt{2}n\sqrt{-3\sqrt{3}a^2 + 6a^2 + 3\sqrt{3} + 6}}.$$
 (9)

In a natural way, it can be noticed that it is needed to match the input voltage from the grid to the output voltage of the VSC affected by a gain. This gain can be obtained by a DC-DC converter that will be analyzed in Section 2.3, but it can drift the system to obtain a high DC gain. If we do not want to increase the DC components, we can take advantage of the transformers used on the VSC's output by modifying the transformer ratio by the factor n, which can be obtained by

ratio =
$$\frac{3\psi}{v_{3\phi}}$$
,
 $n = \begin{cases} 1 & \text{for } m = 1 \\ r - 1 & \text{for } (\text{ratio}) < 0.5 \\ r & \text{otherwise} \end{cases}$ (10)

In this equation, "r" is the greatest integer less than or equal to "ratio."

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The total harmonic distortion (THD) indicates how far is the shape of the generated staircase signal $v_{u,v,w}$, from a pure sinusoidal signal with the grid fundamental frequency. It can be computed by adding all the RMS ratios from single harmonic to the fundamental frequency signal or using the simplified version illustrated in (11), which is utilized for the data presented in this paper:

$$\text{THD} = \sqrt{\left(\frac{v_u}{v_{u_1}}\right)^2 - 1},\tag{11}$$

where v_u represents the output VSC phase voltage and v_{u_1} is the output VSC fundamental frequency phase voltage.

2.3. DC-DC Converter Design. It is important to verify the input and output voltage levels to define the type of the DC-DC converter to be used. A great deal of converters to adapt



FIGURE 3: 84-pulse output voltage.

the DC voltage levels are available in the literature; many of them are encouraged to bring a high gain and are considered to step-up the voltage, but not all of them have the ability to step-down it. Among the ones with both attributes, Divya Navamani et al. [9] combine quadratic boosting with a multiplier cell, while Zhang et al. [10] merge one boost converter, one buck-boost converter, and one buck converter having a quadratic gain. In comparison, Hasanpour et al. [17] use a buck-boost converter along with a coupled inductor for increasing the voltage gain. As we are dealing with a rectified signal, we use V_{mean} (2) as input. The 7-level converter of Figure 2 goes up to $4V_{\rm DC}$, so we use this voltage as the output V_o of the converter. This work deals with the combination of one buck and one boost converter on their basic configuration connected in cascade to increase the dynamic range conversion and be able to reduce or increase the output using a simple configuration, as depicted in Figure 4.

The switch S_1 , diode D_1 , and inductor L in the dashed box constitute the first part of the converter, forming a buck converter, while the second part, that is also the inductor L, switch S_2 , and diode D_2 in the dotted box, is forming the boost converter.

In order to design this DC to DC converter, it is needed to know the parameters and variables of the system where it will be immersed. Considering a balanced system, the power needed for the load will be generated in a balanced way, so the base impedance can be calculated from (12) as

$$Z_B = \frac{\left(v_{3\phi}\left(\text{line}\right)\right)^2}{P_{3\phi}}.$$
 (12)

This impedance is used for the capacitive and inductive component calculation.

The gain of these buck and boost converters considering continuous conduction mode (CCM) can be obtained by (13) and (14), respectively:



FIGURE 4: Positive output buck-boost converter.

$$\frac{V_o'}{V_{\text{mean}}} = D,$$
(13)

$$\frac{V_o}{V_o'} = \frac{1}{1 - D'},$$
 (14)

where *D* is the duty cycle of the switches. It is important to remember that the output voltage of the DC-DC converter will split to the four capacitors of the seven-level inverter of the 84-pulse voltage source converter, so $V_o = 4V_{\rm DC}$. As both converters are connected in a cascaded way, using the expected interfacing gain, the equation that dominates the ratio output/input is

$$\frac{V_o}{V_{\text{mean}}} = \frac{D}{1 - D},\tag{15}$$

where $V_o = 4V_{\rm DC}$ is the converter output voltage and $V_{\rm mean}$ is the source voltage. It is important to notice from (15) that when *D* is lower than 50%, the converter is functioning as a buck, with a transfer ratio close to a linear function; with D = 50%, the output is equal to the input, and for larger values of *D*, the converter has a boost behavior, but it becomes highly nonlinear when *D* is larger than 70%, as depicted in Figure 5. For keeping the conversion ratio within the most linear part of the graphic, the proposal is to have (1/3) < D < (2/3), which bonds the ratio output/input to $(1/2) < (V_o/V_{\rm mean}) < 2$. If a higher ratio is expected, we will use *n* on the output transformers of the VSC.

At the moment of writing, there is a wide variation of switching times allowed on the available devices. We have chosen a low switching frequency $f_s = 20$ KHz in order for this strategy to work with most of the devices. *D* is the duty cycle defined as the time the switch is closed (t_{on}) in relation to the switching period $(T = (1/f_s))$:

$$D = \frac{t_{\rm on}}{T}.$$
 (16)

The controlling variable for the converter output voltage is going to be the duty cycle *D*, so it is convenient to represent (16) as the voltage transfer function:

$$D = \frac{V_o}{V_{\text{mean}} + V_o}.$$
 (17)

The size of the capacitive and inductive components is obtained for continuous conduction mode, considering the motor load is requiring the nominal line current and the impedance as three times the the ratio between nominal voltage and current:



FIGURE 5: Buck-boost voltage ratio.

TABLE 2: Motor and grid parameters.

Parameters	Value	Unit
$P_{3\phi}$	500	HP
$v_{3\phi}$ (line)	2300	V _{RMS}
f_B	60	Hz
$i_{B(a,b,c)}$	93.6	$A_{ m RMS}$
from this		
Z_B	14.188	Ω

$$L = \frac{V_{\text{mean}}}{f_s \Delta_{I_L}} D,$$

$$C = \frac{V_o D}{Z_B f_s \Delta_{V_C}}.$$
(18)

On (18), Δ_{I_L} and Δ_{V_C} are the allowable variations on the inductor current and voltage capacitor and are selected as 1% of the nominal current and 1% of the rated voltage at the steady state.

3. Simulation Results

The proposed methodology is suitable to be used by DC or AC sources to be connected to AC grid or load. In order to test it, this paper uses a 500 HP, $2300V_{RMS}$, 60 Hz, three-phase induction motor as a load, and three-phase AC grid inputs of several levels. If the input was DC, the strategy would initiate from V_{mean} and follow the same steps. Base power and base voltage are selected, and all parameters and variables are normalized using these base quantities [18]. The main motor parameters for connection to the grid are described in Table 2 [5, 18]. Three different ways to feed the motor for free acceleration are described in the following sections.

3.1. Case 1: Free Acceleration and n = 1. Several standard and nonstandard nominal system input voltages are selected for this study [14, 15] and concentrated in Table 3 for easier reading. These voltages include $690V_{\rm RMS}$ used as the output voltage by the largest wind turbine manufacturers and utilized as $v_{3\phi}(V)$ on this proposal [19] and $900V_{\rm DC}$ as the output voltage for a photovoltaic system used as $V_{\rm mean}(V)$ which is normally used when power exceeds $10 \, \rm kW$ [20]. Values of *L* and *C* are obtained according to Section 2.3, and THD is obtained using (11) after 10 seconds. As it is illustrated on this table, THD has no variations when n = 1.

The free acceleration plot for these cases is depicted in Figure 6. A faster response is observed when the ratio $(\bar{\nu}_{3\phi}/\nu_{3\phi}) \longrightarrow 1$.

As illustrated in voltage profile (Figure 7), the behavior of the whole system is a second-order under damped system with base impedance Z_B constant, and components L and Cchange to have faster settling time. Again, the response is faster when the ratio $(\overline{v}_{3\phi}/v_{3\phi}) \longrightarrow 1$.

3.2. Case 2: Free Acceleration and n Variant. By limiting the DC gain to $(1/2) < (V_o/V_{mean}) < 2$ as expressed in Section 2.3, we obtain the results of Table 4, with substantial improvement on the settling time for rotational speed and voltage profile, as observed in Figure 8 for the free acceleration and Figure 9 for the voltage profile. It can be inferred that it is recommended to limit the DC-DC gain. THD is also computed by using (11) after 10 seconds. It is observed that the THD increases when the value of *n* increases.

3.3. Case 3: Free Acceleration and Bézier Curve. If the VSC is intended to connect a motor, the rotor speed regulation tasks and starting up can be smoothed by using a Bézier curve for the voltage that shows a more convenient transition [21, 22]. The component values are the ones indicated in Table 5. This case presents a voltage trajectory given by

$$v_{a,b,c}^{\star} = \begin{cases} 0 & \text{for } 0 \le t \le t_1 \\ v_{a,b,c} \mathfrak{B}_1 & \text{for } t_1 < t < t_2 , \\ v_{a,b,c} & \text{for } t \ge t_2 \end{cases}$$
(19)

with Bézier curves

$$\mathfrak{B}_{j} = \sum_{k=1}^{6} r_{k} \left(\frac{t - t_{j}}{t_{j+1} - t_{j}} \right)^{4+k}, \quad j = 1, 3,$$
(20)

where $r_1 = 252$, $r_2 = -1050$, $r_3 = 1800$, $r_4 = -1575$, $r_5 = 700$, $r_6 = -126$, $t_1 = 0$ s, and $t_2 = 0.5$ s.

The settling time for rotational speed and voltage profile is reduced, making the system faster. As it is illustrated in Table 5, THD increases as n increases. If the variation is bounded to 1% on voltage and current for the DC-DC converter, we can even reduce the value of the L and C to an optimum, which will be calculated on a new research. Figure 10 presents the free acceleration response, and Figure 11 is the voltage profile.

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TABLE 3: Parameter values for case 1: Δ_{I_L} (1%), Δ_{V_C} (1%), n = 1, and $Z_B = 14.19\Omega$.

$v_{3\phi}(V)$	$V_{\text{mean}}(V)$	$\nu^{0.0}_{3\phi}(V)$	L(H)	C(F)	THD(%)
220	297.10	2300	0.0143896	0.000319495	2.43
440	594.21	2300	0.0263209	0.000292203	2.43
600	810.28	2300	0.0337927	0.000275112	2.43
690 (wind turbine)	931.83	2300	0.0376238	0.000266349	2.43
– – (PV array)	900.00	2300	0.0366445	0.000268589	2.43



FIGURE 6: Rotational speed n = 1 (rad/s).



FIGURE 7: Voltage profile n = 1 (V).

			L	0		
п	$\nu_{3\phi}(V)$	$V_{\text{mean}}(V)$	$\nu^{0\cdot 0}_{3\phi}(V)$	L(H)	C(F)	THD(%)
9	220	297.10	2300	0.000915092	2.03179e – 05	6.02
4	440	594.21	2300	0.00435048	4.82972e - 05	3.08
2	600	810.28	2300	0.013857	0.000112812	2.48
2	690 (wind turbine)	931.83	2300	0.0151196	0.000107036	2.48
2	– – (PV array)	900.00	2300	0.0148017	0.00010849	2.48

TABLE 4: Parameter values for case 2: Δ_{I_L} (1%), Δ_{V_C} (1%), and $Z_B = 14.19\Omega$.



FIGURE 8: Rotational speed *n* variant (rad/s).



FIGURE 9: Voltage profile *n* variant (V).

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TABLE 5: Parameter values for case 3: $\Delta_{I_L}(1\%)$, $\Delta_{V_C}(1\%)$, and $Z_B = 14.19\Omega$.

п	$v_{3\phi}(V)$	$V_{\text{mean}}(V)$	$\nu^{0\cdot 0}_{3\phi}(V)$	L(H)	C(F)	THD(%)
9	220	297.10	2300	0.000915092	2.03179 <i>e</i> - 05	6.01
4	440	594.21	2300	0.00435048	4.82972e - 05	3.06
2	600	810.28	2300	0.013857	0.000112812	2.48
2	690 (wind turbine)	931.83	2300	0.0151196	0.000107036	2.48
2	– – (PV array)	900.00	2300	0.0148017	0.00010849	2.48



FIGURE 10: Rotational speed n variant and Bézier curve (rad/s).



FIGURE 11: Voltage profile *n* variant and Bézier curve (V).

4. Conclusions

This proposal defines a straightforward methodology for calculating the DC-DC capacitive and inductive component values used for interfacing energy resources of different AC or DC voltage levels by using a VSC of 84 pulses. The strategy can be used also for driving AC motors or improving power quality on three-phase systems. The use of an 84-pulse voltage source converter at the point of common coupling allows to have low-voltage THD to accomplish standard limits. Defining the voltage transfer function in terms of nfor the DC-AC converter gives the possibility of reducing the settling time to get the load expected characteristics, such as the speed of an induction motor. On this fashion, using a traditional buck-boost converter with a restricted operating range makes the interfacing between different voltage levels as an easy task. The nominal 1% of variation on the current and voltage for reactive components allows to obtain the initial values for base behavior. Bézier curves for smoothing behavior allow the reduction in the settling time and voltage ripple. As the ripple is reduced, further research will be conducted to reduce the capacitive and inductive components to optimum values and being within operating limits. Classical or modern control strategies for power, speed, or any variable required will be better achievable while using a power electronics interface with performance like the one of this proposal.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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