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Research Article

An Improved Active Damping Method Based on Single-Loop Inverter Current Control for LCL Resonance in Grid-Connected Inverters

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This paper investigates active damping of LCL filter resonance in grid-connected inverters with only inverter current feedback control, since it only needs to sample one current to realize both current control and inverter protection. The traditional single-loop inverter current control (SLICC) can damp the LCL filter resonance actively. However, if the control delay is considered in digital control, the system stability will depend on the ratio of the LCL resonance frequency f_{res} to the sampling frequency f_s, and the valid damping region is only up to $f_s/6$. Considering that the design region of the LCL resonance frequency f_{res} is up to $f_s/2$, the system can easily become unstable due to the LCL resonance frequency shifting. Thus, this paper proposes an improved active damping method based on SLICC, including the asymmetric regular sampling method and delay compensation method. The improved sampling method minimizes the control delay without introducing a switching ripple, and the delay compensation method further compensates for the delay effect. With a proper parameter design, the upper limit of the valid damping region is extended up to $f_s/2$, which can cover all the possible resonance frequencies, and it has inherent robustness against grid-impedance variation. Finally, a few simulations in MATLAB/SIMULINK and experiments based on a 6 kW prototype are performed to verify the theoretical analysis.

1. Introduction

Recently, the renewable energy distributed generation technique is attracting more and more attention, to deal with the increasing concern of the exhaustion of fossil fuels and the environmental pollution. Grid-connected inverters are the key devices to connect the distributed systems to the power grid [1]. As the grid-connected inverter is controlled by the pulse width modulation (PWM), the output current contains an amount of switching harmonics. The LCL filter is widely used due to its better attenuation capability of the switching harmonics and cost advantage compared with L filter. However, the LCL filter is a third-order low-damping system, which challenges the stability of the whole system [2].

In order to stabilize the system, a variety of active damping techniques without power losses have been developed. Generally, the traditional active damping techniques can be classified into two modes based on whether an additional sensor is needed, except for the essential sensors of the control current and grid voltage: the single-loop and the multiloop feedback control. The multiloop feedback control methods introduce additional damping terms into the current control loop by sensing additional variables, such as capacitor current [3–6] or capacitor voltage [7]. Due to their flexible and efficient implementation, these methods have been widely used. However, requiring additional sensors increases the hardware cost and affects the system's reliability. Alternatively, a state observer can be used to simplify the system hardware effectively [8, 9], but it is sensitive to system parameter uncertainties and variations [10].

Simultaneously, the single-loop feedback control methods can avoid these problems and have increasingly been studied in [11–25], including inverter current control and grid current control. In [11], it is first pointed out that the inverter current contains capacitor current component so that the inverter current control can promise stable operation. Moreover, inverter current control is beneficial to the instantaneous overcurrent protection for the inverter, which is more convenient to be implemented and popular in industrial applications [12]. But good damping can be achieved only when the resonance frequency is low enough. In order to increase the damping, an active damping inner loop control is introduced. It is implemented by extracting the high-frequency components of the inverter current or grid current to simulate the capacitor current [13–15], and the first-order High Pass Filter (HPF) is the most popular filter. However, when the control current is the grid current, it may not be able to introduce sufficient damping since the high-frequency components have been filtered by the filter capacitor, which might result in the need to compromise between the resonance frequency offset and the resonance suppression ability [16].

On the other hand, the control delay is introduced in the digital control implementation process, and it has a significant influence on all active damping techniques [17–19]. The system stability will depend on the ratio of the LCL resonance frequency f_{res} to the sampling frequency f_s. For the single-loop feedback control without active damping inner loop or the multiloop feedback control, the critical frequency is $f_s/6$ [17, 18], while it can increase to $f_s/3$ at most when adopting the active damping inner loop [20]. Thus, the LCL resonance frequency must be away from the critical frequency to enhance the system damping. Unfortunately, considering the potential variation of the grid inductance, the LCL resonance frequency may shift to the critical frequency; thus, the system stability cannot be promised [21–23]. Hence, how to decrease the control delay and increase the critical frequency is a research focus in recent years.

The control delay is reduced by adjusting the sampling instant [17] or multisampling [12], but the sampling instant may be no longer the switching instant of the power tube. It is easy to introduce the switching frequency harmonics into the control loop and deteriorate the system stability [16]. Alternatively, the filter-based methods are presented in [24–26]. By inserting a digital filter in the forward path, the frequency characteristics around the LCL resonance frequency can be changed. But such a solution relies on the accuk6rate filter parameters; the variation of grid inductance may greatly affect the system stability. Thus, it is very difficult to enhance the system stability only by reducing the control delay or introducing digital filters. Therefore, in [22], a robust method including the double-sampling double-loading (DSDL) mode and a lead grid current control part is proposed, and a similar method based on the inverter current control is proposed [16]. The DSDL mode minimizes the control delay and the lead control part further compensates for the delay effect. However, the active damping inner loop can be equivalent to a second-order filter since a first-order HPF is in series with a first-order lead control part in it. Thus, the order of the system control is increased. The amplitude and phase characteristics of high-order filters vary more sharply and widely, making the parameters design more difficult [15].

In this paper, an improved SLICC is proposed. This method extends the valid damping region up to $f_s/2$, improving the system stability margin greatly without increasing the control algorithm complexity and system cost. And it has inherent robustness against grid-impedance variation. The remainder of this paper is organized as follows. In Section 2, the control scheme and the mathematical model of a three-phase grid-connected inverter with an LCL filter are presented at first. The equivalent impedance model of the SLICC considering the control delay is established, and the detailed system stability analysis is given in Section 3. In Section 4, an improved SLICC for extending the valid damping region up to $f_s/2$ is proposed. Moreover, a step-by-step parameter design procedure is presented. Section 5 shows the simulations and experimental results and Section 6 summarizes the conclusions.

2. System Modeling and Description

Figure 1 shows the circuit diagram and control scheme of a three-phase grid-connected inverter with an LCL filter and a constant DC voltage source U_{dc}, where C is the filter capacitor and L_1 and L_2 are the filter inductance of the inverter side and the grid side, respectively. Considering the worst-case condition, where no passive damping of the resonance exists and the system becomes more unstable, the parasitic series resistances of its filter inductor and filter capacitor are all neglected here. u_g is the grid voltage, and it has been assumed as balanced, which then allows per-phase diagrams to be used for analysis. i_1 and i_2 are the inverter and grid current, respectively. In this paper, to reduce the impact on the low-frequency stability of the system, the synchronous reference frame phase-locked loop (SRF-PLL) with low bandwidth has been employed to synchronize the inverter to the point of common coupling (PCC) voltage [20].

The overall control structure for per-phase based on SLICC is depicted in Figure 2. For simplicity, the equivalent gain of the inverter is set to 1. $G_{\text{PR}}(s)$ is the current controller, whose notation is given as follows [10]:

$$G_{\text{PR}}(s) = K_p + \frac{2K_r\omega_i s}{s^2 + 2\omega_i s + \omega_0^2}, \tag{1}$$

where K_p and K_r are the proportional and resonance gains, respectively, ω_i is the bandwidth of the resonance term, and ω_0 is the grid fundamental angular frequency.

Generally, the digital signal processor (DSP) is introduced to control the grid-connected inverter, and the most common mode for PWM is the single-update mode. Thus, the computation and PWM delays should be considered. Specifically, $G_{d1}(s)$ represents the computation delay, which is one sampling period in the traditional sampling scheme. $G_{d2}(s)$ is the PWM delay, caused by the zero-order hold (ZOH) effect. Thus, the total delay in the system can be expressed as [17]

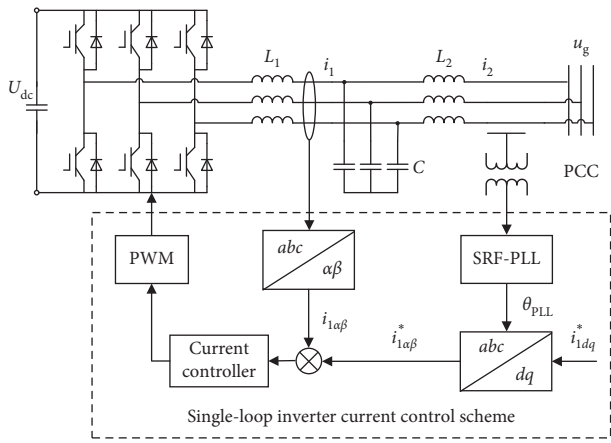

Figure 1: Three-phase grid-connected inverter with an LCL filter.

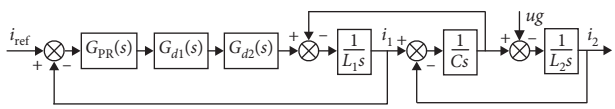

Figure 2: Per-phase control diagram with SLICC strategy.

$$G_d(s) = e^{-1.5sT_s}, \tag{2}$$

where T_s is the sampling cycle of the digital control system.

$G_{LCL}(s)$ is the transfer function of the LCL filter under SLICC strategy, as shown in the following equation:

$$G_{LCL}(s) = \frac{L_2 C s^{21} + 11}{L_1 L_2 C s^3 + (L_1 + L_2)s}. \tag{3}$$

3. Impedance-Based Analysis

This section generalizes the physical circuit property of the SLICC by presenting an impedance-based analysis [27]. For demonstrating circuit properties realized by SLICC, the control diagram is redrawn as in Figure 3(a) by sensing the voltage of the inverter-side inductance instead of the inverter current, and the equivalent circuit of LCL filter can be shown as Figure 3(b). This informs that the SLICC is equivalent to a virtual impedance $Z_v(s)$ connected in series with the inverter-side inductance. The expression of $Z_v(s)$ can be written as

$$Z_v(s) = G_{PR}(s)e^{-1.5sT_s}. \tag{4}$$

Thus, the equivalent virtual impedance $Z_v(s)$ can be shaped by varying $G_{PR}(s)$ and $G_d(s)$. Since the resonance term of $G_{PR}(s)$ mainly affects the frequency characteristics of the system at the fundamental frequency [19], the equivalent virtual impedance $Z_v(s)$ is simplified as $K_p e^{-1.5sT_s}$ for simplicity.

If the control delay $G_d(s)$ is neglected, the equivalent virtual impedance is a constant positive resistance with a value of K_p, which damps the LCL resonance peak. Therefore, the SLICC can provide inherent damping to stabilize the system [18].

When the control delay $G_d(s)$ is incorporated, the frequency expression of the equivalent virtual impedance is yielded as

$$\begin{aligned} Z_v(j\omega) &= K_p(\cos 1.5\,\omega T_s - j \sin 1.5\,\omega T_s) \\ &= R_v(\omega) + jX_v(\omega). \end{aligned} \tag{5}$$

It shows that the control delay changes the constant positive resistance to a virtual impedance which is composed of resistance and reactance, whose frequency characteristics are shown in Figure 4, and f_s is the sampling frequency. The equivalent virtual resistance $R_v(\omega)$ could be positive or negative depending on the frequency range, whose critical frequency f_R is $f_s/6$. Similarly, the equivalent virtual reactance $X_v(\omega)$ could be inductive or capacitive and its critical frequency f_X is $f_s/3$. The negative $R_v(\omega)$ will add open-loop right-half-plane (RHP) poles to the system, introducing a nonminimum-phase closed-loop behavior to the system, which can impair the overall system stability and robustness [20]. The existence of $X_v(\omega)$ will shift the LCL resonance frequency f_{res} [16]. As the damping effect, that is, stability of system, is determined by $R_v(\omega)$ [22], the critical stable frequency of the traditional digital control system adopting SLICC is $f_s/6$. When the actual LCL resonance frequency f_{res} is up to $f_s/6$, the system will be unstable due to the lack of necessary damping for the LCL resonance peak. Therefore, the control delay $G_d(s)$ plays a decisive role in the stability of digital control system.

To identify the critical frequency f_R of $R_v(\omega)$ when the control delay varies, $G_d(s)$ can be rewritten as $e^{-\lambda sT_s}$ (normally $0 < \lambda \le 1.5$). When $R_v(\omega)$ is assumed to zero, it leads to

$$\cos(\lambda \cdot 2\pi x) = 0, \tag{6}$$

where x is the ratio of the critical frequency f_R to the sampling frequency f_s.

Figure 5 shows the relationship between x and λ according to (6). As shown in Figure 5, the critical frequency gradually increases as the control delay decreases. In particular, when the control delay decreases to $e^{-0.5sT_s}$, the critical frequency reaches the upper limit of the LCL resonance frequency design value, that is, $f_s/2$. That is, if the control delay can be reduced to $e^{-0.5sT_s}$, the system stability can be ensured with the SLICC within the design range of the LCL resonance frequency.

Due to the inherent characteristics of the digital control system, reducing the control delay to $e^{-0.5sT_s}$ can only be realized by increasing the sampling frequency. In this case, the sampling frequency should be increased to three times its original value [12]. However, it may lead to problems that introduce the switch ripple into the control loop and multiple intersections between the modulated wave and the carrier [3]. That makes the method impractical.

4. Proposed Active Damping Method

Based on the above discussions, there is a need to decrease the control delay and compensate for its side effects. In this section, an improved active damping method based on SLICC is proposed, which includes the asymmetric regular

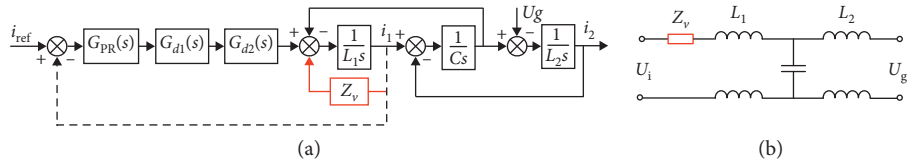

Figure 3: Equivalent control diagram and circuit of control diagram with SLICC strategy.

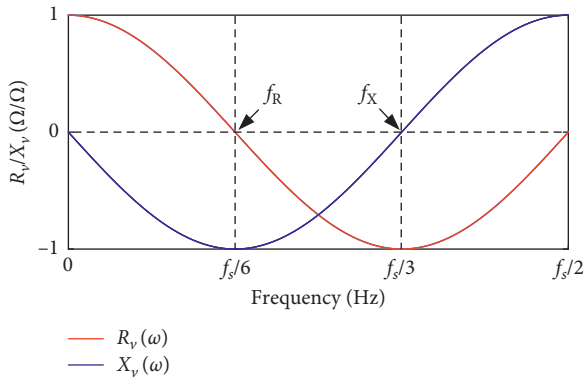

Figure 4: Frequency-domain characteristics of $R_v(\omega)$ and $X_v(\omega)$.

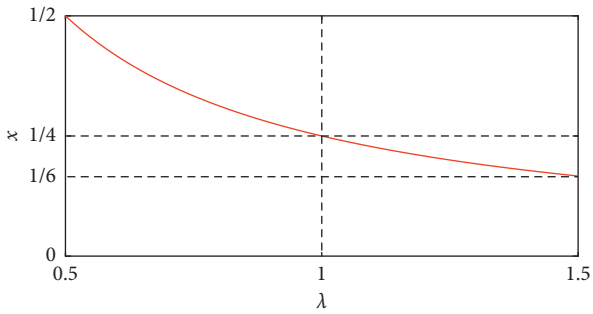

Figure 5: Relationship between x and λ.

sampling method and the delay compensation method. The proposed active damping method can extend the valid damping region up to $f_s/2$, improving the system stability and robustness. The traditional SLICC has inherent robustness against grid-impedance variation, since the grid-impedance decreases the LCL resonance frequency [18]. The proposed active damping method can inherit this feature due to no additional active damping inner loop in the control loop.

4.1. Asymmetric Regular Sampling Method. In the digital control system, in order to avoid the influence of switching noise, the signal sampling and update are operated at the peak or valley of the triangular carrier. The sampling signals are sent to the DSP; then the modulation waveform is obtained by calculating these signals with the control algorithm. Meanwhile, to avoid the phenomenon of multiple intersections between the modulation waveform and the triangular carrier, the calculated modulation waveform is updated at the next sampling instant, as shown in Figure 6(a). The computation delay is the duration between sampling instant of the signal and update instant of the corresponding calculated modulation waveform, which is equal to e^{-sT_s}. The PWM is often modeled as a ZOH, so the PWM delay is considered as half of the sampling period, which is equal to $e^{-0.5sT_s}$. Thus, the total control delay in the control loop is $e^{-1.5sT_s}$.

In order to directly reduce the control delay, the asymmetric regular sampling method is adopted, as shown in Figure 6(b). Instead of sampling and updating the signals one time in a control period, this method samples and updates twice time, which means that the signal sampling and update are operated at the peak and valley of the triangular carrier. Since the sampling frequency and update frequency are both doubled, the control delay is reduced to $e^{-0.75sT_s}$, without changing the switching frequency and introducing the switching ripple. It is worth mentioning that, since the sampling frequency is doubled, this method requires a higher precision current sensor.

4.2. Analysis and Design of Delay Compensation Method. As shown in Figure 5, when the control delay is $e^{-0.75sT_s}$, the critical frequency of the equivalent virtual resistance is around $f_s/3$. In this section, the delay compensation method is further introduced to compensate for the delay effect, realizing $f_R \geq (f_s/2)$ and ensuring that the system has a sufficient stability margin at f_{res}.

Considering that the controller needs to be discretized, the simplest form of the delay compensator can be expressed as [22]

$$G_{C1} = \frac{1}{1 + e^{-0.5ksT_s}}, \tag{7}$$

where $k = 1, 2, \ldots, m$. Since the sampling frequency has doubled, the minimum delay in the control loop is $e^{-0.5sT_s}$. Then the equivalent virtual impedance can be expressed as

$$\begin{aligned} Z_{v1}(j\omega) &= K_P \frac{e^{-0.75sT_s}}{1 + e^{-0.5ksT_s}}\Big|_{s=j\omega} \\ &= \frac{K_p\left(A_1(\omega) + jB_1(\omega)\right)}{C_1(\omega)} \\ &= R_{v1}(\omega) + jX_{v1}(\omega), \end{aligned} \tag{8}$$

where

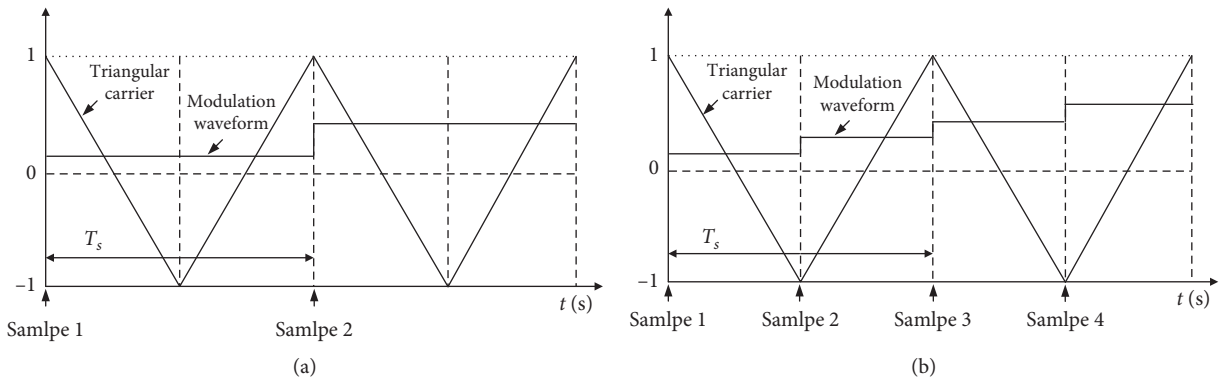

Figure 6: Implementation principle of different sampling method. (a) Symmetry regular sampling method. (b) Asymmetric regular sampling method.

$$\begin{cases} A_1(\omega) = \cos 0.75\,\omega T_s\,(1 + \cos 0.5\,k\omega T_s) + \sin 0.75\,\omega T_s \sin 0.5\,k\omega T_s, \\ B_1(\omega) = \cos 0.75\,\omega T_s \sin 0.5\,k\omega T_s + \sin 0.75\,\omega T_s\,(1 + \cos 0.5\,k\omega T_s), \\ C_1(\omega) = 2 + 2\cos 0.5\,k\omega T_s. \end{cases} \tag{9}$$

In order to ensure $f_R \geq (f_s/2)$, the equivalent virtual resistance should be positive within the interval of $(0, (f_s/2)]$; thus, the constraints are derived as

$$\begin{cases} A_1(\omega) > 0, C_1(\omega) > 0, & f \in (0, 0.5 f_s), \\ A_1(\omega) \geq 0, C_1(\omega) > 0, & f = 0.5 f_s. \end{cases} \tag{10}$$

Therefore, k is within the interval of $[1, 2)$. Figure 7 shows the frequency-domain characteristics of $R_{v1}(\omega)$ and $X_{v1}(\omega)$ with different k values. As can be seen in Figure 7, when $k = 1$, $R_{v1}(\omega)$ decreases as the frequency increases and decreases to 0 at $f_s/2$. That means there is no damping at $f_s/2$, and the more the LCL resonance frequency f_{res} closer to $f_s/2$, the smaller the stability margin. However, the LCL resonance frequency f_{res} can be designed close to $f_s/2$, and the change of the filter inductance L and the filter capacitor C may shift the actual LCL resonance frequency toward $f_s/2$, worsening the system stability margin.

In contrast, when $k = 1.5$, $R_{v1}(\omega)$ stays constant within the interval of $(0, f_s/2]$, which means the system has a sufficient stability margin whatever the LCL resonance frequency f_{res} is. However, $k = 1.5$ cannot be implemented in digital control system, and the only practical case would be $k = 1$. Nevertheless, the main goal of the above analysis is that there is a value that can satisfy the delay compensation requirements. As illustrated in [4, 21, 22], the delay compensation method works through compensating the lagging phase. Thus, we can mimic the delay compensator G_{C1} by the lead compensator.

Figure 8 shows the Bode diagram of the delay compensator G_{C1} for different k ($k = 1, 1.5$). The leading phases at $f_s/2$ are 45° and around 66°, respectively. Apparently, the leading phase at $f_s/2$ when $k = 1.5$ is much larger than it when $k = 1$ that is why the system can be more stable when $k = 1.5$. To compare the performance of the lead compensator with the delay compensator, the leading phases at $f_s/2$ are the same; that is, $\theta_1 = 45°$ and $\theta_2 = 66°$. And the

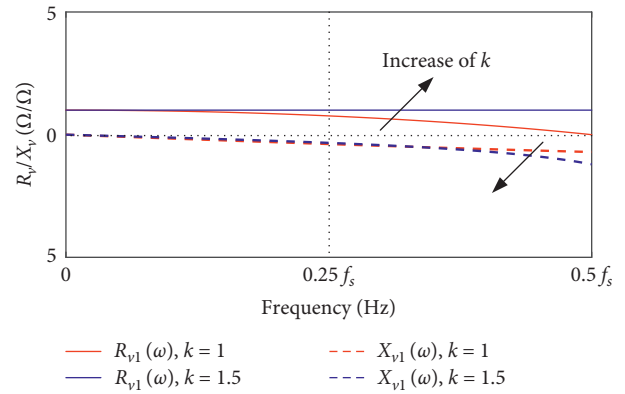

Figure 7: Frequency-domain characteristics of $R_{v1}(\omega)$ and $X_{v1}(\omega)$ with different k values.

attenuation of the transmission coefficient of the open loop is fully compensated, as shown in Figure 8. The form of the compensator can be expressed as [12]

$$G_{C2} = \frac{Ts + 1}{\alpha T s + 1}, \tag{11}$$

where α and T are

$$\begin{cases} \alpha = \dfrac{1 - \sin\theta}{1 + \sin\theta}, \\ T = \dfrac{1}{2\pi f \sqrt{\alpha}}. \end{cases} \tag{12}$$

Thus, the equivalent virtual impedance of the system can be expressed as

$$\begin{aligned} Z_{v2}(s) &= K_P G_{C2}|_{s=j\omega} \\ &= \frac{K_p\,(A_2(\omega) + jB_2(\omega))}{C_2(\omega)} \\ &= R_{v2}(\omega) + jX_{v2}(\omega), \end{aligned} \tag{13}$$

where

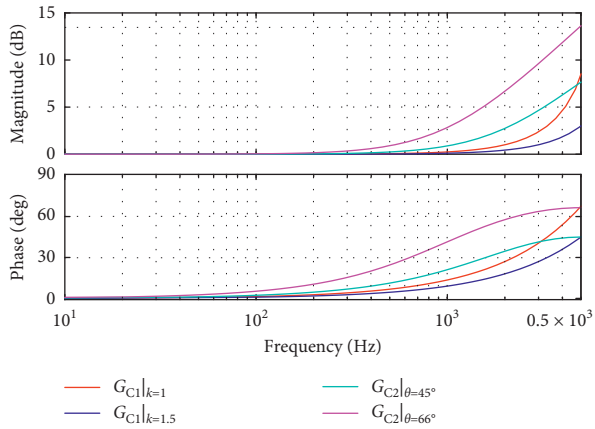

FIGURE 8: Bode diagram of G_{C1} and G_{C2} with different leading phases.

$$\begin{cases} A_2(\omega) = \left(1 + \alpha T^2 \omega^2\right)\cos 0.75\,\omega T_s + (1-\alpha)T\omega \sin 0.75\,\omega T, \\ B_2(\omega) = (1-\alpha)T\omega \cos 0.75\,\omega T_s - \left(1 + \alpha T^2 \omega^2\right)\sin 0.75\,\omega T_s, \\ C_2(\omega) = 1 + (\alpha T \omega)^2. \end{cases} \tag{14}$$

Figure 9(a) shows the frequency-domain characteristics of $R_{v1}(\omega)$ and $R_{v2}(\omega)$; Figure 9(b) shows the frequency-domain characteristics of $X_{v1}(\omega)$ and $X_{v2}(\omega)$. As can be seen from Figure 9(a), through the same leading phase at $f_s/2$, $R_{v2}(\omega)|_{\theta=45^\circ}$ is always greater than $R_{v1}(\omega)|_{k=1}$ within the interval of $(0,\ f_s/2)$. This is because the lead compensator can provide a bigger leading phase. What is more, $R_{v2}(\omega)|_{\theta=45^\circ}$ is greater than $R_{v1}(\omega)|_{k=1.5}$ within the interval of $(0,\ 0.4f_s)$, and the range can be extended to $(0,\ f_s/2)$ by increasing the leading phase. Thus, the system can achieve more effective damping when the lead compensator is introduced, and the parameters design procedure can be more flexible.

It is worth mentioning that $X_{v2}(\omega)|_{\theta=45^\circ}$ is always greater than $X_{v1}(\omega)|_{k=1}$ within the interval of $(0,\ f_s/2)$, even greater than $X_{v1}(\omega)|_{k=1.5}$, as shown in Figure 9(b). And $X_{v2}(\omega)$ can be greater within high-frequency interval by increasing the leading phase θ. This is because of the amplitude amplification effect of the lead compensator, resulting in shifting the actual resonance frequency f_{res} toward $f_s/2$, decreasing the stability margin of the system. Thus, the leading phase θ should be designed carefully.

4.3. Design Guideline for the Proposed Active Damping Method. In this section, a step-by-step parameter design procedure considering the phase margin (PM) and the gain margin (GM) of the system is summarized as follows:

Step 1. Consider the requirements of the power level and the current limit of the inverter; the switching harmonic suppression ability, the filter inductances L_1 and L_2, and filter capacitance C are preliminarily determined [1].

Step 2. Set the cutoff frequency f_c according to the sampling frequency f_s, low-frequency harmonic suppression ability, and overshoot constraint. As reported in [10], to achieve an overshoot within the reasonable range, $f_0 < f_c < 4\% f_s$ is expected with PM_1 at f_c over 60°, where f_0 is the fundamental grid frequency.

Step 3. Specifically, K_p is related to f_c by [5]

$$K_p = 2\pi f_c (L_1 + L_2). \tag{15}$$

When PR controller is adopted, the magnitude of the loop gain at f_0 should be bigger than 75 dB, ensuring that the amplitude error is less 1% at the rated power [5]. Once f_c is specified, K_p and K_r can be determined.

Step 4. Draw the Bode diagram of the open-loop transfer function of the overall system with the asymmetric regular sampling method only. Generally, the PM_2 at f_{res} is expected within the interval of $[30^\circ, 60^\circ]$, and GM > 5 dB is expected [5]. Then examine the actual PM_2 and GM. If the actual PM_2 or GM is not satisfied, go back to Step 3 and slightly decrease K_p and K_r.

Step 5. If the actual PM_2 or GM cannot be satisfied only by decreasing K_p and K_r, introduce the delay compensator and examine the actual PM_2 and GM. Go back to Step 3 and slightly decrease K_p and K_r if necessary.

Step 6. If the actual PM_2 or GM still cannot be satisfied, introduce the lead compensator and set the leading phase θ at $f_s/2$ to be $= \pi/4$. Go back to Step 3 and slightly decrease K_p and K_r if necessary. If it is not satisfied again, increase the leading phase according to the difference between the actual PM_2 and the preset value, and further slightly decrease K_p and K_r. If it is still not satisfied, go back to Step 1 and slightly decrease the LCL resonance frequency and repeat the other steps until the system stability requirements are met. The flowchart can be shown in Figure 10.

The parameters are designed according to the design procedure, as shown in Table 1. Figure 11 shows Bode diagram of the overall system with the designed parameters, and the stability requirements are satisfied, since $\text{PM}_1 = 70^\circ$, $\text{PM}_2 = 31^\circ$, and GM = 6.5 dB.

5. Simulation and Experiment Results

5.1. Simulation Results. To verify the above analysis and the proposed active damping method, a simulation model based on Figure 1 is built in the MATLAB/SIMULINK, and the main system parameters are shown in Table 1.

For verifying the analysis of the critical frequency of the SLICC, the LCL resonance frequency f_{res} is selected as $0.24 f_s$ by intentionally increasing the filter capacitance C to $9.4\,\mu$F. Figure 12 shows the simulated grid current for this case. As shown in Figure 12(a), when f_{res} is bigger than the critical frequency of the traditional SLICC, that is, $f_s/6$, the system cannot be stabilized. After decreasing the control delay by adopting the asymmetric regular sampling method, the system can be stabilized while the grid current still

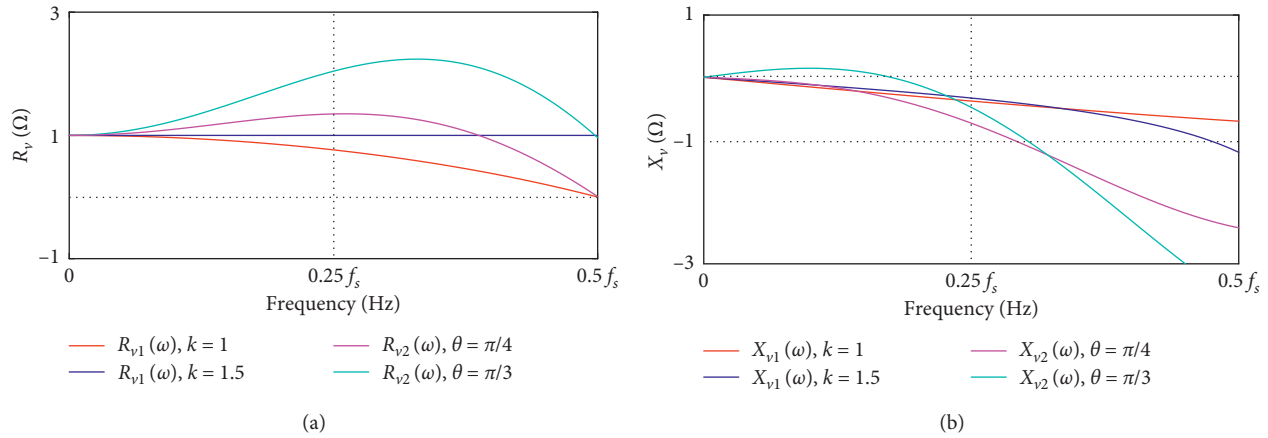

Figure 9: Frequency-domain characteristics of the equivalent virtual impedance with different leading phases. (a) $\mathbf{R_{v1}}(\omega)$ and $\mathbf{R_{v2}}(\omega)$; (b) $\mathbf{X_{v1}}(\omega)$ and $\mathbf{X_{v2}}(\omega)$.

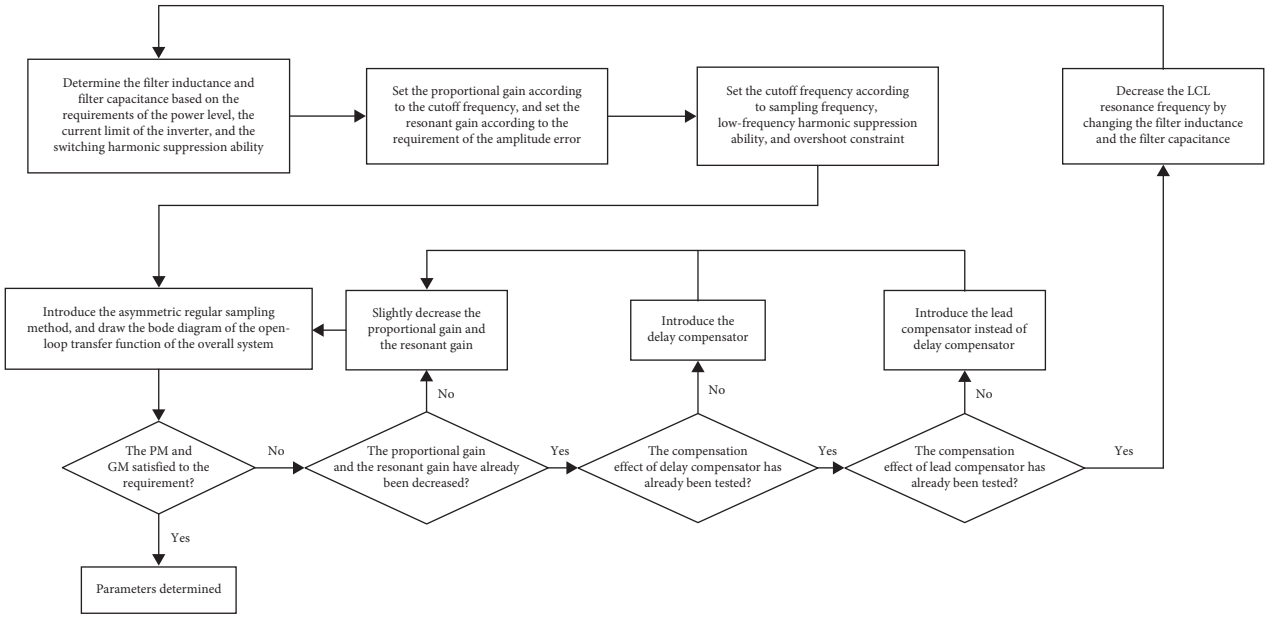

Figure 10: The flowchart of the step-by-step parameter design procedure.

Table 1: System simulation parameters.

Parameter/unit	Value
L_1/mH	2
L_2/mH	0.6
C/uF	4.7
f_s/kHz	10
f_0/Hz	50
U_{dc}/V	750
u_g/V	220
ω_i	π
K_p	10
K_r	1000
α	0.17
T	$7.7e-3$

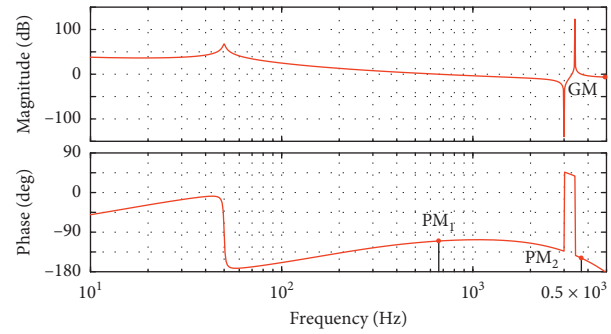

Figure 11: Bode diagram of the overall system.

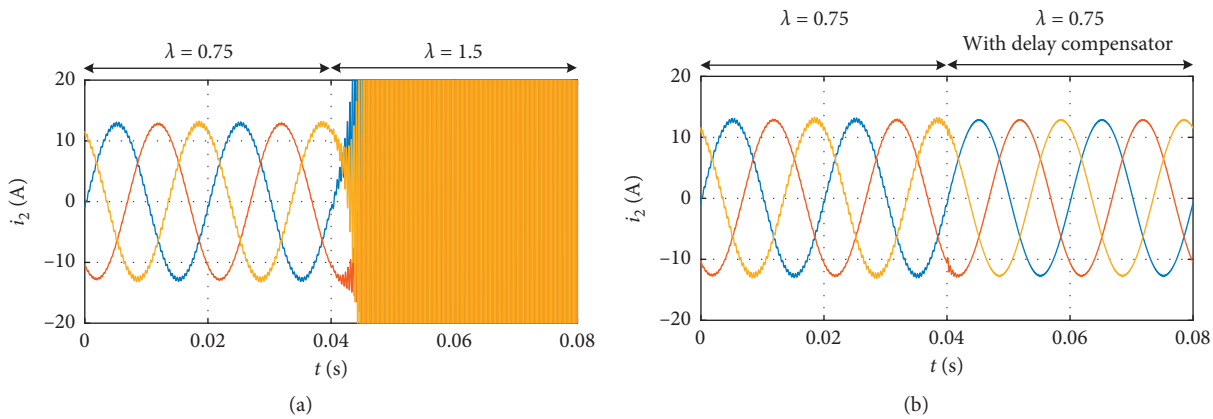

FIGURE 12: Simulation waveforms of the grid current when $f_{res} = 0.24\, f_s$ with different control strategies. (a) Only the asymmetric regular sampling method. (b) The proposed active damping method.

contains oscillation, indicating that the system stability margin is insufficient.

When further adopting the delay compensator, the current oscillation rapidly decays, indicating that the system stability margin has been increased, as shown in Figure 12(b). It is worth mentioning that, under this condition, there is little difference between the results of the delay compensator and the lead compensator (not shown in Figure 12). That means when the LCL resonance frequency f_{res} is relatively low, the system stability margin under the two methods has little difference, which is consistent with the analysis in Section 4.

When the filter capacitance C is regularly designed according to the design guidance, it equals 4.7 μF, as shown in Table 1. In this case, $f_{res} = 0.34\, f_s$, which is close to the critical frequency when the control delay decreases to $e^{-0.75sT_s}$, that is, around $f_s/3$. Figure 13 shows the simulated grid current for this case. With adopting the asymmetric regular sampling method, the control delay reduces to $e^{-0.75sT_s}$, and the system still cannot be stabilized, as shown in Figures 13(a) and 13(b).

The system can be stabilized when further adopting the delay compensator, as shown in Figure 13(a). However, the current still contains high resonance frequency harmonics, which makes the current cannot meet the requirements of total harmonic distortion (THD). Comparatively, when adopting the lead compensator, there is no obvious oscillation in the steady state, as shown in Figure 13(b). It indicates that, at a high level of the LCL resonance frequency, the system has a higher stability margin when adopting the lead compensator.

In addition, the robustness of the proposed active damping method is verified by shifting the LCL resonance frequency. Figure 14 shows the contrastive simulation results under the proposed method with the delay compensator and the lead compensator. The LCL resonance frequency reaches 0.4 f_s by decreasing the filter capacitor C to 75% designed value. The resonance frequency harmonics increase significantly with the delay compensator, as shown in Figure 14(a). Comparatively, with the implementation of the lead compensator, the resonance frequency harmonics increase slightly, as shown in Figure 14(b). Compared to the results shown in Figure 13, it indicates that the higher the resonance frequency, the greater the advantage of the lead compensator, verifying the effectiveness of the analysis and the proposed method.

5.2. Experiment Results. In order to verify the above simulation results, a 6 kW three-phase grid-connected inverter prototype is built in the laboratory, as shown in Figure 15. In practice, the PR controller is decomposed into a direct integrator and a feedback integrator, and they are discretized with a forward difference and backward difference separately [10]. The delay compensator and the lead compensator are discretized with Tustin transform with prewarping to match the frequency responses at f_{res} [5]. Thus, the discretized controller can be implemented in a TI TMS320F28335 DSP. The main system parameters are shown in Table 1.

Figure 16(a) shows the grid current with the asymmetric regular sampling method adopted only. Though the grid current contains large oscillation, the system can be stabilized when the actual LCL resonance frequency f_{res} is close to the critical frequency. That is because of the damping effects of the parasitic series resistances of the filter inductor and filter capacitor in the prototype, leading to the difference between Figures 13 and 16(a).

Figures 16(b) and 16(c) show the grid current with the delay compensator and the lead compensator, respectively. The system stability margin is improved after introducing the delay compensator, and the oscillation rapidly decays, as shown in

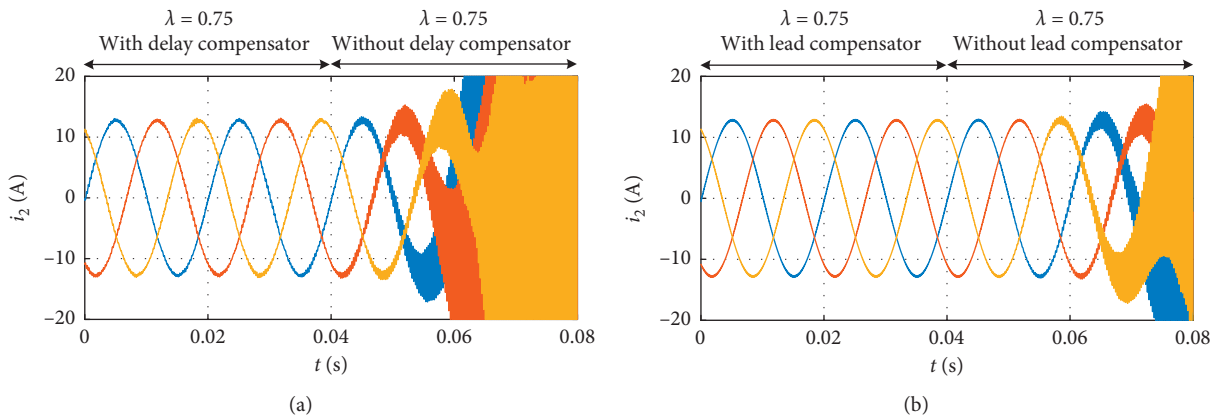

FIGURE 13: Simulation waveforms of the grid current when $f_{res} = 0.34\, f_s$ with the proposed active damping method. (a) Delay compensator. (b) Lead compensator.

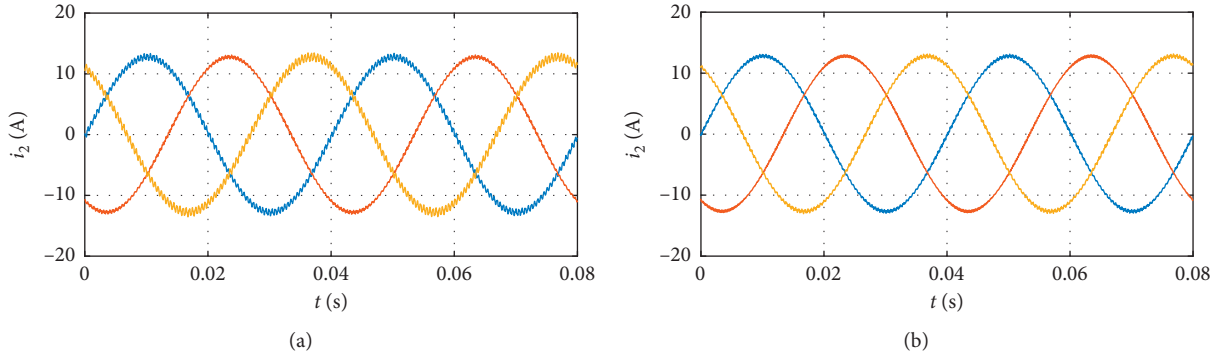

FIGURE 14: Simulation waveforms of the grid current with the proposed active damping method when C decreases. (a) Delay compensator. (b) Lead compensator.

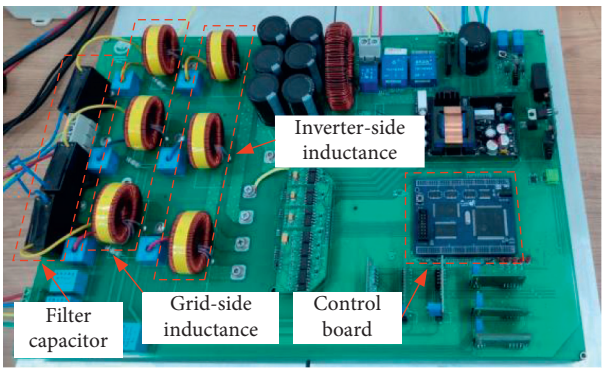

FIGURE 15: Photograph of the three-phase grid-connected inverter prototype.

Figure 16(b). But the resonance frequency harmonics still cannot meet the standards of THD. Comparatively, when adopting the lead compensator, there is no obvious oscillation in the steady state, as shown in Figure 16(c). It indicates that when the system has a high level of LCL resonance frequency, a higher stability margin can be achieved by adopting the lead compensator, verifying the effectiveness of the proposed method and the simulation results.

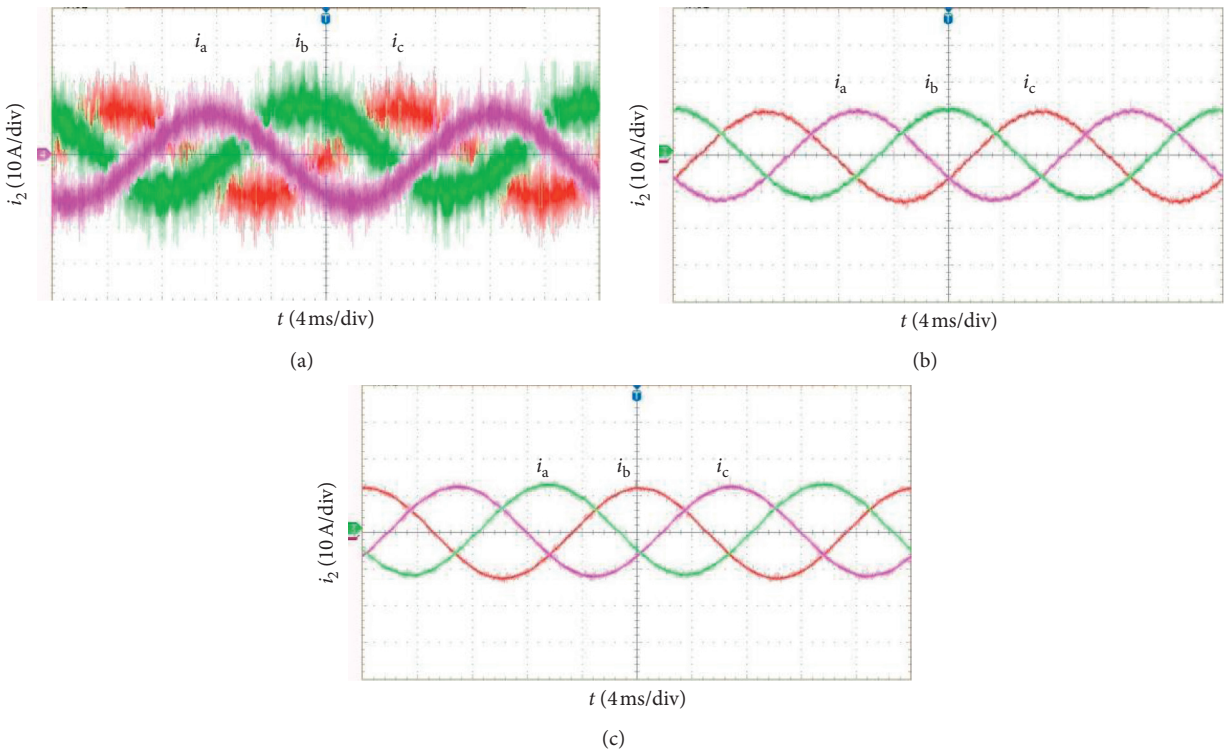

FIGURE 16: Experimental waveforms of the grid current when $f_{res} = 0.34\ f_s$ with different control strategies. (a) Only the asymmetric regular sampling method. (b) The proposed active damping method with the delay compensator. (c) The proposed active damping method with the lead compensator.

6. Conclusions

This paper studies active damping method for LCL-filtered three-phase grid-connected inverters based on SLICC. Through systematic impedance-based analyses, it has been shown that the control delay has changed the equivalent virtual resistance of the SLICC, and the critical frequency of the equivalent virtual resistance locates within the range of the LCL resonance frequency. To ensure the stability of the SLICC, an improved active damping method is proposed. The damping region is widened to $(0, f_s/2)$, which can cover all the possible resonance frequencies. A step-by-step design procedure considering the different resonance frequency range is also formulated. Particularly, the delay compensator may be unable to provide sufficient PM within the interval of high resonance frequency, and the lead compensator could further improve the system stability. The simulation and experimental results show the effectiveness of the proposed active damping method. To mimic the delay compensator more precisely when the control delay is equal to $e^{-0.75sT_s}$ is the future work.

Data Availability

The data that support the findings of this study are included within the article.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

Acknowledgments

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