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Research Article

Neutral-Point Potential Balance Control Strategy on Three-Level Active Power Filters

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This paper presents a simplified strategy in neutral-point (NP) potential balance of the neutral-point-clamped (NPC) three-level three-wire active power filter (APF). By introducing a simplified carrier-based pulse width modulation (CB-PWM) strategy and analysing the occurrence mechanism of NP potential unbalance, we proposed a NP potential balancing control strategy based on the simplified strategy. With this strategy, the NP current in a sampling period can be calculated through the detection of compensating current of APF. The three phase's duration time of reference voltage can also be computed through detecting the voltage fluctuation of upper and lower capacitors accurately, according to the law of charge conservation. Experiment results show that this proposed approach with simplified computation can effectively achieve NP potential balance.

1. Introduction

As the power electronics technology develops fast in recent decades, much attention has been given to the study of power grid optimization [1]. The active power filter (APF) is an important device for harmonic suppression in optimizing power quality, which can compensate the dynamic reactive power and harmonic distortion on the frequency and amplitude in real time [2]. In medium-voltage and high-power applications, multilevel topology has been widely adopted in APF for its numerous advantages, especially the higher DC-bus voltage utilization [3].

The neutral-point-clamped (NPC) three-level converter [4–6] is one of the preferred options in high-power medium-voltage applications for its simple topology and mature control technology. However, the neutral-point (NP) potential unbalance still remains as a major limitation.

Therefore, various modulation strategies have been proposed to solve the problem of NP potential unbalancing in NPC converters. These proposals can be classified into two categories according to their PWM modulation strategies [7]. The first category is space vector PWM (SVPWM) strategy [8–16], including nearest three space vector pulse width modulation (NTSVPWM) and virtual space vector pulse width modulation (VSVPWM). These strategies allocate the duration time of small vector to balance the NP potential. The second category adopts the carrier-based PWM [17–20] which injects zero-sequence voltage in three-phase reference voltage.

The balancing method presented in [13, 14] was based on the opposite effects of a pair of small vectors on neutral-point potential under the SVPWM algorithm. The neutral-point potential is balanced by selecting the positive or negative short vectors in a switching period. Such a method rearranges the time distribution of the short vectors and changes the switching sequence. Thus, the balance of neutral-point voltage is achieved but with prolonged switching transitions due to its complicated and intensive control algorithms.

In [17–20], researchers proposed a strategy that injected zero-sequence voltage in three-phase reference voltage based on carrier-based PWM. However, the NP potential balancing of this strategy requires too complex calculation of zero-sequence voltage. The NP potential control algorithm based on SVPWM was applied in the three-level shunt APF system in [21], which, however, was only simulated in modelling but not verified with experiments.

The present research, aiming to optimize the NP potential balancing, introduces a novel simplified CB-PWM strategy with NP potential balance control to the three-level

three-wire APF system. Compared to the traditional CB-PWM, this strategy is more simplified and can significantly reduce the execution time, compensate the harmonic current, and effectively solve the NP potential offset problem. The effectiveness of this novel control strategy is verified with experiments.

2. Simplified CB-PWM Strategy

2.1. Principle of NPC Three-Level Three-Wire APF. A structural schematic diagram of typical NPC three-level three-wire APF is shown in Figure 1. The NPC three-level converter is connected to power grid through a reactor L_s. C_1 and C_2 are DC-bus capacitors of three-level converter, respectively.

The control diagram of the three-level three-wire APF system is shown in Figure 2. The system consists of current loop with a PI (proportional integral) regulator, a voltage loop with a PR (proportional resonant) regulator and a NP potential balance controller, and grid voltage and load current detection. Besides, simplified CB-PWM strategy for the NPC three-level converter is adopted to generate PWM signals to drive the NPC converter.

Compared to the traditional converter system, the APF system is more complex because it involves an extra step of harmonic detecting including the low-pass filter and the current controller with the PR regulator. The precision of the compensation will be determined by the execution speed of the algorithm.

2.2. Principle of Simplified CB-PWM Strategy. Structural schematic diagram of NPC three-level APF is shown in Figure 1. Each phase of the converter has three switching states as P, O, and N, signifying that the output terminal voltages are U_{dc}, 0, and $-U_{\mathrm{dc}}$, respectively. Table 1 presents the terminal voltage of each phase and switching states of each bridge.

The reference voltage space vector $\overrightarrow{V}_{ref}$ is then introduced in Figure 3. It can be calculated with the terminal voltage of three phases, V_{a}, V_{b}, and V_{c}:

$$\overrightarrow{V}_{ref} = \frac{2}{3}\left(V_a + V_b e^{j(2/3)\pi} + V_c e^{-j(2/3)\pi}\right). \tag{1}$$

Figure 3 shows voltage space vector diagram of the NPC three-level converter. There are 27 switching states on the three-level converter, which means it has a much larger quantity of basic vectors than the two-level converter. As to traditional SVPWM schemes, it takes over long time to select sectors (or triangle region) and calculate the space vector duration. The researchers, based on the two aspects above, propose a simplified CB-PWM strategy, which is applied in a three-level three-wire APF system to reduce the amount of computation greatly.

Figure 3 shows that all vectors are divided into 6 sectors. An easier way for selecting sectors in space voltage vectors is proposed, and the principles that it follows is shown in Table 2.

u_{A_ref}, u_{B_ref}, and u_{C_ref} are reference voltages of three phases. For example, reference voltage space vector $\overrightarrow{V}^{*}_{ref}$ locates in sector I ($S = 1$), which means $u_{A\_ref} > 0$, $u_{B\_ref} < 0$, and $u_{C\_ref} < 0$, as shown in Figure 4. Reference voltage space vector $\overrightarrow{V}_{ref}$ can be obtained from $\overrightarrow{V}_1$ (including $\overrightarrow{V}_{1P}$ and $\overrightarrow{V}_{1N}$), $\overrightarrow{V}_7$, and $\overrightarrow{V}_8$.

Based on traditional voltage-second balance, it can be expressed that

$$\begin{cases} \overrightarrow{V}_{ref} \cdot T_s = \overrightarrow{V}_{1P} \cdot T_{1P} + \overrightarrow{V}_7 \cdot T_7 + \overrightarrow{V}_8 \cdot T_8 + \overrightarrow{V}_{1N} \cdot T_{1N}, \\ T_s = T_{1P} + T_7 + T_8 + T_{1N}. \end{cases} \tag{2}$$

According to simplified CB-PWM strategy, reference voltages of three phases can be obtained:

$$\begin{cases} u_{A\_ref} \cdot T_s = \int_0^{T_s} u_{AO}(t)dt, \\ u_{B\_ref} \cdot T_s = \int_0^{T_s} u_{BO}(t)dt, \\ u_{C\_ref} \cdot T_s = \int_0^{T_s} u_{CO}(t)dt. \end{cases} \tag{3}$$

Equation (3) and Figure 3 show that when $u_{A\_ref} > 0$, terminal voltage of phase A u_{AO} consists of U_{dc} and 0 (indicated by state P and O); when $u_{B\_ref} < 0$, terminal voltage of phase B u_{BO} consists of $-U_{\mathrm{dc}}$ and 0 (indicated by state N and O). Similarly, terminal voltage of phase C u_{CO} consists of $-U_{\mathrm{dc}}$ and 0 (indicated by state N and O).

Therefore, the phases' duration time could be obtained as follows:

$$\begin{cases} T_A = \dfrac{\left(u_{A\_ref} \cdot T_s\right)}{U_{dc}}, \\ T_B = T_s + \dfrac{\left(u_{B\_ref} \cdot T_s\right)}{U_{dc}}, \\ T_C = T_s + \dfrac{\left(u_{C\_ref} \cdot T_s\right)}{U_{dc}}. \end{cases} \tag{4}$$

According to (4), the switching sequence in Sector I is shown in Figure 5.

Thus, three phase's duration time of reference voltage can be concluded as

$$\begin{cases} T_X = \dfrac{U_{X\_ref} T_s}{U_{dc}} \left(u_{X\_ref} \geq 0\right) \\ T_X = T_s + \dfrac{U_{X\_ref} T_s}{U_{dc}} \left(u_{X\_ref} < 0\right) \end{cases}, \quad (X = A, B, C). \tag{5}$$

3. Analysis of Neutral-Point Potential Offset and the Balancing Strategy

3.1. Analysis on Neutral-Point Potential Offset of NPC Three-Level Three-Wire APF. As shown in Figure 3, there are 27 switching states and 19 space vectors in the space vector

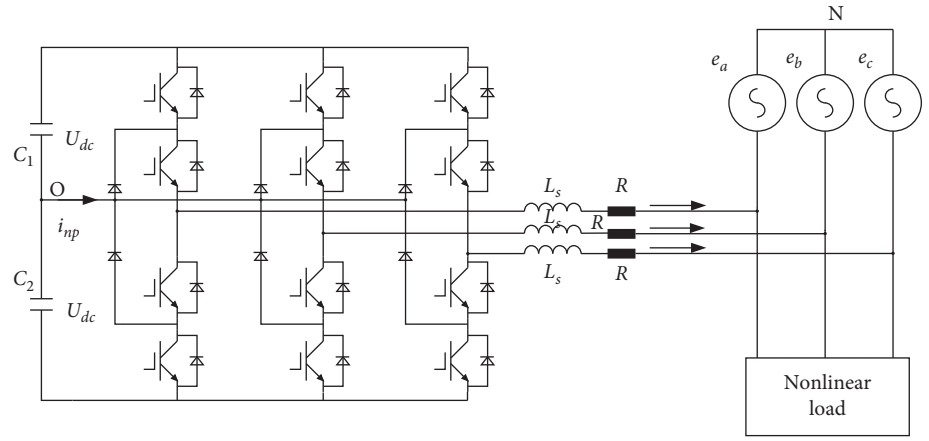


Figure 1: Structural schematic diagram of three-level APF.

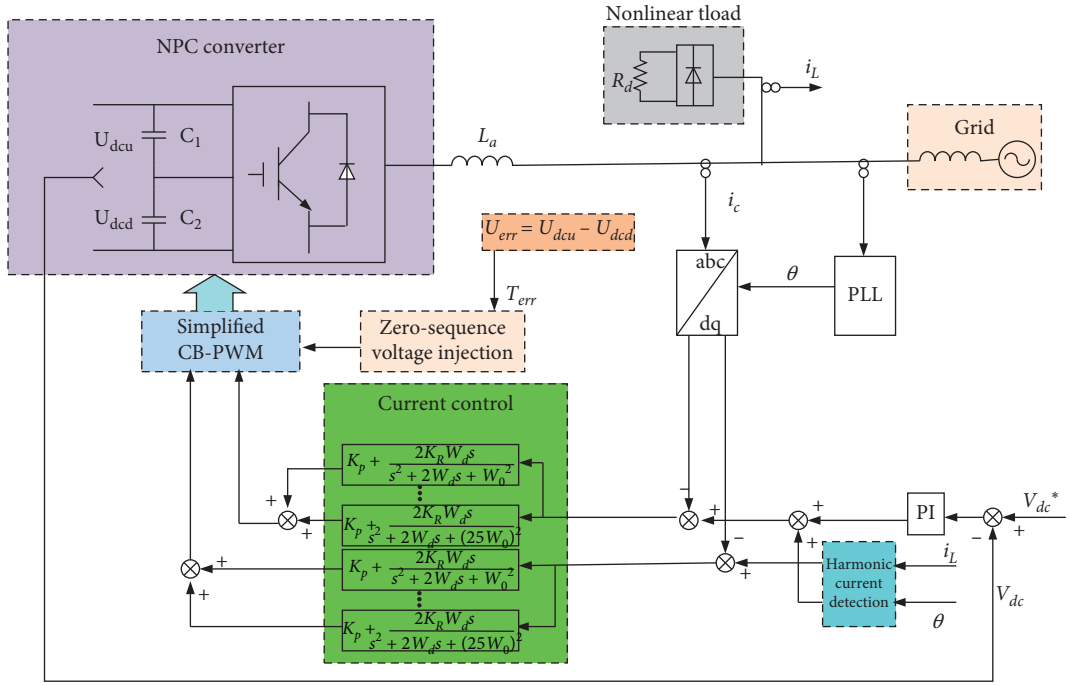


Figure 2: Block diagram of the APF system.

Table 1: Switching states of the three-level NPC converter ($X = A$, B, C).

SX1	SX2	SX3	SX4	Terminal voltage	Switching state
ON	ON	OFF	OFF	U_{dc}	P
OFF	ON	ON	OFF	0	O
OFF	OFF	ON	ON	$-U_{dc}$	N

diagram of the NPC three-level converter. These vectors can be divided into four different types, zero vector, small vector, medium vector, and large vector, based on the different influences of neutral-point potential. The detail will be discussed separately in the following.

When zero vector works, such as PPP, the three-phase load is connected to the positive terminal of DC-bus directly. As shown in Figure 6, no current flows into/out of the neutral point O. Therefore, the zero vector does not have any effect on the neutral-point potential.

As shown in Figure 7, when the large vector (PNN) works, the three-phase load is connected to the positive and negative terminal of DC-bus, respectively. It can be seen that no current flows into/out of the neutral-point O. So, the large vector does not influence the neutral-point potential, either.

Figures 8 and 9 show that when the small or medium vector works, the neutral point O is connected to the load. There is some current flowing into/out of the neutral point O, which will affect the neutral-point potential. The small or the medium vector always have the switching state "O," so there is at least one phase load connected to the neutral point. In such a circumstance, the phase current is equal to the current which flows into/out of the neutral point O. There is the neutral-point potential offset because of the neutral-point current.

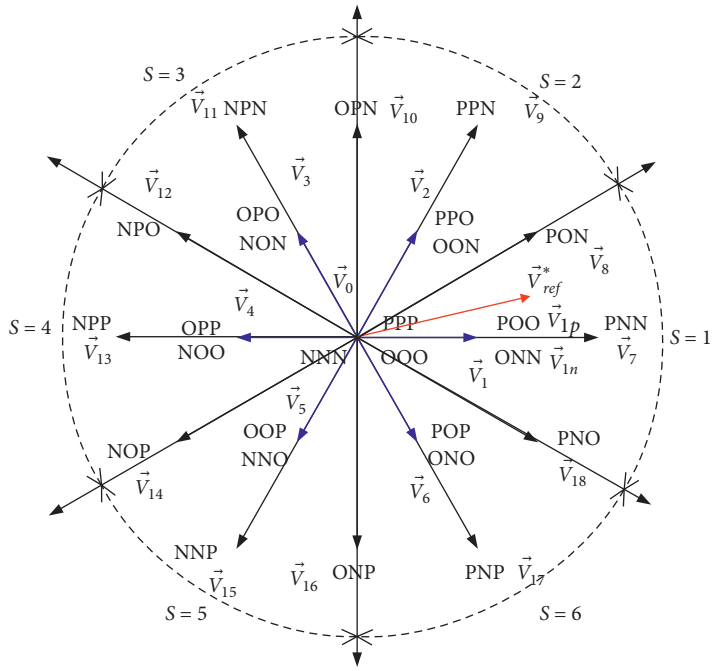


Figure 3: Voltage space vector diagram of the NPC three-level converter.

Table 2: Principles of sector selection.

u_{A_ref}	u_{B_ref}	u_{C_ref}	S
>0	<0	<0	1
>0	>0	<0	2
<0	>0	<0	3
<0	>0	>0	4
<0	<0	>0	5
>0	<0	>0	6

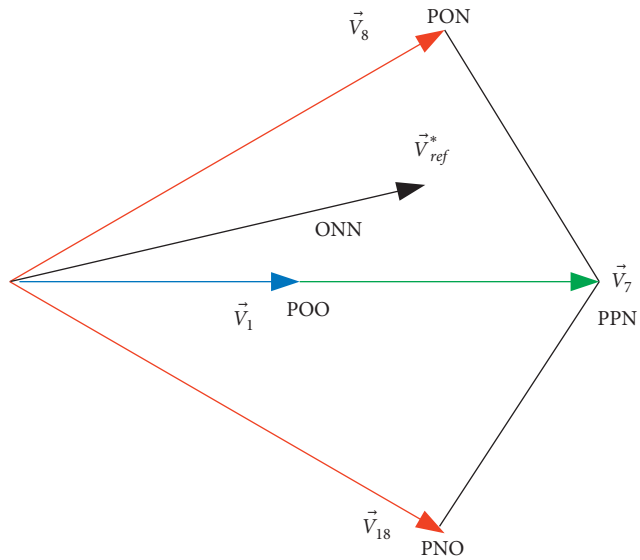


Figure 4: $\vec{V}^*_{ref}$ locating in sector I.

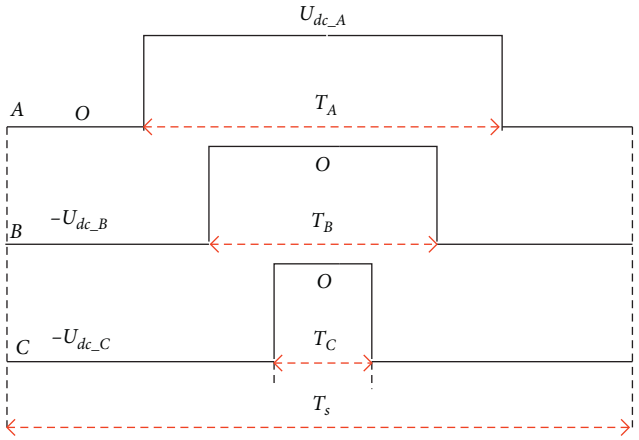


Figure 5: Diagram of PWM waveform in Sector I.

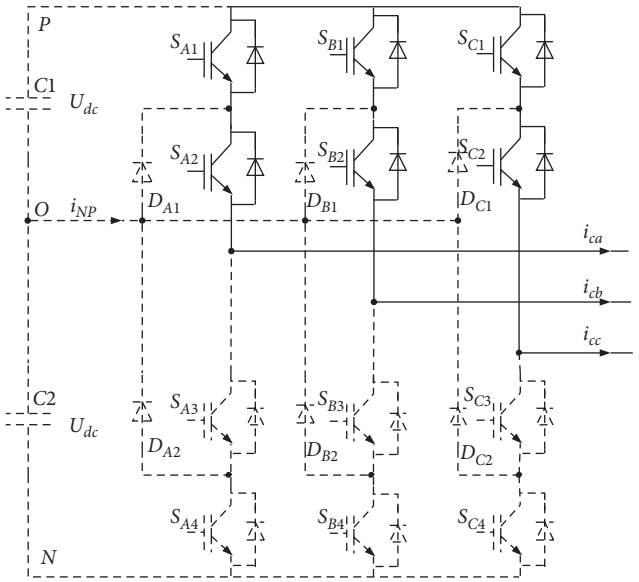


Figure 6: Zero vector (PPP).

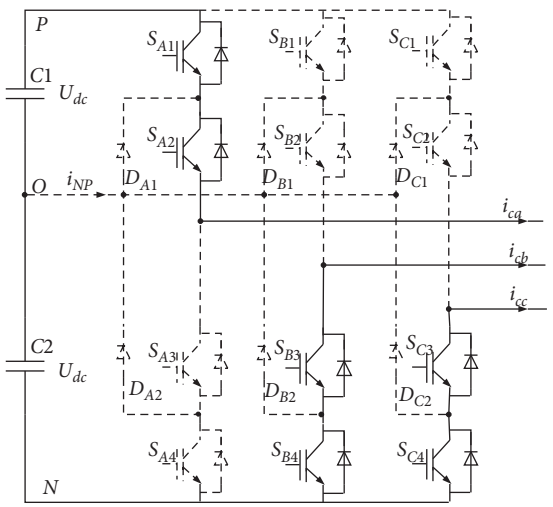


Figure 7: Large vector (PNN).

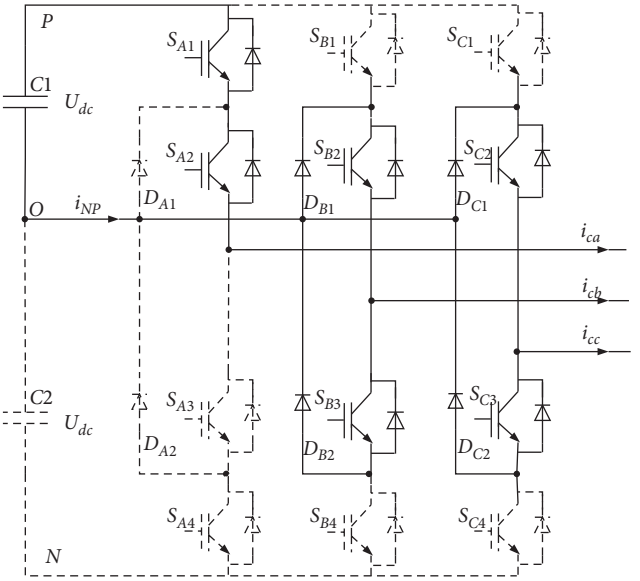


Figure 8: Small vector (POO).

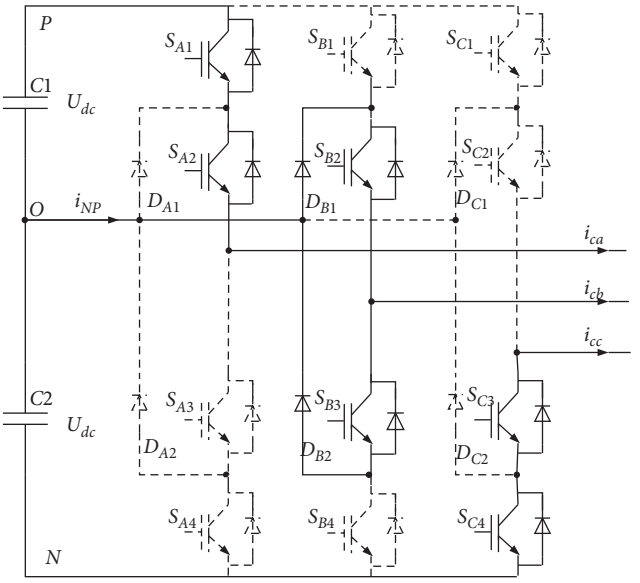


Figure 9: Medium vector (PON).

Table 3 shows the neutral-point current corresponding to different vectors. It can be inferred that small vectors appear in pairs, but the two have opposite effects on neutral-point potential. The PWM waveform can be generated by the seven-stage modulation method by combining the original PWM waveform in Figure 5 and the data in Table 3, as shown in Figure 10.

When the sampling period is small enough, the current of phase current can be considered as constant in a sampling period. According to Figure 10, the average value of neutral-point current i_{NP} can be calculated as

Table 3: Neutral-point current corresponding to different vectors.

Positive small vectors	i_{NP}	Negative small vectors	i_{NP}	Medium vectors	i_{NP}
ONN	i_a	POO	$-i_a$	OPN	i_a
NON	i_b	OPO	$-i_b$	PON	i_b
NNO	i_c	OOP	$-i_c$	PNO	i_c
OPP	i_a	NOO	$-i_a$	ONP	i_a
POP	i_b	ONO	$-i_b$	NOP	i_b
PPO	i_c	OON	$-i_c$	NPO	i_c

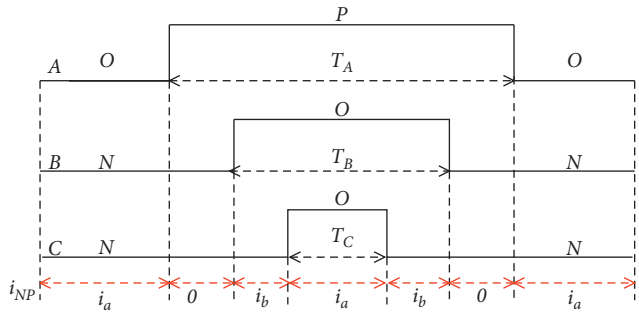


Figure 10: Neutral-point current in a switching period.

$$\begin{cases} i_{\mathrm{NP}} = \dfrac{i_a \cdot (T_s - T_A) + i_b \cdot (T_B - T_C) + (-i_a) \cdot T_C}{T_s}, \\ i_a + i_b + i_c = 0. \end{cases} \tag{6}$$

By solving (6), the neutral-point current i_{NP} can be obtained as

$$i_{\mathrm{NP}} = \frac{i_a \cdot (T_s - T_A) + i_b \cdot T_B + i_c \cdot T_C}{T_s}. \tag{7}$$

3.2. The Neutral-Point Potential Balancing Strategy. In traditional CB-PWM, zero-sequence voltage is injected into three-phase reference voltage to balance the neutral-point potential, which requires complicated calculation. The present study proposes a novel strategy, aiming to make the calculation convenient and simpler.

Compare to the injection of zero-sequence component, we add the common time T_{err} to three phase's duration time T_X ($X = A, B, C$) to balance the neutral-point potential offset. After T_{err} is added, the new three phase's duration time can be obtained as

$$\begin{cases} T_A' = T_A + T_{\mathrm{err}}, \\ T_B' = T_B + T_{\mathrm{err}}, \\ T_C' = T_C + T_{\mathrm{err}}. \end{cases} \tag{8}$$

Thus, the new neutral-point current is

$$i_{\mathrm{NP}}' = \frac{i_A \cdot [T_s - T_A'] + i_B \cdot T_B' + i_C \cdot T_C'}{T_s} = \frac{i_A \cdot [T_s - (T_A + T_{\mathrm{err}})] + i_B \cdot (T_B + T_{\mathrm{err}}) + i_C \cdot (T_C + T_{\mathrm{err}})}{T_s} = i_{NP} - \frac{2i_A}{T_s} \cdot T_{\mathrm{err}}. \tag{9}$$

Based on the principle of charge conservation, the following equation can be obtained:

$$i_{\mathrm{NP}}' \cdot T_s = U_{err} \cdot C, \tag{10}$$

where $U_{\mathrm{err}} = U_{\mathrm{dcd}} - U_{\mathrm{dcu}}$ is the voltage difference between lower and upper DC-link capacitors, U_{dcu} and U_{dcd} the upper and lower DC-link capacitor voltage, respectively, and $C = C_1 = C_2$ is the capacitance of DC-link. Thus, T_{err} can be derived from (9) and (10) directly:

$$T_{\mathrm{err}} = \frac{i_{\mathrm{NP}} \cdot T_s - C \cdot U_{\mathrm{err}}}{2 \cdot i_A}. \tag{11}$$

Equation (9) shows that T_{err} can affect the neutral-point current and can adjust the neutral-point potential. When i_{NP}' is positive, the neutral-point potential will decrease. Thus, T_{err} can be modified by equation (11) to suppress the neutral-point potential offset in theory. The process of modification is shown in Figure 11.

When $\vec{V}_{ref}$ is located in the other sectors, T_{err} can be expressed as follows:

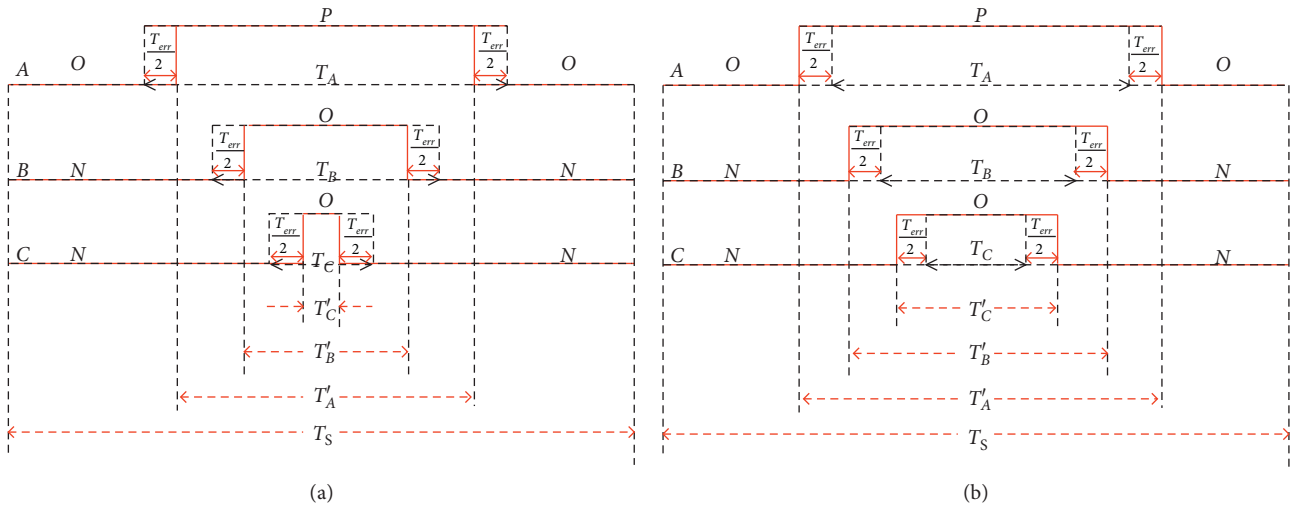


Figure 11: Procedure of duration time modification of PWM waveforms. (a) Neutral-point potential to be decreased. (b) Neutral-point potential to be increased.

$$T_{\text{err}} = \begin{cases} \dfrac{i_{\text{NP}} \cdot T_s - C \cdot U_{\text{err}}}{2 \cdot i_A}, & S = 1, \\ -\dfrac{i_{\text{NP}} \cdot T_s - C \cdot U_{\text{err}}}{2 \cdot i_C}, & S = 2, \\ \dfrac{i_{\text{NP}} \cdot T_s - C \cdot U_{\text{err}}}{2 \cdot i_B}, & S = 3, \\ -\dfrac{i_{\text{NP}} \cdot T_s - C \cdot U_{\text{err}}}{2 \cdot i_A}, & S = 4, \\ \dfrac{i_{NP} \cdot T_s - C \cdot U_{err}}{2 \cdot i_C}, & S = 5, \\ -\dfrac{i_{\text{NP}} \cdot T_s - C \cdot U_{\text{err}}}{2 \cdot i_B}, & S = 6, \end{cases} \tag{12}$$

where S is the sector number. Figure 11 shows that the range of common time T_{err} should follow

$$\begin{cases} T_{\text{err}} \le T_s - \max(T_A, T_B, T_C), & (\text{when } T_{\text{err}} \ge 0), \\ \text{abs}(T_{\text{err}}) \le \min(T_A, T_B, T_C), & (\text{when } T_{\text{err}} < 0). \end{cases} \tag{13}$$

4. Experimental Verification

In order to verify the effectiveness of the proposed balancing strategy, experiments for NPC three-level three-wire APF are conducted. The parameters of the experimental platform are listed in Table 4.

Figure 12 shows the photograph of the experiment equipment including AC supply from the grid, nonlinear load, sensor board connected to controller board, and NPC three-level converter board.

Table 4: Parameters of the experimental platform.

Parameters	Value
Phase voltage (V_s)	110 V (RMS)
Frequency of phase voltage	50 Hz
DC-link voltage ($2U_{\text{dc}}$)	400 V
DC-link capacitance (C_1, C_2)	1350 μF
Output inductor (L_s)	4 mH
Switching frequency (f_s)	10 kHz
Load resistance (R_d)	30 Ω

Figure 13 shows some waveforms before and after compensation by APF. The three-phase uncontrolled rectifier bridge connecting serially with a 30 Ω resistor is selected as the typical nonlinear load. The typical load current waveforms can be found from Figure 13(a). Figure 13(b) shows the load current, the grid current after compensation, and the reference current and output current of APF, respectively. The grid current, compared with the distorted load current, is approximately sinusoidal and symmetrical after the compensation. The same conclusion can be drawn after the THD analysis. The THD of load current reaches up to maximum 24.01%. However, the THD of grid-side current sharply falls to 4.5% because of the compensation. Meanwhile, the actual output compensating current is nearly the same as the reference current, suggesting that APF is with good performance. The experiments and analysis above have verified that the three-level three-wire NPC APF has significant positive performance on improving the quality of power grid.

Figure 14 shows the waveforms of upper and lower DC-link voltage. It can be seen that when the neutral-point potential control strategy is not working, the upper and lower voltage $U_{\text{dcu}}/U_{\text{dcd}}$ diverge in opposite directions. Then, the proposed neutral-point potential scheme starts working. It shows that the differential value between upper and lower DC-link voltage is less than 2 V, suggesting that the neutral-point potential offset is suppressed effectively.

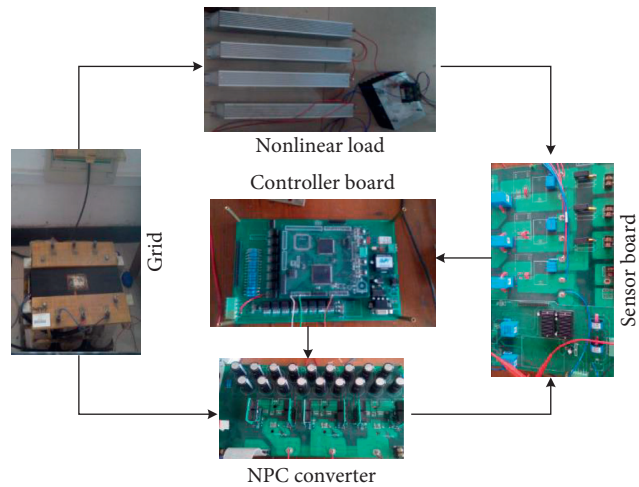
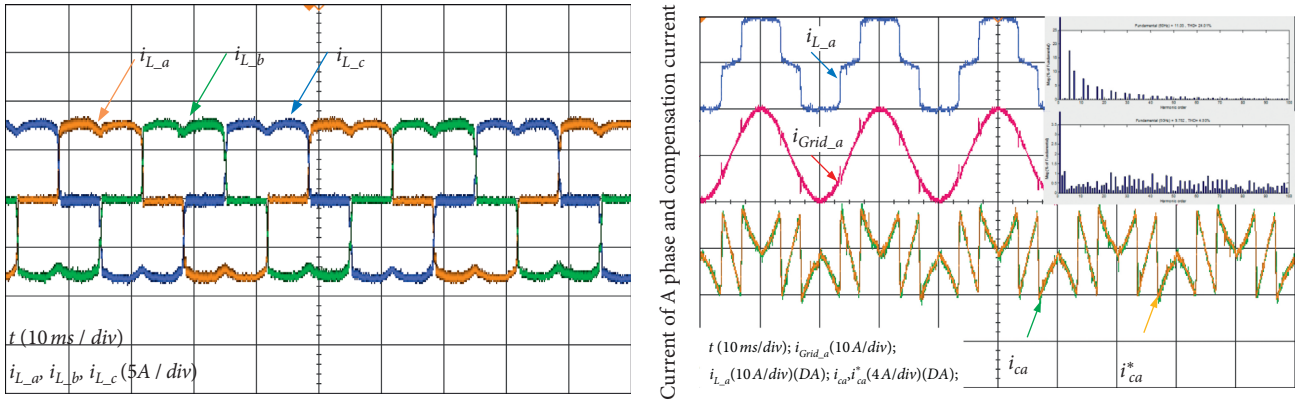


Figure 12: Photograph of the experimental platform.



(a) (b)

Figure 13: Waveforms of some currents. (a) Load current before compensation. (b) Harmonic reference current.

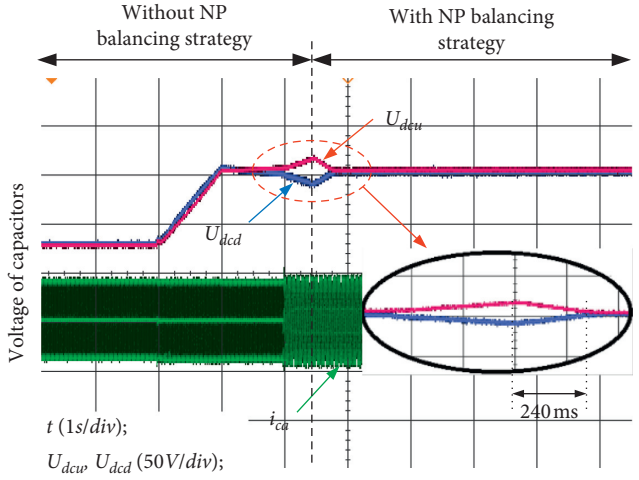


Figure 14: Waveforms of upper and lower DC-link voltage.

The proposed scheme and conventional SVPWM were both programmed on the same TMS320F28335 DSP board to check which algorithm can simplify the calculation. Meanwhile, the same code style and composer configuration were adopted, and all extra optimal measures during the programming were strictly controlled. The results of the experiments showed that it only took DSP 6.4 μs in the proposed scheme to finish the whole calculation, while in conventional SVPWM, it was 9.6 μs, indicating a significant simplification.

5. Conclusions

The present paper, based on a new voltage-second rule for the three-level converter on three-phase three-wire APF systems, proposes a novel simplified neutral-point balancing scheme and verifies its performance in balancing NP potential. Firstly, the duration time of three phases can be calculated directly with this scheme to avoid the complicated selection of space vector sectors by conventional SVPWM. The calculations in the proposed strategy cover multiplication, addition, and few amounts of division. Compared with the large quantity of divisions, even trigonometry operations in conventional SVPWM, the proposed strategy represents a simplified algorithm when applied in the DSP plant.

Secondly, this proposed strategy reconstructs the switching sequence of every phase by modifying the duration time. Its operation is significantly simpler than the traditional method of zero-sequence voltage injection. The experiments in Section 4 have verified the feasibility and effectiveness of the proposed strategy.

Data Availability

The raw/processed data required to reproduce these findings cannot be shared at this time as the data also forms part of an ongoing study.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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References

[1] C. Eyisi, A. S. Al-Sumaiti, K. Turitsyn, and Q. Li, "Mathematical models for optimization of grid-integrated energy storage systems: a review," in *Proceedings of the 2019 North American Power Symposium (NAPS)*, pp. 1–5, Wichita, KS, USA, October 2019.

[2] C. Liu, Y. He, K. Dai, and Y. Kang, "Industrial power distribution system harmonic resonance problem and solution with shunt active power filter," in *Proceedings of the IECON 2017-43rd Annual Conference of the IEEE Industrial Electronics Society*, pp. 1243–1248, Beijing, China, November 2017.

[3] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Ge Baoming, "Medium-voltage multilevel converters-state of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010.

[4] Z. Hao, X. Wang, and X. Cao, "Harmonic control for variable-frequency aviation power system based on three-level NPC converter," *IEEE Access*, vol. 8, pp. 132775–132785, 2020.

[5] A. Pal and K. Basu, "A three-phase three-level isolated DC-AC converter with line frequency unfolding," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11758–11769, 2020.

[6] Z. Xia, Z. Liu, and J. M. Guerrero, "Multi-objective optimal model predictive control for three-level ANPC grid-connected inverter," *IEEE Access*, vol. 8, pp. 59590–59598, 2020.

[7] B. Zhang, Q. Ge, L. Tan, X. Wang, Y. Yu, and J. Liu, "A New PWM scheme for loss balancing and neutral-point voltage balancing in three-level active NPC converter," in *Proceedings of the 2015 IEEE 10th Conference on Industrial Electronics and Applications (ICIEA)*, pp. 1128–1133, Auckland, New Zealand, June 2015.

[8] G. Liu, L. Qu, W. Zhao, Q. Chen, and Y. Xie, "Comparison of two SVPWM control strategies of five-phase fault-tolerant permanent-magnet motor," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6621–6630, 2016.

[9] R. Stala, "A natural DC-link voltage balancing of diode-clamped inverters in parallel systems," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 5008–5018, 2013.

[10] S. Wang, J. Ma, B. Liu, N. Jiao, T. Liu, and Y. Wang, "Unified SVPWM algorithm and optimization for single-phase three-level NPC converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7702–7712, 2020.

[11] F. Bu, T. Pu, W. Huang, and L. Zhu, "Performance and evaluation of five-phase dual random SVPWM strategy with optimized probability density function," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3323–3332, 2019.

[12] A. Gopinath, "A triangular 3-D coordinate system for multilevel SVPWM generation," *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 4061–4070, 2020.

[13] H. Lin, Z. Shu, J. Yao et al., "A simplified 3-D NLM-based SVPWM technique with voltage-balancing capability for 3LNPC cascaded multilevel converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3506–3518, 2020.

[14] V. Janaki Ramaiah and S. Keerthipati, "Hybrid PWM scheme for Pole-phase modulation induction motor drive using carrier-based hexagonal and octadecagonal SVPWM," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 9, pp. 7312–7320, 2020.

[15] L. Gu and K. Jin, "A three-phase isolated bidirectional AC/DC converter and its modified SVPWM algorithm," *Journal of Power Electronics*, vol. 30, no. 10, pp. 989–999, 2019.

[16] B. Sakthisudhursun, J. K. Pandit, and M. V. Aware, "Simplified three-level five-phase SVPWM," *IEEE Transactions on Power Electronics*, vol. 19, no. 7, pp. 2429–2436, 2016.

[17] J.-S. Lee and K.-B. Lee, "Carrier-based discontinuous PWM method for vienna rectifiers," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 2896–2900, 2015.

[18] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 642–651, 2012.

[19] C. Yongdong Li and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2262–2271, 2010.

[20] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 305–314, 2009.

[21] T. Abdelkrim, E. M. Berkouk, A. Benkhelifa, K. Benamrane, and T. Benslimane, ""Neutral point potential balancing algorithm for autonomous three-level shunt active power filter" journal of electrical and control engineering," *IEEE*, vol. 5, no. 2, pp. 20–26, 2012.