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Research Article

Design of Hybrid Posicast Control for Super-Lift Luo Converter

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This article investigates a new Hybrid Posicast Controller (HPC) for Fundamental Positive Output Super-Lift Luo Converter (FPOSLLC) in Continuous Conduction Mode (CCM). It is a feedforward controller that decreases the flippantly damped plant overshoot in the step result. However, because of fluctuations in the natural frequency, the traditional controller technique is sensitive. In this article, a novel HPC is built to alleviate the FPOSLLC's undesired sensitivity and load voltage control. HPC has a feedback loop and a posicast structure. The main design function of posicast is its independent computational time delay. By creating a MATLAB/Simulink model, the FPOSLLC implementation with HPC may be verified under various operating conditions. In comparison to standard PID control, the results of the new HPC have produced little noise in the control signal.

1. Introduction

Luo Converters (LCs) are a type of DC-DC converter that converts a constant DC source voltage to a variable DC load voltage. LCs are more well known in a variety of applications, including renewable energy sources, DC microgrids, electric vehicle battery charging, medical instruments, and FACTS devices, among others. The LCs are nonlinear lightly damped dynamic systems with load limitations, storage components, and an operating duty cycle that explain their performance. As a result, LC controller design is more complicated and puzzling [1]. As a result, the Fundamental Positive Output Super-Lift Luo Converter (FPOSLLC) is chosen for controller design in this article. A FPOSLLC is a type of LC topology. In [2, 3], a control with posicast fundamental is thoroughly explained. It is a feedforward controller for flippantly damped plants that eliminates the oscillatory response. However, the fundamental problem with this control strategy is its sensitivity to plant ambiguity. If the plant's sensitivity is eliminated, the posicast with feedback loop technique is more worthwhile. Support for posicast in a feedback loop solves this problem [4]. The verification of nonlinear controllers for LC has been extensively documented [5]. The developed controller, on the other hand, produced zero overshoot and required only 0.014 s to settle through the transient state for the same converter. The operation of an FPOSLLC in CCM with a Fuzzy Logic Controller (FLC) and a Sliding Mode Controller (SMC) is described in detail [6]. Despite this, in the transient operating state, this FPOSLLC with controller has produced a settling time of 0.006 s.

A study of competent LCs in an open loop for a DC microgrid has been published [7]. However, it is clear that the load voltage of this model caused large overshoots and required a long time to settle. FPOSLLC with classical Proportional Integral (PI) controller is discussed [8]. During the transient stage, the PI control for the same model exhibited huge overshoots in line/load changes and needed a long settling time of 0.038 s. The results of a wide-ranging examination of numerous factors for FPOSLLC are well described [9]. The converter was run in open-loop mode in this article. The design of an LC with a stepping-down converter for EV is described in depth [10]. FPOSLLC performance under multitudinous control has been studied [11].

According to this report, the designed controller resulted in massive overshoots and a protracted settling time. Modified LCs are considered in terms of modelling and adaptive control [12]. The main issue with this control for LCs, however, is that it has resulted in noise in the control signals and enormous ripple factors [13]. There is a lot of information about the LC with power factor correction and output voltage regulation. However, the intended system has produced a THD of 3.15 percent, a long settling period, greater in-rush source current, and massive overshoots in the startup zone. The usage of a PV-fed LC for wiper motors has been documented [14]. Nonetheless, the LC has resulted in massive overshoots in the startup region. Various researchers have examined how traditional PID control for many power converters may necessitate unnecessary configuration to achieve good transient and steady-state performance. Extra switching noise and two stages of gains have resulted from these adjustments. A real-time digital PID implementation for a DC-DC power converter is also more complicated. The features of design of posicast controller for DC-DC power converter has excellent transient/steady-state response, proficient damping of resonant characteristics, easy computation of controller parameters, simple implementation in digital mode, frequency responses of posicast element innately minimized high frequency noise, and elimination of additional controller gain over PID control. Modelling of modified ultra-lift LC is addressed [15]. The use of modelling and SMC for LCs has been well documented [16]. However, according to this paper, the planned model was run at a variable frequency, which resulted in a significant quantity of noise in the control signal. FLC with fused LC-based renewable energy system is recorded [17]. From this article, converter with designed controller has generated more steady-state error along with overshoots. Voltage mode control for positive output elementary LC has been presented [18]. However, the developed control for same converter has resulted in more peak overshoots of 3 V and took long settling time. Novel high gain DC-DC step converter for PV system is well addressed in [19]. However, the simulated output voltage of the designed converter has produced more startup peak overshoots of 20 V. The phase shifting soft switching-based resonant bidirectional DC-DC converter with current limiting has been discussed [20]. The structure of converter has more number of components and also generates the current/voltage stresses of the devices. The design of effective controller for KY boost converter has been discussed [21]. From this article, output voltage of the same model with control has produced long settling time during the start-up transient and steady state regions.

According to the aforementioned literature review, FPOSLLC with a new Hybrid Posicast Controller (HPC) is yet to be disclosed. As a result, this research introduces a novel HPC in CCM for FPOSLLC. The FPOSLLC's controller values are designed with the use of small-signal averaged modelling. The HPC with FPOSLLC is validated using a MATLAB/Simulink model under various operating conditions.

The following are the key contributions of this article:

(i) First, the mathematical modelling of FPOSLLC is obtained, and then the HPC/PID control for FPOSLLC is designed.

(ii) Second, simulation assessments for FPOSLLC over traditional PID control are performed using specially built HPC.

(iii) Finally, PID control is used to discuss the time-domain parameters of the proposed controller.

The organization of this article is as follows. Introduction, literature survey, and motivation of the proposed system are discussed in Section 1. The working and modelling of FPOSLLC are discussed in Section 2. Section 3 presents the detailed design procedure of a new HPC and PID control for FPOSLLC. Results and discussions of designed model with controllers are tested at different working states in Section 4. Section 5 draws the conclusions.

2. FPOSLLC Working and Modelling

2.1. Working of FPOSLLC. A FPOSLLC in CCM is represented in Figure 1(a) [1]. It involves V_{in} (C_1, C_o, L parasitic resistances (r_{c1}, r_c, r_L)), S (D_a, D_b), V_o, and R. Operation of this circuit is alienated into two states of working. In mode 1 (see Figure 1(a)), the switch S is turned on, and then, D_a is conduct/the D_b is a reverse bias, the L and the C_1 are energized to V_{in}. C_o stored energy released to R. i_L rises with V_{in}. During mode 2 operation (Figure 1(c)), S is open, and i_L falls with voltage ($2V_{in}-V_o$) to offer the energy to C_o and R via D_b. So, the ripple of i_L can be expressed as

$$\Delta_{iL} = \frac{V_{in}}{L}\delta T = \frac{V_o - 2V_{in}}{L}\delta T, \tag{1}$$

$$V_o = \frac{2-\delta}{1-\delta}V_{in}. \tag{2}$$

2.2. Modelling of FPOSLLC. The FPOSLLC consists of three storage components. Therefore, assign three state variables such as $i_L = x_1$, $V_{c1} = x_2$, and $V_o = x_3$, respectively. Then, state-space differential equations of the FPOSLLC in mode 1 can be engraved as [16].

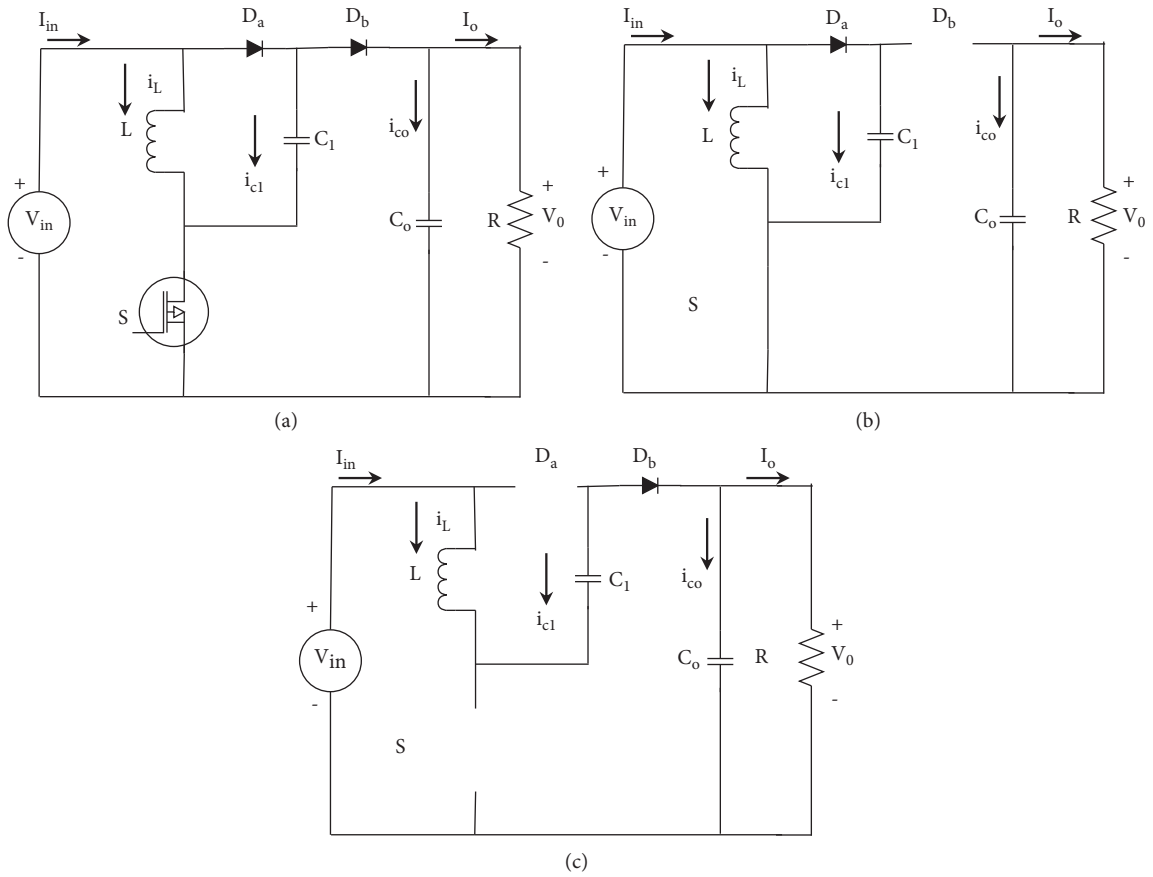

Figure 1: FPOSLLC circuit. (a) Topology. (b) Mode 1 working. (c) Mode 2 working.

$$\begin{cases} L\dfrac{di_L}{dt} = V_{in}, \\ C_1\dfrac{dV_{c1}}{dt} = -i_L - \dfrac{V_{c1}}{R_i} + \dfrac{V_{in}}{R_i}, \quad \text{SwitchON}, \\ C_o\dfrac{dV_o}{dt} = -\dfrac{V_o}{R}. \end{cases} \tag{3}$$

State-space differential equations of the FPOSLLC in mode 2 can be inscribed as [16]

$$\begin{cases} L\dfrac{di_L}{dt} = V_{in} + V_{c1} - V_o, \\ C_1\dfrac{dV_{c1}}{dt} = -i_L, \quad \text{SwitchOFF}, \\ C_o\dfrac{dV_o}{dt} = i_L - \dfrac{V_o}{R}. \end{cases} \tag{4}$$

The state-space average modelling of the FPOSLLC can be attained with support of the equations (1) and (2), and it is written as

$$\begin{bmatrix} \dot{i}_L \\ \dot{V}_{c1} \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} & -\frac{1-\delta}{L} \\ \frac{1}{C_1} & -\frac{\delta}{R_i C_1} & 0 \\ \frac{1-\delta}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_L \\ V_{c1} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1-\delta}{L} \\ \frac{\delta}{R_i C_1} \\ 0 \end{bmatrix} V_{in}, \quad (5)$$

$$Y = [001] \begin{bmatrix} i_L \\ V_{c1} \\ V_o \end{bmatrix},$$

$$A = A_{on}\delta + A_{off}(1-\delta),$$
$$B = B_{on}\delta + B_{off}(1-\delta), C = C_{on}\delta + C_{off}(1-\delta),$$
$$A = \begin{bmatrix} 0 & \frac{1}{L} & -\frac{1-\delta}{L} \\ \frac{1}{C_1} & -\frac{\delta}{R_i C_1} & 0 \\ \frac{1-\delta}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix}, B = \begin{bmatrix} \frac{1-\delta}{L} \\ \frac{\delta}{R_i C_1} \\ 0 \end{bmatrix},$$
$$C = [001], D = [000], \quad (6)$$

where A, B, C, and D are FPOSLLC state-space averaged matrices and δ is duty cycle.

The transfer function (small signal) model of FPOSLLC and eliminating R_i in (4), (5), (6), and (7) is expressed as

$$\frac{\hat{V}_o}{\hat{\delta}} = C[SI - A]^{-1}\left[[A_{on} - A_{off}]X + [B_{on} - B_{off}]V_{in}\right] + [C_{on} - C_{off}]X \quad (7)$$

$$G(s) = \frac{\hat{V}_o}{\hat{\delta}} = V_{in}\left(\frac{-sL\left(2 - \delta/(1-\delta)^2\right) + R}{\left(s^2 LRC_o + sL + R(1-\delta)^2\right)}\right).$$

2.3. Design Calculation of FPOSLLC Circuit Components. The FPOSLLC parameters are developed with the pursuing specifications as chronicled in Table 1.

The design calculation of the FPOSLLC is as follows [5].

(i) Take the δ for FPOSLLC operated in CCM, which is computed using

$$\frac{V_o}{V_{in}} = \frac{2-\delta}{1-\delta} - 1, \delta = 0.667. \quad (8)$$

(ii) Determine I_o by using

$$I_o = \frac{V_O}{R} = \frac{36}{50} = 0.72\text{A}. \quad (9)$$

Table 1: Parameters of FPOSLLC.

Parameter	Symbol	Value
Source voltage step input	V_{in}	12 V
Load voltage	V_o	36 V
Filter coil	L	100 μH
Filter capacitor	C_1 & C_o	30 μF
Operating frequency	f_s	100 kHz
Load resistance	R	50 Ω
Overshoot	λ	0.8
Natural period (damped)	T_d	2.44 ms
Duty cycle	δ	0.5

(iii) Evaluate P_o by using

$$P_o = V_O I_O$$
$$P_o = -36 * -0.72 \quad (10)$$
$$P_o = 25.92\text{W}.$$

(iv) Take the efficiency of the FPOSLLC as 91.8% for this study. Next, compute P_{in} using the efficiency value and

$$\eta = 91.79\%, P_{in} = P_o/\eta,$$
$$P_{in} = \frac{25.92}{0.9179}, P_{in} = 28.238\text{W}. \quad (11)$$

(v) Estimate I_{in} via

$$I_{in} = \frac{P_{in}}{V_{in}} = \frac{28.238}{12}, I_{in} = 2.353\text{A}. \quad (12)$$

(vi) Select $\Delta i_L = 0.6$A by using the specified nominal switching frequency set in Table 1, to be applied in equation (13), and calculate the essential value of the inductor.

$$L = \frac{V_{in}}{f\Delta i_{L1}}\delta, L = \frac{12}{100e^3 * 0.6} * 0.667,$$
$$L = 100\,\mu\text{H}. \quad (13)$$

(vii) Assume $\Delta V_o = 0.12$V by using f_s in Table 1, to be applied in equation (14), and evaluate C_o and C_1.

$$C_o = \frac{(1-\delta)V_o}{f\Delta V_o R}, C_o = \frac{(1-0.667) * -36}{100e^3 * -0.16 * 50},$$
$$C_o = C_1 = 30\,\mu\text{F}. \quad (14)$$

Substitute the FPOSLLC specification in (7) to attain the model in Figure 2(a).

2.4. Open-Loop Study of the FPOSLLC. The MATLAB/Simulink model block diagram and its simulated result of the FPOSLLC in open-loop mode are displayed in Figures 2(a) and 2(b) with $V_{in} = 12$ V and $V_o = 36$ V. It is clearly found that the FPOSLLC in open-loop mode has created massive overshoots

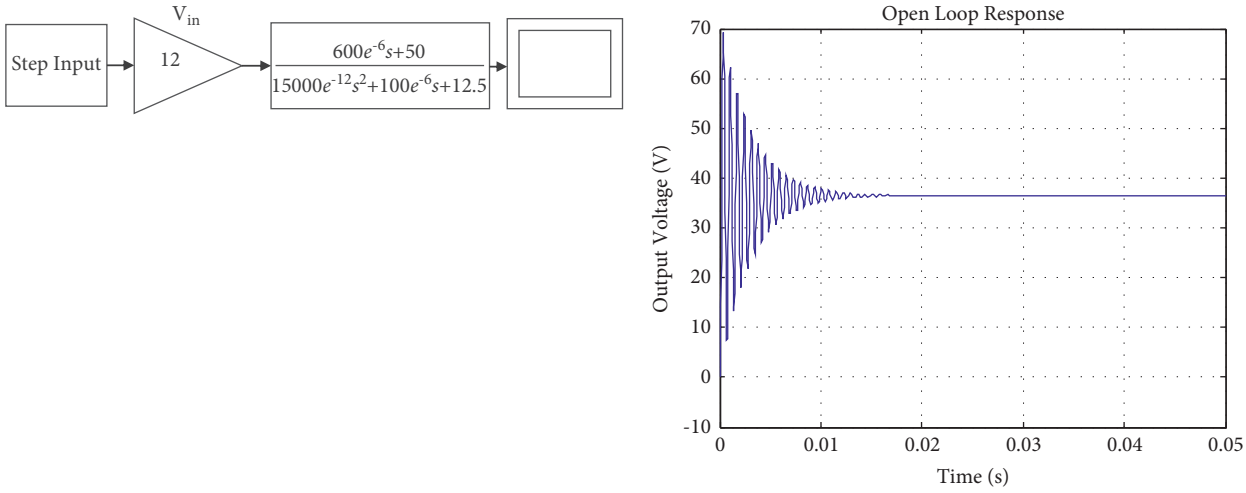

Figure 2: (a) MATLAB/Simulink model of the FPOSLLC and (b) simulated open-loop response of the FPOSLLC.

and took a long time to settle. In order to solve this problem, a new posicast control is designed for FPOSLLC in CCM.

3. Design Controllers

3.1. Principle of Posicast. The step result of lightly damped model is revealed in Figure 3. It is categorized by λ and T_d [2, 3]. Figure 4 indicates the structure of a classical half-cycle posicast. It is intended based on λ and T_d. Precise information of the step result constraints produces control whose smallest zero frequency revokes the leading plant pair. It is known as half-cycle since the surrounded time delay is $T_d/2$. Therefore, HPC arrangement is explained in Figure 5.

The posicast function is prearranged via the following equation [2, 21]:

$$P(s) = \frac{\lambda}{1+\lambda}\left(e^{-sT_d/2} - 1\right). \quad (15)$$

$P(s)$ are λ and T_d. It fundamentally reforms the set values into two portions; primarily, control minus the scale quantity from the set value (R), in order to the peak of a lightly damped result matches to the set final value of FPOSLLC result. The peak time of the step response is $T_d/2$. Next, in this time delay, the complete value of the step reference is smeared to G(s), ensuring that V_o remains constant at set value. Alternative clarification is that the set value, which was previously removed from the input, now cancels any undesirable overshoots since it is delayed by $T_d/2$.

3.2. Modelling of Hybrid Posicast Controller. The main components of HPC are as follows: P(s) is the scaling factor parameterized by λ and the time delay element parameterized by *T*d. There are two design steps for HPC. First, P(s) is developed for the averaged model of the FPOSLLC. Then,

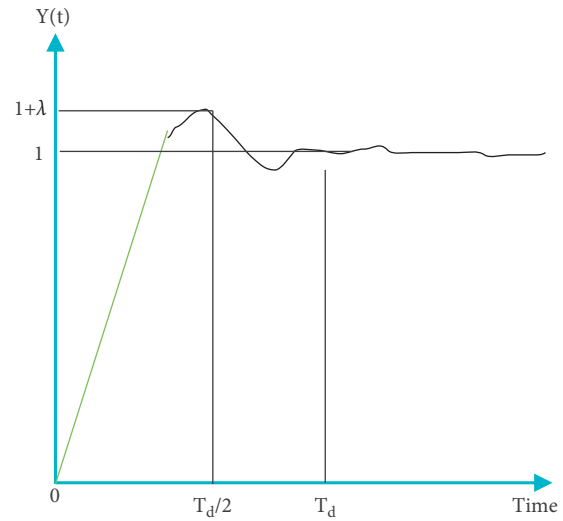

Figure 3: Step result of a flippantly damped FPOSLLC.

C(s) is framed to compensate joined model of (1 + P(s)) G(s). The classical frequency-domain approach is provided. A pure integrator type compensator is matched for the FPOSLLC to stabilize steady-state disturbances.

$$C(s) = \frac{K}{s}. \quad (16)$$

The gain K is selected to reduce the settling time as much as feasible, but not to the point where the overshoot is excessive. A new HPC model (17) is attained by joining the compensator C(s) and the P (s) [3, 21].

$$C(s)(1 + P(s)) = \frac{K}{s}\left(1 + \frac{\lambda}{1+\lambda}\left(e^{-sT_d/2} - 1\right)\right). \quad (17)$$

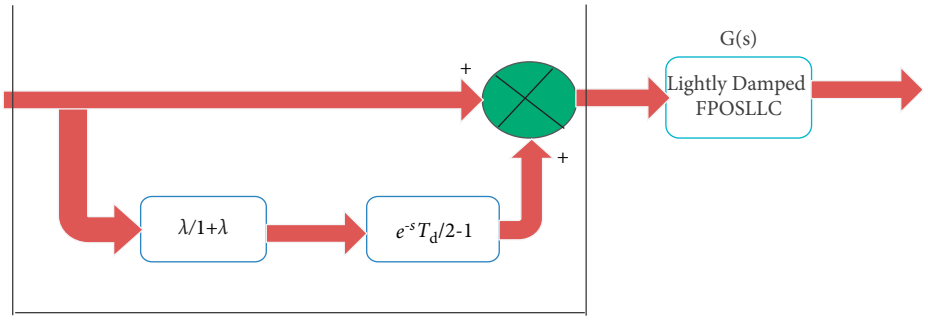

Figure 4: The classical half-cycle posicast.

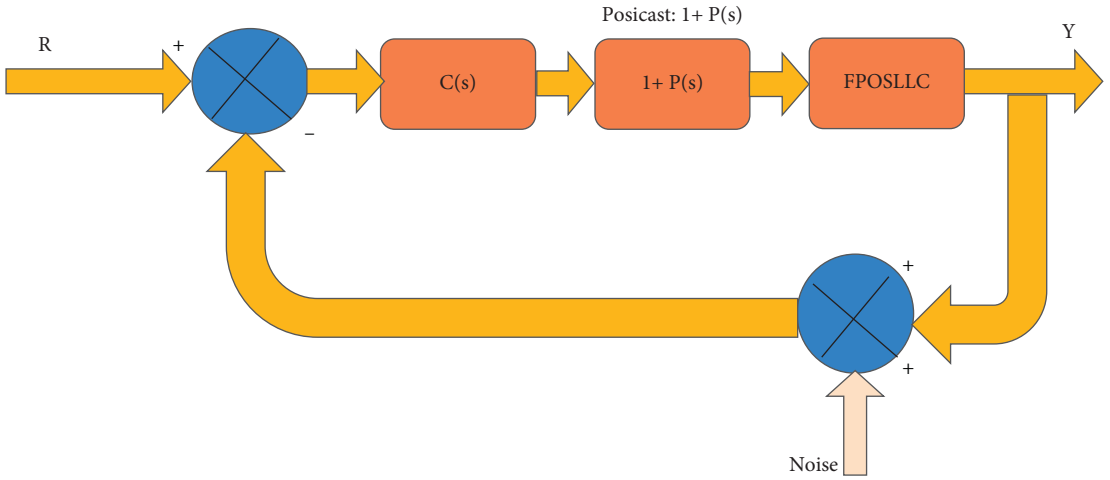

Figure 5: FPOSLLC with HPC.

3.3. Design of a New HPC. Small-signal model transfer function of the FPOSLLC is

$$G(s) = \frac{\hat{v}_o}{\hat{\lambda}} = 12\left(\frac{\left(600e^{-6}s + 50\right)}{\left(150000e^{-12}s^2 + 100e^{-6}s + 12.5\right)}\right). \quad (18)$$

Undamped natural frequency is

$$\omega_n = \sqrt{\frac{1}{LC}}, \quad (19)$$

$$T_d = \frac{2\pi}{\omega_n\sqrt{1-\zeta^2}}, \quad (20)$$

$$\lambda = e^{-\pi\zeta/\sqrt{1-\zeta^2}}. \quad (21)$$

The values of the new HPC parameters are computed using equations (18)–(21). Then, $T_d = 0.00219$ s and $\lambda = 0.8$. The K gain is designed to be as bulky as conceivable to reduce settling time of settling while avoiding unjustified overshoot, and it is fixed to be 7 in this work [2–4, 21].

Now, the model of HPC is

$$C(s)[1 + P(s)] = \frac{7}{s}\left[1 + 0.444\left(e^{-0.001s} - 1\right)\right]. \quad (22)$$

Figure 8 shows the frequency analysis of HPC in an open-loop model, C(s) (1 + P(s)) G(s). The gain margin is approximately infinity, while the phase margin is around 89.8°.

3.4. PID Controller. For the output voltage regulation of FPOSLLC, standard controllers based on the PID control are frequently utilized. The PID controller approach may effectively control the low-order dynamics of power modulators. Traditional PID controller is problematic to surpass in this case because the integrator raises the converter type number, reducing the fixed state error. Controller has two zeros allowing for booming physiognomies to be dampened and the transient result to be enhanced. The PID controller is a simple structure for understanding in comparison with other control methodologies. For new HPC comparison, the PID compensator was designed for the FPOSLLC. In this article, the Ziegler–Nichols tuning method [21–23] is used to evaluate the PID control parameters for transfer function model FPOSLLC, which are obtained from the previous sections. Then, transfer function of PID control is expressed as (23) and its frequency response of open-loop model is illustrated in Figure 7.

$$G_C(s) = 0.23 + \frac{400}{s} + 0.985s. \quad (23)$$

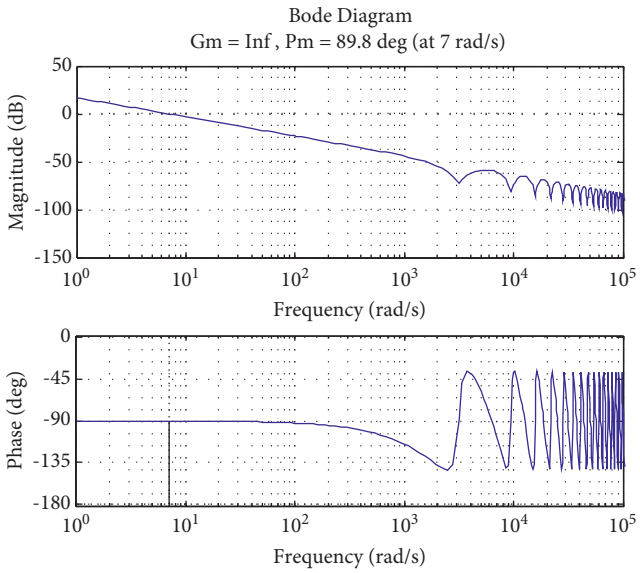

Figure 6: Frequency response analysis of HPC.

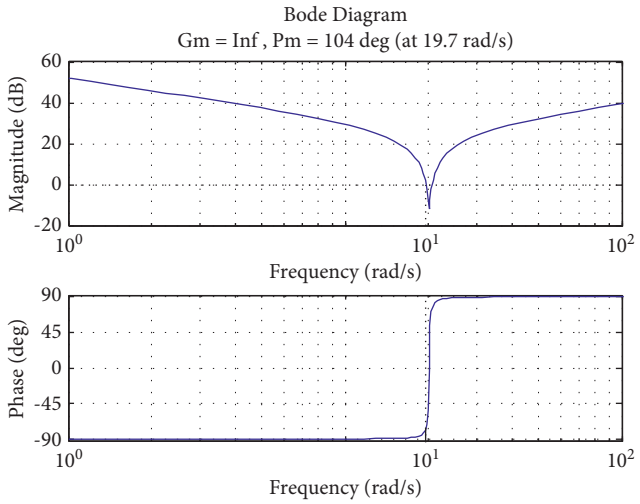

Figure 7: Frequency result of PID control.

When comparing the suggested posicast-based control to traditional PID control, several interesting results emerge. When compared to the PID-compensated system, the posicast-compensated magnitude response is dramatically attenuated at higher frequencies for the same gain margin. As a result, the posicast-compensated system suppresses high-frequency noise far more effectively than the PID method. From Figures 6 and 7, new HPC removes frequency noise superior than the PID control.

4. Simulation Results and Discussion

This part discusses the simulation results of FPOSLLC using HPC and PID controllers. The enactment of converter with controllers is verified at different working circumstances. Figure 8 portrays the Simulink model of FPOSLLC with HPC.

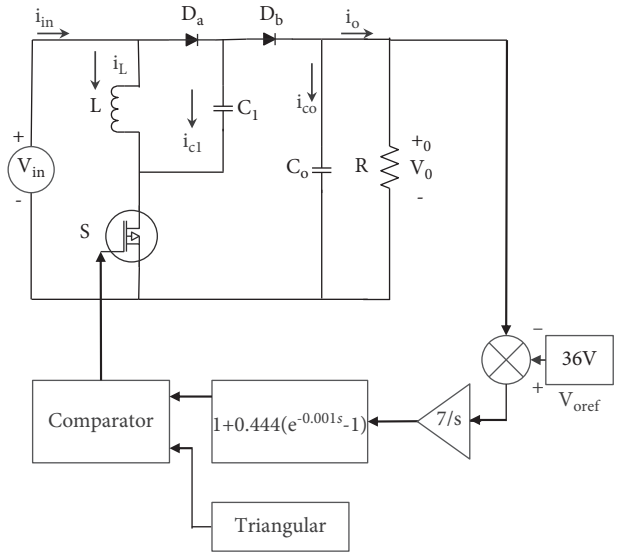

Figure 8: Simulink model of HPC for FPOSLLC.

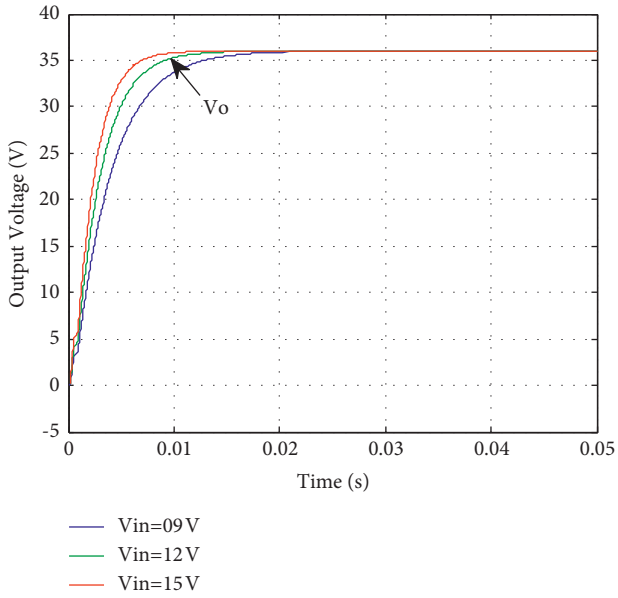

Figure 9: Simulated V_o response of FPOSLLC with HPC for various V_{in}.

4.1. Line Variations. Figures 9 and 10 show the simulated characteristics in the startup for V_o and duty cycle of FPOSLLC with HPC for various V_{in} such as 09 V, 12 V, and 15 V, respectively. It is evident that V_o of the FPOSLLC with HPC has insignificant overshoots and quick settling times of 0.02 s, 0.015 s, and 0.011 s in transient region at different V_{in}.

4.2. Load Variations. Figures 11 and 12 indicate simulated results in startup for V_o and output current of FPOSLLC with designed controller for various R such as 40 Ω, 50 Ω, and 60 Ω, respectively. It is clearly found that V_o of the same converter has generated trifling overshoot and took

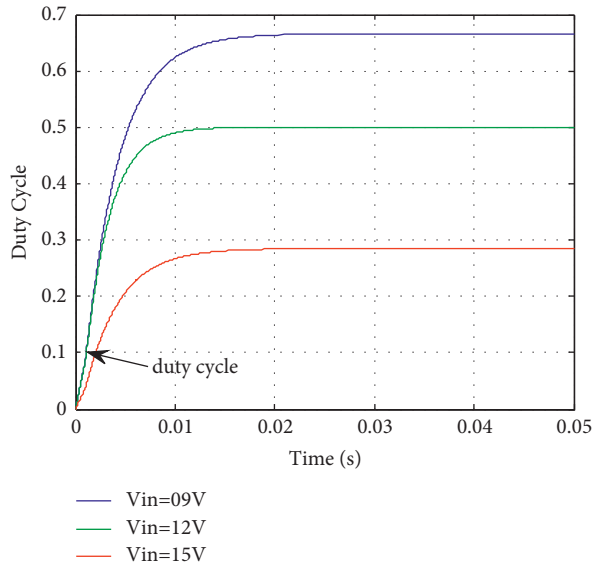

Figure 10: Simulated response of duty cycle of FPOSLLC with HPC for various V_{in}.

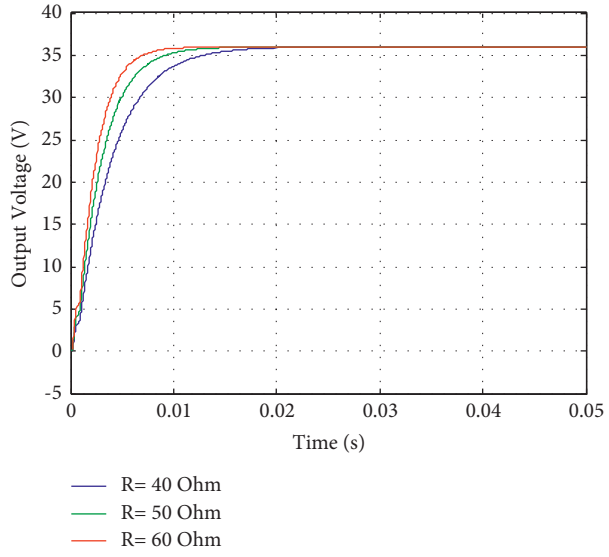

Figure 11: Simulated V_o results of FPOSLLC with HPC for various R.

time of settling 0.014 s, 0.012 s, and 0.011 s intended for $R = 40\ \Omega$, $R = 50\ \Omega$, and $R = 60\ \Omega$ in startup with proficient HPC.

4.3. Various Controller Parameters. Figures 13 and 14 show the simulated V_o results of FPOSLLC with designed controller for various values of T_d and compensator gain K. From these figures, it is found that the output voltage of FPOSLLC with control has null overshoots and small steady-state error for different values of T_d and K.

Results of V_o, duty cycle and quantity of noise of FPOSLLC with HPC are shown in Figure 15. It is observed that the settling time of converter with HPC is 0.03 s.

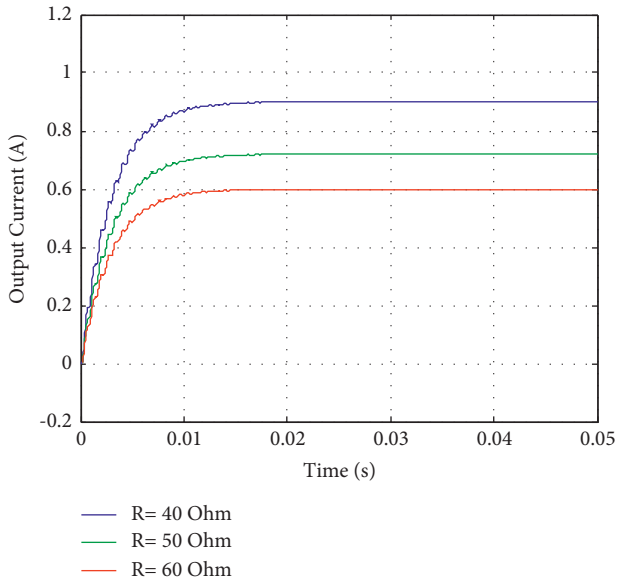

Figure 12: Simulated responses of output current I_o of FPOSLLC with HPC for different R.

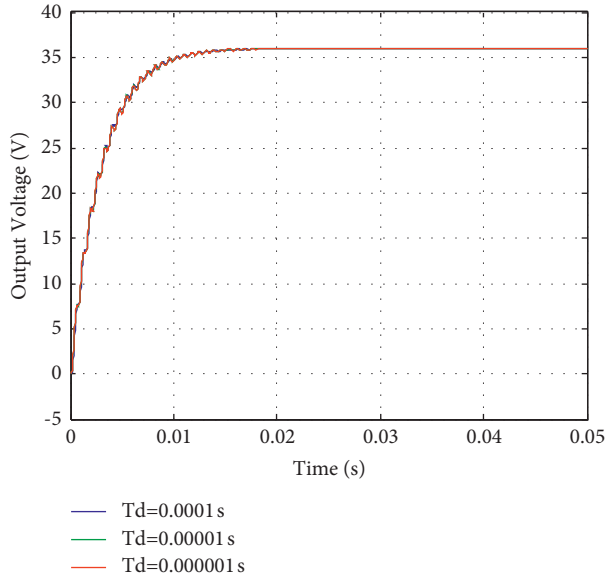

Figure 13: Simulated response of V_o of FPOSLLC with HPC for dissimilar T_d.

4.4. Comparative Analysis of Different Controllers. Figure 16 shows simulated results of FPOSLLC with HPC and PID controller. It could be observed that V_o of FPOSLLC with HPC has a null overshoot, rapid settling time, and excellent noise suppression over the PID controllers. In summary, the HPC performs better than PID.

4.5. Simulation Results of Steady-State Region. Table 2 shows the numerically simulated V_o of FPOSLLC with HPC and PID controller for changing V_{in} from 3 V to 15 V. From this table, it is evident that the output voltage of FPOSLLC with

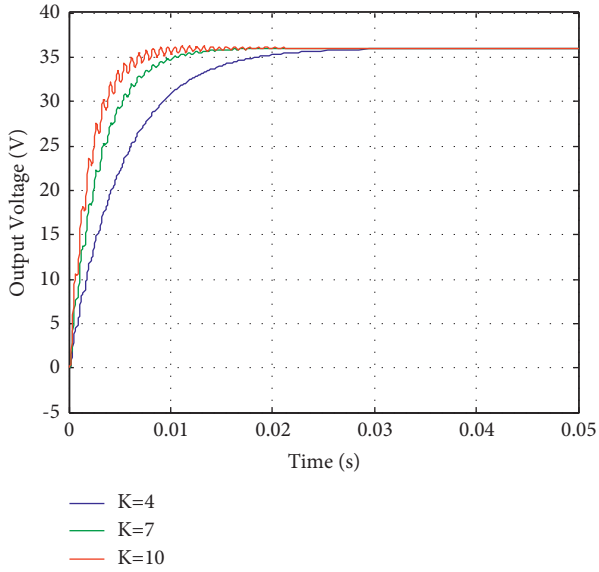

Figure 14: Simulated results of V_o of FPOSLLC with HPC for various K.

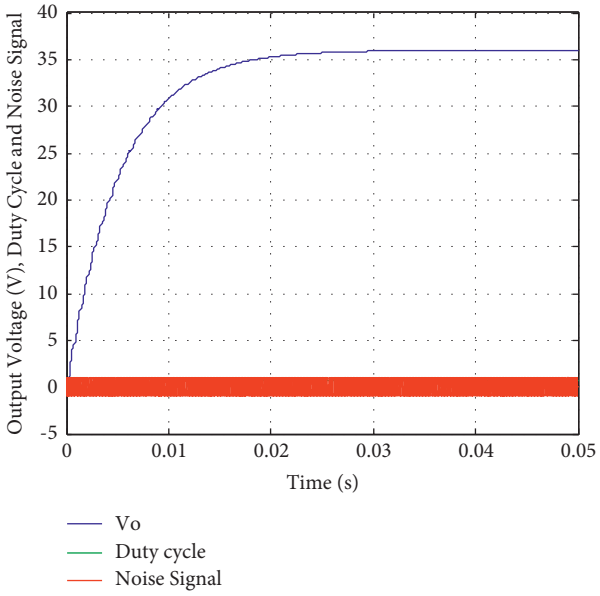

Figure 15: Simulated results of V_o, duty cycle, and quantity of noise of FPOSLLC with controller for constant V_{in} and controller parameters.

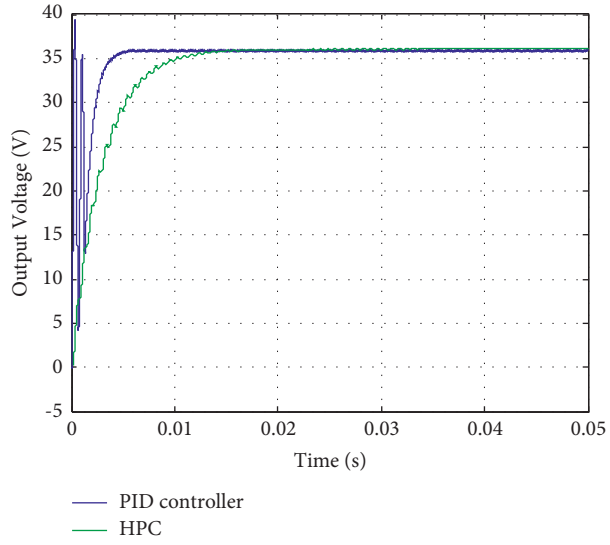

Figure 16: Results of V_o FPOSLLC with HPC and PID control for $V_{in} = 12$ V and $R = 50\,\Omega$.

designed HPC has small deviation in steady-state conditions at input voltage changes from 3 V to 15 V, whereas PID for same converter has more deviations at different V_{in}.

Figures 17 and 18 show the simulated measured/reference output voltage of FPOSLLC with HPC. From these figures, it is clearly observed that the measured V_o follows the reference V_o without overshoot and rapid settling time. Time-domain specifications of FPOSLLC with controllers are recorded in Table 3. From this table, it is evident that the designed controller has proficient performance in comparison with traditional PID control at line and load variations.

Table 2: Output voltage variations with HPC for $K = 7$, $T_d = 0.00219$ s, $\lambda = 0.8$, $R = 50\,\Omega$, and $v_{oref} = 36$ V.

V_{in} (V)	HPC		PID controller	
	V_o (V)	Deviation (V)	V_o (V)	Deviation (V)
3	35.982	0.013	34.912	1.088
4	35.990	0.012	34.980	1.002
5	35.992	0.006	34.991	1.009
6	35.993	0.007	34.992	1.008
7	35.995	0.005	34.995	1.005
8	35.994	0.004	34.994	1.006
9	35.997	0.003	34.996	1.004
10	35.999	0.001	35.997	0.003
11	36	0	36.211	0.211
12	36	0	36.221	0.221
13	36.01	0.01	36.32	0.31
14	36.015	0.015	36.35	0.35
15	36.018	0.018	36.38	0.38

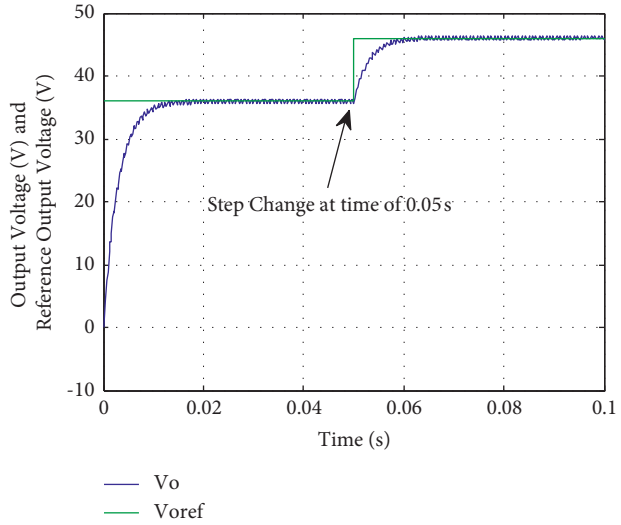

Figure 17: Simulated output voltage responses of FPOSLLC with HPC for reference V_o from 36 V to 46 V at time of 0.05 s.

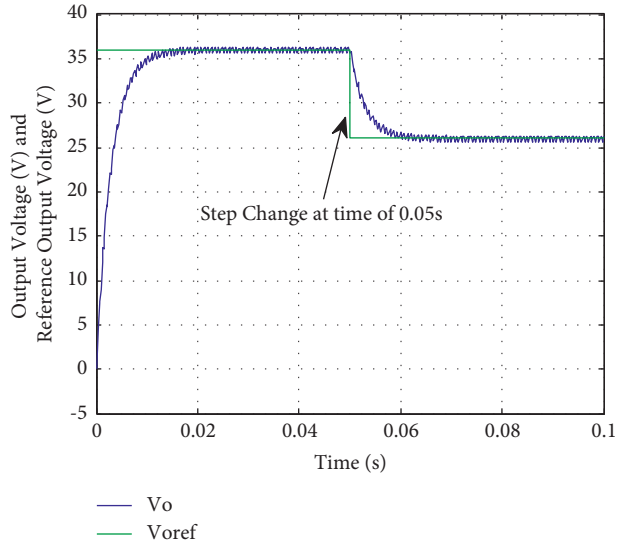

Figure 18: Simulated output voltage responses of FPOSLLC with HPC for reference output step change from 36 V to 26 V at time of 0.05 s.

Table 3: Simulated numerical time-domain specification analysis of FPOSLLC using controllers.

Startup region			Line variations				Load variations			
	M_p	$T_{s\ (s)}$	$V_{in} = 12$ V to 15 V		$V_{in} = 15$ V to 12 V		$R = 50\ \Omega$ to $60\ \Omega$		$R = 50\ \Omega$ to $10\ \Omega$	
			M_p	$T_{s\ (s)}$	M_p	$T_{s\ (s)}$	M_p	$T_{s\ (s)}$	M_p	$T_{s\ (s)}$
HPC	Nil	0.01	2 V	0.01	2 V	0.01	0.5 V	0.01	0.5 V	0.01
PID	4 V	0.005	6 V	0.02	6 V	0.04	1 V	0.02	1 V	0.02

5. Conclusions

A new HPC for output voltage regulation of FPOSLLC in CCM has been built with help of the Simulink software model. For the analytical and ideal techniques of FPOSLLC, the elements of posicast are explicitly computed. Better damping abilities, proficient output voltage regulation in line/load variations, minimized overshoots, quick settling time, reduced high frequency noise, easy digital implementation, and minimizing sensitivity of traditional approach are the main benefits of the newly designed HPC over PID control. Because of the integral compensator and single gain of the new HPC, the FPOSLLC's steady-state response has improved. In contrast to PID control, the new HPC simply wants to modify the gain K, and the compensated plant has improved the gain/phase margins, while the short open-loop bandwidth verifies the conquest of higher frequency noise. Time-domain analysis of HPC for FPOSLLC has proficient performance over the PID control. Finally, for FPOSLLC in CCM, the newly developed HPC has excellent output voltage regulation at different input voltage and load resistance variations. It can be used to power LED drivers, medical instruments, solar systems, and mobile phones. In the future, the hardware model of FPOSLLC with HPC, as well as the design of super-twisting sliding mode control, will be implemented.

Abbreviations

V_{in}: Source voltage
C_1, C_o, L: Storage elements
S: Power switch
D_a, D_b: Diodes
V_o: Load voltage
R: Load resistance
C_o: Output capacitor
i_L: Inductor current
I_{in}: Average input current
I_o: Average output current
δ: Duty cycle
Δi_L: Inductor current ripple
η: Efficiency
P_{in}: Input power
P_o: Output power
ΔV_o: Capacitor ripple voltage
f_s: Operating switching frequency
T_d: Natural period (damped)
λ: Overshoot
K: Gain
ω_n: Undamped natural frequency
$C(s)$: Compensator
$P(s)$: Posicast function
CCM: Continuous Conduction Mode.

Data Availability

The data used to support the study's findings are included in the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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