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Research Article

Performance Enhancement of a Three Phase Boost-Cascaded Fifteen Level Inverter Using the PI Controller

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Photovoltaic power generation is a potential alternative energy source that offers several benefits over other alternative energy sources such as wind, sun, ocean, biomass, geothermal, and so on. Multilevel inverters are essential for power conversion in solar power generation. These multilevel inverters employ three distinct topologies: diode-clamped (neutral-point clamped) inverter, capacitor-clamped (flying capacitor) inverter, and cascaded H-bridge multilevel inverter. The cascaded H-bridge multilevel inverter is more appropriate for photovoltaic applications than the other two topologies. The proposed system asymmetrical cascaded multilevel inverter (ACMLI) is energized using a photovoltaic system (PV). A three-phase cascaded H-bridge fifteen-level inverter for grid-connected solar systems is given in this study utilizing a proportional integral controller. The harmonic distortion was removed using a multicarrier pulse width modulation method. The MATLAB/Simulink is used to simulate the performance of a three-phase cascaded H-bridge fifteen-level inverter in terms of harmonic content and number of switches. To test the performance of the designed system, a hardware prototype was created. From the obtained results, the proposed method reduces the switch count, harmonic distortion, and rejects the external disturbances of input and output variables.

1. Introduction

Automatic regulation is a configuration and research method for a self-regulating device. This automated control technique can be used in a number of applications, such as manufacturing processes and chemical industry. By minimizing the objective function, the automated control deals with the creation of an optimized controller for both offline and online industrial applications, thus satisfying other constraints such as interruption and robustness. PID controllers are most commonly used in many manufacturing applications and process control industries to control the system with the desired fixed point due to flexibility and ease of tuning. The PID controller algorithm is then clarified by three functions, such as proportional gain (K_p), integral gain (K_i), and derivative gain (K_d). In order to get the best plant output, these three parameters are modified. [1–4].

The controller comprises of a fractional derivative, and relative to traditional PID controllers, the integral could achieve improved efficiency and robustness. The fractional controls are calibrated for the satisfactory efficiency of the plant. Controller tuning is the method of getting the

parameters of the controller to match the output requirements that are specified. This work proposed tuning of H controllers for the fractional SISO method [5–10].

The tuning technique of these controllers is based on previous understanding of the regulation of fractional and integer order. The suggested linear input-output mapping of the rule base has been shown to be used. [11] By rendering the fuzzy fractional controller nonlinear by applying saturation with squared membership function, the stability of the fractional controller was checked. The fuzzy fractional order PID controller is then designed for better device dynamic control.

The proportional integral controller is designed for a class of fractional systems. From the simulation and experimental performance, both the fractional PI controller designed and the standard integer order designed for the same set of tuning constraints applied were designed. [7, 12–16] This will guarantee the optimal control quality and robustness to the loop gain variants of the built controllers. In this process, with enhanced efficiency, the two built fractional order controllers function effectively. As compared to the stabilizing integer order PID controller, the built FOPI and FO (PI) controllers will increase the control efficiency for the fractional order systems.

The open-loop transfer functions of many practical systems are highly unstable, making it challenging for the closed-loop system to maintain acceptable stability margins and control efficiency. As a result, a single fixed controller is included in the "robust control" family of such systems. Quantitative feedback theory (QFT) is a method for designing a reliable feedback control system. Horowitz (Horowitz, 1991) and Horowitz, 1992) established an approach that allows for the direct design of closed-loop resilient output and stability criteria. The following is a simple description of the QFT controller design approach: Before designing the QFT in parametric uncertain systems, we must first create plant models (at a fixed frequency; the plant frequency response set is called a template). [17, 18] The nominal open-loop function is then tuned to satisfy its restrictions while still maintaining nominal closed-loop stability. The nonlinear plant is turned into a family of linear and unknown processes in the QFT system. The QFT literature provides a variety of methods for this purpose (Horowitz, 1991), (Horowitz, 1992), Gharib et al. (2010), Gharib et al. (2011), Gharib and Moavenian (2012), including linear time-invariant equivalent (LTIE) of nonlinear plants and nonlinear equivalent disturbance attenuation (NLEDA) techniques (Horowitz, 1991).

A class of nonlinear control approaches relies on feedback linearization under the assumption of measured states [12, 19, 20]. The basic idea is to convert a nonlinear system into a linear system by adding a component to the control force that cancels out the nonlinear dynamics. When this is accomplished, the state equation becomes linear, allowing for the use of traditional control methods. This method is used in this study, with the linear quadratic regulator (LQR) as the control tool; this is a popular choice for vibration reduction. [18].

For industrial use, the fractional controller is used to increase the efficiency of machine operation. The architecture of the FOPID controller not only provides the need for benefit design but also for derivative and integral design instructions. There are two new variables for FOC to tune. This extension will offer even more consistency in the design of PID control. Superior efficiency and robustness can be obtained relative to conventional fractional controllers. [21].

2. Proposed Three Phase Fifteen Level ACMLI

Three single phase H-bridge connections are used to create a three-phase fifteen-level asymmetrical cascaded multilevel inverter arrangement. In a half bridge construction, each cell is produced using independent dc sources. This is linked to the load, which might be linear or nonlinear, balanced or unbalanced. In a single-phase arrangement, each cell's output is linked in series with the next cell. [4].

The three-phase asymmetrical fifteen-level output multilevel inverter setup with the nonlinear or unbalanced load is shown in Figure 1.

The single-phase configuration contains three times the number of switches, input dc sources, power diodes, and gate driver circuit components.

2.1. Multicarrier Pulse Width Modulation. Only by employing the correct pulse with modulation approach can the fifteen-level output voltage be achieved. The gating pulses are generated using a multicarrier pulse width modulation method. Only the suggested multilayer inverter may use the thirteen-level output. The fifteen-level output voltage waveform is created by comparing the sinusoidal 180° displaced reference signal with triangular carrier signals. [13, 22–24].

The suggested inverter is a multilayer inverter, which means it has multiple switching components. As a result, the signals carried by multilayer inverters are based on the number of levels. The suggested multilayer inverter's number of carrier signals (Nc) is calculated using (n-1)/2, where n is the number of output levels. The number carrier signal, for example, is (15–1)/2, which equals seven (7). Because of this, the suggested fifteen-level inverter is seven levels positive (+7Vdc) and seven levels negative (+7Vdc). The phase shifted disposition method is used to arrange the carrier signals, which are then compared to the sinusoidal reference signal to create the gating signals for power switches. The amplitude, frequency, and phase of the carrier signals are all the same. The multicarrier signal is compared to the reference in Figure 2. [4].

The ratio of the reference signal to the carrier signal determines the modulation index (MI) for this amplitude method. Similarly, the frequency ratio is computed by dividing the carrier frequency by the frequency of the reference signal.

$$N_C = \frac{n-1}{2},$$

$$MI_a = \frac{A_r}{A_c\,(n-1)}, \tag{1}$$

$$MI_a = \frac{f_r}{f_c},$$

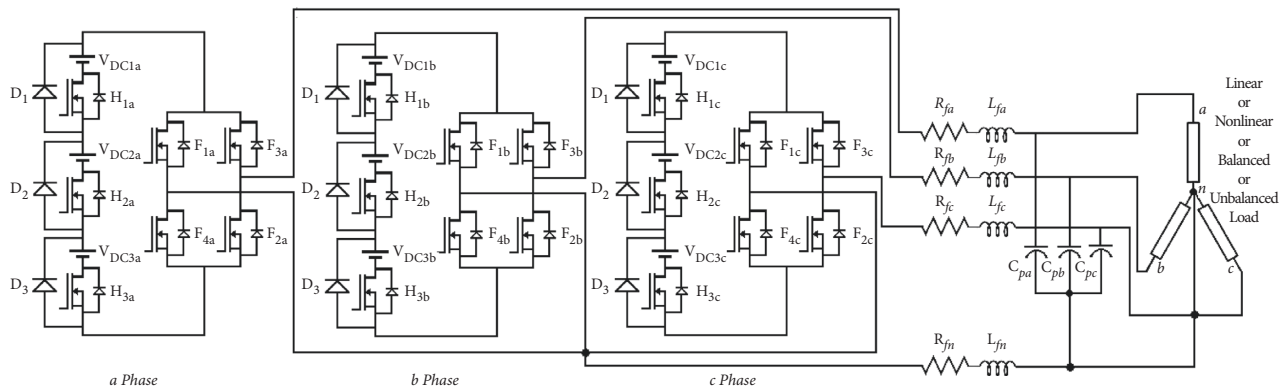


Figure 1: Three-phase fifteen-level asymmetrical cascaded multilevel inverter.

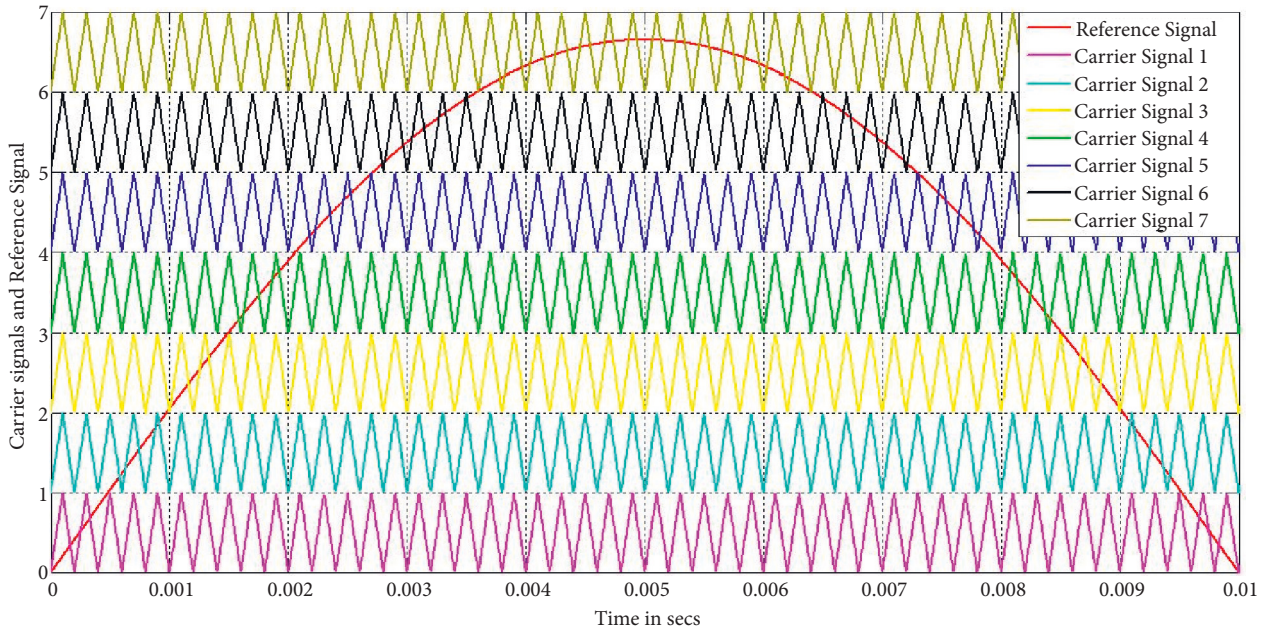


Figure 2: Multicarrier signal compared with the reference signal.

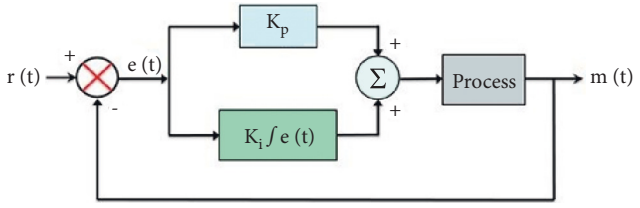


Figure 3: Block diagram of the PI controller.

Table 1: Comparison of P, PI, and PID controllers.

Parameter	Speed of response	Stability	Accuracy
Climbing K	Raise	Decays	Enhances
Climbing K_i	Drop	Decays	Enhances
Climbing K_d	Raise	Enhances	Ineffective

Table 2: Comparison of parameters with various controllers.

Parameter	P controller	PI controller	PID controller
Rise time	Drop	Drop	Minor drop
Overshoot	Raise	Raise	Minor drop
Settling time	Small difference	Raise	Minor drop
Steady state error	Drop	Dramatic change	No change
Stability	Poor	Poor	If K_d little better.

where A_r is the amplitude of the reference signal, A_c is the amplitude of the carrier signal, N is the number of levels, f_r is the frequency of the reference signal, and f_c is the frequency of the carrier signal.

2.2. Proportional Integral (PI) Controller. Because of its simple form, ease of design, and low cost, the PI controller is currently the most extensively used in industrial

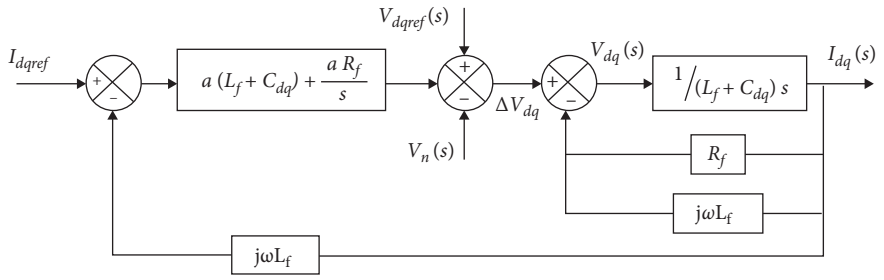


Figure 4: PI controller feedback mechanism.

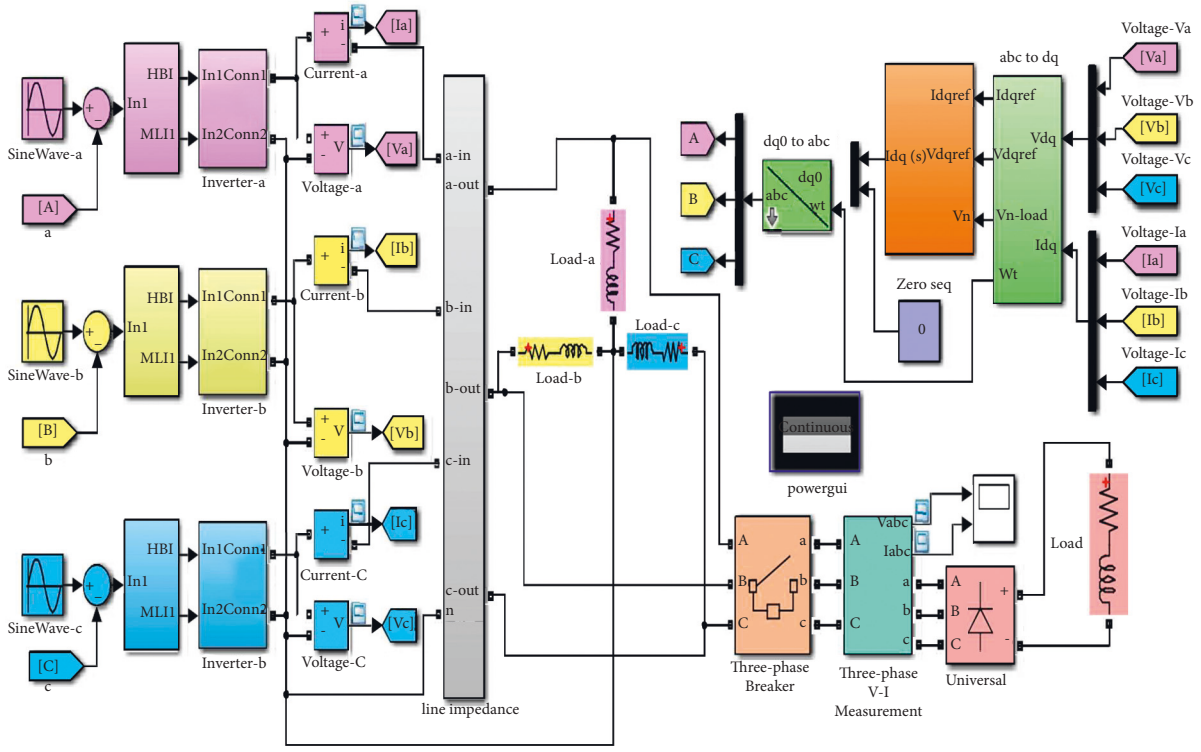


Figure 5: Simulink framework of the three phase fifteen-level cascaded boost multilevel inverter.

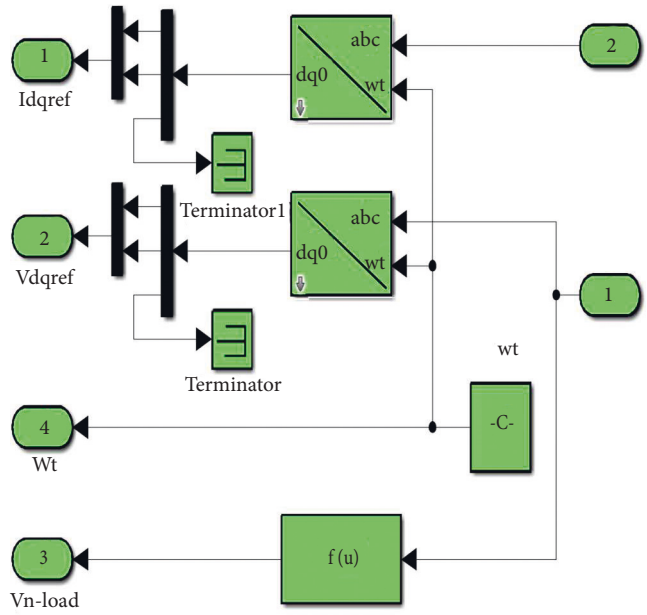


Figure 6: abc to dq transition current and voltage.

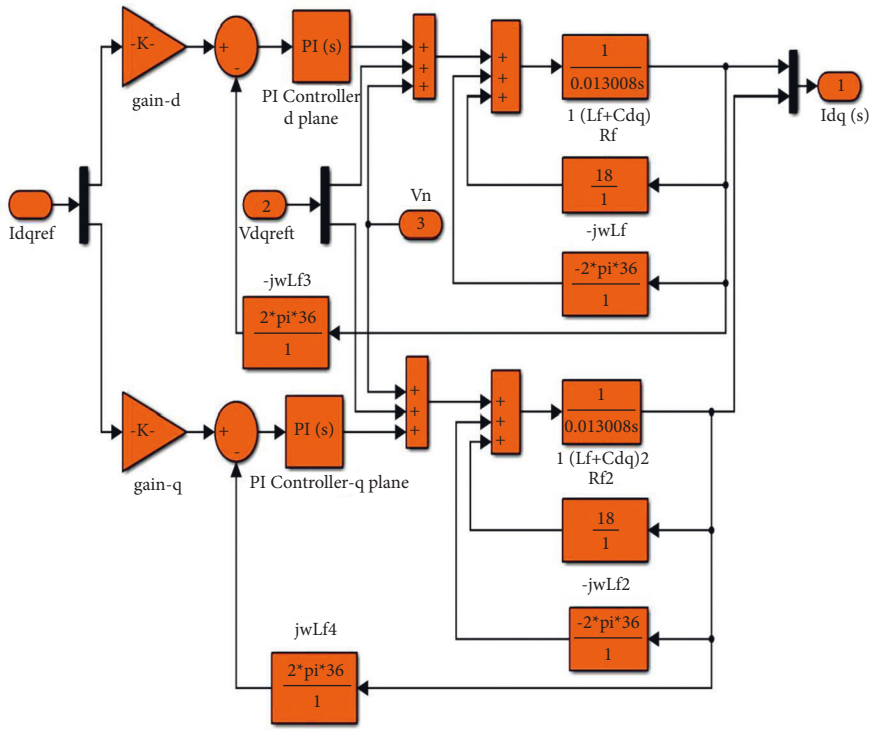


Figure 7: Frame work of PI controller feedback.

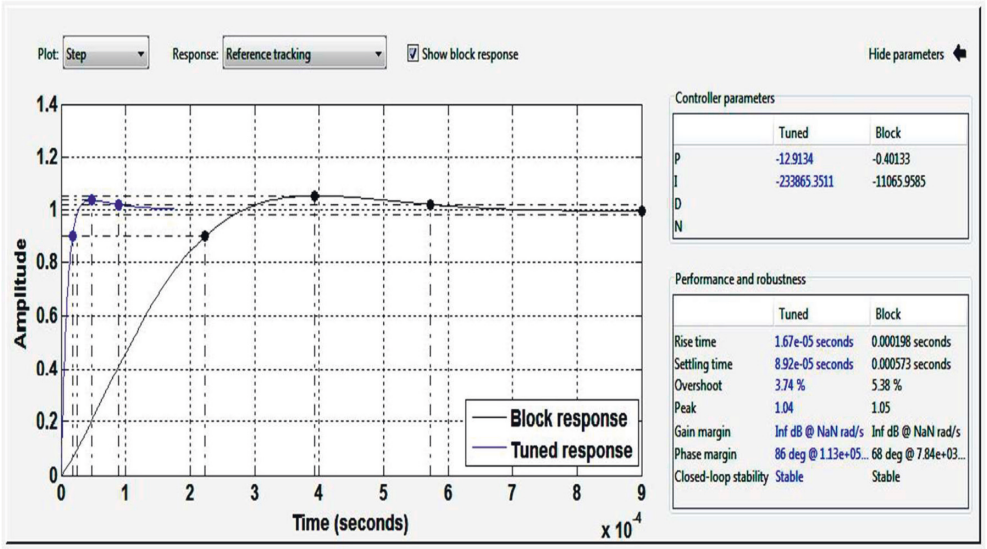


Figure 8: Tracking of reference based on Kp = −12.9134 and Ki = −23 variables.

applications. Despite these benefits, when the controlled object is highly nonlinear and uncertain, the PI controller fails. The PI controller will minimize forced oscillations and steady state errors, allowing on-off and P controllers to function properly. Integral mode, on the other hand, has a negative impact on the system's response time and overall stability. As a result, the PI controller will not increase the reaction time. It is to be expected, given that the PI controller has no way of knowing what will happen with the error in the near future. This difficulty can be overcome by using the derivative mode, which can predict what will happen with the error in the near future, reducing the controller's reaction time. In the industry, PI controllers are frequently employed, especially when response time is not a concern. [17]. where K_p is the proportional gain and K_i is the integral gain.

Figure 3 shows a block diagram of the PI controller. The output response of a PI controller, which uses an integral

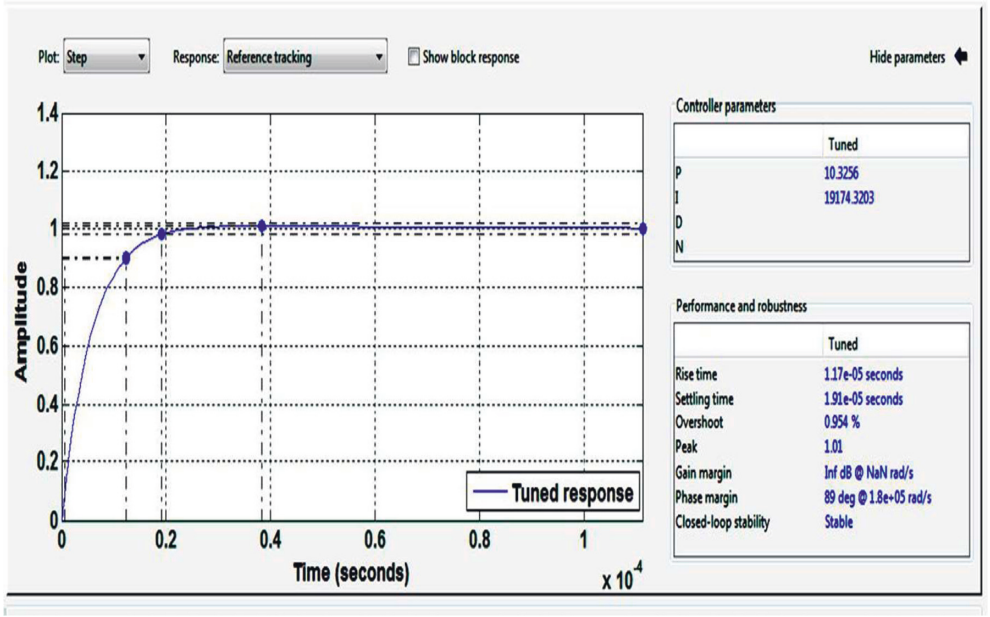


Figure 9: Tracking response of final step Kp = 10.3256 and Ki = 19174.3203.

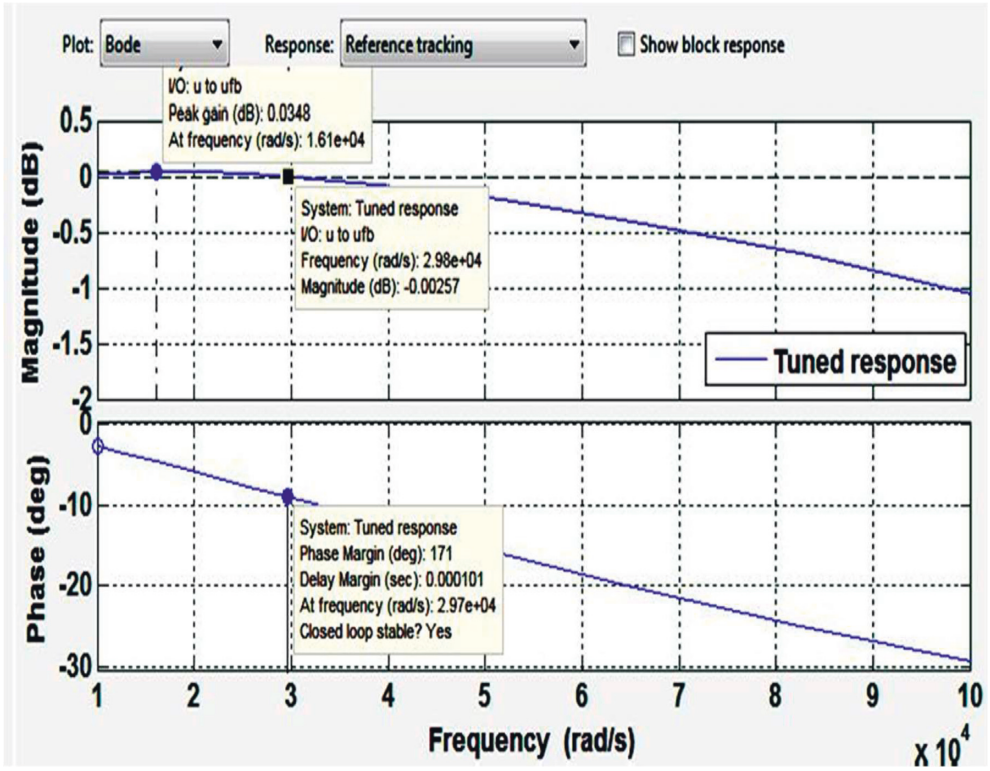


Figure 10: Response of the Bode plot at Kp = 10.3 and Ki = 19174.

error compensation system, is dependent on the integral of the actuating signal in some way. This sort of compensation is achieved by utilizing a controller that generates an output signal with two terms, one proportional to the actuating signal and the other proportional to the integral of the signal. Proportional plus integral controllers, or PI controllers, are examples of such controllers. [18].

$$u(t) = Kp.e(t) + Ki \int e(t)dt, \tag{2}$$

Tables 1 and 2 show the effects of changing the coefficients and control parameters, respectively. The rising time, overshoot, and settling times have all decreased, yet the steady state error has remained the same. The PID controller

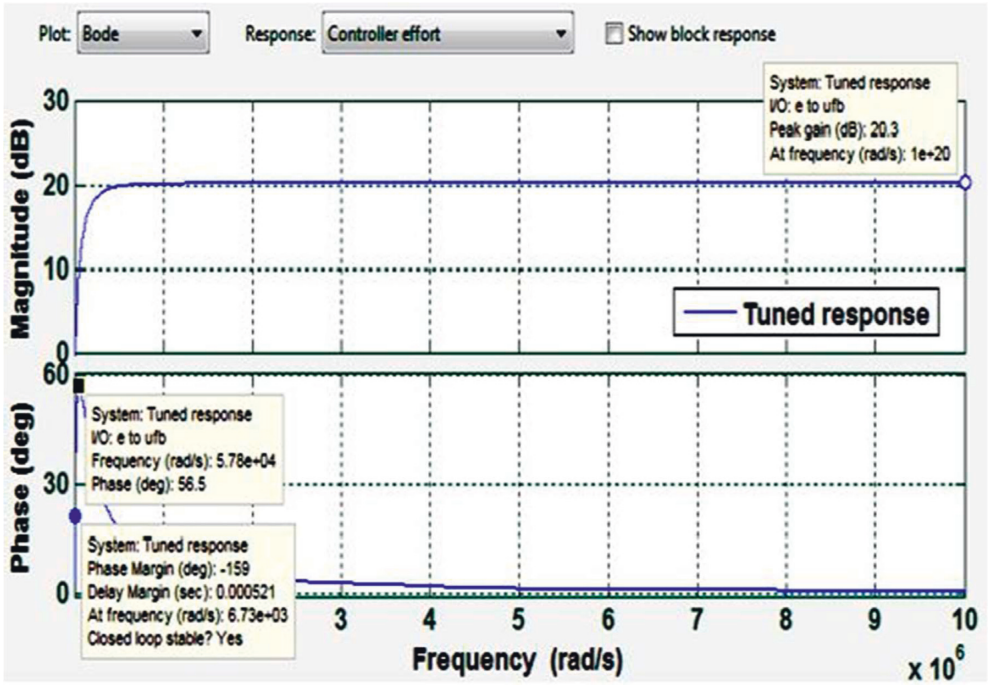


Figure 11: Response of the Bode plot for effort of controller at Kp = 10.3 and Ki = 19174.

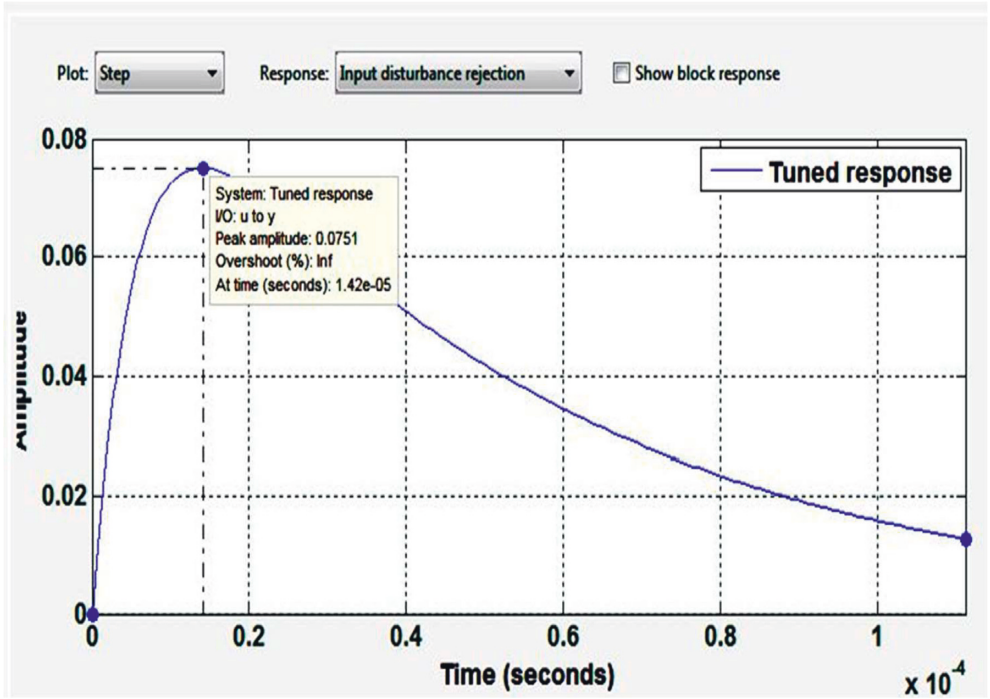


Figure 12: Step response for input disturbance rejection at Kp = 10.3 and Ki = 19174.

outperforms both the P and PI controllers in terms of performance.

2.3. Determining the Settings of the PI Controller. Tuning or enhancing the efficiency of the whole device is the key target of every controller, and the proposed PI controller is as follows:

$$T(s)\left(K_p + \frac{K_i}{s}\right). \tag{3}$$

Almost all Kp and Ki constants of the PI controller are chosen on the basis of checking the various values corresponding to their performance quality on a trial basis. In addition, by reducing the peak overshoot, the PI controller easily decreases the steady state error and increases the

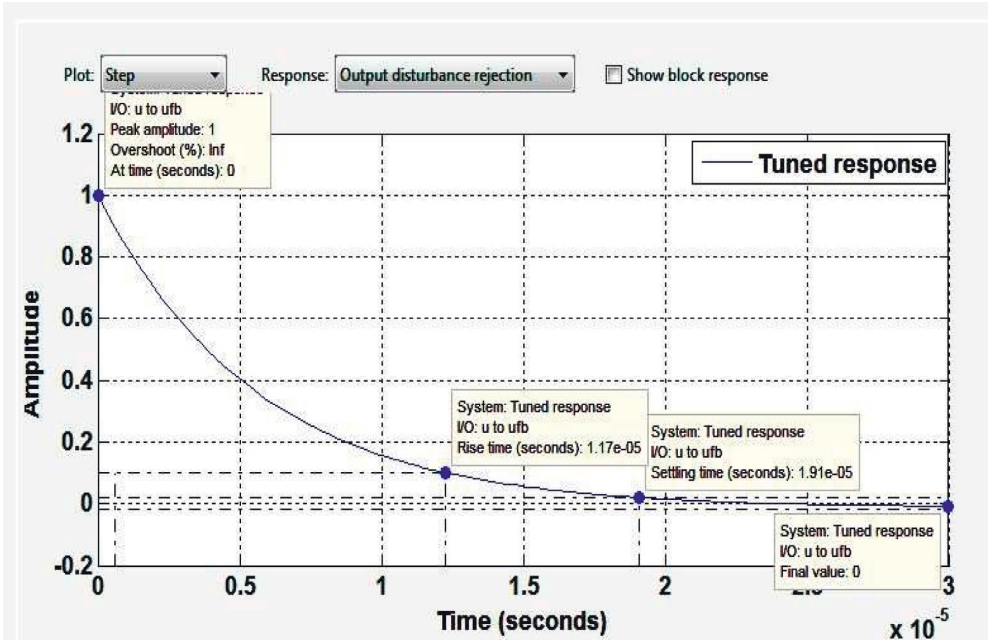


Figure 13: Step response for output disturbance rejection at Kp = 10.3 and Ki = 19174.

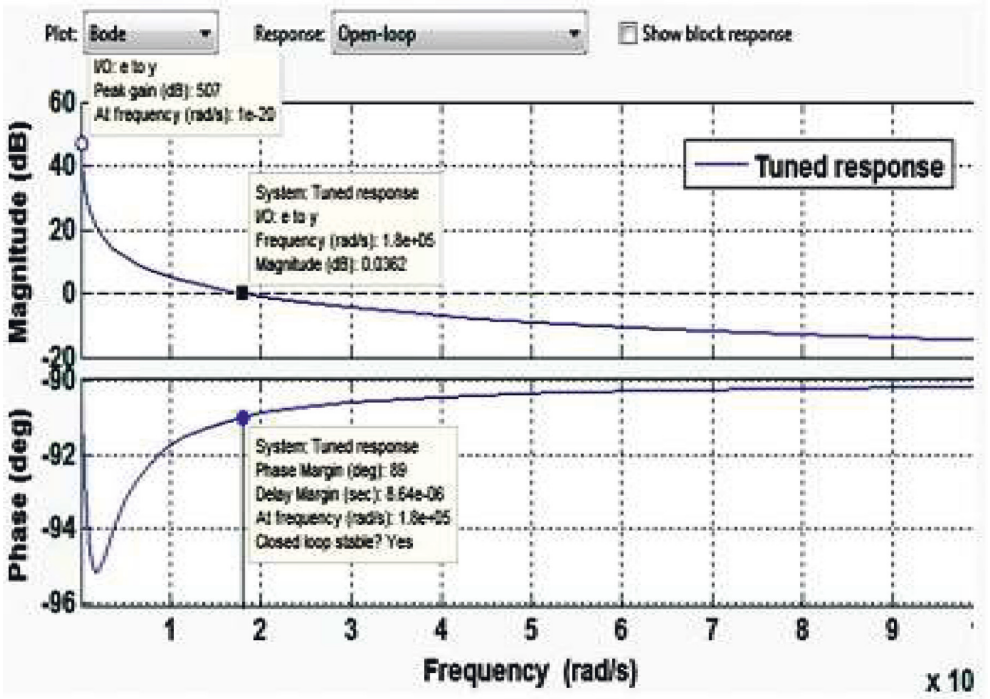


Figure 14: Open loop response of the Bode plot at Kp = 10.3 and Ki = 19174.

system's performance. From the output of the current controller reduction gain block, the closed-loop switch is then obtained.

As seen in Figure 4, the modeled controller was implemented in the proposed boost multilevel inverter of fifteen stages.

As per the load impedance rating, the Kp and Ki values are determined. 0.013008 is the proportional Kp controller, and 36 is the Ki. Depending on the impedance of the load, all values are tuned. [23].

3. Simulation and Hardware Results with the PI Controller

The simulation of the fifteen-level boost cascaded multilevel inverter with a PI controller was introduced in this segment

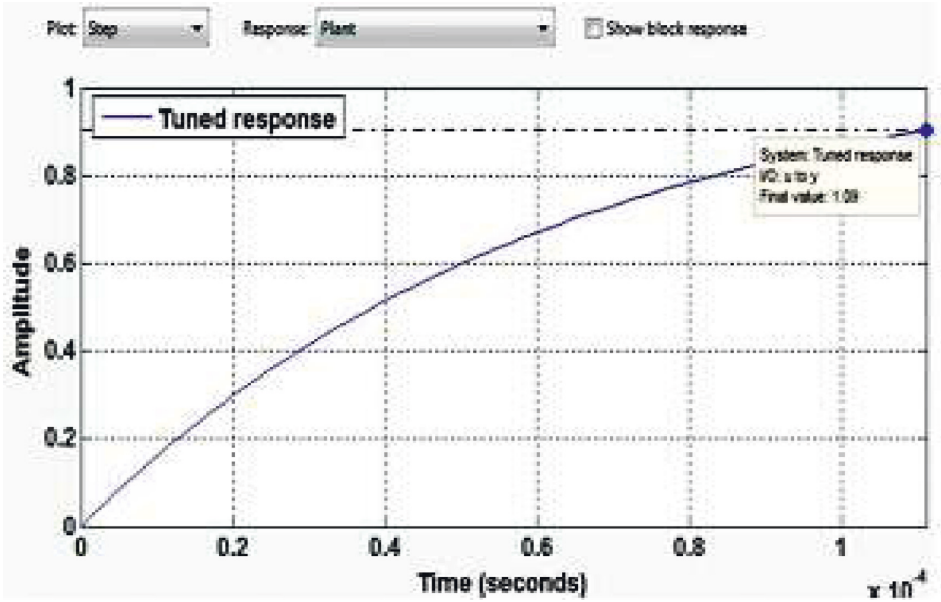


Figure 15: Response plant step at Kp = 10.3 and Ki = 19174.

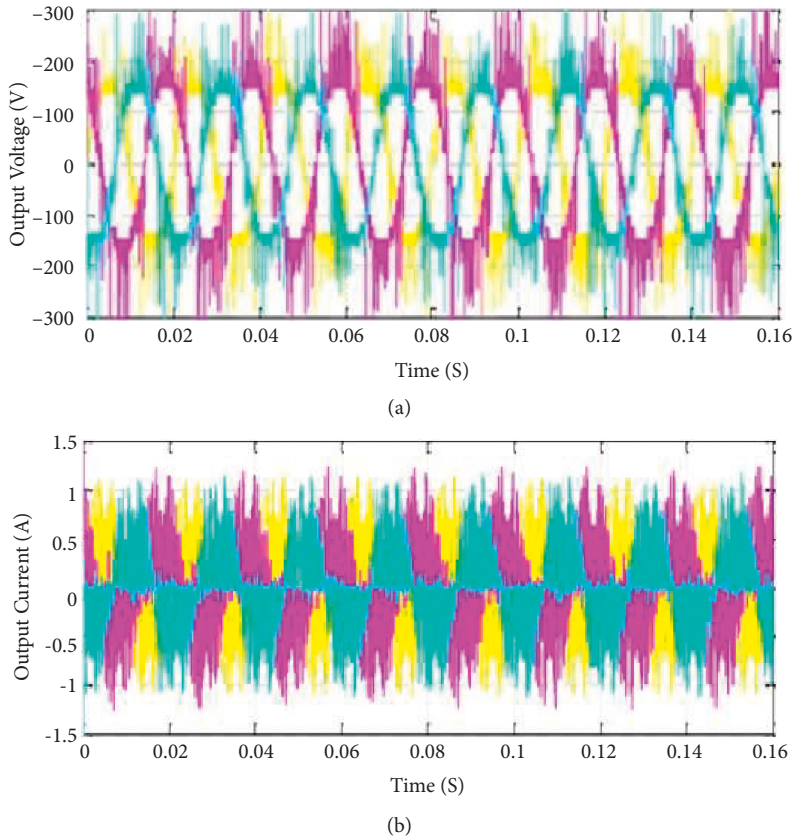


Figure 16: Output waveform of three phases (a) voltage and (b) current.

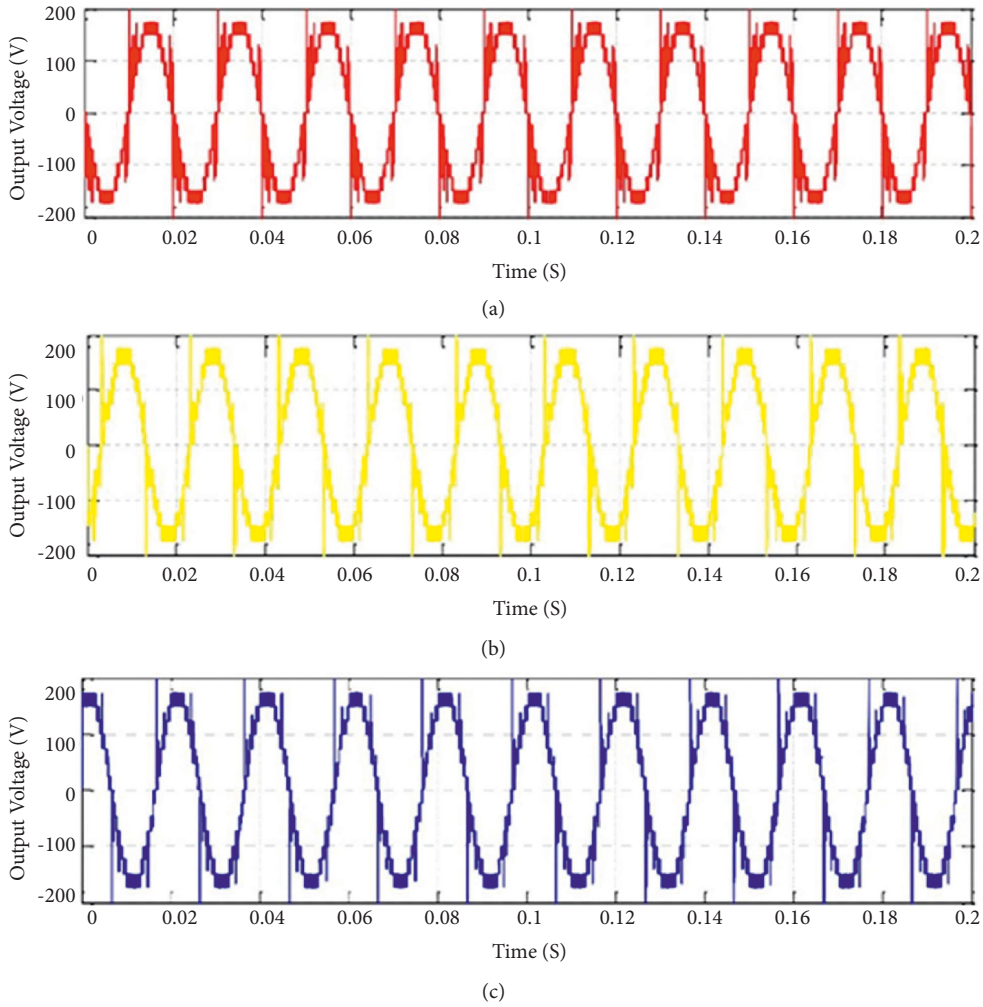


Figure 17: Phase output waveform of three phases (a) phase 'a', (b) phase 'b', and (c) phase 'c'.

and the software component in FPGA was experimentally updated. [2].

3.1. Simulation Results. Figure 5 displays the Simulink diagram of the fifteen-level boost cascaded multilevel inverter with feedback and the PI controller.

In addition, the abc to dq, PI controller input and dq to abc transition blocks are used in this method. As seen in Figure 6, the output voltage and current component are converted into dq to regulate the actual component and to remove the complex component.

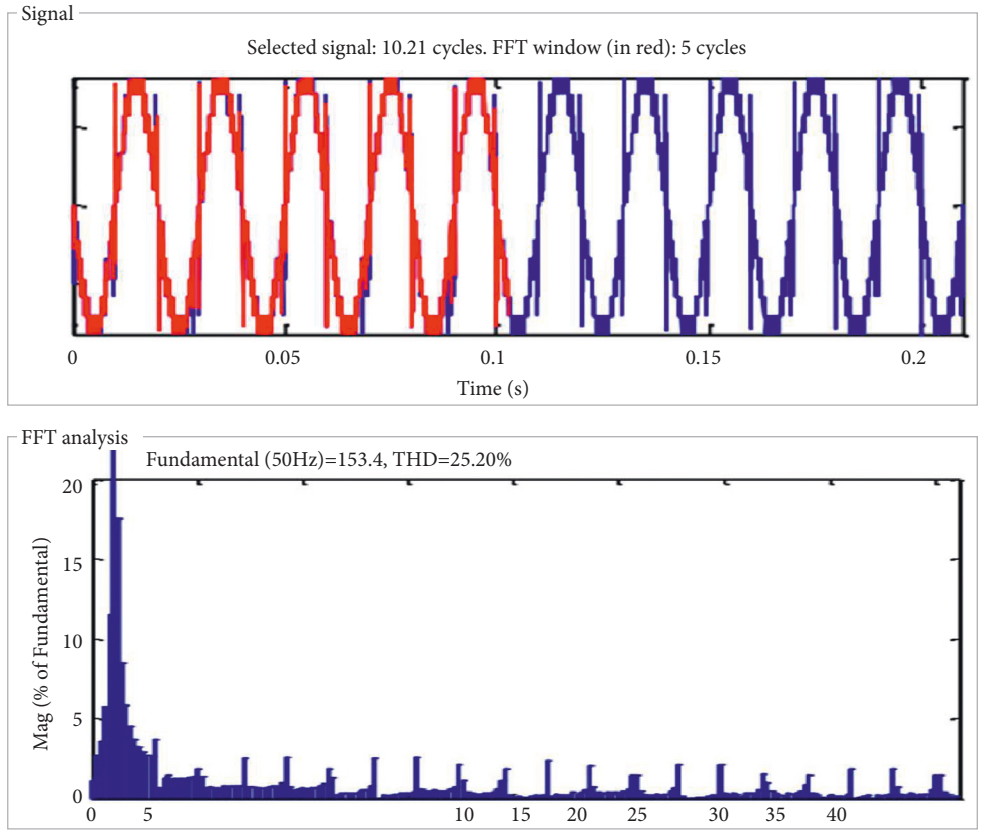
The input from the mathematical modeling of previous parts with the PI controller block was created, as seen in Figure 7. The current and voltage of the output load were compared with the comparison by converting the dq part.

From the unbalanced load voltage, the neutral line voltage and current were calculated and removed from the dq portion. In Figure 7, the calculated the value of Kp is 0.013008 and the value of Ki is 36; values are given in the PI controller block.

As shown in Figure 6, the tuned value of the feedback unit has been given to the dq input to the abc transformation block. The input was assigned to the regulated output voltage component and this can be inserted or subtracted depending on the load output. The gating signal was produced by comparison with the multicarrier signal with the changed relation. In Figures 8–15, the virtual output voltage and current waveforms with voltage harmonics continuum are displayed.

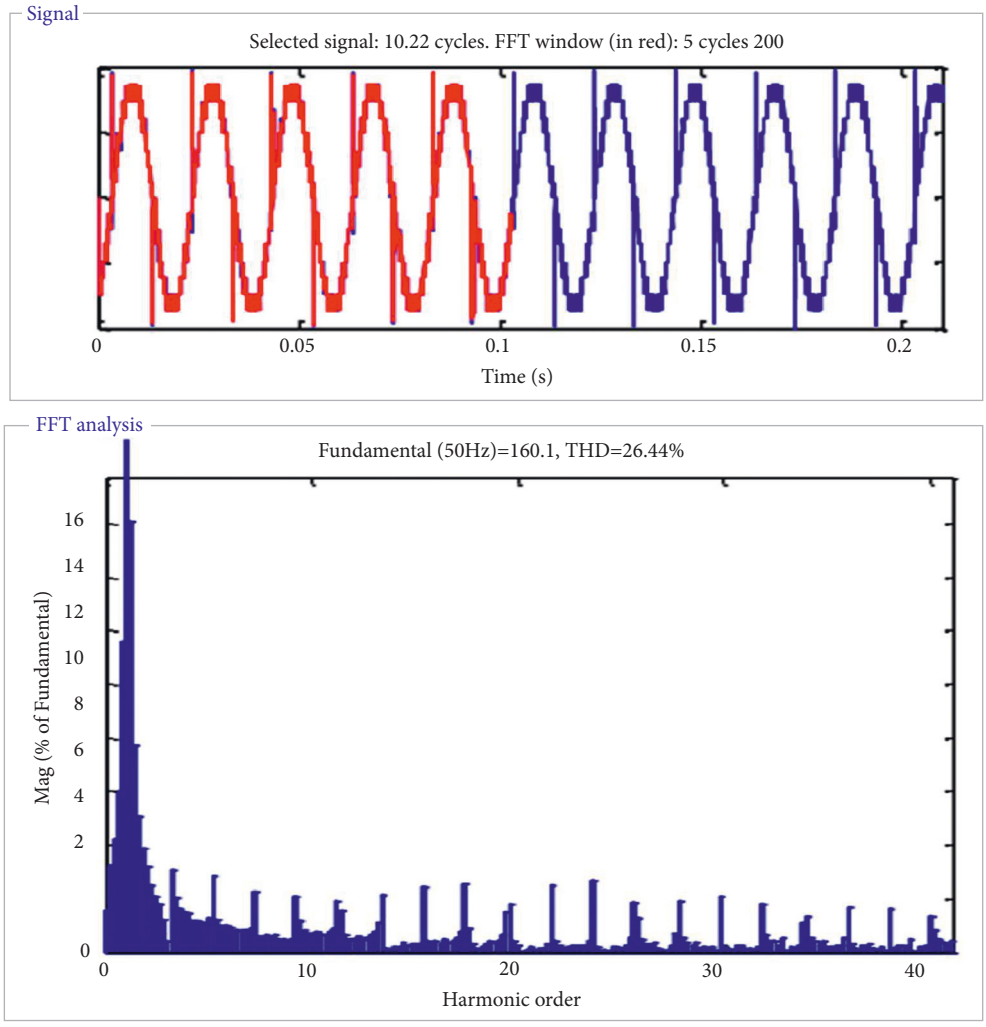
The virtual feedback system, three-phase output and current, phase output voltage, phase output current, and phase output voltage THD range of the planned fifteen-level boost cascaded multilevel inverter with the PI controller are seen in Figures 16–18. The Kp = 0.013008 and Ki = 36 for the PI controller were determined for the unbalanced nonlinear form of the proposed inverter configuration in this converter. In the PI controller, autotuning was allowed to change the value of Kp and Ki based on the feedback system's closed-loop response.

By comparing the previous and current tuned value of Kp and Ki, the output of the closed-loop feedback controller system to decrease harmonics and unbalanced between phase voltages was obtained. A stable system and lower rise time, peak overshoot, and settling time are needed for the target of the closed-loop PI controller system. The reference



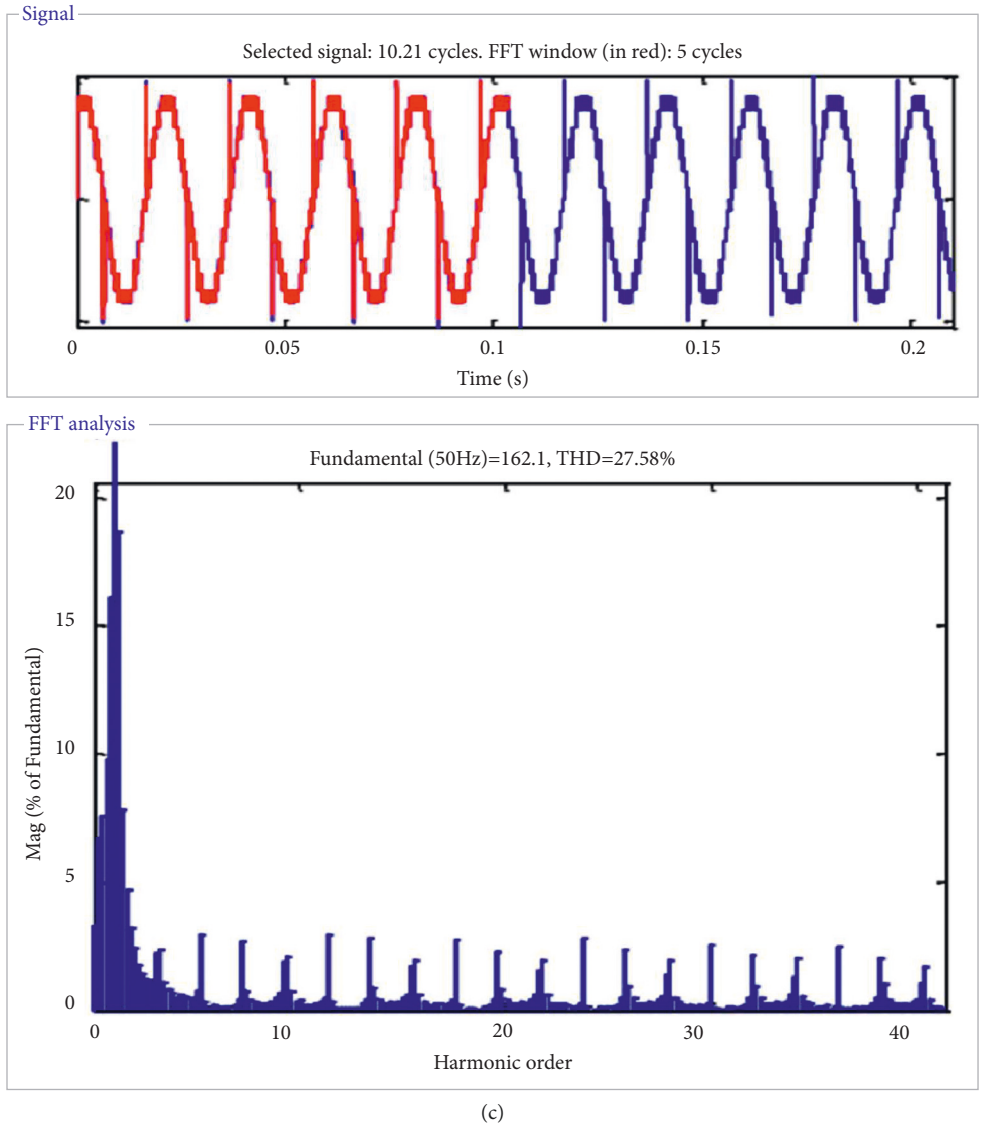
(a)

Figure 18: Continued.



(b)

Figure 18: Continued.



(c)

Figure 18: Harmonic analysis of phase output voltage phase (a) phase 'a', (b) phase 'b', (c) phase 'c'.

was tracked in Figure 8 with Kp = −12.9134 from −0.40133 and Ki −233865.3511 from −11065.9585. The rise time was fairly reduced from 0.000198 sec to 1.67e-05 sec and the settle time was also reduced from 0.000573 sec to 8.92e-05 secs. The reference tracking peak value is 3.74 percent, which is reduced by 5.38 percent. The tuned system reference tracking peak overshoot was reduced by 3.74 percent from 5.38 percent in this respect. Even though the overshoot and settling time were significantly reduced, the peak value is 1.04 from 1.05.

After this, Kp = 10.3256 and Ki = 19174.3203 were adjusted, and as seen in Figure 9, this provided a strong phase response. The reference tracking phase margin of the Bode plot is 171 and the lag margin is 0.000101 sec at the 29700 rad/sec frequency. Figure 10 shows the reference tracking phase margin of the Bode plot. The peak gain of the controller action is −20.3 db at a 1x sec frequency and the phase margin is −159 at 6730 rad/sec with a corresponding 0.000521 sec delay margin as seen in Figure 12. For any controller loop, the rejection of the input and output disturbance is sufficient to minimize the gap between the output to input ratio or to achieve the same as the output relation.

At 142 msec, the input interference of this peak amplitude system is 0.0751. The time of the production disruption raise is 117 msec and 191 msec is the settling time. The observation of input and output disturbance rejection from graph Figures 9–14 Kp = 10.3256 and Ki = 19174.3203 is accomplished with the shortest settling time to reduce the gap between the reference and output.

The output obtained via the inverter at the PI controller Kp = 10.3256 and Ki = 19174.3203 is explained in the following figures from Figures 17 and 18. Figures 17(a) and 17(b) are the three-phase output voltage and the waveform of the current. As opposed to control methods, the output voltage distortions were minimized. However, the output voltage involves major distortions in the quantity and has

(a) (b)

Figure 19: Output waveform for phase 'a' (a) voltage and (b) current.

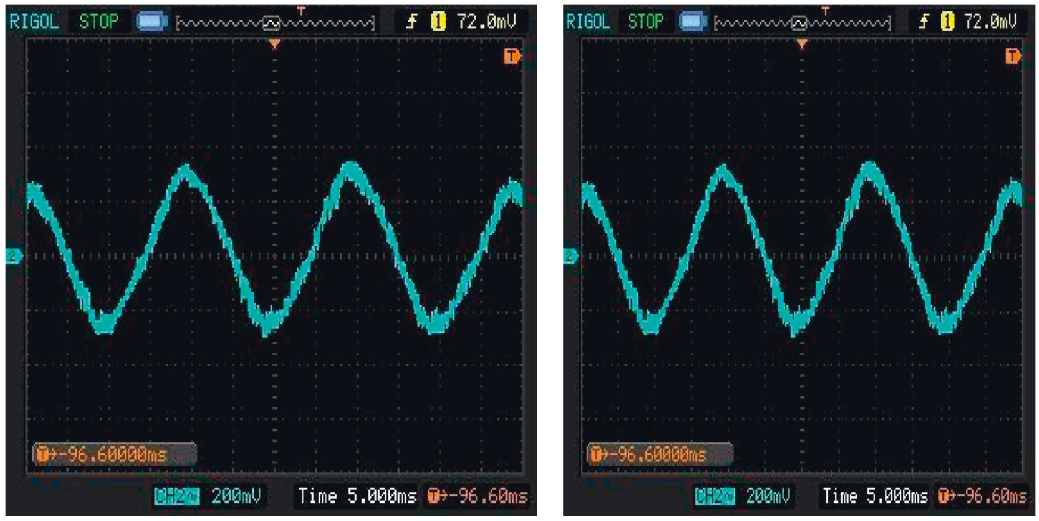
(a) (b)

Figure 20: Output waveform for phase 'b' (a) voltage and (b) current.

not been completely minimized in the waveform. The distortion in the output voltage waveform and the peak value is 163 volts, as seen in Figure 17(a).

Similarly, because of inductive reactance load and step "a", "b", and "c" are 0.96 Amps, 0.83 Amps, and 0.61 Amps, respectively, the output current harmonics were decreased in considerable amounts in Figure 17(b). Because of the nonlinear unbalanced load present, these loads smooth the current waveform and decrease the current harmonics.

Phases *a*, *b*, and *c* have a peak output voltage of 157.3 volts, 161.5 volts, and 150.7 volts are 25.2 percent, 26.44 percent, and 27.58 percent, respectively, in Figures 18(a)–18(c) and their equivalent output voltage proportion of gross harmonics distortion. The simple output voltage was increased and the harmonic portion was substantially reduced relative to the fifteen-level asymmetrical cascaded multilevel inverter without the controller. 153.4 volts, 160.1 volts, and 162.1 volts in phases "a", "b", and "c", respectively, are the first output voltages. In the inverter output phase terminals, the harmonic portion is due to the presence of neutral current or unbalanced voltage and current.



(a) (b)

Figure 21: Output waveform for phase 'c' (a) voltage and (b) current.

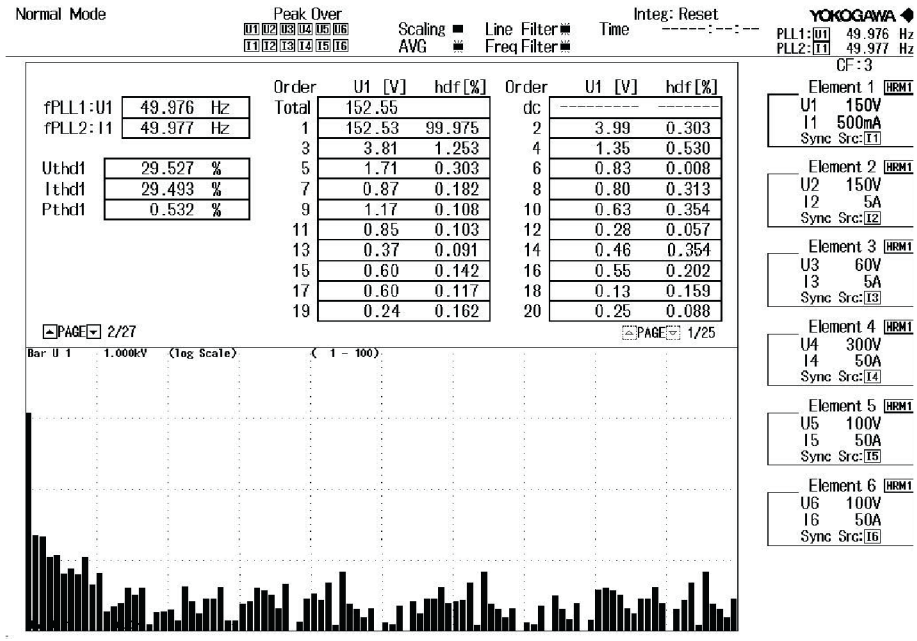


Figure 22: THD spectrum analysis of the phase output voltage.

3.2. Hardware Results. The simulated effects of the fifteen-level boost cascaded multilevel inverter with the PI controller were conducted experimentally to validate designed DC source parameters, nonlinear unbalanced load, and carrier frequency and inverter configuration with the same value.

In Figures 19–21, the inverter hardware phase output was given and the maximum output voltage of the inverter phase "a", "b", and "c" are 152 V, 157 V, and 160 V, respectively. Similarly, in Figures 19(a) and 21(a), the inverter is 0.76 amps, 0.9 amps, and 0.65 amps, respectively. The output voltages of an inverter are distortions that are smaller than those without the output voltage waveform controller, as seen in Figure 19(a). As seen in Figure 20(a), the simple output voltage of the inverter is increased to 152.55 volts. In Figure 22, the output voltage even and odd harmonic component magnitudes are shown, and in the same Figure 22, the estimated component range bar map up to the hundred orders is also presented. The effects of the simulated and hardware configuration are similar to significance, and this suggested scheme provided improved the performance compared to the experimental results without the technique of the controller. In the hardware performance, the THD was lowered by 29.527 percent, and as seen in Figure 22, the unbalanced phase voltage was also increased relative to the previous device. The proposed system did not generate less

than the normal THD value and allowed increased output in switching systems.

4. Conclusion

In this segment, with the lower count of power semiconductor switches and other supporting circuits, the three phase fifteen stage asymmetrical cascaded multilevel inverter with the PI controller was modeled. The output of the PI controller inverter due to unbalanced nonlinear loads has a higher percentage of harmonics. In order to restrict the harmonics and track the output as close as a comparison, PI controller feedback was introduced for this purpose. In order to regulate the voltage and the reference for generating the switching pulses of the inverter PWM, the inner current loops and outer voltage loops were planned. The line impedances are eliminated by cross-coupling the feed-forward loop of imaginary components. In simulation with nonlinear unbalanced loads, the built components are verified. The PI controller's simulated results minimized the steady-state error, peak overshoot, and settling time. In contrast with the open-loop operation of the proposed inverter, the non-linear unbalanced output voltage difference, and the harmonics were minimized. Around the same time, the proposed system did not yield lower THDs and did not conform to the THD limit norm.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] S. S. Lee, Y. Yang, Y. P. Siwakoti, and K.-B. Lee, "A novel boost cascaded multilevel inverter," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 9, pp. 8072–8080, 2021.

[2] R. Ravindran, C. R. Sathiasamuel, P. Ramasamy, and K. Balasubramanian, "MSVM-based hybrid energy-fed quasi-Z-source cascaded H-bridge inverter for grid-connected system," *Int Trans Electr Energ Syst*, vol. 31, no. 12, Article ID e13139, 2021.

[3] Yu Liu, H. Hong, and A. Q. Huang, "Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2249–2258, 2009.

[4] R. Ramkumar, M. V. Kumar, and D. Sivamani, "Fuzzy logic based soft switched active clamped boost converter charging strategy for electric vehicles," in *Proceedings of the 2020 4th International Conference on Electronics, Communication and Aerospace Technology (ICECA)*, pp. 1334–1339, Coimbatore, India, November 2020.

[5] A. Ajami, M. R. J. Oskuee, M. T. Khosroshahi, and A. Mokhberdoran, "Cascade-multi-cell multilevel converter with reduced number of switches," *IET Power Electronics*, vol. 7, no. 3, pp. 552–558, 2014.

[6] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "-voltage levels," *IET Power Electronics*, vol. 7, no. 1, pp. 96–104, 2014.

[7] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, vol. 52, no. 2, pp. 1114–1128, 2011.

[8] E. E. Espinosa, J. R. Espinoza, P. E. Melin et al., "A new modulation method for a 13-level asymmetric inverter toward minimum THD," *IEEE Transactions on Industry Applications*, vol. 50, no. 3, pp. 1924–1933, 2014.

[9] A.-V. Ho and T.-W. Chun, "Topology and modulation scheme for three-phase three-level modified Z-source neutral-point-clamped inverter," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11014–11025, 2019.

[10] A. Hota, S. Jain, and V. Agarwal, "An improved three-phase five-level inverter topology with reduced number of switching power devices," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3296–3305, 2018.

[11] A. Masaoud, H. W. Ping, S. Mekhilef, and A. Taallah, "-level inverter," *IET Power Electronics*, vol. 7, no. 12, pp. 3052–3061, 2014.

[12] Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Power balance optimization of cascaded H-bridge multilevel converters for large-scale photovoltaic integration," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1108–1120, 2016.

[13] Y. Nakagawa and H. Koizumi, "A boost-type nine-level switched capacitor inverter," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6522–6532, 2019.

[14] J. Liao, K. Corzine, and M. Ferdowsi, "A new control method for single-dc-source cascaded H-bridge multilevel converters using phase-shift modulation," in *Proceedings of the 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 886–890, Austin, TX, February 2008.

[15] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters-state of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010.

[16] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded h-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4399–4406, 2009.

[17] M. R. Gharib, "Comparison of robust optimal QFT controller with TFC and MFC controller in a multi-input multi-output system," *Reports in Mechanical Engineering*, vol. 1, no. 1, pp. 151–161, 2020.

[18] V. Dertimanis, E. Chatzi, and S. Masri, "On the active vibration control of nonlinear uncertain Structures," *Journal of Applied and Computational Mechanics*, vol. 7, pp. 1183–1197, 2021.

[19] L. Wang, Q. H. Wu, and W. Tang, "Novel cascaded switched-diode multilevel inverter for renewable energy integration," *IEEE Transactions on Energy Conversion*, vol. 32, no. 4, pp. 1574–1582, 2017.

[20] G. Xu, D. Chen, and A. Qu, "Simple boost modified space vector modulation strategy for three-phase quasi-z-source inverter," in *Proceedings of the IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, pp. 5365–5370, Singapore, October 2020.

[21] M. Mohseni and S. M. Islam, "A new vector-based hysteresis current control scheme for three-phase PWM voltage-source

inverters," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2299–2309, 2010.

[22] Y. He, Y. Xu, and J. Chen, "New space vector modulation strategies to reduce inductor current ripple of z-source inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2643–2654, 2018.

[23] J. Pereda and J. Dixon, "Cascaded multilevel converters: Optimal asymmetries and floating capacitor control," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4784–4793, 2013.

[24] M. R. V. Goutham and M. V. G. Rao, "Control of a three-phase cascaded h-bridge multilevel inverter for stand-alone PV system," *International Journal of Modern Engineering Research*, vol. 2, no. 2, pp. 278–282, 2012.