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Research Article

Design and Simulation of Multichannel Dynamic Measurement Control System

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The circuit system designed in this paper uses FPGA and single-chip microcomputer as the main chips. It uses VHDL language programming and performs functional simulation and verification of the core control program through ModelSim software, and finally, a storage-type dynamic measurement and control system with one-to-multiple channels, adjustable trigger modes, and optional sampling frequency is realized. At the same time, the system is further optimized in terms of power consumption and volume. The storage measurement and control system can successfully record eight-channel dynamic voltage signals, and the relative error of the experimental results is less than 2% through the simulation trigger experiment and Hopkinson bar experiment loading.

1. Introduction

In aerospace, military weapons, oil well fracturing, and other fields, some dynamic parameters of products need to be captured and tested to ensure the stable operation of products.

At present, domestic dynamic test systems often take CPLD as the main control chip, but it has problems such as old chip, large size, few test channels, easy to trigger by mistake, single sampling frequency, and high energy consumption. In this paper, a dynamic test system based on FPGA is designed to solve these problems.

The test instrument uses internal trigger, rigid fixed in the fuze, easy to adjust the mass of the full bomb, the center of mass. Tester size is small, lightweight. The instrument comes with power supply, no lead, easy to use, strong anti-interference ability, after the completion of the launch of the recovery tester, through the computer to read the test data and the special test software to reproduce a number of the parameters-time curve. Ballistic data recorder can resist high overload. The instrument works reliably at −20°C~55°C temperature.

Many weapon development units in the United States have developed test devices based on telemetry technology, such as the United States Army Ballistic Research Institute, Naval Weapons Research Institute, Aberdeen Range, whose test devices are used to test the information in the gun chamber. The telemetry system is divided into the transmitting part and the receiving part. The transmitting part is generally located in the chamber, which is composed of sensors and conditioning circuits, modulation circuits, transmitting antennas, batteries, etc. The receiving part is generally located outside the chamber and consists of the receiving antenna, demodulation circuit, amplification circuit, and recording and memory circuit. The transmitting part sends out the modulated information in the chamber, which is transmitted through the air. The receiving part demodulation and amplification of the modulated signal extract the information in the chamber and store the records.

Sandia National Laboratories of the United States has developed the ultrasmall penetration acceleration recorder, which has the characteristics of low-power consumption, small size, and lightweight. Its data recording state current is 100 mA, power is 1.5 W, data retention time is up to 60 days, and the weight of the recorder is 0.499 kg. It can be used to test uniaxial or triaxial acceleration in the process of penetration.

Storage testing technology can well solve the high temperature and high pressure, high impact, such as information retrieval problem under the bad environment, and storage test system has a resistance to bad environment, small volume, the characteristics of micropower consumption, but the tester based on the technology of storage test can only be read back the data by recycling, projectile, and tester of recycling also has larger uncertainty. And the storage tester cannot get real-time data, which is the disadvantage of the storage test. But with the continuous development of electronic technology, the storage test system will develop toward the direction of large capacity and intelligence and has a broad development space.

2. Hardware Design

Dynamic test system is mainly composed of power management module, analog signal conditioning circuit, multichannel selection circuit, analog-to-digital conversion circuit, memory, and interface circuit [1]. Table 1 shows dynamic test system technical index. The principle of dynamic test system is shown in Figure 1 in which the signal is sampled.

2.1. Volume and Power Consumption. The dynamic test system integrates sensors, circuits, and batteries into a $7 \times 3 \times 3$ cm cylindrical shell with high strength. Compared with the existing $9 \times 5 \times 5$ cm dynamic test system, it is more miniaturized. FPGA Cyclone IV is a chip of Altera Corporation, namely field programmable gate array, which is a semicustom circuit in the field of IC [2]. Compared with the previous generation of devices, the power consumption is 1/5, and the 1.8 V core voltage reduces power consumption and improves reliability. At the same time, micropower optimization has been carried out in terms of power management and memory.

2.2. Power Management. In view of the small size and micropower consumption, the dynamic test system needs to use power management chip to power digital circuit, analog circuit, and sensor separately. The power supply of each part is not affected by each other. When some part of the circuit is not needed to work, the power of the system is reduced to a large extent. In the design of the dynamic test system, the MAX667 model is selected as the power management chip. MAX667 is only a small package volume of 3 mm × 3 mm, occupying very little space in the system. When MAX667 does not output voltage, only 0.5 nA of current is consumed [3].

2.3. Analog Signal Conditioning Circuit. The analog signal generated by the sensor includes the measured dynamic parameter change information, the residual response of the sensor to the main excitation signal, the response of the sensor structure and assembly mode to the actual measured point, and various high-frequency interference noises [4]. In order to improve the measurement accuracy, a filter is generally used to filter out the high harmonics and high-frequency noise in the frequency domain. Compared with a passive filter, the active filter has the advantages of small volume, lightweight, and low energy consumption. Therefore, the system is designed to use an active low-pass filter to regulate the signal, with a cut-off frequency f of 30 kHz and an amplification factor K of about 1.6 times. A voltage follower is added in the rear stage to isolate the dynamic signal from the load by buffering. The analog signal which is determination of resistance and capacitance conditioning circuit is shown in Figure 2.

Table 1: Dynamic test system technical index.

Number of channels	8
Resolution	12 bit
Sampling frequency	50 kHz
Storage capacity	256 M
Recording time	5 min
Data retention time	More than 3 years
Operating temperature	−40°C~+55°C
Acceleration test range	±3000 g

$$
\begin{aligned}
R_1 &= R_2 = 2.65k\Omega, \\
R_3 &= 10k\Omega, \\
R_4 &= 16k\Omega, \\
C_1 &= C_2 = 4.7nf, \\
C_3 &= 0.1\mu f, \\
f &= \frac{1}{2\pi R_1 C_1} \\
&= \frac{1}{2\pi \times 2.65K\Omega \times 1nf} = 60kHz, \\
K &= 1 + \frac{R_4}{R_3} \\
&= 1 + \frac{16K}{10K} = 2.6.
\end{aligned}
\tag{1}
$$

2.4. Multichannel Selection Circuit and Analog-to-Digital Conversion Circuit. In this design, two MAX4634 gate switches are used. The address signals A0 and A1 inside the circuit are combined with chip selection signals MUX0 and MUX1 to generate channel selection signals. The enable and gate ends of the two gate switches are controlled by the program to realize the cyclic gating of the eight-channel dynamic test signal, and then, the cyclic sampling of the eight-channel dynamic test signal by A/D is realized [5]. The system clock is 16 M, and the A/D sampling frequency is 50 KHz. The A/D sampling frequency can be flexibly set through the program to divide the system clock. The analog-to-digital conversion circuit used in the dynamic test system is the 12 bit high-speed, low-power, successive

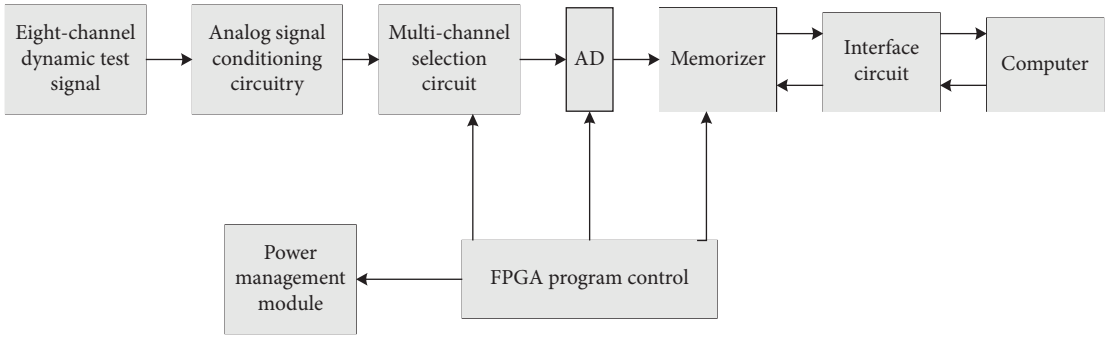

Figure 1: Dynamic test system principle block diagram.

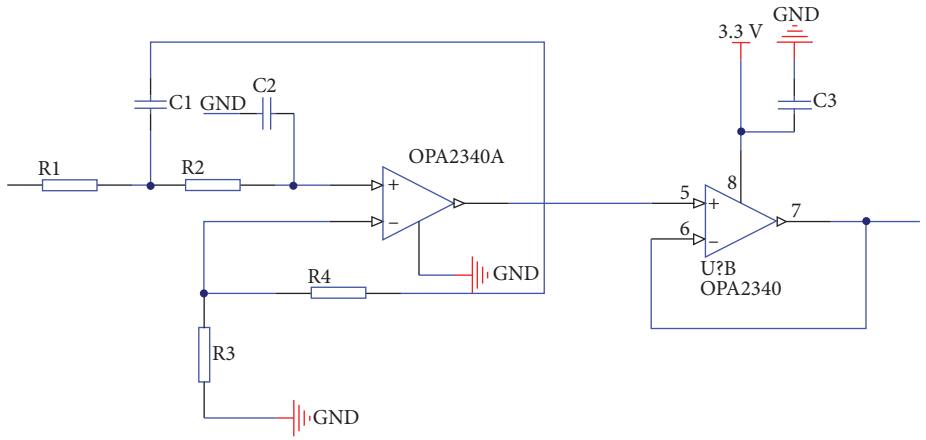

Figure 2: Analog signal conditioning circuit diagram.

approximation AD7492 with a maximum conversion rate of 1.25 Msps. It contains a low noise, wideband wide track/hold amplifier that can handle bandwidths up to 10 MHz. The A/D device begins conversion at the falling edge of the CONVST; at the same time, the BUSY signal is high; and at the end of the conversion, the BUSY signal becomes low. The analog-to-digital conversion circuit is shown in Figure 3.

2.5. Data Storage. Data storage uses a Samsung NAND Flash memory chip K9F1G08U0M. It has a storage capacity of 1056 Mbit and a block page structure that can be divided into 1024 blocks with a block size of 64 pages. Each page size is 2112 bytes. The I/O pins of the K9F1G08U0M have the function of multiplexing and can be used as the input and output ports of data and addresses, as well as the command input port. The connection of temporal logic between Flash and FPGA is shown in Figure 4.

When the trigger signal arrives, Flash starts to write data. When the set storage capacity reaches 256 MB, Flash stops writing [6]. In the low-power consumption state, only the power supply in the dormant state of master and slave controllers and memory is maintained, and the circuit that does not need to work stops the power supply, which greatly reduces the power consumption of the system. The Flash memory must erase data before each write and write data only once after erase. If the data are powered off due to insufficient power supply or other faults, the data that were

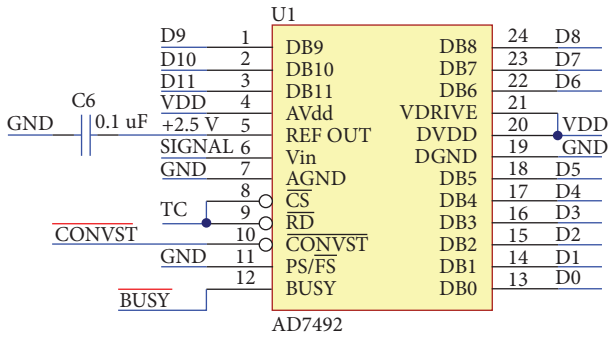

Figure 3: Schematic diagram of A/D conversion circuit.

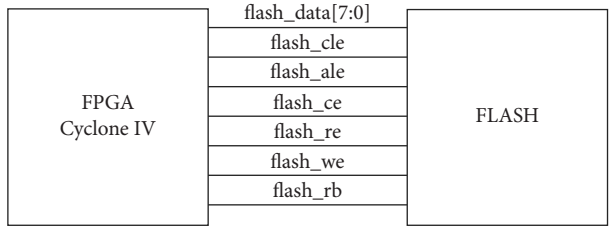

Figure 4: Connection mode between flash and FPGA.

not erased last time can still be read after the fault is removed and powered on again. Flash memory has good nonvolatile [7]. Because the test data in the Flash memory are very important, the data in the Flash memory can be erased only

by connecting the reading interface of the instrument with a special data line and entering the erasure command on the computer. If the power supply fails after the test, the tester can continue to use the method of external power supply, which has been verified in practice.

2.6. Communication Interface Circuit Design. Infrared data transmission is used to communicate between the test system and computer. The FPGA has an integrated codec that converts the asynchronous serial binary code to binary code. In order to realize the data transmission between the system and the host computer, there should be such a codec 3 which can realize the data code conversion at the receiving end. When data need to be read, the test system will store binary data through internal coding and send it through the infrared transceiver. At this time, the transceiver at the receiving end will send the received data to the codec. After decoding, the data will be sent to the USB interface conversion chip and transmitted to the computer through the USB2.0 interface. During circuit programming, the data to be programmed by the computer are sent to the converter chip through the USB2.0 interface, and the converter chip sends it to the codec encoding through the serial interface. After encoding, the data are sent to the test system through the infrared transceiver, and the test system finishes a data programming operation after decoding after receiving it from the transceiver.

3. Software Design

The control logic of FPGA is designed by Verilog language.

3.1. State Transition. The conversion process of FPGA is shown in Figure 5.

3.1.1. Waiting for Electrical Signal. Dynamic test system is waiting for the arrival of the electrical signal.

3.1.2. Cyclic Sampling State. After the dynamic test system is powered on, the upper computer will erase the internal data of the memory and enter the cyclic sampling state. When the trigger signal arrives, the dynamic test system will enter the sequential sampling state [8].

3.1.3. Sequential Sampling. The Flash starts to write data. When the Flash storage capacity reaches the preset capacity, the Flash stops writing data. The sequential sampling ends, and the Flash enters the low-power state.

3.1.4. Low-Power Consumption. At this time, the dynamic test system only needs to maintain the power supply of the master and slave controllers and the dormant state of the memory, and the circuit that does not need to work stops the power supply, which greatly reduces the power consumption of the system.

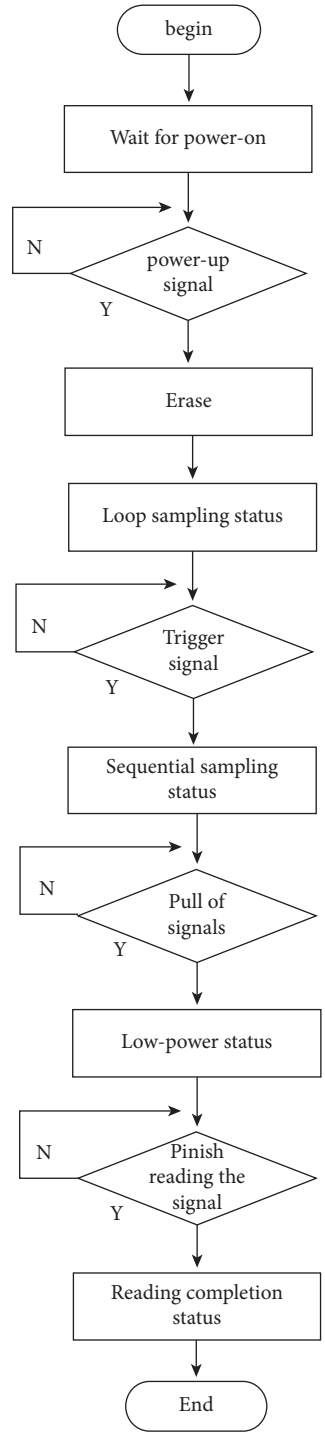

Figure 5: FPGA state conversion flow chart.

3.1.5. Reading Completion State. When the upper computer finishes reading the data inside the Flash memory of the dynamic test system, it enters the reading completion state. The data inside the Flash memory cannot be erased for the use of the next reading, or the internal data can be erased, and the system returns to the cyclic sampling state again.

3.2. Simulation. The FPGA program is simulated by ModelSim software.

3.2.1. Power Status Conversion. The system needs two voltage regulator chips MAX667, which output two voltages of 5 V and 3.3 V, respectively, for use by sensors of different power supply types. Meanwhile, 3.3 V also supplies power for the circuit of the dynamic test system [9]. The enablers of the two MAX667 chips are ONA and ONB, respectively. MAX667_A power-on and power-off use asynchronous zero-clearing D trigger; MAX667_B power-on and power-off use D trigger with asynchronous preset and asynchronous zeroing. M16 is the 16M system clock, TC is the reset, the count is the delay counter, SOFF is the global power-off, WOFF is the MAX667_B power-off, and ON and KRST are the MAX667_A and MAX667_B power-on, respectively. State conversion and simulation of power-on and power-off which is one input controls two outputs program are shown in Figures 6 and 7.

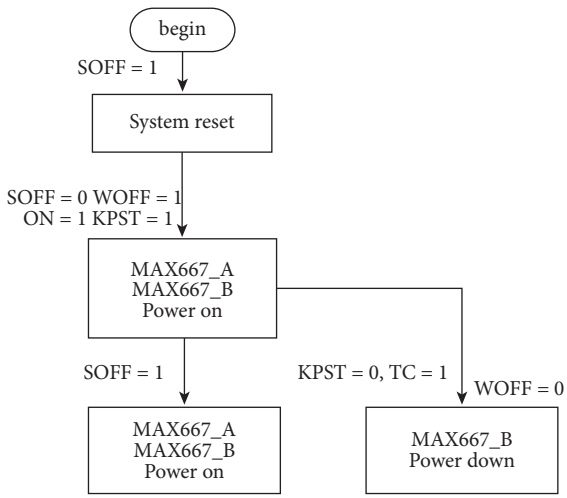

Figure 6: Power status conversion diagram.

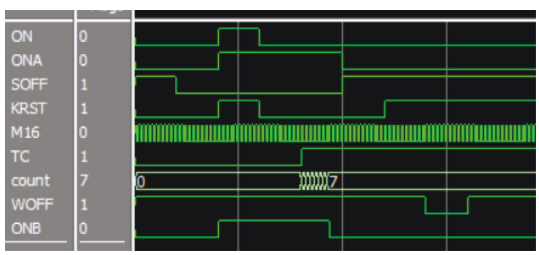

Figure 7: Power-on and power-off program simulation.

3.2.2. Multichannel Signal Gating and Sampling Frequency Selection. By program controlling the enable end (MUX1, MUX0) and the gate end (A1, A0) of the analog switch, the cycle gating of the eight-channel dynamic test signal is realized, and the cycle sampling of the eight-channel dynamic test signal is realized by A/D. Table 2 shows the gate truth values of multichannel signals. The system clock frequency is 16 MHz, and the system clock frequency can be divided by program, so that different sampling frequencies of 200 kHz (CONVST1), 100 kHz (CONVST2), and 50 kHz (CONVST3) can be flexibly selected to improve the experimental efficiency. Multichannel signal gating and system clock frequency division program simulation are shown in Figures 8 and 9. MCLR indicates low level reset, and ONB = 1 indicates the system is powered on. Count = count [10], MUX0 = !Count [10], A1 = count [11], A0 = count[0]. M16 represents 16M clock, and count 1, 2, and 3 represent 250 kHz, 100 kHz, and 50 kHz divider counters, respectively.

4. Trigger Mode

4.1. Internal Trigger. When the system is in the cyclic sampling state, the event that the signals collected exceeds the trigger threshold after AD conversion. Combination of multiple retrigger and internal trigger: when the system is in the cyclic sampling state, the event that the signals collected for several consecutive times exceeds the trigger threshold after AD conversion. This is a good way to prevent accidental triggering.

4.2. External Trigger. Trigger event is caused by a change in a physical quantity other than the measured signal. External trigger can detect whether the dynamic test system can record data normally at any time to improve the success rate of the test.

Table 2: Multichannel signal gating truth table.

Channel	Count	MUX1	MUX0	A1	A0
1	000	0	1	0	0
2	001	0	1	0	1
2	010	0	1	1	0
4	011	0	1	1	1
5	100	1	0	0	0
6	101	1	0	0	1
7	110	1	0	1	0
8	111	1	0	1	1

Trigger signal is the logical or of the external trigger signal and internal trigger signal. When port A is grounded, the external trigger signal is low, and the trigger signal is equivalent to the internal trigger signal [12]. When external triggering is required, disconnect port A from the ground. The potential of point A is 1.65 V, and the external triggering signal is high, and then, the triggering signal is generated. Internal and external trigger signal circuit is shown in Figure 10. The functions of internal penalty and external trigger have been verified.

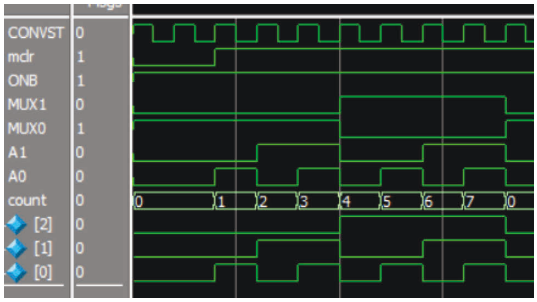

Figure 8: Simulation diagram of multi-channel signal gating program.

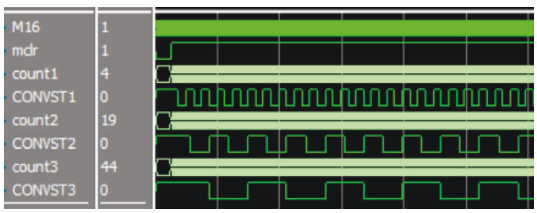

Figure 9: Simulation diagram of system clock frequency division program.

ADD1g5 is the high five bits of the test signal converted by AD, count is the eight-way test signal cycle counter, count 1 is the internal trigger comparison count, TR is the internal trigger signal, WCF is the external trigger signal, and NTR is the trigger signal. The simulation of the trigger signal program is shown in Figure 11.

5. Data Storage

NAND Flash has original bad blocks before delivery, and bad blocks are generated when it is used. However, bad blocks do not affect the function and normal use of Flash. Since the bad block information can be erased and new bad blocks will be generated in the process of use, the bad block information table in Flash should be detected and established before each use. The data corresponding to the column address 4096 in the first and second pages of each Flash selected in the design is not "FF," so as to establish or update the bad block information table. Before the normal operation of Flash, the system queries the established bad block list and covers the bad block by address mapping. The simulation of the detection timing sequence for bad blocks 01 and 02 is shown in Figure 12.

The Flash writes, reads, and erases data. For the write operation: it is necessary to write the initial instruction "80 h" in the reuse I/O, then write the address and data, and finally, write the end instruction "10H." In the design, because the write operation is completed continuously, the flow write operation mode controlled by the WE signal is selected. For read operations: similar to write operations, the start instruction "00H" is first written, then the address is written, and finally, the end instruction "30H" is written. For erasing: the start instruction is "60H," the address of the block to be erased is written, and the end instruction is

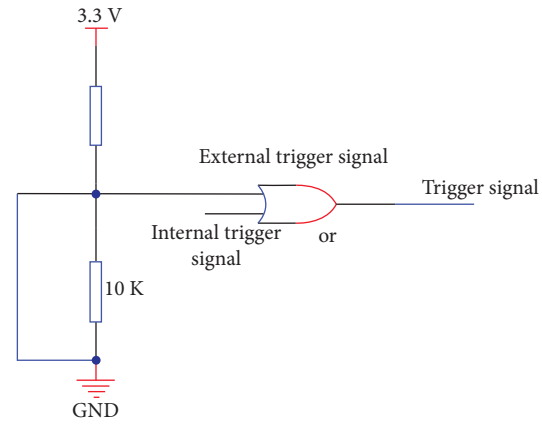

Figure 10: Trigger signal circuit diagram.

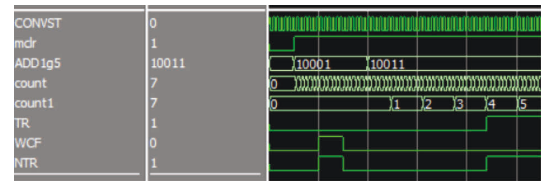

Figure 11: Simulation diagram of trigger signal program.

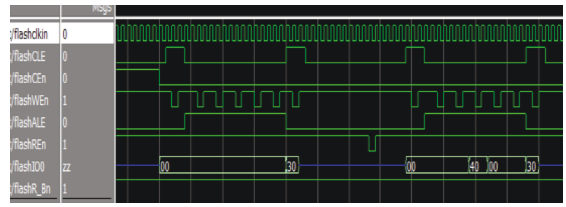

Figure 12: Timing sequence of bad block detection.

"D0H." The simulation of writing, reading, and erasing of Flash block 0 page 1 is shown in Figure 13.

6. Test

6.1. Simulated Trigger Experiment. The testing signal is the output of the signal generator simulating dynamically. The output of the signal generator 1 end of the sine wave by 1, 2, 3, 4 channels and the output of the signal generator 2 side for rectangular wave by 5, 6, 7, 8 channels adjust the trigger voltage amplitude of the signal generator to the system, the dynamic test system of signal acquisition, storage, transmission. Finally, it is displayed by the upper computer, and corresponding signals can be correctly displayed in all eight channels [13], as shown in Figure 14.

6.2. Hopkinson Bar Experiment. The Hopkinson bar was used to carry out the impact experiment on 11200 g acceleration to the piezoresistive acceleration sensor, and a trigger signal was generated [14]. The dynamic test system collects, stores, reads, and filters sensor signals, as shown in Figure 15. The relative error between the test

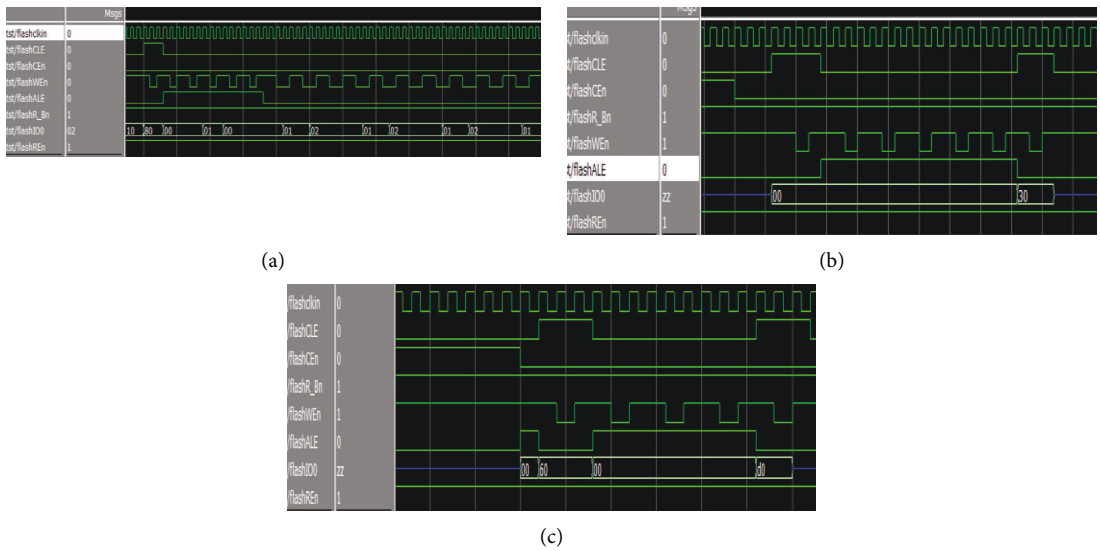

Figure 13: Flash write, read, erase simulation diagram (a) Writing of flash block 0 page 1; (b) Reading of flash block 0 page 1; (c) Erasing of flash block 0.

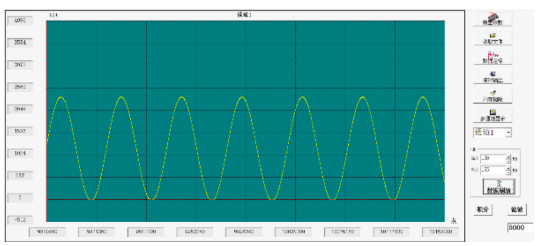

Figure 14: Eight-way signal test diagram.

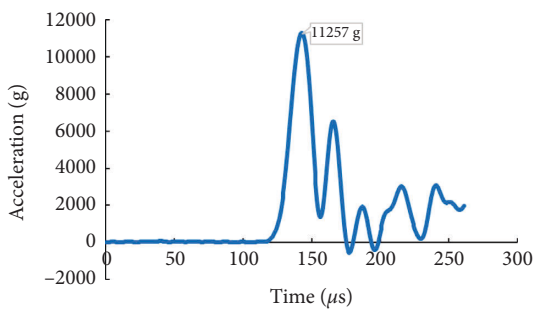

Figure 15: Acceleration test curve.

value of the dynamic test system and the actual value of 11257G is less than 1%. Generally, the relative error of the test system based on acceleration is less than 10%, so the test system meets the requirements of the dynamic test.

7. Conclusions

The circuit was redesigned to optimize volume and power consumption. Verilog language was used for programming, and ModelSim software was used for functional simulation of the program to realize eight-channel signal cycle switching, flexible selection of different sampling frequencies such as 50 kHz, 100 kHz, and 200 kHz, and a combination of multiple reset devices and internal and external triggers. The simulation trigger experiment and Hopkinson bar experiment are carried out on the dynamic test system. The system can accurately realize the signal conditioning, gating, acquisition, storage, and transmission of 8 channels. It solves the shortage of the existing dynamic test system and can be used in aerospace, military, instrumentation, and other fields. The disadvantage of this test instrument is that the proportional relationship between utilization and sensitivity needs to be verified by several tests [15].

Data Availability

The authors confirm that the data supporting the findings of this study are available within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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