Research Article

Design of an Optimized Asymmetric Multilevel Inverter with Reduced Components Using Newton-Raphson Method and Particle Swarm Optimization

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Multilevel inverters have great scope in current developments of grid-connected solar PV systems. Two-level inverters are the simplest kind of multilevel inverter available (MLI). As the number of output levels is raised, the total harmonic distortion decreases. In classic MLI topologies, more electronic components are utilized to get higher-level outputs, which raise the cost, complexity, and volume of typical MLI installations. By reducing the design components, the cost of the system will be reduced. Furthermore, the two- and three-level inverters produce constant dv/dt output, which increases the stress on the power switches. This research proposes an asymmetric MLI topology that is suitable for PV applications and utilizes less number of DC sources and switches. The proposed inverter is controlled by selective harmonic elimination-based pulse width modulation (SHEPWM) to eliminate the lower-order dominant harmonics. The nonlinear equations produced by the SHEPWM are solved for the switching angles of the proposed inverter using the Newton-Raphson (NR) method and particle swarm optimization (PSO) method for various modulation indexes. The performance of the proposed inverter is analyzed based on the total harmonic distortion (THD) of the output for different operating levels of the inverter by comparing similar topologies in the literature. The THD obtained by the NR method is 7.3% and by using PSO is 4.23% at 0.9 modulation index.

1. Introduction

Some common issues arise in the design of medium-voltage converter topologies for a wide range of applications including motor drives, solid-state transformers, and solar photovoltaic systems, including difficulties with high-power solar PV systems that make the control circuitry of the inverter more complicated. The initial development of the multilevel inverter theory was made in 1971 as a replacement for a set of linked power electronic switching devices used in medium-power applications [1]. During the 1971–1981 era, MLIs, such as neutral point clamped (NPC), a flying capacitor (FC), and cascaded H-bridge (CHB), were suggested [2]. The idea of a three-level NPC converter has acquired popularity as a result of its essential circuit design, and they are still available for purchase on the commercial market today. The increase in levels of neutral point clamped topology, on the other hand, results in a significant increase in the number of clamping diodes [3]. Taking use of the inverse retrieval times of the clamping diode, it is possible to
construct an inverter with more levels for medium-power applications using this design [4]. Hence, the neutral point clamped topology and the flying capacitor topologies are too inadequate for medium voltage (MV) and high voltage (HV) applications because they use many condensers requiring prior charging and balancing the capacitors [5, 6]. A large DC-link capacitor is required for single-cell design, which restricts its utility to high and medium voltages, notably in solar PV installations, where a large number of PV panels are connected in series [7]. Because a significant number of series-connected PV panels have equal maximum power point tracking (MPPT) and series resistance, the overall system efficiency will be lowered as a result of the low overall system efficiency [8, 9]. It is possible to operate MPPT at the module level due to the multilevel multilevel CHB converter design, which is adaptable to multiple voltage levels [10]. Furthermore, CHB topologies do not require the use of clamping diodes or capacitors [11, 12]. Partial shading and continuous module characteristics will produce mismatch issues [13]. These mismatches lead to network imbalance and lower power quality [14]. Utilizing CHB converters for PV applications presents a different set of challenges than using them in solid-state transformers or motor drives [15].

Multilevel inverters have made significant strides forward in recent times because of their ability to offer maximum power output at affordable costs [16]. By including the harmonic profile in the IEEE-519 standard, multilevel inverter topologies remove the requirement for massive filters [17]. Electric motors may be guaranteed by lowering THD, dv/dt stress, and common-mode voltages [18]. Multilevel inverters have fewer EMI issues than 2-level and 3-level inverters [19]. Cascading the basic units of the level generation part resulted in a higher output voltage and less THD [20]. The inverter finds applications in PV-fed UPS, propulsion systems, PV power integration, and battery-operated vehicles and needs a simple and direct control method [21]. Therefore, the researchers concentrated on topological construction and modulation [22].

The new architecture with 5 switches for 7 levels was introduced in an effort to reduce the switches as much as possible and the complexity to improve the cost of building circuits [23]. A new diamond-shaped multilevel inverter was developed in [24] by utilizing switched capacitors and DC voltage sources with dual-mode characteristics. This architecture has not redialed any H-bridge back circuit so voltage stress on the switches is lower and can easily be extended to higher levels with fewer switches. A hybrid topology has been proposed by combining 5 levels NPC with 3 levels T-type converter to generate 7 levels output for induction motor applications [25]. The architecture uses three floating capacitors per phase, which are balanced during the PWM switching period using switching-state redundancies for each pole voltage level. A back-to-back T-Connected hybrid multilevel inverter using the reduced switch configuration that generates an 11-level output has been developed by the authors of [26]. This architecture addressed two major drawbacks of traditional MLI topologies such as voltage strain and a larger number of design components. In order to reduce the number of switching components, especially when there are many different output voltage levels, a multilevel inverter containing a bidirectional diode has been introduced by the authors of [27]. This architecture has fewer semiconductor switches at the same number of output voltage levels than symmetric topologies which have recently and traditionally attempted to reduce the number of switches. This makes the proposed inverter a better choice for medium voltage applications such as electric motors and renewable energy systems. Two new topologies have been proposed by the authors of [28] to generate higher levels with a reduced number of switches. The first topology utilizes 3 DC sources and 10 switches to generate 15 levels of output. The second is an extension of the proposed architecture, which uses 4 DC sources and 12 switches to generate 25 levels of output. Structures reported in the literature have addressed several issues such as voltage stress and power losses. However, the use of capacitors in the design of MLIs creates voltage-balancing effects, and the use of diodes will lead to more reverse recovery times. Hence, there is a need to reduce the number of capacitors and diodes in the design of the multilevel inverters.

In this work, an asymmetric MLI with a low switch count was developed, which eliminated the requirement for bidirectional switches, capacitors, and more diodes in the design of the MLI. Due to the absence of bidirectional switches, the proposed topology had no influence on the reverse recovery times of the diode and voltage-balancing effect of input capacitors, and it makes use of a reduced gate control circuit to accomplish this [29–33]. The suggested inverter employs a SHEPWM control approach to suppress the lower-order harmonics [34, 35]. The Newton-Raphson (NR) method is a numerical computation method used to optimize the switching angles of the proposed inverter. Also, a swarm-based optimization called particle swarm optimization (PSO) algorithm had been employed on the proposed inverter to optimize the THD of the output. The suggested inverter operates at three distinct levels (seven levels, eleven levels, and fifteen levels), and the resulting total harmonic distortion has been studied.

2. Design of Asymmetric Multilevel Inverter

This study offered a simple architecture for an asymmetric inverter suited for varying dc sources, such as SPV systems, in its findings [20, 36]. Figure 1(a) depicts the proposed model’s basic cell layout. The bypass diode is coupled to a single voltage source through a power switch. \( V_{dc-out} \) becomes source voltage “\( V \)” when switch “\( S \)” is switched ON, and when switch “\( S \)” is switched OFF, source voltage “\( V \)” is separated from load, resulting in “0” for \( V_{dc-out} \).

To construct the inverter’s “\( n \)” cell structure, which is also referred to as the level generation part (primary circuit), basic cells are cascaded as illustrated in Figure 1(b). A multilevel output can only be generated with a positive bias in this “\( n \)” cell setup. Figure 1(c) shows a full-bridge inverter for the polarity generation part (auxiliary circuit). The proposed inverter was structured by the back-to-back interconnection of the level generation part and polarity generation part. Thus, a complete output cycle of positive
and negative polarity can be achieved by combining the primary and auxiliary circuits together. A polarity generator is similar to the H-bridge module and is used to generate 15 different output voltage levels, seven of which are positive, seven of which are negative, and one of which is zero.

Figure 2 depicts the structure of the proposed multilevel inverter with a 15-level output. This topology includes three dc sources, seven switches, and three diodes. Because of the suggested inverter and switching sequence selections, it is unlikely for IGBTs or diodes to die short circuits with the dc sources. The rating of a significant number of dc sources is determined by the magnitude of their output levels. The $V_{dc}$ step voltage at the output is specified by the dc source reduced voltage rating. Table 1 shows a variety of potential dc voltage source combinations.

The binary technique is one of the three options for dc source selection that are being evaluated for this investigation because multilevel inverters operate at great efficiency while experiencing minimal power losses and increased output voltage levels with the smallest number of devices. As a result, the following dc sources are recommended for 15-level output:

$$
V_1 = V_{dc}, \\
V_2 = 2V_{dc}, \\
V_3 = 4V_{dc}.
$$

As an added benefit, this technique offers asymmetrical operation to multilevel inverters, which is perfect for varying PV voltages caused by changing solar irradiation. For various output step voltages ranging from $+7V_{dc}$ to $-7V_{dc}$ including the “0” voltage level, the switching sequence is variable.

The auxiliary circuit switches $S_4$ and $S_1$ conduct for 7 levels of a +ve half cycle, whereas switches $S_8$ and $S_7$ conduct for 7 levels of a –ve half cycle. Short-circuiting the load with switches $S_4$ & $S_6$ on, or $S_8$ & $S_7$ on, yields the “0” output level. By operating the main and auxiliary circuits as per the switching paths indicated in Table 2, the proposed converter produces a fifteen-level output voltage.

The ON-OFF switching states of all seven switches and different operating modes of the proposed 15-level inverter are shown in Figure 3.

### 3. Comparative Analysis with Conventional Inverters

The core objective of a reduced switch multilevel inverter is to increase the number of levels while employing a few electronic components. Consequently, several contrasts were established among the suggested topology and other multilevel inverters of a similar kind, including switch count, the number of diodes, and dc sources.
Table 1: Selection of DC sources for the proposed inverter.

<table>
<thead>
<tr>
<th>Methods</th>
<th>DC sources selection</th>
<th>No of steps</th>
<th>No of levels</th>
<th>Output voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equal magnitude</td>
<td>$V_1 = V_2 = V_3 = V_{dc}$</td>
<td>4</td>
<td>7</td>
<td>$3V_{dc}$</td>
</tr>
<tr>
<td>Unequal magnitude</td>
<td>$V_1 = V_{dc}$, $V_2 = V_3 = 2V_{dc}$</td>
<td>6</td>
<td>11</td>
<td>$5V_{dc}$</td>
</tr>
<tr>
<td>Binary approach</td>
<td>$V_1 = V_{dc}$, $V_2 = 2V_{dc}$, $V_3 = 4V_{dc}$</td>
<td>8</td>
<td>15</td>
<td>$7V_{dc}$</td>
</tr>
</tbody>
</table>

Table 2: Modes of operations with switching patterns and power flow.

<table>
<thead>
<tr>
<th>Switch operations</th>
<th>Current paths</th>
<th>Load voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1, S_2, S_3, S_4 &amp; S_5$</td>
<td>$V_1 \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow \text{load} \rightarrow S_5 \rightarrow V_1$</td>
<td>$+7V_{dc}$</td>
</tr>
<tr>
<td>$S_2, S_3, S_4 &amp; S_5$</td>
<td>$V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow \text{load} \rightarrow S_5 \rightarrow D_1 \rightarrow V_2$</td>
<td>$+6V_{dc}$</td>
</tr>
<tr>
<td>$S_1, S_3, S_4 &amp; S_5$</td>
<td>$V_1 \rightarrow S_1 \rightarrow D_2 \rightarrow V_3 \rightarrow S_4 \rightarrow \text{load} \rightarrow S_5 \rightarrow V_1$</td>
<td>$+5V_{dc}$</td>
</tr>
<tr>
<td>$S_3, S_4 &amp; S_5$</td>
<td>$V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow \text{load} \rightarrow S_5 \rightarrow D_1 \rightarrow D_2 \rightarrow V_3$</td>
<td>$+4V_{dc}$</td>
</tr>
<tr>
<td>$S_1, S_2, S_4 &amp; S_5$</td>
<td>$V_1 \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow D_1 \rightarrow S_4 \rightarrow \text{load} \rightarrow S_5 \rightarrow V_1$</td>
<td>$+3V_{dc}$</td>
</tr>
<tr>
<td>$S_2, S_4 &amp; S_5$</td>
<td>$V_2 \rightarrow S_2 \rightarrow D_1 \rightarrow S_4 \rightarrow \text{load} \rightarrow S_5 \rightarrow D_1 \rightarrow V_2$</td>
<td>$+2V_{dc}$</td>
</tr>
<tr>
<td>$S_1, S_4 &amp; S_5$</td>
<td>$V_1 \rightarrow S_1 \rightarrow D_2 \rightarrow D_3 \rightarrow S_4 \rightarrow \text{load} \rightarrow S_5 \rightarrow V_1$</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>$S_4 &amp; S_6 (or) S_2 &amp; S_7$</td>
<td>$S_4 \rightarrow \text{load} \rightarrow S_6 \rightarrow S_7 \rightarrow \text{load} \rightarrow S_7 \rightarrow S_5$</td>
<td>0</td>
</tr>
<tr>
<td>$S_1, S_5 &amp; S_7$</td>
<td>$V_1 \rightarrow S_1 \rightarrow D_2 \rightarrow D_3 \rightarrow S_6 \rightarrow \text{load} \rightarrow S_7 \rightarrow V_1$</td>
<td>$-V_{dc}$</td>
</tr>
<tr>
<td>$S_2, S_6 &amp; S_7$</td>
<td>$V_2 \rightarrow S_2 \rightarrow D_3 \rightarrow S_6 \rightarrow \text{load} \rightarrow S_7 \rightarrow D_1 \rightarrow V_2$</td>
<td>$-2V_{dc}$</td>
</tr>
<tr>
<td>$S_1, S_2, S_6 &amp; S_7$</td>
<td>$V_1 \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow D_1 \rightarrow S_6 \rightarrow \text{load} \rightarrow S_7 \rightarrow V_1$</td>
<td>$-3V_{dc}$</td>
</tr>
<tr>
<td>$S_3, S_6 &amp; S_7$</td>
<td>$V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow \text{load} \rightarrow S_7 \rightarrow D_1 \rightarrow D_2 \rightarrow V_3$</td>
<td>$-4V_{dc}$</td>
</tr>
<tr>
<td>$S_1, S_3, S_6 &amp; S_7$</td>
<td>$V_1 \rightarrow S_1 \rightarrow D_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow \text{load} \rightarrow S_7 \rightarrow V_1$</td>
<td>$-5V_{dc}$</td>
</tr>
<tr>
<td>$S_2, S_3, S_6 &amp; S_7$</td>
<td>$V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow \text{load} \rightarrow S_7 \rightarrow D_1 \rightarrow V_2$</td>
<td>$-6V_{dc}$</td>
</tr>
<tr>
<td>$S_1, S_2, S_5, S_6 &amp; S_7$</td>
<td>$V_1 \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow \text{load} \rightarrow S_5 \rightarrow V_1$</td>
<td>$-7V_{dc}$</td>
</tr>
</tbody>
</table>

Figure 3: Continued.
Figure 4(a) provides a comparative analysis of the number of switches, sources, diodes, and capacitors required for various configurations referenced in this paper and the suggested topology. This contrast illustrates that the proposed topology is designed with fewer components. Different components required with respect to the number of levels are presented in Figure 4(b). Figure 5 shows the comparison between the number of switches, diodes, dc sources, and total standing voltages (TSV) of the proposed inverter with other topologies. Here, the comparisons were made with the recent topologies reported in the literature for analyzing the effectiveness of the proposed topology. From these comparisons, it is evident that the proposed topology utilizes less number of components than all other topologies.

4. Fundamental Switching Frequency Control (SHEPWM)

Multilevel inverters benefit from selective harmonic elimination, which is one of the most effective PWM control...
Figure 4: (a) Comparative analysis of proposed inverter with conventional inverters and (b) comparative analysis of components to levels ratio of proposed inverter with conventional inverters.

Figure 5: Comparative analysis of components required for the MLI topologies.
techniques available. Selective harmonic elimination pulse width modulation (SHEPWM) can be used to accomplish FSFC control. In most cases, the waveform of the output of an inverter is stated using the Fourier series expansion. In equation (2), the simplified expression of inverter output is represented in the following equation:

\[ V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t). \]  

where \( V_n = n^{th} \) harmonic and the quarter-odd wave’s symmetry makes the even harmonics zero. So \( V_n \) is given in equation (3) neglecting the even-order harmonics

\[ V_n = \begin{cases} \frac{4V_{dc}}{n\pi} \sum_{i=1}^{k} \cos(n\alpha_i) & \text{for odd values of } n'0; \text{ for even values of } n' \end{cases} \]  

where \( \alpha_i \) is the switching angles of \( i^{th} \) harmonic and is between \( 0^0–90^0 \) (i.e., \( 0 < \alpha_i < \pi/2 \)).

SHEPWM suppresses lower-order harmonics while harmonic filters eliminate the rest. The 5\text{th}, 7\text{th}, 11\text{th}, 13\text{th}, 17\text{th}, and 19\text{th} harmonic voltages were suppressed using a 15-level asymmetric inverter using SHEPWM control. Using 15-level output reduces bulky and costly filters by reducing the 5\text{th} to 19\text{th} harmonics. Equation (4) can be found by extending equation (3) for odd “\( n \)”.

\[
\begin{align*}
4V_{dc} \pi & \left[ \cos \alpha_1 + \cos \alpha_2 + \ldots \right. = V_1 \\
5V_{dc} \pi & \left[ \cos 5\alpha_1 + \cos 5\alpha_2 + \ldots \right. = V_5 \\
7V_{dc} \pi & \left[ \cos 7\alpha_1 + \cos 7\alpha_2 + \ldots \right. = V_7 \\
11V_{dc} \pi & \left[ \cos 11\alpha_1 + \cos 11\alpha_2 + \ldots \right. = V_{11} \\
13V_{dc} \pi & \left[ \cos 13\alpha_1 + \cos 13\alpha_2 + \ldots \right. = V_{13} \\
17V_{dc} \pi & \left[ \cos 17\alpha_1 + \cos 17\alpha_2 + \ldots \right. = V_{17} \\
19V_{dc} \pi & \left[ \cos 19\alpha_1 + \cos 19\alpha_2 + \ldots \right. = V_{19}
\end{align*}
\]

where \( V_5, V_7, V_{11}, V_{13}, V_{17}, V_{19} \) are the harmonic voltages of 5\text{th}, 7\text{th}, 11\text{th}, 13\text{th}, 17\text{th}, and 19\text{th} harmonics, respectively, and as a consequence, they are equal to zero, and the resultant could be given in equation (6). The 1\text{st} harmonic in equation (4) is equal to the modulation index, which may be represented as follows:

\[
M = \frac{V_1}{V_{1_{\max}}},
\]

where \( V_{1_{\max}} = \text{Peak fundamental voltage} = V_1 \) max = \( 4kV_{dc}/\pi \), \( V_1 = \text{Actual fundamental voltage} \), \( k = \text{Degree of freedom} m = (N - 1)/2, N = \text{No of levels} \)
Substituting equation (5) in equation (4), the transcendental equations for the 15-level inverter can be written in the following equations:

\[
\frac{4V_{dc}}{\pi} (\cos \alpha_1 + \cos \alpha_2 + \cos \alpha_3 + \cos \alpha_4 + \cos \alpha_5 + \cos \alpha_6 + \cos \alpha_7) = M
\]

\[
\frac{4V_{dc}}{5\pi} (\cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\alpha_3 + \cos 5\alpha_4 + \cos 5\alpha_5 + \cos 5\alpha_6 + \cos 5\alpha_7) = 0
\]

\[
\frac{4V_{dc}}{7\pi} (\cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\alpha_3 + \cos 7\alpha_4 + \cos 7\alpha_5 + \cos 7\alpha_6 + \cos 7\alpha_7) = 0
\]

\[
\frac{4V_{dc}}{11\pi} (\cos 11\alpha_1 + \cos 11\alpha_2 + \cos 11\alpha_3 + \cos 11\alpha_4 + \cos 11\alpha_5 + \cos 11\alpha_6 + \cos 11\alpha_7) = 0
\]

\[
\frac{4V_{dc}}{13\pi} (\cos 13\alpha_1 + \cos 13\alpha_2 + \cos 13\alpha_3 + \cos 13\alpha_4 + \cos 13\alpha_5 + \cos 13\alpha_6 + \cos 13\alpha_7) = 0
\]

\[
\frac{4V_{dc}}{17\pi} (\cos 17\alpha_1 + \cos 17\alpha_2 + \cos 17\alpha_3 + \cos 17\alpha_4 + \cos 17\alpha_5 + \cos 17\alpha_6 + \cos 17\alpha_7) = 0
\]

\[
\frac{4V_{dc}}{19\pi} (\cos 19\alpha_1 + \cos 19\alpha_2 + \cos 19\alpha_3 + \cos 19\alpha_4 + \cos 19\alpha_5 + \cos 19\alpha_6 + \cos 19\alpha_7) = 0
\]

The switching angles must not violate the constraints

\[
\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2}.
\]

(7)

Using constraint equation (7), it is possible to solve the set of nonlinear equations in (6) and derive the switching angles necessary for the fifteen-level inverter. It is possible to solve these equations with the use of the SHEPWM control method, as well as optimization approaches to optimize the inverter’s switching angles. An objective function that is associated with the variables to be analyzed is necessary for every optimization approach.

The output harmonic voltages are influenced by the switching angles of the inverter. When attempting to meet the aforementioned goals, the generalized harmonic voltage objective function (OF) takes on the following form:

\[
OF = \min_{\alpha} \left\{ \left( 100 + \frac{V_1^* - V_1}{V_1} \right)^4 + \sum_{k=2}^{N_h} \frac{1}{h_k} \left( 50 \cdot \frac{V_{kh}}{V_1} \right)^2 \right\}
\]

(8)

To minimize the 5th, 7th, 11th, 13th, 17th, and 19th harmonics, equation (8) could be expanded as follows:

\[
OF = 100 \times \left( \frac{V_1^* - V_1}{V_1} \right)^4 + \left( \frac{50}{V_1} \right)^2 \times \left( \frac{V_5^2}{5} + \frac{V_7^2}{7} + \frac{V_{11}^2}{11} + \frac{V_{13}^2}{13} + \frac{V_{17}^2}{17} + \frac{V_{19}^2}{19} \right)
\]

(9)

where \( V_{1d} \) = Desired fundamental voltage, \( V_1 \) = Actual fundamental voltage, \( V_5 \) = Harmonic voltage of 5th Harmonic, \( V_7 \) = Harmonic voltage of 7th harmonic, \( V_{11} \) = Harmonic voltage of 11th harmonic, \( V_{13} \) = Harmonic voltage of 13th harmonic, \( V_{17} \) = Harmonic voltage of 17th harmonic, \( V_{19} \) = Harmonic voltage of 19th harmonic.

The purpose of this study is to lower the total harmonic distortion (THD) by minimising the aforementioned objective function. The transcendental equation (6), which fulfil the constraint of equation (7) with the objective function (9), could be solved by utilizing the N-R technique for the proposed multilevel inverter to achieve the lowest total harmonic distortion (THD) and the best switching angles.

5. Results and Discussions

Seven IGBT switches, three switched diodes, and three DC sources are used to construct the suggested asymmetric inverter, which is implemented in MATLAB–Simulink. To produce the switching pulses, a pulse width modulation technique known as selective harmonic elimination has been used. Among other characteristics, the switching frequency is 50 Hz, the maximum harmonic frequency is 1 kHz, and the Nyquist frequency for total harmonic distortion is 5 kHz. The inverter’s load is modeled as a nonresistive load with \( R = 27 \Omega \) and \( L = 10 \text{mH} \). The nonlinear equations described in equation (6) have been solved by using the Newton-Raphson method and the particle swarm optimization
method for getting the switching angles of the proposed inverter. The switching angles are evaluated using SHEPWM at different modulation indexes, and the best THD is obtained at a 0.9 modulation index.

5.1. Computation of Switching Angles and Analysis of Results Using Newton-Raphson Method. The seven switching angles for seven switches in the inverter are first computed by a numerical successive approximation technique known as Newton-Raphson (N-R) approach [33]. The computation of switching angles involves equations (6) with (7). The step-by-step procedure followed in the N-R method for the solution of nonlinear equations is described as follows:

Step 1: For the calculation of switching angles, a matrix is formulated with seven (1–7) switching angles in equation (10) as follows:

\[
\mathbf{a}^T = [\alpha_1^0, \alpha_2^0, \alpha_3^0, \alpha_4^0, \alpha_5^0, \alpha_6^0, \alpha_7^0].
\]  

Equation (11) and the transpose matrix of its partial derivation concerning switching angles is given in equation (12).

\[
\frac{\partial F}{\partial \alpha}^T = \begin{bmatrix}
-\sin(\alpha_1^0) - \sin(5\alpha_2^0) - \sin(7\alpha_3^0) - \sin(11\alpha_4^0) - \sin(13\alpha_5^0) - \sin(17\alpha_6^0) - \sin(19\alpha_7^0) \\
-\sin(\alpha_2^0) - \sin(5\alpha_3^0) - \sin(7\alpha_4^0) - \sin(11\alpha_5^0) - \sin(13\alpha_6^0) - \sin(17\alpha_7^0) - \sin(19\alpha_7^0) \\
-\sin(\alpha_3^0) - \sin(5\alpha_4^0) - \sin(7\alpha_5^0) - \sin(11\alpha_6^0) - \sin(13\alpha_7^0) - \sin(17\alpha_7^0) - \sin(19\alpha_7^0) \\
-\sin(\alpha_4^0) - \sin(5\alpha_5^0) - \sin(7\alpha_6^0) - \sin(11\alpha_7^0) - \sin(13\alpha_7^0) - \sin(17\alpha_7^0) - \sin(19\alpha_7^0) \\
-\sin(\alpha_5^0) - \sin(5\alpha_6^0) - \sin(7\alpha_7^0) - \sin(11\alpha_7^0) - \sin(13\alpha_7^0) - \sin(17\alpha_7^0) - \sin(19\alpha_7^0) \\
-\sin(\alpha_6^0) - \sin(5\alpha_7^0) - \sin(7\alpha_7^0) - \sin(11\alpha_7^0) - \sin(13\alpha_7^0) - \sin(17\alpha_7^0) - \sin(19\alpha_7^0) \\
-\sin(\alpha_7^0) - \sin(5\alpha_7^0) - \sin(7\alpha_7^0) - \sin(11\alpha_7^0) - \sin(13\alpha_7^0) - \sin(17\alpha_7^0) - \sin(19\alpha_7^0)
\end{bmatrix}
\]  

Step 2: This step involves the design equations of the N-R approach from the following equations (16) to (19)

\[
F(\mathbf{a}^0) = F^0.
\]  

Equation (14) is linearized to get the \( \mathbf{a}^0 \)

\[
F^0 + \left[ \frac{\partial F}{\partial \mathbf{a}} \right] \mathbf{a}^0 = \mathbf{T},
\]

and

\[
\mathbf{a}^0 = [d\alpha_1^0, d\alpha_2^0, d\alpha_3^0, d\alpha_4^0, d\alpha_5^0, d\alpha_6^0, d\alpha_7^0].
\]

Equation (18) can be solved using the inverse of the equation represented in the following form:
5.1.1. Equal Magnitude of dc Sources. Considering the input dc sources as the ratio of 1:1:1, i.e., all the dc sources with equal magnitude, a seven-level output voltage is produced at the inverter output. The magnitudes of the dc sources are assumed as \( V_1 = 37 \text{ V}, V_2 = 37 \text{ V}, \) and \( V_3 = 37 \text{ V}, \) resulting in a peak voltage of 111 V. Figure 6 depicts the switching pulses generated by the proposed inverter’s seven-level operation. Figure 7 depicts the 7-level output voltage waveform of the proposed inverter with equal magnitude dc sources, and Figure 8 depicts the corresponding THD of the 7-level output of the proposed inverter, which is 15.36%.

5.1.2. Unequal Magnitude of dc Sources. Considering the input dc sources as the ratio of 1:2:4, i.e., the dc sources with unequal magnitude, an eleven-level output voltage is generated by the proposed inverter’s seven-level operation. Figure 9 depicts the 11-level output voltage waveform of the proposed inverter with unequal magnitude dc sources, and Figure 10 shows the 11-level output voltage waveform of the eleven-level output of the proposed inverter, which is 19%.

5.1.3. Binary Approach of DC Sources. Considering the input dc sources as the ratio of 1:2:4, i.e., the dc source magnitudes are different from one to another, a fifteen-level output voltage is produced at the inverter output. Here, the magnitude of dc sources is taken as \( V_1 = 37 \text{ V}, V_2 = 74 \text{ V}, \) and \( V_3 = 74 \text{ V} \) to get a peak voltage of 185 V. The switching pulses of the eleven-level operation of the proposed inverter are shown in Figure 9. Figure 10 shows the 11-level output voltage waveform of the proposed inverter with an unequal magnitude of dc sources. Figure 11 shows the corresponding THD of the 11-level output of the proposed inverter, which is 11.17%.

5.2. Computation of Switching Angles and Analysis of Results Using Particle Swarm Optimization. PSO is defining swarm’s sociological behavior. Each particle’s PSO vectors are \( 1 \times N \) and the vector of each particle. The best individual location in an identified particle is the local best, and the best position in the whole swarm is the global best. PSO is ideally suited to solving complex problems due to its low computation effort and quick computer coding. Initial values such as other traditional iterative methods are not required for PSO. In the following steps, the PSO mechanism is articulated:

**Step 1:** Initialize the parameters of particle vectors \( x_i \), \( V_o \), \( P_{best} \), \( G_{best} \) and inertia weight of the particle \( C_0 \). Choose the number of generations as 200 and the size of the population as 50, and every particle is randomly initialized as switching angles between 0° and 90°.

**Step 2:** Test the conditions for \( (C_1 + C_2)/2 < C_0 < 1 \). The system would then be guaranteed to converge to a stable equilibrium if the two criteria were met. If false, go to Step 1.

**Step 3:** The new position and velocity vectors of particles were determined using the following equation:

\[
\begin{align*}
\dot{x}_i(t + 1) & = \dot{v}_i(t) + C_{out}.rand1, \\
\dot{v}_i(t) & = \left( \dot{P}_i - \dot{x}_i(t) \right) + C_{acc}.rand2 \left( G^i - \dot{x}_i(t) \right).
\end{align*}
\]

(21)

Then, the new position is defined as follows:

\[
\dot{x}_i(t + 1) = \dot{x}_i(t) + \dot{v}_i(t + 1).
\]

(22)

**Step 4:** Evaluate the objective function of the particles using equation (23) to find the switching angles (1 to 7), such that the harmonics of the 5th, 7th, 11th, 13th, 17th, and 19th harmonics are eliminated at the inverter output.

\[
OF = \min_{\alpha} \left\{ \left[ \left( 100 \times \frac{V^* - V}{V^*} \right)^4 \right] + \sum_{k=5}^N \frac{1}{k!} \left( \frac{50 \times V_k}{V_1} \right)^2 \right\}.
\]

(23)

**Step 5:** Check for the constraint of the objective function as

\[
\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2}.
\]

(24)
Figure 6: Switching pulses of proposed inverter for seven-level operation: (a) primary circuit and (b) auxiliary circuits using NR method.

Figure 7: 7-Level output voltage of the asymmetric inverter.

Figure 8: THD of output voltage for 7-level operation.

Figure 9: Switching pulses of proposed inverter for eleven-level operation: (a) primary circuits and (b) auxiliary circuits using NR method.
Figure 10: 11-Level output voltage of the asymmetric inverter.

Figure 11: THD of output voltage for 11-level operation.

Table 3: Switching angles and THD of output voltage with the variation of modulation index using the Newton-Raphson method.

<table>
<thead>
<tr>
<th>S. no</th>
<th>$M_i$</th>
<th>$\alpha_1$</th>
<th>$\alpha_2$</th>
<th>$\alpha_3$</th>
<th>$\alpha_4$</th>
<th>$\alpha_5$</th>
<th>$\alpha_6$</th>
<th>$\alpha_7$</th>
<th>%THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5</td>
<td>6.32°</td>
<td>13.71°</td>
<td>23.56°</td>
<td>36.3°</td>
<td>49.42°</td>
<td>58.8°</td>
<td>67.3°</td>
<td>14.42</td>
</tr>
<tr>
<td>2</td>
<td>0.55</td>
<td>6.54°</td>
<td>12.51°</td>
<td>23.58°</td>
<td>35.78°</td>
<td>46.32°</td>
<td>57.1°</td>
<td>66.8°</td>
<td>12.85</td>
</tr>
<tr>
<td>3</td>
<td>0.6</td>
<td>6.31°</td>
<td>12.16°</td>
<td>23.31°</td>
<td>37.4°</td>
<td>45.76°</td>
<td>55.7°</td>
<td>65.8°</td>
<td>11.37</td>
</tr>
<tr>
<td>4</td>
<td>0.65</td>
<td>5.82°</td>
<td>12.11°</td>
<td>22.56°</td>
<td>36.57°</td>
<td>45.91°</td>
<td>54.32°</td>
<td>65.57°</td>
<td>10.28</td>
</tr>
<tr>
<td>5</td>
<td>0.7</td>
<td>5.78°</td>
<td>12.16°</td>
<td>22.35°</td>
<td>37.61°</td>
<td>46.24°</td>
<td>55.12°</td>
<td>65.36°</td>
<td>9.27</td>
</tr>
<tr>
<td>6</td>
<td>0.75</td>
<td>5.82°</td>
<td>12.12°</td>
<td>22.93°</td>
<td>37.34°</td>
<td>46.46°</td>
<td>55.78°</td>
<td>64.21°</td>
<td>8.83</td>
</tr>
<tr>
<td>7</td>
<td>0.8</td>
<td>5.78°</td>
<td>11.91°</td>
<td>22.48°</td>
<td>36.67°</td>
<td>45.38°</td>
<td>55.67°</td>
<td>63.7°</td>
<td>8.17</td>
</tr>
<tr>
<td>8</td>
<td>0.85</td>
<td>5.91°</td>
<td>11.22°</td>
<td>20.53°</td>
<td>31.26°</td>
<td>40.36°</td>
<td>51.78°</td>
<td>62.32°</td>
<td>7.45</td>
</tr>
<tr>
<td>9</td>
<td>0.9</td>
<td>5.61°</td>
<td>10.93°</td>
<td>18.62°</td>
<td>26.54°</td>
<td>34.82°</td>
<td>44.62°</td>
<td>61.21°</td>
<td>7.30</td>
</tr>
<tr>
<td>10</td>
<td>0.95</td>
<td>5.92°</td>
<td>11.05°</td>
<td>19.21°</td>
<td>26.23°</td>
<td>34.39°</td>
<td>46.48°</td>
<td>62.92°</td>
<td>7.41</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>5.06°</td>
<td>12.32°</td>
<td>22.3°</td>
<td>36.5°</td>
<td>44.27°</td>
<td>55.8°</td>
<td>65.23°</td>
<td>7.49</td>
</tr>
</tbody>
</table>

Figure 12: Switching pulses of proposed inverter for 15-level operation: (a) primary circuits and (b) auxiliary circuits using the NR method.
**Figure 13:** 15-level output voltage of the asymmetric inverter.

**Figure 14:** 15-level output current of the asymmetric inverter.

**Figure 15:** THD of the output voltage of the proposed inverter for 15-level operation.

**Figure 16:** Control methodology of proposed MLI using PSO algorithm.
Table 4: Switching angles and THD of output voltage with the variation of modulation index using PSO for 15-level operation.

<table>
<thead>
<tr>
<th>S. No</th>
<th>(M_i)</th>
<th>(\alpha_1)</th>
<th>(\alpha_2)</th>
<th>(\alpha_3)</th>
<th>(\alpha_4)</th>
<th>(\alpha_5)</th>
<th>(\alpha_6)</th>
<th>(\alpha_7)</th>
<th>%THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5</td>
<td>5.48°</td>
<td>12.78°</td>
<td>21.86°</td>
<td>35.4°</td>
<td>47.42°</td>
<td>56.8°</td>
<td>64.3°</td>
<td>9.42</td>
</tr>
<tr>
<td>2</td>
<td>0.55</td>
<td>5.34°</td>
<td>11.56°</td>
<td>23.61°</td>
<td>36.3°</td>
<td>45.32°</td>
<td>56.1°</td>
<td>62.8°</td>
<td>7.85</td>
</tr>
<tr>
<td>3</td>
<td>0.6</td>
<td>5.21°</td>
<td>10.76°</td>
<td>22.36°</td>
<td>37.4°</td>
<td>45.76°</td>
<td>54.7°</td>
<td>63.8°</td>
<td>7.37</td>
</tr>
<tr>
<td>4</td>
<td>0.65</td>
<td>4.88°</td>
<td>11.21°</td>
<td>21.56°</td>
<td>36.56°</td>
<td>44.91°</td>
<td>55.32°</td>
<td>64.5°</td>
<td>7.28</td>
</tr>
<tr>
<td>5</td>
<td>0.7</td>
<td>4.59°</td>
<td>11.56°</td>
<td>22.35°</td>
<td>37.61°</td>
<td>43.24°</td>
<td>56.12°</td>
<td>65.32°</td>
<td>7.27</td>
</tr>
<tr>
<td>6</td>
<td>0.75</td>
<td>4.36°</td>
<td>12.32°</td>
<td>22.93°</td>
<td>36.34°</td>
<td>41.46°</td>
<td>56.78°</td>
<td>64.21°</td>
<td>6.8</td>
</tr>
<tr>
<td>7</td>
<td>0.8</td>
<td>4.19°</td>
<td>11.98°</td>
<td>20.68°</td>
<td>35.67°</td>
<td>42.38°</td>
<td>54.67°</td>
<td>65.7°</td>
<td>5.5</td>
</tr>
<tr>
<td>8</td>
<td>0.85</td>
<td>4.03°</td>
<td>12.2°</td>
<td>21.56°</td>
<td>31.26°</td>
<td>42.36°</td>
<td>53.67°</td>
<td>64.32°</td>
<td>5.19</td>
</tr>
<tr>
<td>9</td>
<td>0.9</td>
<td>3.9°</td>
<td>12.1°</td>
<td>20.9°</td>
<td>29.9°</td>
<td>38.1°</td>
<td>48.7°</td>
<td>61.1°</td>
<td>4.23</td>
</tr>
<tr>
<td>10</td>
<td>0.95</td>
<td>4.23°</td>
<td>12.18°</td>
<td>19.16°</td>
<td>28.91°</td>
<td>41.2°</td>
<td>51.72°</td>
<td>62.3°</td>
<td>5.17</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>4.41°</td>
<td>12.32°</td>
<td>22.2°</td>
<td>31.52°</td>
<td>42.7°</td>
<td>52.8°</td>
<td>63.23°</td>
<td>5.30</td>
</tr>
</tbody>
</table>

Figure 17: Convergence characteristics using PSO algorithm.

Figure 18: Switching pulses of proposed inverter for 15-level operation: (a) primary circuits and (b) auxiliary circuits using PSO.
Step 6: Check for $P(X_i) < P(P_i)$, if not then $i = i + 1$ go to step 3.

Step 7: Update the particle’s best local position if the best local position is better than before. Thus, replaces the local best position.

Step 8: $P_g = \min (P_{\text{neighbor}})$.

Step 9: Termination criteria for a maximum of 200 iterations and terminate the process if the optimal switching angles are achieved.

Figure 16 illustrates the control methodology for the proposed inverter. Here, the inverter is controlled by optimal switching angles. The optimal switching angles of the MLI are obtained by synthesizing the inverter’s output into Fourier series representation, as shown in equation (3). This equation is further expanded in terms of the switching angles of the inverter as given in equation (4). Additionally, the nonlinear transcendental equations were formulated by considering the harmonics to be minimized, as shown in equation (6).

Using Simulink’s solver, the particle swarm optimization (PSO) is used to find the best possible switching angles based on the objective function given in equation (9). The fundamental output voltage equation is assigned with modulation index, which is obtained from the dc-link control. The solutions of the nonlinear equations are stored in lookup tables. Then, the switching angles decoder decodes the firing angles of the corresponding switch and produces the pulse related to the corresponding switching angle.

The switching angles for each modulation index are computed offline and stored in lookup tables. The switching angles for the modulation index from 0.5 to 1 were determined using the PSO algorithm and tabulated in Table 4. The corresponding THD of output voltage for all of these modulation indexes is calculated and found to be the minimum (4.23%) at 0.9 modulation index. The PSO takes 114 iterations to converge.
<table>
<thead>
<tr>
<th>Author</th>
<th>Inverter</th>
<th>Algorithm</th>
<th>No of sources</th>
<th>No of switches</th>
<th>No of levels</th>
<th>Max. O/p voltage</th>
<th>%THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zeng et al. [29]</td>
<td>K-type unit MLI</td>
<td>Fundamental frequency control (SHEPWM)</td>
<td>1</td>
<td>12</td>
<td>13</td>
<td>6Vdc</td>
<td>5.3%</td>
</tr>
<tr>
<td>Meraj et al. [33]</td>
<td>Cross-switched MLI</td>
<td>Newton-Raphson method (SHEPWM)</td>
<td>2</td>
<td>6</td>
<td>7</td>
<td>3Vdc</td>
<td>12.04%</td>
</tr>
<tr>
<td>Dhanamjayulu1</td>
<td>Cascaded MLI</td>
<td>Carrier-based PWM</td>
<td>4</td>
<td>12</td>
<td>31</td>
<td>15Vdc</td>
<td>3.34%</td>
</tr>
<tr>
<td>Meraj et al. [31]</td>
<td>PSMLI</td>
<td>Nearest level control technique (SHEPWM)</td>
<td>2</td>
<td>10</td>
<td>9</td>
<td>4Vdc</td>
<td>9.9%</td>
</tr>
<tr>
<td>Meraj et al. [30]</td>
<td>PSMLI</td>
<td>Nearest level control technique (SHEPWM)</td>
<td>4</td>
<td>20</td>
<td>17</td>
<td>8Vdc</td>
<td>5.15%</td>
</tr>
<tr>
<td>Meraj et al. [24]</td>
<td>Diamond-shaped MLI</td>
<td>Sine pulse modulation technique</td>
<td>1</td>
<td>11</td>
<td>15</td>
<td>7Vdc</td>
<td>3.36%</td>
</tr>
<tr>
<td>Hosseinpour et al. [27]</td>
<td>Symmetric topology</td>
<td>LS PWM</td>
<td>5</td>
<td>8</td>
<td>15</td>
<td>7Vdc</td>
<td>6.87%</td>
</tr>
<tr>
<td>Vanaja et al. [37]</td>
<td>Asymmetric topology</td>
<td>Nearest level control technique (SHEPWM)</td>
<td>3</td>
<td>8</td>
<td>15</td>
<td>7Vdc</td>
<td>4.31%</td>
</tr>
<tr>
<td>Fahad et al. [38]</td>
<td>Asymmetric topology</td>
<td>Nearest level control technique (SHEPWM)</td>
<td>4</td>
<td>11</td>
<td>15</td>
<td>7Vdc</td>
<td>5.5%</td>
</tr>
<tr>
<td>Azad and Kumar [39]</td>
<td>Symmetric topology</td>
<td>Genetic algorithm (SHEPWM)</td>
<td>3</td>
<td>7</td>
<td>15</td>
<td>7Vdc</td>
<td>4.36%</td>
</tr>
<tr>
<td>Proposed</td>
<td>Asymmetric modular multilevel inverter</td>
<td>Newton-Raphson method (SHEPWM)</td>
<td>3</td>
<td>7</td>
<td>11</td>
<td>5Vdc</td>
<td>11.17%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Particle swarm optimization (SHEPWM)</td>
<td>3</td>
<td>7</td>
<td>15</td>
<td>7Vdc</td>
<td>7.30%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>7Vdc</td>
<td>4.23%</td>
</tr>
</tbody>
</table>
the solution of transcendental equations. The convergence characteristics with the number of iterations vs objective function values (THD) are shown in Figure 17.

The switching pulses corresponding to the generated switching angles are shown in Figure 18(a) for the primary circuit and Figure 18(b) for an auxiliary circuit. Figure 19 shows the 15-level output voltage and current waveforms of the proposed inverter with the binary approach of dc sources (1:2:4 ratio), and Figure 20 shows the corresponding THD of the 15-level output of the proposed inverter, which is 4.23%. Figure 19 confirms that the output current waveform approximately resembles the sinusoidal waveform without using any filter at the output of the inverter. Also, it is in phase with the load voltage so that the power factor is maintained approximately unity.

The total harmonic distortion (THD) of the 15-level inverter output is measured using switching angles calculated by the PSO method at a modulation index of 0.9. The output voltage’s total harmonic distortion (THD) is 4.23% at 264.9 V, as shown in Figure 20. The THD of the results of the proposed inverter was compared with the work reported in the literature and is given in Table 5. The detailed comparison of the results of the proposed inverter was compared with the work reported in the literature. It reveals that the proposed asymmetric inverter utilizes less number of switches compared to the other topologies and also produces less % THD without employing any filter at the output.

6. Conclusion

An asymmetric 15-level inverter with 7 switches and 3 diodes had been developed in this paper to optimize the size of the design topology. The inverter also operated 7-level and 11-level operations with a proper choice of dc source selection. The lower-order dominant harmonics in the inverter output had been minimized using a low-frequency switching modulation (SHEPWM). The transcendental equations generated in SHEPWM had been solved using the Newton-Raphson method and particle swarm optimization methods to obtain the switching angles. The THD of the inverter output had been analyzed for 7-level, 11-level, and 15-level operations using equal magnitude, unequal magnitude, and binary approaches of dc sources, respectively. Using the NR method, the THD obtained at output voltage for 7-level operation is 15.36%, for 11-level operation is 11.17%, and for 15-level operation is 7.30%. Hence, it is confirmed that the 15-level operation of the proposed inverter produces lower THD than other level operations. Consequently, the proposed inverter is controlled by using particle swarm optimization for 15-level operation with the binary choice of the sources, and the THD obtained at output voltage is 4.23%. These results are compared with the similar topologies presented in the literature and concluded that the proposed inverter gives lower THD using the PSO algorithm.

Data Availability

The data sources employed for analysis are presented in the text.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References


