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Research Article

Mathematical Modeling and Performance Evaluation of 3D Ferroelectric Negative Capacitance FinFET

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Ferroelectric negative capacitance materials have now been proposed for lowering electronics energy dissipation beyond basic limitations. In this paper, we presented the analysis on the performance of negative capacitance (NC) FinFET in comparison with conventional gate dielectrics by using a separation of variables approach, which is an optimal quasi-3D mathematical model. The result has been signified steeper surface potential (ψ), lower threshold voltage (V_{th}), 1.2 mA of on-state current (Ion), and enhanced immunity of negative capacitance FinFET against short channel effects (SCE's) like 35.3 mV/V of drain-induced barrier lowering (DIBL), 60 mV/dec of subthreshold swing (SS) along with smallest off state current (I_{off}) among another conventional gate dielectric. Hence, NC FinFET can be a potential candidate for low power and high-performance device.

1. Introduction

Lower power consumption is now highly concerned issue for developing digital technology using metal oxide semiconductor field effect transistors (MOSFETs), which follows Moore's law and, down scaling the size of semiconductor device improves number of transistors per chip, exponentially increases functionality. Nevertheless, lower scale transistors are more prone to short channel effects (SCE's) [1]. A significant short channel phenomenon known as threshold voltage roll off occurs when the threshold voltage drops as the gate length decreases. Short-channel MOSFETs switch on at a smaller gate voltage than long-channel MOSFETs as a consequence [2–4]. By lowering the channel length, the area of the gate oxide and the gate oxide capacitance have dropped. But, a minimum amount of gate oxide capacitance is required for improved channel control [5]. This is accomplished by lowering the thickness of the gate oxide. Quantum mechanical tunneling happens when the thickness of SiO_2 is less than 1.2 nm [6, 7]. Gate oxide leakage current rises when the gate oxide is scaled further. In addition, the device's power usage increases significantly when it is turned off. This difficulty may be mitigated by utilizing a high-k dielectric material, which has a large dielectric constant. The use of a high-k dielectric material allows for a larger gate oxide than SiO_2 with the same oxide capacitance. The phrase equivalent oxide thickness, or EOT, refers to the thickness of a SiO_2 film that must be employed in substitute of a high-k dielectric to achieve the same oxide capacitance [7]. Nitride SiO_2 were used to increase dielectric constant about 5 along with reduction of EOT to 2 nm [8]. Besides that, HfO_2 dielectric-based FET technology enable down scaling of EOT to 0.8 nm in recent device [9]. Nevertheless, even if EOT can be reduced to zero, some basic limits resists decline of V_{dd} [10]. One of the limits addressed as, "Boltzmann limit," because of that it is not possible to decrease V_{dd} below 0.5 V [11]. For overcoming this limit, band to band tunneling can be useful. But, tunneling device has lower on-state current [12, 13]. Moreover, it is proposed that whenever the insulator capacitance is negative, then device can

overcome Boltzmann limit by reducing V_{dd} further. The negative capacitance (NC), in this situation, would result in an internal amplification of the surface potential in response to the applied gate voltage Vg [13]. In 2016, transient NC was measured in ferroelectric HfO_2 with Gd doping by the application of low voltage [13]. At the same time, similar NC effect was verified in ferroelectric Zr doped hafnium dioxide, widely known as HZO [14]. NC FET with HZO exhibit larger on/off ration at constant on state current, reported in 2018 [16]. GaAs/InN Tunnel NC FET shows higher immunity to Short Channel Effects (SCE's) [17]. It is expected that if gate oxide is replaced by ferroelectric negative capacitance material, the performance of device can be improved. In this paper, we used HZO as ferroelectric negative capacitance material to form a FinFET structure. The performance parameters like threshold voltage, surface potential profile, on-state current, and short channel effects (SCE's) of HZO with silicon channel are investigated in comparison with HfO_2 and Al_2O_3 as gate oxide by using compact mathematical model. The physical architecture of our proposed 3D FinFET can be observed from different direction in Figure 1, and the parameters value used for the architecture has been listed in Table 1.

2. Physical Architecture

Table 2, describes the research on NC-FinFET from 2017 to 2020, where the impact of negative capacitance material can easily be realized.

3. Mathematical Model

3.1. Surface Potential Model. A field effect transistor (FET) is a voltage-controlled semiconductor device. Electrostatic potential between source and drain in FET is induced by DC biasing voltage. The area between the source and drain is known as channel or Si-body and the electrostatic potential in channel is controlled by DC gate voltage. Generally, FinFET exhibit three-dimensional surface potential. The surface potential can be expressed by the following equation [30, 31].

$$\frac{\delta^2\psi(x,y,z)}{\delta x^2}+\frac{\delta^2\psi(x,y,z)}{\delta y^2}+\frac{\delta^2\psi(x,y,z)}{\delta z^2}=\frac{\mathrm{qN_{ch}}}{\epsilon_{\mathrm{ch}}}, \quad (1)$$

where $N_{\mathrm{ch}}$is channel doping, ϵ_{ch} is permittivity of channel material, and ψ is surface potential.

The total surface potential can be expressed through the following equation [30],

$$\begin{aligned}\psi(x,y,z)&=\psi_{\mathrm{sb}}+E_{\mathrm{sb}}(H_{\mathrm{fin}}-x)+\frac{q}{2\varepsilon_{\mathrm{si}}}N_A(H_{\mathrm{fin}}-x)^2\\&+\sum_{r=1}^{\infty}\frac{1}{\sinh(\gamma_r L_{\mathrm{eff}})}\left[V_r'\sinh(\gamma_r y)+V_r\sinh(\gamma_r(L_{\mathrm{eff}}-y))\right]\\&\left[\sin(\gamma_r x)+\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}t_{\mathrm{oxf}}\gamma_r\cos(\gamma_r x)\right]\sum_{s=1}^{\infty}\sum_{r=1}^{\infty}P_{\mathrm{sr}}[\sinh\{\chi_{\mathrm{sr}}(T_{\mathrm{fin}}-z)\}\\&+\sinh(\chi_{\mathrm{sr}}z)]\frac{\sin(\alpha_s(y-L_{\mathrm{eff}})}{\cos(\alpha_s L_{\mathrm{eff}})}\left[\sin(\beta_r x)+\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}t_{\mathrm{oxf}}\beta_r\cos(\beta_r x)\right].\end{aligned} \quad (2)$$

3.2. Threshold Voltage Model. Threshold voltage is another important parameter for MOSFET, which can be defined by the minimal voltage required for turning on MOSFET. Threshold voltage can be derived by following equations:

$$V_{\mathrm{TF}}=V_{\mathrm{TF}}^0-\Delta V_{\mathrm{TF}}^1-\Delta V_{\mathrm{TF}}^2. \quad (3)$$

$$\begin{aligned}V_{\mathrm{TF}}^0&=V_{\mathrm{fb}}^f+2\phi_b+\frac{Q_{\mathrm{it}}^f}{C_{\mathrm{oxf}}}-\frac{\varepsilon_{\mathrm{ch}}}{C_{\mathrm{oxf}}}\frac{d\psi_{1D}(x)}{\partial x}\bigg|_{x=0}=V_{\mathrm{fb}}^f+\left(1+\frac{C_s+C_{\mathrm{it}}^f}{C_{\mathrm{oxf}}}\right)2\phi_b-\frac{C_s}{C_{\mathrm{oxf}}}\psi_{\mathrm{sb}}+\frac{\mathrm{qN_{ch}}t_s}{2C_{\mathrm{oxf}}},\\\Delta V_{\mathrm{TF}}^1&=\frac{\varepsilon_{\mathrm{ch}}}{C_{\mathrm{oxf}}}\frac{\partial\psi_{2D}(x,y)}{\partial x}\bigg|_{x=0,y=y_{\min}^f}=\frac{\varepsilon_{\mathrm{ch}}}{C_{\mathrm{oxf}}}\sum_{\mathrm{r=1}}^{\infty}\frac{\gamma_r}{\sinh(\gamma_r L_{\mathrm{eff}})}\times\left[V_r'\sinh\left(\gamma_r y_{\min}^f\right)+V_r\sinh\left(\gamma_r\left(L_{\mathrm{eff}}-y_{\min}^f\right)\right)\right],\\\Delta V_{\mathrm{TF}}^2&=\frac{\varepsilon_{\mathrm{ch}}}{C_{\mathrm{oxf}}}\frac{\partial\psi_{3D}(x,y,z)}{\partial x}\bigg|_{x=0,y=y_{\min}^f,z=T_{\mathrm{fin}}/2}=\frac{2\varepsilon_{\mathrm{ch}}}{C_{\mathrm{oxf}}}\sum_{s=1}^{\infty}\sum_{\mathrm{r=1}}^{\infty}P_{\mathrm{sr}}\sinh\left(\frac{\chi_{\mathrm{sr}}T_{\mathrm{fin}}}{2}\right)\times\frac{\sin\left(\alpha_s\left(y_{\min}^f-L_{\mathrm{eff}}\right)\right)}{\cos(\alpha_s L_{\mathrm{eff}})}\beta_r.\end{aligned} \quad (4)$$

V_{TF}^0, ΔV_{TF}^1, and ΔV_{TF}^2 can be calculated as follows [32]:

3.3. Drain Current Model. Subthreshold current, the small amount of drain current, which can flow through the channel for below threshold voltage, is an important parameter for determining the performance of MOSFET, which can be expressed by following equation [33]:

$$I_{\mathrm{DS}}=\frac{q\mu_n(kT/q)\left(n_i^2/N_a\right)[1-\exp(-V_{\mathrm{DS}}/(\mathrm{kT}/q))]}{\int_0^{\mathrm{L_{eff}}}\left(dy/\int_0^{H_{\mathrm{fin}}}\int_0^{W_{\mathrm{fin}}}\exp[q\psi(x,y,z)/\mathrm{kT}]\mathrm{dxdz}\right)}. \quad (5)$$

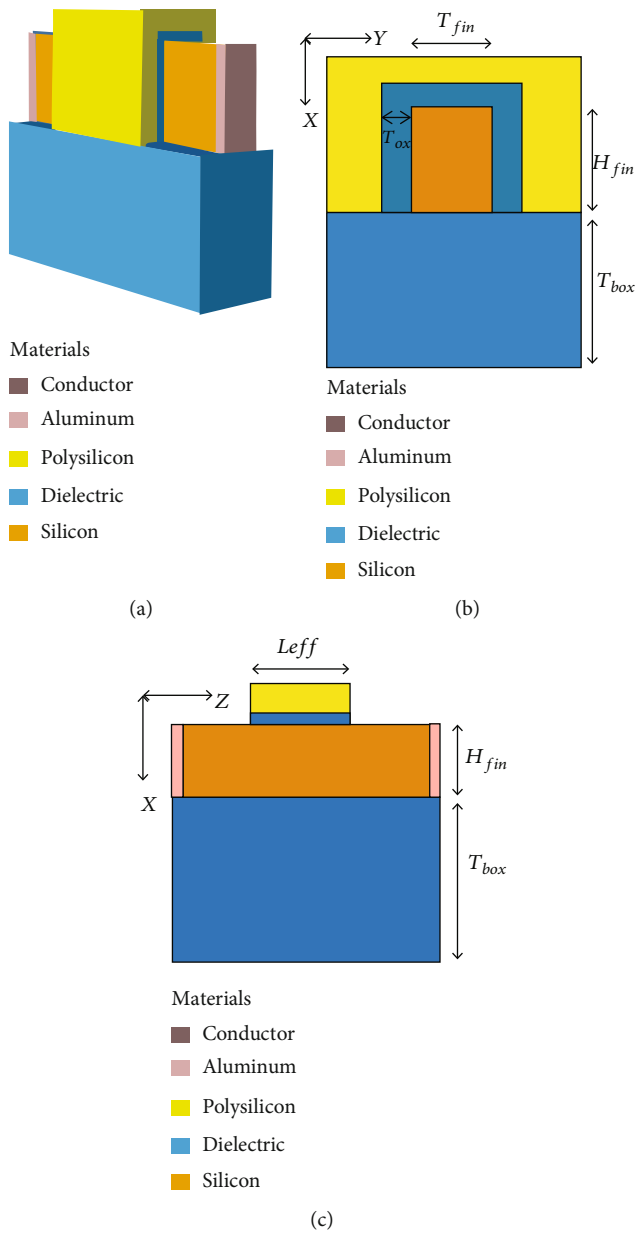

Figure 1: (a) 3D-FinFET Cross-sectional diagram. (b) XY direction. (c) XZ direction.

Table 1: Proposed device parameters.

Symbol	Designation	Value
L_{eff}	Effective channel length	16 nm
H_{fin}	Height of fin	10 nm
T_{fin}	Thickness of fin	4 nm
T_{ox}	Oxide thickness	1 nm
N_{ch}	Channel concentration	$10^{16}\,\text{cm}^{-3}$
T_{box}	Buried oxide thickness	20 nm

3.4. Transconductance. Transconductance, directly related to gain, determines how rapidly a transistor may activate when sweeping the gate voltage. [34]. Due to change in surface charge, a higher value of transconductance cause higher drain current, which is responsible for increasing device sensitivity. Operation point of a sensor can be determined by using the maximum transconductance gate voltage. Most of the devices tested have maximum transconductances greater than 10 *uS*. [35]

The transconductance can be defined by following equation:

$$g_m = \frac{\text{dI}_D}{\text{dV}_{\text{GS}}}. \tag{6}$$

3.4.1. Drain Induced Barrier Lowering (DIBL). DIBL reduces the nanoscale MOS threshold voltage by modifying the source-to-drain potential barrier. This permits the device

Table 2: Previous study on NC-FinFET.

Highlights	T_{fin} (nm)	T_{ox} (nm)	H_{fin} (nm)	L_g (nm)	SS (mV/decade)	Year [reference]
Sub-10 nm NC-FinFET is analyzed operating at 0.25 V	3	0.7	—	9	—	2017 [18]
Investigation of CMOS logic circuits using NC-FinFET	8	—	34	30	—	2017 [19]
FE capacitor of Sub-60 mV/decade NC-FinFET with sub-10 nm	10	1.4	40	90	36.31	2017 [20]
NC-FinFET with minimal hysteresis of 0.48Vand sub-20 mV/dec SS	40	1.4	40	70	<20	2017 [21]
Design and evaluation of performance of SRAM using 7 nm-node NC-FinFET	6.5	1	32	21	—	2017 [22]
Analysis of fin-LER variability in NC-FinFET	9.6	2	25	22	—	2017 [23]
TCAD simulation to design NC-FinFET to avoid instability of NC state	4	0.5	—	20	48	2017 [24]
Analysis of process variations impact on NC-FinFET	6.5	1	32	21	—	2018 [25]
Analysis of spacer designs for FinFET and NC-FinFET	6	0.9	42	16	65.6	2019 [26]
Ge NC-FinFET in presence of fixed trap charges is analyzed	8	1	9	20	—	2019 [27]
Improved SS and drain current in NC-FinFET	7 7	1 1	40 40	500 20	34.5 53	2019 [41]
Relation between TFE and stability of 6 T NC-FinFET-based SRAM cell	8	0.65	42	20	—	2019 [28]
GIDL issue in NC-FinFET is analyzed	7	0.9	50	20	75	2020 [29]

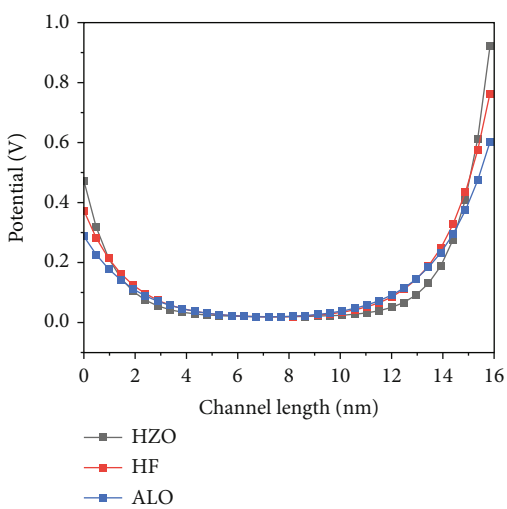

Figure 2: Comparison of surface potential profiles of HZO, Al_2O_3, and HfO_2-based FinFET with channel length $L = 12$ nm.

channel to conduct lesser gate voltages. [36]. The DIBL is calculated as the proportion of the difference in threshold voltage observed at the minimal value to the maximum priority of the drain current. Shift in threshold voltage (V_{th}) to alter in drain voltage (V_{ds}) is characterized as a drain-induced barrier lower [37].

$$\mathrm{DIBL}\left(\frac{\mathrm{mV}}{V}\right) = \frac{\Delta V_{\mathrm{th}}}{\Delta V_{\mathrm{ds}}}. \tag{7}$$

3.4.2. Subthreshold Swing. The switching effectivity of low power digital device can be evaluated by the characteristics of drain current at the subthreshold region of device, which is commonly known as subthreshold swing. The analytical model of subthreshold swing is developed by solving the Poisson's equation in the channel region at cutline position $x = T_f/2$, $y = H_{\mathrm{fin}}$ [38].

According to [39], the subthreshold swing expression is

$$S = \left[\frac{q}{2.3\mathrm{kT}}\frac{\partial \Psi(x,y,z)}{\partial V_{\mathrm{GS}}}\right]^{-1},$$
$$S = \left[\frac{q}{2.3\mathrm{kT}}\left(\frac{\partial \psi_{1D}}{\partial V_{\mathrm{GS}}} + \frac{\partial \psi_{2D}}{\partial V_{\mathrm{GS}}}\bigg|_{z=0} + \frac{\partial \psi_{2D}}{\partial V_{\mathrm{GS}}}\bigg|_{z=L_f} + \frac{\partial \psi_{3D}}{\partial V_{\mathrm{GS}}}\bigg|_{y=0} + \frac{\partial \psi_{3D}}{\partial V_{\mathrm{GS}}}\bigg|_{y=H_{\mathrm{fin}}}\right)\right]^{1}. \tag{8}$$

3.5. Off Current. Off current is directly depending on Subthreshold Slope (SS). It can be calculated by following equation [40]:

$$I_{\mathrm{off}} = 100\frac{W}{L}10^{-V_{\mathrm{Th}}/\mathrm{SS}}. \tag{9}$$

3.6. Short Channel Effects in NC-FinFET. Negative capacitance is used to counteract short-channel effects in highly scaled FETs [18, 20, 22]. The key short channel parameter of inverse subthreshold swing can be written as

$$\mathrm{SS} = 2.3\frac{K_B T}{q}\frac{\partial V_g}{\partial \psi_s} = 2.3\frac{K_B T}{q}\left(1 + \frac{C_{\mathrm{dip}}}{C_{\mathrm{ox}}}\right), \tag{10}$$

where ψ_s is surface potential, $K_B T$ is multiplication of Boltzman constant and temperature, and C_{dep} and C_{ox} are depletion layer capacitance and gate oxide capacitance. In conventional MOSFET, the factor $(1 + C_{\mathrm{dip}}/C_{\mathrm{ox}})$ is always above unity. By making oxide capacitance negative in nature is one method to lower the value of Subthreshold Swing. If

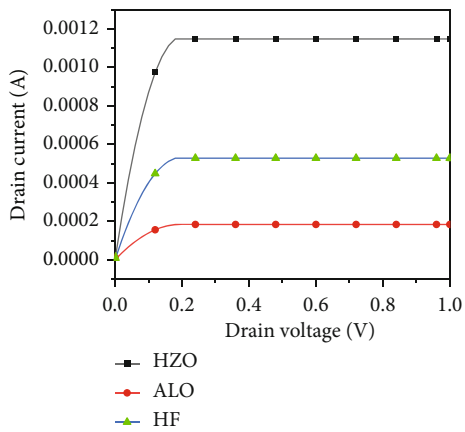

Figure 3: Comparison of on-state saturated current characteristics with variation of oxide, HZO, Al_2O_3, and HfO_2 in FinFET.

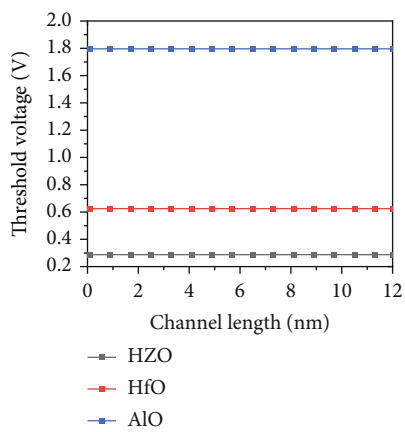

Figure 4: Comparison of threshold voltage estimated for HZO, Al_2O_3, and HfO_2-based FinFET for different channel length.

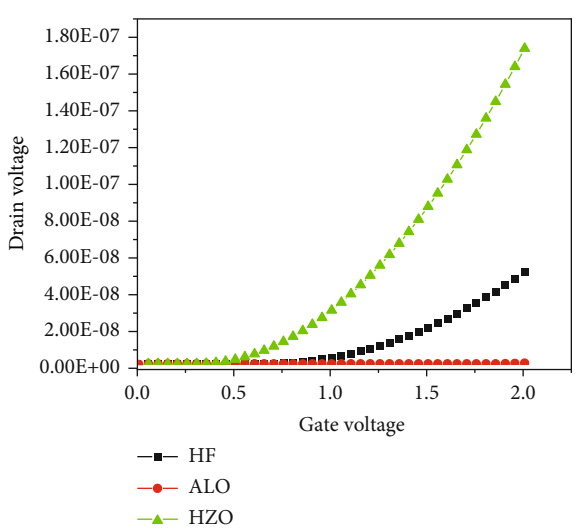

Figure 5: Comparison of transfer characteristics for HZO, Al_2O_3, and HfO_2-based FinFET by varying gate voltage.

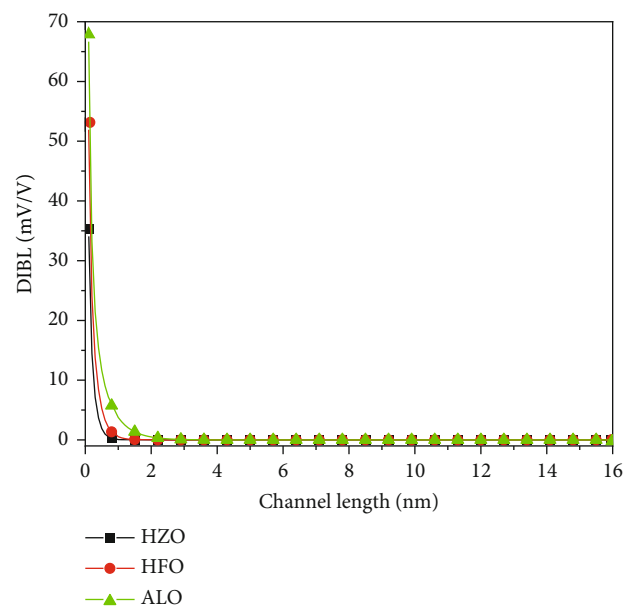

Figure 6: Comparison of DIBL for HZO, Al_2O_3, and HfO_2-based FinFET's keeping channel thickness, W fixed at 4 nm and effective channel length, L_{eff} varies from 2 to 16 nm.

ferroelectric material, which adopts the property of negative capacitance, is chosen, this will be attainable [15, 42–44]. Equivalent oxide capacitance (C'_{ox}) in NCFET is achieved by adding ferroelectric (C_F) and dielectric capacitance (C_{ox}) in series.

$$C'_{ox} = \frac{C_{ox} C_F}{C_F - C_{ox}}. \tag{11}$$

Therefore, the NCFET's subthreshold swing can be represented as

$$SS = 2.3 \frac{K_B T}{q} \frac{\partial V_g}{\partial \psi_s} = 2.3 \frac{K_B T}{q} \left(1 + \frac{C_{dip}}{C'_{ox}}\right). \tag{12}$$

Confirming that the SS for the condition can be lowered to the Boltzmann limit.

Drain Induced Barrier Lowering (DIBL) can be calculated as mentioned in Equation (7). As DIBL depends on threshold voltage, threshold voltage of NCFET computed by the following expression:

$$V'_{Th} = V_{Th0} + |\eta| V_d, \tag{13}$$

where η is the factor of DIBL and V_{Th0} is threshold voltage at zero drain voltage. The factor of DIBL is positive for conventional MOSFET, on the other hand negative for NCFET [45]. With the increment of drain voltage, the threshold voltage will increase in NCFET and that is opposite to conventional MOSFET. This results to negative DIBL factor. Hence, DIBL is lower for NCFET.

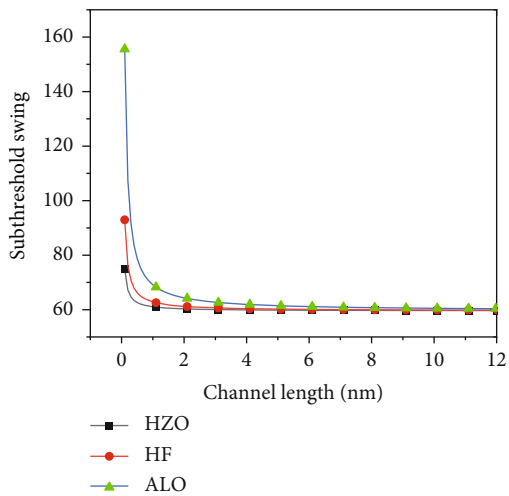

Figure 7: Comparison subthreshold swing (SS) for HZO, Al_2O_3, and HfO_2-based FinFET's.

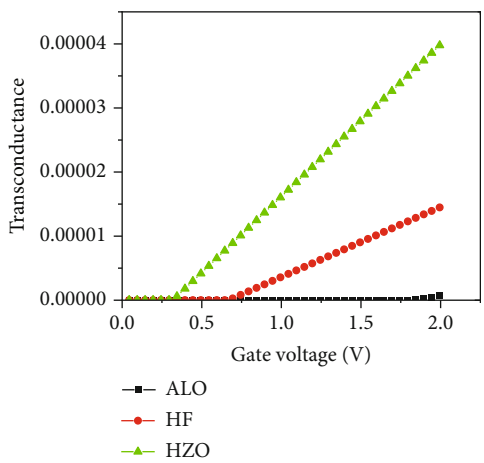

Figure 8: Comparison of transconductance for HZO, Al_2O_3, and HfO_2-based FinFET's by stepping up the gate voltage, V_g from 0 to 2 V.

4. Result and Discussion

The performance parameter like surface potential, threshold voltage along with short channel effects have been studied for negative capacitance ferroelectric hafnium zirconium oxide (HZO) in FinFET (NC-FinFET). Surface potential along the channel length is shown for different dielectric material in Figure 2, considering drain voltage 1 V. FinFET with HZO has higher potential around 0.9 V, while other dielectric-based FinFET has 0.79 V and 0.6 V simultaneously. Furthermore, the rise of potential in drain side of channel is steeper for NC-FinFET. This is due to ferroelectric negative capacitance property of channel, which results faster rising of surface potential [46]. Also, the steeper slope increases the total electric field along with the rate of electron velocity, thus, significantly higher on-state current, shown in Figure 3. For the range of 0 to 1 V of drain voltage, NC-FinFET with HZO shows 3 to 4 times higher drains current than FinFET with Al_2O_3 and HfO_2, respectively. Moreover, sharp change of surface potential restricts increased carrier velocity. Hence, velocity saturation problem is reduced drastically.

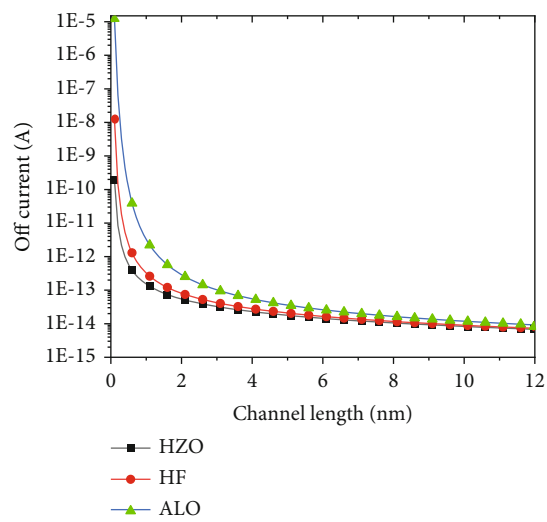

Figure 9: Comparison of transconductance for HZO, Al_2O_3, and HfO_2-based FinFET's keeping channel thickness, W fixed at 4 nm and effective channel length, L_{eff} varies from 2 to 16 nm.

The threshold voltage profile for different gate dielectric is shown in Figure 4. HZO-based NC-FinFET exhibits lower threshold voltage, which further results high on-state current together with high operational speed of device [47], whereas the threshold voltages are constant for these three dielectric with decrements of channel length. Ferroelectric thickness [48] and temperature [49] have a significant impact on ferroelectric capacitance. Threshold voltage drops when ferroelectric thickness rises because ferroelectric capacitance reduces because of increased ferroelectric thickness. Besides that, negative oxide capacitance of NCFET might also result in a drop in threshold voltage [50]. Afterwards, the transfer characteristic plotted for different oxide in Figure 5, considering drain voltage 1.2 V, depicts lowest threshold voltage and highest after threshold current for HZO-based NC-FinFET.

The DIBL signifies the difference of threshold voltage with variation of drain voltage. In Figure 6, DIBL's are plotted for three gate dielectrics HZO, HfO_2, and Al_2O_3. These curves depict increment of DIBL with the declination of channel length. The maximum level of DIBL for lowering channel length of HZO-based NC-FinFET is about 35.3 mV/V and it is around 54.5 mV/V for HfO_2-based FinFET. That is because the reverse DIBL effect of negative capacitance material. The overall charge in the channel decreases with rising drain voltage as negative flowing charges are drawn out. As a result, reduction of DIBL is triggered [51]. Because of lower DIBL, the output resistance will be substantially higher for NCFET's. Moreover, drain voltage induced breakdown is significantly reduced for NCFET's [52].

The reciprocal of the steepest slope of transfer characteristics yielded the subthreshold slope (SS). Smaller SS exhibits

Table 3: Comparison of different characteristic of FET technology.

FET technology	Drain current (mA)	Threshold voltage (V)	Minimum subthreshold slope	Off current (A)	Transconductance (μS)	DIBL
NC-FinFET with HZO	1.2 mA	0.3 V	60 mV/dec	$6.82 \times 10^{-15} A$	40μS	35.3 mV/V
FinFET with HfO_2	0.5 mA	0.67 V	61 mV/dec	$7.30 \times 10^{-15} A$	10μS	54.4 mV/V
FinFET with Al_2O_3 dielectric	0.15 mA	1.8 V	70 mV/dec	$9.21 \times 10^{-15} A$	0.1μS	67.8 mV/V
FinFET with $SiO_2 + HfO_2$ dielectric [54]	0.073 mA	0.128 V	72.7 mV/dec	$4.16 \times 10^{-5} A$	—	30 mV/V
Hetero-junction $Si_{1-x}Ge_x$ FinFET [55]	—	—	52.67 mV/dec	1.38×10^{-18} A	—	52.37 mV/V
Bulk MOSFET [56]	—	—	88 mV/dec	5×10^{-5} A	—	—
SOI MOSFET [56]	—	—	65 mV/dec	50 μA/μm	—	150 mV/V

lower off state leakage current. In Figure 7, it is demonstrated that the reduction of SS occurs when the channel length is larger. That is because of having the opposite proportionality of channel length and drain current. As HZO has ferroelectric negative capacitance property and higher dielectric constant, therefore SS for HZO-based NC-FinFET reaches theoretical limit of 60 mV/decade. Hence, this lower value presents higher immunity to SCE's [53].

Transconductance is the derivative of transfer characteristics of FET and implies speed of device. In Figure 8, it can be observed that after threshold voltage, transconductance of HZO-based device is significantly shot up and the rate is around 4 times higher than conventional HfO_2-based device. Here, the drain voltage is varied from 0 to 2 V by considering step size of 0.5 V.

As gate length is reduced, the drain depletion zone and source depletion region slowly contact and penetrate each other, reducing barrier heights. Lowering the source barrier increases charge carrier injection via the short channel, and the gate may lose control, hence off-state current increased. It can be seen from Figure 9, FinFET with HZO have less off-state current as compared to HfO_2, and Al_2O_3 dielectric-based FinFET.

Table 3 depicts the figure of merits from mathematical analysis for comparing three-gate oxide from this work and recent literature at a glance. It is seen that the drain current for HZO is around 2 and 10 times higher from FinFET with HfO_2 and Al_2O_3 subsequently. Moreover, 40 μS of transconductance, which is around 4 times higher than conventional HfO_2 gate oxide-based device and significantly lower DIBL. Additionally, FinFET with HZO have comparatively less off-state current from device with other gate oxide.

5. Conclusion

In this research work, the performance parameter of NC-FinFET with HZO in comparison with Al_2O_3 and HfO_2-based FinFET's are investigated. The surface potential, threshold voltage, DIBL, Subthreshold Swing, off current, output, and transfer characteristics are thoroughly investigated for all of three channel dielectrics. The stepper surface potential of HZO-based NC-FinFET is the major cause for the controllability of velocity saturation. The 0.3 V threshold voltage found in NC-FinFET guarantees high on state current, which is 16 times higher than FinFET with $SiO_2 + HfO_2$ dielectric. Besides that, the 35.3 mV/V of DIBL and 60 mV/dec of Subthreshold Swing (SS) reveal worthiness of NC-FinFET with HZO in a very low dimension. The off-state current of NC-FinFET is around 98% and 35.04% lower than $SiO_2 + HfO_2$ dielectric and Al_2O_3 dielectric-based FinFET simultaneously. Therefore, hafnium zirconium-based negative capacitance FinFET device outperforms the conventional FinFET with Al_2O_3 and HfO_2 dielectric in case of suppression of SCE's and off-state current. Hence, it can be the potential candidate for low power and high-speed device fabrication.

Data Availability

The parameter data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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