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Research Article

Modelling, Simulation, and Implementation of Effective Controller for KY Stepping Up Converter

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This paper studies on a new Hybrid Posicast Control (HPC) for Fundamental KY Boost Converter (FKYBC) worked in Continuous Current Mode (CCM). Posicast is a feed-forward compensator. It reduces the overshoot in the step result of the flippantly damped plant. But the conventional controller approach is sensitive owing to the changes in the natural frequency. So, as to reduce this undesirable sensitivity and load potential control of FKYBC, a HPC is designed in this article. Structure of HPC is posicast with feedback loop. The independent computational time delay is the main design function of the posicast. The enactment of the FKYBC with HPC is confirmed at various operating regions by making the MATLAB/Simulink and experimental model. The posicast function values are implemented in Arduino Uno-ATmega328P microcontroller. The results of new HPC have produced minimal noise in control signal in comparison with traditional PID control.

1. Introduction

A positive/negative DC source is important for most of the real-time applications such as audio amplifier, LED driver, the medical instruments, the mobile communications, the robot communication systems, the signal generator, central processing unit in PC, and the data transmission interface devices. Therefore, DC source is not directly taken from supply mains, and it is derived from the DC-DC converters. Based on this reasons, many DC-DC converters was designed such as Cuk, KY, and Luo converters (LC) [1–4]. Amid these converters, KY converters are simple in structure, small voltage stresses/volume of the circuit components, minimized voltage/current ripples, and less number of circuit components in comparisons with LCs and Cuk converters [5]. In this article, Fundamental KY Boost Converter (FKYBC) is considered for study. Though the controller design is a challenging one for nonlinear damped dynamics of FKYBC that are functions of the load parameters, the new research in modern digital signal technology has recommended a new control to enhancing FKYBC regulation [5].

Hence, in this article, a new Hybrid Posicast Control (HPC) is designed for FKYBC operated in Continuous Conduction Mode (CCM). Posicast Control (PC) is a feed-frontward controller approach for flippantly damped plants [6]. Control of this approach is capable to suppress the waver response of a lightly damped plant; still, the problem is warmth to plant ambiguity. This problem is solved by designing a new posicast in feedback loop, which minimizes the sensitivity to parameter changes of the plant. Many researchers has detailed the conventional PID control for power electronics converter needs the additional arrangement changes to attain the proficient transient and steady state performance [7]. Therefore, the digital implementation of PID control for power converter is more complicated. The main benefits of the closed loop effect of HPC over the PID control has excellent transient and steady state behavior, easy to obtain the controller parameters, predictable response by small-signal averaged model, easy to implement

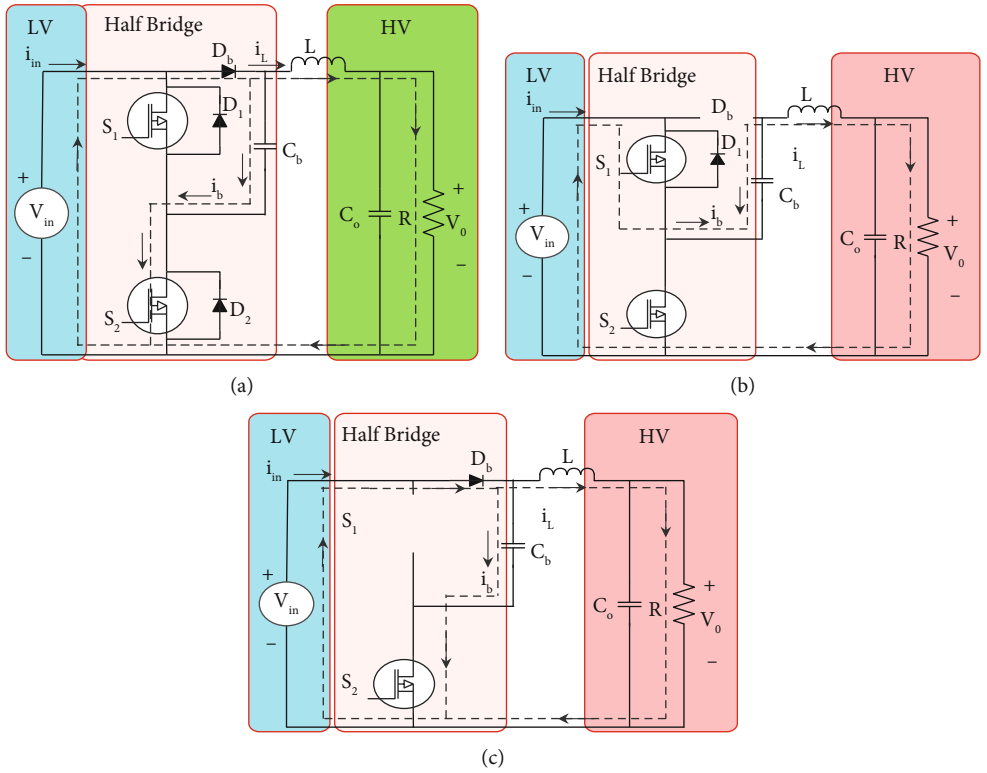

Figure 1: FKYBC: (a) topology, (b) state 1 operation, and (c) state 2 operation.

in digital-time platform, eliminate the damping effects provided for multiple sets of control gains, no need of extra changes in the control structure, and naturally minimizes the high frequency noise [8, 9].

A KY boost converter with only voltage loop classical PI control has been well executed [10]. From this article, the authors have not addressed controller design; output voltage ripples of this converter has produced 0.6 V and also not discussed input voltage and load resistance changes of same converter. Small signal mathematical modeling of KY converter in CCM is well presented [11]. Still, the authors have carried out only simulation study of this converter model, and besides, the same converter has twisted output ripple voltage of -0.8 V in open-loop mode. Nonlinear control for KY converter has been presented [12]. Conversely, load potential and coil current controls of this model have created overshoots of 1 V/0 V and took settling time of 0.02 s/0 s in line/load variations with minimal ripples of current and voltage. Implementation of linear quadratic regulator plus FLC for LC is well executed [13]. It is seen from this article that the output voltage ripples of this model has generated -0.95 V and output current ripple of -0.15 A. Fixed and FM operation of SMC for various topologies of LCs is well recorded [14–16]. But the load potential and coil current of it have produced huge overshoots, trifling steady-state errors, and took setting time in line modifications. The PC for stepping-down converter is well addressed [17]. The broad analysis of various nonlinear controllers for LCs was addressed [18, 19]. Though the output voltage of the LCs has spawned huge overshoots in load troubles, the detailed modeling of various DC-DC converters was deliberated [20]. However, the linear controllers are very complex for LCs and KY converters at different operating states. In the above literature reviews, it is seen that a new HPC for FKYBC have not been reported.

Table 1: Specification of FKYBC.

Parameter name	Symbol	Value
Source voltage	V_{in}	16 V
Load voltage	V_o	24 V
Filter coil	L	8 μH
Capacitors	C_b and C_o	1953 μF and 866 μF
Operating frequency	f_s	100 kHz
Load	R	5.769 Ω
Overshoot	λ	0.978
Damped natural period	T_d	0.00053 s
Duty cycle	δ	0.5

Hence, this paper discusses how to attempt the design and implementation of a new HPC for FKYBC in CCM. Posicast parameters are derived with support of the small-signal averaged model of FKYBC.

The main contributions of this article are as follows: first, the mathematical modelling of FKYBC is derived and then designed the HPC/PID control for FKYBC. Secondly, simulation and experimental analysis are carried out using

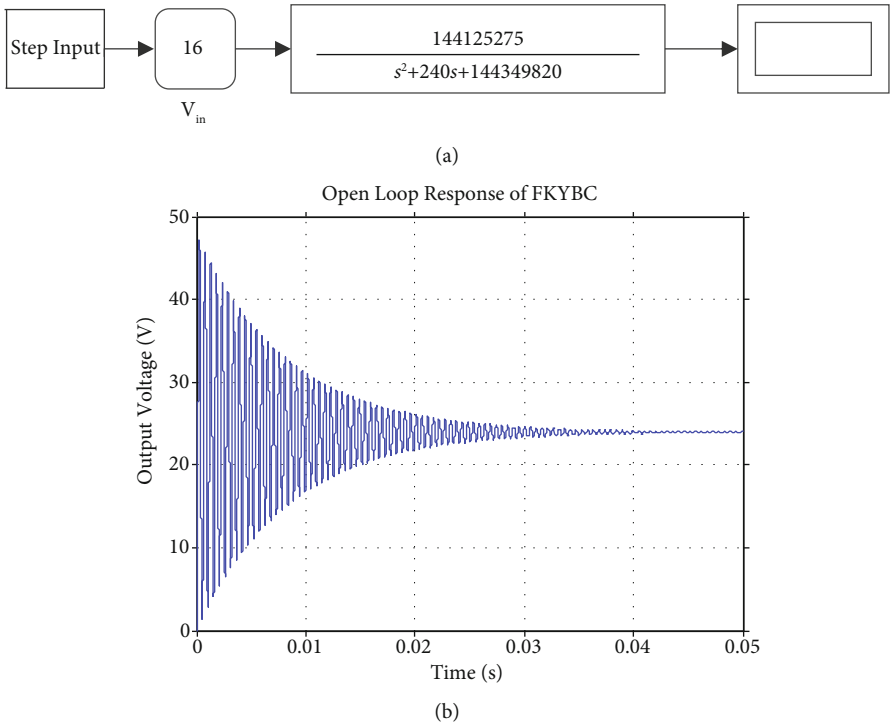

Figure 2: (a) MATLAB/Simulink model of FKYBC and (b) simulated open-loop response of FKYBC.

designed HPC for FKYBC over the conventional PID control. Thirdly, the time domain specifications of proposed controller is discussed with PID control.

The organization of this article is as follows: the introduction and literature review of KY converters and LCs along with their control methodologies are detailed in Section 1. Operation and averaged modeling of FKYBC are discussed in Sections 2 and 3. Open-loop analysis of FKYBC is presented in Section 4. The design of HPC and PID control for FKYBC is detailed in Section 5. In Sections 6 and 7, the results of the converter with controllers are discussed. In Section 8, the conclusions are addressed.

2. Operation and Modeling of FKYBC

The FKYBC circuit is exemplified in Figure 1(a). It contains two switches (POWER) S_1 and S_2, diode D_b, energy storage-shifting capacitor C_b, output filter components L, and C_0. Moreover, V_b and V_0 are the potential across C_b and C_0, and i_L is inductor current. The FKYBC is one of the modern DC-DC converter topologies. It produces that the output voltage is more than the V_{in} with microlevel ripples in the V_0 as well as i_L. Here, the FKYBC is operated in CCM with two states of operation, and its circuits are represented in Figures 1(b) and 1(c). In state 1 operation (refer to Figure 1(b)), S_1 is ON and S_2 is OFF, and D_b is nonconduction mode during the time period of $(0, \delta T)$. So, the current flow path is indicated in arrow direction as shown in Figure 1(b). Consequently, the potential across inductor V_L plus the output potential V_o will equal the input potential V_{in} plus the potential V_b, causing the L to be energized. Furthermore, the flow of electrons through C_0 = flow of

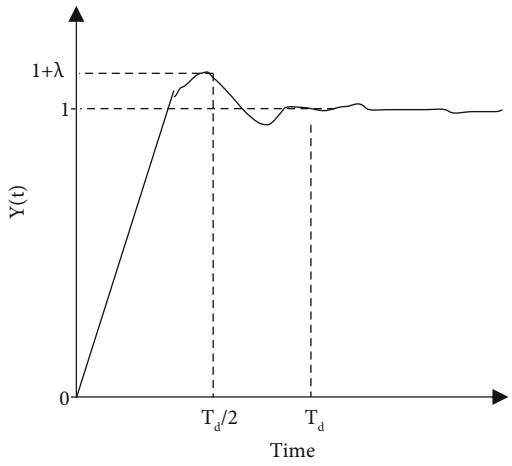

Figure 3: Result of a lightly damped FKYBC 55 with step input.

electrons through L minus flow of electrons through load R. Also, C_b released the energy in this mode. Consequently, the state space differential equations of the FKYBC during mode 1 is engraved as

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{in} + V_b - V_o}{L}, \\ \dfrac{dV_o}{dt} = \dfrac{i_L}{C_o} - \dfrac{V_o}{RC_o}, \\ \dfrac{dV_b}{dt} = -\dfrac{i_L}{C_b}, \end{cases} \quad \text{Switch ON.} \tag{1}$$

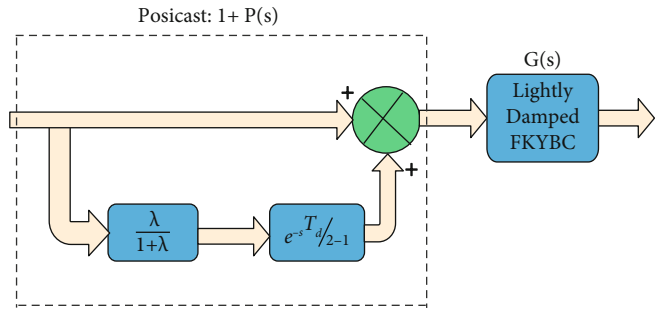

Figure 4: The classical half-cycle posicast.

During state 2 operation (see Figure 1(c)), S_2 is closed, D_b is conducted, and S_1 is open. The current flow direction is marked in the arrow as shown in Figure 1(c). Consequently, $V_L = V_{\text{in}}$ minus the V_0, so coil L is to be deenergized. Also, the C_b gets energized to V_{in} in a short span of period during this mode. So, the state space differential equations of same converter in state 2 is expressed as

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{\text{in}} - V_o}{L}, \\ \dfrac{dV_o}{dt} = \dfrac{i_L}{C_o} - \dfrac{V_o}{RC_o}, \\ v_b = V_{\text{in}}, \end{cases} \quad \text{Switch OFF.} \tag{2}$$

During steady-state operating region of FKYBC, the i_L does not vary shortly; the current is equal during both at the end of switches' ON and OFF states. In addition, the i_L is equal at the starting of switch OFF state and at the end of switch ON state. So, the gain of voltage of FKYBC is written as

$$\frac{V_{\text{o}}}{V_{\text{in}}} = 1 + \delta. \tag{3}$$

Meanwhile, $0 < \delta < 1$, $V_{\text{o}} > V_{\text{in}}$.

Assume no losses in the FKYBC, input power = output power, which is expressed as

$$V_{\text{o}} I_{\text{o}} = V_{\text{in}} I_{\text{in}}. \tag{4}$$

Substituting (3) in (4) to obtains

$$\frac{I_{\text{o}}}{I_{\text{in}}} = 1 + \delta. \tag{5}$$

The improved averaged and transfer function models of the FKYBC are derived and discussed in the next sections. The specifications of FKYBC circuit are enumerated in Table 1.

3. Improved Averaged Model of FKYBC

The averaged model of the FKYBC Equation (6) can be derived from Equations (1) and (2) with the help of averaging technique

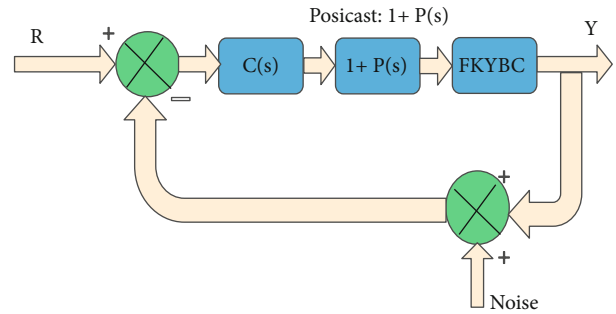

Figure 5: FKYBC with HPC.

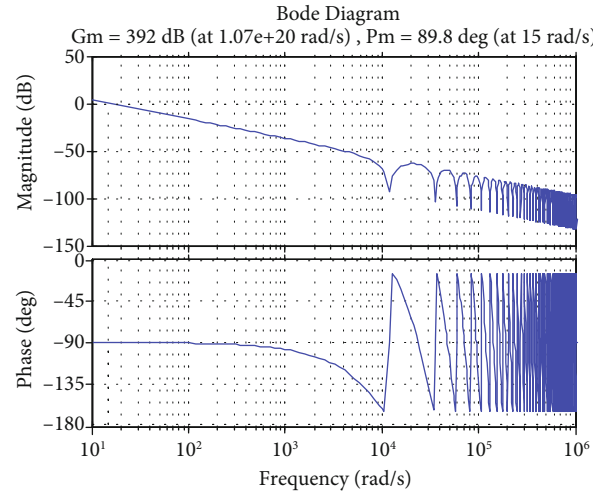

Figure 6: Frequency analysis of HPC.

$$\begin{cases} \dfrac{d\langle i_L \rangle}{dt} = \dfrac{\langle V_{\text{in}} \rangle - \langle V_o \rangle}{L} + \dfrac{\langle V_b \rangle \delta}{L}, \\ \dfrac{d\langle V_o \rangle}{dt} = \dfrac{\langle i_L \rangle}{C_o} - \dfrac{\langle V_o \rangle}{RC_o}. \end{cases} \tag{6}$$

From (6), $\langle i_L \rangle$, $\langle V_o \rangle$, $\langle V_b \rangle$, and $\langle V_{\text{in}} \rangle$ are the equivalent averaged value of i_L, V_o, V_b, and V_{in}.

The V_b in Equation (7) can be derived from Figure 1(a) by presumptuous that the V_b falls linearly within the time period of $(0, \delta T)$ and its slope $= -i_L/C_b$.

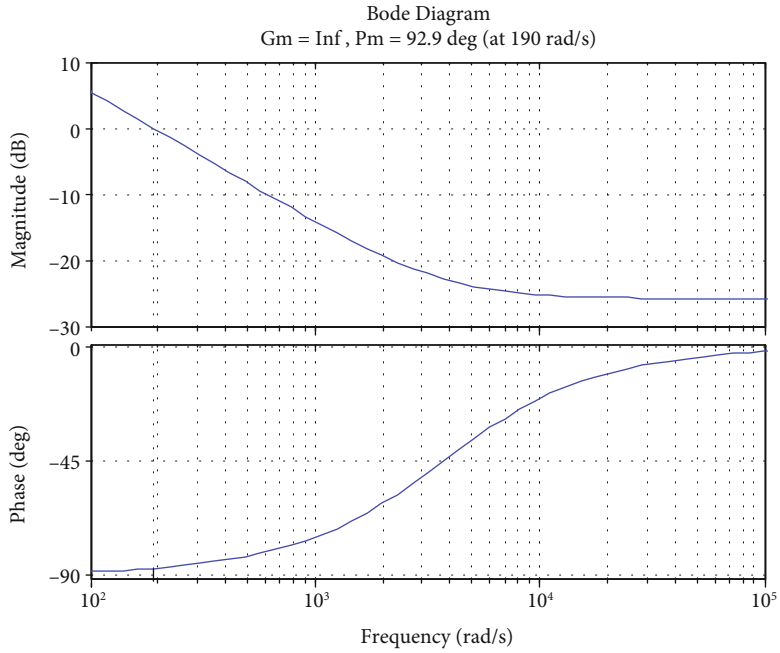

Figure 7: Frequency response of PID control.

$$\langle V_b \rangle = \langle V_{\text{in}} \rangle - \frac{\langle i_L \rangle}{2f_s C_b}\{\delta\}^2. \tag{7}$$

Then, substituting Equation (7) in Equation (6) to attain the proficient averaged model of the FKYBC, it is expressed as

$$\begin{cases} \dfrac{d\langle i_L \rangle}{dt} = \dfrac{\langle V_{\text{in}} \rangle (1+\delta)}{L} - \dfrac{\langle V_o \rangle}{L} - \dfrac{\langle i_L \rangle \delta^3}{2f_s C_b L}, \\ \dfrac{d\langle V_o \rangle}{dt} = \dfrac{\langle i_L \rangle}{C_o} - \dfrac{\langle V_o \rangle}{RC_o}. \end{cases} \tag{8}$$

Adding the C_b and the f_s in Equation (8) studied the theoretical dynamic characteristics of the FKYBC. Suppose that i_L, V_0, V_{in}, δ, and V_b are the dc values of $\langle i_L \rangle$, $\langle V_0 \rangle$, $\langle V_{\text{in}} \rangle$, δ, and $\langle V_b \rangle$, correspondingly. $\widehat{i_L}$,$\widehat{V_o}$, $\widehat{V_{\text{in}}}$, $\widehat{\delta}$ and $\widehat{V_b}$ are the small ac disparities of $\langle i_L \rangle$, $\langle V_0 \rangle$, $\langle V_{\text{in}} \rangle$, δ, and $\langle V_b \rangle$, correspondingly. Hence, the equivalent dc values plus the overlaid small ac changes can be expressed by the $\langle i_L \rangle$, $\langle V_0 \rangle$, $\langle V_{\text{in}} \rangle$, δ, and $\langle V_b \rangle$, with the assumption that the ac modifications are low in magnitude compared to the dc value, and it is written as

$$\begin{cases} \langle i_L \rangle = I_L + \widehat{i_L}, & \widehat{i_L} << I_L. \\ \langle V_o \rangle = V_o - \widehat{V_o}, & \widehat{V_o} << V_o. \\ \langle V_{\text{in}} \rangle = V_{\text{in}} - \widehat{V_{\text{in}}}, \text{ with } & \widehat{V_{\text{in}}} << V_{\text{in}}. \\ \langle \delta \rangle = \delta - \widehat{\delta}, & \widehat{\delta} << \delta. \\ \langle V_b \rangle = V_b - \widehat{V_b}, & \widehat{V_b} << V_b. \end{cases} \tag{9}$$

Considering Equation (9) into Equation (8) and then removing the corresponding DC values obtained

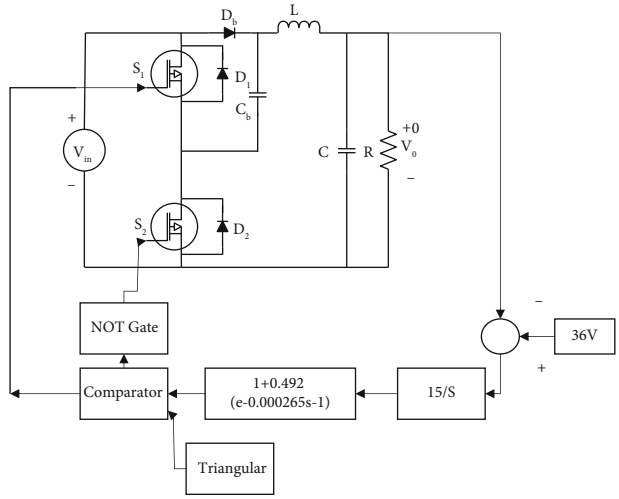

Figure 8: MATLAB/Simulink model of HPC for FKYBC.

$$\begin{cases} \dfrac{dI_L}{dt} = \dfrac{V_{\text{in}}(1+\delta)}{L} - \dfrac{V_o}{L} - \dfrac{I_L \delta^3}{2f_s C_b L}, \\ \dfrac{dV_o}{dt} = \dfrac{I_L}{C_o} - \dfrac{V_o}{RC_o}. \end{cases} \tag{10}$$

Accordingly,

$$\begin{cases} V_o = \dfrac{2V_{\text{in}}(1+\delta) f_s C_b R}{2f_s C_b R + \delta^3}, \\ I_L = \dfrac{2V_{\text{in}}(1+\delta) f_s C_b}{2f_s C_b R + \delta^3}. \end{cases} \tag{11}$$

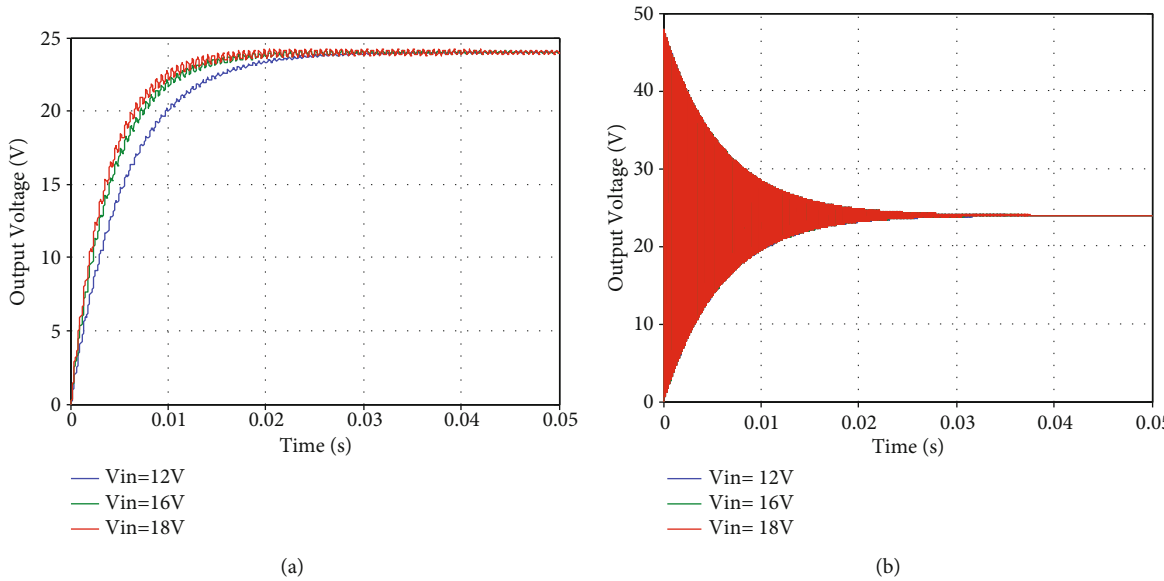

FIGURE 9: Simulated V_o responses of FKYBC for different V_i using (a) HPC and (b) PID controller.

Equation (12) can be attained by combining Equation (9) and Equation (8), then removing the ac values and ignoring the complex order ac relations due to their ranges are little.

$$\begin{cases} \dfrac{dI_L}{dt} = \dfrac{V_{in}\hat{\delta} + \hat{V}_{in}(1+\delta)}{L} - \dfrac{\hat{V}_o}{L} - \dfrac{3\delta^2 I_L\hat{\delta} + \delta^3\hat{i}_L}{2f_s C_b L}, \\ \dfrac{dV_o}{dt} = \dfrac{\hat{i}_L}{C_o} - \dfrac{\hat{V}_o}{RC_o}. \end{cases} \tag{12}$$

Model from the duty ratio to the V_o of the FKYBC can be derived with help of the Laplace transform on Equation (12), and it is expressed as

$$G(s) = \frac{\hat{v}_o}{\hat{\delta}} = \left(\frac{(V_{in}/LC_o) + (3\delta^2 I_L/2LC_o f_s C_b)}{\left(s^2 + \left((\delta^3/2f_s LC_b) + (1/RC_o)\right)s + \left(\delta^3/2Rf_s LC_o C_b\right) + (1/LC_o)\right)} \right). \tag{13}$$

4. Open-Loop Response of FKYBC

The MATLAB/Simulink model and its simulated open-loop response of FKYBC are exposed in Figures 2(a) and 2(b) by $V_{in} = 16$ V and $V_o = 24$ V. It is clearly found that the FKYBC in open-loop mode has created large peak overshoots and took a long time to settle. In order to solve this problem, a new posicast control is designed for FKYBC in CCM.

5. Design of Effective Controllers

5.1. Fundamental of Posicast. The step result of lightly damped model is revealed in Figure 3. It is categorized by overshoot λ and the damped time period T_d [6–9].

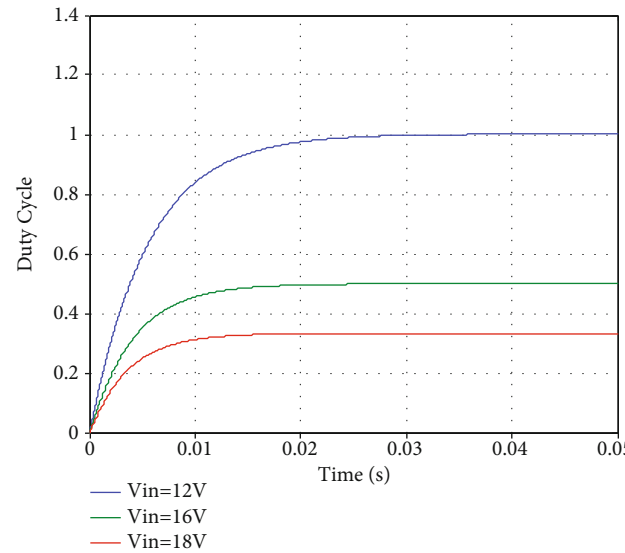

FIGURE 10: Simulated response of duty cycle of FKYBC with HPC for various V_{in}.

Figure 4 indicates the structure of a classical half-cycle posicast. It is intended based on the λ and the T_d. Precise information of the step result constraints produces a control whose smallest zeros frequency revoke the leading plant pair. It is known as half-cycle since the surrounded time delay is $T_d/2$. Therefore, HPC arrangement is explained in Figure 5.

The posicast function is prearranged via

$$P(s) = \frac{\lambda}{1+\lambda}\left(e^{-s(T_d/2)} - 1\right). \tag{14}$$

$P(s)$ is the λ and the T_d. It fundamentally reforms the set values into two portions; primarily, control minus the scale quantity from the set value (R), in order to the peak of a

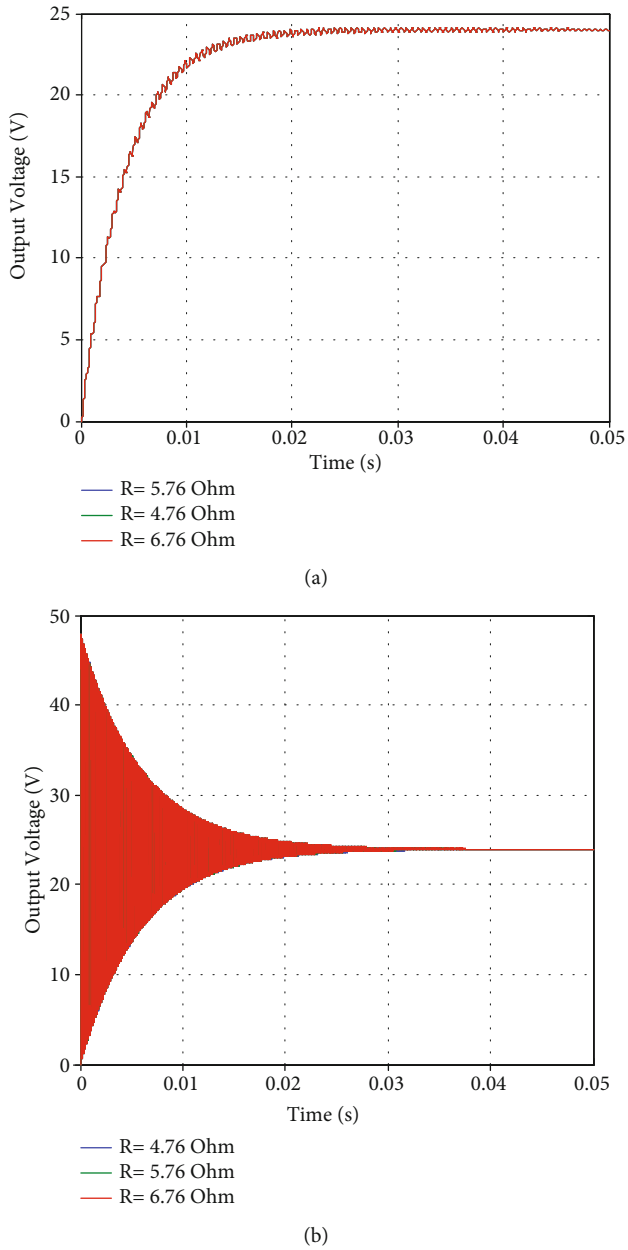

Figure 11: Simulated V_o results of FKYBC for various R (a) with HPC and (b) with PID control.

lightly damped result matches to the set final value of FKYBC result. The peak time of the step response is $T_d/2$. Next, this time delay, the complete value of the step reference is smeared to $G(s)$, ensuring that the V_o remains constant at set value. Alternative clarification is that the set value, which was previously removed from the input, now cancels any undesirable overshoots since it is delayed by $T_d/2$.

5.2. Fundamental of Posicast. The main components of new HPC, $P(s)$ is a scaling factor parameterized by λ and the time delay element parameterized by T_d. There are two design steps for new HPC. First, $P(s)$ is developed for the averaged model of the FKYBC. Then, $C(s)$ is framed to compensate joined model of the $(1 + P(s))\, G(s)$. The classical frequency domain approach is provided. A pure integrator type compensator is matched for the FKYBC to stabilize steady-state disturbances.

$$C(s) = \frac{k}{s}. \tag{15}$$

The K gain is selected to reduce the settling time as much as feasible, but not to the point where the overshoot is excessive. A new HPC model (16) is attained by joining the compensator $C(s)$ and the $P(s)$.

$$C(s)(1 + P(s)) = \frac{K}{s}\left(1 + \frac{\lambda}{1+\lambda}\left(e^{-s(T_d/2)} - 1\right)\right). \tag{16}$$

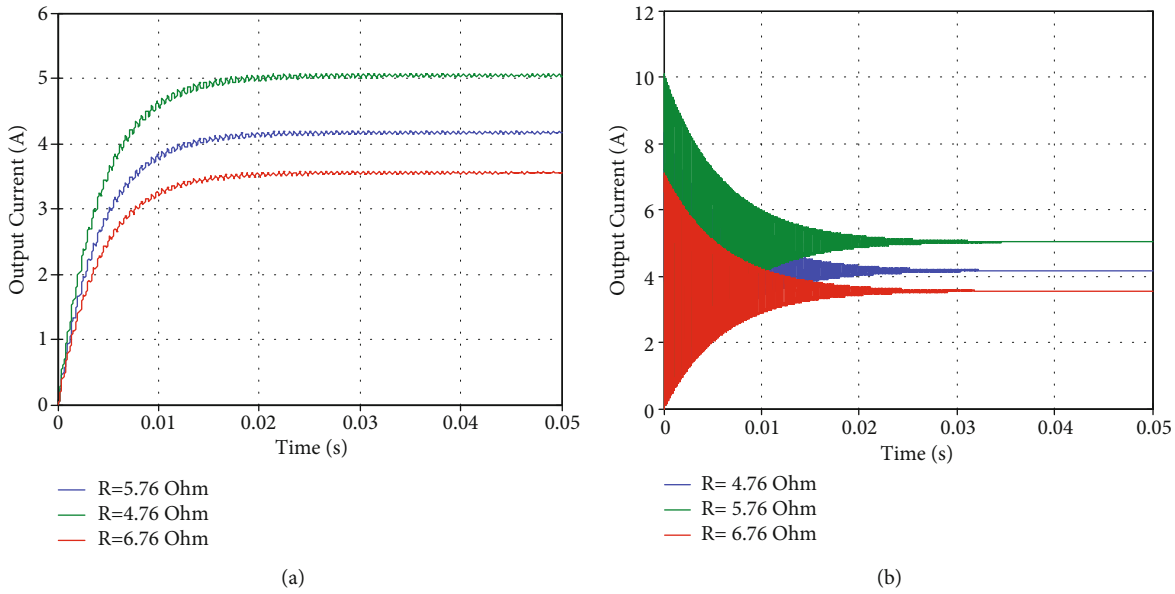

FIGURE 12: Simulated responses of I_o of FKYBC for unalike load R (a) with HPC and (b) with PID control.

5.3. New HPC. The small signal transfer function model of FKYBC along with their specifications is

$$G(s) = \frac{\hat{v}_o}{\hat{\lambda}} = 16\left(\frac{(144125275)}{(s^2 + 240s + 144349820)}\right). \quad (17)$$

Undamped natural frequency is

$$\omega_n = \sqrt{\frac{1}{LC}}, \quad (18)$$

$$T_d = \frac{2\pi}{\omega_n\sqrt{1-\zeta^2}}, \quad (19)$$

$$\lambda = e^{-\pi\zeta/\sqrt{1-\zeta^2}}. \quad (20)$$

The values of the new HPC parameters are computed using Equations (18) to (20). Then, $T_d = 0.00053$ s and $\lambda = 0.978$. The K is designed to be as large as possible to reduce settling time while avoiding unjustified overshoot, and it is set to be 15 in this work.

Substituting the controller parameters in (16), it is rewritten as

$$C(s)[1 + P(s)] = \frac{15}{s}\left[1 + 0.492\left(e^{-0.000265s} - 1\right)\right]. \quad (21)$$

Figure 6 shows the frequency analysis of HPC in an open-loop function, $C(s)\,(1 + P(s))\,G(s)$. The gain margin remains 392 db, while the phase margin is around 89.8°.

5.4. PID Controller. For the V_o of FKYBC, standard controllers based on the PID control are frequently utilized. The PID controller approach may effectively control the low-order dynamics of power modulators.

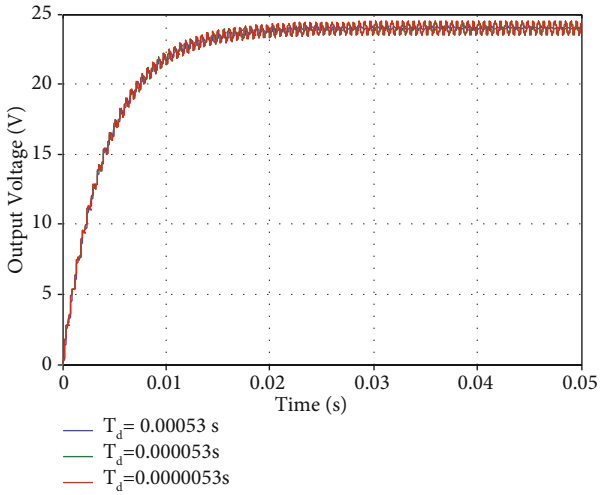

FIGURE 13: Simulated response of V_o of FKYBC with HPC for dissimilar T_d.

The PID controller is difficult to surpass in this case because the integrator raises the converter type number, reducing the error (steady sate). Controller has double zeros allowed for resonant physiognomies to be dampened and the transient result to be enhancing. The PID controller is simple structure for understanding in comparison with other control methodology. For new HPC comparison, the PID compensator was designed for the FKYBC. In this article, the Ziegler Nichols tuning method [7, 15, 20] is used to evaluate the PID control parameters for transfer function model FKYBC, which are derived from the previous sections. Then, transfer function of PID control is expressed as (22), and its frequency response of open-loop function is illustrated in Figure 7.

$$G_C(s) = 0.051 + \frac{200}{s} + 0.95s. \quad (22)$$

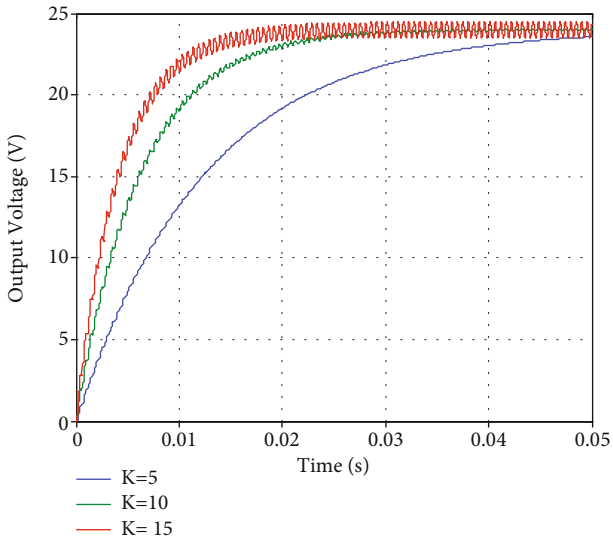

Figure 14: Simulated results of V_o of FKYBC with HPC for various K.

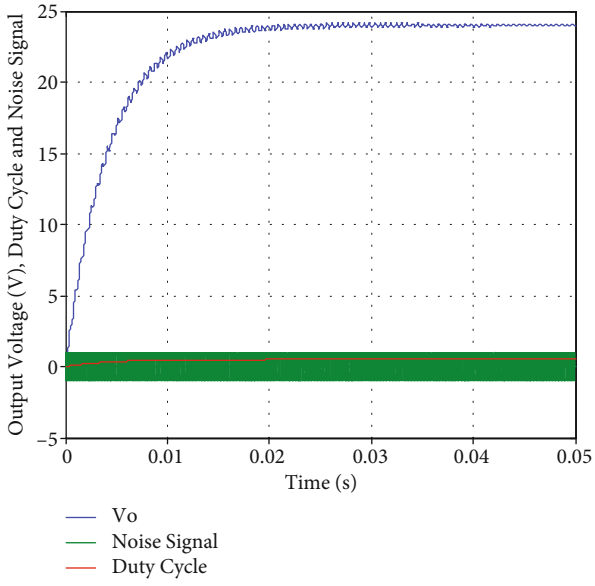

Figure 15: Simulated results of V_o, δ, and noise of FKYBC with controller for constant V_{in} and controller parameters.

From Figures 6 and 7, new HPC with system removes huge frequency noise superior than the PID control.

6. Simulation Results and Discussions

Simulation results and discussions of FKYBC with HPC and PID controllers are discussed in this part. The enactment of same converter with controllers is tested at various operating conditions via line variations, load variations, and steady-state region changes. The MATLAB/Simulink model of FKYBC with HPC is exposed in Figure 8.

6.1. Line Variations. Figures 9(a), 9(b), and 10 display the simulated V_o and duty cycle of FKYBC with HPC and PID

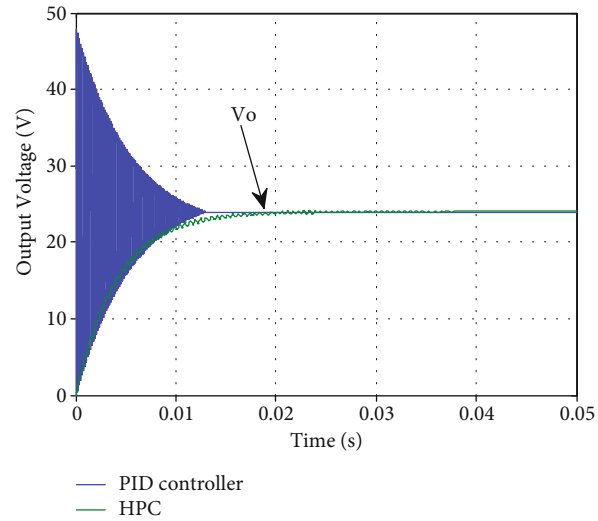

Figure 16: Simulated response of V_o FKYBC for fixed $V_{in} = 16\,V$ and load $R = 5.76\,\Omega$.

Table 2: Variations with HPC for $K = 15$, $T_d = 0.00053\,s$ and $\lambda = 0.978$, $R = 5.76\,\Omega$, $V_{ref} = 24\,V$.

V_{in} (V)	V_o (V)	Deviation (V)
3	23.982	0.018
4	23.990	0.01
5	23.992	0.008
6	23.9925	0.0055
7	23.994	0.006
8	23.9951	0.0051
9	23.9961	0.0031
10	23.997	0.003
11	23.998	0.002
12	23.9984	0.0016
13	23.9986	0.0014
14	23.999	0.001
15	23.999	0.001
16	24	Nil
17	24.01	0.01
18	24.02	0.02
19	24.04	0.04
20	24.06	0.06

control in transient state for various V_{in} such as 12 V, 16 V, and 18 V, respectively. From these responses, it is evident that the FKYBC with HPC has produced null overshoots and quick settling times of 0.02 s, 0.017 s, and 0.016 s, respectively, whereas the same model with PID control had more overshoots of 22 V and settling times of 0.032 s, 0.03 s, and 0.028 s at different V_{in}.

6.2. Load Variations. Figures 11 and 12 demonstrate the simulated responses in the start-up for V_o and output current of FKYBC with HPC and PID control for various load

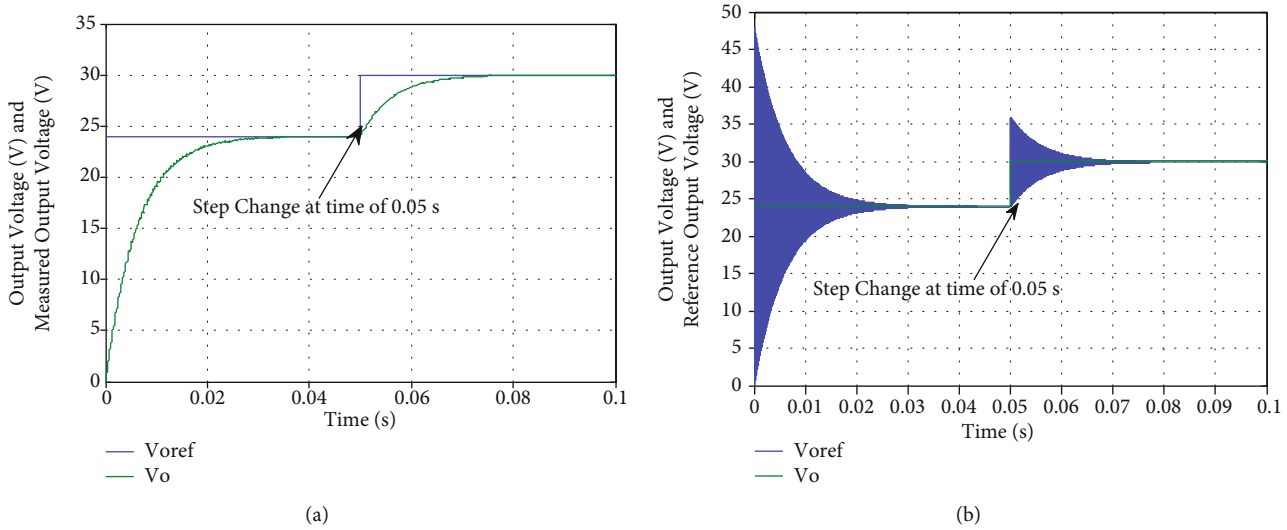

FIGURE 17: Response of V_o of FKYBC with designed controller when reference output voltage from 24 V to 30 V: (a) HPC and (b) PID control.

R such as 4.76 ohm, 5.76 ohm, and 6.76 ohm. It is seen that V_o of the same converter with HYC has produced insignificant overshoot and settling time of 0.022 s, 0.021 s, and 0.02 s, while FKYBC model with PID control have generated more overshoots of 22 V and settling times of 0.032 s, 0.031 s, and 0.028 s at different load R.

6.3. Various Controller Parameters. The simulated V_o responses of the FKYBC with HPC for various values T_d and compensator gain K are displayed in Figures 13 and 14. From these results, it is evident that V_o of FKYBC with control has null overshoots and minimal steady-state error for different values of T_d and K.

Figure 15 shows the simulated V_o, δ, and noise quantity of the FKYBC with HPC. It is visibly seen that the V_o of FKYBC with new HPC has null overshoots and quick settling time during noise signal.

6.4. Comprehensive Analysis of Controllers. Figure 16 shows the simulated V_o responses of FKYBC using an HPC and a PID controller. Over the PID controllers, the V_o of FKYBC with HPC has a negligible overshoot, a rapid settling time, and excellent noise suppression. The proposed HPC has performed well in this region.

6.5. Steady-State Region and Set Point Variations. Table 2 shows the recorded simulated output voltage of FKYBC with HPC for various V_{in} from 3 V to 20 V in steady-state region. From this table, it is found that the designed controller has proficient performance during the steady-state operating condition with small deviations. Figures 17(a) and 17(b) show the simulated V_o responses of FKYBC with HPC and PID control for the step change reference output voltage from 24 V to 30 V. From these figures, it is evident that the designed HPC is performed well during step change reference output voltage without overshoot and quick settling time over the PID control.

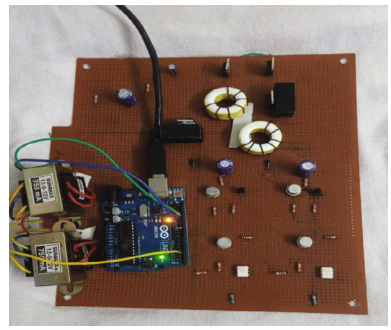

FIGURE 18: Hardware model of FKYBC with HPC.

7. Experimental Results and Discussions

Experimental result of FKYBC with HPC is discussed in this section. The performance of the FKYBC with HPC is verified at transient state and line variations. The prototype model of FKYBC with HPC (LED driver load) is shown in Figure 18. The parameters of the power circuits are as follows:

$S_1 - S_2$ IRFN 540 (MOSFET)
D_b FR306 (Diodes)
$C_b - C_o$ 1953 μF&866 μF/1000V
$L8\mu$H/5A

The constraints of the HPC are implemented in ArduinoUno-ATmega328P microcontroller as shown in Figure 18. Here, opto-coupler MCT2E along with amplification circuit is used as driver circuit. Figures 19(a)–19(c) show the experimental V_o and V_{in} responses of the FKYBC with HPC through the transient region and input voltage changing from 16 V to 12 V and 16 V to 18 V. From these results, it is evident that the FKYBC with HPC has minimal peak overshoots and quick settling time in line and start-up regions. Figure 20 shows the graphical numerical simulation and experimental analysis of output voltage of FKYBC with

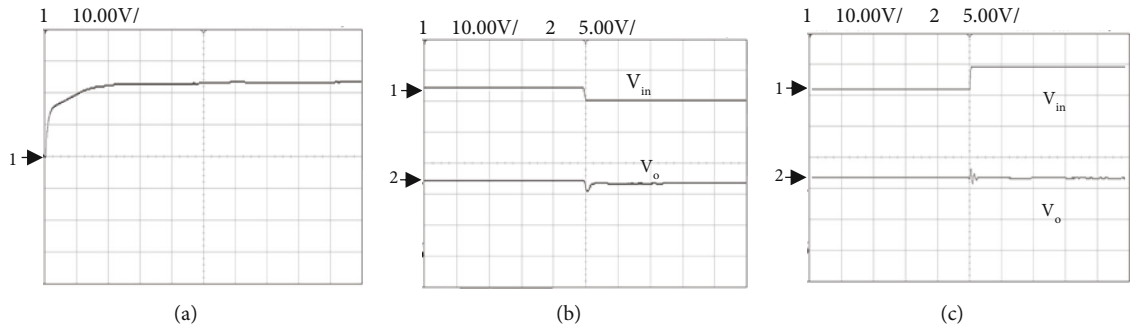

Figure 19: Experimental V_o responses of FKYBC with HPC: (a) transient state, (b) input voltage change from 16 V to 12 V, and (c) V_{in} change from 16 V to 18 V [Ch 1: 10 V/Div, Ch 2: 5 V/Div].

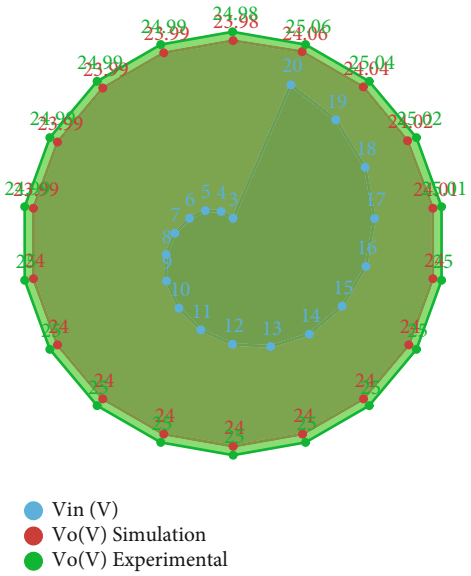

Figure 20: Graphical numerical simulation and experimental analysis of V_o of FKYBC with HPC at different V_{in}.

HPC at various input voltage. From this result, the small deviations of V_o of same converter with different input voltage for simulation/experiments are found.

8. Conclusion

A new HPC for output voltage regulation of FKYBC in CCM has been established effectively using Simulink software besides prototype models. The new HPC parameters were implemented in digital platform with the help of the Arduino Uno-ATmega328P microcontroller. The elements of posicast are directly computed for analytical and ideal approaches of FKYBC. The main benefits of new designed HPC over PID control have better damping abilities, proficient output voltage regulation in line/load variations, minimized overshoots, quick settling time, reduced high frequency noise, easy digital implementation, and minimizing sensitivity of traditional approach. The steady-state response of the FKYBC has improved based on the integral compensator along with single gain of new HPC. In gap to the PID control, the new HPC only desires to adjust the K, and the compensated plant has enhanced the gain/phase margins and, its constricted open-loop bandwidth confirms conquest of huge frequency noise. Finally, the designed new HPC has proficient output voltage regulation for FKYBC in CCM. It is apt for power supply in LED driver, medical instruments, solar system, and mobile communication.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] F. L. Luo and H. Ye, *Essential DC–DC Converters*, CRC Press & Taylor & Francis Group, New York, 2006.

[2] F. L. Luo and H. Ye, "Positive output super-lift converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 105–113, 2003.

[3] K. I. Hwu and Y. T. Yau, "Two types of KY buck–boost converters," *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 2970–2980, 2009.

[4] K. I. Hwu, W. C. Tu, and Y. H. Chen, "A KY boost converter," *IEEE Transactions on Power Electronics*, vol. 25, pp. 2699–2703, 2009.

[5] K. I. Hwu and Y. T. Yau, "KY converter and its derivatives," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 128–137, 2009.

[6] O. J. M. Smith, "Posicast control of damped oscillatory systems," *Proceedings of the IRE*, vol. 45, no. 9, pp. 1249–1255, 1957.

[7] L. Guo, J. Y. Hung, and R. M. Nelms, "PID controller modifications to improve steady-state performance of digital controllers for buck and boost converters," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, pp. 381–388, Dallas, TX, 2002.

[8] G. Cook, "An application of half-cycle posicast," *IEEE Transactions on Automatic Control*, vol. AC-11, no. 3, pp. 556–559, 1966.

[9] J. Y. Hung, "Feedback control with posicast," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 1, pp. 94–99, 2003.

[10] D. Sumanth, R. Janga, and P. Vijay, "Design of conventional controller for KY converter based standalone hybrid system with state space modelling," *International Journal of Engineering Research & Technology (IJERT)*, vol. 8, no. 16, pp. 187–191, 2020.

[11] K. I. Hwu, W. Z. Jiang, and J.-J. Shieh, "Study and simulation on control-to-output transfer function of KY boost converter," *IECON2015-Yokohama*, vol. 9-12, pp. 000146–000149, 2015.

[12] K. R. Kumar, "FLC and PWM SMC for KY boost converter," *Journal of Circuits, Systems and Computer*, vol. 28, no. 11, pp. 0218–1266, 2019.

[13] K. Ramash Kumar, N. Arunkumar, and T. S. Sivakumaran, "Implementation of non-linear controller for contemporary DC-DC converters," *International Journal on Electrical Engineering and Informatics*, vol. 11, no. 4, pp. 622–637, 2019.

[14] S. Muthukaruppasamy, A. Abudhahir, A. Gnana Saravanan, J. Gnanavadivel, and P. Duraipandy, "Design and implementation of PIC/FLC plus SMC for positive output elementary super lift Luo converter working in discontinuous conduction mode," *Journal of Electrical Engineering and Technology*, vol. 13, no. 5, pp. 1886–1900, 2018.

[15] C. T. Rim, G. B. Joung, and G. H. Cho, "A state space modeling of non-ideal DC-DC converters," in *IEEE Power Electronics Specialists Conference*, pp. 943–950, Kyoto, Japan, 1988.

[16] J. J. Babu and V. Thirumavalavan, "Switched-mode Luo converter with power factor correction and fast regulation under transient conditions," *Soft Computing*, vol. 24, pp. 13319–13329, 2020.

[17] K. Udhayakumar, P. Lakshmi, and K. Boobal, "Hybrid posicast controller for a DC-DC buck converter," *Serbian Journal of Electrical Engineering*, vol. 5, no. 1, pp. 121–138, 2008.

[18] R. Adlakha, A. Khosla, and D. Joshi, "Comparative analysis of positive output super lift DC-DC Luo converters," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 18, no. 2, pp. 707–716, 2020.

[19] K. Ramash Kumar and S. Jeevananthan, "Analysis, design and implementation of hysteresis modulation sliding mode controller for negative output elementary boost converter," *Journal of Electric Power Components and Systems*, vol. 40, no. 3, pp. 292–311, 2012.

[20] R. D. Middlebrook and S. Cuk, "A general unified approach to modeling switching converter stages," in *IEEE Power Electronics Specialists Conference*, pp. 18–34, Cleveland, OH, USA, 1976.