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Research Article

A Virtual Fabrication and High-Performance Design of 65 nm Nanocrystal Floating-Gate Transistor

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Floating-gate transistor lies at the heart of many aspects of semiconductor applications such as neural networks, analog mixed-signal, neuromorphic computing, and especially in nonvolatile memories. The purpose of this paper was to design a high-performance nanocrystal floating-gate transistor in terms of a large memory window, low power, and extraordinary erasing speeds. Besides, the transistor achieves a thin thickness of the tunnel gate oxide layer. In order to obtain the high-performance design, this work proposed a set of structure parameters for the device such as the tunnel oxide layer thickness, Interpoly Dielectric (IPD), dot dimension, and dot spacing. Besides, this work was successful in the virtual fabrication process and methodology to fabricate and characterize the 65 nm nanocrystal floating-gate transistor. Regarding the results, while the fabrication process solves the limitation of the tunnel oxide layer thickness with the small value of 6 nm, the performance of the transistor has been significantly improved, such as 2.8 V of the memory window with the supply voltage of ±6 V at the control gate. In addition, the operation speeds are compatible, especially the rapid erasing speeds of 2.03 μs, 28.6 ns, and 1.6 ns when the low control gate voltages are ±9 V, ±12 V, and ±15 V, respectively.

1. Introduction

The solid-state floating-gate transistor was introduced in 1967 by Pearson, Kahng, and Sze [1]. Over the past decades, the transistor has been considered a vital component in semiconductors such as analog mixed-signal, artificial intelligence, neuromorphic computing, and especially nonvolatile memories [2–4]. There are many compelling reasons why the floating-gate transistor has been widely used in many applications. First, the transistor has an extraordinary feature that is nonvolatile, and the feature can retain data even when removing the power supply. Secondly, the threshold voltage of the device is not one constant value as in the traditional MOSFET; hence, the floating-gate transistor has been becoming an essential element in multilevel cell memories, analog mixed-signal, and neural network, etc. applications where the transistor is used as the flexible control element [5, 6].

In recent years, the industry has demanded the scaling down of semiconductor devices to satisfy the three key requirements including high density, rapid speed, and low power [7–11]. However, for the specific 65 nm process, the limitation of the tunnel oxide layer thickness, which is one of the most critical parameters of the device, is 9 nm which would not decrease to follow the scaling trend [12, 13]. The tunnel layer, which allows the charges from quantum dots to go through in the write and erase operations, directly affects the performance of the floating-gate transistor like memory window, operation speeds, endurance, and especially leakage power. Regarding the leakage power, in the advanced technology nodes, the scaling down dimension of the semiconductor device caused the leakage current to become dominant and impact the quality of devices, especially when the thickness of the tunnel oxide layer is thin. Figure 1 illustrates the impacts of the leakage current of the floating-gate transistor [14]. In the high electric fields,

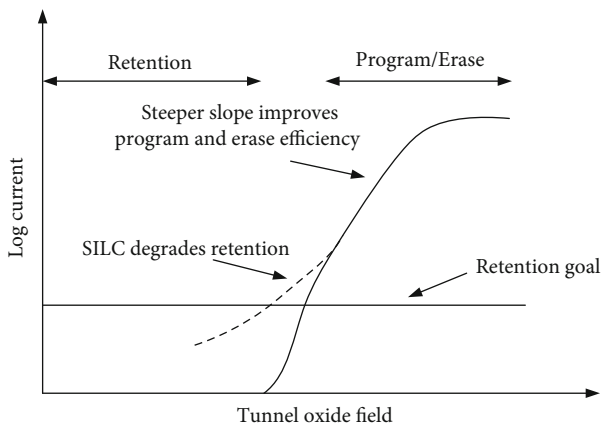

Figure 1: Tunnel oxide field versus log current of the tunnel oxide layer [14].

a steep slope will provide the achievements of fast writing and erasing speeds. However, in the low electric fields, when the charges must be retained in the storage gate, the figure shows that the Stress-Induced Leakage Current (SILC) occurs and degrades the retention feature.

Much research has been published to deal with the limitation of tunnel layer thickness which is causing the problems mentioned above, such as work [1] which showed the graphene flash memory (GFM), which enhanced the controlling carrier concentration and the performance of devices such as high speed and low leakage current. In 2019, work [15] obtained an excellent Fowler-Nordheim tunneling process by deploying new materials like Antiferroelectric (AFE) and Silicon-doped Hafnium Oxide (HSO). Among the publishes, one attempt to improve the performance is studying a promising structure called a nanocrystal floating-gate transistor. The design replaces the continued floating gate of the conventional structure with a sea of quantum dots for storage charge purposes. There are many papers focused on that nanocrystal structure recently. The work [16] fabricated a nanocrystal memory device called MIS (metal insulator semiconductor). The materials are investigated to improve the leakage current and retention feature, such as hafnium dioxide (HfO_2) as the high k tunnel oxide layer, and germanium (Ge) for the nanocrystal layer. In 2016, the authors in [17] proposed a nanocrystal structure with only 3.3 nm, 5 nm, and 10 nm thicknesses of the tunnel, storage charges, and Interpoly Dielectric (IPD) layers, respectively. With regard to the performance, while the work obtained a large memory window of 3 V, the disadvantages are the considerably high control gate voltage of 12 V and the low writing speed of 0.3 s. On the other hand, in 2018, the work in [18] provided the 0.2 s and 0.04 s of the writing and erasing speeds, respectively. However, this work obtained a small value of 1.2 V memory window with the control gate voltage of 10 V. Regarding this study, the proposed nanocrystal floating-gate transistor can achieve a large memory window of 10.1 V and high write speed and erase speed values of 0.05 s and 28.6 ns, respectively. With that good performance, especially the extraordinary erasing speed, this work shows better values when it comes to the studies in [19, 20], where the memory windows are less than 2 V in work [19] and only 2.5 V in work [20]. In work [19], while the write speeds are compatible to this work, the erasing speeds are 0.215 s and 0.18 s for the two experiments which are much lower compared with this proposed nanocrystal floating-gate transistor.

Thus, it is clear that although the mentioned studies have solved the scaling down problem, the performances of the floating-gate transistor are not optimized and achieved compatible results. Therefore, this paper suggested designing a high-performance nanocrystal floating-gate transistor in terms of a large memory window, low power, and extraordinary erasing speeds. Furthermore, in order to achieve the targets, this study proposed the set of optimized structure parameters as well as the successful virtual fabrication processes and the methodology to fabricate and characterize the 65 nm technology node. The fabrication consists of two-dimensional and three-dimensional processes. This paper shows that the designed transistor can be fabricated with a thin thickness of the tunnel layer with a value of 6 nm. While the thickness value ensures the leakage current, the proposed device has a compatible performance compared to the previously published works, such as an excellent memory window of 2.8 V with a low control gate voltage of ±6 V, and the compatible writing speed is 0.05 s. In particular, the extraordinary erasing speeds can be achieved at the values of 2.03 μs, 28.6 ns, and 1.6 ns when the control gate voltages are ±9 V, ±12 V, and ±15 V, respectively.

The remainder of this work is organized as follows: Section 2 introduces an overview structure and modeling of the nanocrystal floating-gate transistor. Moreover, the virtual fabrication processes and methodology for the two-dimensional and three-dimensional designs are also presented in this section. Section 2 also gives the complete fabrication parameters and conditions. Next, the results of the characterization and discussion are shown in Section 3. Finally, Section 4 gives the conclusion.

2. Nanocrystal Floating-Gate Transistor: Concepts and Virtual Fabrication Processes

2.1. Nanocrystal Floating-Gate Transistor: Concepts. Researchers have investigated a CMOS-based design that is the floating-gate transistor recently. The floating-gate device has one more gate, which is floating, than the traditional MOSFET, which makes the critical nonvolatile feature of the floating-gate transistor. Figure 2(a) demonstrates the conventional floating-gate transistor with the additional floating gate fabricated below the IPD layer that can be fabricated by Oxide-Nitride-Oxide (ONO) layers and above SiO_2 layers for storage charge purposes.

Figure 2 demonstrates a conventional floating-gate transistor and a new structure where the silicon quantum dots are used as the floating gate. In Figure 2(a), there are two polysilicon (Poly) gates which are floating and control gates. The upper layer is the control gate, which is applied with a high voltage during operation, and the floating one surrounded by oxide layers is the floating gate. The layer placed between the two layers above is the IPD. Moreover, the

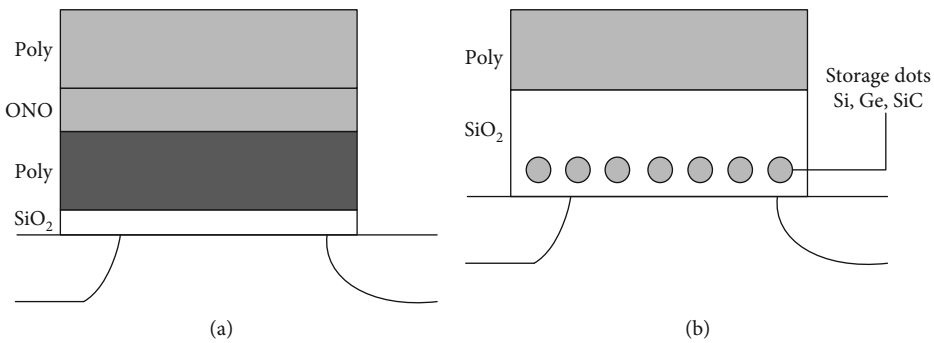

Figure 2: Floating-gate transistor structure: (a) conventional; (b) nanocrystal [22].

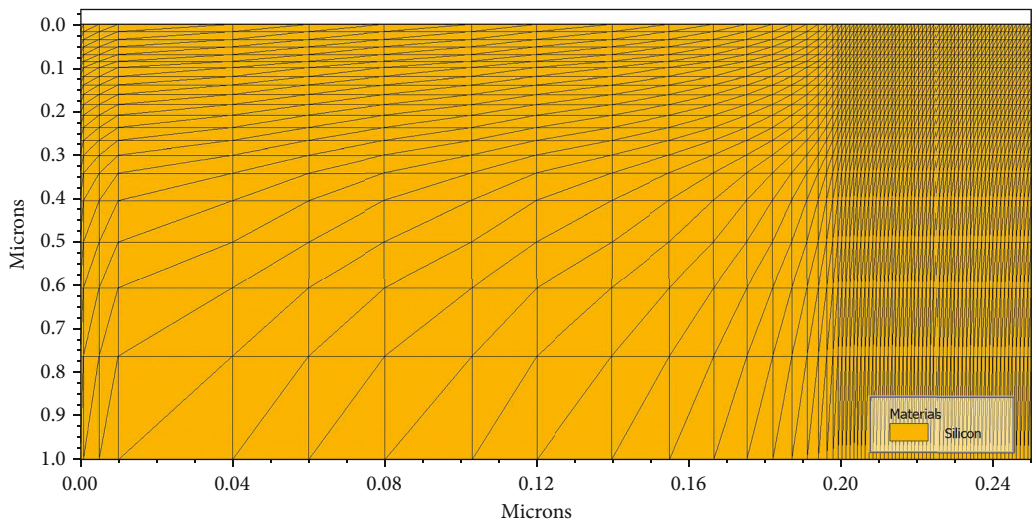

Figure 3: Mesh design.

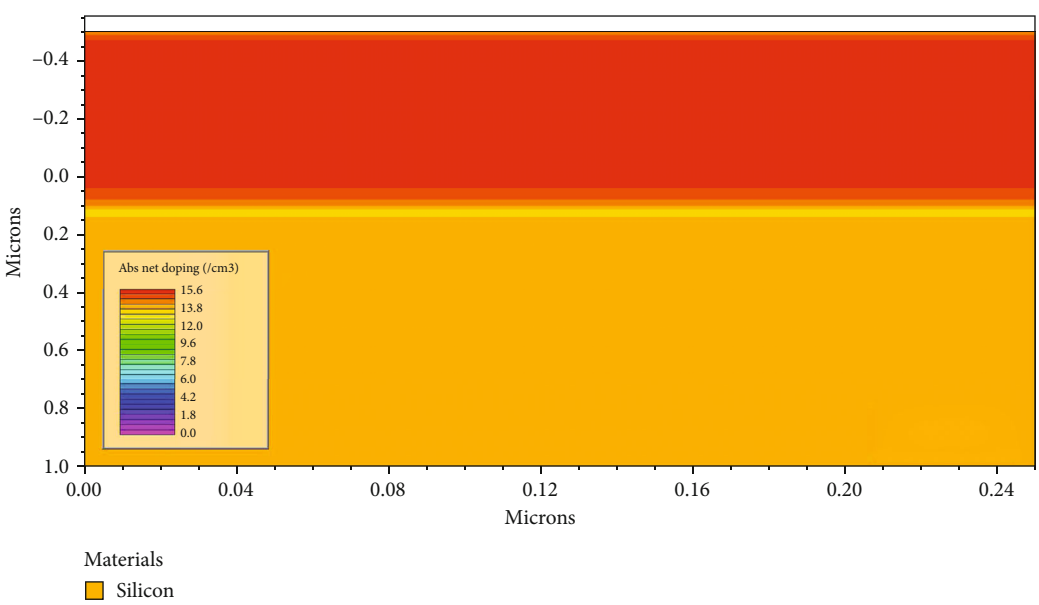

Figure 4: Epitaxy layer creation.

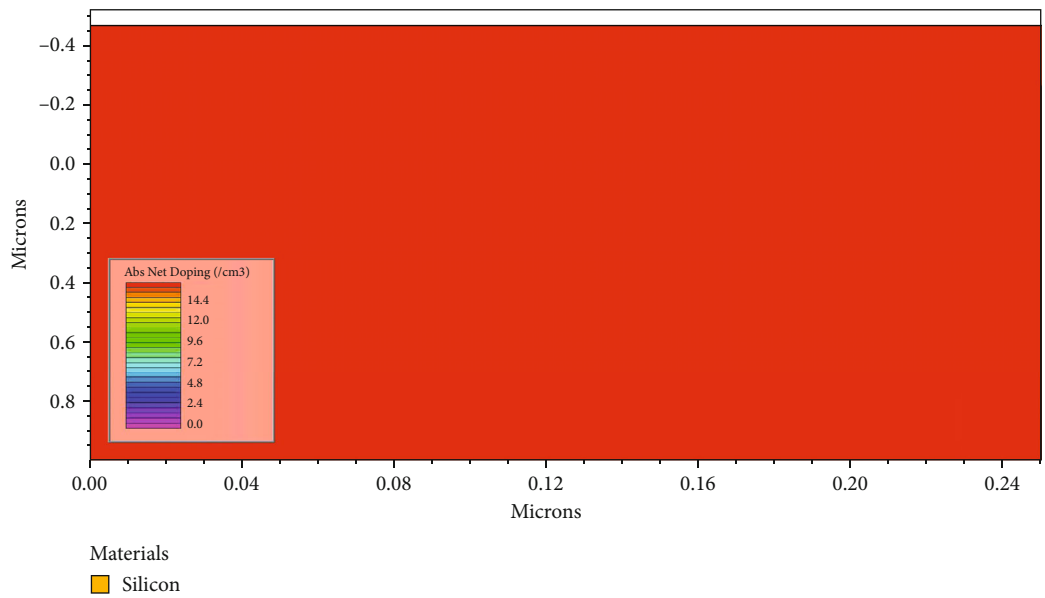

Figure 5: P well creation.

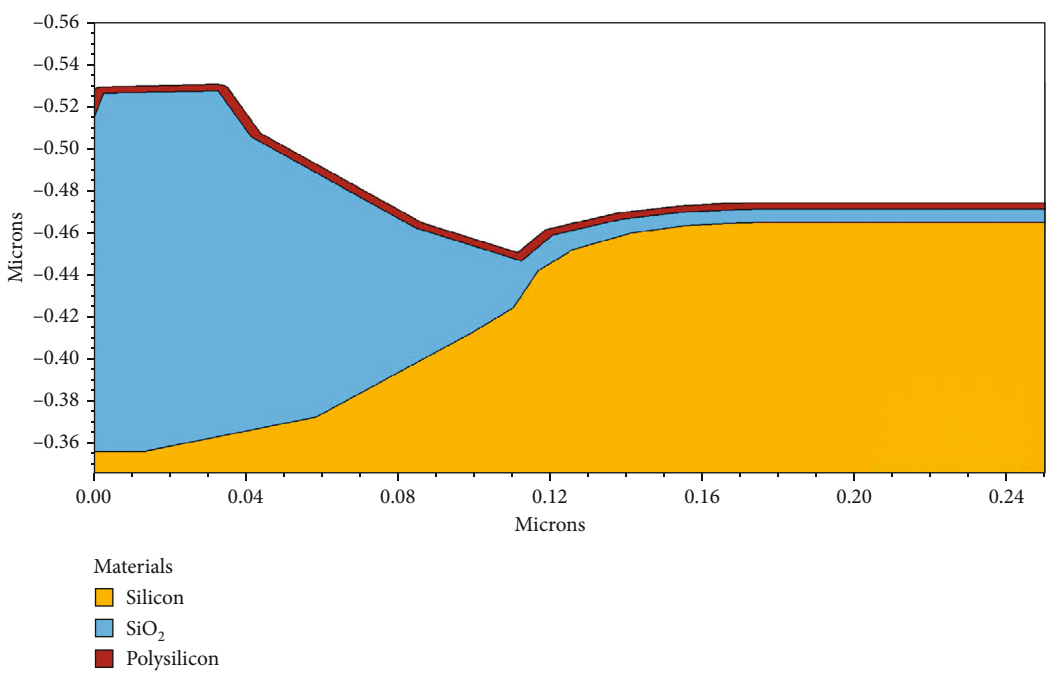

Figure 6: Continuous floating-gate creation.

crucial tunnel oxide layer is fabricated under the floating gate. The thickness of the tunnel oxide has to be considered carefully because of the transfer charge behavior during the writing and erasing configurations. Furthermore, the one should have a reasonable thickness in order to guarantee the reliability feature when the power supply is removed [21].

This is because all the charges are stored on a polysilicon gate that makes the conventional structure tend to fail due to isolation, where the critical discharge paths occur if any weak points appear, which dramatically affects the quality of the device. To prevent failure, the charges are distributed on the quantum dots. A representation of this structure is given in Figure 2(b). While the conventional floating-gate transistor has a continuous floating gate, the new structure has many discrete nodes for charge storage. Furthermore, the nanocrystal structure offers several advantages compared to the conventional one. First, the main advantage is that the tunnel oxide thickness is thicker while still preserving the fundamental operation principles. Second, the power supply

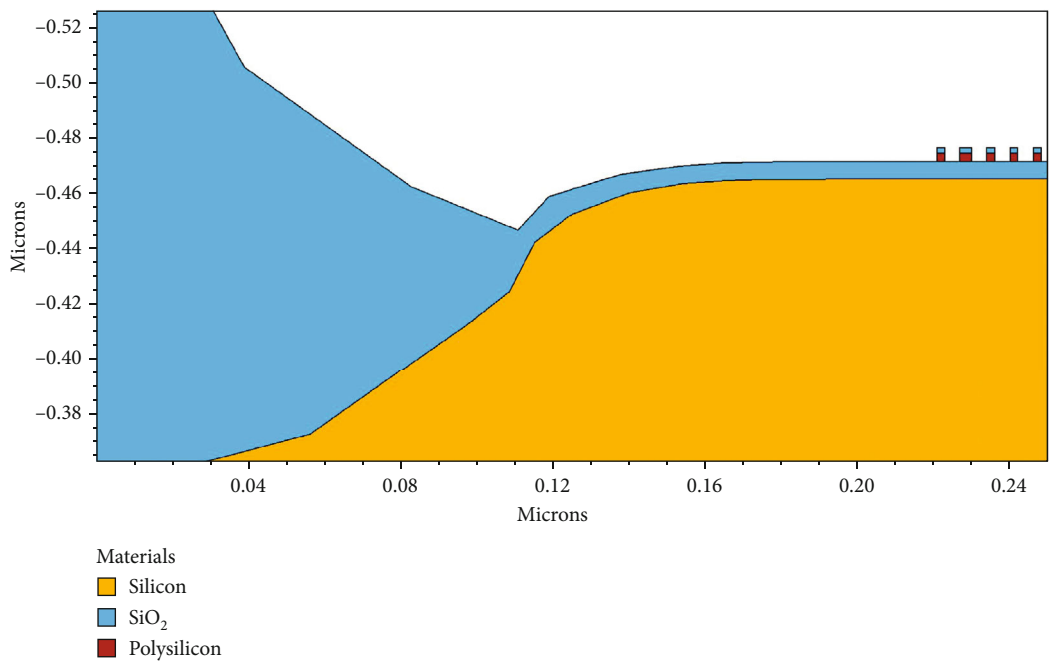

Figure 7: Quantum dot creation.

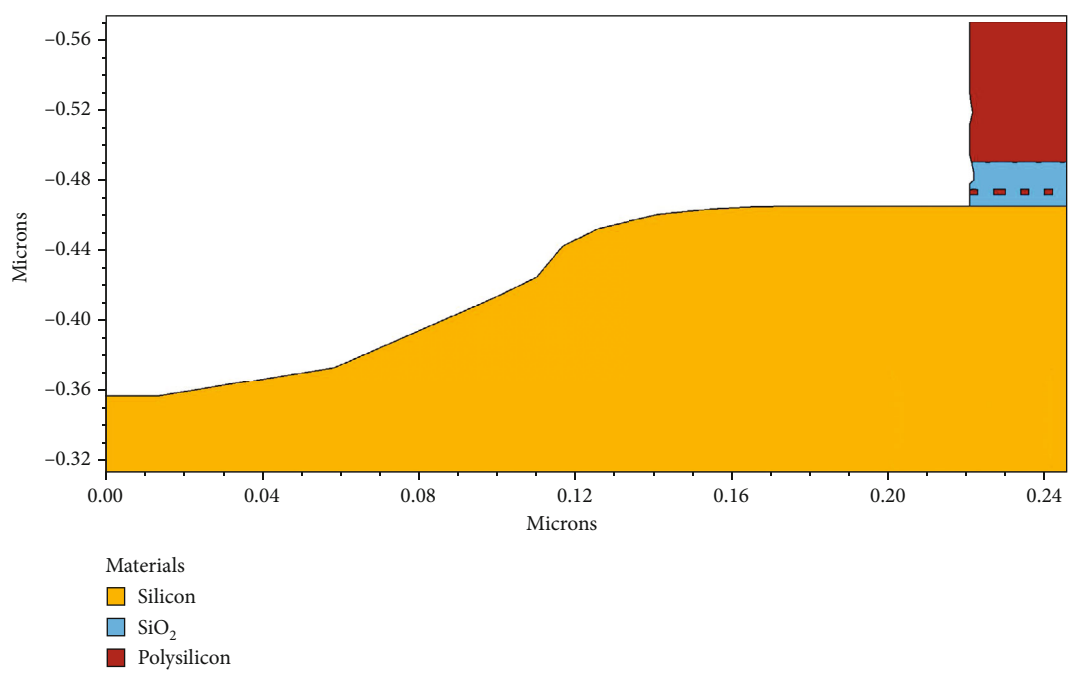

Figure 8: IPD layer creation.

is lowered when the thickness of the tunnel layer is decreased. Last, the structure obtains high operation speeds.

The biggest challenge when fabricating the nanocrystal floating-gate transistor is that while the quantum dots should be small, dense, and uniform, an extreme density leads to the dots acting the same as the continued floating gate [14]. Regarding the operation, there are three states: write, erase, and read. Whereas the write and erase states will provide the memory window value, which is one of the most important values to evaluate the transistor's quality, the read state is used to determine whether the transistor is at the write or erase state. This work provides the fundamental characterization in Section 3 as well.

2.2. Nanocrystal Floating-Gate Transistor: Virtual Fabrication Process. This section presents the essential steps and methodologies of the virtual fabrication process. Furthermore, the complete parameters and fabrication conditions are

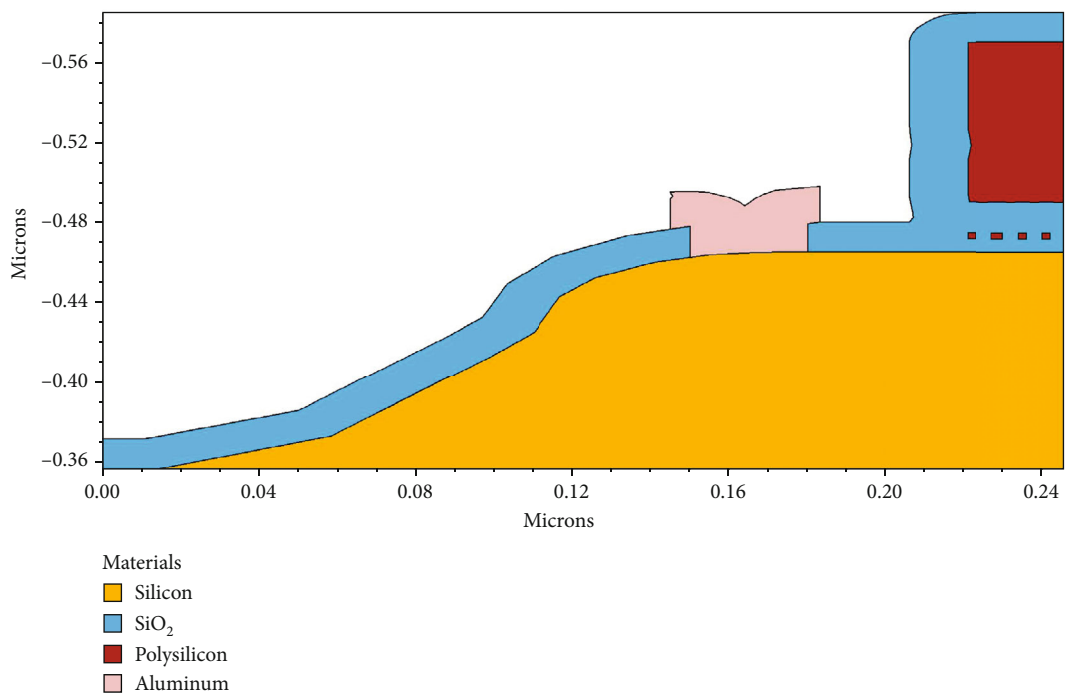

Figure 9: Source and drain creation.

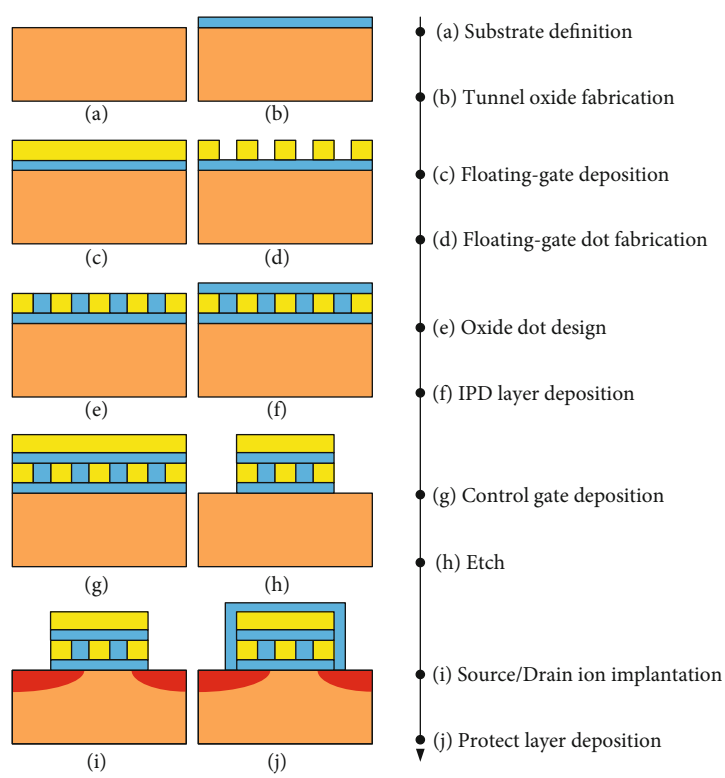

Figure 10: Virtual fabrication process.

shown. In this work, the TCAD tools including Athena, DevEdit3D, and Tonyplot tools were used in fabricating the two- and three-dimensional designs.

With regard to the two-dimensional design, the flow consists of ten main steps to fabricate the virtual structure. Firstly, the process begins by designing the mesh and is followed by determining the wafer usage. The mesh, which plays an important role in the proposed process, was accurately defined because of the significant impact of simulation accuracy and simulation time, which are trade-offs [23].

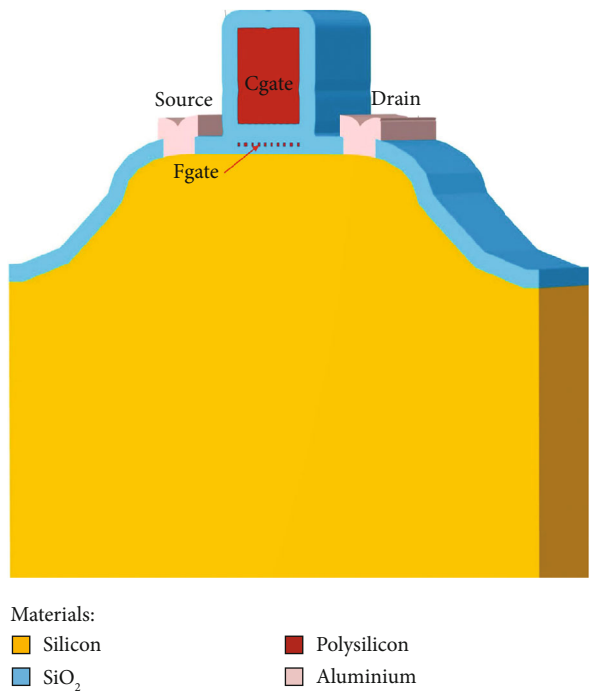

Figure 11: Virtual fabricated nanocrystal floating-gate structure.

Table 1: Parameters and conditions of the nanocrystal floating-gate transistor fabrication processes.

Fabrication steps	Simulated conditions
2D* mesh	x-axis from 0 to 0.25 μm and spacing 0.03 μm (other areas), 0.013 μm (channel), and 0.005 μm in S/D regions y-axis from 0 to 1 μm and spacing 0.01 μm
Silicon (100)	Dope boron 1×10^{14} atoms/cm^3
Epitaxial	Dope arsenic 1×10^{16} atoms/cm^3, 1000°C, and 0.5 μm
P well	Dope boron 8×10^{12} atoms/cm^3 and 100 KeV
Locos	Conventional
Tunnel oxide	890°C and dry oxide
Channel doping	Doped boron 3×10^{12} atoms/cm^3 and 100 KeV
Floating gate	3 nm, dope phosphorus 4×10^{10} atoms/cm^3, and 20 KeV
Silicon dioxide	15 nm
Control gate	80 nm, dope phosphorus 2.5×10^{12} atoms/cm^3, and 30 KeV
Oxide for protecting device	15 nm
Aluminum contacts	18 nm
Source/drain doping	Dope arsenic 1.535×10^{12} atoms/cm^3 and 55 KeV Fermi method (1000°C)

There are two main stages which are designed on the x-axis and y-axis. While the former was defined from 0 μm to 0.25 μm with a spacing of 0.013 μm in the channel and spacing of 0.005 μm and 0.03 μm in the source/drain regions and the rest regions, respectively, the latter is configured from 0 μm to 1 μm with a spacing of 0.01 μm. The mesh is given in Figure 3.

On the other hand, this paper proposed using a silicon wafer with the (100) orientation for the wafer definition, which enhances the process of thermal oxidation compared to others [24]. Next, a substrate of p-type was fabricated with a concentration of boron dopant of 1.0×10^{14} atoms/cm^3. Afterwards, the arsenic dopant was doped with a temperature, time, and concentration of 1000°C, 1 hour, and 1.0×10^{16} atoms/cm^3, respectively. As a result, an epitaxy layer with a thickness of 0.5 μm was created above the substrate and is illustrated in Figure 4. Next, a P well was doped with the boron dopant and is given in Figure 5. The values of the concentration, energy, and temperature are 8×10^{12} atoms/cm^3, 100 KeV, and 1200°C, respectively. In order to obtain the 6 nm thickness as a target in this work, the thermal oxidation with the dry oxide method was adopted with a

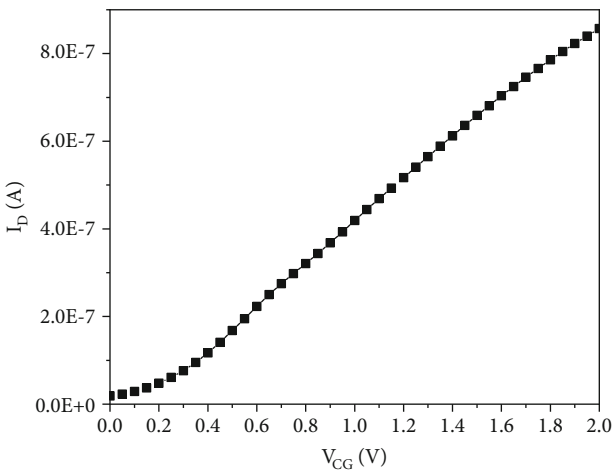

Figure 12: Initial threshold voltage.

Table 2: Input voltages for the initial condition simulation.

	V_{CG}	V_D	V_S	V_{Sub}
Value (V)	2	1	0	0

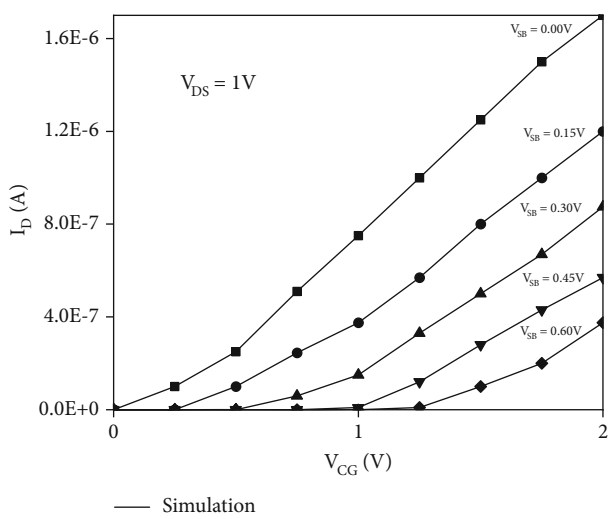

Figure 13: The impact of the V_{SB} on the I_D–V_{CG}.

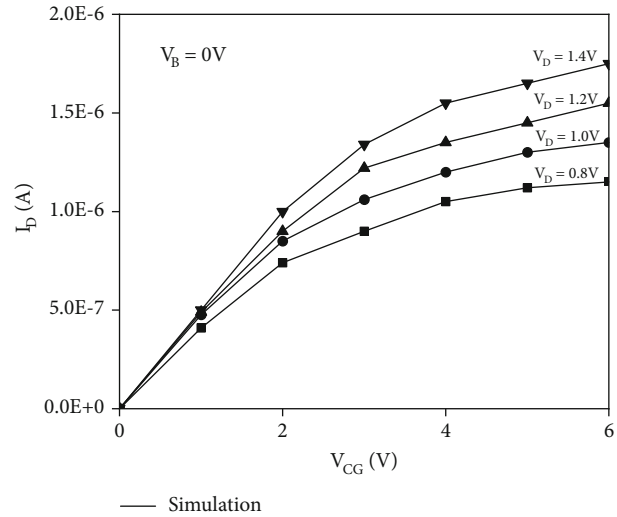

Figure 14: The impact of the V_D on the I_D–V_{CG}.

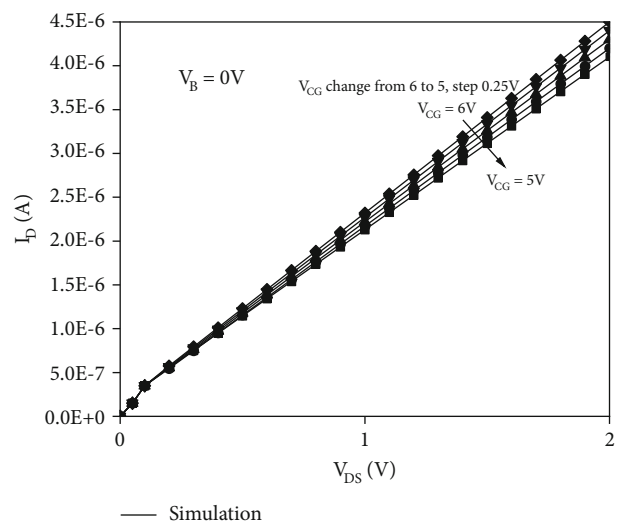

Figure 15: The impact of the V_{CG} on the I_D–V_{DS}.

pressure of 1 atm at 890°C. Meanwhile, the thickness value was calculated carefully before proceeding with the fabrication process. This procedure took precisely 10 minutes in the experiment to obtain exactly 6 nm of SiO_2 thickness.

Next, with an energy of 100 KeV and concentration of 3×10^{12} atoms/cm^3 of boron dopant, the channel was doped. In the third step, the implementation of the quantum dots with the polysilicon material was conducted. That is the main different step between the nanocrystal structure and the conventional structure during fabrication. As mentioned in the section above, the density of the quantum dots would impact the performance of the device, and the main difficulty during fabrication is that while the dots should be small, dense, and uniform, the high density of dots will lead to the dots acting as the continues floating gate. Thus, this work conducted many experiments and found the appropriate value of the dot dimension and spacing for the 65 nm process as follows. First, the continuous floating gate was created and is presented in Figure 6. Second, in the etching process, each quantum dot has height and length dimensions of 3 nm and 2 nm, respectively. Moreover, the dots were doped with the phosphorus dopant with a concentration of 4×10^{10} atoms/cm^3 and 20 KeV energy. The purpose of these steps is that they can improve the electrical conductance of the storage charge dots. Figure 7 demonstrates the quantum dots after design.

With regard to the IPD layer creation, a lot of experiments were conducted to evaluate the thickness of the layer while the device achieves the expected performance simultaneously, by targeting high-quality devices such as a large

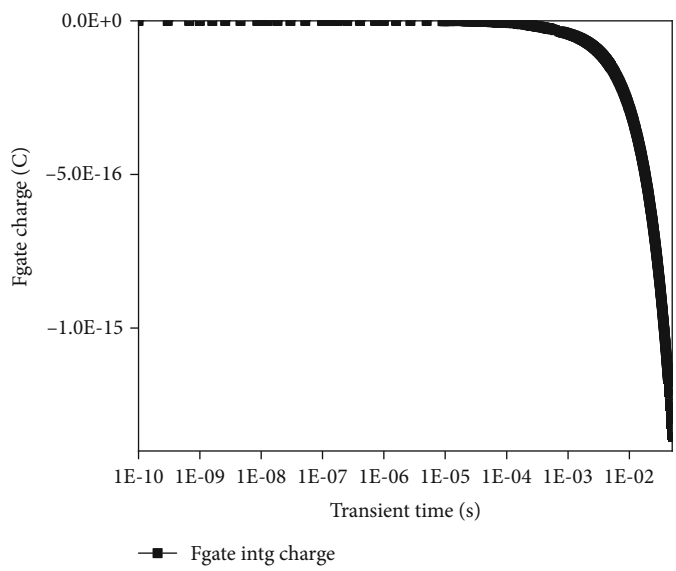

Figure 16: Quantum dot charges in write operation.

Table 3: Input voltages for the write simulation.

	V_{CG}	V_D	V_S	V_{Sub}	T_{Pulse}
Value (V)	6	1	0	0	0.05 s

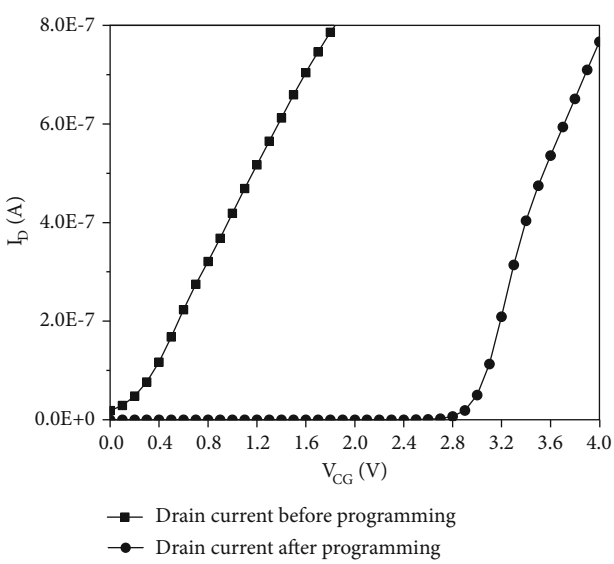

Figure 17: Memory window.

Table 4: Input voltages for the erase simulation.

	V_{CG}	V_D	V_S	V_{Sub}	T_{Pulse}
Value (V)	-6	1	0	0	0.1 s

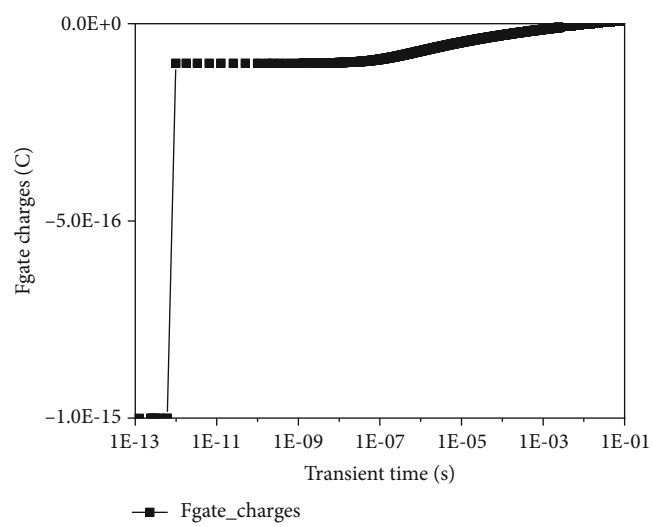

Figure 18: Quantum dot charges in erase operation.

memory window, minimized leakage, and high erasing speed with low supply voltages. The work proposed a value of 15 nm for the silicon dioxide as the IPD layer.

Following this, a thickness of 80 nm of the control gate was designed with materials of polysilicon and phosphorus, which is presented in Figure 8. The energy and concentration are 30 KeV and 2.5×10^{12} atoms/cm^3, respectively, followed by creation of the source and drain regions. The control gate, quantum dots, IPD, and tunnel oxide layers were etched to preserve the source and drain regions. In Figure 9, the drain and source were fabricated by the Fermi method with 55 KeV energy at 1000°C and a concentration of 1.535×10^{12} atoms/cm^3 of arsenic dopant. Finally, a 15 nm thickness of the SiO_2 layer was implemented to protect the device during operation. The virtual fabrication process is given in Figure 10.

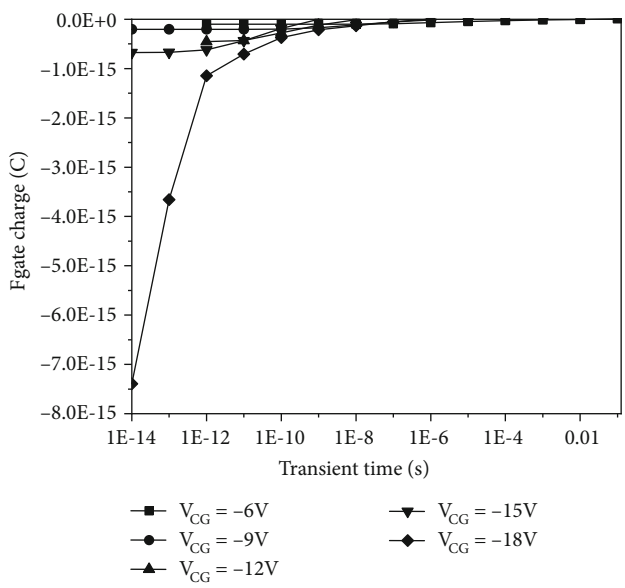

Figure 19: Erase speeds with V_{CG} vary.

To simulate the device's performance, the source and drain terminals were created using an aluminum material with a thickness of 18 nm. The complete structure of the nanocrystal floating-gate transistor is shown in Figure 11, and the detailed parameters and conditions for the virtual fabrication processes are summarized in Table 1.

3. Characterization and Discussion

This section gives the characterization and discussion of the nanocrystal floating-gate transistor, which was designed by the TCAD tools in Section 2. The characterization consists of DC simulations including the threshold voltage at the initial condition, the impact of the voltage of source body (V_{SB}), voltage of drain (V_D) on the drain current I_D versus control gate voltage (V_{CG}) charts, and the impact of the V_{CG} on the I_D versus voltage of drain-source (V_{DS}) behaviors, and the transient simulations such as quantum dot charges during write/erase operations, memory window, and erasing speeds at different conditions. The characterization was performed by the use of the Atlas tool.

3.1. DC Simulations. Figure 12 gives the current of drain (I_D) versus the voltage of the control gate (V_{CG}) of the device, which is used to determine the threshold voltage at the initial condition. From the figure, the control gate voltage change from 0 V to 2 V leads to a significant change in I_D. When the control voltage varies from 0.2 V to 0.6 V, the current rapidly increases from approximately 0.5×10^{-7} A to over 2×10^{-7} A. The configuration of input voltages is given in Table 2 below.

Therefore, the threshold voltage at the initial condition of the nanocrystal floating-gate transistor is 0.2 V. Regarding the impact of the V_{SB} on the I_D–V_{CG} in order to study the body effect of the nanocrystal floating-gate device, Figure 13 shows the changes in the drain current when the V_{SB} varies from 0 V to 0.6 V with the step of 0.15 V. The threshold voltage of the transistor is larger when increasing the V_{SB}; the trend is similar to the traditional MOSFET.

Figures 14 and 15 give the changes of V_D and V_{CG} on the I_D–V_{CG} and I_D–V_{DS} graphs, respectively. The increases in V_D from 0.8 V to 1.4 V result in considerable increases in I_D. The results are as expected as there is no saturation current of I_D compared to the traditional MOSFET, and then, I_D will continue to rise if the V_D increase. Besides, in Figure 15, when V_{CG} decreases from 6 V to 5 V with the step of 0.25 V, the I_D witnesses a slight decrease, which follows the behavior of the nanocrystal floating-gate transistor.

The above DC simulations show that the threshold voltage of the designed transistor of this paper is 0.2 V, and the device characteristics when input voltages changed are stable same as in device theories.

3.2. Write Operation: Quantum Dot Charges and Memory Window. At the beginning, the total of charges on the quantum dots of the designed device is zero. The graph in Figure 16 demonstrates the total charges in the quantum dots during the write operation. The total charges on the quantum dots change from 0 C to -1.4×10^{15} C in 0.05 s. The Hot Electron Injection and Fowler-Nordheim tunneling mechanisms were enabled in this work. Table 3 provides the configuration of input voltages and the period for simulation.

Meanwhile, the threshold voltage of the nanocrystal floating-gate transistor rises from 0.2 V to 3 V. Therefore, the memory window, which is one of the most critical parameters of the device, was determined as 2.8 V.

The threshold voltages of the device during the write operation and the memory window are shown in Figure 17. While the line on the left is the relation between the drain current and control gate voltage at the initial condition, the line on the right is at the write operation.

3.3. Erase Operation: Quantum Dot Charges. In opposition to the write operation, the total charges on the quantum dots will be transferred to the substrate in the erase operation. The condition for input settings is given in Table 4.

Moreover, the Fowler–Nordheim mechanism was enabled for the simulation because it obtained the power dissipation improvement and tunneling efficiency [25]. The results of the erase state are demonstrated in Figure 18. The charges witness a drop from -1.4×10^{-15} C to 0 C, which tends to decrease from 3 V to 0.2 V of the threshold voltage. The value of 0.2 V represents the voltage at the initial state. In other words, the state of the nanocrystal floating-gate transistor changes from after the writing state to the initial state where there is no change in the quantum dots.

The erasing speed depends on the number of charges on the dots and the input voltage of the control gate. In this work, we studied the erasing speeds of the nanocrystal floating-gate transistor with the variation of V_{CG}. The results are given in Figure 19. When the values of V_{CG} are ±6 V, ±9 V, ±12 V, and ±15 V, the erase speeds are 0.1 s, 2.03 μs, 28.6 ns, and 1.6 ns, respectively. Based on the speed values above, this paper achieves promising results in speed when

Table 5: Nanocrystal floating-gate transistor performance comparison.

	[17]		[19]		[20]	This work
Device structure						
Structure	Nanocrystal (underlap channel)	Nanocrystal	Nanocrystal	Nanocrystal	Nanocrystal	Nanocrystal
Underlap channel length (nm)	8	X	X	X	X	X
Tunnel oxide thickness (nm)	3.3	3.3	3.3	3.3	3.3	6
Dot dimension $[x \times y]$ (nm)	3×5	3×5	X	X	3×5	3×3
Dot material/dimension $[x \times y]$ (nm)	Poly/5×5	Poly/5×5	Poly/4×10	Poly/4×10	Poly/5×5	Poly/2×3
IPD material/thickness (nm)	SiO_2/10	SiO_2/10	SiO_2/10	SiO_2/10	SiO_2/10	SiO_2/15
Control gate material/thickness (nm)	X	X	Poly/1000	Aluminum/1000	Aluminum/80	Poly/80
Device performance						
W/E voltage (V)	12/X	12/X	12/-12	12/-12	12/-12	12/-12
Memory window (V)	3.1	2.5	1.27	1.08	2.5	10.1
Transient performance						
Write speed (s)	0.3	0.3	0.17	0.05	1.85	0.05
Erase speed (s)	X	X	0.215	0.180	0.2	2.86×10^{-8}

X was not available.

increasing the control gate voltage to the appropriate numbers. In addition, the material of the tunnel oxide layer is SiO_2 which provides good results. In the future, the materials of Al_2O_3, ZrO_2, or HfO_2 can be taken into account to investigate the operation speeds further. The erase speed comparison between this work and the published papers is presented in the next subsection.

3.4. Performance Comparison. In this subsection, a performance comparison between the nanocrystal floating-gate transistor in this work and the related studies in the 65 nm process is given in Table 5.

Regarding the memory window, it is clear that the value of 10.1 V from this paper is much higher than the values in works [17, 19, 20] with the same input voltage of 12 V. The values of published works are less than 3.1 V. In detail, the memory windows are 3.1 V/2.5 V, 1.27 V/1.08 V, and 2.5 V of works [17, 19, 20], respectively. There are a few reasons why this work has a large memory window. First, good control of the voltage drops through the control gate, which decides the voltage of the floating gate during the write operation, was performed. Second, in the fabrication process, this work proposed to dope the phosphorus into the floating gate and control gate in order to improve electrical conductance. Third, the appropriate quantum dot dimensions were investigated and proposed in this study.

With regard to the writing speed, while the nanocrystal structure of this work can obtain 0.05 s, study [17] has only 0.3 s. In work [19], the structure that uses Poly for the control gate achieves 0.17 s, and the other obtains 0.05 s. Besides, work [20] has a very low value of 1.85 s.

When it comes to erasing speed, the device from this paper can achieve an excellent value of 28.6 ns instead of only 0.215 s/0.180 s in work [19] or 0.2 s in work [20].

4. Conclusion

This paper successfully designs a high-performance nanocrystal floating-gate transistor in terms of memory window, low power, and remarkable erasing speeds. The set of structure parameters like oxide layer thickness, IPD layer, dot dimension, and dot spacing as well as the virtual fabrication processes and methodology for the two-dimensional and three-dimensional structures are proposed for the specific 65 nm process. This work shows that with the thin tunnel oxide thickness of 6 nm, the designed nanocrystal floating-gate transistor achieves excellent results such as the large 2.8 V memory window, the compatible writing speed of 0.05 s with the low control gate voltage of ±6 V, and the drain voltage of only 1 V. In particular, the rapidly erasing speeds obtain the values of 2.03 μs, 28.6 ns, and 1.6 ns when the control gate voltages are ±9 V, ±12 V, and ±15 V, respectively. Regarding the input voltages of ±12 V, the performance of the designed transistor in this work is much better than that in the published works. The good performance of the nanocrystal floating-gate transistor would help enhance the performance, data retention, and flexibility, especially in reducing the fragmentation of the nonvolatile memories, and computing speed of the neuromorphic applications which demand high-speed operations.

Data Availability

The data for this work is stored and maintained in Github with the following link: https://github.com/Steve-Dang459/tcadas/tree/main/Nanocrystal%20floating%20gate%20transistor.

Conflicts of Interest

The authors declare no potential conflict of interests.

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