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Retraction

Retracted: Hardware Realization of Kinematic Mechanism and Control System of Multifunctional Industrial Robot

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This article has been retracted by Hindawi following an investigation undertaken by the publisher [1]. This investigation has uncovered evidence of one or more of the following indicators of systematic manipulation of the publication process:

(1) Discrepancies in scope

(2) Discrepancies in the description of the research reported

(3) Discrepancies between the availability of data and the research described

(4) Inappropriate citations

(5) Incoherent, meaningless and/or irrelevant content included in the article

(6) Peer-review manipulation

The presence of these indicators undermines our confidence in the integrity of the article's content and we cannot, therefore, vouch for its reliability. Please note that this notice is intended solely to alert readers that the content of this article is unreliable. We have not investigated whether authors were aware of or involved in the systematic manipulation of the publication process.

Wiley and Hindawi regrets that the usual quality checks did not identify these issues before publication and have since put additional measures in place to safeguard research integrity.

We wish to credit our own Research Integrity and Research Publishing teams and anonymous and named external researchers and research integrity experts for contributing to this investigation.

The corresponding author, as the representative of all authors, has been given the opportunity to register their agreement or disagreement to this retraction. We have kept a record of any response received.

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[1] K. Zhang, J. Gao, Y. Wang, and M. Liang, "Hardware Realization of Kinematic Mechanism and Control System of Multifunctional Industrial Robot," *Security and Communication Networks*, vol. 2022, Article ID 1940708, 5 pages, 2022.

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Research Article

Hardware Realization of Kinematic Mechanism and Control System of Multifunctional Industrial Robot

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In order to improve the position control accuracy of industrial robots and solve the problems of poor real-time and reconfigurability of traditional motion controllers, a hardware implementation method for the motion mechanism and control system of multi-functional industrial robots is proposed. The video acquisition system is suitable for infrared detectors containing 4 channels or readout circuits in 4 channels. The video display system is compatible with the old AV/S-Video interface, and is also suitable for computer system video graphics array (VGA) analog video interface and high-definition video interface. Multimedia Interface (HDMI) digital high-definition video interface display terminal equipment. The hardware circuit of video acquisition and corresponding video interface image output is designed, including signal amplification circuit, analog-to-digital conversion circuit, video information buffer circuit, video display digital-to-analog conversion circuit, and interface hardware circuit, to realize the digitization of image information acquisition and image information. Display simulation, construct VGA, AV/S-Video, and HDMI timing sequence with hardware description language through Field programmable gate array (FPGA) to complete the display of corresponding terminal equipment. The experimental results show that the experimental data was substituted into the formula and the variance $\sigma = 0.09$ mm was found, indicating that the detection error of the system is less than 0.27 mm, which meets the detection requirements. Through the 3D contour reconstruction experiment of the workpiece, the expected function realization of each module is proved, and the feasibility of the system software and hardware system is verified. This design has good scalability and stability, reducing labor costs.

1. Introduction

With the rapid development of electronic technology, infrared detection technology has been widely used in military and civilian fields [1]. Any object can produce infrared radiation as long as its temperature is above absolute zero (−273°C), like visible light, its radiation can be absorbed, reflected, and refracted. The infrared detector is the core of the infrared system, it uses infrared sensors to convert the detected infrared radiation into electrical signals suitable for transmission and detection, and the infrared imaging display system can be designed using infrared detectors. The infrared imaging display system needs to include modules such as infrared signal readout, signal reception and processing, and video signal display. At present, there are still many video display systems that need to use terminal display equipment with PAL/NTSC standard AV/S-Video interface, computer monitors with a video graphics array (VGA) analog video interface will also be widely used [2]. At the same time, with the rapid development of electronic technology in recent years, especially the popularization of high-speed mobile networks and the Internet, there are higher requirements for the definition and frame rate of image collection, the High-Definition Multimedia Interface (HDMI) that supports higher video specifications has been widely used in computer systems and digital display devices [3]. HDMI is a digital high-definition multimedia interface, the transmission of direct digital signals can reduce the loss caused by multiple analog-to-analog conversions, at the same time, it can make the transmission distance longer, the signal bandwidth larger, and the anti-interference ability better (1).

Huang believes that an important part of production automation, both production efficiency and speed have higher standards for the flexibility of industrial robots. Therefore, higher requirements for trajectory tracking and speed control are put forward, the end effector is required to accurately complete the task, this requires a good control system to control the end effector, let the controlled object better adjust parameters in terms of position and speed [4]. Tian is aimed at the control of AC servo motors, all that needs to be done is to use it as a control object on the basis of a six-degree-of-freedom industrial robot. After the control system receives the work instruction from the host computer, it also refers to the information fed back by the sensor, under the combined action of the two, the control of the movement of the end effector is realized. It can be seen that the structure of the control system has a feedback loop, which constitutes a closed-loop control system [5]. Tippetts believes that industrial robots are generally multidegree-of-freedom, that is, multijoint. In order to realize the motion trajectory of the end effector, all joints need to be mobilized together, and industrial robots need to be able to complete tasks in coordination with peripheral equipment. It can be seen that the structure of industrial robots is more complicated than ordinary systems, its control system is much more complicated than ordinary control system [6]. An infrared imaging display system with AV/S-Video, VGA, HDMI video interfaces is designed. Due to the multivariable and nonlinearity of industrial robots, there is currently no complete system theory, it also brings certain difficulties to the design of the control system and also brings certain obstacles to the production activities. But with the development of industrial robots for decades, nowadays, considerable progress has been made. In order to further improve the control accuracy, a good control system is especially important. It can be seen that the design of the industrial robot control system is of contemporary and developmental significance.

2. System Framework

As shown in Figure 1, the infrared detector outputs the analog video signal through 4 readout circuits, after the signal amplifying circuit enters the analog/digital conversion circuit, the converted digital video data is sent to the FPGA, the SRAM ping-pong buffer algorithm is used to realize the buffering of the video and transmit it to the video drive module of the three interfaces together with the corresponding timing signal constructed by FPGA. VGA display module: the digital video signal is input to the VGA display chip ADV7123, the ADV7123 chip completes the digital-to-analog conversion of the digital video signal, and the analog video data and the line synchronization signal Hsync and frame synchronization signal Vsync generated by FPGA are transmitted to the display through the VGA interface [7]. AV/S-Video display module: the analog video signal (RGB format) converted by the ADV7123 chip together with the line synchronization signal Hsync generated by the FPGA, and the frame synchronization signal Vsync is also input into the PAL/NTSC video format conversion chip AD725. AD725 transmits the video signal through the AV/S-Video interface to the terminal device for display. HDMI display module: FPGA combines the digital video signal with the corresponding line synchronization signal Hsync, the frame synchronization signal Vsync is also input into the HDMI driver chip ADV7511. ADV7511 converts the video signal into a TMDS signal and transmits it to the terminal device for display through the HDMI interface.

The universal control interface board can mainly complete the communication channel, radio frequency front end, frequency synthesizer, radio frequency exchange and other radio frequency module control, frequency insertion, bus interface, module working status report, and other functions. In order to realize the required function, the basic circuit structure block diagram of the interface board is shown in Figure 1. FPGA, as the core of system interface processing, completes the control interface drive function, flexible expansion of RS232, RS422, RS485, LVDS, SPI, I2C, and other buses through FPGA analysis protocol. The chip selects the JXCLX25 programmable logic device of the 58th Institute of China Electricity Branch, and its highest frequency can reach 200 MHz. DSP selects a certain type of 32 bit floating-point digital signal processor from 58 Institute of China Electric Power, complete the initial configuration and module health management functions, working frequency 150 MHz. SRAM is used as a temporary memory for online updates of FPGA and DSP programs, and FLASH is used as a memory for health management related data [8].

3. Hardware Design

3.1. Signal Amplifier Circuit. The 4-channel analog video signal output by the infrared detector readout circuit is first amplified through the follower circuit. This level of amplification does not change the voltage amplitude of the analog video signal, it only increases its driving capability. The signal after the first stage of amplification enters the second stage of differential amplification, complete the adjustment of single-ended signal to differential signal, reduce the interference of common mode noise, at the same time, adjust the amplitude range of the signal to meet the requirements of the analog-to-digital conversion module for the amplitude of the input signal [9].

3.2. Analog-to-Digital Conversion Circuit. The analog-to-digital conversion circuit realizes the conversion of analog signals to digital signals through 4 channels of analog-to-digital converters and input the converted digital video signal to FPGA.

3.3. FPGA Buffer and Transmission Module. The output of the infrared detector is the analog signal of the detected image gray value, after being sampled by the analog-to-digital converter, it is converted into a digital gray value signal in the range of $0 \sim 2x$ (x is the sampling bit width of the analog-to-digital converter), corresponding to the gray value signal to the video signal of the RGB888 system, RGB (0, 0, 0) corresponds to all black and RGB (255, 255, 255)

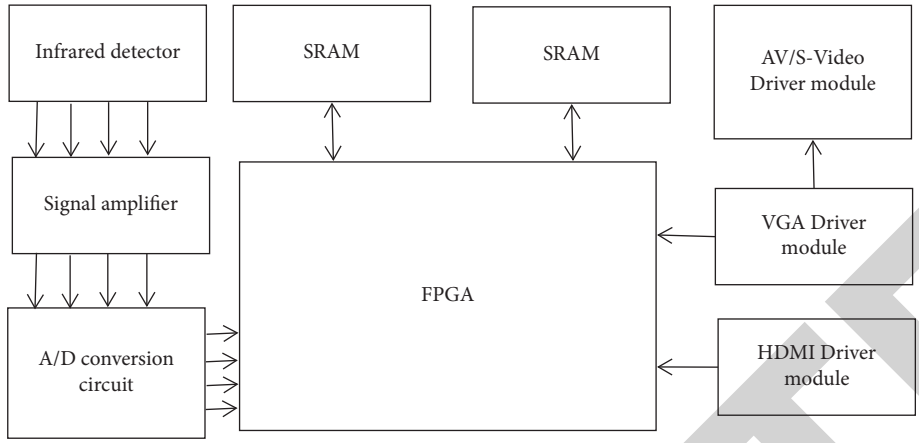

Figure 1: Schematic diagram of system structure and functional modules.

corresponds to all white. FPGA first constructs the input digital video signal line by line, and then sends the digital video signal into SRAM for buffering and transmission to the video drive module.

3.4. VGA Interface Driver Module. ADV7123 chip of Analog Devices, Inc., is adopted, its maximum sampling rate is 330 MHz, low power consumption, 3 channels of 10 digital-to-analog video converters. The video signal adopts the RGB888 system, and the extra-high video signal input pin is grounded. IOR, IOG, and IOB signals are the positive current output terminals of the red (R), green (G), and blue (B) channels, respectively. The COMP signal is used for the compensation of the internal reference operational amplifier and should be connected to the analog power supply terminal with a capacitor of 0.1 μF. Vref is a 1.235 V voltage reference output, usually connected to the power supply terminal with a 0.1 μF capacitor. The Rset pin is used to control the full amplitude of the video signal, usually a sliding rheostat is connected between the Rset pin and the ground, adjusting the resistance value on Rset can adjust the analog video output to obtain the best brightness on the display [10]. In addition, an operational amplifier is added to the output terminals of IOR, IOG, and IOB to improve the driving capability, realize long-distance transmission, and connect a 75 Ω terminating resistor. R0 ~ R7, G0 ~ G7, B0 ~ B7, SYNC, BLANK, CLOCK, and PSAVE are provided directly by FPGA. PSAVE is the energy-saving control pin connected to a logic high level to disable it. The FPGA provides Hsync (line) and Vsync (field) synchronization signals, which are directly connected to the 15-pin VGA display interface connector.

3.5. AV/S-Video Interface Driver Module. The AD725 chip of Analog Devices is used to convert the VGA analog video signal (RGB format) to the PAL/NTSC format and transmit it to the display terminal device through the AV or S-Video interface for display. The VGA interface mainly includes 2 synchronization signals and 3 video signals, that is, the horizontal synchronization (line synchronization) signal Hsync, the vertical synchronization (frame synchronization) signal Vsync, and R (red), G (green), and B (blue) three-color video signal. The Hsync and Vsync logic levels are input to the AD725 to produce integrated synchronization, the R (red), G (green), and B (blue) three-color video signals are correspondingly input to the RIN, GIN, and BIN input pins on the AD725 chip to convert the video format and output. AD725 supports PAL and NTSC video. PAL is the progressive phase inversion quadrature balanced amplitude modulation system, which is the standard adopted by TV, and NTSC is the National Television System Committee standard and the standard adopted by American television. The PAL/NTSC mode selection is determined by the pin STND, and the corresponding input clock pin is 4FSC. When the input STND is high, the chip works in NTSC mode, the corresponding input clock frequency should be 14.318180 MHz. When STND is low, the chip works in PAL mode, and the corresponding input clock frequency should be 17.734475 MHz. Video output provides two interface methods: AV interface, the corresponding signal is the composite video output of pin 10 (CMPS) and S-Video interface, using brightness and chroma to form image control, pin 11 (LUMA) is the brightness output, and pin 9 (CRMA) is the chroma output [11].

3.6. HDMI Interface Driver Module. ADV7513 chip of Analog Devices, Inc., is adopted to drive the terminal equipment display. ADV7513 supports HDMIV1.4 protocol, the maximum sampling frequency is 165 MHz. FPGA inputs the digital video signal (RGB888 format) to the ADV7513 chip D0-D23 pins, at the same time, a horizontal synchronization signal Hsync and a frame synchronization signal Vsync are provided. HDMI can transmit video signals and audio signals at the same time, since this design only contains video signals, the audio-related input pins (SPDIF, I2S, MCLK, LRCLK, SCLK) are grounded. HPD is a hot-swappable pin, used to detect the presence of HDMI devices, if the device exists, the master and slave devices can use DDC (Display Data Channel, corresponding pins SDA, SCL, DDCSDA, DDCSCL, used for the transmission of EDID and HDCP) to obtain the EDID of the other device. CEC

(consumer electronic control) is an extended HDMI function for manufacturers to customize HDMI messages. TX0$^+$/TX0$^-$, TX1$^+$/TX1$^-$, and TX2$^+$/TX2$^-$ are converted by TMDS encoder and include video information, differential signal output pins for audio information and control information, TXC+/TXC- is a differential clock signal output pin, it is also output to the terminal device for display through the HDMI interface.

4. Module Debugging Test and Experimental Results

The experimental equipment used in the debugging experiment is as follows:

(1) FPGA data processing circuit board-block

(2) Computer: main frequency Pentium 2.8 memory 1 GMB, operating system Windows XP

(3) One USB emulator

(4) One linear CCD camera with integrated semiconductor laser

The software used in the debugging experiment are:

(1) Visual *C*++6.0

(2) Quar tusII environment

4.1. Data Transmission Debugging between FPGA and Linear CCD. This task is mainly to verify whether the linear array CCD camera can transmit data with the FPGA data processing board according to the correct timing, ensuring that the data entering the FPGA is correct and free of glitches. The test method uses the test picture that comes with the camera itself. The data corresponding to the test picture has certain regularity, as shown in Figure 2.

The camera is dual-column output in odd and even segments, within every 512 pixels in the test picture, the pixel value of the odd segment increases from 0 to 255, the pixel value of the even segment is decremented from 255 to 0. Before the experiment, the camera should be set through the serial port as follows: sample mode, row rate, output mode, and test picture mode.

The task of this experiment is to check whether the spot center extraction algorithm can correctly extract the spot center, the detection method is to import the pixel data obtained from the embedded logic instrument into MATLAB, the formed light spot data pattern is shown in Figure 3. It can be obtained from the figure that the extremum of the spot center should be at the 2073th pixel, at this time, the value of the spot center position calculated by the embedded logic analyzer is the 1318th pixel in this data period, the starting data for this period is at the 159th pixel, at this time, the setting starting value of the embedded logic analyzer is −512 pixels, therefore, after calculation: 512 + 159 + 1402–2073, the result is consistent with the value in MATLAB, so the correctness of the spot center algorithm is verified.

The task of this experiment is to detect whether the USB serial bus can correctly receive the data transmitted by the

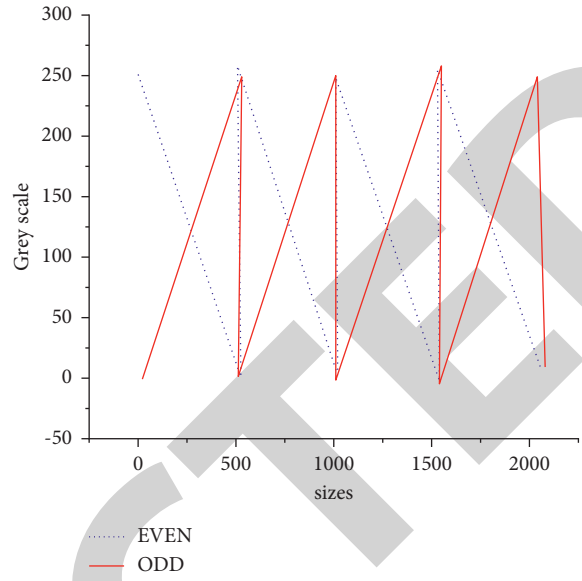

Figure 2: CCD test picture.

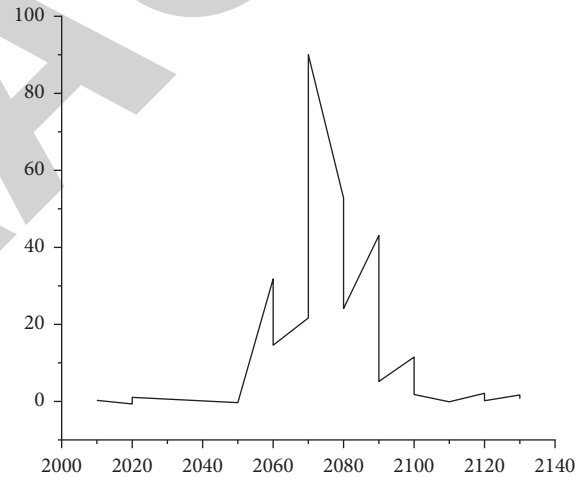

Figure 3: The image formed by pixel data in MATLAB.

FPGA, the detection method is to compare whether the light spot center data obtained by the embedded logic analyzer is consistent with the data received by the USB.

When the USB interface of FT245BM is connected to the host, a driver program provided free of charge by FTDI must be installed on the PC, the driver virtualizes the USB port into a serial port, make the USB port communicate with the PC like a standard serial port, but essentially all data communication for the virtual serial port is completed through the USB bus. In this experiment, set the serial port control MSComm in VC as follows.

This m mscomm. SetCommPort is set to 3, which means that serial port 3 is used.m mscomm. SetSettings is set to 9600,n,8,1 (this rate is the default, in fact the VCP driver always transfers data at the fastest rate).Set the switch status of COM 3 through m_ MSComm. SetPortOpen.Read in or Output data through m mscomm. Input and m mscomm.

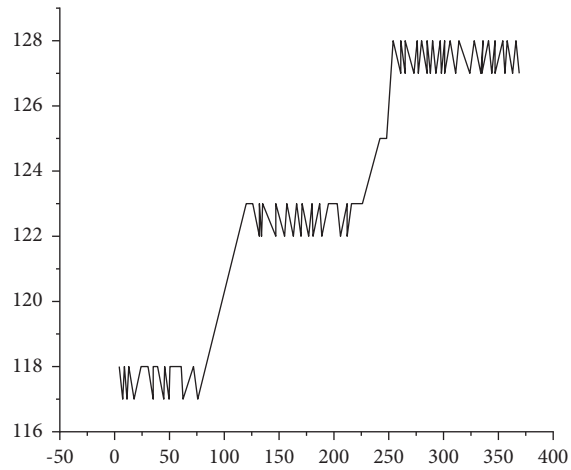

Figure 4: The data shown in MATLAB.

Output.Set m mscomm. SetRThreshold to 1 when reading data.As long as the data is transmitted to the PC, the m_MSComm.CommFvent event will be triggered immediately and the data of COM3 will be automatically read (Figure 4).

Analyze the experimental data, according to the following mean square error formula:

$$\sigma = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(x_i - \overline{x})^2}. \quad (1)$$

Substituting the experimental data into formula (1), the variance $\sigma = 0.09$ mm, it shows that the detection error of the system is less than +0.27 mm, which meets the detection requirements.

5. Conclusion

The linear CCD-based imaging sensor is adopted, which makes the structure of the three-dimensional contour detection system more compact. FPGA has powerful signal processing functions, fast parallel processing capabilities, and reconfigurable features. the use of FPGA-based data processing solutions enhances the flexibility of the system and improves the real-time and reliability of the vision system. The system adopts a modular design with software and hardware, which is convenient for fault maintenance and structural adjustment, at the same time, the USB transmission scheme is adopted to realize the communication with the upper computer, it meets the requirements of image data for transmission rate, makes the system easy to use, and improves the versatility of system hardware.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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