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Research Article

Study on Low-Cost, Low-Voltage Multiprogrammable Nonvolatile Memory Cells for UHF Tag Chips

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This paper proposes a low-voltage, low-cost multiple-time-programmable nonvolatile memory (MTP NVM) based on a standard CMOS 0.13 μm process for UHF RFID chip applications. The design of the differential structure cell using the tunneling effect reduces the read and write voltage. The read and write simulation test results show that the read and write operating voltage is 10 V, which is 30% lower than that of conventional EEPROMs. Because the UHF RFID tag chip requires higher voltage reduction, the structured memory cell is well suited for UHF RFID applications.

1. Introduction

In Ultra High Frequency (UHF) Radio Frequency Identification RFID tag chips, nonvolatile memory (NVM) occupies an important position in the entire UHF RFID tag as the carrier for storing information. Since NVM consumes most energy in a UHF tag chip, the voltage of NVM will have the most direct impact on the overall tag cost. To reduce the cost of the UHF tag chip, the NVM part must be designed for low voltage. Electrically erasable memory (EEPROM) is used as the memory for RFID tags by traditional RFID manufacturers due to its mature technology. In a conventional UHF tag chip, the NVM is the main power consumption module of the tag chip when it performs write operations. Because NVM needs charge pump to generate high voltage to provide voltage signal to the corresponding location of the storage unit when writing, reducing voltage becomes extremely important for NVM of UHF tags. Reducing the read/write voltage and cost of the NVM will be of great importance to the development of UHF RFID tag chips.

In this paper, we propose an MTP NVM cell based on the standard CMOS process to address the high operating voltage of EEPROM. The cell is a differential structure, which reduces the read and writes voltage. It has lower cost and lower voltage than the conventional EEPROM memory cell.

2. System Architecture and Storage Units

The basic composition of the tag chip is shown in Figure 1, which includes the Radio Frequency (RF) analog front-end, digital baseband, and memory three parts [1]; the main role of each part in the entire tag chip is as follows.

The RF analog front-end is the rectification of the modulated RF signal received from the antenna into a DC voltage that powers the entire chip and demodulates the modulated signal, thus enabling backscatter modulation, etc. The function of the digital baseband module is to complete the processing of data. The digital baseband parses the commands transmitted by the analog front-end, responds to the commands according to the corresponding protocol, decodes the baseband signals and stores the information data in the memory. Alternatively, the data are obtained from the memory according to the command and are encoded and then transmitted to the analog front-end. The memory is to complete the storage of data.

The NVM system architecture consists of the components shown in Figure 2. Many storage units are arranged according to certain rules to form a storage array [2], and all data are stored in the storage array. Under the command and coordination of the built-in controller, the row decoder and row driver work together to allow the system to select a row

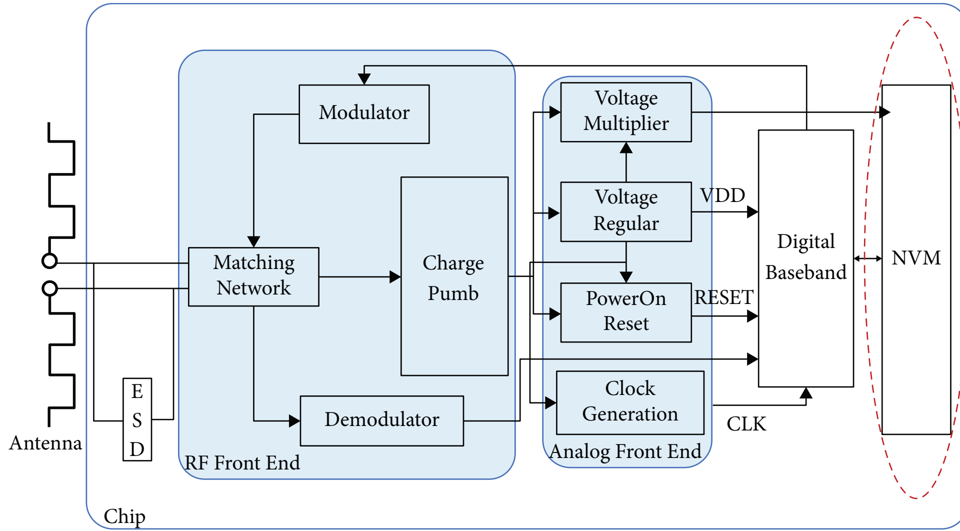

Figure 1: The basic components of a label chip.

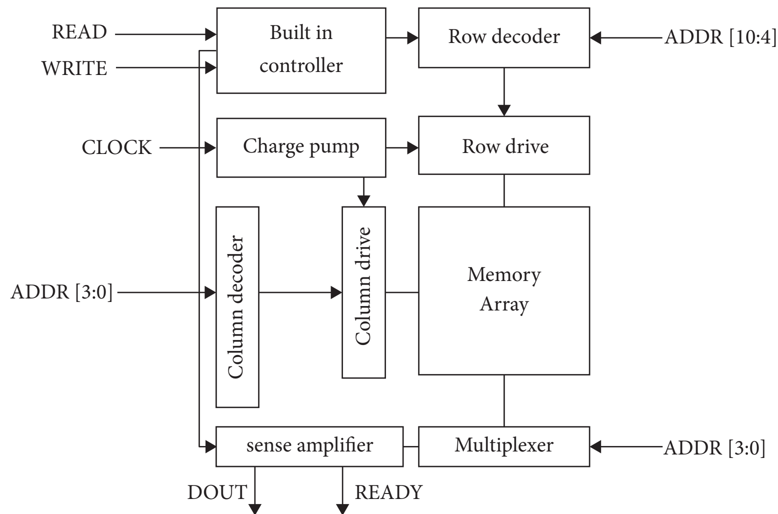

Figure 2: NVM system architecture.

(logically a word) in the array, while the column decoder, column driver, and multiplexer selector work together to select a column (logically a bit) within the selected word. The charge pump generates the high voltage required for programming during write operations. The sense amplifier converts the current analog given by the memory cell to digital logic levels during read operations.

The part of conventional RFID memory generally uses EEPROM memory cell, whose reference structure is shown in Figure 3. The structure has two transistors, M1 tube is used as a selector tube and its gate is connected to voltage VSG. M2 tube is used as a control tube to store data and its gate is connected to voltage VCG. When VCG and VSG are added with high voltage and VS and VD are grounded, a positive electric field is formed between the floating gate and the drain. Due to the F-N tunneling effect, electrons enter the floating gate from the drain side, causing the floating gate to accumulate a negative charge and the threshold voltage to rise. The above process is defined as an “erase” operation, when the data “1” is stored. When VCG is grounded, VSG and VD are connected to high voltage and VS is suspended, a negative electric field is formed between the floating gate and the drain, electrons return from the floating gate to the drain, the floating gate discharges, and the threshold voltage returns to normal. The above process is defined as a “programming” operation, at which time the data “0” is stored.

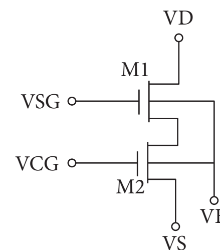

Figure 3: EEPROM memory cell structure.

EEPROM can perform memory read and write operations. Still, because it requires a special process and a multilayer mask, a differential structure MTP memory cell compatible with the standard CMOS process is designed for these deficiencies in this paper concerning the structure in literature [3]. The memory cell is programmed with the high-efficiency tunneling effect-Fowler–Nordheim (the tunneling effect is expanded in detail in Section 3), which enables fast writing and reduces the burden on the high-voltage generation circuit. As shown in Figure 4, M3 is defined as the reading tube, M1C, M1T, M2, M0C, M0T, M3; these six PMOS tubes together form a nonvolatile memory cell of the differential structure. There are two floating gates in this memory cell: M1C and M1T are connected to form the left floating gate FG1, and M0C and M0T are connected to form the right floating gate FG0. These two floating gates store unequal charges, respectively. The two floating gates store unequal charges, which then form different voltages on the two floating gates. When the corresponding bias voltage is added to the memory cell, the output ports RBL1 and RBL0 will generate differential currents I_{RBL1} and I_{RBL0}, which in practice need to be compared by a sense amplifier to distinguish the value stored in the memory cell (logic "0" or logic "1"). This enhances the output, and it is possible to define the output logic "0" for $I_{RBL0} > I_{RBL1}$ and "1" for $I_{RBL1} > I_{RBL0}$. The memory cell stores data mainly by the charge movement (injection or removal of electrons) on the floating gate of the PMOS transistor, i.e., the change of charge.

MTP memory cells require no additional process steps and masks, are compatible with standard CMOS processes, and offer a significant cost advantage over EEPROMs, which require additional processes and multiple masks at a fraction of the cost of standard CMOS processes.

3. Fowler–Nordheim Tunneling Effect

The MTP memory cell achieves the capture and removal of electrons by the attempted penetration effect, according to the principle of capacitive voltage division, as shown in Figures 5 and 6 [4].

It can be simply assumed that V_A is the voltage on the port A connected to the source-drain-substrate of M1 tube; C_1 is the capacitance from the floating gate to the source-drain-substrate of M1 tube; V_T is the voltage on the port T connected to the source-substrate of M2 tube [2]; C_2 is the capacitance from the floating gate to the source-drain-substrate of M2 tube; the charge on the floating gate FG is Q_{FG} [5]; V_{FG} is the voltage on the floating gate FG; Q_0 is the initial charge when the control tube is M1; and Q_0 is the initial charge when the voltage on the floating grid is also at "0" potential when the "0" potential is biased on the control tube M1 and the tunneling tube M2 at the same time. Then the floating grid charge Q_{FG} and the floating grid voltage V_{FG} are

$$Q_{FG} = (V_{FG} - V_A)C_1 + (V_{FG} - V_T)C_2 + Q_0, \tag{1}$$

$$V_{FG} = \frac{C_1}{C_1 + C_2}V_A + \frac{C_2}{C_1 + C_2}V_T + \frac{Q_{FG} + Q_0}{C_1 + C_2}. \tag{2}$$

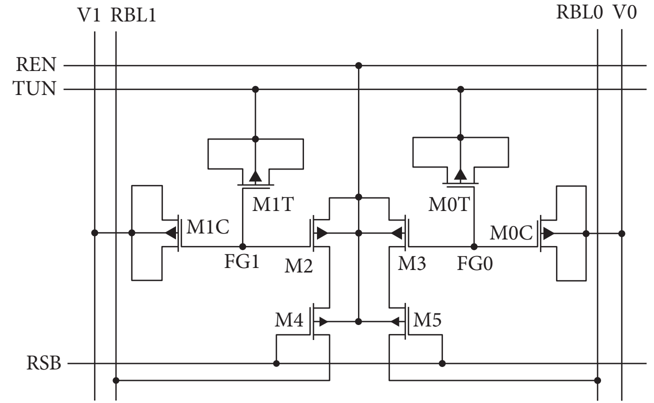

Figure 4: Storage cell structure.

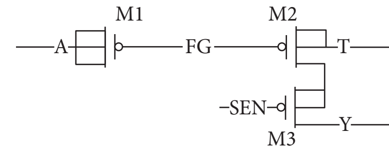

Figure 5: Schematic diagram of the circuit structure.

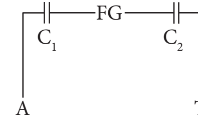

Figure 6: Schematic diagram of a capacitor voltage divider.

Define the coupling coefficient of the control tube as $\alpha_1 = C_1/(C_1 + C_2)$. The coupling coefficient of the tunnel penetration tube is $\alpha_2 = C_2/(C_1 + C_2) = 1 - \alpha_1$. The coupling coefficient of the general control tube can reach 0.9 or more, while the coupling coefficient of the tunneling tube is very low. This can effectively reduce the operating voltage, and equation (2) can also be written as

$$V_{FG} = \alpha_1 V_A + \alpha_2 V_T + \frac{Q_{FG} + Q_0}{C_1 + C_2}. \tag{3}$$

Here, it can be seen that the voltage V_{FG} on the floating gate is mainly influenced by the voltage on the control tube M1 port A [6]. When a high voltage V_A is applied on the control tube M1 port A and a 0 potential is applied on the port T of the tunneling tube M2, the voltage on the floating gate will be close to the high voltage V_A; when the electric field that can be formed on the gate oxide layer of the tunneling tube is as high as 1 e^9 V/m, using the F-N tunneling effect in the channel, the charge across the gate oxide layer reaches the polycrystal in the floating gate. The charge on the floating gate changes, and thus the voltage on the floating gate change to

$$\Delta V_{FG} = \frac{\Delta Q_{FG}}{C_1 + C_2}. \tag{4}$$

If the read voltage VS is applied from the source terminal T of the tunneling tube M2 during the read operation, the read current output from the drain terminal flows out from

the Y port through the selector tube M3 so that the memory cell can be treated as a single MOS tube during the read operation, and the A terminal of the control tube is equivalent to its gate terminal; however, when the voltage on the floating gate changes due to the change of charge, it can be derived from (2), which is equivalent to the voltage change ΔV_A on the "gate" A, i.e,$\Delta V_{FG} = \Delta Q_{FG}/C_1 + C_2$.

$$\Delta V_A = \frac{\Delta Q_{FG}}{C_1}. \quad (5)$$

Then, during the read operation, the memory cell storing data "1" has a threshold voltage with a different state than the memory cell storing data "0" due to the different charge changes on the floating gate.

$$\Delta V_{th} = \frac{\Delta Q_{FG}}{C_1}. \quad (6)$$

The data change of the memory cell is achieved by a programming operation and an erase operation where a high voltage is applied to the control tube of the memory cell during the programming operation [7]. Due to the principle of capacitive voltage division, the voltage on the floating gate is much higher than the voltage on the tunneling tube, which results in a tunneling effect on the gate of the tunneling tube [8]. This allows the floating gate to trap or remove the charge. The state of the floating gate then reflects the change in charge.

4. Floating Grid State Analysis

Because of the existence of the tunneling effect, the charge can be shuttled between the tunneling tube and the floating gate, and the read/write operation of the memory cell is done by the change of the state of the floating gate (that is, the change of the number of charges). Since there is no bias voltage at both ends of the transistor at the moment $T = 0$ (i.e., the initial state), the state of the floating gate is also without voltage change. There is no charge in the floating gate in this state, which is equivalent to two capacitors in series, and its state is shown in Figure 7.

A bias voltage of 10 V is added to the VA and VT terminals from the moment $T = 1$. Changing the amount of floating gate charge is to add the corresponding bias voltage to the transistor [8]. At the time of data writing, i.e., the floating gate captures charge. At the time of data erasure, the floating gate erases the charge. The process is shown in Figures 8 and 9, starting from the initial state ($T = 0$), i.e., $VA = VT = 0$ V, when the floating gate voltage is also 0 V. The subsequent states ($T = 1$, 2, 3) add bias voltages to VA and VT, i.e., $VA = 10$ V, $VT = 0$ V, which causes the gate oxide layer of one of the MOS transistors to form a corresponding electric field to change the total amount of charge on the floating gate. After adding the corresponding bias voltage, the cross capacitive coupling between the two transistors forms a strong electric field in the gate oxide layer of the MT of the attempted transistor, and the charge can pass through the gate oxide layer of the MOS tube by the F-N attempted penetration effect. After capturing the charge from the floating gate ($T = 2$) and continuously adding bias voltage at both ends for some time, the voltage change of the floating gate can make the electric field of the gate oxide layer decrease, thus slowing down the process of attempted penetration. At this point, the bias voltage at both ends of the transistor ($T = 3$) is removed, and the charge of the floating gate has been changed [9].

The relationship between the floating gate voltage and the MC side [9], and the MT side is shown in Figure 10. The simulation result is shown as the solid line in the above figure by setting the voltage at the MC terminal to 0–3.5 V and setting the voltage at the MT terminal to zero. The other process is reversed, setting the voltage at the MT terminal to 0–3.5 V and setting the bias voltage at the MC terminal to zero [3]. The simulation result is shown as the dashed line in the above figure. When the voltage at the MC side of the control terminal changes from 0 to 3.5 V without adding the bias voltage at the MT side, it can be seen that the voltage of the floating gate also increases, and the other process is similar. It can be seen that the MC terminal has a greater effect on the floating gate than the MT terminal does on the floating gate, from which it can be seen that the voltage of the floating gate is mainly controlled by the voltage at the MC terminal [6].

On the other hand, the device modeling and simulation of the memory cell using Synopsys, Sentaurus TCAD (Technology Computer-Aided Design) software in reference [5], are shown in Figure 11 with three different initial charges states after an erase programming operation. All three simulation results can achieve the same erase stable state and stable program state. After each erase operation, the charge on the floating gate changes to $Q_{FG} = 6.931\ e^{-15}$; after the erase operation, the charge on the floating gate is $Q_{FG} = -1.666\ e^{-14}$, thus proving that the charge can be shuttled between the tunneling-pass tube [10] and the floating gate to store and erase information.

5. Simulation Analysis

The MTP memory array is arranged according to the cell structure given above, the memory cells are in symmetric form, and the 16 memory cells are arranged in parallel by bit expansion, with all REN, TUN, and RSB connected, as a basis for word expansion to a 512-bit memory array. In addition, the array of memory consists of a row control circuit, column control circuit, and read circuit. Its structure is shown in Figure 12, and then the read and write function is verified.

5.1. Main Function Timing Diagram. The most important operations of memory are read and write command operations. Before the read and write signals are powered on, the corresponding data lines and address lines are ready and waiting to be undone after the operation is completed. And its same moment can only execute one of the read and write commands.

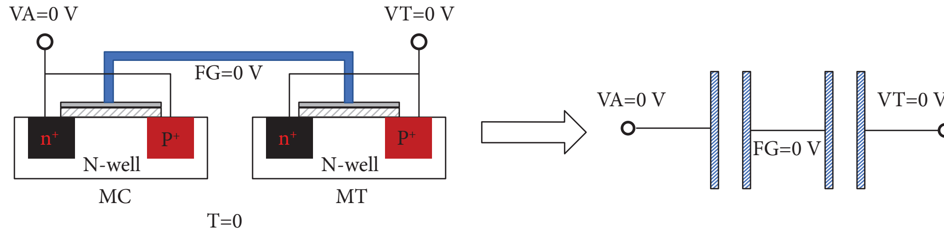

FIGURE 7: Floating gate state without bias voltage.

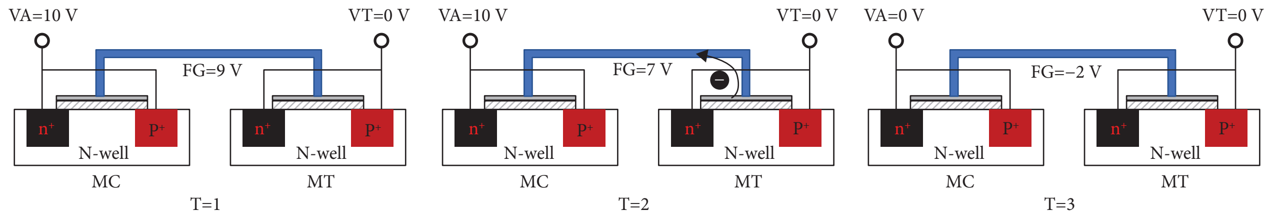

FIGURE 8: Schematic diagram of charge capture by FG.

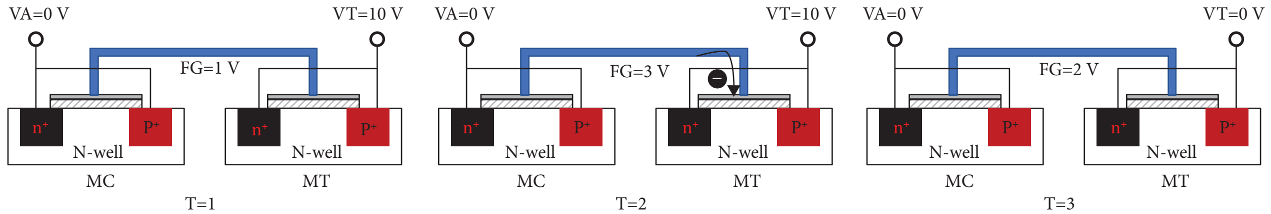

FIGURE 9: Schematic diagram of FG erasure charge.

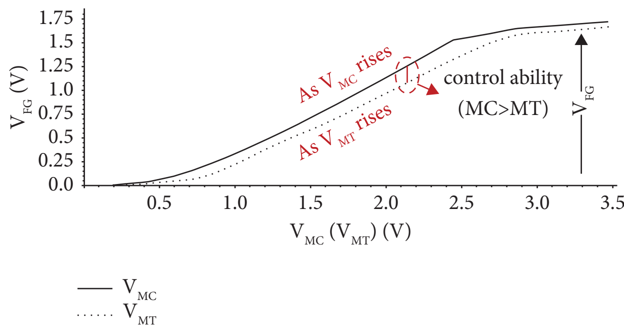

FIGURE 10: Relationship between floating gate voltage and MC and MT bias voltage.

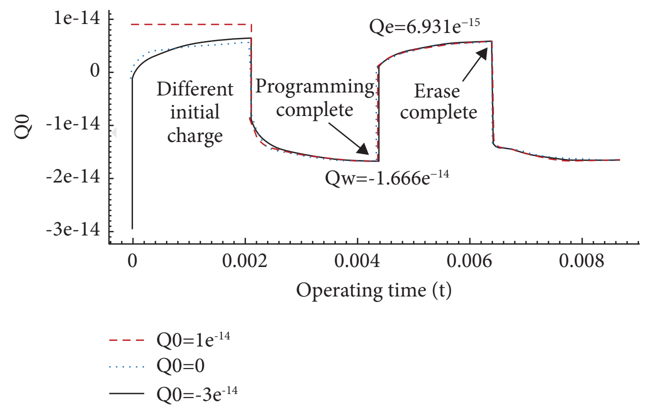

FIGURE 11: Floating gate charge state.

5.1.1. Read Operation Timing. Its state is shown in Figure 13(a). When the memory IP_EN = “1” is idle, it receives the read command READ sent by the digital baseband, and the READY signal becomes “0.” The internal decoding circuit of the memory decodes the long-prepared address data and enables to read the corresponding address data. The READY signal returns to “1” after DOUT reads the result from the idle state.

5.1.2. Write Operation Timing. Its state is shown in Figure 13(b). When the memory IP_EN = “1” is idle, the read command WRITE is received from the digital baseband, and the READY signal becomes “0.” The internal decoding circuit of the memory decodes the long-prepared address data, enables the corresponding address data, and is written to the memory. The READY signal returns to “1” when the write operation continues for some time and is completed.

5.2. Read and Write Command Simulation. The simulation result of the write operation is shown in Figure 14: when the external Write signal is input, the control circuit first sends the Erase signal to perform the erase operation for 2 ms, and when the erase operation is completed, the control circuit continues to send the Program programming signal. The

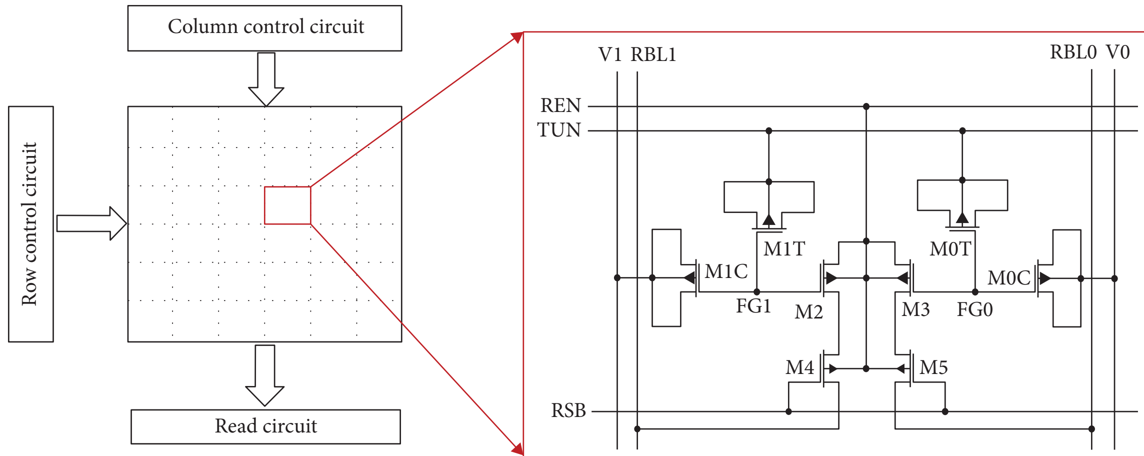

Figure 12: Storage array schematic.

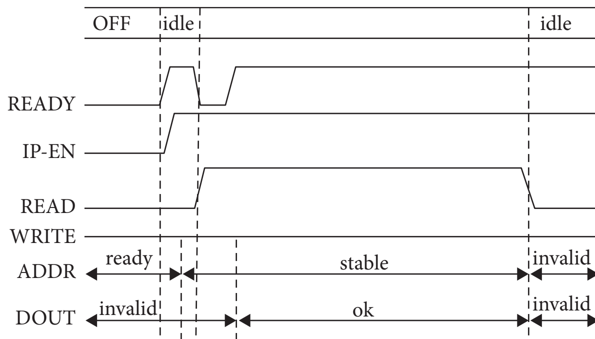

Figure 13: (a) Timing diagram of a read operation. (b) Timing diagram of a write operation.

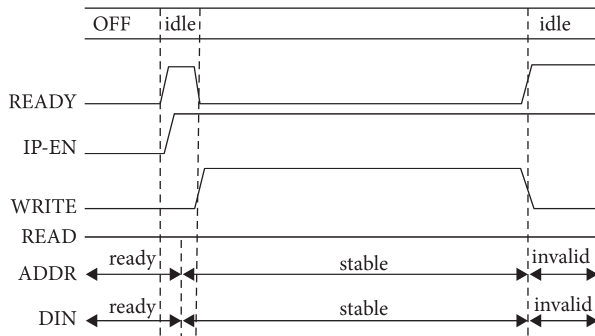

Figure 14: Simulation results of a write command.

charge pump turns on with the Erase or Program start. The output high voltage V_h and V_m have about 0.2 ms jump when the two signals alternate, which is about 2.6 ms in the figure, and the simulation result shows that the charge pump needs 60 us to rise to the required high voltage, and the output result is $V_h = 10.1$ V or so, and $V_m = 4.8$ V. The output of the charge pump turns on with the Erase or Program off, the output high voltage V_h drops from 10.1 V to 500 mV in 100 ns time, and V_h drops from 4.8 V to 31 mV in 100 ns time. Output signal is "1" when V_h reaches 10 V, and below 10 V, the output signal. The Ready signal changes from "1" to "0" after the Write signal comes, and when the write operation is completed, it changes from "0" to "1" when the write operation is completed. The dashed line in the figure shows the drop at 4.6 ms for the execution of the Read command.

The simulation result of the Read command is shown in Figure 15. When the Read command is applied outside the memory, the memory control circuit sends out the Control-Read signal, which lasts for 0.1 ms, and Ready drops to "0" signal at 4.6 ms. Then DOUT rises to "1" signal, and at 4.7 ms Read turns off, the Control-Read signal also follows to turn off; then, DOUT drops to "0" signal at 4.7 ms.

From the above read/write simulation and functional timing diagram, it can be seen that the memory cell designed in this paper can achieve the basic read/write function of the memory, and the high voltage required during the read/write operation is 10 V, which is about 30% lower than the 16 V required for conventional EEPROM.

While the simulation of the read and write commands of the memory is given above to verify the read and write functions of the memory, the voltage distribution of each port inside the memory cell is given below, as shown in Figure 16, which lists the block diagram of the MTP array and the detailed voltage distribution for the write and read operations of the MTP cell in the selected and unselected rows of the MTP array. During the programming operation, a high voltage difference of 10 V is added in the two electrodes of FG1 (FG0) and REN. Electrons will be injected into FG1 (FG0) from the M2 (M3) channel to reduce the FG1 potential until the voltage difference between FG1 (FG0) and REN is less than the tunneling threshold. For unselected MTP cells during erase and program operations, the voltage distribution ensures that the voltage difference across all devices is less than the tunneling channel threshold, thus avoiding a tunneling effect to maintain the original state. For read operations, the MUX block is responsible for the row and column where the selected cell is located. A sensing amplifier based on a positive feedback scheme is used to improve the read sensitivity of the current difference signal on RBL0 and RBL1.

From the voltage distribution of MTP above and the signal diagram of EEPROM ports given in the literature [6], Table 1 compares the voltage of MTP and EEPROM ports, it

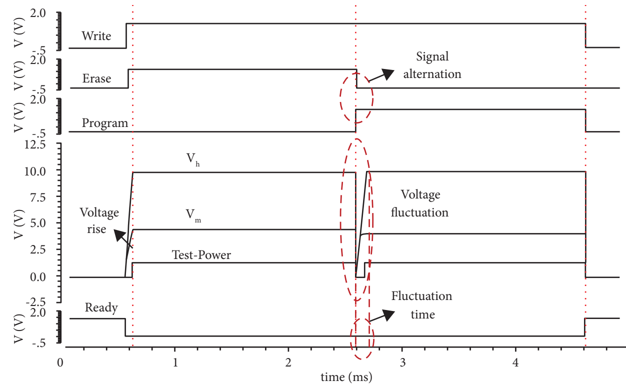

Figure 15: Read command simulation results.

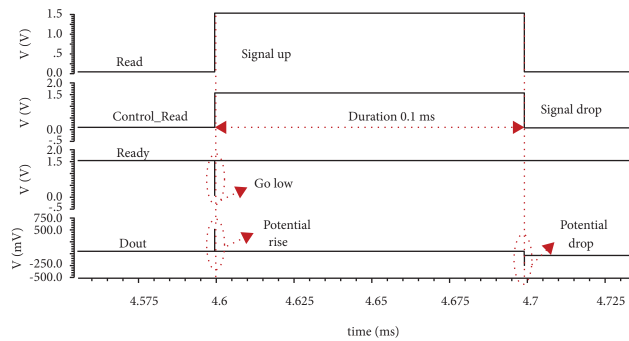

Figure 16: Voltage distribution for write and read operation of MTP.

Table 1: Voltage of each port of MTP and EEPROM.

MTP storage unit offset					
Operation	V0	V1	TUN	REN	RSB
Writing '1'	0	10 V	10 V	0	5 V
Writing '0'	10 V	0	10 V	0	5 V
Writing protection	5 V	5 V	5 V	5 V	5 V
Reading protection	0	0	0	1 V	0
EEPROM storage unit signal offset					
Operation	VSG	VCG	VD	VS	VB
Program	16 V	0	13.5 V	Floating	0
Erase	16 V	15 V	0	0	0
Read	1.8 V	1.8 V	1.5 V	0	0

can be seen that, for the write operation, MTP requires 10 V (V1 = TUN = 10 V) and EEPROM requires 16 V (VSG = 16 V) for programming. The dashed lines in the table show that the voltage required for the MTP is much lower than the EEPROM voltage of 16 V or more, so the low voltage characteristic of the MTP makes it ideal for UHF RFID applications.

6. Conclusions

UHF electronic tag chip as a key component in the Internet of Things has been widely used worldwide and is the focus of current research. One of the cores of UHF electronic tag chip is memory; traditional RFID manufacturers use EEPROM as the memory of RFID tags, but in the UHF tag chip needs to

reduce the voltage and cost, EEPROM has a high cost (need special coprocess support and multilayer mask) and high voltage deficiencies, and for these deficiencies this paper uses standard CMOS process to design the MTP. On the other hand, the high voltage required for the read/write process is about 10 V, which is 30% lower than that of conventional EEPROM.

Data Availability

All data included in this study are available upon request to the corresponding author.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

Authors' Contributions

YHX and CL designed the method and wrote the paper; NB and YW performed the experiments and analyzed the data; all authors have read and agreed to the published version of the manuscript.

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References

[1] N. Bai, L. Wang, Y. Xu, and Y. Wang, "Design of a digital baseband processor for UHF tags," *Electronics*, vol. 10, no. 17, p. 2060, 2021.

[2] K. Ming, X. Zhang, S. Ren, and J. Sun, "Spatial Pyramid Pooling in Deep Convolutional Networks for Visual Recognition," *IEEE Transactions on Pattern Analysis & Machine Intelligence*, no. 9, pp. 1904–1916, 2015.

[3] S. Li, L. Cai, Y. Xiao et al., "A 20 dBm passive UHF RFID tag IC with MTP NVM in 0.13-μm standard CMOS process. Circuits and systems I: regular papers," *IEEE Transactions on*, vol. 99, pp. 1–14, 2020.

[4] M. Takahashi, S. Wang, T. Horiuchi, Q. Li, K. Y. Yun, and S. Sakai, "Novel Ferroelectric CMOS Circuits as a Nonvolatile Logic," *American Physical Society*, vol. 44, no. 7, pp. 467-468, 2008.

[5] B. Wang, L. Man-Kay, J. Yi, T. Chi-ying, and A Bermak, "A -12.3 dBm UHF passive RFID sense tag for grid thermal monitoring," *A IEEE Transactions on Industrial Electronics*, vol. 66, no. 11, pp. 8811–8820, 2019.

[6] Li De, *An Optimized 512bit EEPROM Design for RFID Tag Chips. Diss*, Tianjin University, Tianjin, China, 2012.

[7] L. Ma, K. Hu, Y. Zhu, and H. Chen, "Cooperative artificial bee colony algorithm for multi-objective RFID network planning," *Journal of Network and Computer Applications*, vol. 42, pp. 143–162, 2014.

[8] X. Wang, J. Zhang, Z. Yu, S. Mao, S. C. G. Periaswamy, and J. Patton, "On remote temperature sensing using commercial UHF RFID tags," *IEEE Internet of Things Journal*, vol. 6, pp. 10715–10727, 2019.

[9] J. Shen, X. Wang, B. Wang et al., "Fully Integrated Passive UHF RFID Transponder IC with a Sensitivity of −12 dBm," in *Proceedings of the IEEE International Symposium on Circuits & Systems IEEE*, Beijing, China, May 2013.

[10] Z. Jin, *Research on Key Technologies in the Design of Passive UHF Radio Frequency Identification Tags*, Xi Dian University, Xi'an, China, 2011.