Hindawi
Scientific Programming
Volume 2022, Article ID 7838252, 10 pages
https://doi.org/10.1155/2022/7838252

Research Article

A Reference Source Circuit Design for Voltage Controlled Oscillator Chips

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Received 15 July 2022; Revised 29 July 2022; Accepted 1 August 2022; Published 29 August 2022

Academic Editor: Punit Gupta

The basic principle and typical structure of the bandgap voltage reference source are introduced in detail in this paper. The performance index of the bandgap voltage reference is analyzed. The core circuit of a bandgap voltage reference source with good temperature characteristics and a high power supply rejection ratio (PSRR) is designed, in which a two-stage differential operational amplifier with a buffer stage is used, a start-up circuit without a capacitor is used to reduce the start-up time, and a common beta multiplication self-bias circuit is used to attenuate the effects of the power supply voltage. It is shown from the final HSPICE simulation results that the reference voltage temperature coefficient is approximately 7 ppm/°C within the range of -20 to 80°C in temperature, and the average PSRR can reach more than −56 dB within the range of 1 Hz to 10 kHz in frequency.

1. Introduction

A voltage-controlled oscillator or VCO is a circuit element that adjusts its oscillation frequency in response to an input voltage. The simplest and most common control input is a DC potential derived from a special musical keyboard which acts rather like a complicated switched potentiometer, with each key closing a switch on a continuous resistive element. The design of such a circuit is not altogether straightforward because the oscillator must be made to swing over the entire audible range, a frequency range of some 11 octaves.

It is known that a chip of voltage-controlled oscillator is an indispensable part of an electronic product. Because of the rapid development of portable miniaturized portable electronic products, such as mobile phones and laptops, higher requirements for the layout area and the stability of the output frequency are put forward to the chip of the voltage-controlled oscillator, in which the voltage reference source plays an important role. It provides an accurate and stable bias current and voltage reference for other functional blocks in the chip [1, 2]. Temperature independence and voltage stability are important indicators of voltage reference sources, which affect the stability and performance index of the chip of oscillator output frequency directly [3, 4]. Therefore, it is of great practical significance to design a voltage reference source that has lower temperature drift and a higher PSRR. A voltage-controlled oscillator or VCO is a circuit element that adjusts its oscillation frequency in response to an input voltage. The simplest and most common control input is a DC potential derived from a special musical keyboard which acts rather like a complicated switched potentiometer, with each key closing a switch on a continuous resistive element. The design of such a circuit is not altogether straightforward because the oscillator must be made to swing over the entire audible range.

A large number of researches on bandgap voltage reference have been carried out at home and abroad. The research content is mainly concentrated on the following two methods: The first one is to reduce the temperature drift [5, 6]. Usually, the temperature drift of the first-order compensated voltage reference source is 20–60 ppm/°C. Therefore, higher-order curvature compensation must be

performed in order to reduce the temperature drift. The most commonly used method is second-order curvature compensation, i.e., increasing the proportional to absolute temperature (PTAT) term, including the second-order curve compensation technology, exponential curve compensation technology, and VBE linearized technology [7, 8], which are all based on the temperature coefficient compensation method of the resistance ratio. The disadvantage is that there are many difficulties in the implementation of the specific circuit, and when the circuit makes the reference output be a certain value at a certain temperature, the temperature drift of the operational amplifier will have an important impact on the temperature coefficient of the voltage reference source [9, 10].

The second one is to improve the PSRR [11, 12]. During the operation of a voltage controlled oscillator, a large number of high-frequency noises are produced by the switching and breaking of the switch tube. This will have a negative impact on the voltage reference source, so it is required to improve the PSRR in a wide frequency range [13, 14]. There are two main methods to improve the PSRR asfollows: The first one is to let the core circuit of the bandgap voltage reference source be isolated from the power supply voltage source by using the common source grid device; The second one is to let the closed-loop feedback be established between the power supply voltage source, and the voltage reference source so that the power fluctuation can be fed to the reference circuit to improve the power rejection ratio by the feedback loop [13]. The above two methods can both improve the PSRR at low frequencies, but when the working frequency increases, the PSRR will be reduced greatly [15, 16].

In the design, a full differential structure is used to improve the PSRR (50 dB above). A large-sized tube is used to design the amplifier to reduce the proportion of the offset voltage in the reference source. The self-bias current source circuit is used to obtain the best structure and parameters of the circuit and device.

2. The Basic Principle of the Bandgap Voltage Reference Source

The typical bandgap voltage reference source circuit is shown in Figure 1. When the temperature drift is −2.2 mV/°C at room temperature, the two triode $Q1$ and $Q2$ emitters produce a voltage V_{BE}, and at the same time produce a thermal voltage $V_{\mathrm{T}}(V_{\mathrm{T}} = \mathrm{kT/q})$, which is a PTAT term. At the same time, the temperature drift at room temperature is also +0.085 mV/°C [17].

It can be obtained from the "virtual break" of the operational amplifier as follows:

$$V_{\mathrm{out}} = V_{BE2} + I\left(R_2 + R_3\right) = V_{BE2} + \frac{V_Y - V_Z}{R_3}\left(R_2 + R_3\right). \tag{1}$$

If the open loop gain of the operational amplifier is large enough, it can be obtained as follows:

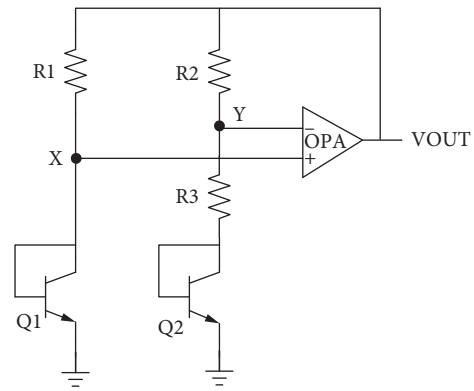

Figure 1: The structure of a typical bandgap voltage reference source circuit.

$$V_X = V_Y \Rightarrow V_{\mathrm{out}} = V_{BE2} + \frac{V_Y - V_Z}{R_3}\left(R_2 + R_3\right)$$

$$= V_{BE2} + \frac{\Delta V_{BE}}{R_3}\left(R_2 + R_3\right),$$

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln n, \tag{2}$$

$$\frac{\partial \Delta\, V_{BE}}{\partial T} = \frac{V_T}{T}\ln n,$$

$$V_{\mathrm{out}} = V_{BE2} + \frac{V_T \ln n}{R_3}\left(R_2 + R_3\right),$$

$$\frac{\partial V_{\mathrm{out}}}{\partial T} = \frac{\partial \Delta\, V_{BE2}}{\partial T} + \frac{V_T}{T}\frac{R_2 + R_3}{R_3}\ln n. \tag{3}$$

A proper selection of the value of R_2, R_3, and n can make the value of formula (3) be to 0. At this moment, it can be assumed that the output voltage is independent of temperature.

3. Design of a Functional Circuit

3.1. Core Circuit. The core circuit of the bandgap voltage reference source is shown in Figure 2. V_{REF} is realized by the voltage drop produced by the sum of two currents on the resistor R_4: one current is proportional to the voltage V_{BE} of the transistor, and the other is proportional to V_{T}. The two currents are mirrored to the output current through the MOS tube M3, and then the output voltage as a reference is determined by the output load resistor R_4 (in the range of ensuring the normal operation of the MOS transistor) so that the required value of the output voltage can be changed easily.

If the three PMOS tubes M1, M2, and M3 have the same ratio of width to length, then the following conclusions can be drawn:

$$I_1 = I_2 = I_3 = I,$$

$$I = I_2 = \frac{V_Y}{R_2} + \frac{V_Y - V_Z}{R_3}. \tag{4}$$

Because of the effect of the amplifier, it will be obtained as follows:

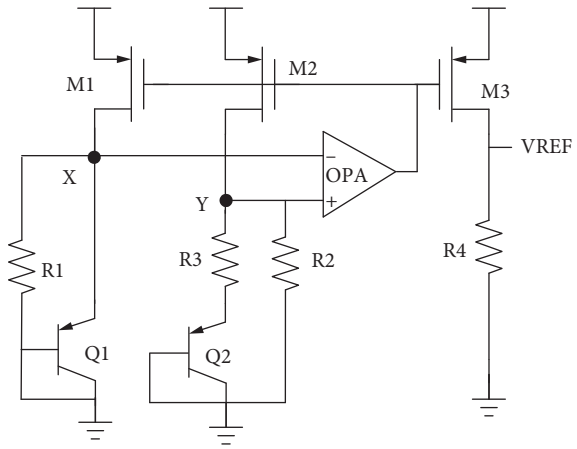

Figure 2: The core circuit of the bandgap voltage reference source.

$$V_X = V_Y \Rightarrow I = \frac{V_X}{R_2} + \frac{V_Y - V_Z}{R_3}. \tag{5}$$

If $R1 = R2$, the current flow over $Q1$ and $Q2$ is equal, so the following conclusions are obtained:

$$V_X - V_Z = \Delta V_{BE} = V_T \ln n, \tag{6}$$

$$I = \frac{V_{BE}}{R_2} + \frac{V_T \ln n}{R_3} \Rightarrow V_{\text{ref}} = IR_4 = \left(\frac{V_{BE1}}{R_2} + \frac{V_T \ln n}{R_3}\right) R_4 = \frac{R_4}{R_2}\left(V_{BE1} + \frac{R_2}{R_3} V_T \ln n\right). \tag{7}$$

According to the formula (7), the resistance value of R_2 and R_4 can be adjusted to obtain the reference voltage of different values by the resistance partial pressure method according to different needs.

The whole bandgap core circuit is scanned to the temperature. The results are shown in Figure 3.

As it can be seen from the diagram, the maximum value of the output voltage is 1.2393 V, and the minimum value is 1.2379 V. The absolute value of reference output voltage variation shall not exceed 1.4 mV in the temperature range of −40 to 125°C. The relative temperature drift is maintained at a relatively wide range of temperatures. The value is about 8.4 ppm/°C.

In the range of 2.5 V to 5.5 V, DC, voltage characteristics of the core circuit, and the simulation results are shown in Figure 4.

From Figure 4, it can be seen that starting from 2.9 V, the reference voltage is stable at about 1.22 V (when the power voltage increases, the output voltage of the reference source increases at the same time because the devices are temperature sensitive. Without an additional circuit, the output voltage has a certain dependence on the power supply voltage, which is close to the design specification of 1.22 V and also satisfies the actual voltage range of the power supply.

3.2. Start-Up Circuit. When the power supply is powered on, if there is no start-up circuit, the input terminal of the operational amplifier will be at a low potential, and the core circuit will be in a zero-current state. At the same time, the transistor cannot be turned on; the whole circuit will come into an unknown state. Therefore, a start-up circuit is necessary to be added to complete the starting of the entire circuit.

In the actual design, considering the integrity of functions of the entire chip circuit in different modes, the start-up and bias circuit are designed as shown in Figure 5:

The start-up circuit is composed of NMOS tubes I13, I27, and I17, and PMOS tube I16. The operation process is that when the electric circuit is abnormal, the voltage of the A point may be high, and the B point voltage is low so that the current of the offset circuit is zero, and the circuit cannot work normally. At this time, the B channel potential is increased by the path of the power supply through the NMOS tube I13, so that the NMOS tube I29 and I30 are turned on, the A point potential is pulled down, and the bias circuit works normally. Then, the leakage current of the NMOS tube I29 is adjusted proportionably by the resistor I6, so as to provide a suitable and stable bias current for the subsequent circuit. After normal operation, the voltages of A and B in the bias circuit are very stable. It is not affected by the start circuit. The NMOS tube I13 cuts off, the connection between the start circuit and the bias circuit is broken, and the starting process is completed.

3.3. Bias Circuit. The bias circuit is used to provide a stable bias current for the operational amplifier in the reference source circuit. In order to make the generated bias current less sensitive to the power supply voltage, some voltages that are not highly related to the power supply voltage can be used to generate the bias current. These voltages, which are not related to the voltage of the power supply, are often used in transistors, such as the reverse breakdown voltage of Zener diodes. At the same time, these voltages can further reduce the susceptibility of the current source to the power supply voltage. The self-bias structure further improves the current source based on the sum. The β multiplication self-bias circuit is designed according to the requirements as shown in Figure 5.

In order to facilitate adjustment, the width-to-length ratios of the NMOS tubes I14 and I15 are made the same, and the width to length ratios of the PMOS tubes I24 and I26 are also made the same so as to ensure the matching of the two sides of the circuit and the equalization of their threshold voltages. Take the NMOS tube I29 with a channel width four times that of the NMOS tube I30 ($K = 4$). Therefore, it will be obtained as follows:

$$\beta_{29} = K \bullet \beta_{30}, \tag{8}$$

$$V_{GS10} = V_{GS11} + IR. \tag{9}$$

If the current I is used to represent the NMOS tubes I29 and I30 and ignore the effect of the body effect on the I30 tube, then it will be obtained as follows:

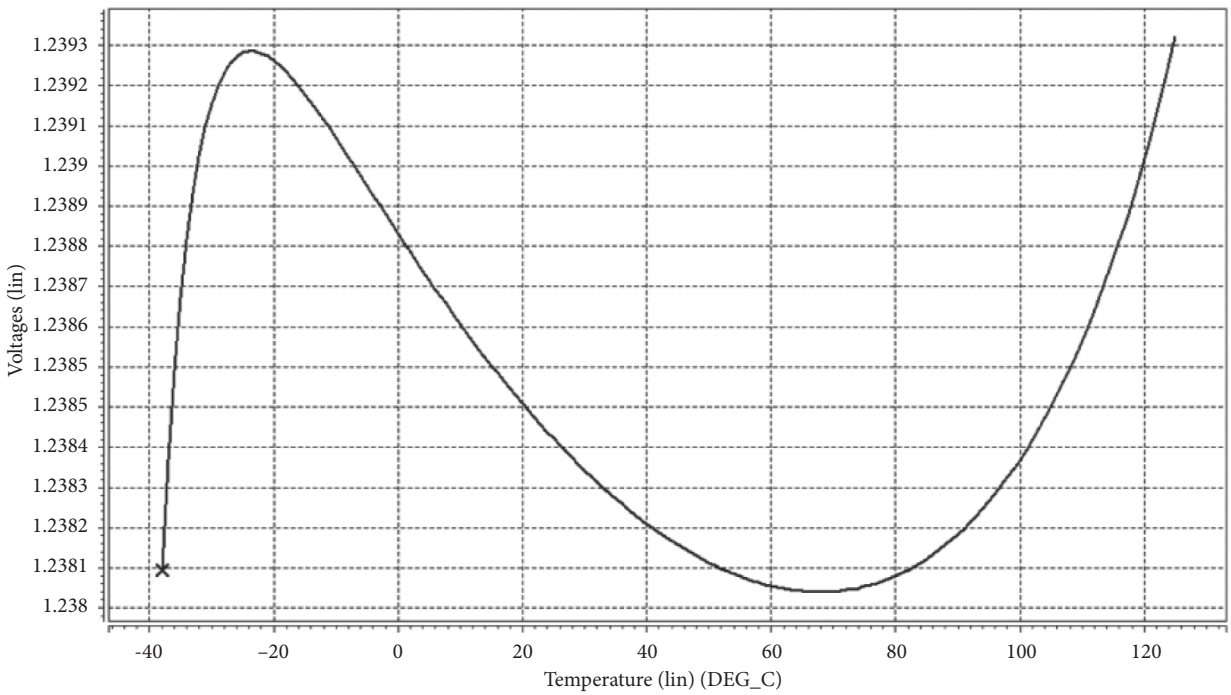

Figure 3: The core circuit temperature characteristics of the output voltage.

$$V_{GS29} = \sqrt{\frac{2I}{\beta_{29}}} + V_{THN}, \tag{10}$$

$$V_{GS30} = \sqrt{\frac{2I}{K \bullet \beta_{29}}} + V_{THN}. \tag{11}$$

From the above formulas (8)–(12), I can be calculated as follows:

$$I = \frac{2}{R^2 \beta_{29}} \bullet \left(1 - \sqrt{\frac{1}{K}}\right)^2. \tag{12}$$

The current I is exactly the bias current provided for the operational amplifier in the voltage reference source.

3.4. Operational Amplifier Circuit. The open loop gain of the operational amplifier needs to be increased so that the input offset voltage can be reduced and the PSRR can be increased. Therefore, a two-stage operational amplifier is used to solve this problem in this design. The first stage uses a common dual-end input and single-end output differential structure to provide high gain. The second stage uses a common-source MOSFET amplifier to simplify the circuit and provide a large swing. The simulation indexes of the operational amplifier are the gain margin, phase margin, and the PSRR.

The detailed design of the operational amplifier is shown in Figure 6.

The tubes M1 and M2 are of the same size to form the source end coupling pair. The tubes M5 and M6 constitute a current mirror to provide a bias current for the coupling pair.

The structure of the CMOS differential amplifier and the current source load used together is shown in Figure 6. When the gates of tubes M1 and M2 are grounded, the current flowing through the M1–M4 tubes is $I_{ss}/2$ each. The drain end voltage of tube M4 is equal to the gate voltage of tubes M3 and M4 and the drain end voltage of tube M3. Therefore, the leakage voltage difference between tubes M1 and M2 is zero. The same result of the leakage of the M4 tube and the gate voltage of tube M3 is used to offset the next level at a specific current level. Moving the common cascade technology to the second level of the two-level operational amplifiers can make the compensation simple and remove the level displacement circuit.

As a frequency compensation capacitor, Cc and its parallel resistor R form the main pole to reduce the bandwidth of the amplifier to guarantee the stability of the two-stage amplifier.

To ensure the stability of the operational amplifier, the phase shift should be less than 180° when the gain is reduced to 0 dB, and the general margin should be greater than 60°, that is, the phase shift should be less than 120°. This usually means that a small dampening oscillation of the step effect of the feedback system can provide rapid stability. For a larger phase margin, the system is more stable, but the time response is slowed down. Therefore, a phase margin of 60° is usually considered the most suitable value.

In order to ensure the stability of the operational amplifier, it should be ensured that when the phase shift reaches 180°, the gain is less than 0 dB, and generally, there is a 10 dB margin. In other words, when the phase shift reaches 180°, the gain is less than -10 dB.

The simulation results of phase margin and gain margin are shown in Figures 7 and 8.

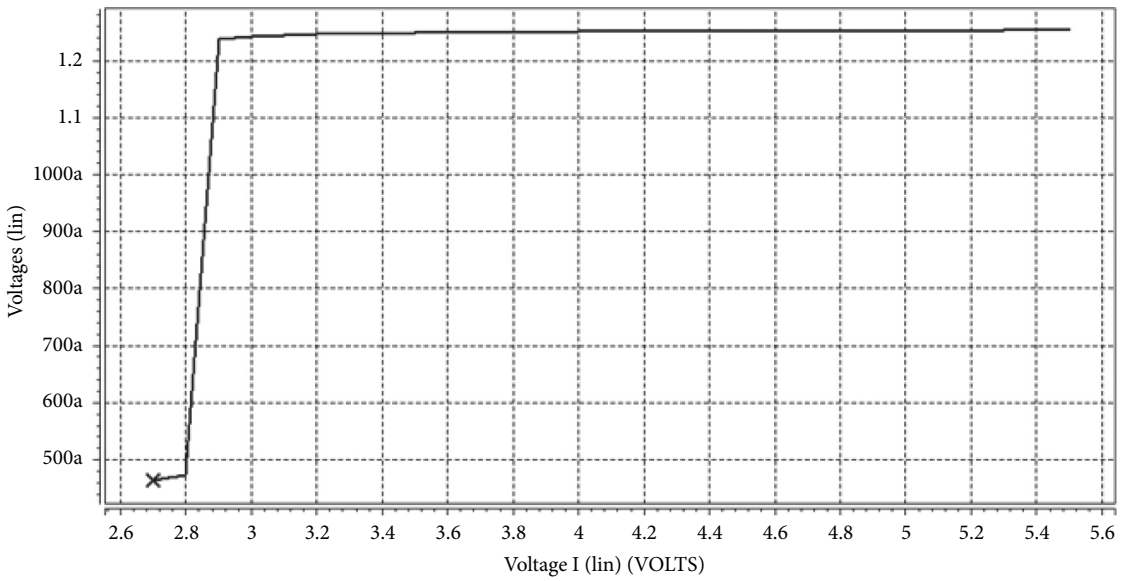

Figure 4: Voltage characteristics of the core circuit.

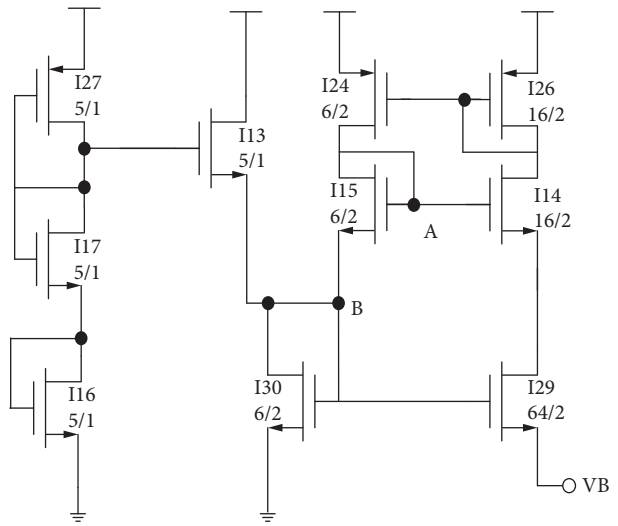

Figure 5: Start-up and a bias circuit.

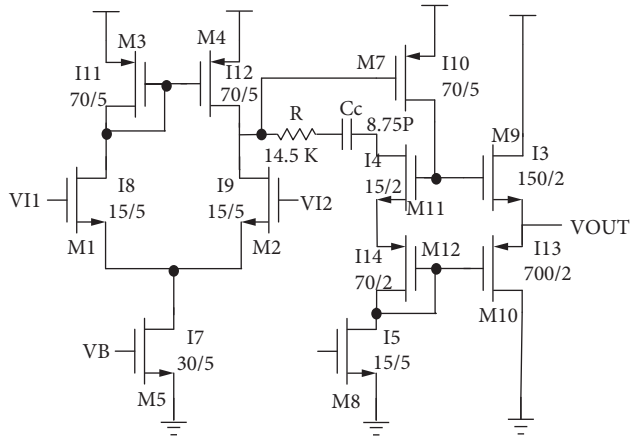

Figure 6: Two-stage operational amplifier with output buffer.

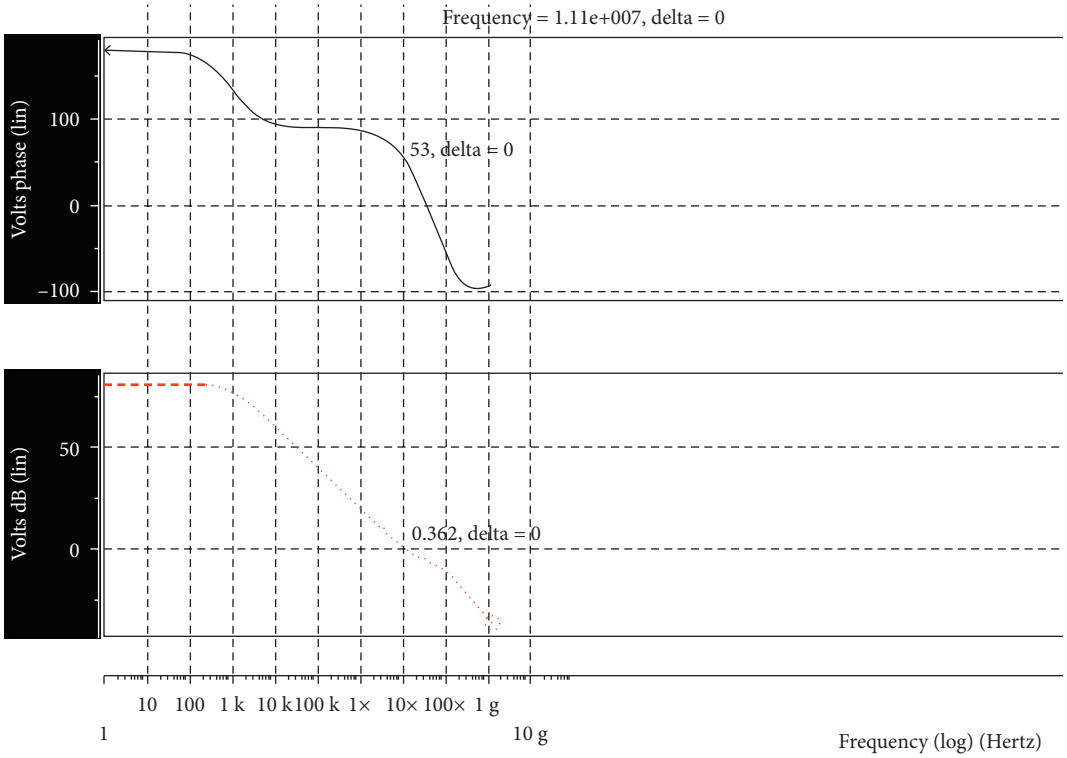

Figure 7: Phase margin simulation of the two-stage operational amplifier.

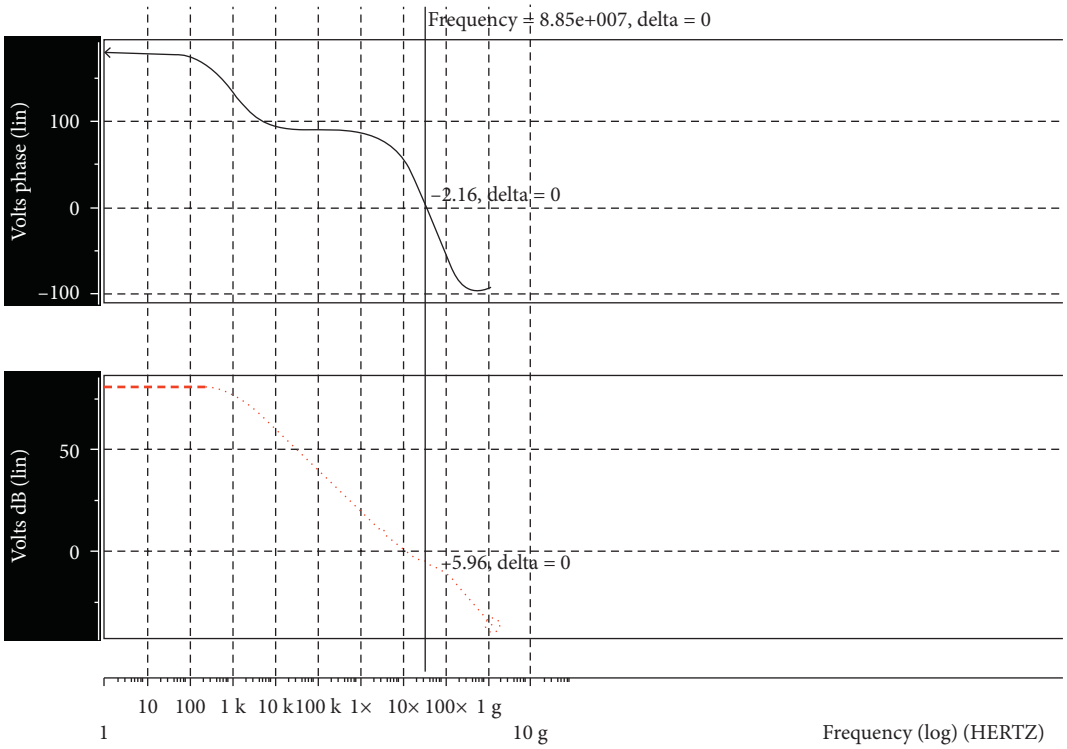

Figure 8: Gain margin simulation of the two-stage operational amplifier.

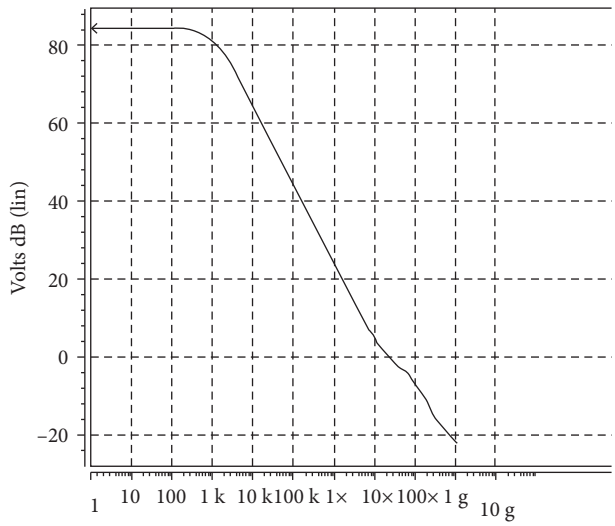

Figure 9: Open-loop gain simulation of the operational amplifier.

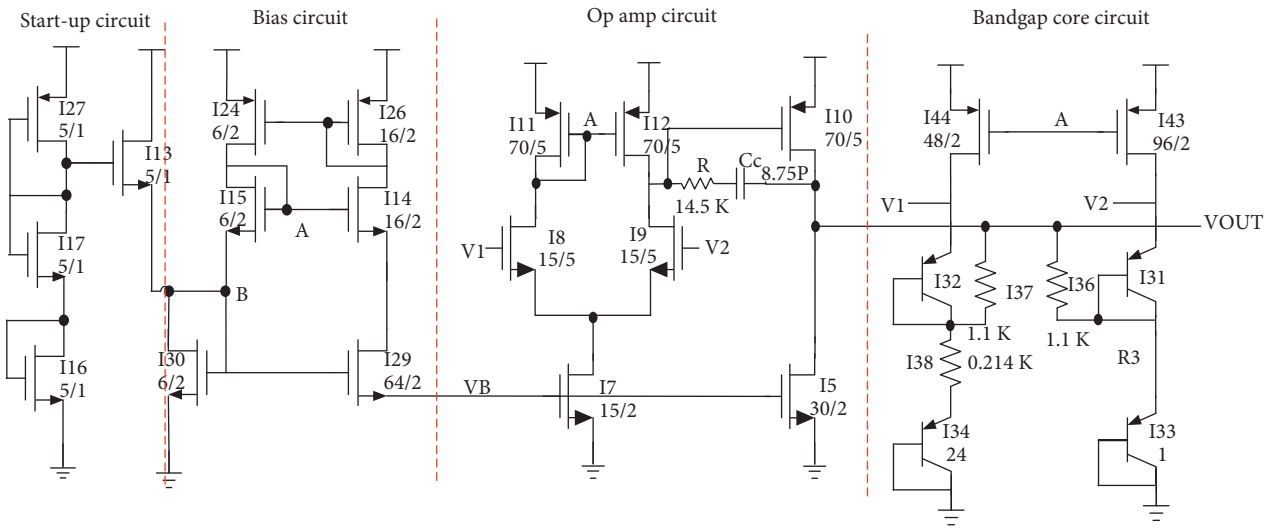

Figure 10: Integrated bandgap voltage reference source circuit.

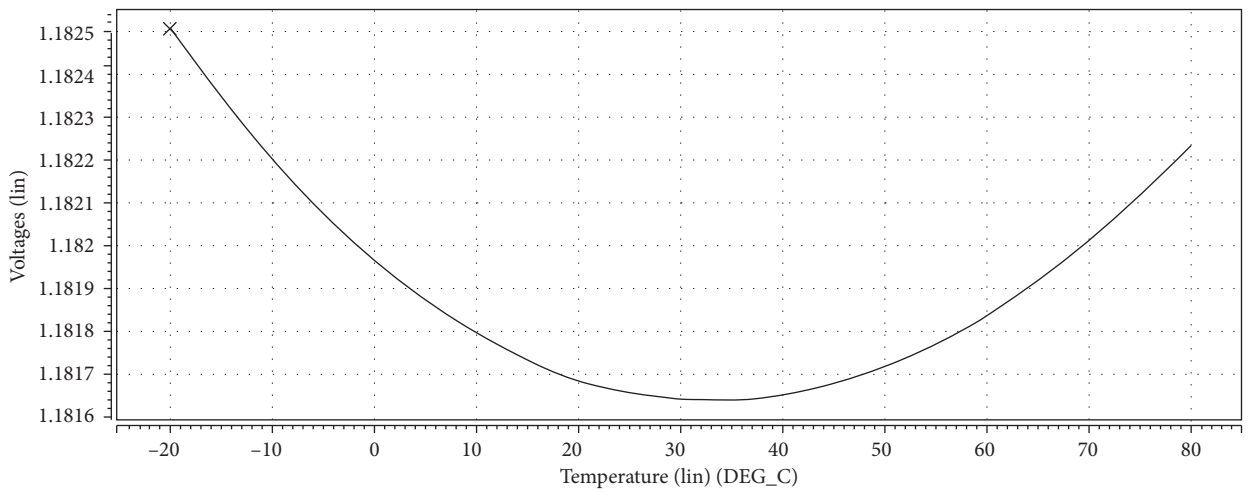

Figure 11: Temperature characteristic curve of bandgap voltage reference source circuit.

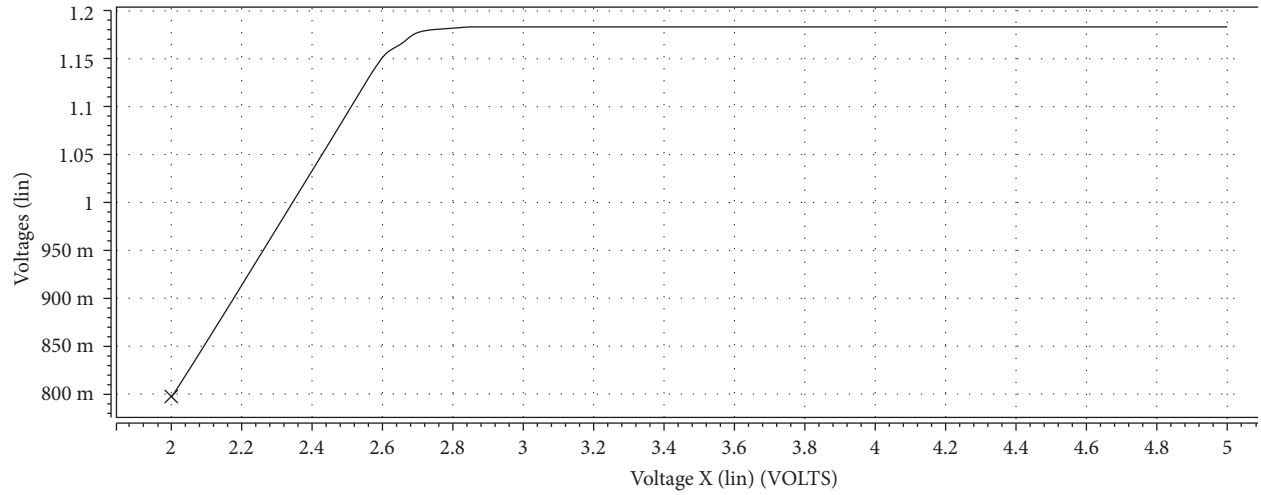

Figure 12: Output voltage characteristic curve of bandgap voltage reference source circuit.

It can be seen from Figure 7 that the phase margin of the designed operational amplifier is 53° (greater than 45°), which can make the operation stable.

It can be seen in Figure 8 that when the phase shift reaches 180°, the gain is -5.9 dB, which meets the design requirements.

The simulation result of open-loop gain is shown in Figure 9. It can be seen from the diagram that, under the typical conditions, in the range of operating frequencies 0 Hz to 10 kHz, the open-loop gain of the operational amplifier is above 50 dB, which ensures the stable operation of the operational amplifier and meets the design index.

4. Simulation of an Integrated Bandgap Voltage Reference Source Circuit

The entire circuit of the bandgap voltage reference source is composed of the core circuit, start-up circuit, bias circuit, and the two-stage operational amplifier as shown in Figure 10.

In the range of −20°C to 80°C on temperature, the entire circuit is scanned to the temperature. The curve of temperature characteristics is shown in Figure 11.

As can be seen in Figure 11, the maximum reference output voltage is 1.1825 V, and the minimum one is 1.18185 V. The absolute value of the reference output voltage change does not exceed 0.85 mV. The circuit maintains high-temperature stability over a relatively wide range of temperature variations. The relative temperature drift is approximately 7 ppm/°C.

When the circuit is carried on the voltage analysis, the curve that the output voltage changes with the power supply voltage is shown in Figure 12 ,which can be seen the stability of the power supply voltage. The voltage-canning range is from 2 V to 5 V, and the operating temperature is set to the typical value of 25°C.

As can be seen clearly in Figure 12, starting from 2.7 V, the output voltage is stable at 1.18 V, which is almost constant and is close to the design specification of 1.2 V (when designing a 1.2 V reference output voltage, it is assumed that the operational amplifier is an ideal amplifier of which the gain is infinite). However, the gain of the operational amplifier cannot be infinite in practical application. The reference output voltage is less than the ideal value considering the effect of gain). The circuit maintains high voltage stability in a wide variation range of supply voltage, which also satisfies the actual voltage range of the power supply.

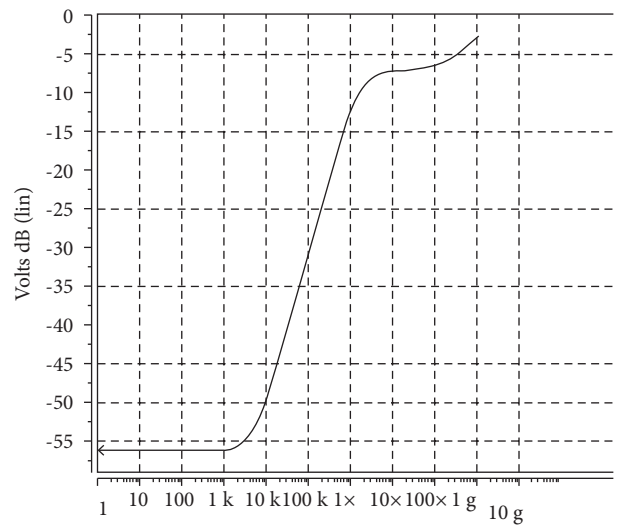

Figure 13: PSRR curve of the bandgap voltage reference source circuit.

The simulation result of the PSRR is shown in Figure 13. The ability of the circuit to suppress power noise can be seen in the curve. It shows that the value of PSRR can be less than −50 dB under typical conditions within the range of frequencies 0 Hz–10 kHz and can reach −55 dB at low frequencies, which meets the design index.

5. Layout Design

The layout of the bandgap voltage reference is most important in the whole design because it has a crucial influence on the overall chip performance. The layout of the whole circuit is shown in Figure 14.

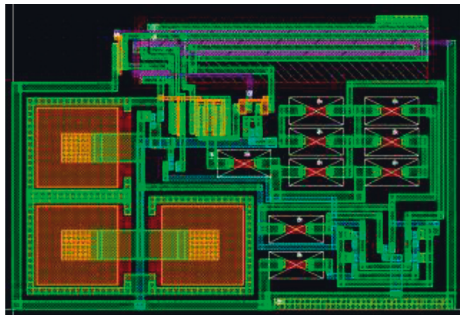

Figure 14: Layout of the bandgap voltage reference source circuit.

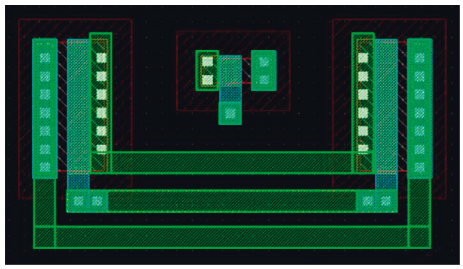

Figure 15: Layout of NPN tubes with different sizes.

In Figure 14, the Miller compensation capacitor of 3 pF is used. The gate of the output part of the layout connects to a larger MOS capacitor to stabilize the output, and the capacitor is placed on the edge of the BG module. The oscillator module is placed on the BG module. At the same time, the bandgap reference module is surrounded by a power supply layer and a ground layer, and the output driver module is placed at the far end of the BG module.

The two NPN tubes of two different sizes (6 : 1) in the bandgap datum realize the difference between the two emitters and the base voltage, so the matching of the two tubes is very important. In the design, the big tube is decomposed into two tubes so as to surround the small tube in the middle, as shown in Figure 15, so that the NPN tube can be less affected by the outside interference source when the electrons are collected and emitted.

6. Conclusions and Discussion

The voltage reference source designed in this paper mainly includes four parts: a core circuit, a start-up circuit, a bias circuit, and an operational amplifier. During the selection of the core circuit structure, considering the advantages of high precision, low noise, low-temperature drift, and the general application in the industry, the bandgap voltage reference source is taken into account. Therefore, the final selection is based on the Brokaw bandgap reference circuit. Then a capacitor-free starting circuit is designed so as to reduce start-up time. During the selection of bias circuits, a common self-bias circuit, which is independent of the supply voltage and multiplied by β, is adopted to ensure the constant bias current. In the design of an operational amplifier, the PNP bipolar transistor is selected to provide the two differential amplifiers for the input and MOSPET transistors in order to increase the gain and reduce the noise. At the same time, the buffer level is added to reduce the output impedance, and increase the amplitude of the output signal.

Finally, the circuit has been simulated by HSPICE of which the temperature drift is about 8.4 ppm/°C in the range of −40 to 125°C on temperature, and the value of PSRR can reach −56 dB in the range of 1 Hz to 10 kHz on frequency. The design not only meets the requirements but also has the advantages of simple structure and high stability compared to the same type of voltage reference source circuit, and especially has good performance in temperature drift, power supply voltage adjustment, and so on. It has good practical value.

Data Availability

The datasets used and analyzed during the current study are available from the corresponding author on reasonable request.

Conflicts of Interest

The authors declared that there are no conflicts of interest.

Acknowledgments

This research was funded by the Natural Science Foundation of Hunan Province (2020JJ7052).

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