VLSI Design

Selected Papers from the International Mixed Signals Testing and GHz/Gbps Test Workshop

Guest Editors: Bozena Kaminska, Marcelo Lubaszewski, and José Machado da Silva

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Editorial

Selected Papers from the International Mixed Signals Testing and GHz/Gbps Test Workshop

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This special issue of the VLSI Design journal is dedicated to the 13th IEEE International Mixed Signals Testing Workshop (IMSTW) and 3rd IEEE International GHz/Gbps Test Workshop (GTW), held in June 2007 at Póvoa de Varzim, Portugal.

For the first time these two workshops were joined together in a single event dedicated to all aspects of testing, design for testability and reliable design of integrated mixed signals/technologies, functions, and systems. These include testing, design verification, and design for manufacturability of monolithic mixed signals/technologies systems-on-chip, circuits running in the multi-GHz clock range and/or including I/O capable of multi-Gbps data rates, and heterogeneous systems including system-in-package and printed circuit board implementations. The technology spectrum included analogue, mixed signals, high-speed input/output, radio-frequency (RF), micro-electro-optical-mechanical systems (MEOMSs), and nanotechnology.

This special issue comprises the most outstanding contributions selected from the best papers presented at this joint event, after having undergone an additional reviewing process, and constitutes a display of advanced research focusing on challenges and solutions associated with domains in the forefront of complex chip design. The selected nine papers address the test and characterization of A/D converters (ADC), fault modeling, simulation, and diagnosis of analog circuits, builtin calibration and diagnosis of RF transmitters, and test of MEOMS devices.

The paper from Vincent Kerzérho et al. presents a technique which allows the dynamic testing of ADC for harmonic distortion using waveform generators with the same resolution as the ADC under test. Another issue with ADC testing concerns the complexity of data processing. A new algorithm for estimating ADCs' nonlinearity is proposed by E. J. Peralías et al., which is based on the spectral processing of the ADC output to estimate its harmonic amplitudes and phase-shifts from which the INL signature is derived, as an alternative to resorting to the time-consuming code histogram test.

Every millisecond cut in testing time can save millions of dollars in a production run. That can be achieved after finding the proper set of tests. With the "Choice of a High-Level Fault Model for the Optimization of Validation Test Set Reused for Manufacturing Test," as presented by Y. Joannon et al., the number and efficiency of test stimuli can be optimized. Fault modeling and simulation is also crucial for diagnosis purposes. Augusto and Almeida present "A Tool for Single-Fault Diagnosis in Linear Analog Circuits with Tolerance Using the T-vector Approach" which accounts for tolerances in components' values.

High frequencies in the gigahertz range together with the use of diverse digital modulation methods such as binary phase-shift keying (BPSK) and quadrature (QPSK) phase-shift keying, code division multiple access (CDMA), and orthogonal frequency division multiplexing (OFDM), complicate the testing of RF transceivers. V. Natarajan et al. show how built-in testing features can be used to help diagnosing and calibrating functional parameters.

A method for diagnosing capacitive MEMS accelerometers is proposed by L. A. Rocha et al. which allows

estimating overetching, mismatch, and Young's modulus parameters relying on the measurement of pull-in voltages and resonance frequency.

The advances in MEMS technology allow the development of devices for RF applications, namely as switches. RF MEMS-based switches are characterized (compared namely with FET's and PIN diodes) by presenting low insertion loss, power consumption, fabrication cost, and intermodulation, further with high isolation (tens of GHz). The paper presented by E. Simeu et al. describes a new method to test RF MEMS which allows extracting the high-frequency characteristics of the switch from the envelope of its response to a low-frequency actuation test stimulus.

MEMS switches are also good candidates to be used as builtin test circuitry. The loopback testing of multigigahertz devices can be enhanced by using MEMs switches, taking advantage of their higher bandwidth and smaller size compared to traditional relays, and SiGe logic to configure a variety of active loopback structures, as it is shown by D. C. Keezer et al.

MEMS devices have been also developed for biochemical and microfluidics applications, namely on droplet-based peptide synthesizers for initial diagnosis of cancer or virus. H. G. Kerkhof et al. address the reliability of these diagnoses with a technique to detect droplet presence or purity problems via current or impedance measurements using electrodes near the peptide collector area.

On behalf of the journal, we would like to conclude this Editorial to thank our former Chief Editor, Dr. Bernard Courtois for his support in the publication of this Special Issue. We would also like to take this opportunity to thank the help and advice of various reviewers. They read the manuscript submissions, provided invaluable feedback to the authors, and shared their professional wisdom and insight.

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Research Article

ADC Production Test Technique Using Low-Resolution Arbitrary Waveform Generator

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Recommended by José Machado da Silva

Standard production test techniques for ADC require an ATE with an arbitrary waveform generator (AWG) with a resolution at least 2 bits higher than the ADC under test resolution. This requirement is a real issue for the new high-performance ADCs. This paper proposes a test solution that relaxes this constraint. The technique allows the test of ADC harmonic distortions using only low-cost ATE. The method involves two steps. The first step, called the learning phase, consists in extracting the harmonic contributions from the AWG. These characteristics are then used during the second step, called the production test, to discriminate the harmonic distortions induced by the ADC under test from the ones created by the generator. Hardware experimentations are presented to validate the proposed approach.

1. INTRODUCTION

Analog-to-digital converters (ADCs) are nowadays part of complex systems developed for diverse domains such as medical applications, telecommunications, and consumer applications. The increasing performances of such systems induce the need of developing high-speed and high-resolution ADCs. In addition to developing high-resolution ADCs, a relevant challenge is to have test instrument performances higher than ADC under test performances.

Indeed, the common way to test ADCs in production is the DSP-based method [1]. In order to achieve such a test, there is a need of an arbitrary waveform generator (AWG), and a capture memory, combined with a processing unit in the tester. The accuracy of such a test depends on the instrument performances. The most critical instrument is the AWG. As a rule of thumb, the signal delivered by the generator must be 10 dB better than the specification limits of the ADC, to ensure acceptable test conditions. Consequently, it is commonly admitted that the generator resolution should be at least 2-bit higher than the tested ADC resolution.

In this context, it is clear that there is a great interest in developing new test solutions that relax the constraints on the test instrument performances.

Digital-to-analog converters (DACs) are the main components of AWGs. In [2–5], solutions for the compensation of DACs nonlinearity are proposed. These solutions are based on hardware modifications. Unfortunately, in our context, the DACs are already embedded in test instruments. In [6], a digital processing technique is proposed to compensate for DAC nonlinearity without any hardware modification. This technique could be suitable for the compensation of AWGs, but the technique needs high-performance instruments to implement the calibration routine. As a consequence, if there is a need of a high-performance instrument for calibration, the interest in using a low-performance AWG is reduced.

Some publications address another approach [7–9]. This approach consists in relaxing constraints on AWG performances by discriminating the sources of errors in the test path or by virtually improving the performances of the test instrument.

Two techniques deal directly with low-performance stimuli for converter testing. The first technique; the SEIR [7], is a histogram-based technique dedicated to the test of ADC linearity using low-linearity stimuli. The second one is the 2-ADC method [8] that permits to estimate noise parameters from ADCs under test. Both methods overcome the performance issue of the stimuli by discriminating the

errors of the DUT from the errors of the setup. However, these methods are dedicated to the measurement of linearity or noise of an ADC under test. None of them address the measurement of harmonics in order to compute some dynamic parameters.

Finally, another method, the wobbling technique, is proposed in [9] that reduces the effect of rounding from the converter in order to accurately estimate its dynamic parameters. In particular, the wobbling-based technique improves the repeatability of the harmonic distortion measurements. Although this method proved to be efficient, the level of the harmonics of the AWG still needs to be lower than those of the ADC under test to avoid any fault masking. Consequently, this solution does not solve the problem for most of the current ADCs.

A conventional solution to reduce the AWG nonlinearities is to use a filter centred on the test frequency. However, this solution is quite expensive as a new filter is required for each test frequency, involving a complex test board with costly calibration phase.

In this context, the objective of this paper is to propose a method to test ADC harmonic distortions using only a low-cost ATE. This method relies on an initial learning phase, in which the AWG characteristics are estimated. These AWG characteristics are subsequently used to discriminate the harmonic distortions induced by the ADC under test from the ones induced by the AWG.

The paper is organized as follows. The first section presents the usual ADC test parameters and the instrumental constraints in order to achieve a correct test. The theoretical developments of the proposed method and its application for low-cost mass production test are described in Section 3. Several experimental validations are presented in Section 4. Finally, Section 5 gives some concluding remarks.

2. ADC TEST

2.1. Conventional ADC test

Real-life ADCs are affected by errors, usually classified in two types [1, 10, 11]:

(a) stochastic errors: noise, aperture uncertainty (jitter), and coupling between analog and digital part;
(b) deterministic errors: nonlinearities, distortion.

Several parameters are defined in order to characterize and test ADCs [12, 13]. The traditional dynamic parameters are total harmonic distortion (THD), spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SINAD). The critical static parameter is the integral nonlinearity (INL). The above set of parameters can be derived [11, 14, 15] or computed [1] from the harmonic values and/or the noise value. A very common way to evaluate these harmonic and noise values of a given converter relies on spectral analysis, that is, to apply a single-tone sine wave to the converter input and compute the FFT on the output signal.

DSP-based method is usually used in order to measure these parameters. The typical DSP-based test architecture is described in Figure 1. The analog stimulus is usually generated by an AWG, and the output signal is captured and stored in a logic analyzer.

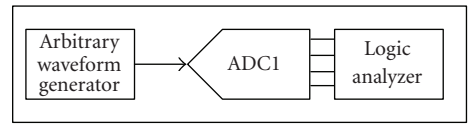

Figure 1: DSP-based test architecture.

Table 1: Common H2 amplitude versus converter resolution.

Converter resolution	Common H2 (dB)
12	−88
10	−73
8	−55

In order to achieve a correct evaluation of the ADC parameters, there are some constraints concerning the instrument performances and in particular for the AWG. Indeed, an ideal test signal is a pure sine wave, but a real-life signal applied to the converter input is obviously deteriorated by the noise and the harmonics induced by the AWG. Clearly, the noise and the harmonic levels of the test signal should be low enough to be negligible in front of the noise and harmonics induced by the converter under test. The condition for an accurate evaluation of the ADC parameters is therefore the use of an AWG with better performances than the ADC under test. Sections 3 and 4 detail this condition regarding the noise and the harmonic distortions induced by the AWG.

2.2. Harmonic distortions induced by the AWG

We only focus on harmonic estimation. Indeed, the method developed in [16] can be used to estimate noise features in a similar test configuration to the one proposed in this paper. This method uses one generator to supply the same test signal simultaneously for two ADCs under test. These two ADCs share the same sampling clock. Using the properties of correlated noise sources disturbing both ADCs, by simple postprocessing calculations, it is possible to discriminate the noise provided by each ADC under test from the one induced by external sources.

To illustrate the influence of the AWG on harmonics measurements, we only consider the second-order harmonic, H2, but similar behavior could be obtained with other harmonics. Table 1 gives an idea of H2 amplitude that could be induced by converters according to practical experiments and datasheets.

As previously explained, AWG consists of a DAC with harmonic distortions. Consequently, if we consider a sine wave generated by an AWG and converted by an ADC, the digital signal at the output of the ADC is deteriorated by both components. In the worst case, the H2 amplitude induced by both sources can be summed. Table 2 gives the true H2 amplitude of the tested ADC, and the measured H2 amplitude considering the influence of the AWG.

Table 2: H2 measurement, ADC versus DAC/ADC setup.

Test configuration	True H2 (dB)	Measured H2 (dB)
8-bit ADC tested using 8-bit DAC	−55.0	−49.0
8-bit ADC tested using 10-bit DAC	−55.0	−54.0
8-bit ADC tested using 12-bit DAC	−55.0	−54.8

It can be seen that the correct estimation of the ADC harmonics requires the use of an AWG with a resolution at least 2 bits higher than the resolution of the ADC under test.

3. METHODOLOGY

Section 2 has demonstrated that there are strong constraints on the test instrument performances to be able to perform conventional ADC test applying the DSP-based method.

This section presents a test method for mass-production testing of ADC harmonic distortions using low-cost testers. A low-cost tester may be defined as a tester embedding low-end AWGs that would not be efficient enough to apply a conventional DSP-based test. As a rule of thumb, the price of a time slot for a tester that embeds some high-performance analog instruments is commonly twice the price of a time slot for a tester composed of digital channels and low-performance analog instruments. The theoretical fundamentals are given in the first part. Section 4 describes the first step of the method that consists in estimating the AWG-harmonic contribution. Section 5 is dedicated to the production test stage in which ADCs are tested using a postprocessing correction of the AWG errors.

3.1. Theoretical fundamentals

Let us consider a sine wave applied to an ADC. Using a Fourier series expansion, the output signal can be expressed by (1). In this equation, we distinguish the quantized sine-wave $x(n)$ that would be obtained if the ADC was ideal and the sum of all the harmonic values introduced by static and dynamic nonlinearity of the converter [11]

$$s(n) = x(n) + \sum_{k\geq 0} H\mathrm{conv}_k^{\mathrm{Amp}} \cos(k(\theta_n + \theta_0) + \theta_k), \qquad (1)$$

where n is the sample index, θ_0 the initial phase shift, θ_k the phase shift induced by dynamic nonlinearity, $H\mathrm{conv}_k^{\mathrm{Amp}}$ the amplitude of the kth harmonic H, induced by the converter, named conv, and θ_n is the nominal sampling phase given by

$$\theta_n = 2\pi\left(\frac{P}{M}\right)n, \qquad (2)$$

where P is the number of cycles (i.e., signal periods) and M the number of samples in the test record.

In Section 4, we will restrict our study to static nonlinearity contributions, which are dominant in most of ADC architectures, especially for those using a sample-and-hold in the input circuitry. The effects of the other contributions, mainly due to parasitic elements, will be evaluated in further studies.

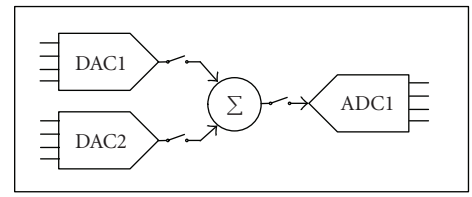

Figure 2: Hardware setup for test development.

Equation (3) is the simplification of (1) considering only static nonlinearities

$$s(n) = x(n) + \sum_{k\geq 0} H\mathrm{conv}_k^{\mathrm{Amp}} \cos(k(\theta_n + \theta_0)). \qquad (3)$$

Equation (3) may also apply to a DAC and can thus be used to express the signal generated by an AWG.

3.2. Learning AWG harmonic contribution for postprocessing

According to [16] and considering a system of two DACs and one ADC connected by a set of switches and a combiner as illustrated in Figure 2, it is possible to discriminate the harmonic contribution of the three converters. The idea is to exploit different configurations and test conditions in order to separate the harmonic contribution of each converter.

Let us consider a test configuration in which the output of DAC1 is directly connected to the ADC1 input. The spectrum of the output signal can be computed and we can extract the values of the harmonics H_k. Obviously, the output signal is impacted by errors of both converters. In other words, the measured spectrum includes the harmonic contribution of DAC1 as well as the harmonic contribution of ADC1. According to (4), setting a zero initial phase shift, we can write the following:

$$H\mathrm{meas}_k = H_k^m = (H\mathrm{dac1}_k^{\mathrm{FS}} + H\mathrm{adc1}_k^{\mathrm{FS}}). \qquad (4)$$

In this equation, we assume that amplitudes of harmonics created by the DAC are negligible with respect to the fundamental amplitude of the signal. In this way, we can consider that the ADC is driven by a single-tone signal.

Equation (4) establishes a relation between the harmonic contributions of the two converters involved in the test configuration. In this equation, the left member is known and corresponds to the amplitude of the kth spectral bin measured at the output of the ADC, while the right member represents the unknowns. This relation is possible because at first we fix the initial to zero ($\theta_0 = 0$), and there is no dynamic nonlinearity ($\theta_k = 0$).

This example demonstrates the relationship between one configuration and its resulting equation, which leads to the fundamental idea of the new test method. By using different configurations—DAC1/ADC1, DAC2/ADC1, or DAC1+DAC2/ADC1—we are able to obtain a set of different equations. So, with an adequate set of configurations

(i.e., system of five independent (5)), we are able to discriminate the harmonic contribution of each converter

$$\begin{aligned} H_k^{m,a} &= H\mathrm{dac1}_k^{\mathrm{FS}} + H\mathrm{adc1}_k^{\mathrm{FS}}, \\ H_k^{m,b} &= H\mathrm{dac2}_k^{\mathrm{FS}} + H\mathrm{adc1}_k^{\mathrm{FS}}, \\ H_k^{m,c} &= H\mathrm{dac2}_k^{\mathrm{FS/2}} + H\mathrm{adc1}_k^{\mathrm{FS/2}}, \\ H_k^{m,d} &= H\mathrm{dac1}_k^{\mathrm{FS}} + H\mathrm{dac2}_k^{\mathrm{FS/2}}\cos(k\pi) + H\mathrm{adc1}_k^{\mathrm{FS/2}}, \\ H_k^{m,e} &= H\mathrm{dac1}_k^{\mathrm{FS}} + H\mathrm{dac2}_k^{\mathrm{FS/2}}\cos(k\varphi_1) + H\mathrm{adc1}_k^{\mathrm{FS}}\cos(k\varphi_2) \end{aligned} \tag{5}$$

with $\varphi_1 = \pi - 2arcos(1/4)$, $\varphi_2 = \pi - arcos(1/4)$.

Note that the combiner influence is neglected in the development of this method. Indeed, the combiner used for further experimentations is a fully resistive element. As a consequence, noise should be the main contribution of this element. This assumption has been verified during practical experimentation.

A system of a two-channel AWG has two DACs. If we connect this system to an ADC by set of switches and a combiner, we obtain the setup required for our method. Therefore, it is possible to apply this method to estimate the harmonic contribution of the AWG in the objective to perform a postprocessing correction of this AWG to test ADCs.

3.3. Mass production test using postprocessing correction

The method described in Section 2 permits to estimate the harmonic contributions of the AWG and the tested ADC. Five test configurations are required to achieve this estimation.

After one application of the whole method, if we change the ADC and repeat the complete procedure, we will have a new test result for the ADC under test, but still the same AWG contribution. In fact, once the AWG is characterized, there is only one unknown in (4). Solving this equation, it is therefore possible to determine the harmonic contribution of every new ADC using only one test.

In summary, considering mass production test, we need to apply the five required test configurations in order to estimate the AWG harmonic contribution. Then we only need one additional test per ADC under test and the ADC harmonic contribution is estimated by performing a postprocessing correction of the AWG contribution. As a consequence for mass production test, the test time required to extract the AWG contribution with the five test configurations is negligible compared to total testing time. In other words, the test time required to apply our method is completely comparable to the test time required to apply a conventional ADC test. However, there is no need of AWGs with higher performances than the ADC under test.

4. EXPERIMENTAL VALIDATIONS

Large sets of hardware measurements have been performed to validate the proposed approach. The purpose of the experimentation is to evaluate the efficiency of our method to accurately test an ADC using an AWG of the same resolution. The experimental setup is first introduced, then the protocol is described, and finally results are presented. The performance of the proposed test strategy is evaluated by comparing the THD and SFDR [12, 13].

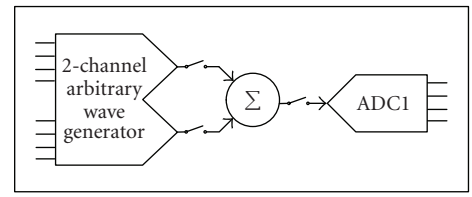

Figure 3: Experimental test setup.

Table 3: Test results for the standard test using low-resolution AWG versus reference test setup.

	THD (dB)	SFDR (dB)
Standard test with AWG2021	−51.6	52.5
Reference test	−68.4	63.5

4.1. Experimental setup

In order to experiment the test strategy, we use a two-channel AWG Sony/Tektronix AWG2021 containing two 12-bit DACs, a resistive splitter/combiner, and a 10-bit ADC, as presented in Figure 3.

Moreover, to compare the results of our method to a conventional ADC test, some reference measurements have been performed using a standard test setup with high-performance analog generator.

Finally, to demonstrate that the AWG is not efficient enough to accurately characterize the ADC dynamic performances without the proposed method, the conventional DSP-based method has been implemented by directly connecting one output of the AWG to the input of the ADC. Table 3 presents the results of this test in comparison with the reference measurements regarding THD and SFDR test parameters.

An error of more than 16 dB is observed on the estimation of the THD, and more than 11 dB on the estimation of the SFDR. This clearly demonstrates that despite the AWG has a resolution 2 bits higher than the ADC under test, it is not efficient enough to set up an accurate DSP-based test. It has been demonstrated in Section 2.2 that a test instrument must have a resolution at least 2 bits higher than the ADC under test resolution to get reliable results. Nevertheless, we observed that a 12-bit resolution for the AWG is not high enough to accurately test a 10-bit ADC because it exhibits worse performances than common 12-bit converters in terms of THD and SFDR.

4.2. Experimental protocol

In order to validate the method, four ADCs of the same batch have been tested. These four samples were chosen in order to

Table 4: Estimated values of the AWG harmonic components using the 5-test procedure.

	Estimation of AWG harmonics				
	Using ADC#1	Using ADC#2	Using ADC#3	Using ADC#4	σ
H2 (dB)	−59.5	−60.1	−58.7	−58.1	0.9
H3 (dB)	−52.0	−52.1	−52.2	−52.3	0.1
H4 (dB)	−79.7	−77.1	−86.4	−90.6	6.2
H5 (dB)	−84.1	−87.5	−90.7	−94.0	4.2
H6 (dB)	−88.7	−82.9	−84.4	−83.6	2.6
H7 (dB)	−94.5	−108.8	−107.6	−120.9	10.8
H8 (dB)	−93.5	−97.2	−87.9	−85.0	5.5
H9 (dB)	−94.9	−84.3	−91.3	−88.3	4.5
H10 (dB)	−93.7	−105.3	−87.3	−82.7	9.8

Table 5: Average THD measurements reference test versus 1-test procedure.

	THD reference (dB)	THD estimation (dB)	Measurement difference (dB)
ADC#1	−66.6	−67.3	0.7
ADC#2	−68.1	−66.7	−1.4
ADC#3	−62.6	−62.4	−0.2
ADC#4	−60.5	−60.6	0.1

Table 6: Average SFDR measurements reference test versus 1-test procedure.

	SFDR reference (dB)	SFDR estimation (dB)	Measurement difference (dB)
ADC#1	68.7	67.9	0.8
ADC#2	70.1	70.0	0.1
ADC#3	67.0	66.7	0.3
ADC#4	63.3	62.1	1.2

represent a significant population of converters considering the SDFR and THD variations. Indeed, these samples have THD varying from −60.5 dB to −68.3 dB and SFDR varying from 63.3 dB to 70.3 dB.

Each of these four ADCs has been tested with a conventional ADC test procedure to obtain reference measurements. The test has been performed ten times to estimate the repeatability of the technique. The evaluated dynamic parameters are the THD and the SFDR.

Then the proposed method has been applied considering both the 5-test procedure used in the preliminary learning phase and the 1-test procedure used during production test. As for the conventional ADC test, the THD and the SFDR parameters are computed from the estimated values of the harmonic components. Again, the test has been performed ten times on each ADC.

4.3. Experimental results of the full test procedure

4.3.1. Learning phase validation

In order to validate the learning phase that permits to characterize the AWG, the 5-test procedure described in Section 3.2 has been applied to the four-sampled ADCs. Results are presented in Table 4 that gives the estimated values of the harmonic components induced by the AWG for 2nd to the 10th harmonics. The last column gives the standard deviation for each harmonic considering the four estimations using the 5-test procedure with 4 different ADCs.

Analyzing these results, it appears that the amplitude of the most significant harmonic components is well estimated when taking into account the different converters used during the 5-test procedure. More precisely in this experiment, the major contributors to the AWG harmonic distortion are the H2 and H3 components. Similar values are obtained for the amplitude of these components whatever the converter used during the procedure (around −59 dB for the H2 harmonic and −52 dB for the H3 harmonic, with a standard deviation of less than 1 dB). For harmonic components with lower amplitude, results show a larger spread depending on the converter used during the procedure. In fact, these harmonics are nearby or below the noise floor and they are not relevant. As a consequence, even a rough estimation of these harmonics will not strongly impact the test-procedure efficiency.

In summary, these results demonstrate that the 5-test procedure allows the extraction of the amplitude of the most significant harmonic components induced by the AWG with a good accuracy, whatever the converter used during the procedure.

4.3.2. Production test validation

Using the AWG harmonic distortion estimated during the learning 5-test procedure, we defined a postprocessing on the response of the ADC under test. The objective of this section is to validate the effectiveness of this postprocessing correction of AWG errors in order to accurately test subsequent ADCs with only a 1-test procedure per ADC.

Table 7: THD estimation accuracy versus AWG resolution.

	AWG resolution	THD reference (dB)	THD estimation (dB)	Measurement difference (dB)
ADC#1	12	−61.8	−61.7	−0.1
	10	−61.8	−62.0	0.2
	8	−61.8	−62.4	0.6
	6	−61.8	−61.7	−0.1
ADC#2	12	−59.8	−59.1	−0.7
	10	−59.8	−58.8	−1.0
	8	−59.8	−58.9	−0.9
	6	−59.8	−59.1	−0.8

Table 8: SFDR estimation accuracy versus AWG resolution.

	AWG resolution	SFDR reference (dB)	SFDR estimation (dB)	Measurement difference (dB)
ADC#1	12	63,9	65,1	−1,2
	10	63,9	64,7	−0,8
	8	63,9	65,4	−1,5
	6	63,9	66,0	−2,1
ADC#2	12	63,0	62,8	0,2
	10	63,0	62,6	0,4
	8	63,0	61,8	1,2
	6	63,0	62,1	0,9

To this aim, we consider the amplitude of the AWG harmonic components extracted with the 5-test procedure using ADC#1. Then the 4 samples of ADCs are tested ten times using the 1-test procedure described in Section 3.3, and postprocessing correction on the response of the DUT is performed to remove the AWG contribution. Results are presented hereafter in comparison with the reference measurements obtained using a conventional ADC test setup and a high-performance AWG.

Table 5 gives the average THD measurements for the four ADC samples tested ten times, using either a conventional ADC test (2nd column) or the 1-test procedure with postprocessing correction (3rd column). Each result is the average of ten measurements. The last column gives the difference between the two measurements.

Table 5 shows that the maximal difference between the proposed method and a conventional ADC test is less than 1.5 dB. This result is very interesting especially when we consider the repeatability of the measurement for the same product on ATE that is around 1 dB.

Results for the SFDR estimation are given in Table 6. As for the THD measurements, we have good estimations. The estimation uncertainty (1.2 dB) is in the same range of the test production scattering (1.3 dB) on the SFDR measurement for the same ADC.

All these results demonstrate that once the harmonic contribution of the AWG has been extracted in the initial learning phase, it is possible to accurately test the ADC dynamic parameters (SFDR and THD) using the 1-test procedure and postprocessing correction.

4.4. Test production validation versus AWG resolution

4.4.1. Introduction

The conclusion of the first experiments is twofold. At first, the 5-test procedure, also called learning phase, gives a stable estimation of the amplitudes of the most significant harmonic components induced by the AWG whatever the ADC used. This conclusion leads to the second experimentation. Indeed the second experimentation allows us to conclude that once the harmonic contribution of the AWG has been extracted in the initial learning phase, it is possible to accurately test the ADC dynamic parameters (SFDR and THD) using the 1-test procedure and a postprocessing correction. These two first experiments were performed with a 12-bit AWG. It has been demonstrated (cf. Table 3) that this AWG is not efficient enough to accurately characterize the ADC dynamic performances using the standard DSP-based method. To go further, a third experiment has been carried out in order to estimate the lowest resolution acceptable for the AWG relatively to the accuracy of the new production test results.

4.4.2. Experimental protocol

The test setup is similar to the previous one, that is, made of a Sony/Tektronix AWG2021, a resistive combiner, and a 10-bit ADC.

Two ADCs were tested, each converter being tested four times, each test being performed with a different AWG

resolution (from 12 bits to 6 bits, by steps of 2 bits). We reduced the AWG resolution by increasing its quantization noise.

4.4.3. Experimental results

Table 7 presents the results of THD measurements for the two ADCs. Three different results are given

(i) reference measurement made with a high-performance AWG in a conventional test setup;
(ii) estimation with our method;
(iii) estimation error.

Table 8 gives the same kind of results as Table 7, but for a different dynamic parameter: SFDR.

Production test repeatability usually shows variations of dynamic parameter estimations of around 1.5 dB. Considering this limit of acceptance for dynamic parameter estimations, Tables 7 and 8 give positive results. Indeed, considering THD estimation for both ADCs, whatever the AWG resolution between 12 bits and 6 bits, there is no estimation error over 1.5 dB. Considering SFDR parameter estimation, there is only one error estimation over this limit; this is for the ADC#1 tested with a 6-bit AWG.

The fact that the limit has not been exceeded for the test of ADC#2 can be explained by the difference between the two ADCs reference measurements. Indeed, the SFDR reference of ADC#1 is better than the one of ADC#2. In other words, for ADC#1 the highest spurious harmonic is closer to the noise level than for ADC#2. As a consequence, the noise contribution to this spurious harmonic is higher. As the noise contribution is random, it induces some measurement variations and errors higher for ADC#1 than for ADC#2.

From the experimental results, we can conclude that the harmonic distortion generated by the AWG is not anymore a limiting factor for most ADCs testing. For example, let us consider a 10-bit ADC. In order to set up a conventional test, the AWG resolution must be at least of 12 or 13 bits. Using the proposed new approach, the constraints on AWG resolution can be considerably relaxed.

5. CONCLUSION

In this paper, we propose an ADC test solution based on the estimation of ADC harmonics and a postprocessing correction of AWG errors on the test response. The method relies on a preliminary learning phase in which the AWG harmonic contribution is estimated. The AWG characteristics are then used during production test with a postprocessing correction of the test data in order to remove the AWG contribution.

Thanks to the proposed method, it is possible to accurately measure ADC harmonics using an ATE with standard-performance AWG, whereas a conventional DSP-based test requires an AWG with a resolution at least 2 bits higher than the ADC under test. This method can be associated to the 2-ADC method [8], that is suited to noise measurements in a test setup similar to the one required to apply the novel method. Indeed, using these two methods we can test all the ADC dynamic test parameters. As a consequence, one of the main benefits of the method is that it allows the test of a wide range of converters with the same standard test equipment, and without the need of customising the test board for every new product. Moreover, after the learning phase, there is no additional test time compared with a conventional ADC test procedure. To go further, it has been proven that using this new approach the constraints on AWG resolution can be considerably relaxed. The validation has been achieved with some 10-bit ADCs. From an industrial point of view, this method is interesting for high-resolution converters. As a consequence, the next experimental validation would be done on higher resolution converters. The same type of ADCs is used for the learning step and the industrial test step of the validations. The approach should still be valid if the two steps were made with different types of converters, at the condition that the AWG settings (frequency and amplitude of the sine wave) are kept both steps.

The theoretical developments have been made under the assumptions that the combiner has no distortion influence and that the ADC is not influenced by dynamic nonlinearity. The combiner influence has been verified during practical experimentations. The ADC used for practical experimentations was not influenced by dynamic nonlinearity. Further theoretical developments would be done in order to take into account ADC architectures that do not prevent dynamic nonlinearity.

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Research Article

Simple Evaluation of the Nonlinearity Signature of an ADC Using a Spectral Approach

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This work presents a new method to estimate the nonlinearity characteristics of analog-to-digital converters (ADCs). The method is based on a nonnecessarily polynomial continuous and differentiable mathematical model of the converter transfer function, and on the spectral processing of the converter output under a sinusoidal input excitation. The simulation and experiments performed on different ADC examples prove the feasibility of the proposed method, even when the ADC nonlinearity pattern has very strong discontinuities. When compared with the traditional code histogram method, it also shows its low cost and efficiency since a significant lower number of output samples can be used still giving very realistic INL signature values.

1. INTRODUCTION

The parameters that characterize the transfer function of an ADC, such as the integral nonlinearity (INL), are some of the most important specifications that must be known to insure the correct operation of the ADC in a certain application. One of the standardized methods to estimate these parameters is the code histogram test [1, 2]. Its main drawback is the excessive cost of its application, especially due to the large number of samples that must be acquired (more than one million) and to the fact that this number increases, in general, in an exponential way with the number of bits of the ADC. The synchronization between the acquisition and the signal stimulation is also a nonelemental task. On the contrary, this method can achieve a very precise measurement independently of the shape of the transfer characteristic; it is a clear trade-off between time and precision.

These drawbacks make the histogram method unfeasible for low-speed and high-resolution converters (>15 bits). For these kinds of converters, the use of methods based on spectral processing can be satisfactory acquiring only some tens of thousands of samples independently of the ADC resolution [3–6]. Although this estimate leads to a partial description of the static behavior of the ADC and, for example, it is not a reliable method to calibrate the nonlinearity, such description may be enough to show a malfunctioning and it may be very useful to set a test protocol [7–9].

This paper presents a new and simple method for ADC nonlinearity (INL) estimation using the spectral processing of its response to a sine-wave excitation. The method does not require a concrete functional form for the ADC transfer curve or for the INL, as [3, 4], nor to apply specific expansion series as in [6], although it is based on a continuous and differentiable mathematical model of the converter transfer function. To reach high precision in the INL estimation, the transfer function should have enough smooth shape; however, we will show that it can be also applied in many cases with strong discontinuities, giving INL signatures good enough to describe the nonlinear behavior of the ADC, this validating its use for rapid production test. The mathematical bases of this method are the standard definition of the INL and the local variation of the ADC transfer function around each ideal transition.

The organization of this paper is as follows. Section 2 introduces the general hypotheses to apply the new method and the mathematics to obtain the INL signature. The method adaptation for its application through the spectral estimation is derived in Section 3. Section 4 shows some

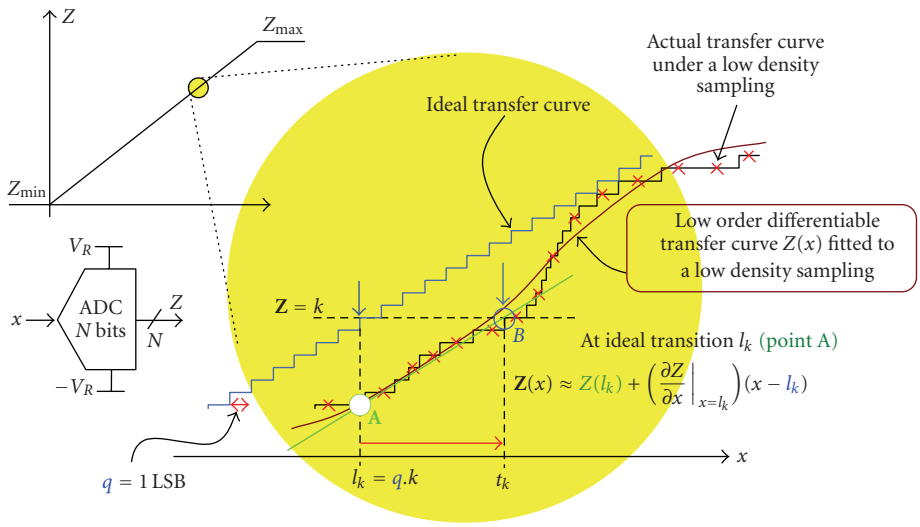


FIGURE 1: Modelling the non-linearity: the first order Taylor's expansion of the transfer function $\mathbf{Z}(\mathbf{x})$ around an ideal transition $\mathbf{l_k}$. $\mathbf{t_k}$ represents the real transition where the output code Z changes from $k-1$ to k.

simulated and real examples of application for the proposed method and Section 5 draws the conclusions.

2. MODELLING THE NONLINEARITY

The ADC basic model that we are considering supposes that the transfer curve: (1) is a smooth nonnecessarily polynomial function $Z(x)$, continuous and differentiable with respect to the input, (2) it must be strictly increasing and therefore with a nonzero derivative. The description as a continuous function must be also understood in the way that the resolution of the converter is high enough to consider the quantization effect embedded in other noise contributions.

Mathematically, the proposed input-output model is

$$z = Z(x) + \varepsilon(x), \quad \exists \partial_x Z \neq 0, \quad \forall x \in [-V_R, V_R], \tag{1}$$

where the error function $\varepsilon(x)$ is of the same order than the quantization error. Without any loss of generality, the input range will be considered bipolar and centred at zero, $[-V_R, V_R]$.

Figure 1 illustrates the nonlinearity modeling. Both the ideal and a hypothetic real transfer function of an N-bit converter are shown. The curve $Z(x)$ is that obtained by fitting a low-density sampling of the real transfer curve. Considering the previous conditions, a first-order Taylor's expansion of the mild transfer function $Z(x)$ is going to be calculated around each ideal transition, l_k. The set of points formed by the ideal transitions can be expressed as $l_k = q \cdot k$, $k \in [-2^{N-1}, 2^{N-1} - 1]$, where $q = 2V_R/2^N$ is the LSB of the N-bit ADC. Then, we have

$$Z(x) \approx Z(l_k) + \partial_x Z(l_k) \cdot (x - l_k), \quad \forall\ x \approx l_k. \tag{2}$$

Evaluating the expression at the corresponding real transition, $x = t_k$, where the output code value changes from $k-1$ to k,

$$k \approx Z(l_k) + \partial_x Z(l_k) \cdot q\mathrm{INL}_k, \tag{3}$$

where it has been used that $k \approx Z(t_k)$ and the standard INL definition $\mathrm{INL}_k = (t_k - l_k)/q$ [1].

From (3), the following expression for the INL can be obtained:

$$\mathrm{INL}_k \approx \frac{k - Z(l_k)}{q\,\partial_x Z(l_k)}. \tag{4}$$

Notice that this expression can be evaluated only if it is possible to obtain the derivative of the function $Z(x)$.

If the second derivative exists, an alternative expression can be obtained using the second-order Taylor's expansion. In any case, in this work only the expression (4) will be used since the nonlinearity of the ADC is considered very small: $\max_k\{|\mathrm{INL}_k|\} < 2^{N-10} (N > 10)$.

3. APPLICATION OF THE MODEL USING A SPECTRAL APPROACH

This section shows how to apply expression (4) in the case that a spectral measurement is used to process the ADC response to a sinusoidal input.

Let us assume that the input excitation is

$$x(t) = A\cos(\omega_x t + \varphi_x) + B \tag{5}$$

and that it covers all the input range without causing the ADC saturation ($A \approx V_R$, $B \approx 0$). The input frequency ω_x is low enough to produce unimportant dynamic effects. The phase-shift φ_x and the offset B do not need to be known a priori. The amplitude, A, has to be known only when the gain of the ADC, g, is very different from the unity and/or it is wanted to estimate the gain error of the A/D conversion.

For such input, the ADC output is a superposition of harmonics of the excitation frequency,

$$Z(x(t)) = C_0 + \sum_{n \geq 1} C_n \cos(\omega_n t + \varphi_n), \quad \omega_n = n\omega_1, \tag{6}$$

where the frequency ω_x and the phase-shift φ_x are identified with the frequency ω_1 and the phase-shift φ_1 of the main harmonic, respectively. Rejecting, in a first approximation, the other harmonics ($n > 1$), the input amplitude can also be related to the amplitude of the 1st harmonic by means of the gain g of the ADC. Using a simple linear model $Z(x) \approx (g{\cdot}x)/q + z_{\text{os}}$, where g is the gain and z_{os} is the offset of the ADC [1], it can be obtained as follows:

$$\begin{aligned} C_1 &= g{\cdot}A/q, \\ C_0 &= (g{\cdot}B)/q + z_{\text{os}}, \\ \omega_1 &= \omega_x\,, \\ \varphi_1 &= \varphi_x. \end{aligned} \tag{7}$$

A more suitable model, but more costly, could still use the previous linear relationship but considering as outputs the sine-wave signal $\hat{z}(t) = C_A\cos(\omega_z t + \varphi_z) + C_B$ that best fits to (6) in the sense of the least mean-squared error. In this case, expressions (7) are still valid using the parameters C_A, C_B, ω_z, and φ_z. In any case, whatever the model is, the transfer function derivative in (4) can now be calculated in an indirect way:

$$\begin{aligned} \partial_x Z = \frac{\partial_t Z(x(t))}{\partial_t x(t)} &= \frac{\sum_{n\geq 1}\omega_n C_n \sin\left(\omega_n t + \varphi_n\right)}{\omega_x A \sin\left(\omega_x t + \varphi_x\right)} \\ &\approx \frac{g}{q}\left[1 + \sum_{n\geq 2}\frac{C_n}{C_1}\frac{n\sin\left(n\omega_1 t + \varphi_n\right)}{\sin\left(\omega_1 t + \varphi_1\right)}\right], \end{aligned} \tag{8}$$

where the relations in (7) have been applied to the simplest model.

Now, let us evaluate expressions (6) and (8) at the ideal transitions, $Z(l_k)$, $\partial_x Z(l_k)$.

If τ_k are the time instants in which the sinusoidal input signal crosses the ideal transitions of the ADC, $x(\tau_k) = l_k$ (see Figure 2), it can be written as

$$\begin{aligned} l_k &= A\cos\left(\omega_x\tau_k + \varphi_x\right) + B \\ &\longrightarrow \omega_x\tau_k = -\varphi_x + \operatorname{Arccos}\left(\frac{l_k - B}{A}\right). \end{aligned} \tag{9}$$

Applying relations (7),

$$\delta_k = \omega_1\tau_k \approx -\varphi_1 + \operatorname{Arccos}\left(\frac{g{\cdot}k + z_{\text{os}} - C_0}{C_1}\right) \tag{10}$$

that gives the phases used in (6) and (8)

$$\omega_n t + \varphi_n|_{t=\tau_k} = n\omega_1\tau_k + \varphi_n = n\delta_k + \varphi_n \tag{11}$$

to obtain, respectively, $Z(l_k)$ and $\partial_x Z(l_k)$. Finally, expression (4) for the INL becomes

$$\text{INL}_k \approx \frac{k - \left(C_0 + \sum_{n\geq 1}C_n\cos\left(n\delta_k + \varphi_n\right)\right)}{g{\cdot}\left[1 + \sum_{n\geq 2}\left(C_n/C_1\right)\left(n\sin\left(n\delta_k + \varphi_n\right)/\sin\left(\delta_k + \varphi_1\right)\right)\right]}. \tag{12}$$

Notice that in (10) and (12) the only quantities to evaluate are the harmonic amplitudes $\{C_n\}$, the phase-shifts $\{\varphi_n\}$, and the gain g of the ADC. All of them can be estimated using the spectral processing of the output. In general, z_{os} in (10) can be considered null, which is equivalent to consider that z_{os} is cancelled out by the input offset. When $g = 1$ and $z_{\text{os}} = 0$ are used in (10) and (12), the ADC intrinsic nonlinearity is being estimated, that is, the nonlinearity signature without gain and offset effects. This is the INL usually evaluated according to the standards [1, 2].

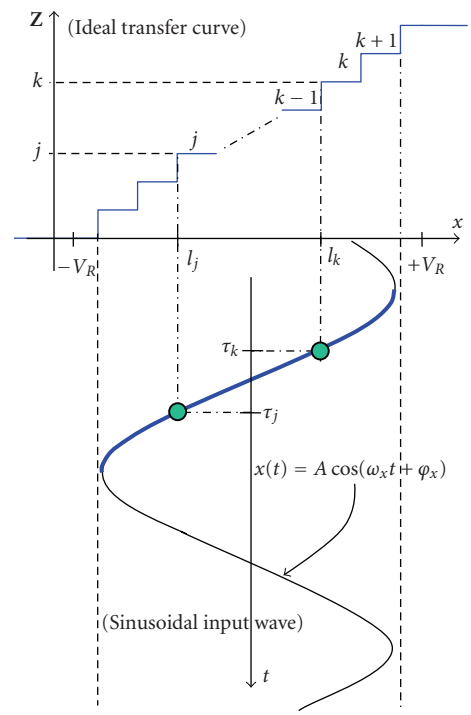


FIGURE 2: Defining the input wave crossing points τ_k over the ADC ideal transitions $\mathbf{l_k}$. According to (10), these timing points allow work out the phase values of the output harmonics when the input wave crosses an ideal transition.

The number of harmonics that must be selected to apply (12) depends on both the spectral discrimination that the total noise allows and the reliability of the mathematical method used to estimate the harmonic parameters. In all of our experiments, we have used a conservative criterion: the selected harmonics are those with amplitudes at least 10 dB over the spectrum noise floor. Mathematical methods to estimate spectra are basically based on discrete-time Fourier transform (DTFT) [1, 2].

In very good coherent experiments (input frequency and sampling frequency are commensurable values), and when the noise is small enough and well described by additive white model, simple relationships can be used. Being acquired L samples of the ADC output, $\{z_i\}_{i=1}^{L}$, with the sampling frequency f_s and satisfying the input wave frequency $f_x = (M/L)f_s$ with M and L relative prime integers (to excite at least L ADC different levels), the DTFT is obtained of the output register, $\{\zeta_j\} = \text{FFT}\{z_i\}$, selecting after that the most significant spectral lines respect to the noise floor, $\{\zeta_{j_n}\}_{n=1}^{H}$. The main harmonic occurs at $j_1 = M$. The correct frequencies for the other lines must be

carefully identified because if high-order harmonics exist, $\omega_n > \omega_s/2$, their spectral lines are folded at the DTFT interval $[0, f_s/2]$. With these considerations, expressions to estimate the parameters involved in (12) are

$$\begin{aligned}
\omega_1 &= 2\pi f_s M/L,\\
\omega_n &= n\omega_1,\\
C_0 &= \underset{i}{\text{mean}}(\{z_i\}),\\
C_n &= (2/L)||\zeta_{j_n}||,\\
\varphi_n &= (-1)^{p_n}\text{Arg}(\zeta_{j_n}),\\
p_n &\underset{k\geq 0}{=} \begin{cases} 0, & \omega_n/\omega_s \in [k, (2k+1)/2[,\\ 1, & \omega_n/\omega_s \in [(2k+1)/2, (k+1)[, \end{cases}\\
g &= q\cdot \text{rms}\{z_i\}/\text{rms}\{x(t)\},
\end{aligned} \tag{13}$$

where $\text{rms}\{x(t)\}$ is the root mean square of the input wave and p_n corrects the inversion of estimated phase for the case that a spectral line is folded.

Although it has been suggested about (12) that the value of the gain g is not strictly necessary for the intrinsic nonlinearity evaluation, in (13) it has been included an expression that uses the root mean square for its estimation. This expression allows a simple way to evaluate g because it is easy to measure the rms value of the input signal using a wattmeter. For a low-distortion ADC (such as it has been considered for the application of the method), the difference of the gain value estimated using this way is usually less than 0.5% respect to the gain value estimated using a standardized method, such as that estimating g through the slope of the best-fitting line to the transition set, or the slope of the straight line that joins the extreme transitions on the ADC transfer function [1].

If R registers ($R > 1$) of length L are acquired to average the noise, all of them must be consecutively taken to do not lose the phase information. This is the same as to trace a unique register with $R{\cdot}L$ output samples of L-sample periodicity. In this way, (13) is still used but with the averaged module and the averaged phase spectrum values,

$$\begin{aligned}
\overline{||\zeta_j||} &= \sqrt{\text{mean}_{m=1,\ldots,R}\{||\zeta_j^{(m)}||^2\}},\\
\overline{\text{Arg}(\zeta_j)} &= \text{mean}_{m=1,\ldots,R}\{\text{Arg}(\zeta_j^{(m)})\},\\
&\text{with } \{\zeta_j^{(m)}\}_{m=1}^{R} = \text{FFT}\{z_i^{(m)}\}.
\end{aligned} \tag{14}$$

If a coherent sampling is not possible, *windowing* to each register should be applied to reduce the spectral leakage, $\{\zeta_j^{(m)}\}_{m=1}^{R} = \text{FFT}\{w_i z_i^{(m)}\}$, where $\{w_i\}_{i=1}^{L}$ is the convolution window. In general, the expressions in (13) have to be corrected since the estimates are biased depending on the applied window. In [2, 10], there are some suggestions to select the most appropriate window. For all of our noncoherent experiments, we have used a 4-term cosine-class window and an estimation method based on phase regression presented in [11], which requires that $R \geq 2$.

When high-order harmonics exist and they are folded in the $[0, f_s/2]$ band, a particular input frequency has to be selected in such a way that no significant harmonic overlaps. Problems are minor if coherent sampling and no windowing are applied. We have always selected test frequencies that lead spectral lines to separate each other at least 10 bins, when 4-term cosine window has been used.

The DC component is evaluated by means of the weighted mean of the samples, using as weight function the convolution window,

$$C_0 = \underset{m}{\text{mean}}\left\{\frac{\sum_i w_i z_i^{(m)}}{\sum_i w_i}\right\}. \tag{15}$$

4. APPLICATION EXAMPLES

4.1. Simulated experiments

This section shows the simulation results obtained applying the introduced method in two different models for the ADC. The first converter, ADC_1, has a very regular transfer curve and a smooth INL. For the second one, ADC_2, the transfer curve is nonmonotonic and its INL has very strong discontinuities.

4.1.1. Nonspectral approach (DC sweep) on low-speed, high-resolution ADC_1 model

Before applying (12), let us show the immediate approximation of (4). The ADC_1 has been excited using a DC signal whose value is changing inside the input range. For each value of the input, $\overline{x}_i$, it is obtained an output register to calculate the corresponding average code $\overline{z}_i$. Using the set $\{(\overline{x}_i, \overline{z}_i)\}$ it can be built the Mth order best-fitting polynomial model, $Z_M(x)$, which allows to apply (4) directly.

ADC_1 is a high-level model of a 14-bit $\Sigma\Delta$ converter, with reference voltages 0.0 V and 5.0 V but with a practical input range [0.5 V,4.5 V]. The model reproduces the nonlinear, noisy, and frequency behavior. The sampling frequency is $f_s = 100\,\text{kHz}$. The noise due to both the input and the ADC, referred to the input, is approximately 2LSBs rms white noise. A DC sweep with about 4000 points has been carried out in the range [0.7 V, 4.3 V]. For each DC value, it has been taken a register of 50 points, being the obtained code in the range $Ik = [-5792, 5801]$. Using this dataset, the $M = 32$nd-order best-fitting polynomial has been calculated by means of the first class Chebyshev base. The choice of the order is deduced from the harmonic significant number found in the experiment that will be described in next subsection. For each value k of Ik, it has been evaluated $Z_M(l_k)$, $\partial_x Z_M(l_k)$, and INL_k in (4).

On the other hand, it has been applied the standard sinusoidal histogram method [1, 2] to determine a good estimate of the INL (*real INL* from now on) in order to establish a reference for comparison purpose. The obtained results are depicted in Figure 3.

Figure 3(a) shows the superposition of both estimates. The thick line is the curve calculated by (4). To show the reliability achieved, in Figure 3(b) it is depicted the difference

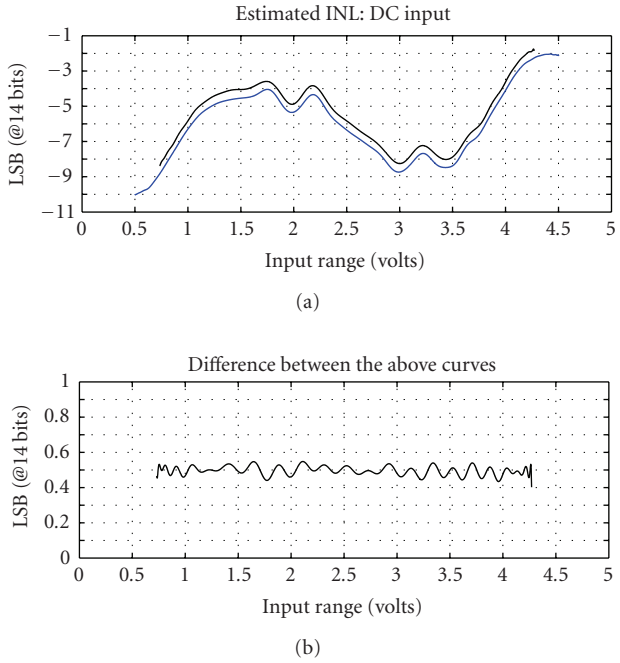


FIGURE 3: (a) INL estimates of the example ADC_1. In thick (black) line the one obtained by (4), in thin (blue) line the *real INL* evaluated by the Histogram method. (b) Differences between both estimates in (a).

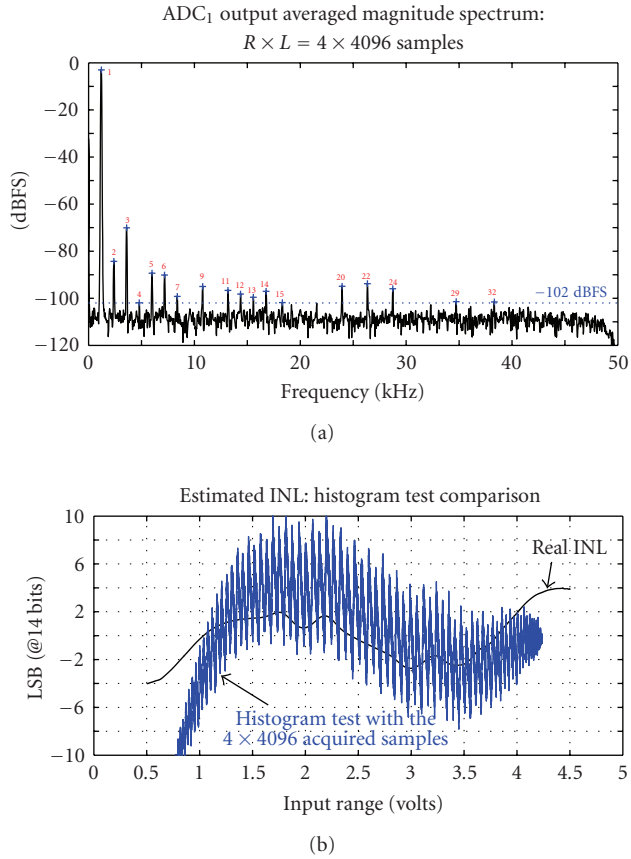


FIGURE 4: (a) Typical averaged magnitude spectrum obtained from the ADC_1 output. It is used for the selection of the spectral lines taken as harmonics. (b) Comparison between two ADC_1 INL Histogram estimations: in thin (blue) line the one estimated with very few samples, (the four registers acquired to apply the new method). In thick (black) line the *real INL*.

between both curves, which is affected by a systematic 1/2 LSB error. This is because, for convenience, (2) and (3) have been obtained using the transitions and not the code centres. This is not very important since, in general, the offset value of the ADC is not used in the expression (12) and so it must be corrected by means of the elimination of its mean value. In any way, it can be noticed the high accuracy achieved by the method. This is justifiable since the INL curve of this ADC follows a very smooth behavior.

4.1.2. *Spectral approach (sine input) on low-speed, high-resolution ADC_1 model*

For the same ADC_1 converter, it has been simulated a set of 35 experiments that use a sinusoidal input and calculate the INL from (12). To estimate the parameters from the spectrum, it has been used the procedure described in [11]. The amplitude of the sinusoidal input is approximately −3 dBFS, the offset is about 100LSBs, and the frequency is near $f_s/83$. The phase has been evenly spread inside the range $[-\pi, \pi]$ all over the experiments. The equivalent noise at the input is approximately 1LSB rms white noise. In each experiment, $R = 4$ consecutive registers of $L = 4096$ samples are used. A set of 500 samples have been eliminated at the beginning of the four registers to reduce the settling errors. A typical spectrum is shown in Figure 4(a). As the background noise is about −112 dBFS, the spectral lines selected are those that have the amplitude higher than −102 dBFS. The typical selection detects about 15 harmonics with orders up to 30th. Figure 4(b) shows a comparison between the *real INL* (thick line) and the estimated (thin line) using the histogram method but with only the above four acquired registers. It is obvious that the number of acquired samples is not still enough to sketch the INL shape. On the other hand, the results obtained in one of the experiments using the spectral estimation and (12) are shown in Figures 5(a) and 5(b). As it can be noticed, our method gives good enough results with the 4·4096 acquired samples. Both INL curves have been depicted with the offset corrected, since the offset of the ADC_1 has been supposed null $z_{os} = 0$. To show how robust the estimate from (12) is, Figure 5(c) depicts the differences between the INL of each experiment and the *real INL*.

4.1.3. *Spectral approach (sine input) on medium-speed, high-resolution model ADC_2*

The ADC_2 is a high-level model of a 16-bit pipeline converter that operates with reference voltages of −2.0 V and 2.0 V. The sampling frequency is $f_s = 5.0$ MHz. The noise due to both the input and the ADC, referred to the input, is approximately 1LSB rms white noise. The amplitude of the

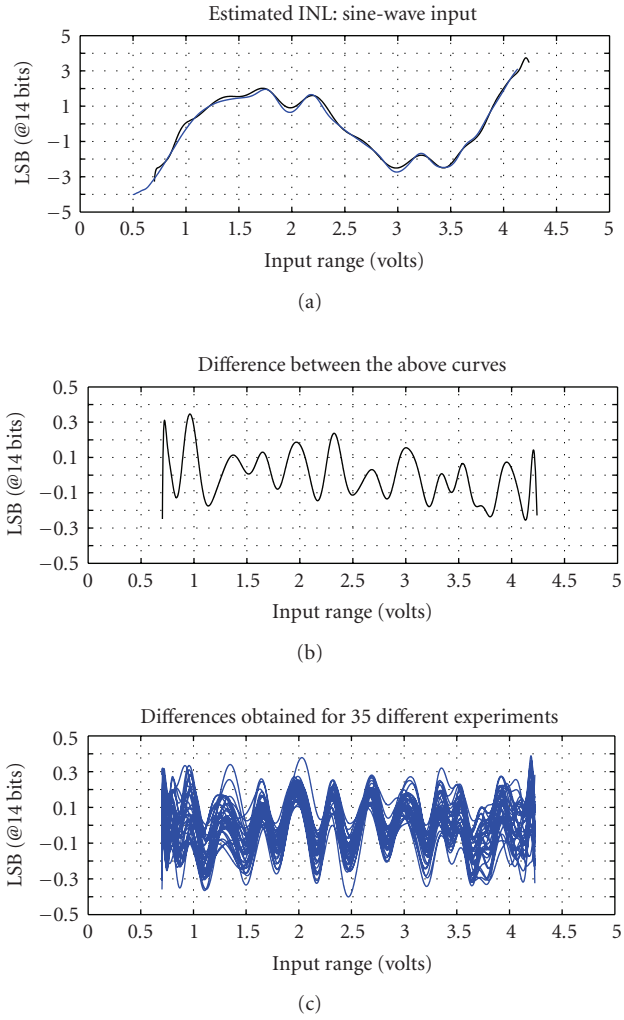


Figure 5: (a) Overlapped ADC_1 INL curves: in thick (black) line the one obtained by spectral estimation and (12). In thin (blue) line the *real INL*. (b) Difference between the two above INL signatures. (c) Differences obtained for all of the experiments on the ADC_1.

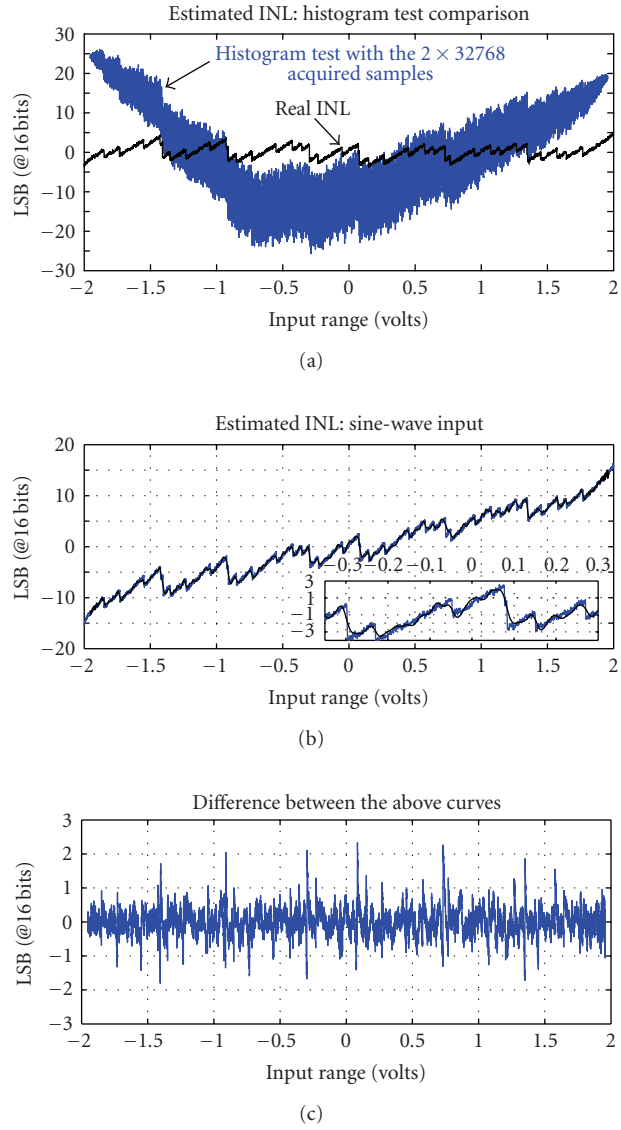
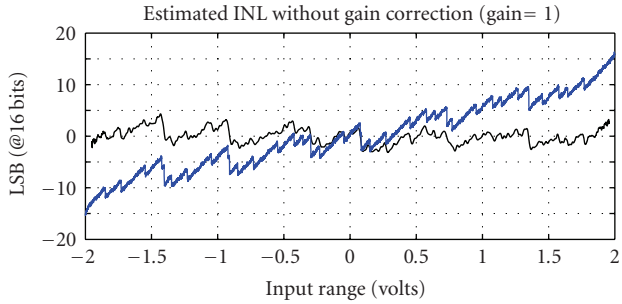


Figure 6: (a) Comparison between two ADC_2 INL Histogram estimations: in thin (blue) line the one estimated with very few samples (the two registers acquired to apply the new method). In thick (black) line the *real INL*, (no gain effect has been included). (b) Overlapped ADC_2 INL estimations: the estimated using the spectral approach and (12), and the *real INL* (gain effects are included). (c) Difference between the above INL signatures in (b).

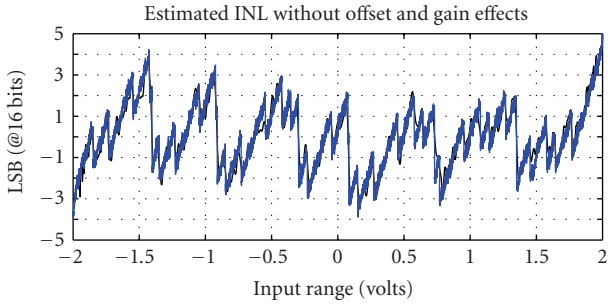
input signal is approximately −0.2 dBFS, the offset is about 10LSBs and the frequency is near $f_s/222$.

The phase has been evenly spread allover the experiments inside the range $[-\pi, \pi]$. In these experiments, it has been taken two consecutive registers with 32768 samples each. In this example, the background noise appears at about −130 dBFS, so the selected spectral lines are those that are harmonics with amplitudes higher than −120 dBFS.

The so irregular and discontinuous structure of the INL of this ADC leads to a typical selection about 150 harmonics with orders up to 600th. Figure 6 shows the typical results obtained. Figure 6(a) shows a comparison between the *real INL* (thick line) and the one estimated (thin line) using the histogram method with the above two acquired registers. The number of acquired samples is not still enough to sketch the INL shape. However and in spite of such a discontinuous structure of the nonlinearity of the ADC_2, the estimate from (12) absolutely follows the *real INL* evaluated using the standardized histogram method (Figure 6(b)). The difference between both estimates has been depicted in Figure 6(c). Biggest differences occur at the higher transitions, where the smoothing effect due to the limited number of harmonics that has been selected is more evident. Even if the gain is not evaluated, the intrinsic nonlinearity of the ADC (the one where the gain and the offset are corrected) still can be extracted. Figure 7(a) shows the results obtained for the ADC_2 making $g = 1$ in (10). Although the difference is noticeable, if the gain and offset are eliminated from both curves (subtracting their best-

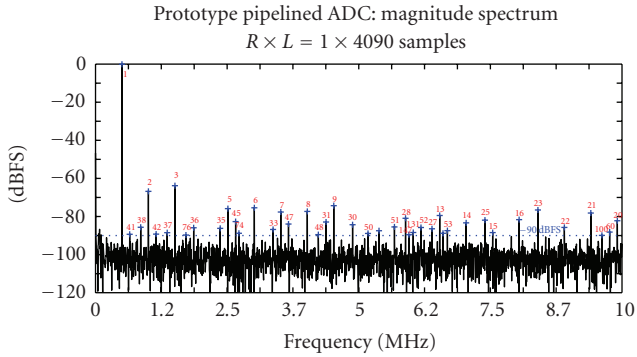


(a)

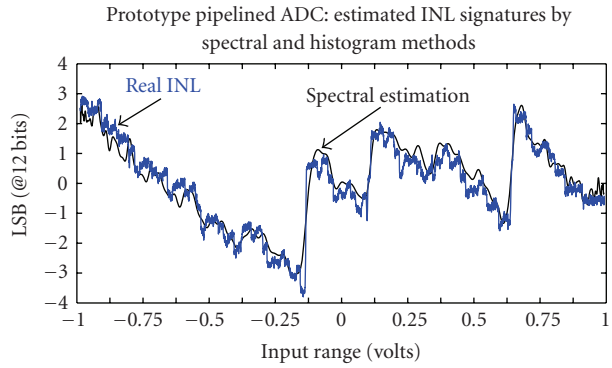


(b)

Figure 7: (a) Thick (black) line: estimated ADC_2 INL using (12) and taking the gain equal to 1. In thin (blue) line the *real INL* where gain effects are included. (b) Overlapping of the two above estimations after the gain and offset effects have been corrected.



(a)



(b)

Figure 8: (a) Typical magnitude spectrum obtained from the prototype Pipeline ADC output. (b) Comparison between two INL estimations: In thin (blue) line, the *real INL*. In thick (black) line the INL estimation from the spectral approach and (12) using the spectrum in (a) (gain and offset effects have been corrected).

fitting lines), a good approximation can be achieved as Figure 7(b) shows.

4.2. *Real experiments*

This section shows the results obtained applying the introduced method to a real ADC. This converter has a transfer curve with very strong discontinuities.

4.2.1. *Spectral approach (sine input) on high-speed, low-voltage experimental prototype ADC*

The ADC under test is a fully differential 12-bit pipeline converter prototype in a 120 nm CMOS technology with reference voltages −1 V and 1 V. The sinusoidal input has been nonbuffered AC coupled to the ADC and generated using the Agilent N8241A AWG, with amplitude of −0.1 dBFS and a frequency of 500 kHz approximately. In this case, as a good coherent experiment has been done, only a register of 4090 samples has been acquired using a 20 MHz sampling master clock (neither averaging nor windowing has been applied). Figure 8(a) shows a typical nonwindowed magnitude spectrum, with the floor noise at about −100 dBFS. The harmonics selected were those with the amplitude higher than −90 dBFS, and the typical selection takes about 45 harmonics with orders up to 150th.

Figure 8(b) compares the INL pattern obtained using the spectral approach (from (12)) with the *real INL* estimated using the standard histogram method. Notice that the INL evaluated from our proposed method describes the shape of the *real INL* good enough, even in hard discontinuities. Best results are obtained if more registers have been acquired, since noise averaging improves both uncertainty and the number of selected harmonics.

5. CONCLUSIONS

In this paper, a new method for the INL estimation of ADCs has been presented which is based on a continuous model of the ADC transfer function. The method uses a spectral processing of the ADC output to estimate its harmonic amplitudes and phase-shifts from which the INL signature is derived. Different ADC examples with very different nonlinearity pattern have been performed to validate the proposed method. The obtained results have been compared with those obtained from the traditional histogram method and have proven not only the feasibility of the new method, even when the ADC nonlinearity has very strong discontinuities, but also its low cost and efficiency since a significant lower number of output samples can be used still giving very realistic INL signature values.

ACKNOWLEDGMENTS

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Research Article

Choice of a High-Level Fault Model for the Optimization of Validation Test Set Reused for Manufacturing Test

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With the growing complexity of wireless systems on chip integrating hundreds-of-millions of transistors, electronic design methods need to be upgraded to reduce time-to-market. In this paper, the test benches defined for design validation or characterization of AMS & RF SoCs are optimized and reused for production testing. Although the original validation test set allows the verification of both design functionalities and performances, this test set is not well adapted to manufacturing test due to its high execution time and high test equipment costs requirement. The optimization of this validation test set is based on the evaluation of each test vector. This evaluation relies on high-level fault modeling and fault simulation. Hence, a fault model based on the variations of the parameters of high abstraction level descriptions and its related qualification metric are presented. The choice of functional or behavioral abstraction levels is discussed by comparing their impact on structural fault coverage. Experiments are performed on the receiver part of a WCDMA transceiver. Results show that for this SoC, using behavioral abstraction level is justified for the generation of manufacturing test benches.

1. INTRODUCTION

New efficient methods have emerged to design analog, mixed and RF (AMS & RF) or hybrid integrated circuits (ICs). Nowadays, the test of these ICs is becoming a crucial challenge for manufacturers. The trend toward miniaturization imposes to develop more and more integrated systems. Thus, electronic components are becoming systems-on-chip (SoCs) or systems-in-package (SiPs). This increasing complexity forces designers to define new design methodologies adapted to these complex systems with shorter time-to-market (TTM) and lower manufacturing cost constraints. However, the problem is not only to achieve short TTM but also to control the quality of final products. In fact, this growing complexity and the multiphysics systems integration increase the production testing difficulties and the test costs. In one hand, the SoC complexity involves low testability (i.e., low component parameters controllability and observability). In the other hand, new component natures (RF, mechanical,...) and their relative manufacturing processes involve fault modeling difficulties. Currently, the production test of AMS & RF SoCs is often performed by using a subset of the manually generated characterization test stimuli. Then, the evaluation of this subset is empirically made.

This paper relies on a method to evaluate and to generate a manufacturing test set from an initial characterization test set [1]. This method is performed on a Wireless SoC (WSOC) thanks to high-level fault injection and simulation techniques. The increasing SoCs complexity involves high transistor level simulation times for AMS & RF systems. In some cases, it is even impossible to simulate the whole system at the transistor level. This problem can be partially solved by describing the electrical system with higher description level (behavioral or functional level) rather than transistor level. So, when it becomes impossible to simulate faulty descriptions at low level, we propose to use functional or behavioral level descriptions. The aim of this paper is to define the most adapted abstraction level to measure the quality of a WSOC manufacturing test set. Obviously, there is a trade off between the qualification accuracy and the computation time.

In the first part, the fault injections and simulation techniques with functional, behavioral, and transistor description level are presented. The definitions of the faults models

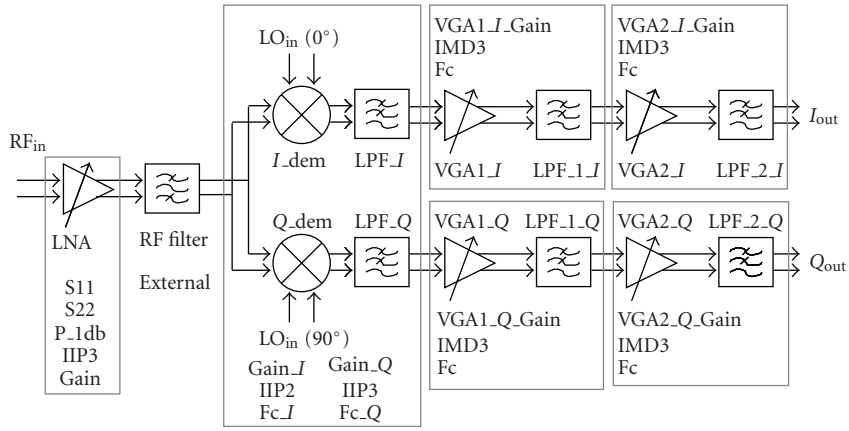

Figure 1: WCDMA receiver part (RX).

used to validate circuits at several abstraction levels are given. Then, the different descriptions of the WCDMA system applied to validate our method are presented. In the fourth section, our PLAtform for system qualification with mixed and analog signals (PLASMA) is detailed. Then, results provided by PLASMA for the receiver part of the WCDMA transceiver with functional and behavioral level are compared. Finally, the accuracy of functional and behavioral fault coverage is compared with structural fault coverage. This last step justifies the choice of behavioral level for the qualification of production testing.

2. HIGH-LEVEL FAULT MODELING AND FAULT INJECTION IN PLASMA

Faults injection and simulation techniques can be performed on models described at all abstraction levels. Obviously, the choice of the abstraction level is always a trade off between model accuracy and computation time. Modeling level used for the qualification of production test set must be close to physical level because manufacturing defaults are made of physical parameters modifications (oxide thickness, length, width, etc.). Thus, transistor fault modeling level, based on parameter variations of low-level components (inductor, capacitor, resistor, or transistor) is generally the most adapted for the test set generation applied on analog circuits. However, due to too high simulation times, this level is not adapted for the simulation of complex SoCs. So, we propose to use higher abstraction level descriptions to perform the manufacturing test generation. These high-level descriptions of the WSoC already exist because they have been developed and validated during the top-down design flow. The functional level is used for the development of the SoC architecture by converting system specifications into functional blocks. The behavioral level is used for the description of the system with more details than the previous level, in particular electrical effects (nonlinearity, coupling effects, impedances mismatching, etc.). The behavioral level allows fitting blocks interfaces by describing the system with more accuracy. This level has led to the standardization of behavioral languages like VHDL-AMS [2].

PLASMA interacts with the Mentor Graphics' ADvance MS RF VHDL-AMS simulator to perform the test set evaluation. So, PLASMA inherits all the characteristics of this simulator. It means that fault injection can be done

(i) on multilevel abstraction systems (i.e., transistor, behavioral, functional levels),

(ii) on multilanguage descriptions (Spice, VHDL-AMS, VHDL),

(iii) on multinature systems (analog, digital, RF, etc.).

In PLASMA, the fault model is made of only a single and small variation of one parameter in the original description. We call this faulty description a mutant. We assume that a huge modification of the description has little chance to appear during the design and the manufacturing processes. However, if this kind of fault appears, it should be easy to detect.

3. WCDMA SYSTEM

The studied system is the receiver part of a wideband code divided multiple access (WCDMA) transceiver. WCDMA is a technology used for third-generation cellular systems (3G). The frequency range down-link (bases station to user equipment) or receiver part is [2110–2170 MHz]. The modulation defined in the WCDMA standard is a classical IQ modulation based on two signals: I "in-phase" component of the waveform, and Q represents the "quadrature" component. WCDMA standard specifies several parameters: maximal and minimal output power, maximal power out of frequency band, adjacent channel leakage ratio (ACLR).

Figure 1 presents the architecture of the receiver part (Rx). It is a classical architecture made of low-noise amplifier (LNA), external surface acoustic wave (SAW) RF filter, mixers, base-band voltage gain amplifiers (VGA), and internal filters. Digital registers (not illustrated in Figure 1) control the LNA and VGA gains. These registers permit to control the receiver parameters; they can be used to control the system during validation [3].

Table 1: Limits of amplifier parameters.

Parameters	Typical value	Minimum	Maximum
Gain	13.85 dB	11.85 dB	15.85 dB
S11	−14.47 dB		−10.25 dB
S22	−6.1 dB		−1 dB
IIP3	−0.24 dBm	−5.03 dBm	
IIP1	−8.84 dBm	−18.4 dBm	

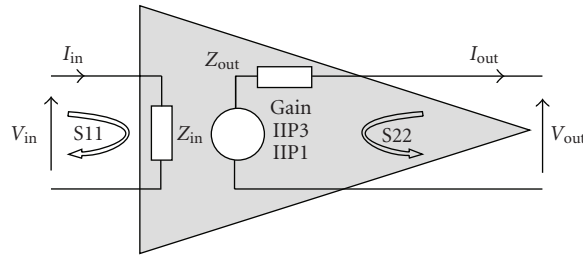

Figure 2: Behavioral model of LNA.

3.1. Functional model

In the top-down design flow, the architecture is first described at the functional level. The system functional specifications are budgeted into several functional blocks. Functional model does not implement electrical equations but only analytical relations between input and output (gain, transfer function, etc.). For example, functional description of LNA is only made of gain parameter; its specified values are presented in the first line of Table 1. The functional description of WCDMA receiver part is written with the VHDL-AMS language.

3.2. Behavioral model

In the following, the behavioral model of the LNA is presented in order to figure out this modeling level. In behavioral modeling, two classes of parameters, functional and electrical parameters, are defined. The choice of these parameters follows the verification plan [4]. The verification plan begins by identifying particular area of concern in the design. For example, if an area of concern is the loading of one block on another, the plan specifies that impedance matching must be modeled. In our case, the amplifier model is made of one functional parameter, the power gain (Gain), and several electrical parameters: input and output impedances (Z_{in}, Z_{out}), S parameters (S11, S22), compression point at 1 dB (IIP1), third-order intermodulation distortion (IIP3) (Figure 2). Table 1 specifies the limits of several parameters. Each parameter is defined by a typical value and with one or two worst-case values (minimum and/or maximum admitted values). For example, the gain is specified by two limits because both limits are significant; the other parameters have only one significant limit.

The other blocks of the system are also modeled following the verification plan with a few additional parameters: IIP2 (second-order intermodulation distortion), DC offset, and cut off frequency. Figure 1 gives a parameters list for each block. Finally, the receiver part is modeled by only 23 functional and electrical parameters (Figure 1). These parameters are the most significant parameters in the system design. Obviously, our qualification process could be also applied on a description involving additional parameters. The entire WCDMA transceiver is modeled with VHDL-AMS language.

3.3. Transistor-level model

In this study, the transistor-level description is considered to be the reference because it is close to the physical level. Then, we assume that this level allows us to evaluate the quality of our test set optimization. Only LNA has been described at the transistor level (Figure 3) because it would be too time-consuming to simulate the entire system at the transistor level. So, our evaluation is only realized on LNA functional, behavioral, and transistor-level parameters. LNA is particularly interesting because numerous behavioral parameters have been defined for this component. But, the transistor-level evaluation should also be realized for each block in the system. The simulation of the transistor-level LNA description embedded into the system is possible using the multiabstractions simulation technique. It means that simulations are realized using several abstraction levels for the different blocs in the systems: in this case, only the LNA is described at the transistor-level and the other blocs are described at the behavioral level. The simulations are realized with the Mentor Graphics' ADvance MS RF simulator. In addition, the Mentor Graphics behavioral VHDL-AMS library's CommLib RF [5] has been used.

The 2.1 GHz LNA circuit given in Figure 3 includes an amplification stage based on a cascode structure. The advantage of this architecture is to decrease noise and to improve linearity. Input and output matchers are added for the impedance matching.

4. PLASMA: PLATform FOR SYSTEM QUALIFICATION WITH MIXED AND ANALOG SIGNALS

PLASMA is an automatic test set qualification and generation platform which uses fault injection and simulation techniques. The fault simulation technique relies on the comparison of the simulation results of fault-free and faulty circuits (Figure 4). Faulty and fault-free descriptions are simulated with the same vectors. When the comparison of fault-free and faulty circuits simulation results involves a difference, the fault has been both activated and propagated toward one or more primary outputs; we say that the fault is detected. Although PLASMA contains an automatic stimuli generator, only test set qualification part and optimization will be discussed in this paper. The optimization involves the reduction of the initial test set by identifying and saving only the vectors which detect a fault.

4.1. Fault-free models definition

Fault-free descriptions are simulated with predefined input vectors. These descriptions provide simulation results which

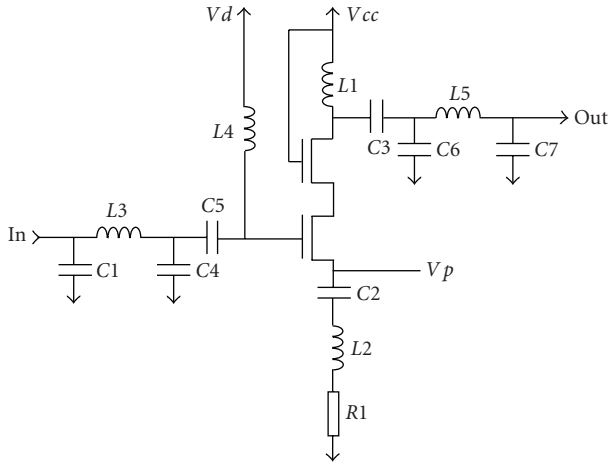

Figure 3: Structural model of LNA.

are "good" measurement values and which allow us to define fault-free measurement ranges. The comparisons with faulty circuits results are only possible thanks to these fault-free measurement ranges. Fault-free descriptions are defined as descriptions with parameters values within the specification ranges. Most popular methods to define a fault-free population sample are: Monte Carlo (MC) analysis and worst-cases combinations [6–8]. In our case, fault-free circuits simulations are performed using MC analysis and the statistical distributions of each behavioral parameter. For example, these distributions can be known by MC of transistor-level macrocomponents. We do not take into account correlations between two or more parameters. The number of fault-free simulations is decreased by drawing fault-free models with a predefined statistical distributions and by computing the statistical characteristics (i.e., the average μ and the standard deviation σ) of each result. The number of fault-free simulated models is increased as long as μ and σ variations are not negligible. Finally, the fault-free measurement ranges are defined in order not to reject fault-free circuits so the limits are computed at 6σ.

4.2. Faulty models definition

In part II, the fault model has been defined as a variation of one parameter. The original abstraction level for which PLASMA has been developed is the behavioral level. Obviously other abstraction levels can be managed by PLASMA. In the following, we will show that the best results are achieved with the behavioral level. Mutants are generated by translating one parameter of the original description to a value outside of its specifications, but the definition of this faulty value is difficult. When this value is too close to specifications limits, the fault is hardly detectable because circuit robustness and simulator accuracy mask it. When this value is too far from the fault-free detection limits, the fault is easily detected but it is also less realistic and it could be detected by most of stimuli.

The detection limit of the faulty value is fixed by simulating successive faulty values. The first value is defined far from the specification limits (but within minimal and maximal admitted faulty value limits defined bellow), then a dichotomy algorithm allows PLASMA to determine the faulty detection limit. During the detection limit computation, we define a faulty circuits range ("Faulty circuits" grey area Figure 5). This range is made of faulty circuits that have a probability to appear. Out of this range, the fault is very infrequent. The maximal and minimal admitted faulty parameter values $P_{\max\_\text{fault}}$ and $P_{\min\_\text{fault}}$ are computed with tolerance ranges (minimal and maximal specified values): $P_{\max\_\text{fault}} = P_{\max} + 5(P_{\max} - P_{\text{typ}})$. The fault detection limit is computed for every mutated parameter and every qualified vector. Relative parameter coverage (RPC_{Pi}) qualifies this detection limit for the Pi parameter; RPC is defined in

$$\text{RPC}_{\text{Pi}} = 1 - \frac{P_{\text{fault}_{\text{Pi}}} - P_{\max_{\text{Pi}}}}{P_{\max\_\text{fault}_{\text{Pi}}} - P_{\max_{\text{Pi}}}}, \quad (1)$$

where $P_{\text{fault}_{\text{Pi}}}$ is the detection limit P_{lim} for the Pi parameter represented in Figure 5, $P_{\max\,\text{Pi}}$ the maximum limit of Pi specification ranges, and $P_{\max\_\text{fault}\text{Pi}}$ the maximal faulty value possible for Pi.

When the detection limit equals to the specification limit, then the RPC is 100%. The closer this detection limit is from the specification limits, the higher is the RPC. The test set optimization is realized by saving for each Pi the vector that leads to the highest RPC.

5. TEST SET OPTIMIZATION FOR WCDMA RX PART BASED ON FAULT SIMULATION DESCRIBED AT HIGH ABSTRACTION LEVEL

5.1. Generation of the initial test set

During the design of complex electrical systems, a verification plan must be defined. This plan defines how to validate the design. This plan leads to the definition of test benches. These test benches are made of vectors which aim to validate system within all configurations (Gain, Offset) and with different input signals characteristics (frequency, power). For example, these vectors or stimuli verify the values of the programmable gains, the IIP3, the IIP2, and so forth. Generally, this manually generated test set is assumed to be adapted to the complete verification of the specifications. The aim of PLASMA is to evaluate and to optimize this test set.

The validation test set is made of stimuli with single tone signals applied on the RF_{in} input and the RX LO_{in} input (Figure 1). Signals are defined by frequency, power, and phase. The stimuli are also made of control parameters: gains configuration controlled by digital registered inputs. In the following experimental results, a test set made of 98 manually proposed single tone vectors is evaluated. These test benches have been optimized with PLASMA.

5.2. WCDMA functional and behavioral faulty descriptions

Faulty descriptions of WCDMA receiver are defined as presented in part II. The number of faulty descriptions is

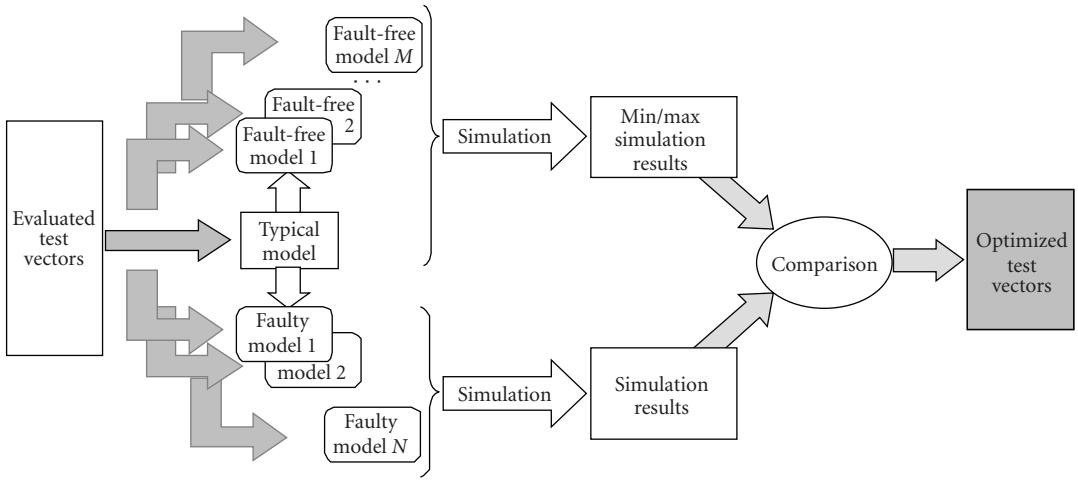

Figure 4: Test vector qualification & optimization.

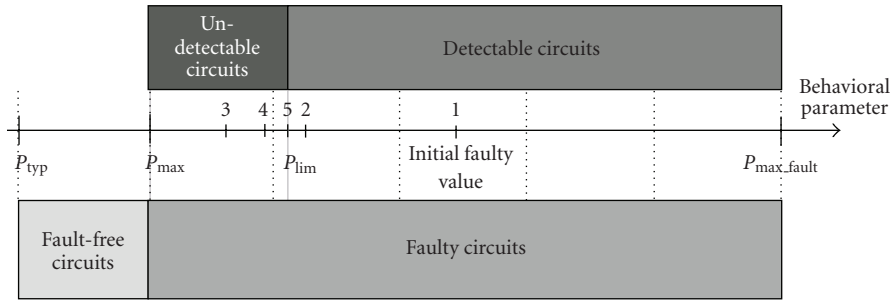

Figure 5: Definition of faulty value.

fixed by the number of parameters used in the original description. When one of these parameters is specified by two limits (e.g., the gain in Table 1), two mutants are generated on this parameter: a first one for the low limit and a second for the high limit; when it is specified by one limit (e.g.: IIP3), only one mutant is generated.

Due to this consideration, in a functional fault simulation approach, the receiver part of WCDMA SoC is modeled by 12 functional parameters (Gains and cutoff frequencies); it involves the generation of 24 faulty models. Behavioral description made of 23 behavioral parameters implies the generation of 36 behavioral faulty models because a few parameters are defined by only one limit.

5.3. Optimization results

The simulation has been realized with ADMS RF from Mentor Graphics on a 3 GHz Pentium-4, with 1 GB RAM, running a Linux operating system.

98 validation vectors have been optimized with our PLASMA tool. A first compaction is performed with the functional description and a second with the behavioral description (Table 2).

Over 24 functional mutated parameters, 18 have been detected by the 98 validation vectors during the entire dichotomy process. Then, the mutation score is 75% and the total computation time is about 11 hours 46 minutes. With the functional description, the average RPC computed with all functional parameters equals 65.6%. Each vector of the 98 initial test vectors detects at least one functional faulty parameter but after compaction, only 2 vectors are kept to achieve the same RPC. Hence, the number of predefined stimuli can be divided by 49.

During the optimization with the behavioral description, 92 vectors (out of 98) are qualified as redundant vectors because they do not increase the final RPC value (87.8%). The simulation time needed to perform this optimization at the behavioral level is 17 hours 39 minutes. The behavioral faults which have not been detected concern the variations

Table 2: Compaction, MS, average RPC, and simulation time comparison.

	Functional fault model	Behavioral fault model
Compaction rate	2/98 ⇒ 49x	4/98 ⇒ 24.5x
Mutation score	18/24 = 0.75	32/36 = 0.89
Relative parametric coverage	65.6%	87.8%
Simulation time	11 h 46 min	17 h 39 min

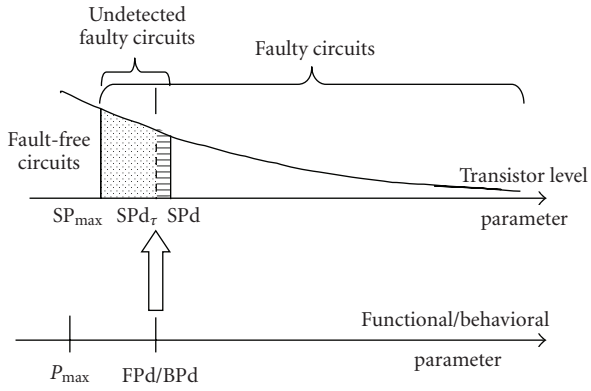

Figure 6: Detection limit of structural parameter.

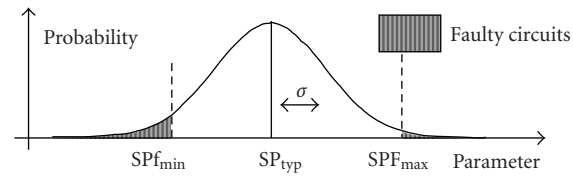

Figure 7: Capability process definition.

of S22, or IIP3 parameters. S22 variation is not detected due to the system robustness which masks its impact. In addition, our test vectors which only consist of single tone signals are not relevant for the detection of the IIP3 mutation. IIP3 mutants could be detected by a test set adapted to their activation and propagation in the system.

We observe that the simulation of our predefined test set at the behavioral abstraction level involves a high value of the average RPC. In addition, the comparison between functional and behavioral simulations shows that at the behavioral level simulation time is increased by about 50%. Now, we want to qualify and to compare, at the transistor level, these two optimized sets of test vectors.

6. EVALUATION OF FUNCTIONAL AND BEHAVIORAL FAULT MODELING FOR MANUFACTURING TEST

6.1. Principle of fault modeling evaluation

In the previous part, the results of the validation test set optimization have been shown, the efficiency of this optimization for manufacturing test is evaluated in this part. The advantage of our optimization technique based on high-level faults injection is the time reduction to qualify system test vectors; but is this fault modeling efficient for manufacturing test? The evaluation will be provided by making a comparison with a fault model described at a lower abstraction level: the transistor fault model. In the next section, the first analyzed high abstraction level is the functional level and then the behavioral level is analyzed.

The first stage of this evaluation is the computation of the *structural faulty parameter detection limit* (SPd) (Figure 6). This value is the limit that would be obtained if a transistor faulty description was used; we assume that it is the reference. SPd is computed with our PLASMA tool using a transistor-level description of the LNA only. In fact, in order to decrease the simulation time, only LNA is described at this transistor level (the other blocs are described at the behavioral level). Moreover, we only simulate compacted test set determined in Section 5.2.

The second stage of the evaluation is the comparison between structural and high-level faulty parameter detection limits. This comparison is only possible if the two detection limits are given at the same abstraction level. Thus, the *functional faulty parameter detection limit* (*FPd*) and the *behavioral faulty parameter detection limit* (*BPd*) computed during the optimization (Section 5.2) must be translated to structural parameter detection limits (SPD$_T$) (Figure 6). The conversion is performed by simulating each macrocomponent at the transistor level. In our case, this evaluation is only performed on the LNA. Thus, several test benches are used to measure the LNA functional parameters (Gain) or behavioral parameters (S11, IP1, etc.). The detection limits of high-level parameters FPd and BPd are converted to structural level SPd$_T$ by determining the single parametric deviation that involves at least one high-level parameter going out of its detection limits. But the comparison between SPd and SPd$_T$ is not enough because the same error between two different parameters has not the same impact on the final test quality. Thus, instead of comparing SPd and SPd$_T$, our high-level testing approach will be evaluated by comparing the number of undetected faulty circuits estimated with our approach with the number of undetected faulty circuits induced with transistor-level fault model.

During the design of system, engineers can estimate the distribution of parameters values. The capability process (CPk) (2) is a statistical parameter that allows designers to qualify the robustness of the structural parameters according to both the process and the device specifications. Parameters are assumed to have a Gaussian distribution and the CPk is defined by

$$\mathrm{CPk} = \frac{\mathrm{Min}\left((\mathrm{SP_{typ}} - \mathrm{SPf_{min}}); (\mathrm{SPf_{max}} - \mathrm{SP_{typ}})\right)}{3\sigma}, \quad (2)$$

where SP$_{typ}$ is the typical value of a parameter defined in the specifications, SPf$_{max}$ and SPf$_{min}$ are specified limit values, σ is the standard deviation (Figure 7).

The probability to produce a faulty circuit (hatched area) can be computed with the CPk values. Some faulty circuits are not detected (the darkest area in Figure 5) by the test vectors. These undetected circuits are present due to the system robustness, the measuring device accuracy or due to stimuli not adapted to the detection. Obviously, we aim to decrease this undetected number by finding the most relevant stimuli. In our case, the SPd value for each transistor parameter involves mutants which are not detected with the optimized test set. The number of these mutants is represented by the union of dotted and hatched areas in Figure 6. The dotted area is the number of undetected mutants estimated with high abstraction level descriptions. The hatched area (between SPd and SPd$_T$) represents the

Table 3: Structural parameter detection limits (SPds) computed.

	Structural specifications				Evaluation at structural level		Evaluation at functional level			Evaluation at behavioral level		
	Structural parameter	Typical value	Limit value	Faulty circuits (PPM)	Detection limit of structural parameter SPd	Undetected faulty circuits with SPd (PPM)	Detection limit of translated functional parameter SPd_T	Undetected faulty circuits with SPd_T (PPM)	Error of undetected faulty circuits (%)	Detection limit of translated behavioral parameter SPd_T	Undetected faulty circuits with SPdt (PPM)	Error of undetected faulty circuits (%)
Resistance (Ω)	*R*1 Max	2,500*E*+00	3,250*E*+00	7,944*E*−01	3,254*E*+00	8,791*E*−02	X	7,944*E*−01	88,93	3,253*E*+00	7,111*E*−02	2,12
Capacitor (F)	*C*3 Max	1,000*E*−12	1,100*E*−12	7,944*E*−01	1,100*E*−12	8,785*E*−02	X	7,944*E*−01	88,94	1,100*E*−12	7,099*E*−02	2,12
	*C*6 Max	1,400*E*−12	1,540*E*−12	7,944*E*−01	1,541*E*−12	8,794*E*−02	1,543*E*−12	3,220*E*−01	29,46	1,541*E*−12	7,111*E*−02	2,12
	*C*7 Max	1,000*E*−11	1,100*E*−11	7,944*E*−01	1,100*E*−11	8,802*E*−02	1,106*E*−11	6,324*E*−01	68,53	1,100*E*−11	7,116*E*−02	2,12
Inductor (H)	*L*1 Min	1,000*E*−06	9,500*E*−07	7,944*E*−01	9,498*E*−07	8,788*E*−02	1,149*E*−07	7,944*E*−01	88,94	9,498*E*−07	7,113*E*−02	2,11
	*L*1 Max	1,000*E*−06	1,050*E*−06	7,944*E*−01	1,050*E*−06	8,819*E*−02	X	7,944*E*−01	88,90	1,050*E*−06	7,099*E*−02	2,16
Transistor	LM_X2 Min	2,400*E*−07	2,360*E*−07	7,944*E*−01	2,360*E*−07	8,819*E*−02	X	7,944*E*−01	88,90	2,360*E*−07	7,143*E*−02	2,11
	LM_X2 Max	2,400*E*−07	2,567*E*−07	7,944*E*−01	2,568*E*−07	8,790*E*−02	3,663*E*−07	7,944*E*−01	88,93	2,567*E*−07	7,119*E*−02	2,10
	WF_X2 Min	1,000*E*−05	9,900*E*−06	7,944*E*−01	9,900*E*−06	8,802*E*−02	X	7,944*E*−01	88,92	9,900*E*−06	7,116*E*−02	2,12
	WF_X2 Max	1,000*E*−05	1,200*E*−05	7,944*E*−01	1,201*E*−05	8,793*E*−02	1,660*E*−05	7,944*E*−01	88,93	1,201*E*−05	7,108*E*−02	2,12

number of faulty circuits that are assumed to be detected with high-level qualification but which are not detected.

In the case of Figure 6, the high-level evaluation is a little bit too optimistic because a few circuits defined with high-level description as "detected faulty circuits" are not really detected (as shown with transistor fault model). This mistake is due to the fact that, in the high-level descriptions, the effects of parameters correlated variations are not modeled. In fact, our fault model is based on a single functional or behavioral variation but a modification of one structural fault leads to the variations of several high-level parameters.

6.2. Simulation results

Simulation results are presented in Table 3. The four first columns "(Structural specifications)" detail the specifications of the LNA transistor-level description: typical values, limit values, and the probability of occurrence of faulty circuits (computed with CPk).

Columns entitled "Evaluation at structural level" present the SPd values and the probability of undetected faulty circuits obtained during the analysis of WCDMA RX part with the LNA described at the transistor level and the other blocks described at the behavioral level. For all parameters, this number is equal to 0.088 PPM. This value is always the same because the number of faulty circuits is fixed by designers at 0.79 PPM for each parameter and faulty parameters are always detected during the 10 dichotomy loops. This number will be different if we use more dichotomy steps. This iteration number has not been increased because it is already close to the specified limit value (0.5% of the specified limit).

The other columns show the detection limits computed with high-level simulations and translated to the structural level (SPd_T). They are first obtained with the simulations of functional descriptions and then with behavioral level description. The errors made on the estimation of undetected faulty circuits computed with high abstraction level are presented on the grey columns. These values qualify the accuracy of using high-level descriptions.

The behavioral analysis shows that the SPd_T limits are very close to the SPd reference limits (ex: $R1$:SPd $= 3.254\,\Omega$ and $\mathrm{SPd}_T = 3.253\,\Omega$). Hence, the error on the estimation of the undetected faulty circuits is only 2%. With functional descriptions, results are really bad. For example, a variation of the resistance $R1$ does not lead to the modification of LNA Gain ($\mathrm{SPd}_T = X$). Therefore, the error made on the undetected faulty circuits estimation is far from undetected faulty circuits computed with structural simulations (88%). For the inductance $L1$, the variation involves a variation of the LNA gain ($\mathrm{SPd}_T = 11{,}5\,\mathrm{nH}$) but the value is very far from specification limit value that leads a number of detected circuits close to 0. Thus, the error on undetected faulty circuits is important (88%). In the best case ($C6$ capacitor), the error on the estimation is 29% but this error is again too high.

The errors achieved by functional fault simulations are too important. On the contrary, in our case study, errors involved in by behavioral simulations are acceptable. Therefore, we can conclude that behavioral fault modeling can be adapted to the qualification and the optimization of manufacturing test set. However, the efficiency of the behavioral model is directly linked to the accuracy of the original behavioral description which can vary through the verification plan definition.

7. CONCLUSION

In this paper, a test generator (PLASMA) has been presented and evaluated. In the proposed strategy, the validation test benches developed by designers to verify subblocs parameter specifications are reused. We show that reusing these test benches for the production testing is relevant. Generally the number of validation test benches is huge, so we propose to optimize them thanks to a high-level fault injection method. The optimization has been applied with functional and behavioral fault models. We assume that the detection of high abstraction level faults allows the detection of numerous physical defects. This assumption is verified by comparing simulation results generated with the high-level fault models and the transistor fault model. The metric used to evaluate our high level fault model accuracy is the number of un-detected faulty circuits. This metric qualifies the efficiency of the test stimuli. Results show that the numbers of undetected mutants is almost the same with a behavioral or a structural fault model but is different when we use functional fault model. These results have been obtained for the faults detection of an LNA embedded in a complete WCDMA receiver. In our case, the functional description is not adapted to the qualification of production test set. On the contrary, behavioral level description is interesting because it decreases test set qualification time and involves a good test set optimization.

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Research Article

A Tool for Single-Fault Diagnosis in Linear Analog Circuits with Tolerance Using the T-Vector Approach

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In previous works of these authors, a technique for doing single-fault diagnosis in linear analog circuits was developed. Under certain conditions, one of them assuming *nominal* values for the circuit parameters, it was shown that only two measurements taken on two selected circuit nodes, at a single frequency, were needed to detect and diagnose any parametric fault. In this paper, the practical value of the technique is improved by extending the application to the diagnosis of faults in circuits with parameters subject to *tolerance*. With this in mind, single parametric faults with several strengths are randomly injected in the circuit under study and, afterwards, these faults are diagnosed (or the diagnosis fails). Results are reported on a simple active filter. Conclusions are drawn about the robustness and effectiveness of the technique.

1. INTRODUCTION

The practical implementation of analog fault detection and diagnosis is a matter of importance, and many researchers are nowadays working on it. In recent papers, a technique for doing single-fault diagnosis in linear analog circuits was developed [1–3]. This technique presents several nice properties.

(i) It shows that fault diagnosis can theoretically be done with only two measurements (corresponding to two circuit variables) at a single frequency, in case where there are not any ambiguity sets in the circuit.
(ii) It allows to build fault dictionaries (FDs) where only one complex vector is needed to be stored for each circuit parameter and each test frequency.
(iii) In theory, a sufficient FD can be built with information gathered only at one single frequency.
(iv) The technique indicates how to reduce (if possible) the number of test points to a minimum of two. This is an important issue for industry application.

However, the technique has also several drawbacks:

(i) it applies only to linear circuits;
(ii) it applies only to single faults;
(iii) all the circuit parameters, except the faulty one, must have their nominal values.

This last disadvantage is the most important. In fact, in real circuits all parameters are subject to fluctuations due to the manufacturing process and aging, for instance, and there is a tolerance range where the real value of the component is.

Here, the application of the diagnosis technique to circuits where the components, such as resistors, capacitors, and amplifier gains, have random values located in a specified tolerance interval is reported. The study relies on simulations, and thus the effect of some real sources of errors (e.g., imprecision in the measurements) is not accounted for.

The paper is organized as follows. In the next two sections, we report briefly on relevant published results and present the theoretical support of the technique. Then, the procedure which tackles the tolerances and the tools developed for its implementation are presented. Finally, results

on the fault diagnosis of an active filter are reported and the practical applicability of the technique is discussed.

2. PREVIOUS WORK AND STATE-OF-THE-ART

The problem of *practical single-fault diagnosis under the assumption of element tolerances* is addressed in this paper. Under the hypothesis of "exact" parameter values it was shown before [1, 4] that two measurements, at a single frequency, done at two different test points properly chosen, could be sufficient to diagnose any fault. The necessary conditions and an algorithm for selecting the test points were presented.

In [3] a set of tools developed for evaluating the technique under the above "ideal" case was presented and its application was reported. In the present paper, we give an account of an extended set of tools that can cope with the existence of tolerances in the components, the "real" case.

In terms of fault diagnosis' techniques taxonomy [5], this one can be classified as a *simulation-before-test* (SBT) approach since the information for diagnosis *is stored before the circuit is tested*. It can also be classified as a *fault-dictionary* technique, as one set of vectors (T-vectors), independent of the fault value, is recorded before the test and is used in diagnosis.

The fault diagnosis problem has been addressed under many perspectives and according to several goals (e.g., fault detection or fault diagnosis) and problem formulation (e.g., single or multifrequency diagnosis, circuit parameters with or without tolerance, all or only some circuit variables available for measurement), not to mention the diversity of circuits themselves: linear, nonlinear, resistive, dynamic, analog, and mixed (or analog-digital). Recall that fault diagnosis in digital circuits is a mature discipline (see, e.g., [6–8]), quite self-contained, and independent of analog-fault diagnosis.

The problem of defining conditions under which a circuit is diagnosable has had many answers. When all the element values must be calculated (i.e., when multiple faults are allowed), usually several test points and test frequencies must be used. Seminal compilations of works on this issue are [9–13], and many more contributions are spread through circuits and systems journals and conference proceedings.

Some researchers tackled the fault-diagnosis problem in electronic circuits by using artificial intelligence (AI) techniques. For instance, [14] presents a matured methodology for model-based diagnosis of analog circuits using the constraint-logic programming approach. The modeling of the diagnosed circuit is generalized to arbitrary analog circuits consisting of linear elements (nonlinear circuits, such as diodes and operational amplifiers with output saturation, are included in the approach by doing the piecewise linearization of their characteristics). Both hard and parametric faults are considered in the diagnostic process. Fault situations with multiple-hard and single parametric faults can be diagnosed. An example, a 4-stage, eighth order, bandpass filter illustrates the approach.

The work from [15] is also based on AI. The detection and location of faults in analog circuits are done by checking that the measurements are consistent with the circuit function. The representation of information (component behavior and structure of the circuit) is unique (according to the authors) and accommodates the imprecise nature of analog circuits. A model of the circuit is formed from the constraints imposed by the behavior of the components and the interconnections. The values of the parameters within the circuit are deduced by propagating the effects of measurements through this model. Faults are implied from the detection of inconsistencies, and located by tentatively suspending constraints within the model.

In [16], is presented a quite original approach to circuit fault diagnosis of nonlinear electronic circuits. It consists in a branch-fault location (as opposed to node fault location) approach which requires a single excitation source at one test frequency. Branch diagnosis equations are constructed by modulating the bias of nonlinear devices in the network. The constraints on the bias equations and test frequency are addressed for a general network where q network elements are modulated or q bias transitions are used. A network element whose value is varied externally (i.e., by test equipment) is defined as a modulated element. The proposed technique has been applied to several examples consisting, mainly, in cascade amplifiers with bipolar transistors.

We now review some recent work relevant to the present article.

In [17], the selection of test nodes has been studied extensively and efficient techniques, called inclusion methods and exclusion methods, were proposed. The order of computation of the methods depends linearly on the number of test nodes. It is also proportional to $f \log f$ where "f" is the number of faults. The concept of "minimal set of test nodes", a novelty in analog circuit fault diagnosis, was defined. Polynomial time algorithms were proposed for the first time to generate such sets. Note that the faults considered in the study were hard or catastrophic faults (shorts or opens), while our method, based on the "T-vectors", is appropriate for both hard and soft (or parametric) faults.

In [18], an efficient method to select an optimum set of test points for dictionary techniques in analog fault diagnosis was proposed. It is based on searching for the minimum of the entropy index attained with the available test points. The test point with the minimum entropy index is selected to construct the optimum set of test points. The method is polynomial bounded in terms of computational cost. The frequency used was 1000 Hz (note: we can use any number of test frequencies in our work). The faults under study were also catastrophic; in fact, they were the same used in [17].

In [19], were presented symbolic techniques for the selection of test frequencies in multifrequency parametric fault diagnosis of analog linear circuits. The proposed approach was based on the evaluation of the condition number and the norm of a sensitivity matrix of the circuit under test. The initial set of frequencies, from where the test frequencies were chosen, had values separated by octaves (heuristic choice).

3. FAULT SIMULATION EQUATIONS

The theoretical results in this work are a by-product of the technique used to assemble the equations that simulate

the circuit with a single fault. This technique was coined FARUBS (from "Fault Rubber Stamps") in [20], and has been used to build efficient fault simulators for nonlinear DC circuits [21, 22], for linear dynamic circuits in the time domain [23, 24] and for linear dynamic circuits in the frequency domain [25]. We briefly review the technique here, as it is the base for the diagnosis method discussed in the present work.

The circuit equations, which are assembled using modified nodal analysis (MNA) according to the "rubber stamps" methodology [26], are written as

$$\mathbf{Mx} = \mathbf{b}. \tag{1}$$

In most simulators, (including those we have developed) this linear system of equations is solved with triangular decomposition (or "LU decomposition") of the circuit matrix **M**; that is, after calculating a lower triangular matrix **L** and an upper triangular matrix **U** such that

$$\mathbf{M} = \mathbf{LU}, \tag{2}$$

then two triangular systems of equations are solved:

$$\begin{aligned} \mathbf{Ly} &= \mathbf{b} \quad (\text{to get } \mathbf{y}),\\ \mathbf{Ux} &= \mathbf{y}. \end{aligned} \tag{3}$$

The solution, **x**, consists of the node voltages and some currents in the circuit.

To simulate *single faults*, it was developed a fault-injection technique that reuses the above **M** matrix and joins to it an additional line $\boldsymbol{\ell}$ (representing a scalar equation) and an extra column **c** (corresponding to an extra variable ϕ, the *fault variable*). These additional line and column are placed in the bottom and in the right position, respectively, in the matrix of the faulty circuit, which is

$$\begin{bmatrix} \mathbf{M} & \mathbf{c} \\ \boldsymbol{\ell} & \alpha \end{bmatrix} \begin{bmatrix} \mathbf{x}_f \\ \phi \end{bmatrix} = \begin{bmatrix} \mathbf{b} \\ 0 \end{bmatrix}, \tag{4}$$

where α is a scalar that depends on the fault value. Note that the dimension of the faulty circuit matrix is equal to that of **M** plus one.

As **M** was already factorized during the simulation of the nominal circuit, and due to the special location of $\boldsymbol{\ell}$ and **c** in the faulty matrix, the LU factorization of the faulty system is

$$\begin{bmatrix} \mathbf{L} & \mathbf{0} \\ \mathbf{p} & \chi \end{bmatrix} \begin{bmatrix} \mathbf{U} & \mathbf{q} \\ \mathbf{0} & 1 \end{bmatrix} \begin{bmatrix} \mathbf{x}_f \\ \phi \end{bmatrix} = \begin{bmatrix} \mathbf{b} \\ 0 \end{bmatrix}. \tag{5}$$

Thus, only the vectors **p** and **q** and the scalar χ have to be calculated (or factorized), and two triangular systems have to be solved, to get the solution $\mathbf{x}_f$ of each faulty circuit. This approach is much faster to accomplish than doing the factorization of the complete faulty circuit matrix, and it allowed the authors to simulate faults efficiently in quite a variety of circuit types and analysis domains (nonlinear DC circuits, linear circuits in the time domain and in the frequency domain) [21, 23, 25].

```
#        DIAGNOSIS ALGORITHM
#
# Given T-vectors, the nominal circuit
#   output and the faulty circuit output

# Calculates coefficients of variation
#   for each element. The suffix 'r'
#   refers to 'real' and the suffix 'i'
#   refers to 'imaginary'
foreach test frequency f
  foreach element e
    foreach diagnosis variable v
        calculates phi(v)=delta(v)/t(v)
    end
    calculates av_phi_r(f,e),av_phi_i(f,e)
    calculates std_phi_r(f,e), std_phi_i(f,e)
    calculates
       cv_phi_r(f,e)=std_phi_r(f,e)/av_phi_r(f,e)
    calculates
       cv_phi_i(f,e)=std_phi_i(f,e)/av_phi_i(f,e)
    calculates
          cv_phi(f,e)=|cv_phi_r(f,e)|+|cv_phi_i(f,e)|
  end
end

# Gets cumulative coefficients of variation
#   for each element(integrates in test frequency)
foreach element e
  sumCV(e)=0
  foreach test frequency f
    sumCV(e)+=cv_phi(f,e)
  end
end

# Cumulative coefficients of variation sorted
foreach element e
  print sumCV.sorted
```

Figure 1

3.1. Mathematical results on testability and diagnosis

We now proceed with the development of the diagnosis equations, which are based on those previously presented.

Equation (4) can be recast as

$$\begin{aligned} \mathbf{Mx}_f + \mathbf{c}\phi &= \mathbf{b},\\ \boldsymbol{\ell}\mathbf{x}_f + \alpha\phi &= 0. \end{aligned} \tag{6}$$

From (1) it is known that $\mathbf{b} = \mathbf{Mx}$. Thus,

$$\begin{aligned} \mathbf{Mx}_f + \mathbf{c}\phi &= \mathbf{Mx},\\ \mathbf{M}(\mathbf{x} - \mathbf{x}_f) &= \mathbf{c}\phi,\\ \mathbf{x} - \mathbf{x}_f &= (\mathbf{M}^{-1}\mathbf{c})\phi,\\ \boldsymbol{\delta}_x &= (\mathbf{M}^{-1}\mathbf{c})\phi. \end{aligned} \tag{7}$$

The difference between the nominal and the faulty solutions, $\boldsymbol{\delta}_x = \mathbf{x} - \mathbf{x}_f$, is a very important quantity in the diagnosis technique.

```
OK: file sizes are equal! 47 47
FREQS:
100.0 :: 316.227766016838 :: 1000.0 ::
                3162.27766016838 :: 10000.0
VARS:
1 # 2 # 3 # 4 # VE # EK

### Phi Vectors ###      <<Phi(R3) and Phi(R2)>>
.................
Frequency 1000.0
.................
Element   R3
NaN
6.99580550958382e-005+6.20248991084592e-005i
6.70606691758615e-005+6.08430836547017e-005i
6.70606691758613e-005+6.08430836547016e-005i
6.99580550958388e-005+6.20248991084595e-005i
6.97232581572351e-005+6.35018149548326e-005i
Average real = 6.8752141340127e-005
Average imag = 6.18475560962309e-005
StDev real   = 3.0941363916074e-006
StDev imag   = 5.48714590589808e-007
CoefVar = 0.0538762681908556

Element   R2   <<NOTE EQUAL COMPONENTS OF Phi(R2)>>
NaN
0.00022015845533617+2.68568737830714e-005i
0.00022015845533617+2.68568737830715e-005i
0.00022015845533617+2.68568737830715e-005i
0.00022015845533617+2.68568737830715e-005i
0.00022015845533617+2.68568737830715e-005i
Average real = 0.00022015845533617
Average imag = 2.68568737830715e-005
StDev real   = 9.72765620492388e-019
StDev imag   = 1.62489092389066e-020
CoefVar = 5.02349813427531e-015
R2: FAULT DETECTED AT FREQUENCY 1000.0 WITH 5 VARS
.................
##### CoefVars Sorted #####

5.02349813427531e-015  R2  1000.0
1.22410483912364e-013  R2  316.227766016838
2.48632314663702e-013  R2  100.0
2.88584372227596e-013  R2  3162.27766016838
4.66725805913812e-012  R2  10000.0
0.0400848838576815  EK  1000.0
0.0534377155424465  C1  1000.0
0.0538762681908556  R3  1000.0
0.0606496874624565  C2  1000.0
0.230260703063673  R1  1000.0
0.39519074837353  EK  316.227766016838
.................
##### Cumulative Coefficients Sorted #####

R2 5.33190872807606e-012          <= FAULTY ELEMENT
R3 9.04248096927732
C2 9.1873349235148
C1 13.2305723964512
EK 34.1657723496047
R1 103.5795315601
```

Figure 2

ϕ is a complex scalar and $\mathbf{M}^{-1}\mathbf{c}$ is a complex column vector. We name it *the testability vector, or T-vector,* $\mathbf{t}$:

$$\mathbf{t} = \mathbf{M}^{-1}\mathbf{c}. \tag{8}$$

The testability vector is clearly associated to a specific circuit element. Recall that the connectivity vector $\mathbf{c}$ is used to insert the fault effect in the correct lines of the matrix. It contains the information about the position of the faulty element.

Finally, we can state that

$$\boldsymbol{\delta}_x = \phi\mathbf{t}, \tag{9}$$

that is, the difference vector $\boldsymbol{\delta}_x$ is related to the testability vector $\mathbf{t}$ through a multiplication by a complex scalar. This scalar, ϕ, is the fault variable (see (4)).

Recall that the equations are written in the complex domain. Multiplication of one complex vector by a complex scalar, say by $w = Ae^{j\theta}$, corresponds to rotate by an angle θ, and magnify by a quantity A all the complex (scalar) elements belonging to the vector. Thus, the relation between $\mathbf{t}$ and $\boldsymbol{\delta}_x$ is such that all the element-wise divisions of the corresponding elements of these vectors are equal to ϕ.

This fundamental observation is the basis of the diagnosis technique. To diagnose a circuit, given a circuit measurement taken at a known test frequency, ω_k, we calculate $\boldsymbol{\delta}_x$ and test it against all the T-vectors calculated at the same ω_k by performing the element-wise division of the vectors. The faulty element is the one corresponding to a T-vector where those divisions lead to the same value (or approximate values, as we will discuss in Section 4).

An example, with four variables, is shown in Figure 4. In this case, $\phi = 1e^{j90^\circ}$; thus all $dx_k \equiv \delta_{x_k}$ elements from $\boldsymbol{\delta}_x$ are obtained from the t_k elements by performing a rotation of 90° and without magnifying the amplitudes (as $|\phi| = 1$).

It is important to remember that all the equations developed so far assume a test frequency ω_k; for each test frequency new systems of equations (nominal and faulty) must be assembled and solved and, of course, the T-vectors also depend on the test frequency. A fault dictionary is assembled with the knowledge of the nominal circuit, the test frequencies, and the test variables (or observed variables).

4. THE DIAGNOSIS TOOLS

The set of tools developed for implementing the technique comprises several modules implemented in Ruby (http://www.ruby-lang.org/en):

(i) a custom, Spice-like, AC simulator: Bode diagrams are plotted with *gnuplot* (http://www.gnuplot.info) (an example is in Figure 6); the simulator optionally generates the T-vectors (option .tcalc);
(ii) a tool for detecting ambiguity sets in the circuit;
(iii) a tool for diagnosing faults;
(iv) a generator of random faulty circuits;
(v) several short scripts for gluing the above tools, plotting, doing batch simulations, and so on.

The detection of ambiguity was discussed in [3]. The presentation here is focusing instead on the fault-diagnosis procedures.

We begin by showing an example of diagnosis in the ideal case (a circuit having one faulty element, but where the remaining elements have their nominal values). Only after this preliminary example, the tolerance issue will be addressed.

It should be taken in mind that the final purpose of the experiments reported here is to gather data on how well

```
.....................
### Phi Vectors ###
.....................
Frequency 1000.0
.....................
Element   R3
NaN
4.11025876252038e-005+6.20529208644854e-005i
3.85275153793496e-005+6.09314693410627e-005i
3.72375111722833e-005+6.04160597588955e-005i
4.20532432359983e-005+6.22680832755847e-005i
4.09610982177306e-005+6.3261739896268e-005i
Average real = 3.99763911261131e-005
Average imag = 6.17860546272593e-005
StDev real   = 4.01895330008084e-006
StDev imag   = 5.63938060111311e-007
coefVar = 0.109660440302241

Element   R2
NaN
0.000163854504268449+6.57866075980587e-005i
0.000163217132362275+6.7381867889833e-005i
0.000159908292471298+6.8175220615005e-005i
0.000166000579325496+6.49259686482508e-005i
0.000164674557652282+6.55528845794772e-005i
Average real = 0.00016353101321596
Average imag = 6.63645098661249e-005
StDev real   = 4.55342990419006e-006
StDev imag   = 6.78960521560267e-007
coefVar = 0.038075219866987
.....................
##### CoefVars Sorted #####

0.038075219866987  R2  1000.0
0.0645184732681056  EK  1000.0
0.0693721726727367  C1  1000.0
0.109660440302241  R3  1000.0
0.143770473187838  R1  1000.0
0.173011441710792  C2  1000.0
0.577863242399773  R2  316.227766016838
0.652429840632239  R2  100.0
0.7933705619231  EK  316.227766016838
1.82429463961435  C1  316.227766016838
.....................
##### Cumulative Coefficients Sorted #####

R2 7.30067145232321
EK 9.64772701427247
C1 10.3314117573221
R3 13.7108644868272
C2 14.5143391019754
R1 21.8407476144575
```

Figure 3

parametric faults of several strengths are correctly diagnosed in circuits with elements subject to tolerances (the "real", practical, case). This will provide data about the robustness of the technique. The "ideal" fault diagnosis example has the objective of introducing the main ideas, and paves the way for the "real" fault diagnosis with tolerances presented afterwards.

4.1. Fault diagnosis with nominal component values

For diagnosing a fault there are available the nominal solution and the T-vectors, both calculated at the selected test

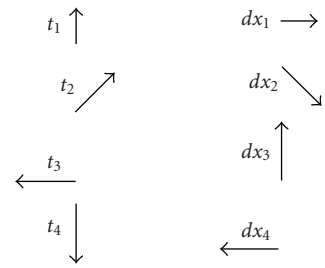

Figure 4: Relation between the difference of the nominal and the faulty solutions and the **t** vector. Note that all $dx_k \equiv \delta_{x_k}$ elements from $\boldsymbol{\delta}_x$ are obtained from the t_k elements by a magnification factor of 1 and a rotation of 90°, that is, $\boldsymbol{\delta}_x = 1e^{j90^\circ}\mathbf{t}$ and, thus, $\phi = 1e^{j90^\circ}$.

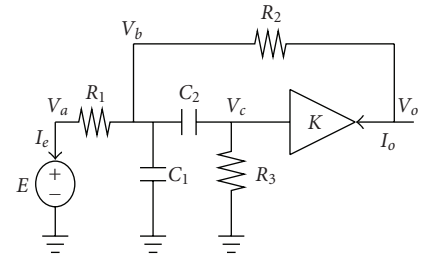

Figure 5: Sallen-Key bandpass section.

frequencies. The faulty circuit is simulated (this emulates the process of performing measurements in a real faulty circuit) and the output (i.e., the solution) is collected. The $\hat{\boldsymbol{\phi}}$ vectors are calculated from this data. (It should not be any confusion between ϕ, the scalar in the equations, and the vector $\hat{\boldsymbol{\phi}}$, whose elements are ϕ_k, which is calculated in the practical application of the technique. In the ideal circuit case, these ϕ_k are all equal and are also equal to ϕ when the T-vector corresponds to the faulty element; but in the real case, due to the tolerances, the ϕ_k are different among them and different from ϕ even when the T-vector corresponds to the faulty element.)

The diagnosis tool implements the algorithm described, in pseudocode, below. For each test frequency it calculates $\hat{\boldsymbol{\phi}}$ for each possible faulty element (i.e., evaluates the components $\phi_k = \delta_{x_k}/t_k$ of $\hat{\boldsymbol{\phi}}$, corresponding to the element-wise ratio defined by (9)) and also computes the average (av_phi), standard deviation (std_phi), and coefficient of variation (cv_phi) of the real and of the imaginary parts of the elements $\phi(v)$ of $\hat{\boldsymbol{\phi}}$. Then, by summing those coefficients of variation for all the test frequencies, the cumulative coefficients of variation for each element (sumCV(e)) are calculated and sorted: the lowest one indicates the *diagnosed* faulty element.

Parametric faults corresponding to ±5 times the allowed tolerance for the component are injected in the nominal circuit.

In this example it was inserted a specific fault in R_2 in the Sallen-Key bandpass filter (Figure 5). For simplicity we assume here that all circuit variables are measured.

When the circuit parameters are nominal except the faulty one (the "ideal" faulty circuit case), $\hat{\boldsymbol{\phi}}$ has its components, $\phi\_v = \delta\_v/t\_v$, all equal, at each frequency, only when

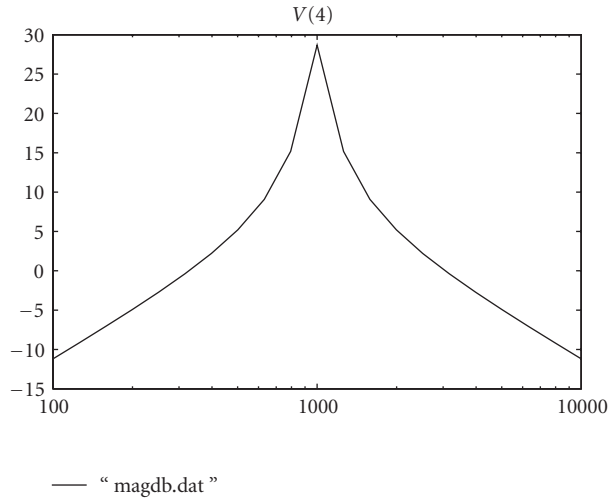

FIGURE 6: Bode magnitude plot of the Sallen-Key bandpass filter from Section 4, calculated with the custom AC simulator and plotted with *gnuplot*.

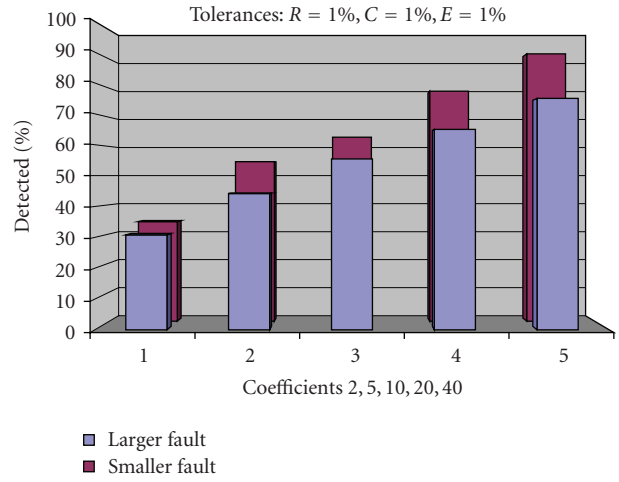

FIGURE 7: Percentage of fault detection for tolerances $\text{tol}_R = 1$, $\text{tol}_C = 1$, and $\text{tol}_{VCVS} = 1$ percent (data from Table 1).

"probing" the faulty element (i.e., when the T-vector in the division corresponds to it).

The coefficients of variation are ideally zero when probing the faulty element and not zero in the other cases. This is illustrated below (the complete output is truncated, and some comments were inserted in the listing): the cumulative coefficient of variation of R_2, 5.33×10^{-12}, is not zero due to rounding errors, but R_2 is correctly diagnosed as faulty.

The tool uses the database of T-vectors (*fault dictionary*), created when simulating the nominal circuit, and the simulation output file of the faulty circuit (which simulates the measurements).

The above report from the tool has the following information:

(i) the simulation frequencies;
(ii) a list with the circuit variables, where numbers are node voltages and VE and EK refer to the currents in the input source (VE) and in the controlled source (EK);
(iii) a list of the $\phi_k = \delta_{x_k}/t_k$ for each circuit parameter, here shown only for R_3 and R_2 at 1000 Hz;
(iv) the first value, $\phi_1 = \delta_{x_1}/t_1 = \text{NaN}$ (means "not a number"), corresponds to node 1, which is forced by the input source. Obviously this node is useless for diagnosis.

4.2. Diagnosis with circuit parameters subject to tolerance

When the parameters are subject to tolerance, there is not a "zero" cumulative coefficient of variation for the faulty element. We can expect, however, that the minimum cumulative coefficient corresponds to the faulty element.

The output below shows the results for a random circuit where the resistors have 1%, and the capacitors and the amplifier gain have 2% tolerance. The inserted fault was also in R_2. Notice that the components of $\hat{\phi}$, for R_2, are not all equal, as in the ideal case, although they show approximate values. However, the cumulative coefficient of variation is minimum for R_2 (although quite different from zero), which corresponds to a correct diagnosis.

5. ROBUSTNESS OF THE TECHNIQUE

A large set of experiments was conducted to check the robustness of the diagnosis tool under the effect of tolerances. Larger circuits are being investigated, but here we only present the results obtained from the Sallen-Key bandpass filter. The parameters of the experiment are the following.

(i) The circuit under diagnosis is shown in Figure 5. There are 6 parameters (R_1, R_2, R_3, C_1, C_2, and K) to be diagnosed in this circuit. This means that diagnosis "by chance" has $1/6 = 16.7\%$ probability of being correct (this value is the bottom line for comparing the values in Tables 1 and 2 and in Figures 7 and 8).
(ii) Six test frequencies are used, spanning (in a logarithmic scale) from 500 Hz to 5 KHz.
(iii) Each percentage of diagnosis, shown in Tables 1 and 2 and in Figures 7 and 8, was calculated from a sample of 500 circuits randomly generated (this means that 10000 circuits were simulated and diagnosed to gather the data).
(iv) Tables 1 and 2 are plotted in Figures 7 and 8. Although the information conveyed by them is the same, we feel that both representations are useful.
(v) It takes 0.36 seconds to generate, simulate, and diagnose one circuit sample.

The multiplier coefficient, MulCoef, defines the strength of the fault. The fault injected randomly is calculated as $P_F = P_0 \times (1 \pm \text{MulCoef} \times \text{tol}_P)$, where P_0 is the nominal value, P_F is the faulty value, and tol_P is the tolerance assigned to

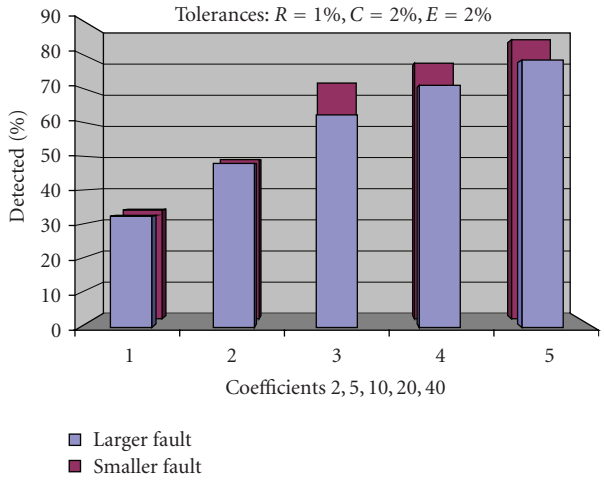

FIGURE 8: Percentage of fault detection for tolerances $\text{tol}_R = 1$, $\text{tol}_C = 2$, and $\text{tol}_{VCVS} = 2$ percent (data from Table 2).

TABLE 1: Percentage of fault detection for tolerances $\text{tol}_R = 1\%$, $\text{tol}_C = 1\%$, and $\text{tol}_{VCVS} = 1\%$.

MulCoef	Larger	Smaller
2	30.5	34.2
5	44.2	54.8
10	55.4	63.2
20	65	79
40	75	91.8

TABLE 2: Percentage of fault detection for tolerances $\text{tol}_R = 1\%$, $\text{tol}_C = 2\%$, and $\text{tol}_{VCVS} = 2\%$.

MulCoef	Larger	Smaller
2	32.4	33.6
5	47.8	49.2
10	62	72.8
20	65	79
40	78	86.2

the circuit element subject to the fault. The "+" signal in the definition of P_F leads to the column labeled *larger*; the "−" signal leads to the column labeled *smaller*.

5.1. Analysis of the results

There are some conclusions to be drawn from the analysis of Tables 1 and 2 (or from Figures 7 and 8).

First, there is a strong increase in the percentage of correct diagnosis when the strength of the fault increases. This is expected because with "harder" faults the solution of the faulty circuit goes away from the region of an "acceptable" value explained by the tolerances.

Second, for equal fault strength, the fault corresponding to a value smaller than the nominal is detected correctly more often than that corresponding to a value larger than the nominal. This can be seen in Figures 7 and 8 because the darker bars in the back of the plot, corresponding to the smaller fault values, are always taller than those in the front. We could not find a reasonable explanation for this observation.

Two sets of tolerances were studied (in one case, 1% for all components; in the other case, 2% for capacitors and for amplifier gains). A comparison between the corresponding plots does not reveal significant trends among them.

Finally, and recalling that diagnosing by chance in this example has an expected success rate of 1/6 = 16.7%, we can guess that the diagnosis of "light" faults is not robust by comparing the percentages in the first line in the tables, corresponding to MulCoef = 2, with 16.7%; these faults are almost inside the tolerance region.

6. CONCLUSION

In this paper are presented *the first diagnosis results with practical meaning* obtained with a tool built on top of a novel fault diagnosis technique which has been developed in the last few years.

It were presented an introduction and a review of the current state-of-the art on the subject of fault diagnosis, and the mathematical principles supporting the technique. Then, an extensive set of fault diagnosis results based on a Sallen-Key bandpass section was reported. It was seen that, when specifying common tolerance values, the likelihood of a correct diagnosis went from about 30% in the case where the fault was twice the maximum allowed tolerance ("light" fault) to about 80%–90% when the fault was 40 times that limit (almost an "hard" fault).

There are other issues of practical importance to be researched in the near future: the reduction on the number of diagnosis variables; the selection of effective test frequencies; the observation of the variation of the percentage of correct diagnosis with the type of the faulty element; the collection of statistics on the rank of the coefficients of variation of the faulty element (when it is not the first, is it the second, the third…?); and, obviously, the application of the technique to more complex circuits.

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Research Article

Built-in Test Enabled Diagnosis and Tuning of RF Transmitter Systems

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Built-In RF test is a challenging problem due to the need to measure the values of complex test specifications on-chip with the precision of external RF test equipment. BIT techniques are necessary for guiding system adaptation during field operation. Prior research has demonstrated that embedded RF sensors can generate significant information about RF circuit performance. In this paper, we propose a test methodology that enables efficient BIT and BIT-enabled tuning of RF systems. A test generation approach is developed that co-optimizes the applied test stimulus, the type of embedded sensors, and the system response capture mechanisms for maximal accuracy of the BIT procedure. This BIT technique is also used to perform diagnostic testing of the transmitter. The information gathered from diagnosis is used to tune the transmitter for improved performance. Simulation results demonstrate that BIT-assisted diagnosis and tuning can be performed with good accuracy using the proposed methodology.

1. INTRODUCTION

Wireless communications for both mobile and in-office (point-to-point communication) applications is undergoing a revolution due to the proliferation of different communication standards spanning diverse communication bandwidths. In addition, to the use of scaled CMOS technologies for high frequency wireless technologies running into the 10's of GHz (seemingly impossible till a few years ago) are posing daunting technological challenges both in design and manufacturing test. A complex multiband, multiradio system may integrate FM radio (100 MHz), RFID (13 MHz), Digital TV (800–1600 MHz), GPS (1.5 GHz), Bluetooth (2.4 GHz), Wi-Fi (2.4–5 GHz), 802.11 (2.4–5 GHz), Wi-Max (2.5–3.5 GHz), and UWB (3–10 GHz) using a combination of multiple RF transceivers and use of *software radio* design principles [1–3] using CMOS RF technology. This integration problem is made worse by the rapid deployment of scaled RF CMOS technologies in high-frequency RF transceivers. As the authors of [4] point out, individual scaled 90 nm CMOS transistors are unconditionally stable above 40 GHz. Hence, matching networks, feedback mechanisms, and loading networks must be designed very carefully to prevent oscillations in high-frequency circuits. In the future, higher speed circuits will be possible with scaled devices. However, the resulting circuits will be increasingly susceptible to manufacturing process variations and coupled noise from various on-chip sources. The former results in RF circuit nonidealities due to nonlinear behavior and mismatch effects. The latter is manifested as signal integrity problems due to

(i) power and ground bounce effects at the package level,
(ii) On-chip substrate coupling noise between digital and analog functions,
(iii) noise induced by electromagnetic radiation, and
(iv) transient errors.

Any combination of the above can degrade overall quality of service (QoS) and cause spectral content to spill over into adjacent communication channels. It is clear that future advanced scaled-CMOS RF front end modules will need to be carefully tested and calibrated to avoid these problems. In addition, to manage device degradation in the field, self-test and self-calibration capability must be designed into the transceiver itself.

In the past, there has been significant work in the area of built-in RF test using embedded sensors. The concept

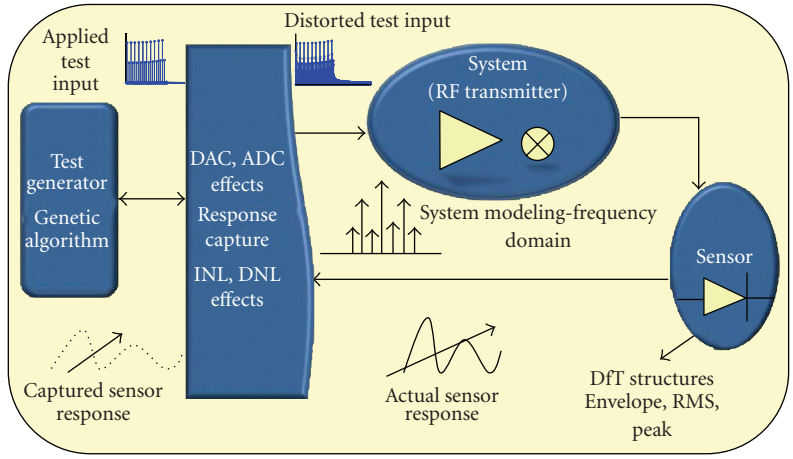

Figure 1: Building blocks of the proposed test simulator.

of *alternate test* has been used to derive compact low-cost test procedures [5–8]. Alternate tests make use of a compact stimulus to estimate multiple specifications of a system with high accuracy using a single data acquisition. The test is designed in such a way that the response of the device under test (DUT) to the applied stimulus is strongly correlated with the test specifications of the DUT of interest under random process variation effects. The procedure allows accurate diagnosis of the DUT's test specifications during field operation without the use of complex RF test instrumentation.

In this work, a formal built-in test methodology for RF systems is proposed that supports diagnosis and tuning of the same. The test framework uses special embedded RF sensors for test response data acquisition from different points of the RF signal path. The proposed methodology determines the *best stimulus to apply* (generated by software running on the transceiver DSP) and the *best embedded sensors* [9–11] *to use* (prior work focused only on one specific sensor type for an application) for high-quality parametric test and diagnosis.

The *impact of the data converters* specific to the RF transceiver being tested is considered in the design methodology. The best sensors to use are those that have the *least* impact on RF DUT performance, while generating the *maximum* amount of test information. The volume of data generated by each sensor and the resulting test time is also considered. Section 2 describes various modeling techniques that underline the design infrastructure. Section 2.4 describes the test generation algorithm that is used to generate a test stimulus that maximizes the test information that can be obtained from the DUT response. The generated test stimulus is stored in the system DSP and used to test the system periodically during system idle time. Section 2.5 presents built-in RF test-assisted diagnosis and tuning techniques that improve the performance of the transmitter. Section 3 presents simulation results for the BIT assisted diagnosis and performance tuning of an RF transmitter. Conclusions and future work are discussed in Section 4.

2. MODELING THE COMPONENTS OF THE RF TEST SIMULATOR

The key components of the RF test simulator are shown in Figure 1. The following are key BIT design goals.

(i) Accurate behavioral modeling of all the components of an RF transceiver (mixer, power amplifier, LNA, etc.). This is essential to developing a high-quality built-in test solution as use of behavioral models permits rapid simulation-driven test generation.

(ii) The applied tests are generated by an algorithm that *co-optimizes* the test stimulus, the on-chip test stimulus generation and response capture hardware (test access points, test response sensors) in such a way that the nonidealities of the hardware (linearity, noise) are taken into consideration while searching for the "best" built-in test solution (combination of test stimulus, test access points, and sensors employed for built-in test).

2.1. Transmitter modeling

Although, transistor-level simulation of all the submodules yields high accuracy of simulation, long simulation times make this impractical. The primary objective of test generation is to determine the optimal set of test stimuli [12, 13] rather than to verify the functionality of the design.

As long as the behavioral modeling approximations preserve the relative "goodness" of one possible test stimulus versus another, it can be used for fast test generation with little loss in test accuracy as shown in [12, 13].

The underlying assumption is that the variations in specification data and measurement data follow the same statistical trend under behavioral parameter perturbations as they would for transistor level parameter perturbations. Figure 2 shows the modeling approach (similar to that proposed in [12, 13]) employed for the RF system—under-test.

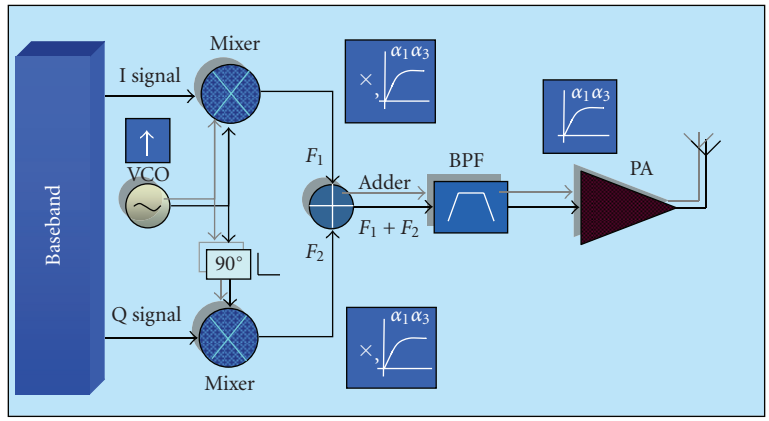

Figure 2: Block diagram of the behavioral model of an RF transmitter.

The behavioral model of each subblock was constructed as follows.

Filter: The transfer functions of the bandpass filters of the RF subsystem are realized as linear transfer functions with specified magnitude and phase characteristics.

Amplifiers: The amplifiers of the RF subsystem (e.g., LNA) are realized by implementing a nonlinear transfer function of the type

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t), \tag{1}$$

where α_0 = DC offset, α_1 = small signal gain, α_2, α_3 = nonlinearity coefficients.

The coefficients are "fitted" to the specified linear (gain) and nonlinear (harmonics and intermodulation terms) effects of the amplifiers concerned. Using the time domain input versus output characteristic as given by (1), the corresponding output frequency spectrum (both magnitude and phase) is computed. In general, the computation complexity is $O(N^3)$, where N is the number of test tones used for test generation/simulation.

Mixers: Mixers are modeled as nonlinear transfer functions followed by an ideal multiplier. The nonlinear transfer function is realized in the same manner as discussed earlier for amplifiers. The frequency mixing operation is realized by the multiplication operation

$$y(t) = C \times x_1(t) \times x_2(t), \tag{2}$$

where C represents the conversion gain of the mixer.

Oscillator: The peak amplitude value corresponds to the local oscillator frequency; the amplitudes adjacent to the frequencies fall off according to the phase-noise characteristics of the local oscillator.

In the above, the coefficients α_0, α_1, and so forth that are used to define the linearity of amplifiers are extracted from the input-output ($P_{\text{in}} - P_0$) relationship of the amplifier as determined by transistor level simulation via least squares polynomial fitting. Alternatively, they can also be extracted from the 1 dB compression point and IIP3 specifications of the amplifiers. The relationship between P1 dB and IIP3 can also be used to obtain the behavioral parameters of the subsystems. Equation (3) describes the modeling process mathematically;

$$\alpha_3 = \frac{P_0}{(P_{1\text{dB}}^2 P_{\text{in}}/0.145) + (3P_{\text{in}}/4)}, \qquad \alpha_1 = \frac{\alpha_3 P_{1\text{dB}}^2}{0.145}. \tag{3}$$

2.2. Modeling ADC/DAC nonlinearity

The nonlinearities of the ADCs/DACs used for data acquisition and stimulus generation (in production test systems) significantly affect the signal quality of both the applied test stimulus and the observed test response. The capture characteristics are modeled from the specified nonlinear characteristics of the PCI6115 data acquisition card (DAQ) used in the prototype test system. The PCI6115 is used as a low cost replacement for an ATE to transfer test data to the baseband processor (in our case, a PC). The INL and DNL characteristics obtained from the datasheets of the PCI6115 DAQ card are used to characterize the sourcing and digitizing properties of the data acquisition system used in this work. The frequency domain inputs and outputs of the developed digitizer model are shown in Figure 3. It can be observed that the signal quality of the test response is significantly affected by the nonlinearities of the sourcer/digitizer modules.

2.3. Modeling test response sensors

In this section, the modeling of three different types of test response sensors has been discussed.

2.3.1. Envelope detector sensor

The envelope detector employed is shown in Figure 4 and its uses as a test response sensor were first proposed by Han and Chatterjee in [14]. This is a common circuit for AM demodulation, composed of a diode, a resistor, and a capacitor. Through proper adjustment of the RC constant value, the requisite envelope detection can be performed. The value of the RC time constant should be such that

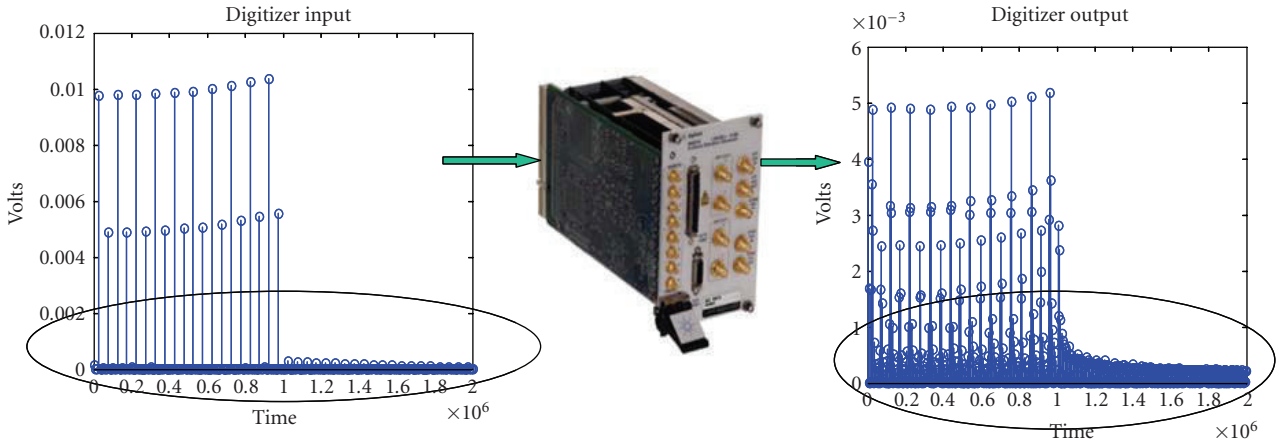

Figure 3: Test response before and after the digitizer module.

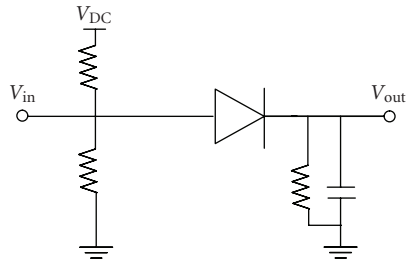

Figure 4: The schematic of the envelope detector.

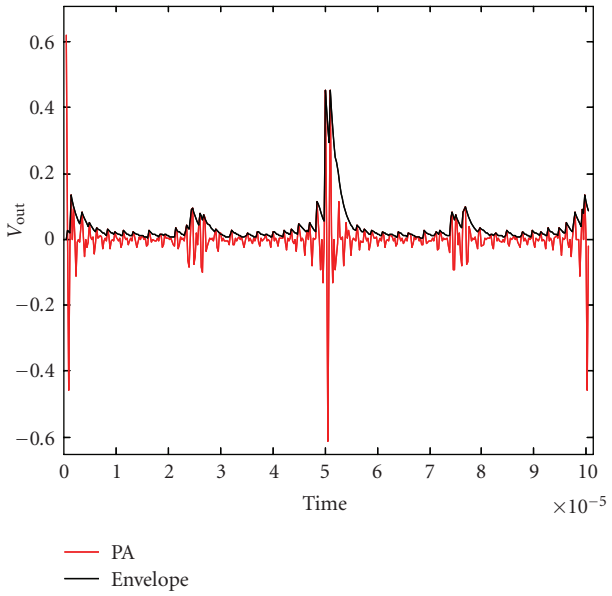

Figure 5: Envelope detector output.

$fo \ll 1/RC \ll fc$. This allows the circuit to track the low-frequency envelope of the RF signal. Considering that the above two frequencies have large separation, the RC time constant can be picked to make the decoded envelope immune to process variations.

A key consideration is the loading of the circuit under test (CUT) by the envelope detector. The input impedance of the envelope detector depends mainly on the bias resistors and the capacitance of the diode. The bias resistors are relatively large compared to the typical 50 Ohm RF matching impedance. During the normal operating mode, the power for the envelope detector can be turned off using a switch [14]. Hence, the diode behaves like an open switch. In general, the capacitance of a diode is several tens of farads. Therefore, the impedance (loading) of the envelope detector has negligible effect on the RF DUT performance. Figure 5 shows the transient output of the envelope detector showing that it follows the RF envelope. The observed output is a transient waveform and hence it has much more information compared to the o/p of RMS or peak detectors. However, this added information comes at the cost of having to process much more data than just single DC RMS or peak values.

2.3.2. *RMS detector sensor*

Figure 6 shows the RMS detector circuit [15] used as the test case in this research. Elements L1 and C1 form the matching network, providing a 50 Ohm match at 1.5 GHz.

The low value of S11 for this detector (<−45 dB) results in minimal loading of the RF system. R_2 is chosen so that the circuit provides the "true" RMS value of the input signal to the detector. Though it is debated in [16] that this does not achieve true RMS detection, the accuracy achieved is good for the purpose of this work.

The output of the detector for a multitone input stimulus is plotted in Figure 7 for four different specified combinations of input power levels. It is observed that both the DC value as well as the ripple voltage increases with the increase in input power level.

2.3.3. *Peak detector*

The conceptual diagram of a standard peak detector is shown in Figure 8. The biasing and matching circuits have not been shown for simplicity. The output is a DC voltage indicating

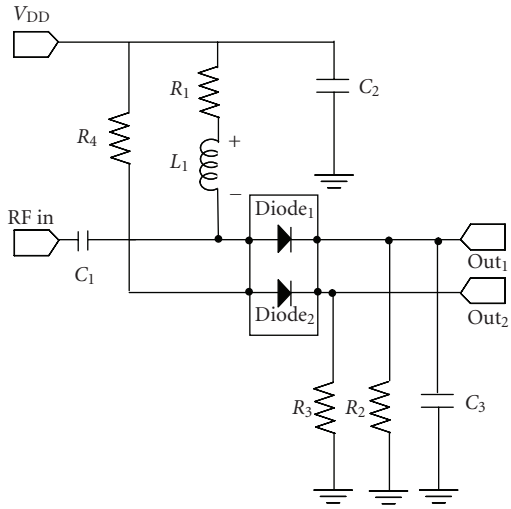

Figure 6: Schematic diagram of the RMS detector.

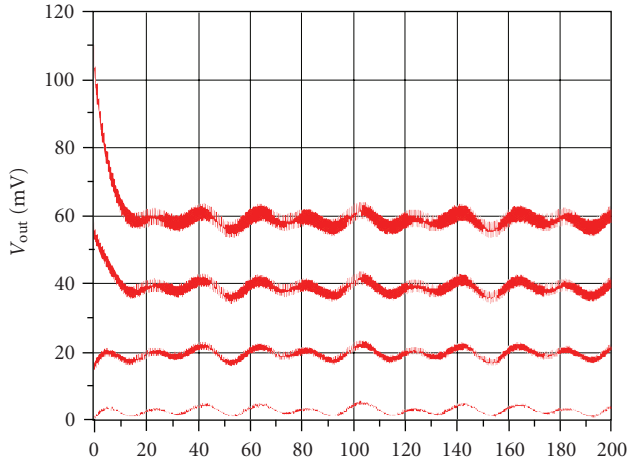

Figure 7: RMS detector output for different power levels of multitone input signal.

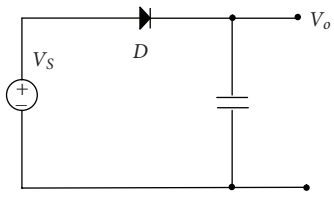

Figure 8: Conceptual diagram of the peak detector.

the peak of the applied voltage. As shown in Figure 8, the voltage V_o takes some time to reach its final value. This transient response is ignored and the final steady-state value is considered as the peak value.

Figure 9 shows the transient output voltage for different power levels of a multitone input signal. The voltage attains its steady-state level after a certain amount of time depending on the input power level. This information is used to model the peak detector.

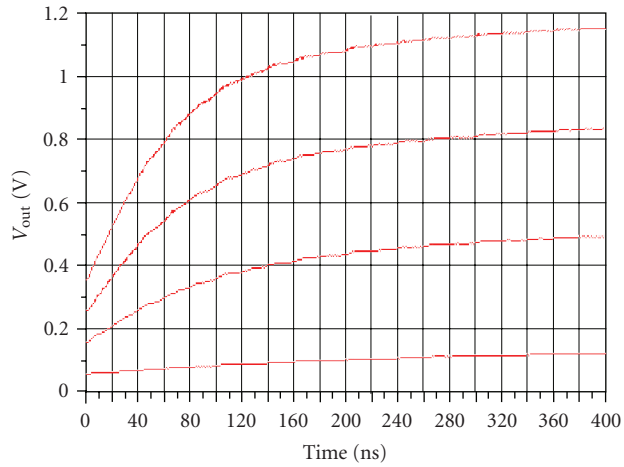

Figure 9: Transient response of the peak detector to multitone input signals of different power levels.

2.4. Test generation

Alternate test procedures have been extensively used in the past for analog/RF circuits to accurately predict specifications of interest. In this approach, regression functions such as those generated by MARS [8] are used to build a mapping function between the test response and the DUT specifications using a set of devices with random process variations called the *training set*. During the actual test, trained MARS models are used to predict the specifications of the DUT from the observed test response.

It should be noted here that a *defect filter* is used to screen out devices with catastrophic faults, and only the devices that "pass" the defect filter are considered for this study. This defect filter consists of simple algorithms that analyze the test response of the DUT to determine whether it has characteristics that are different from the "training set" of devices used to build the MARS regression model described earlier. The alternate test quality is highly correlated to the sensitivity of the observed measurement response to changes in the process parameters. For a given DUT, there are several test generation algorithms [17] available for optimizing the input test stimulus. In this work, a genetic algorithm-based test generator (as shown in Figure 10) is used due to the nonlinear nature of the search space to avoid local convergence. An optimized multitone test input is used as the test stimulus of choice. The multitone test stimulus is binary coded to result in a genetic individual of length 100 bits, with each tone represented by a 5 bit gene sequence.

Crossover and *mutation* are the two mechanisms by which a new generation of solutions is created [18]. Figure 11 shows an example case of crossover. In crossover, two parent genes are crossed over in an arbitrary fashion defined by the crossover probability to result in a completely new child. In mutation a single bit of the gene sequence is randomly mutated as determined by a mutation probability to result in a new child. These two mechanisms are responsible for the creation of new individuals which in-turn are assessed for their fitness. There is one another mechanism known as

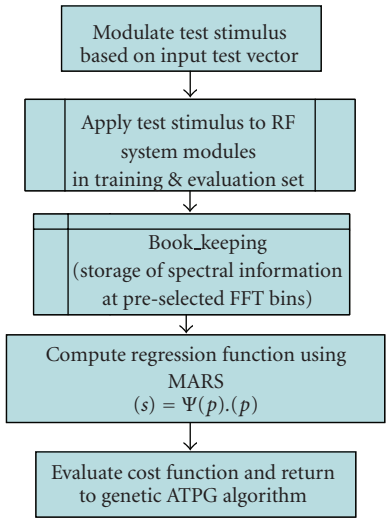

Figure 10: GA-based optimization routine.

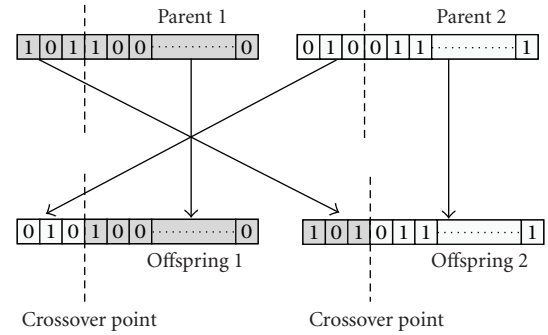

Figure 11: Single-point crossover operation for reproduction in the GA.

elitism in which genes with a particular fitness values are classified as *elite* and are passed on from one generation to another without any crossover or mutation. This ensures that a "minimum" fitness is passed on from one generation of solutions to another. Further insights into the algorithms can be found in [8].

The multitone test stimulus is a carefully crafted test stimulus with selected number of tones and varying amplitude levels. A set of 20 tones are uniformly deployed across a bandwidth of 1 MHz. The amplitude levels are allowed to have 32 (2^5) levels of variation ranging from −70 to 10 dBm. Thus, each tone can be coded into a 5 bit gene sequence to result in a 100 bit gene individual. This waveform is then converted to the frequency domain by means of the Fourier transform.

Figure 12 shows the frequency domain representation of two multitone signals with 20 component tones with coherent and noncoherent sampling. The wide-skirts observed in Figure 12 are the outcome of noncoherent sampling of the time domain waveform. Coherency is mathematically represented [19] as follows:

$$\frac{f_{\text{in}}}{f_s} = \frac{n_{\text{window}}}{n_{\text{record}}}, \tag{4}$$

where f_{in} is the input frequency of the multitone signal; f_s is the sampling frequency; n_{window} is the number of cycles of the signal that fits in a sampling window; and n_{record} is the number of data points in the FFT of the signal. The presence of unwanted tones in the test input degrades the test quality significantly. Hence, it is very critical that the multitone is coherently sampled. The genetically optimized waveform is then used to obtain the response of the component receivers. The subsystem specifications are computed by mapping the response to the subsystem specifications using nonlinear regression techniques.

The proposed test simulator as described above is used to evaluate different BIT alternatives. A set of candidate BIT solutions is first selected for evaluation. Each candidate consists of a set of sensors (envelope, rms, or peak) attached to a specified set of nodes (output of mixer or power amplifier). The test generation algorithm produces an optimized test stimulus for each BIT candidate. The BIT candidates are then ranked in order of the accuracy with which the test specifications of the RF DUT can be predicted from the observed test response. Since the hardware cost of each BIT solution is also known, the test designer can then pick the best solution from a cost versus accuracy perspective as desired by the test customer.

2.5. Built-in RF test-assisted diagnosis and tuning procedure

The BIT technique evaluated by the test simulator is used to drive diagnosis and tuning procedures for the RF transceiver. The diagnosis and tuning performed here restores the performance of the DUT in the presence of process variation induced performance degradation. Figure 13 describes the proposed approach. A built-in envelope tracking sensor (or other sensors as presented earlier) at the output of the transmitter is used to capture the transmitter response. The envelope detector consumes very little area overhead and is robust to process variations. The sensor captures the envelope of a multisine test stimulus, and "response features" extracted from this envelope are used to track the power and nonlinearity specifications (amplitude and phase distortion) of the power amplifier (PA). The transmitter can be tested during production testing, or while the system is idle (concurrent testing).

The captured response is a low-frequency signal that contains information about the linearity of the PA, is sampled, and fed to the baseband processor. The performance parameters of the transmitter are then predicted accurately from analysis of the obtained response envelope using nonlinear regression mapping functions built from calibration experiments.

The test stimulus is designed to exercise the nonlinearities of the PA. Optimized test stimuli is fed individually to I and Q channels to exercise PA non-linearity. When multiple nonidealities (I/Q mismatch, frequency offset) are present in the transmitter, a test stimulus optimization

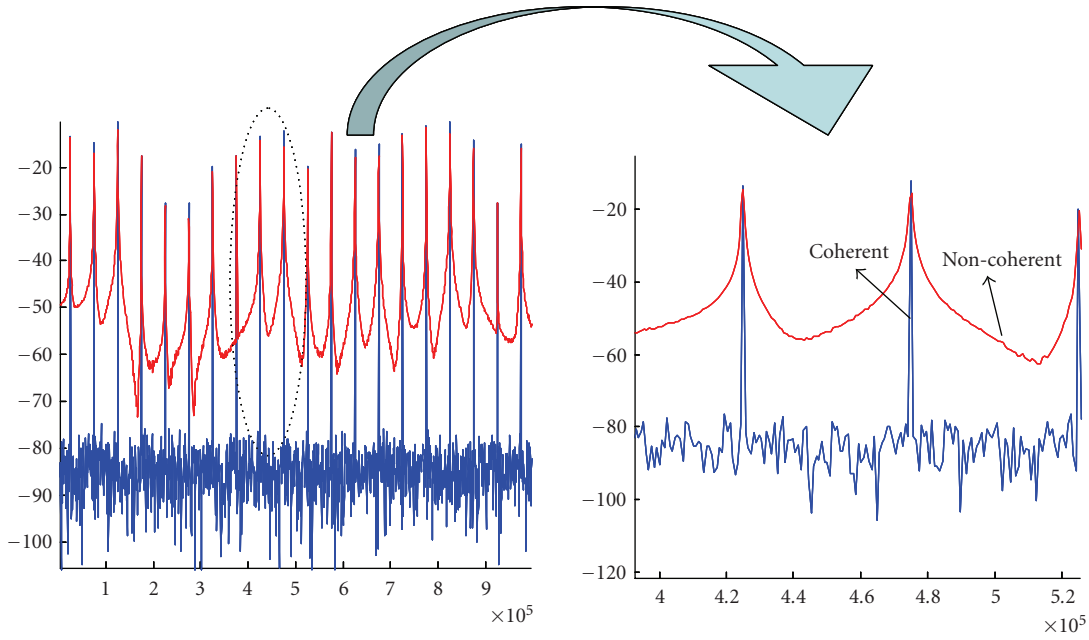

Figure 12: Coherently and noncoherently sampled response.

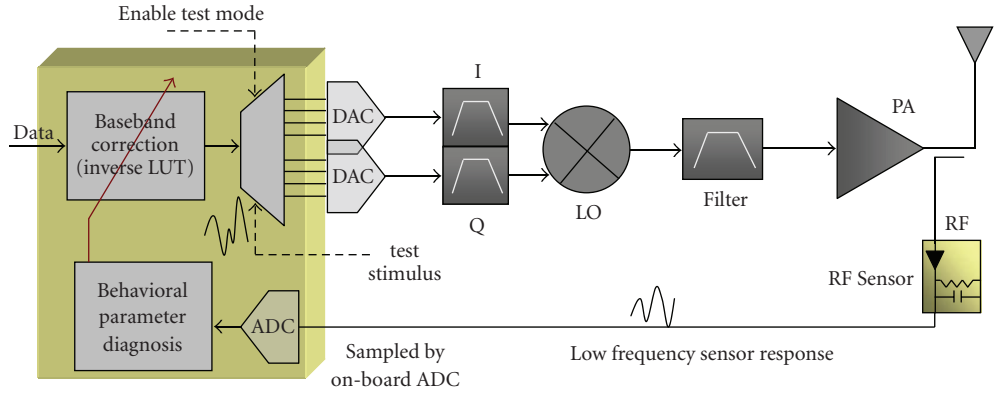

Figure 13: The proposed transmitter diagnostic testing and compensation approach.

algorithm is used to design the test stimulus to increase the accuracy of transmitter specification prediction from the obtained response. Using the captured "response features" of the transmitter, the behavioral performance parameters are predicted. After the PA nonlinearity is determined, an inverse function to the predicted PA transfer characteristics is computed to determine the predistortion coefficients (alpha values) and stored in a lookup table (LUT) in the DSP for correction (tuning). During real-time operation, the input signal to the transmitter instance is predistorted by the corresponding polynomial to tune out the effects of nonidealities present in the transmitter system.

3. VALIDATION OF THE PROPOSED METHODOLOGY

The proposed BIT design methodology has been validated on a wireless RF transmitter. The transmitter was modeled as described in Section 2. The proposed test simulator was implemented in Matlab.

3.1. BIT evaluation

The test simulator allows evaluation of different choices of test access points (nodes at which test response sensors are inserted) and test response sensors, while taking into account the nonlinearity and noise of the on-chip test response data acquisition and stimulus generation hardware. Optimized tests are generated for each such test configuration using the genetic algorithm-based test generator described earlier and the "best" test configuration (the one that allows the specifications of the DUT to be predicted from the test response with the highest accuracy with minimal hardware cost) is used for on-chip BIT.

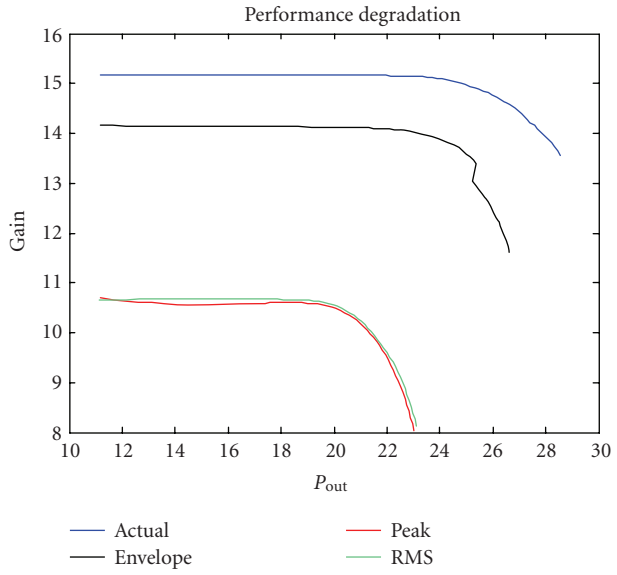

Figure 14: Performance degradation of the power amplifier for three types of sensors.

Table 1: Performance degradation of the power amplifier at 15 dBm output power level.

Component	Actual	Envelope	Peak	RMS
PA	15.16	14.14	10.58	10.64

Table 2: Evaluation of the test quality for three types of DfT solution.

Error type	Envelope	Peak	RMS
Rms_error	0.1475	0.2	0.21

3.1.1. Impact of test response sensors on performance of transmitter

For simplicity, the sensors were deployed only at the output of the power amplifier of the RF transmitter. The performance degradation simulation was performed using Agilent Advanced Design System (ADS). The performance degradation plots in terms of the operating *gain* of the transmitter are shown in Figure 14. The results are quantified numerically in Table 1 for a specified level output power level of the transmitter.

It is observed that the envelope detector provides the least performance degradation of 1 dB at an output power of 15 dBm.

3.1.2. Impact of test response sensors on test quality

The quality of the alternate test procedure employed was determined by the accuracy with which the specifications of the DUT could be predicted from the obtained BIT response. The rms prediction error over a large number of sample DUTs was used to quantify the quality of the BIT technique. This is shown in Table 2.

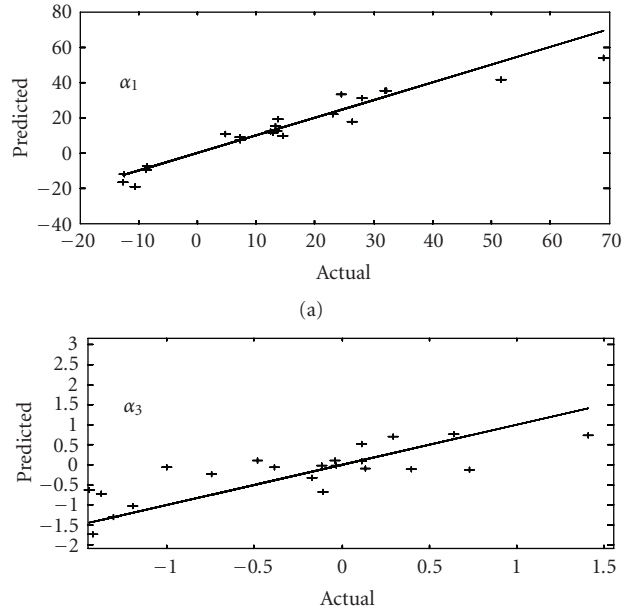

Figure 15: Diagnostic parameter estimation for the evaluated BIT technique.

3.1.3. Sensor selection

In general, the BIT solution that provides the least amount of performance degradation while providing acceptable accuracy of specification prediction from the test response is chosen as the final test solution. The envelope detection sensor attached to the output of the transmitter was found to have the best performance of the three sensors investigated in this work. It is important to note here that the developed tool has the capability to select the best possible DfT solution given an available set of sensors and their designs (e.g., there are many different ways in rms sensor can be designed). In the following, the recommended DfT solution is used to perform diagnostic testing and tuning of the RF transmitter.

3.1.4. BIT-assisted diagnosis of the RF transmitter

The best possible test input as generated by the test simulator for the recommended DfT solution is stored in the system DSP and is used to drive the BIT procedure from the DSP. The behavioral parameters α_1 and α_3 of (1) are used to characterize the transmitter's performance and are predicted from the obtained BIT response to the applied test stimulus. The developed BIT technique was evaluated on a set of 23 instances of the transmitter. The prediction plots of the diagnostic parameters for the transmitter are shown in Figure 15. As seen from the plots, the parameters are estimated with good accuracy.

3.1.5. Transmitter tuning

Once the polynomial of (1) corresponding to the transmitter is known, a lookup table based inverse correction

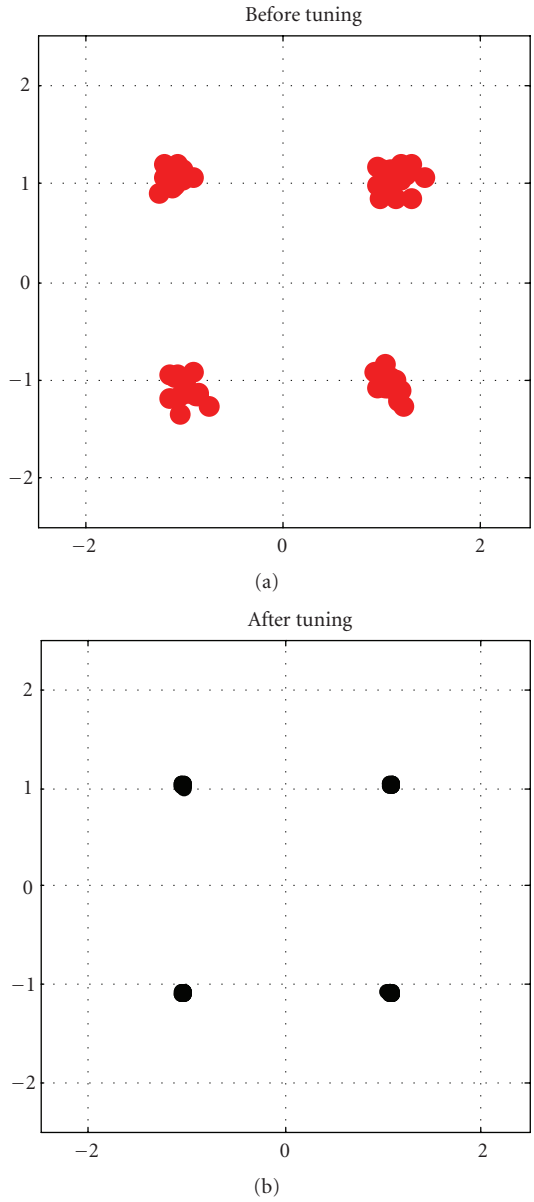

FIGURE 16: OFDM-QPSK constellation plots for a transmitter.

function that predistorts the input of the transmitter to compensate for its intrinsic nonlinearity is used to improve transmitter performance. To evaluate the effectiveness of the tuning procedure, the transmitter was interfaced with a baseband OFDM module and the system was simulated by transmitting QPSK modulated frames. Figure 16 shows the transmitted OFDM-QPSK constellation plots with and without digital predistortion. As observed from the plots, the nonlinear characteristics of the transmitter are compensated accurately (nonlinearity results in a "spread" of each of the four constellation points corresponding to OFDM-QPSK as observed in the left constellation diagram.

Currently, test quality along with the performance degradation of the sensor is used as the primary method for BIT sensor selection. In general, the dynamic range of the sensors, the volume of sensor data generated as well as the complexity of the sensor design and performance (sensor bandwidth and loading of the DUT) will need to be considered as well and can be incorporated easily into the test simulator.

4. CONCLUSION AND FUTURE

A methodology for optimizing built-in test infrastructure to diagnose and tune an RF transmitter is presented here. *The evaluated BIT technique* can *accurately diagnose the system performance parameters*. Also, a tuning procedure for digital predistortion is proposed that accurately compensates for system nonlinearities. These results justify the need to co-optimize the DfT structures along with the response capture characteristics to result in a highly accurate BIT. Current work is focused on extending the approach to a complete RF transceiver.

ACKNOWLEDGMENT

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Research Article

A Pull-in Based Test Mechanism for Device Diagnostic and Process Characterization

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A test technique for capacitive MEMS accelerometers and electrostatic microactuators, based on the measurement of pull-in voltages and resonance frequency, is described. Using this combination of measurements, one can estimate process-induced variations in the device layout dimensions as well as deviations from nominal value in material properties, which can be used either for testing or device diagnostics purposes. Measurements performed on fabricated devices confirm that the 250 nm overetch observed on SEM images can be correctly estimated using the proposed technique.

1. INTRODUCTION

The use of microsystems, containing sensors and actuators, in commercial products calls for simple and automated diagnostics and fault detection mechanisms.Despite the already wide use of these microsystems, their testing techniques tend to be complex and cost-intensive. If on one hand, the complex nature of microsystems, where multiple energy domains interact at the microlevel, imposes an additional level of difficulty, then on the other hand, the large number of fabrication processes available, each of them with their own unique characteristics, makes it difficult to have a process independent test mechanism.

Capacitive accelerometers are among the most commercially available microelectromechanical systems (MEMS), and several built-in self-test (BIST) schemes have been proposed to ensure high-reliability levels [1–4]. In [1], a simple functional test is performed. An electrical test signal is used to stimulate the device, and movement is detected. As this is a very simple functional test, it does not fully evaluates the device, making it unsuitable for more advanced tasks such as diagnostic and manufacturing tests. In [2–4], differential BIST approaches are presented. In [2, 3], the voltage that results from the self-testing operation is used as an indication of asymmetries between capacitors caused by fabrication defects or operational failures, while in [4] a dedicated test signal is applied, and the capacitive readout signal holds information of eventual asymmetries or defects occurring in the device.

A more recent approach [5] proposes the use of the current consumed during a pull-in transition to detect possible failures. Pull-in [6] is a unique feature of capacitive MEMS devices that can provide detailed information about their characteristics. Since the electrostatic force due to a field is inversely proportional to the square of the deflection, and the restoring force of the beam is, to a first approximation, linear with deflection, an unstable system results in case of a deflection, v, beyond a critical value, v_{crit}. The pull-in voltage, V_{pi}, is defined as the voltage that is required to obtain this critical deflection and depends mainly on dimensions, residual stress level, and design, which makes it ideal to characterize structural materials in surface micromachining processes [7, 8]. Unlike the case of the comb drive, which is based on area-varying capacitors, the design of most electrostatic actuators relies on gap-width varying capacitors, and the pull-in phenomenon has to be considered [9]. Pull-

in causes the displacement range due to electrostatic forces to be limited to 1/3 of the gap between the electrodes, in case of a motion perpendicular to the capacitor plate orientation.

In this paper, the use of the pull-in voltage as a test parameter is proposed. Furthermore, when pull-in voltage measurements are combined with the measurement of the resonance frequency (a single measurement is needed), the fabrication process nonidealities like overetching and process asymmetries can be estimated. Consecutive pull-in voltage measurements can be used to make accurate diagnostics as well as to perform electronic calibrations.

This paper is organized as follows. Section 2 introduces the pull-in voltage, and in Section 3 the details of the test mechanism are discussed. In Section 4, the test method is evaluated, and a discussion of the experimental results is performed. Finally, in Section 5 some conclusions are presented.

2. PULL-IN VOLTAGE

The simplest symmetric micromechanical system suitable for studying the pull-in voltage is composed of three electrodes, one movable and connected to a suspension beam with a certain spring constant k (see Figure 1(a)), and the other two fixed on a rigid supporting substrate. This is often the case of capacitive accelerometers, which have separate electrodes for sensing and actuation.

For a given applied voltage, global stable equilibrium in the microsystem under analysis occurs, if the second derivative of the potential energy of the system with respect to deflection is positive: $\partial^2 U_p/\partial x^2 > 0$. Thus, the pull-in voltage (V_{pi}) results from $\partial^2 U_p/\partial x^2 = 0$ and is determined by the beam material, the beam dimensions, residual stress, and the electrodes dimensions (electrostatic energy). The residual stress should not affect V_{pi}, and therefore the beam should be suspended using folded tethers at each end [10]. This approach ensures that the built-in strain energy component caused by longitudinal stress is negligible.

Due to the symmetry of the structure, three pull-in voltages can be defined as shown in Figure 1(a): asymmetric-right (V_{pr}), asymmetric-left (V_{pl}), and symmetric (V_{ps}). Assuming ideal conditions, analytical expressions for the three pull-in voltages can be found [6]:

$$V_{\text{pr}} = V_{\text{pl}} = \sqrt{\frac{8}{27}\frac{d_0^3 k}{\varepsilon_0 w l}},$$
$$V_{\text{ps}} = \sqrt{\frac{1}{2}\frac{d_0^3 k}{\varepsilon_0 w l}}, \quad (1)$$

where d_0 is the capacitor initial gap, k is the mechanical spring, $\varepsilon_0 = 8.8546 \times 10^{-12}$ is the air permittivity, and w and l are the capacitor plate width and length, respectively.

If nonideal process conditions are now considered (see Figure 1(b)) like overetching [11], capacitor gap mismatch, and Young's modulus (E) value deviations, the pull-in voltage values will vary, making them suitable to estimate the nonidealities and to be used as a diagnostic mechanism.

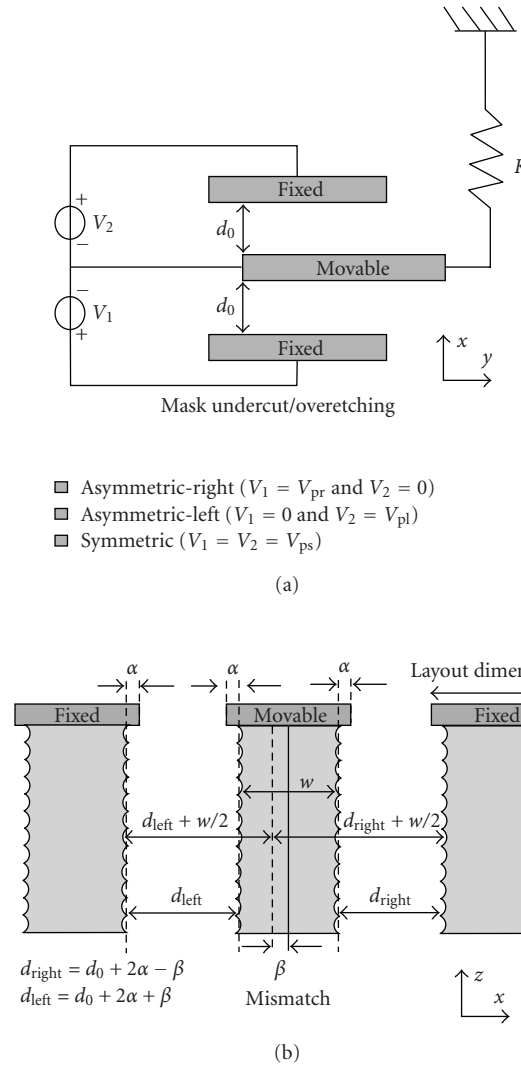

Figure 1: Sketch of the basic device with (a) ideal conditions and (b) with overetch and asymmetries.

3. TEST ALGORITHM

The pull-in phenomenon is an intrinsic property of actuated microelectromechanical systems, and therefore it can be used as a test mechanism. Fabricated devices often exhibit smaller dimensions than the actually designed ones (e.g., due to overetching). Overetching can be considered uniform along the microfabricated device [11], which means that all layout dimensions will be affected by the same parameter α. This will have a uniform effect on all three pull-in voltages. Small gap mismatches (a few nm) are also observed in fabricated devices. In this case, the gap mismatch (β) will affect differently the three pull-in voltages and consequently, it becomes easy to estimate β from the differences between V_{pl} and V_{pr}. The parameter α is more difficult to estimate, because there is an extra unknown parameter: the Young's modulus—its average bulk value is known, but it can show large deviations. If we introduce a new measurement, the

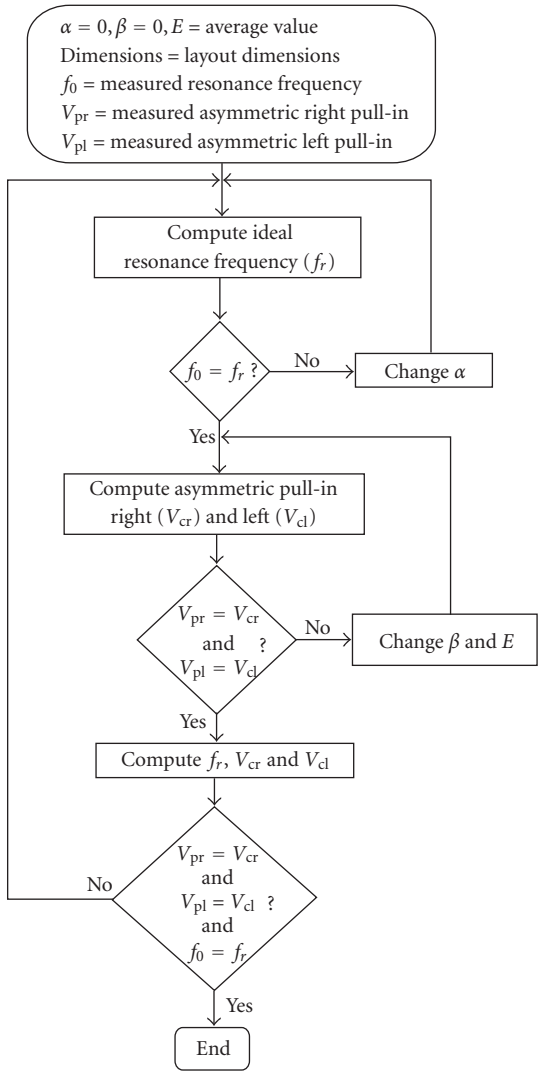

Figure 2: Flow chart to estimate α, β, and E from measurements.

resonance frequency, both α and E can be estimated, and a clear description of the mechanical device is achieved.

A flow chart of the proposed scheme is shown in Figure 2. After this initial estimation, the parameters susceptible of changing with aging and device operations are the Young's modulus and the gap mismatch [12], while the structure dimensions remain constant. This implies that consequent pull-in measurements are an excellent diagnostic parameter. Since the sensitivity of the device is known, test signals can also be applied to the actuation capacitors to calibrate the full system (device plus readout electronics).

One disadvantage of the proposed technique is that it relies on very accurate device models that can predict the device electromechanical behavior. These models have to incorporate all the nonidealities existing in the microdomain, like capacitor fringe fields and residual stress, which makes modeling one of the critical parts of the proposed test scheme.

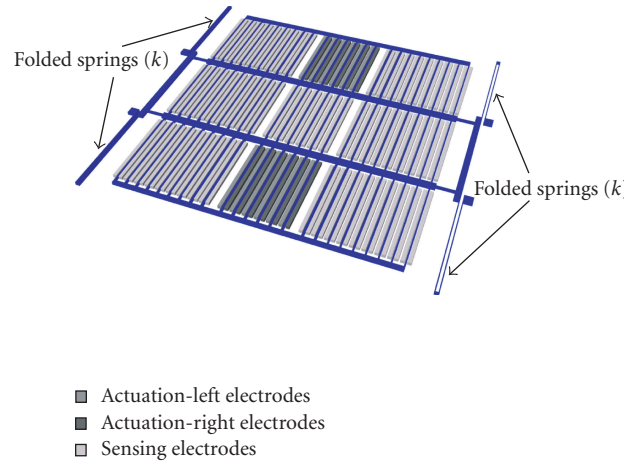

Figure 3: Drawing of the accelerometer.

4. EVALUATION OF THE METHOD

Accelerometers fabricated within the Bosch epipoly process [13] were used to evaluate the proposed test scheme. A drawing of the device being used is depicted in Figure 3. Several sets of electrodes are used for sensing while two sets of differential capacitors are used for actuation (left and right).

4.1. Mechanical domain

The mechanical spring of the structure is composed of 4 folded beams. Assuming that the trusses joining the folded-beam segments are rigid, an approximate analytical expression for k can be found [14]:

$$k(\alpha) = 4\frac{6EI}{(L+2\alpha)^3} = 2Eh\left(\frac{b-2\alpha}{L+2\alpha}\right)^3, \quad (2)$$

where $I = h(b-2\alpha)^3/12$ is the moment of inertia of the beams, E is the Young's modulus, α is the overetch parameter, and h, b, and L are the thickness, width and length, respectively, of each beam. A finite-element model (FEM) reveals that this expression overestimates in 4% the actual mechanical spring. This difference is not significant and can be explained by the fact that the analytical model does not consider the bending of the small beam joining the two beams of the folded beam topology.

4.2. Electrical domain

The device under study has 12 actuation capacitors. The total electrostatic energy can be written as (neglecting fringe fields):

$$U_{\text{elect}}(\alpha) = \frac{1}{2}12C(\alpha)V^2 = \frac{1}{2}12\varepsilon_0\frac{w(l-2\alpha)}{d+2\alpha}V^2, \quad (3)$$

where d is the capacitor gap distance, w (thickness of the mechanical layer) is the capacitor width, and l is the capacitor length. The analytical (3) does not take into account the

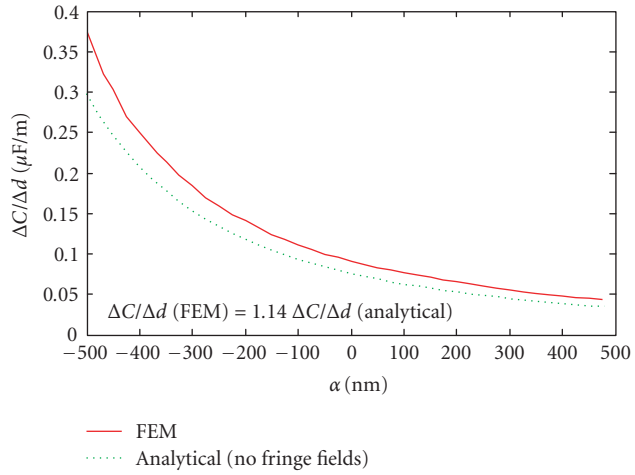

Figure 4: Comparison between FEM model and analytical models.

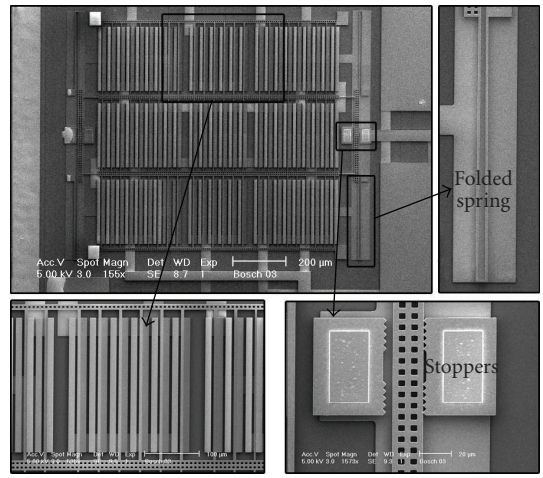

Figure 5: Fabricated device.

Table 1: Main nominal parameters of the device (layout dimensions and bulk material mean values).

Parameter	Value
Spring length (l)	340 μm
Spring width (b)	3 μm
Mechanical layer thickness (h)	10.6 μm
Capacitor length (l)	282 μm
Capacitor width (w)	10.6 μm
Capacitor gap (d)	2 μm
Young's modulus (E)	163 GPa (Poly-Si)
Density (ρ)	2.5 g cm^{-3}

effect of fringe fields, and since in electrostatically actuated MEMS these are very difficult to quantify, numerical methods (FEM) have been used instead. Capacitive FEM simulations for changing α were computed and compared with $(\partial C/\partial d)(\alpha)$. Comparative results are shown in Figure 4, and a small deviation between models can be noticed. The analytical model underestimates the effect of the fringe fields (about 14%). These results prove that fringe-fields contribute to the total electrostatic force and therefore cannot be neglected. The electrostatic force used for the computation of the pull-in voltages is

$$F_{\text{elect}} = 1.14\frac{\partial U_{\text{elect}}(\alpha)}{\partial d}. \quad (4)$$

4.3. Fabricated devices

The fabricated accelerometers (see Figure 5) are composed of four folded springs, 340 μm long and 3 μm wide (layout dimensions), connected to two rigid central bars of about 1 mm long. Parallel-plate capacitors with a 2-μm gap are used for actuation. The displacement measurement involves sensing the changes of various sets of differential capacitors. The main device layout parameters and bulk material properties are shown in Table 1.

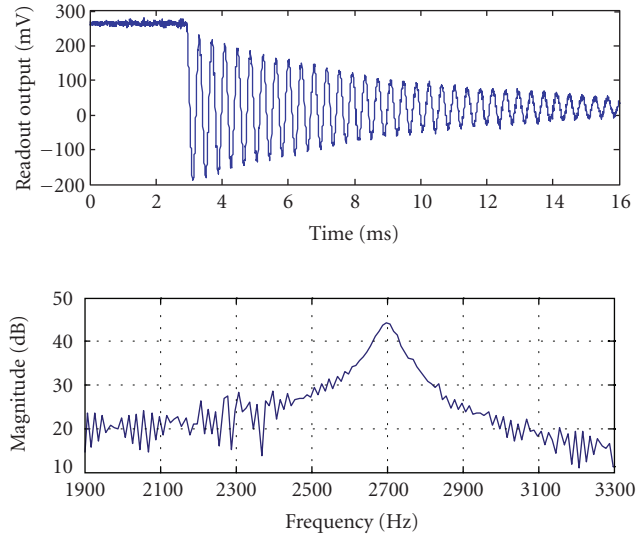

Figure 6: Resonance frequency measurements.

4.4. Experimental results

A batch of 16 devices, fabricated on the same run, was used in the experiments. The devices are encapsulated in vacuum which facilitates the measurement of the resonance frequency. The resonance frequency is determined by acquiring the devices free oscillations followed by a FFT (see Figure 6). The pull-in voltages are retrieved from displacement measurements (see Figure 7) performed while increasing the actuation voltage from zero until an abrupt change is detected. The voltage at which this abrupt change is detected corresponds to the pull-in voltage.

In case of nonfunctional devices, no displacement is observed when actuation voltages are applied. Stiction is detected in devices showing full displacement with no voltage applied.

The measured pull-in voltages showed large deviations (both for asymmetric and symmetric actuation) from device to device, while the deviations between resonance

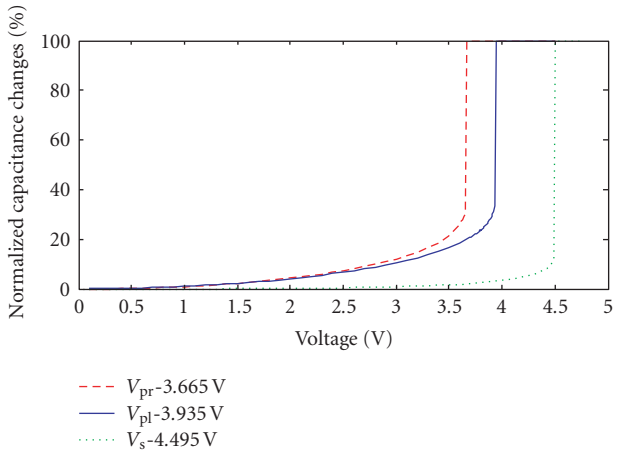

Figure 7: Pull-in measurements.

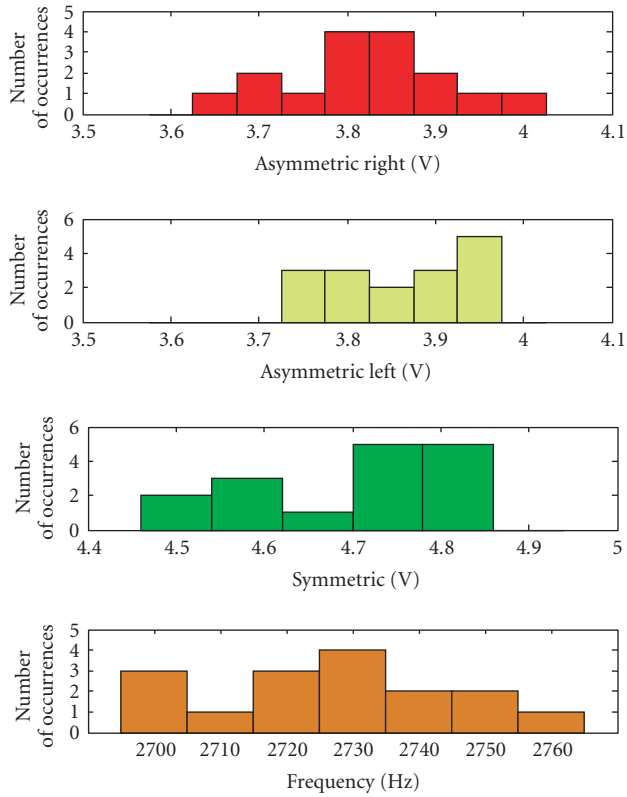

Figure 8: Histogram of the pull-in voltages and resonance frequency measurements.

frequencies were small (ranging from 2700 till 2760 Hz). The experimentally measured values for three of the devices are shown in Table 2. Figure 8 shows the histograms of several measurements that have been performed.

After applying the algorithm of Figure 2 to the set of values retrieved from the measurements, the parameters α, β, and E are estimated. The analytical expressions introduced in the previous subsections are used for the computation of the pull-in voltages. Table 3 presents the estimated values of α, β, Young's modulus, resonance frequency, and pull-in voltages

Table 2: Pull-in and resonance frequency measured values.

	Parameter	Value
Device 1	Asymmetric right-V_{pr}	3.665 V
	Asymmetric left-V_{pl}	3.935 V
	Symmetric-V_s	4.495 V
	Resonance frequency-f_0	2700 Hz
Device 2	Asymmetric right-V_{pr}	3.781 V
	Asymmetric left-V_{pl}	3.955 V
	Symmetric-V_s	4.70 V
	Resonance frequency-f_0	2730 Hz
Device 3	Asymmetric right-V_{pr}	3.751 V
	Asymmetric left-V_{pl}	3.911 V
	Symmetric-V_s	4.679 V
	Resonance frequency-f_0	2720 Hz

Table 3: Estimated α, β, and E values and simulated pull-in voltages and resonance frequency.

Device	α	β	E	
1	253 nm	60 nm	142.8 GPa	
2	257 nm	38 nm	148 GPa	
3	255 nm	35 nm	145.2 GPa	
Device	V_{pr}	V_{pl}	V_s	f_0
1	3.665 V	3.934 V	4.482 V	2700 Hz
2	3.782 V	3.956 V	4.693 V	2735 Hz
3	3.750 V	3.910 V	4.665 V	2716 Hz

regarding the devices whose measurements are shown in Table 2. Figure 9 shows the histograms of the estimated parameters from all the tested devices. The symmetric pull-in does not contribute with extra information but can be used to confirm the estimated values for α, β, and E.

4.5. Method verification

The values estimated from the measurements of the 16 devices are in very good agreement (α and E estimated values present a very low standard deviation), which was expected since they all were fabricated in the same run. However, it is interesting to notice that while the estimated values for α and E have a very low standard deviation, the estimated mismatch (β) values exhibit a large standard deviation. Since the deviations on the pull-in voltages are caused by gap mismatches (β) and these have influence on device performance, the correct mismatch estimation is one of the strong points of the proposed test approach. The observed mismatches have to do with lateral gradient stresses that often are neglected, or with overetch asymmetries that originate small deviations in the gaps.

In order to verify the estimated average values, some devices were observed using a scanning electron microscope (SEM). Two illustrative SEM images are shown in Figure 10. These SEM images reveal that the devices present an overetching very close to the average one obtained after the test method being proposed. This very good agreement

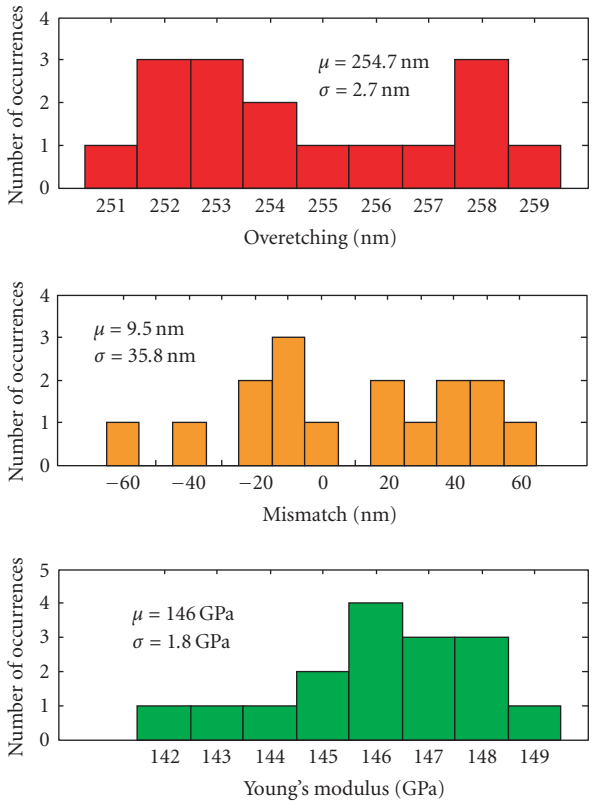

FIGURE 9: Histograms of estimated overetch, mismatch, and Young's modulus obtained from the tested devices.

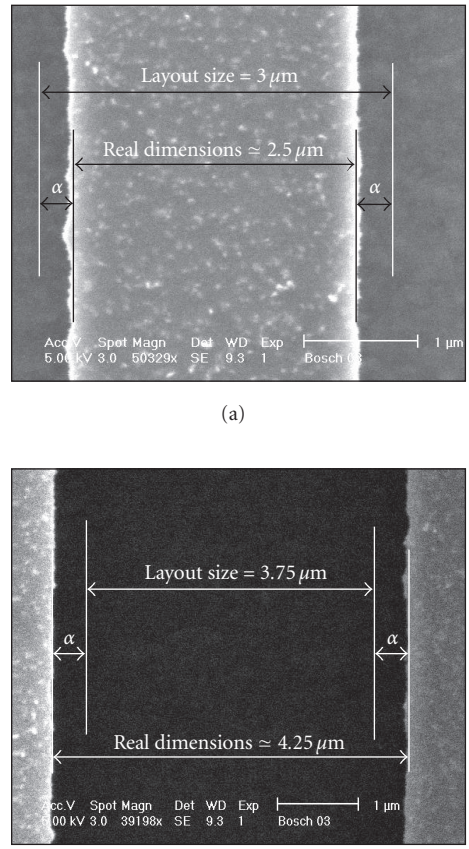

FIGURE 10: SEM photographs of (a) a folded beam and (b) capacitor gap at the stopper.

proves that pull-in voltage measurements can be used to accurately estimate process deviations and device performance.

4.6. Discussion

Like several other MEMS test techniques, the proposed test scheme uses a variable electrical signal to stimulate the device, and the device response can be used to obtain very important device information and most of all to obtain confidence on device functionality (a damaged device will present no pull-in behavior). So far, it has been shown that with this technique the device performance can be characterized but that is not enough to achieve a full BIST technique. Another important parameter in production is testing time. For the measurements presented in this paper, time was not an issue and the pull-in measurements ranged from several seconds to a few minutes (depending on the resolution of the increasing voltage steps used). The minimum achievable test time is directly connected to the dynamics of the device, that is, as the pull-in voltage assumes a quasistatic behavior, the time between steps must guarantee that the device gets to a stable state. Therefore, if a window of 200 mV is considered around the pull-in voltage (the actuation voltages does not start at zero but at a value close to the pull-in expected voltage), with a step resolution of 1 mV and a settling time below 10 milliseconds, a pull-in voltage measurement would require around 2 seconds.

In order to achieve a full BIST technique, on-chip test circuits must be integrated for generating the necessary electrical signals for actuating the device and analyzing the responses. A very simple diagnostic mechanism can be the storage of the initial pull-in voltages on-chip, so that they can be compared with consecutive pull-in voltage measurements. Pull-in voltage deviations from the original values can be used for diagnostic purposes. Before proposing an on-chip test method, long-term measurements must be performed to check and correlate known failure mechanisms with long-term pull-in deviations. First experimental results from the proposed test mechanism prove that the differences between expected pull-in voltages (using layout dimensions) and measured pull-in voltages can be explained from fabrication (overetch, gap mismatches, and Young's modulus deviations). We expect that long-term measurements will be able to give us information on device failures through shifts in the pull-in voltages, and it is likely that different failure modes will present different pull-in deviations in time.

Another advantage of this technique is the fact that it can be used to electrically calibrate an accelerometer. Normal accelerometer calibration (as an example we consider a ±1 g accelerometer) is done by applying a 1 g acceleration followed by a −1 g acceleration (putting the sensitivity axis

along the earth gravity field) while checking the response. Usually, this is done manually and it is not a good solution for remotely placed sensors or sensors with difficult access. Since a very accurate model is obtained with the proposed scheme, the actuation voltages that give the same response as a ± 1 g can be computed and used to electrically calibrate the sensor.

5. CONCLUSIONS AND FUTURE WORK

A novel technique is presented which allows estimating over-etching, mismatch, and Young's modulus parameters in capacitive MEMS accelerometers or electrostatic microactuators, relying on the measurement of pull-in voltages and resonance frequency. The underlining theoretical justification is described, and preliminary results obtained with a set of fabricated devices show that results in very good agreement with the expected ones can be obtained, confirming thus the validity of the used MEMS models and the feasibility of the method as a testing technique. The method was tested within a surface micromachining process, but it can be extended to other surface micromachining processes or to more recent technologies like SOI-based processes. The important features are the correctness of the device models and a readout mechanism for pull-in voltage measurements.

In the future, long-term pull-in measurements are needed to check if pull-in deviations from the initial measured values will give information on device's performance deterioration with aging. Future work includes also the identification of failure modes and the estimation of errors due to uncertainty on the measurements and how those can influence the correct estimation of the device parameters.

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Research Article

Using Signal Envelope Detection for Online and Offline RF MEMS Switch Testing

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The test of radiofrequency (RF) integrated circuits at their ever-increasing operating frequency range requires sophisticated test equipment and is time-consuming and, therefore, very expensive. This paper introduces a new method combining low-frequency actuation signal as test stimuli and signal envelope detection applied on the RF output signal in order to provide a low-cost mean for production testing of RF MEMS switches embedded in system-in-package (SiP) devices. The proposed approach uses the principle of alternate test that replaces conventional specification-based testing procedures. The basic idea is to extract the high-frequency characteristics of the switch from the signal envelope of the response. Output parameters like "on" and "off" transition time are extracted at low frequency and used in a regression process to predict RF conventional specifications like S-parameters. The paper also provides a set of recursive estimation algorithms suitable for online testing. In this context, "on" and "off" transition time estimated from the output low-frequency envelope is used as test metrics and is concurrently updated using recursive algorithms. Validation results obtained on a capacitive RF switch model are presented.

1. INTRODUCTION

The trend toward more portable solutions, with more embedded functions, drives the demand for the system-in-package (SiP) technology. Cellular handset designs represent a good example of this global trend. Today, a cellular mobile must offer multiband and multimode in addition to Bluetooth networking, global positioning system (GPS), and wireless local area network (WLAN), not to mention the user applications such as games, audio, and video (TV on Mobile). The International Technology Roadmap for Semiconductors defines a system-in-package as any combination of semiconductors, passives, and interconnects integrated into a single package [1]. This definition clearly indicates that an SiP can combine different die technologies and applications with active and passive components to form a complete system or subsystem, whereas a system-on-chip (SoC) is created from one single die. Consequently, an SiP usually includes logic and memory components, but it also increasingly includes analog, mixed-signal and RF components, and micro-electromechanical systems (MEMS). These various components are interconnected by wire-bond, flip-chip, stacked-die technology, or any combination of above. The final packaged SiP is looking like any conventional SoC package. Figure 1 shows an example of interconnection of multiple die components in an SiP for Global system for mobile communication (GSM) application. As shown in Figure 2, different type of carriers can be used to incorporate the whole package made of the dies and their interconnections.

SiP offers a unique advantage over SoC in its ability of integrating MEMS with circuitry to provide a fully functional system, not just acting as a simple sensor or actuator. The need for various RF bands in mobile phones is a key driver for the introduction of components that can switch the received or transmitted RF signal to the appropriate blocks.

These new heterogeneous integrated systems pose many challenges from a test perspective. Generally, because of factors such as cost, quality, and reliability, an SiP must be created from bare dies with a high-quality level, in other terms, from known-good-dies (KGD). The manufacturing process, and particularly the packaging step, is more

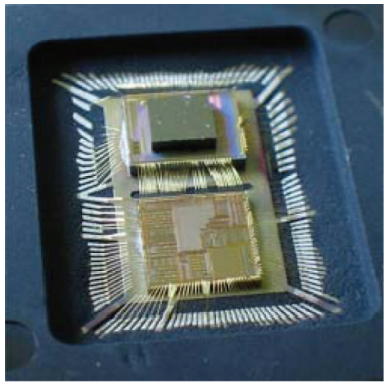


Figure 1: Multiple die components and interconnections on an SiP for GSM application.

complex, potentially increasing the likelihood of failing devices. Indeed, MEMS packaging process is a critical operation on its own because of the requirements for the cavity sealing. Therefore, assembling MEMS into an electronic system puts more requirements on mass production. Last but not least, the test strategy and its consequences on methods and design-for-test (DfT) features must be carefully considered.

In this paper, we aim at developing a low-cost production test approach for RF MEMS switches embedded in SiP devices. Since the RF MEMS switch is embedded together with other devices, the most important difficulty is to obtain measures at the output of the switch in order to detect and diagnose potential faults. In the approach we present, the output of the switch is monitored by means of an envelope detector. The low-frequency output of this detector is then used to predict the actual high-frequency performances of the switch. This approach relaxes the constraints on sampling speed and timing accuracy when applied to very high-speed RF components.

The rest of the paper is structured as follows. First, Section 2 briefly reviews some previous works on RF MEMS testing. Behavioral modeling of capacitive switches is discussed in Section 3. Emphasis is given to dynamic modeling of a series capacitive switch. Section 4 deals with the proposed testing scheme. Different switching parameters are presented and the way of extracting them from the output envelope for offline and online testing purposes is discussed. Monte Carlo simulation and nonlinear regression are discussed in Section 5. The simulation results show accurate prediction of S-parameters using the estimated transient time. Section 6 suggests a set of recursive algorithms for online monitoring of transition times, allowing online testing schemes for RF MEMS switches. Conclusions are given in Section 7.

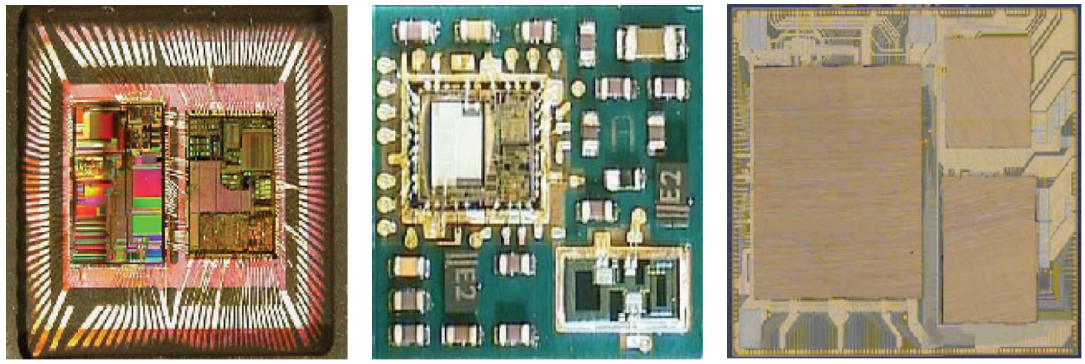
2. PREVIOUS WORKS

Work on RF integrated circuit testing has been largely triggered by the need of testing RF transceivers. This problem can be illustrated by an example strategy of a path-based testing approach, where a receiver or transmitter channel is tested from antenna to digital baseband as a whole. At a first glance, we might expect that testing the system parameters, such as bit error ratio (BER) for the receiver path or error vector magnitude (EVM) for the transmitter, would ensure a sufficient coverage at a reasonable cost. This is not the case because such a test requires expensive RF instruments, and the test of the RF switch cannot guarantee all the specifications and, more importantly, the quality and the reliability of the component, thus of the whole system.

Because of the long evaluation time needed and expensive RF ATE (automated test equipment) required by elaborate performance tests, the production testing of high performance SiP is a major component of the total manufacturing cost. Indeed, ICs production testers with RF capabilities supporting frequencies of GHz range are prohibitively expensive. Further increase of the costs is due to the key problem with testing RF dies coming from the fact that many complex RF specification values need to be determined during production test at high operating frequencies [2, 3]. Testing a significant number of devices in this way is therefore prohibitive and impractical. RF MEMS switches are among the most test demanding RF devices.

In recent years, alternate tests have been considered as a promising solution for low-cost test of RF components [4–6]. In contrast to the previous work using classical functional testing methods, the test specifications of the device-under-test (DUT) are not measured directly using conventional methods. Instead, in alternate testing approaches, the test specification values of the DUT are computed directly from the observed test response when a specially crafted stimulus is applied.

Previous works on RF MEMS switches [7, 8] have exposed the advantages of testing them at lower test frequency instead of performing the measurements by investigating them at the intended signal frequency. In [7], the reliability assessment of a capacitive shunt switch is considered. It is shown that a low frequency of 10.7 MHz is already sufficient for detecting the main features of the switch cycle such as pull-in voltage, rise- and fall-times of the switching action and the difference between the on-capacitance and the off-capacitance (ΔC). A square wave of 10 kHz is used as actuation signal. The output signal is bandpass filtered around the switched voltage frequency. A diode detector is used for demodulation followed by an amplifier. Although some failure mechanisms may be related to GHz frequencies, it is shown in [7] that many failure modes can be investigated at this lower test frequency. Therefore, the test procedure requires only standard components that are less expensive and easier to use in order to build a measurement sufficiently rich to investigate important properties of the switching behavior, such as rise- and fall-times and stability. Taking the test of an RF MEMS switch as illustration example, in [8] the authors study the monitoring of an SiP integrating MEMS devices. Similarly as in [7], a capacitive shunt switch is used here to illustrate the proposed scheme.



(a) (b) (c)

Figure 2: Examples of carrier style of an SiP package: (a) Leadframe, (b) Laminate, (c) Silicon-Based.

3. BEHAVIORAL MODEL OF CAPACITIVE SWITCHES

A number of different criteria can be used to classify MEMS switches. Taking into account the actuation mechanism, the electrostatic, electromagnetic, or electrothermal principle can be considered. The electrostatic principle is the most convenient for the fabrication that can be compatible with typical RF technologies. Switches based on the electrostatic principle are also smaller and faster.

Depending on the circuit configuration, switches can be of series or parallel (shunt) types. These two configurations are illustrated in Figure 3. The switching element can be designed as a beam fixed on both ends, as a cantilever or as a membrane. The choice of the form of the element is driven by the demand on the switch stiffness that defines the necessary switching voltage or by the facility to be used in certain switch configurations.

The type of switching contacts distinguishes two different approaches to the switch application. There are switches creating a resistive (metal to metal) contact or a capacitive (contact-less) one. The first group allows DC applications and can be used up to 60 GHz, whereas the second group covers the frequency range from 6 to 120 GHz. An important parameter describing the quality of capacitive switches is the capacity ratio in the "on" and "off" states. Typical key specifications of today switches include

(i) $C_{ON}/C_{OFF} > 100$,

(ii) actuation voltage <20 V,

(iii) number of switching cycles to failure $>10^9$,

(iv) $t_{down} \sim 5$ microsecond,

(v) $t_{up} \sim 3$ microsecond.

To allow investigation of phenomena such as pull-down, release, power handling, and source noise effects, a behavioral model of the switch is needed with the control voltage V_c that can be an arbitrary continuous function of time.

3.1. Low-frequency dynamic analysis

There are a number of physical mechanisms available for switch actuation. Among these, the electrostatic (or capacitive) conversion is one of the most mature. This is probably because actuators using this conversion are commonly produced with surface micromachining technology that is compatible with integrated circuit fabrication process.

The electrostatic mechanism is based on the interaction between the mechanical and electrical quantities in a condenser having one electrode fixed and the other electrode movable. A voltage applied between both electrodes causes the displacement of the movable electrode. In a transversal capacitive transducer, the movable electrode is displaced off-plane, perpendicularly to the electrode surface. In order to avoid the electrical contact between actuating electrodes, the dielectric layer between these electrodes must be introduced.

The original distance between the electrodes H defined in Figure 4 varies by the displacement x when the transducer is in function. The instantaneous transducer capacity is

$$C = \frac{\varepsilon A}{H - x + (t_d/\varepsilon_d)}, \tag{1}$$

where $A = Ww$ is the area of electrodes, ε the permittivity of air, t_d and ε_d are the thickness and the relative dielectric constant of the dielectric layer, respectively. Supposing that the voltage does not change during the movement of the movable electrode, the electrostatic force is given by

$$F_e = \frac{\varepsilon A U^2}{2\left(H - x + (t_d/\varepsilon_d)\right)^2}. \tag{2}$$

The dynamic model of the cantilever beam is useful for determining the switching time of the switch, the frequency bandwidth of the mechanical part, and the effect of damping. In case of small displacements, the dynamic response of the MEMS beam is given by

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = \frac{\varepsilon A U^2}{2\left(H - x + (t_d/\varepsilon_d)\right)^2}, \tag{3}$$

where x is the beam displacement, m is the beam mass, the spring constant k due to a uniform force applied over the entire beam is given by

$$k = \frac{2Ew}{3}\left(\frac{T}{a}\right)^3. \tag{4}$$

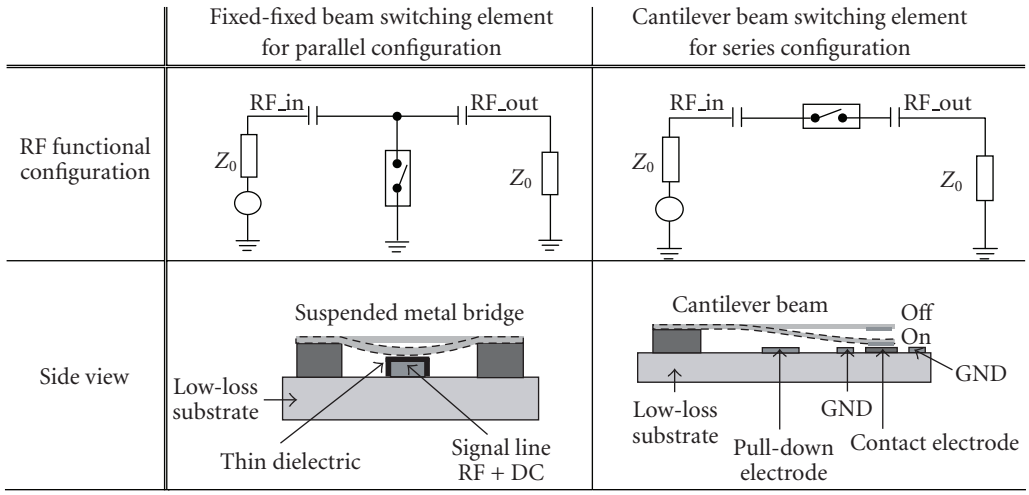
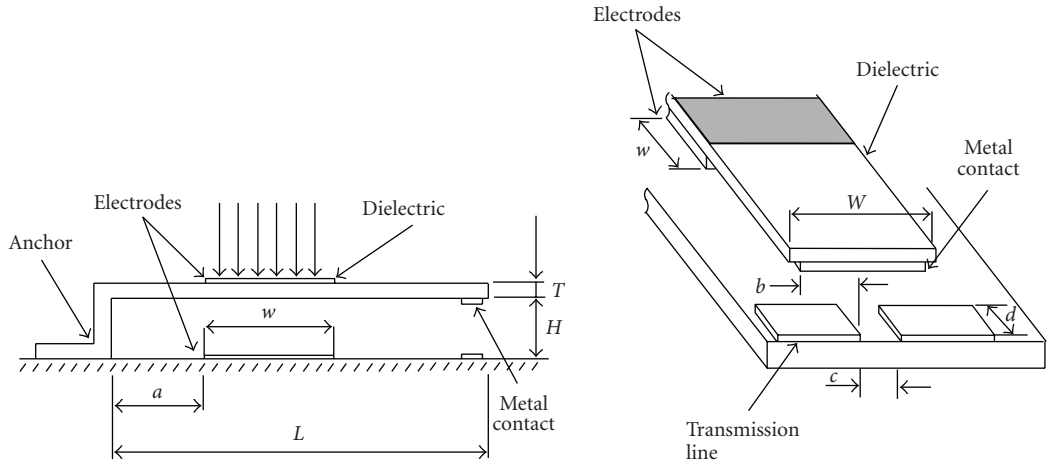


Figure 3: Parallel and series configurations of RF MEMS capacitive switches.



$L = 200\,\mu$m, $W = 50\,\mu$m, $T = 1\,\mu$m, $H = 3\,\mu$m, $w = 100\,\mu$m, $a = 100\,\mu$m, $b = 15\,\mu$m, $c = 10\,\mu$m, $d = 20\,\mu$m

(c)

Figure 4: Design parameter of a cantilever beam switch: (a) side view and (b) perspective view.

An approximate formula for the damping coefficient for a cantilever beam is given in [9] by

$$b = \frac{3\mu S^2}{2\pi H^3}, \tag{5}$$

where S is the area of the beam, a, T, H, and w are the design parameters defined in Figure 4, and E and μ are Young's modulus and the coefficient of viscosity, respectively.

3.2. High-frequency equivalent circuit

A capacitive series switch with resistive (metal-to-metal) contact is shown in Figure 5(a). The corresponding circuit model of the RF section is shown in Figure 5(b). For a cantilever switch with two contact areas, the capacitance is composed of a series capacitance (C_s) between the transmission lines and the switch metal and a parasitic capacitance (C_p) between the open ends of the transmission lines. The total series capacitance is $C_s/2$ with

$$C_s = \frac{\varepsilon A_s}{H - x + (t_d/\varepsilon_d)}, \tag{6}$$

where A_s is the contact area in both sides. It is seen that the capacitance C_s has a strong dependence on the displacement x. The MEMS series switch resistance between the contact areas is dependent on its length and width. The transmission line loss must be added to obtain the total switch resistance which is assumed constant. In the down-state position, it is possible to model the transmission lines by a series inductance. For simplicity, the inductance of the switch is supposed negligible in the rest of the paper and the

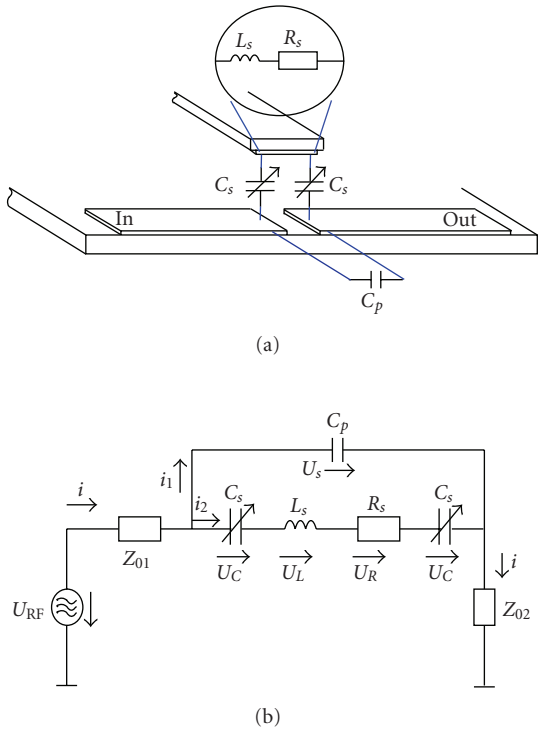


FIGURE 5: (a) RF capacitive switch showing the input and output RF transmission line and the switching contact placed on the free end of the cantilever, and (b) circuit model corresponding to the RF behavior.

impedances Z_{01} and Z_{02} represent incoming and outgoing transmission line sections.

3.3. *Complete model of the switch*

The equations governing the complete behavior of the switch can be readily solved with a nonlinear simultaneous differential equation solver such as Matlab/Simulink. The complete model of the series switch is given in Figure 6. For the simulation of this model, the physical parameter values given in Figure 4 have been considered.

4. USING ENVELOPE DETECTION TO EXTRACT LOW-FREQUENCY OUTPUT PARAMETERS

In order to facilitate the embedded test of an RF switch, the evaluation of the test response needs to be handled by an on-chip analog detector with a low-frequency output. In this work, we use an embedded envelope detector to capture a low-frequency signal describing the switching behavior of the device. Figure 7 shows an envelope detector embedded in an RF MEMS serial switch. It consists simply of a diode and resistor-capacitor (RC) filter.

In a positive half cycle of the input signal, the diode is forward biased and the capacitor C_t charges up rapidly to a peak value of the input signal. When the input signal falls below this value, the diode becomes reverse biased and the capacitor discharges slowly through the load resistor R_t. The discharging process continues until the next positive half cycle. Thereafter the charging-discharging cycle is continued. The values of R_t and C_t are to be chosen appropriately to perform the required envelope detection. The envelope detector output signal is shown in Figure 8.

An RF input signal of 1 GHz is applied to the incoming transmission line of the switch and a simple pulse signal (Figure 8(a)) is applied to its electrodes as actuation input. The RF output signal obtained on the outgoing transmission line is plotted in Figure 8(b). The corresponding envelope detector output is represented in Figure 8(c).

For an actuation signal applied to the switch (functional, or a special test actuation), easily measurable output parameters must be extracted from the observed low-frequency test response. Conventional performances (such as *S*-parameters) can be predicted from this estimation using a nonlinear regression equation. The following output parameters can be extracted from the low-frequency test response.

(i) Transition time. This is given by the time to switch from the "off" to the "on" state and vice versa. The conventional definition of the transition times is the time required for the output RF signal to rise from 10% to 90% of its value for off-to-on transition and 90% to 10% for on-to-off transition. However, since the corresponding values will be difficult to evaluate, we will use the definition of t_{on} and t_{off} given in Figure 9. These values are easily obtained from the output envelope as shown in Figure 9.

(ii) Off/on voltage ratio. This parameter is given by the ratio of the test signal amplitudes in the "off" and "on" states. A good approximation of this ratio is given by A_{off}/A_{on}, where A_{on} and A_{off} are, respectively, the switch on- and the switch off- envelope amplitudes defined in Figure 9.

(iii) Actuation voltages. The switch-on voltage V_{on} is the minimal voltage required to switch the device from the "off" to the "on" state. The switch-off voltage V_{off} has an analog definition.

5. COMPUTING S-PARAMETERS FROM LOW-FREQUENCY OUTPUT PARAMETERS

Monte Carlo simulation was combined with a nonlinear regression analysis to generate mappings from the low-frequency output parameters to high-frequency *S*-parameters. A Monte Carlo simulation is first done to generate a sample of 200 switches. A Gaussian distribution is applied for each physical parameter given in Figure 6, with a variation coefficient of 0.4 (standard deviation = 0.4 × nominal value).

For each of the 200 switches, the *S*-parameters are computed at an operating frequency of 1 GHz. The alternate test stimulus is a simple low-frequency pulse signal. The feature extraction algorithm uses the signal envelope to compute an estimation of the transition time (T_{on} and T_{off}). These samples are fed into a regression model generated

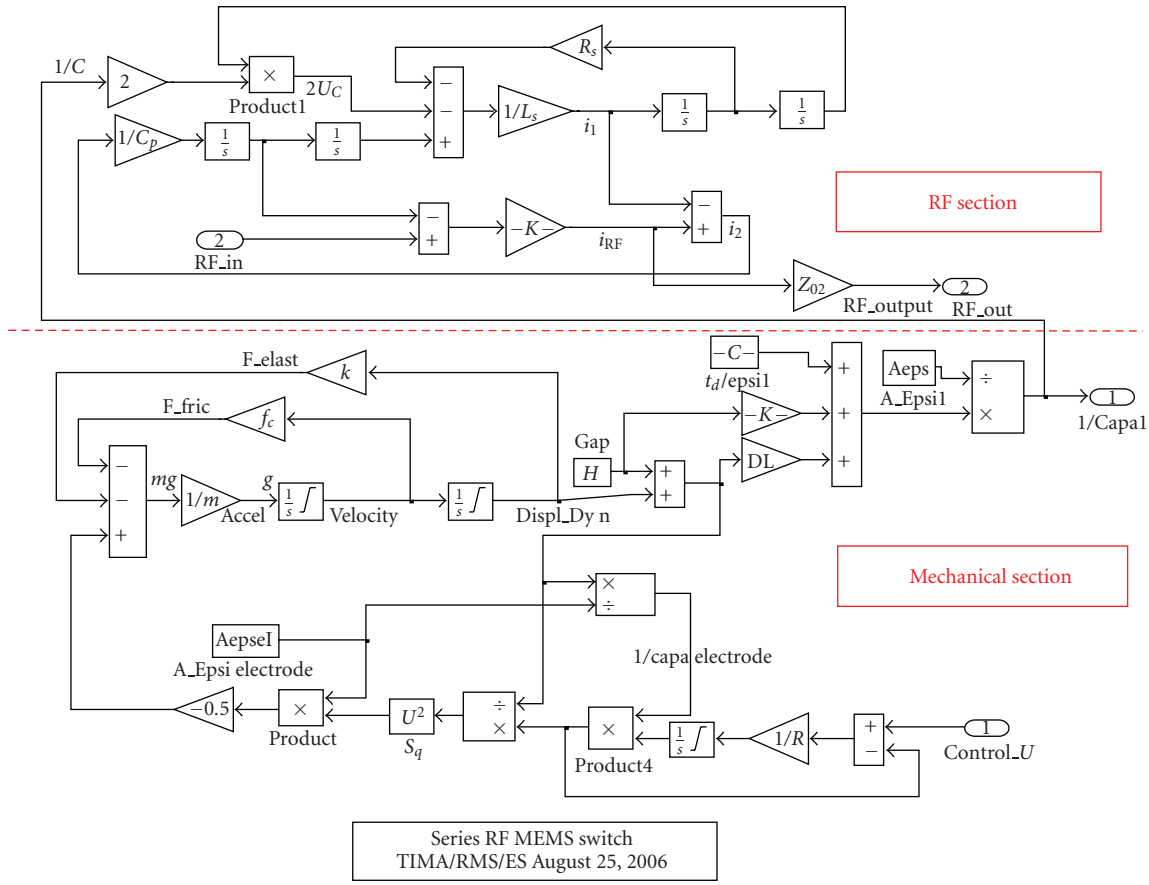


Figure 6: Matlab/Simulink dynamic model of the RF switch.

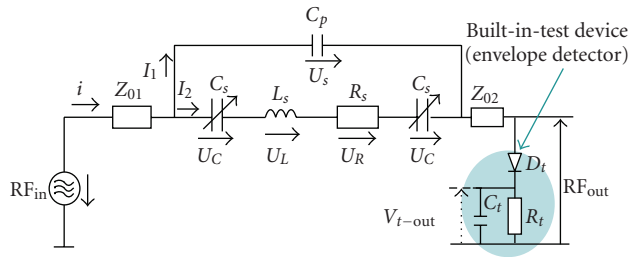


Figure 7: Envelope detector embedded in an RF MEMS serial switch scheme.

by 100 instances of the switch Matlab/Simulink model. The regression procedure aims at finding the best fitting curve to the set of 100 points by minimizing size of the offsets (the residuals) of the points from the curve. The least square regression methods use the sum of the squares of the offsets instead of the offset absolute values because this allows the residuals to be treated as a continuous differentiable quantity. Our experimental procedure aims at providing a fitting function for the independent variable X which is a vector of component T_{on} and T_{off} that estimates high-frequency parameter S_{ij} for a given $x = (t_{\text{on}}, t_{\text{off}})$. The linear least squares fitting technique is the simplest and the most commonly used form of regression method that provides a much simpler analytic form for the fitting parameters than other nonlinear regression fitting algorithm such as MARS [10] which is used in [4, 5, 11] for alternate test. In addition, the fitting technique can be easily generalized from a linear fitting to any nonlinear expression provided that the parameters to be estimated appear linearly in the fitting function. In fact, the functional relationship between the S_{ij} and $x = (t_{\text{on}}, t_{\text{off}})$ is assumed to be a combination of nonlinear expressions as exponential (e^x), power (x^n), and logarithm (lnx), with additive or multiplicative constants. The data are first transformed in such a way that the resulting line is a straight line. For this reason, standard forms for exponential, logarithmic, or power laws in the nonlinear fitting function expression are first explicitly computed.

The accuracy of the regression result is validated by a separate set of 100 instances that are generated independently from the training set. Figure 10 shows the predicted versus actual specifications of 100 instances in this validation set for S_{12} and S_{12} specification parameters. As shown in Figure 10, the specification S_{12} is predicted with a relatively good accuracy using only the transition times.

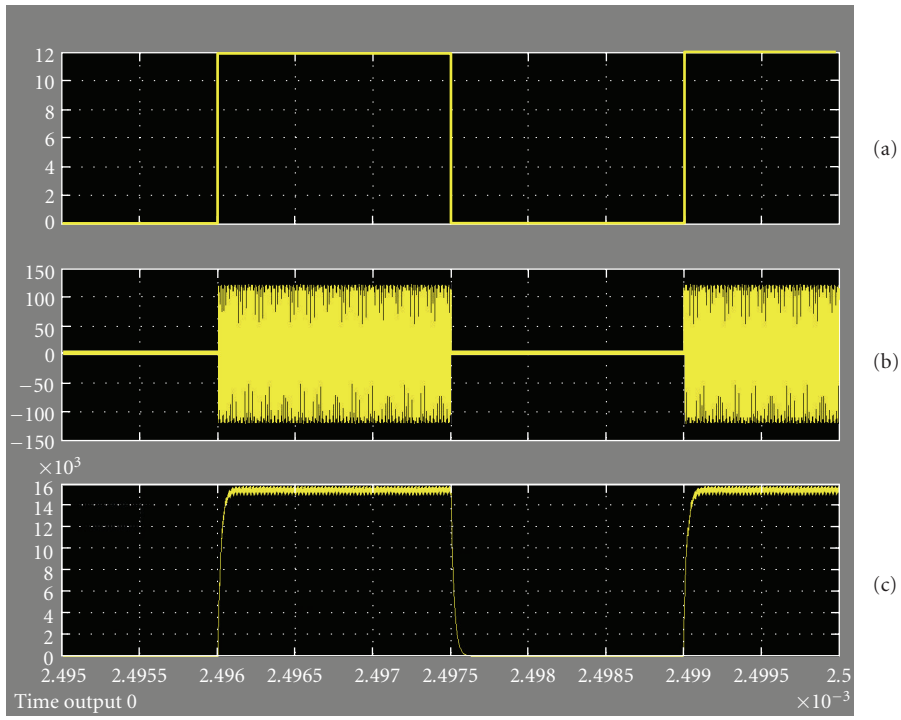


Figure 8: Test signal simulation: (a) switch actuation control signal, (b) RF output signal, (c) detected envelope of the output signal.

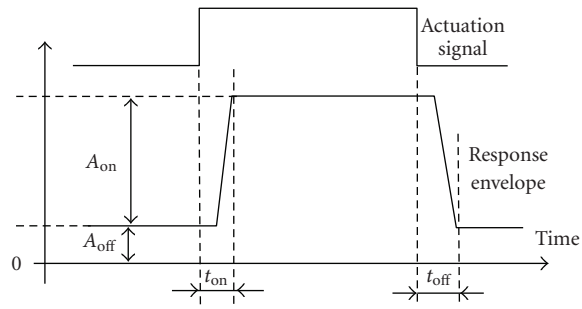


Figure 9: Low-frequency output parameters: t_{on} is the total delay time of a rising edge; t_{off} is the total delay time of a falling edge; A_{on} is the envelope amplitude in the "on" state; and A_{off} is the envelope amplitude in the "off" state.

6. RECURSIVE ESTIMATION-BASED ONLINE MONITORING OF TRANSITION TIMES

In this section, we are suggesting three recursive estimation algorithms that can be used for online monitoring of low-frequency test metrics extracted from the switching envelope signal. All the switching characteristics can be used as test metrics in a procedure of low-frequency offline testing as well as in online monitoring scheme. In the offline testing case, a special test stimulus is applied on the actuation input of the switch. The test decision is taken by comparing the switching characteristics estimated from the output envelope to their nominal values. In the context of online testing scheme, the switching characteristics are estimated concurrently to the normal operation of the switch by means of a recursive identification algorithm. The value of each of the test metrics is updated at each operation. For the switching cycle K, an estimation $\hat{\theta}(t)$ of the mean value of the switching test metric $\theta(t)$ is given by

$$\hat{\theta}(t) = \frac{1}{t}\sum_{i=1}^{t}\varphi(i), \tag{7}$$

where $\hat{\theta}(t)$ is the mean value of the parameter for the t first switching cycles and φ(i) is the value of the test metric measured for the switching cycle i. Since new data appears recursively, we must avoid repeating all calculations at each stage. This involves the use of a recursive formula that expresses $\hat{\theta}(t)$ in terms of $\hat{\theta}(t-1)$.

Theorem 1. *A recursive form of* (7) *expressing* $\hat{\theta}(t)$ *in terms of* $\hat{\theta}(t-1)$ *is (see proof in the appendix)*

$$\hat{\theta}(t) = \frac{t-1}{t}\hat{\theta}(t-1) + \frac{\phi(t)}{t}. \tag{8}$$

In the context of online testing, it is necessary to adapt the estimator quickly when appears a change in the device. Weighting factors are introduced in the mean value calculation to give more weight to the new data compared

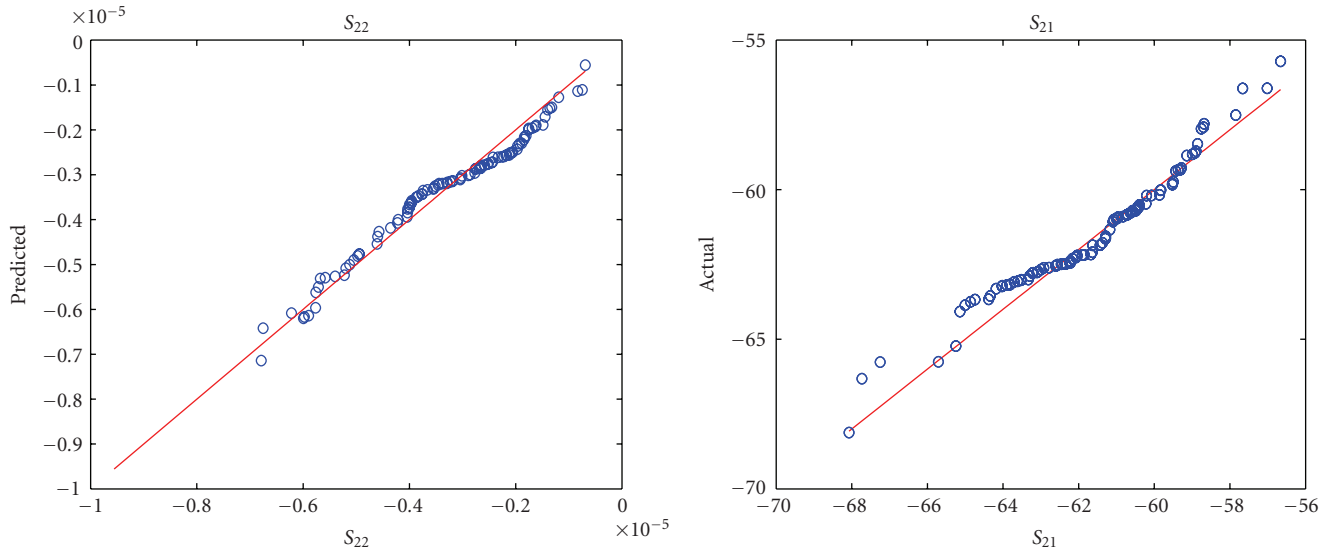


Figure 10: Predicted S-parameter for RF MEMS Switch.

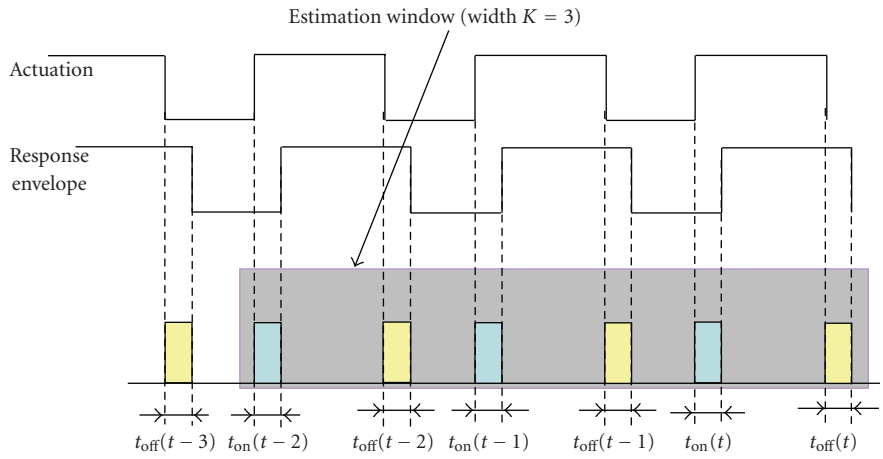


Figure 11: Sliding window recursive estimation.

with the older. The weighting or forgetting factors allow then to forget old information. The mean value is then given by

$$\hat{\theta}_\lambda(t) = \frac{\lambda^t\phi(0)+\lambda^{t-1}\phi(1)+\cdots+\lambda^{t-i}\phi(i)+\cdots+\lambda\phi(t)+\phi(t)}{\lambda^t+\lambda^{t-1}+\cdots+\lambda^{t-i}+\cdots+\lambda+1} = \frac{\sum_{i=0}^{t}\lambda^{t-i}\phi(i)}{\sum_{i=0}^{t}\lambda^i}, \tag{9}$$

where the forgetting factor λ verifies: $0 < \lambda < 1$.

Theorem 2. *When the time value t is great enough, a recursive form of* (9) *expressing* $\hat{\theta}_\lambda(t)$ *in terms of* $\hat{\theta}_\lambda(t-1)$ *is given by (see proof in the appendix)*

$$\hat{\theta}_\lambda(t) = \lambda\hat{\theta}_\lambda(t-1) + (1-\lambda)\phi(t). \tag{10}$$

In another recursive estimation algorithm, only the data included in a sliding window are used in the estimation formula. All the past data that are out of this sliding window are not taken in the updating of the test metric estimation value. The mean value of the test metric is then estimated through a sliding window of width K as shown in Figure 11 (for $K = 3$).

In this case, the mean value estimation is given by the following definition equation:

$$\hat{\theta}_K(t) = \frac{1}{K}\sum_{i=0}^{K-1}\phi(t-i), \tag{11}$$

where K is the width of the estimation window.

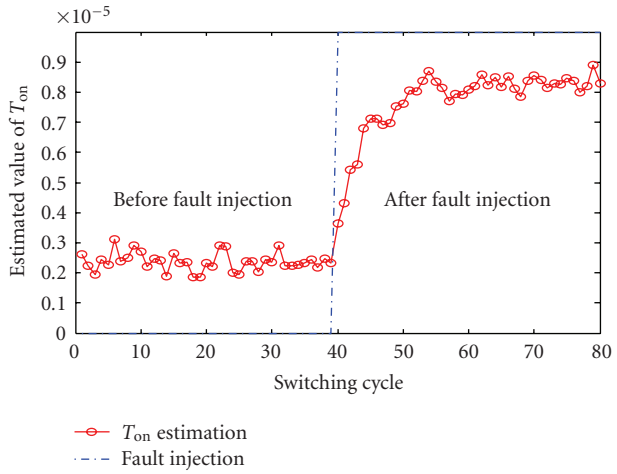


FIGURE 12: Simulation of recursive estimation for online fault detection using the sliding window algorithm.

Theorem 3. *A recursive form of* (11) *expressing* $\hat{\theta}_K(t)$ *in terms of* $\hat{\theta}_K(t-1)$ *is given by (see proof in the appendix)*

$$\hat{\theta}_K(t) = \hat{\theta}_K(t-1) + \frac{\phi(t) - \phi(t-K)}{K}. \tag{12}$$

To test the efficiency of the proposed online testing scheme, many fault injections have been simulated on the RF MEMS switch Matlab/Simulink model of Figure 5. Among the recursive algorithms proposed above, the sliding window method seems to be a good trade-off between the complexity of online fault detection scheme and its efficiency in terms of fault latency and fault coverage.

Figure 12 gives an example of parametric fault detection using the estimation of off-to-on transition time. A parametric fault corresponding to a 50% decrease of the electrode area ($A = Ww$) was injected in the behavioral model of the switch. It is evident that this is a typical parametric manufacturing fault. However, this type of fault may also occur in an operating application when the hermetic packaging requirements of RF MEMS switch are no longer guaranteed. It is clear from this figure that the injected fault is quickly detected since the T_{on} mean value estimated before the fault injection is soon significantly different than the mean value obtained after the fault injection.

7. CONCLUSIONS

The main objective of this work is to find a way of testing RF MEMS switches that leads to a low-cost implementation and that speeds up the whole process of conventional functional testing of RF devices embedded in SiP packages. We have suggested a testing scheme of capacitive RF MEMS switches based on an envelope detector that provides a low-frequency output. Simulation results show that this signal provides important properties of the switching behavior, such as transition times, actuation voltage, and switching voltage ratio. From data provided by Monte Carlo simulation, we have implemented a multivariate regression algorithm to build nonlinear mappings that link the low-frequency test metrics to conventional specifications parameters of RF devices such as *S*-parameters that are available at RF operating frequency only. As a consequence, the conventional high-frequency specifications of the switch are predictable from the low-frequency signal envelope. The results obtained using the proposed methodology show that the high-frequency specifications can be predicted with good accuracy from the transition time measurement. In the proposed methodology, the test is performed using a low-frequency envelope signal without requiring access to high-frequency information, thus eliminating the need for expensive RF ATE. For online testing purposes, the paper also provides a set of recursive algorithms aiming at low-cost online monitoring of low-frequency test features extracted from the switching envelope signal, instead of testing the RF device at its typical operating frequency.

APPENDIX

Proof of Theorem 1. The mean value estimation of the test metric $\theta(t)$ for the t first measurements is given by

$$\hat{\theta}(t) = \frac{1}{t}\sum_{i=1}^{t}\varphi(i) \;= \frac{1}{t}\sum_{i=1}^{t-1}\varphi(i) + \frac{1}{t}\varphi(t)\ ,$$

Since

$$\frac{1}{t}\sum_{i=1}^{t-1}\varphi(i) = \frac{t-1}{t}\left(\frac{1}{t-1}\sum_{i=1}^{t-1}\varphi(i)\right) = \frac{t-1}{t}\theta(t-1),$$

$$\hat{\theta}(t) = \frac{1}{t}\sum_{i=1}^{t-1}\varphi(i) + \frac{1}{t}\varphi(t) = \frac{t-1}{t}\hat{\theta}(t-1) + \frac{\varphi(t)}{t}. \tag{A.1}$$

□

Proof of Theorem 2. Since the weighted mean value estimation of the test metric is given by

$$\hat{\theta}_\lambda(t) = \frac{\sum_{i=0}^{t}\lambda^{t-i}\varphi(i)}{\sum_{i=0}^{t}\lambda^{i}} = \frac{N_\lambda(t)}{D_\lambda(t)} \tag{A.2}$$

for the numerator term we have

$$\begin{aligned} N_\lambda(t) &= \sum_{i=0}^{t}\lambda^{t-i}\varphi(i) \\ &= \sum_{i=0}^{t-1}\lambda^{t-i}\varphi(i) + \varphi(t) \\ &= \lambda\left(\sum_{i=0}^{t-1}\lambda^{(t-1)-i}\varphi(i)\right) + \varphi(t) \\ &= \lambda\cdot N_\lambda(t-1) + \varphi(t). \end{aligned} \tag{A.3}$$

And for the denominator $D_\lambda(t)$ we have

$$D_\lambda(t) = \sum_{i=0}^{t}\lambda^i = 1 + \lambda\sum_{i=0}^{t-1}\lambda^i = 1 + \lambda\left(\sum_{i=0}^{t}\lambda^i - \lambda^t\right) = 1 - \lambda(D_\lambda(t) - \lambda^t). \tag{A.4}$$

Then $D_\lambda(t) = (1-\lambda^{t+1})/(1-\lambda)$ and finally it follows that

$$\hat{\theta}_\lambda(t) = \frac{N_\lambda(t)}{D_\lambda(t)} = \frac{\lambda\cdot N_\lambda(t-1)}{(1-\lambda^{t+1})/(1-\lambda)} + \frac{\varphi(t)}{(1-\lambda^{t+1})/(1-\lambda)}, \tag{A.5}$$

and since $D_\lambda(t-1) = (1-\lambda^t)/(1-\lambda)$ we have

$$\hat{\theta}(t) = \frac{\lambda.}{(1-\lambda^{t+1})/(1-\lambda)}\frac{1-\lambda^t}{1-\lambda}\frac{N_\lambda(t-1)}{D_\lambda(t-1)} + \frac{\varphi(t)}{(1-\lambda^{t+1})/(1-\lambda)} = \frac{(1-\lambda^t)\lambda\hat{\theta}_\lambda(t-1) + (1-\lambda)\varphi(t)}{1-\lambda^{t+1}}, \tag{A.6}$$

and finally for t great enough since $0 < \lambda < 1$, $\lambda^t \underset{t\to\infty}{\to} 0$, it follows that

$$\hat{\theta}_\lambda(t) = \frac{(1-\lambda^t)\lambda\hat{\theta}_\lambda(t-1) + (1-\lambda)\varphi(t)}{1-\lambda^{t+1}} \underset{t\to\infty}{\longrightarrow} \lambda\hat{\theta}_\lambda(t-1) + (1-\lambda)\varphi(t). \tag{A.7}$$

□

Proof of Theorem 3. For an estimation window width K, the mean value estimation of the test metric is given by

$$\hat{\theta}_K(t) = \frac{1}{K}\sum_{i=0}^{K-1}\varphi(t-i) = \frac{1}{K}\left[\left(\sum_{i=0}^{K-1}\varphi(t-i) - \varphi(t) + \varphi(t-K)\right) + \varphi(t) - \varphi(t-K)\right],$$

$$\hat{\theta}_K(t) = \frac{1}{K}\left[\left(\sum_{i=0}^{K-1}\varphi((t-1)-i)\right) + \varphi(t) - \varphi(t-K)\right].$$

Then $\hat{\theta}_K(t) = \hat{\theta}_K(t-1) + \dfrac{\varphi(t)-\varphi(t-K)}{K}$. (A.8)

□

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Research Article

MEMS Switches and SiGe Logic for Multi-GHz Loopback Testing

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We describe the use of microelectromechanical system (MEMS) switches and SiGe logic devices for both passive and active loopback testing of wide data buses at rates up to 6.4 Gbps per signal. Target applications include HyperTransport, fully buffered DIMM, and PCI Express, among others. Recently introduced MEMS devices provide >7 GHz bandwidth in a very small package (needed to handle wide buses). SiGe logic supports >7 Gbps signals when active shaping of the waveform is required. Each loopback module typically supports between 9 and 16 differential channels. Multiple cards are used to handle applications with very wide buses or multiple ports. Passive cards utilize MEMS for switching between the loopback (self-test) mode and traditional automated test equipment (ATE) source/receiver channels. Future active card designs may provide additional waveform-shaping functions, such as buffering, amplitude attenuation/modulation, deskew, delay adjustment, jitter injection, and so forth. The modular approach permits precalibration of the loopback electronics and easy reconfiguration between debug or characterization testing and high-volume production screening.

1. INTRODUCTION

During the past few years we have developed a modular approach for production testing at multiple-GHz rates using conventional automated test equipment (ATE) [1–4]. The modules have included various configurations of "driver" and "receiver" channels that multiplex low-speed (<1 Gbps) ATE signals up to 6.4 Gbps as needed for device-under-test (DUT) testing. Some applications have required as many as 50–100 differential pair signals, each running at these multi-Gbps rates [4]. We have successfully applied this approach on two popular ATE platforms: (1) the Agilent/Verigy 93000-P1000 and (2) the Teradyne UltraFlex with "high-speed-digital" (HSD) and limited "serial-bus-6 GHz" (SB6G) channels.

In this paper, we extend the technique to loopback testing by introducing several new passive and active modules. We target two I/O standards including HyperTransport3 (HT3 at 5.2 Gbps) and fully-buffered dual in-line memory module (FB-DIMM at 4.8 Gbps). Section 2 describes a newly-developed microelectromechanical (MEMS) switch technology which is critical to the loopback solutions that are introduced in Section 3. A comparison of passive loopback modules using either miniature mechanical relays or MEMS is provided in Section 4. Active loopback solutions are shown in Section 5.

Loopback testing, illustrated in Figure 1, is a form of built-in self-test (BIST), whereby the device-under-test (DUT) contains appropriate logic to synthesize test signals which are transmitted through the DUT outputs, and are used to stimulate the DUT inputs. During loopback testing, the DUT outputs take the place of test signals which traditionally are supplied by the ATE. This greatly reduces the need for high-performance ATE resources for the loopback tests. Usually this type of testing requires minimal support from the ATE, so it is highly economical especially when testing high-speed devices.

However, loopback testing is only one of many types of tests that need to be applied to the DUT. For example, DC parametric tests (such as input leakage measurements, input and output voltage sensitivities, etc.) require direct connection of the ATE resources to the DUT I/O. Furthermore,

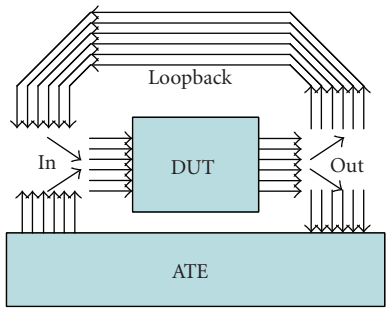

Figure 1: Loopback testing in an ATE test configuration.

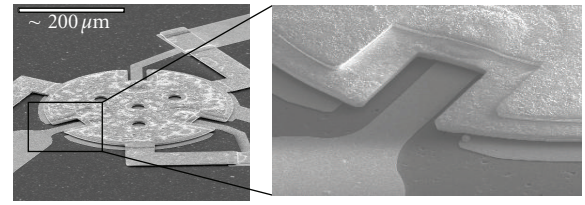

Figure 2: SEM photographs of the high force disk actuator (a) and details of the switch contact area (b).

loopback testing tends to be a pass/fail type test, so direct connections to the ATE are also required for functional diagnostic testing.

Since at least two connections are needed for each DUT I/O (one for loopback and one for traditional testing), and each must support a clean (stub-free) 50-Ohm transmission path, a high-performance switch is needed for each I/O. Logically, 2 : 1 multiplexers and 1 : 2 fanout buffers might be considered. However, a passive connection to the ATE is preferred so that DC parametric and AC waveform characteristics can be tested using traditional ATE resources. In this paper, we demonstrate the advantages of MEMS for this switching application.

2. MEMS SWITCH TECHNOLOGY

As in many testing applications, loopback tests require a way of switching between different signal sources and receivers. Specifically (as shown in Section 3), we need to switch between the ATE resources and the DUT I/O. The traditional approach is to use mechanical (or "reed" type relays). However, the large channel-counts and need for ultra-high bandwidth has forced the development of an even smaller technology called microelectromechanical systems (MEMS) switches. These have proven to be well suited to the loopback testing application, and represent a critical enabling technology for wide-bus applications above 3.2 Gbps (see the performance measurements in Sections 4 and 5).

Recently, TeraVicta has introduced a MEMS switch called TT712.The TT712 switch is fabricated using metal deposition processes found in most CMOS microelectronics manufacturing facilities. However, it also incorporates a number of proprietary features that enable both high performance and high reliability. The TT712 uses a unique device-on-package construction in which the MEMS device is fabricated directly onto the primary packaging material, in this case a ceramic (alumina) wafer with conductive metal vias. Individual switch features are patterned using conventional sputter deposition and etching processes with bulk metal layers (including the sacrificial material) fabricated via electroplating. A selective metal etch is used to remove this sacrificial metal layer (the "release" process), leaving the free standing MEMS switch structure. A scanning electron micrograph (SEM) is shown in Figure 2.

This "device-on-package" architecture has several significant benefits, especially in high-bandwidth test applications. First, the use of conductive vias minimizes the conduction paths within the device and between the device and the printed circuit board, directly reducing insertion loss and minimizing the length of radiating conductive elements that degrade high-frequency performance [5]. This, coupled with surface mount technology (SMT) compatible ball grid array (BGA) solder ball attachment, provides reliable, highly manufacturable signal connections that deliver chip-level high-frequency performance to the circuit board. The use of an alumina substrate also provides substantially lower high-frequency losses than the silicon substrates used in other MEMS switches [6]. This is especially true for devices operating at higher frequencies and for through-substrate via designs like the TT712.

Failures due to stiction between metal surfaces following removal of the sacrificial metal are minimized by key features of the proprietary high force disk actuator (HFDA). This uses a circular design to maximize contact stability and to restore force within the smallest possible footprint. This design also maximizes contact force (proportional to electrode area), which is a key factor in enabling low contact resistance (insertion loss) [7]. Contact stability is further optimized using a "three point" contact configuration, which helps assure that the force on the active electrical contact is highly uniform and repeatable. This results in a very low loss, highly repeatable contact configuration as shown.

The large restoring force of this design is required to provide reliable (stiction free) operation. Although this results in a relatively high switch voltage (68 V), low voltage operation (3–5 V) can be achieved through the use of a separate charge pump IC.

Switches with multiple contact configurations, such as single-pole-double-throw (SPDT) and double-pole-double-throw (DPDT) are constructed by connecting multiple HFDAs in a single package. This is illustrated by the solid model of the basic DC-7 GHz SPDT switch shown in Figure 3, which is shaded according to electric potential of the metal surface (darkest features corresponding to the highest field). The RF signal is conducted into the switch through a central terminal (RF common), which connects to two HFDAs on the device.

The package is carefully matched to 50-Ohm impedance throughout a very wide bandwidth. Typical RF performance of the DC-7 GHz SPDT switch is presented in Figure 4, and shows that these devices have insertion loss of less than 0.1 dB

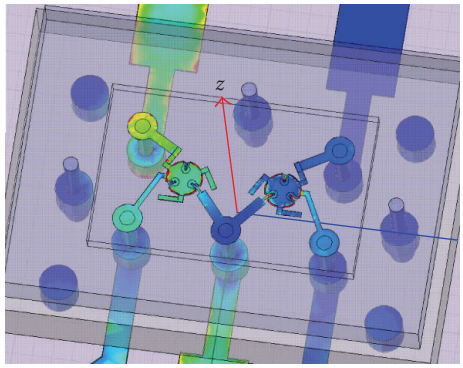

Figure 3: Ansoft model of the DC-7 GHz SPDT switch.

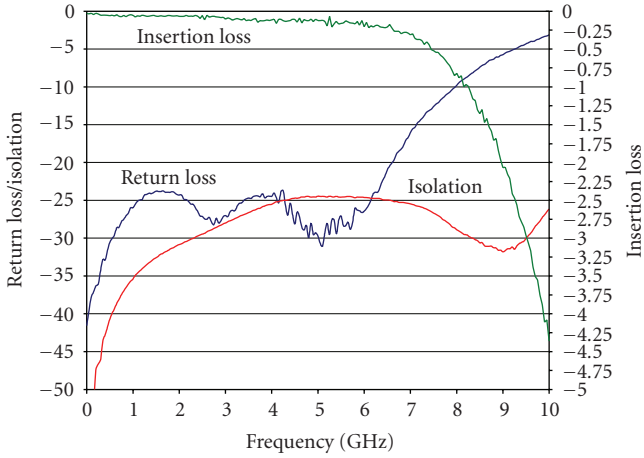

Figure 4: Typical RF performance of the DC-7 GHz SPDT switch.

at frequencies less than 1 GHz (<0.4 dB at 7 GHz), more than 20 dB of return loss and at least 25 dB of isolation. These devices are capable of switching up to 15 W of continuous RF power, with a peak power handling capability of at least 30 W.

In addition to the MEMS Switch's electrical and reliability advantages, there are two other very attractive features important for the loopback test application. First, the electrostatic nature of the actuator is inherently a low-power device, requiring an insignificant amount of current ($\ll$1 uA) to maintain the desired state. Therefore, there is negligible power dissipated within the switches of the loopback module. This feature reduces the cooling requirements. Even more important for large signal-count applications is the significantly smaller package size as compared with typical RF mechanical relays. This is illustrated in Figure 5. The MEMS package has a somewhat smaller footprint, but a *much* shorter height. This shorter dimension is a great advantage when designing thin loopback modules which permits the use of more modules to handle higher-density buses.

Notice that the footprint of the TT712 package is heavily dominated by the external connections. The internal switch elements account for a very small fraction of the device

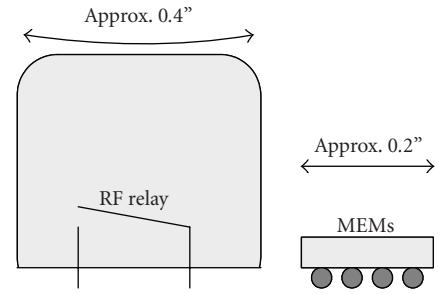

Figure 5: Size comparison of typical mechanical RF relay and MEMS switch packages.

footprint (as seen in Figure 3). Therefore, the MEMS technology has the potential to provide higher levels of integration and therefore support for much higher bus densities.

3. LOOPBACK MODULE DESIGNS

Fundamentally, the minimal loopback test requires that the DUT outputs be connected to appropriate DUT inputs as introduced in Figure 1, and shown in more detail in Figure 6. This allows the internal built-in self-test (BIST) circuits to generate test stimulus patterns for its own inputs, which are then analyzed by internal BIST circuitry as well. However, because we also need to do extensive DC parametric tests, as well as lower-speed functional tests, there must be an option to break the loopback path and substitute connections directly to/from the ATE (also shown in the figure). Switches (relays) are the obvious choice for this. However, great care is required in order to preserve signal integrity at multi-GHz rates.

The design of a suitable loopback module can leverage many of the features that we have previously applied to "driver" and "receiver" modules. For example, in the design of these earlier modules we have taken great care in selecting connectors, relays, and active components that can support the high bandwidth required for multi-GHz signals. We have also devised a common card configuration that fits within the physical constraints of the ATE testheads, while allowing for a maximum number of modules. In many test applications, the entire available volume located directly under the device-interface-board (DIB) is occupied by our modules.

Figure 7 shows a bottom view of a 2-slot DIB with one of our early 2-card loopback boards mounted in "Slot 1." This loopback board was specifically designed to be a direct "drop-in" replacement for a 9-channel HyperTransport driver module (8 data and a clock signal). In this application, Slot 2 (empty in the photo) normally holds a receiver module which likewise can be replaced with another loopback card. The two cards connect to one another through an array of coaxial connectors (upper right corner of the photo), thereby completing the connection of 9 differential pairs for the loopback test.

The cards have mechanical RF relays that allow the DUT I/O to either be connected in the loopack configuration or directly to ATE channels ("low speed" connections). This

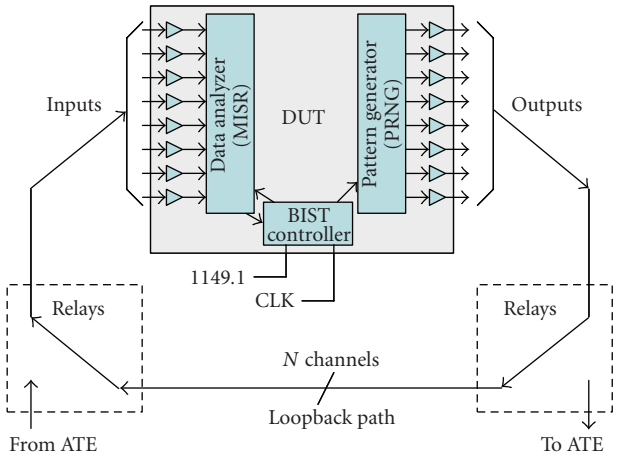

Figure 6: Minimum signal connection paths for loopback and switches to allow direct connection to ATE channels.

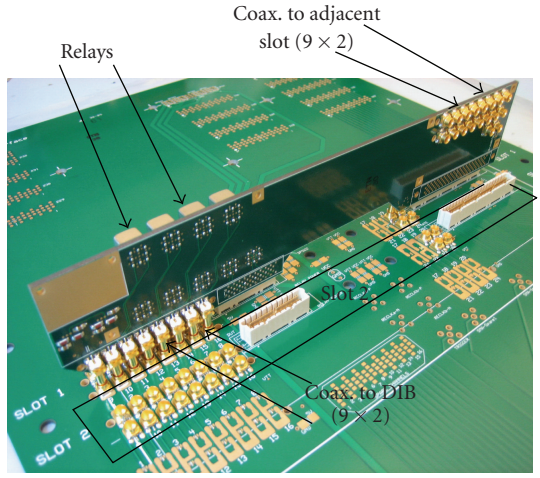

Figure 7: Nine-channel passive loopback card in a 2-slot configuration (slot 2 is empty). Bottom view of DIB.

arrangement is illustrated in Figure 8. In the figure the heavy dark arrows show the loopback path and also represent the coaxial connectors (which can be seen in Figure 7). The thinner lines/arrows show the "low speed" connections to/from the ATE.

In other designs (where drop-in compatibility was not required), we incorporated both the driver and receiver loopback switches onto a single card. This eliminates the card-to-card coaxial connections and reduces transmission line lengths. The "single-card" loopback arrangement is shown in Figure 9. Performance characteristics for each of these configurations are given in the following sections.

In order to remove heat and to tightly control the module temperature (for improved timing accuracy) we construct water-cooled heatsinks for each card. When using mechanical relays, the total module thickness is between 0.75 and 1.00 inch and is largely limited by the height of the relay packages. The use of MEMS switches not only reduces the

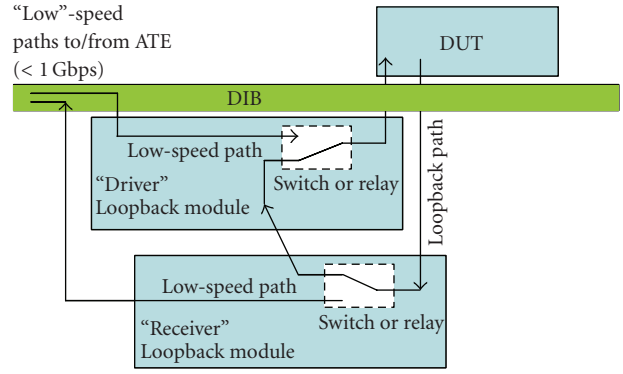

Figure 8: Two-card *passive* loopback switch arrangement. These loopback modules are "drop-in" replacements for active driver and receiver modules.

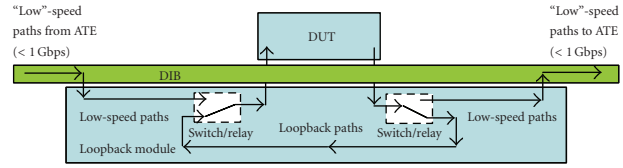

Figure 9: Single-card *passive* loopback switch arrangement. A customized single-card arrangement provides a more efficient (higher-performance) loopback path.

power dissipation, but also allows the total module thickness to be reduced by about 1/4 inch, freeing up space for more modules under the DIB.

4. PASSIVE LOOPBACK MODULE PERFORMANCE

In this section, we demonstrate the performance of several "passive" loopback cards, beginning with a 2-card arrangement (as in Figures 6 and 7), comparing cards built with mechanical RF relays to those using MEMS. We also demonstrate a single-card configuration (as shown in Figure 9) which uses MEMS.

Figure 10 shows the performance of an individual passive loopback card designed for the 2-card configuration (Figure 8). Here the data eye diagram is shown at 3.2 Gbps and 5.0 Gbps. There is a clear degradation of the data eye above 3.2 Gbps. We have determined that this is due to a combination of factors, including dielectric loss, skin effect loss, losses within the relays and small impedance discontinuities in the signal path. Channel-to-channel *skew was less than 10 picoseconds*. The losses are even more evident when both driver and receiver loopback cards are operated together, as shown in Figure 11.

In order to check the performance of the MEMS switches, we built a new passive loopback card using these in place of the mechanical relays (otherwise the designs were very similar to that shown in Figures 7 and 8). The new card using MEMS exhibited similar performance to the earlier design as shown in Figure 12 (compare to Figure 10). Although the jitter and loss characteristics are similar to those of

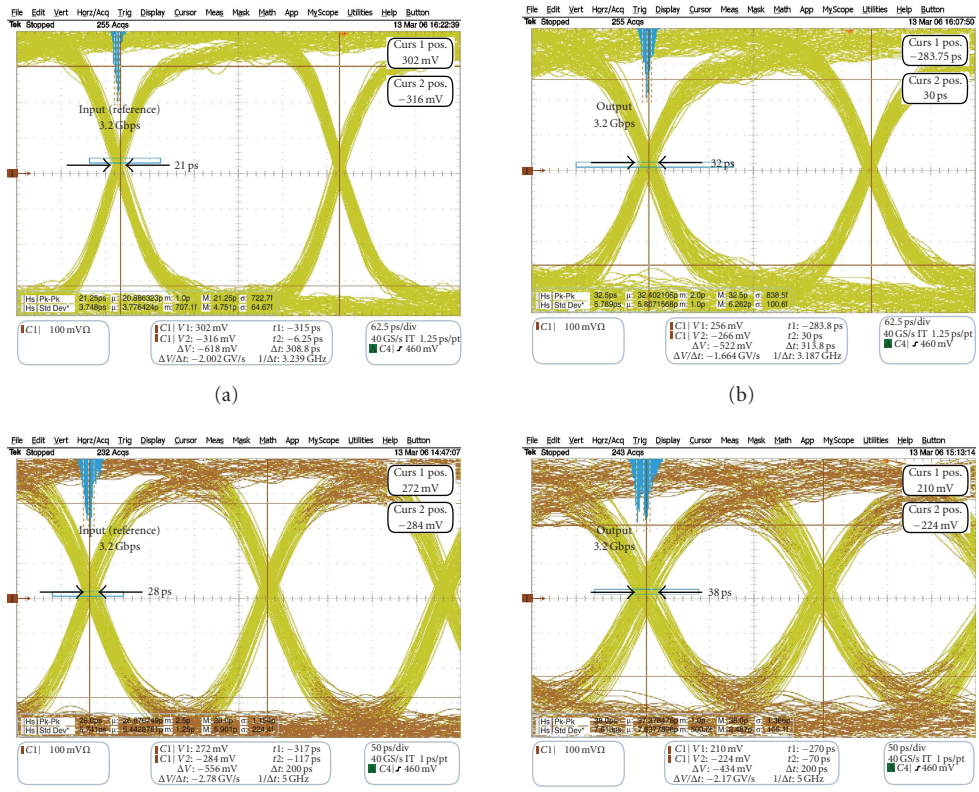

FIGURE 10: Individual card performance of a 2-card passive loopback configuration, using *mechanical RF relays*.

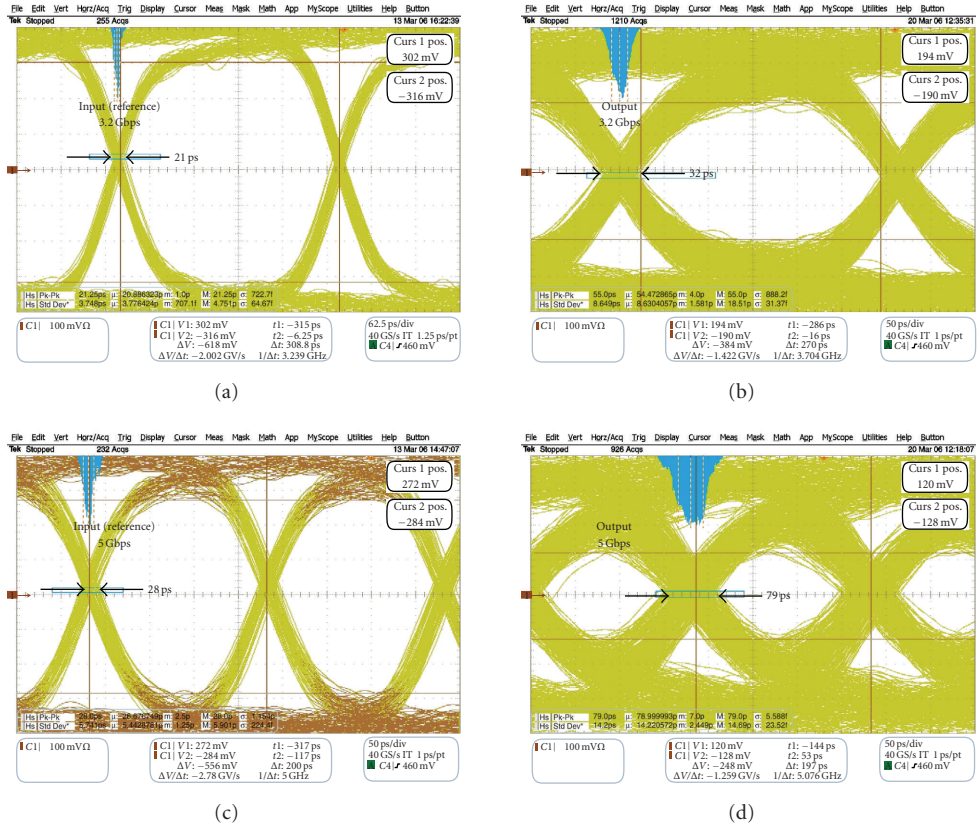

FIGURE 11: Full 2-card performance using *mechanical relays*.

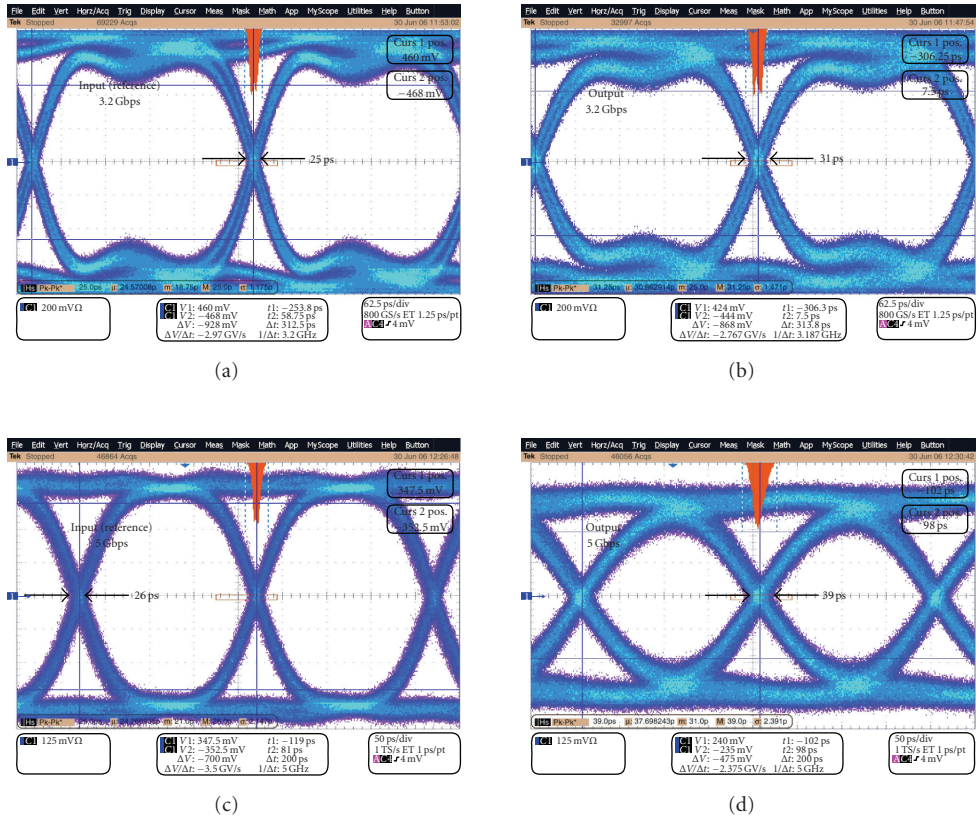

FIGURE 12: Individual card performance of a 2-card passive loopback configuration, *using MEMS relays* (compare to Figure 10).

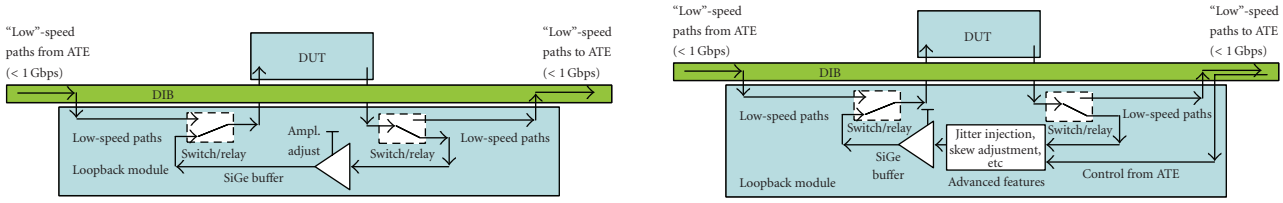

FIGURE 13: (a) The basic *active* loopback configuration and (b) active loopback with advanced features.

the mechanical relay card, there is a big improvement in power dissipation (much lower) and a significant reduction in module thickness.

Even though these passive loopback cards were able to pass data at rates up to 5 Gbps and beyond, the signal amplitude was increasingly attenuated above 3.2 Gbps. To provide full performance at higher rates required the use of *active* circuits, as shown in the next section.

5. ACTIVE LOOPBACK MODULE PERFORMANCE

As we saw in Section 4, the performance of passive loopback cards is somewhat limited by the dielectric and skin-effect losses. In some applications these losses are realistic and/or can be tolerated (i.e., when the input receivers have high sensitivity). However, in other cases we desire to recover the full amplitude signal before transmitting back to the DUT. This requires an *active* circuit, typically a buffer or amplifier. If a variable amplitude buffer/amplifier is used, then we can adjust the amplitude to emulate either small- or large-signal situations. For instance, this can be used to measure or screen for input sensitivity.

This basic "active loopback" configuration is shown in Figure 13(a). In our cards we have utilized commercially-available SiGe buffers with variable amplitude adjustment (100 mV to 700 mV) in order to handle data rates up to ~7 Gbps. Only about 10 picoseconds of skew is introduced throughout this range. We can also include features such as jitter injection, preemphasis, skew adjustment, and so forth depending on the type of testing required. This is illustrated

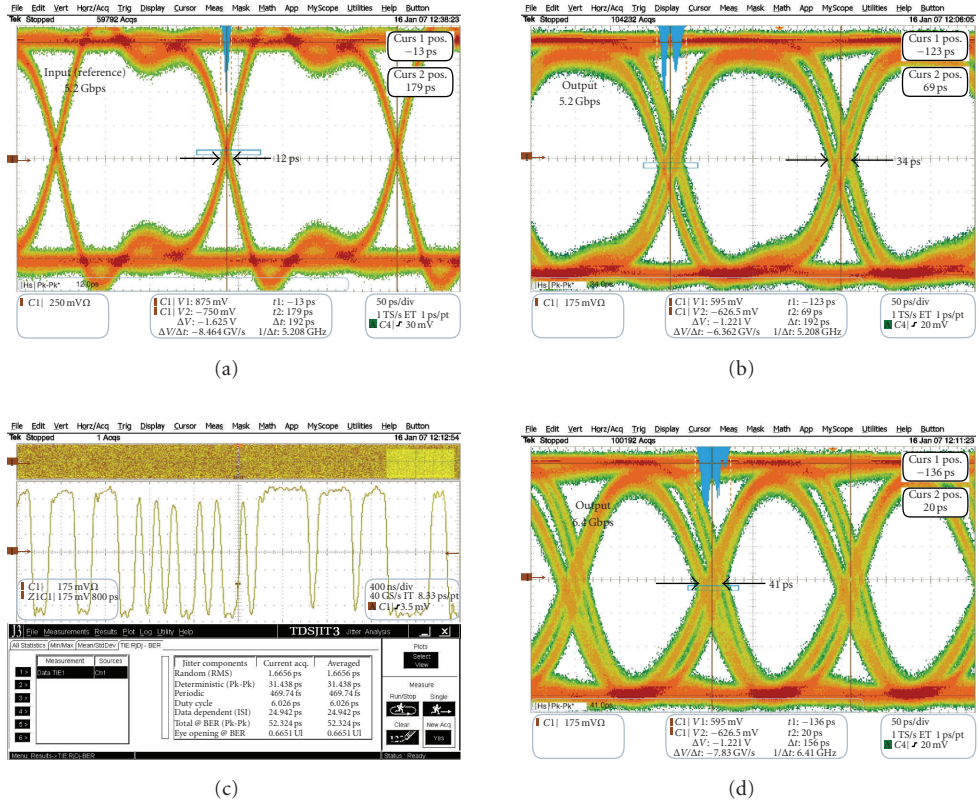

Figure 14: HyperTransport3 active loopback performance at 5.2 Gbps and 6.4 Gbps. Jitter analysis is at 6.4 Gbps.

in Figure 13(b). Such features may be implemented in future designs using SiGe logic technology.

To support HyperTransport3 loopback testing, we have constructed a 16-channel active loopback card, with each channel having a variable-amplitude differential SiGe buffer (as in Figure 13(a)). The entire card has an adjustable DC offset for matching to the DUT characteristics.

The typical performance (data eye diagrams) for one of the HyperTransport3 active loopback channels is shown in Figure 14 for both 5.2 Gbps and 6.4 Gbps. It can be seen that this card provides exceptionally good performance up to the target test rate of 5.2 Gbps and even to 6.4 Gbps. The channels add about 22 picoseconds to the total jitter. A detailed jitter analysis shows that RJ = 1.66 picoseconds, DJ = 31 picoseconds, and TJ = 52 picoseconds at BER = 10^{-12}.The card actually functions up to 8.0 Gbps, with gradually degrading data eyes above 6.4 Gbps. We have measured *channel-to-channel skew* across all 16 channels to be *less than 10 picoseconds*.

6. LIMITATIONS AND DISCUSSIONS

While the loopback cards demonstrated here met their target performance objectives, between 3.2 and 6.4 Gbps, it is clear that more work is required to handle higher rates (10 Gbps and above). Even with our best efforts, we are not able to completely eliminate jitter. As we increase frequency, the significance of "small" jitter increases and can pose the limiting obstacle to achieve these speeds. Future development is required to realize some "advanced" loopback features that we have suggested, such as jitter injection, deskew, preemphasis, and so forth.

As small as the current MEMS switch is, it is still not small enough for extreme applications involving hundreds of loopback channels. On the other hand, the fundamental MEMS technology lends itself to higher levels of integration, which therefore promises to solve this problem in the near future. Also, a higher-performance MEMS switch has recently been introduced by TeraVicta that has <0.4 dB insertion loss from DC to >20 GHz [8]. This level of performance will be required for loopback testing above 10 Gbps.

7. CONCLUSIONS

In this paper, we have shown that loopback testing of multi-Gigahertz devices can be enhanced by using MEMS switches and SiGe logic devices. The modular approach provides a high degree of flexibility. Achieving low-distortion signals at 5 Gbps and 6.4 Gbps requires careful attention to details within the module design, including the choice of relays, connectors, and logic components. Very careful attention to transmission line design is necessary to achieve picosecond delay matching and impedance matching. Newly developed

MEMS switches provide higher bandwidth and smaller size compared to traditional relays. Readily available SiGe logic can be used to configure a variety of active loopback structures that exhibit minimal losses up to 6.4 Gbps.

ACKNOWLEDGMENTS

This work was conducted as a joint R&D project between Georgia Tech and IBM Canada. The authors are grateful to IBM engineers for their efforts in designing, constructing, and testing the thermal management systems. The system-level experiments, characterization, and debug were conducted using equipment at the IBM Canada facility.

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Research Article

A Dependable Microelectronic Peptide Synthesizer Using Electrode Data

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The research in the area of microelectronic fluidic devices for biomedical applications is rapidly growing. As faults in these devices can have serious personal implications, a system is presented which includes fault tolerance with respect to the synthesized biomaterials (peptides). It can employ presence and purity detection of peptide droplets via current (charge) tests of control electrodes or impedance (phase) measurements using direct sensing electrodes near the peptide collector area. The commercial multielectrode array performs better in pure and impure detection of peptides in impedance and phase. Our two-electrode X-MEF case shows slightly poorer results. In both cases the phase is the best choice for contents detection. If there are presence or purity problems, the location is marked, and repeated peptide synthesis at another collector site is initiated.

1. INTRODUCTION

There is a rapid increase in with the complex control and massive signal processing nowadays available in advanced CMOS technology [1]. This development is especially of importance in life-science applications. However, in these applications, usually strict regulations are applied in terms of patient safety and the quality of materials used.

In a previous paper, we have suggested the implementation of a new droplet-based peptide synthesizer for point-of-care diagnostics using a new advanced heterogeneous technology, combining automotive SoC and fluidics technology [2]. As defects in these devices can have serious personal implications, like an incorrect initial diagnosis of cancer or virus, a system is presented in this paper which includes fault tolerance with respect to the quality of synthesized (peptide) biomaterials.

Our approach employs new presence and purity detection of peptide droplets via current or impedance measurements using either *control* or *direct sensing* electrodes near the peptide collector area. In the case of droplet presence or purity problems, the location is marked in the embedded RAM-based database, and repeated synthesis at the same or another site is initiated.

2. PEPTIDE SYNTHESIS

Our previously presented microelectronic fluidic (MEF) device [2] is able to synthesize many peptides via the conventional Fmoc method, but at a *micro*scale. This new device is fully software programmable, via a dedicated on-chip processor tailored for massive parallel fluidic operations and calculations.

As a demonstrator, we have studied a peptide consisting of nine amino acid elements (9-chain).

AMLDLLKSV

This particular antigenic peptide is being used for the detection of soft tissue sarcoma (STS), a form of cancer [3].

Because in the normal process of peptide synthesis some amino acids may be less efficient in peptide coupling reactions (between 5% and maximum 20%), we have compared

the previous "pure" peptide with the following *potential side-product, the* 8-mer peptide.

AMDLLKSV

This 8-mer potential impurity may be considered as an altered peptide ligand (APL) [4], a nonimmunogenic modification of the original antigenic peptide. The *immune response* of a T-cell (category of white blood cells in blood) is crucial for cancer detection as it recognizes the presented antigenic peptide. For details is referred to the general biomedical literature. An APL will only rarely cause this immune response and together with the requirement of sufficient volume, it is hence unlikely to result in a false alarm with regard to cancer detection.

In the normal case, peptide binding and cancer cell detection takes place in two steps: first, the MHC tetramers (set of molecules displayed on cell surfaces that are responsible for antigen presentation) have to be charged with peptide, and after a sufficient amount of MHC tetramers have been loaded with *antigenic* peptide, they will interact with the T-cell receptor of cancer cell specific T-cells indicating the presence of cancer cells that present this particular antigen.

As a result, it is not important to determine *which* APLs are involved (test all kind of chain permutations) or how much (volume percentage), but rather take care that sufficient (10 nmol) pure peptides are present to guarantee correct immune response detection. Any deviation exceeding the pure peptide measurement error (<1%) will result in the setting of a flag in our software. This flag will start up our fault tolerance procedure as discussed in Section 6. Subsequent proper action can be choosing another peptide collector site and start afresh, or enhancing the current site with more pure peptides and remeasure.

3. PEPTIDE PRESENCE AND PURITY TESTS VIA CONTROL AND DIRECT SENSING ELECTRODE MEASUREMENTS

It has been shown in the past, that there is a direct relationship between the degree of binding of amino acids in a peptide using solid-phase synthesis and the peptide conductivity [5]. Hence, one approach to detect the purity of a peptide is to measure the *conductivity* of the fluid containing the peptide by using *direct sensing* electrodes. The latter means there is a direct contact between the electrodes and the biofluid. In [5], the electronics for measuring this *conductance* have been suggested; it uses discrete operational amplifiers and passive components to achieve its goal.

As an alternative approach, the change in dielectric value of a pure/impure peptide droplet could be used for this purpose [6, 7]. This employs capacitive *control* electrodes (not in direct contact with the fluid) and further requires RF sources. However, this would result in a complex implementation on a chip.

We will discuss our two new test methods: one using (capacitive) *control* electrodes and transient current sensors as test infrastructure, while in the other approach, *direct sensing* electrodes measuring the phase at low frequencies is being used. Together, they form a powerful evaluation set in order to obtain a dependable MEF device.

4. TESTS BASED ON CONTROL ELECTRODE AND DIRECT SENSING ELECTRODE INFRASTRUCTURES

At the end of the peptide synthesis cycle, it has been shown to be of key importance to be able to detect the presence and purity of the produced peptides on the MEF top substrate [2]. Instead of the traditional chemical method in *macro*synthesis, we intended to use some electrical way for on-chip peptide presence and purity detection. Two methods are proposed in this paper: using the droplet *control* electrodes or the *direct sensing* electrodes; they can also be used simultaneously.

Both methods have been evaluated by actual measurements on our MEF, and for direct sensing, our MEF device and a commercial multielectrode array (MEA) device [8, 9] have been used for comparison. The base solution for dissolving the peptides was 0.1% TFA. This is Triflouroacetic acid, usually employed for peptide cleavage at the last step of peptide synthesis. The droplets containing these target peptides for the pure and impure cases have a concentration of 0.5 mmol/L.

During the measurements, three droplet cases have been considered. They are 0.1% pure TFA, 0.1% TFA with pure peptide, and 0.1% TFA with impure peptide; hence only the solution contents changes, from pure TFA to a TFA mixture with peptide. The measurement methods and results will be separately discussed for both types of electrodes.

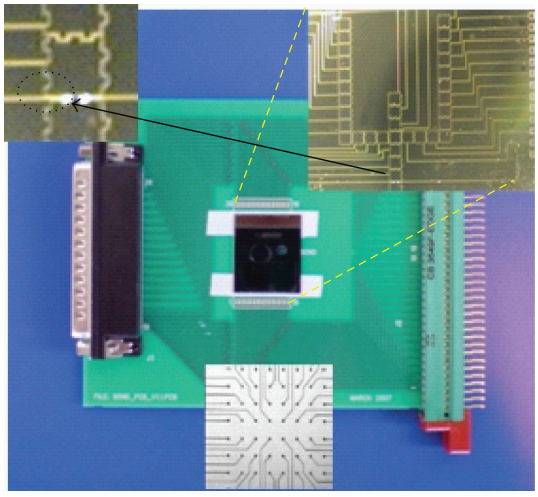
4.1. Control electrode measurements

Our microfluidic X-MEF chip, wire-bonded on a PCB which has been used in the test experiments, is shown in Figure 1(a) (top right).

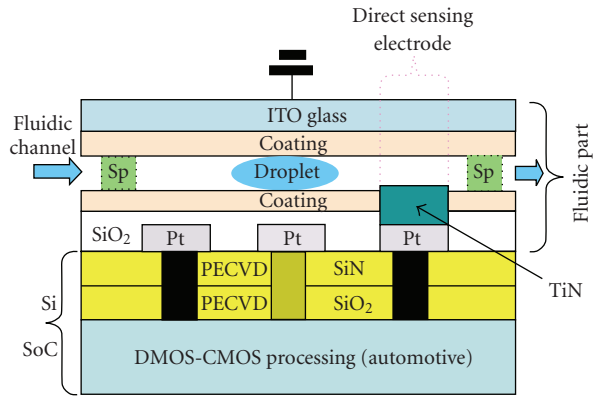
The top left of the figure shows both the control (serrated edged rectangles) and direct sensing electrodes (two white dots) in that chip. They are accessible from the interface ports on the PCB.

The bottom of Figure 1(a) shows the second object of our measurements, being the multielectrode structure of a commercially available MEA device [8, 9].

This is a commercial design and not directly linked to our X-MEF design. However, it can serve to show if it is worthwhile to extend our *two*-direct sensing electrodes to *many* electrodes for the sake of increased measurement sensitivity. Figure 1(b) shows a cross-section of the combined fluidic SoC chip [2]. Basically, the fluidic part is built on top of an SoC using our proven interconnect technology. The SoC contains all (driver and measurement) electronics and digital signal processing (DSP) hardware. The control electrodes are made of Platinum, while the direct sensing electrodes use TiN. A photomicrograph of the layout of the fluidic part in the right top of Figure 1(a) shows two-droplet input channels (left & right), which merge in a third channel forming a cross. At the bottom end of this third channel, the green arrow indicates the location of the two-direct sensing



(a) Our X-MEF chip and PCB (top), and the commercially available MEA (bottom)



(b) Cross-section of the combined fluidic SoC chip

FIGURE 1: experimental PCB including our fluidic chip (X-MEF) for tests on direct sensing electrodes and control electrodes [1, 2].

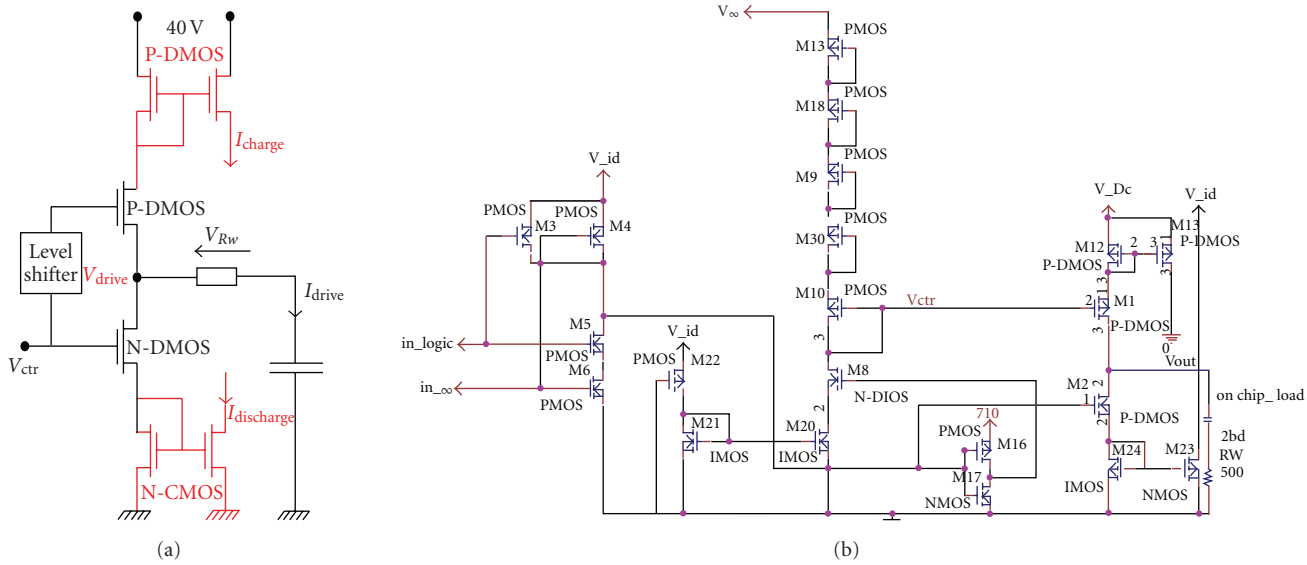


FIGURE 2: The DMOS-CMOS interface circuit schematics. (a) Basic principle of the DMOS-CMOS high-voltage driver. Red parts indicate the additional test hardware required for the peptide presence and purity detection. The capacitor represents the control electrode impedance. (b) Complete implemented DMOS-CMOS interface circuit scheme.

electrodes of which a detailed view is seen on the top left of Figure 1(a).

For droplet movement control, a DMOS-CMOS level shifter circuit was designed to "amplify" the digital control signals from a 3.3 V SoC control system into a higher voltage (40 V–80 V). This circuit is suitable to drive the control electrodes on the device and thus facilitate the transport and other operations of droplets. Besides their usage for transporting the droplets, the control electrodes can also be *reused* for detection purposes: capacitive sensing for the presence and contents of droplets.

Figure 2(a) shows the principle of the double-diffused MOS (DMOS) high-voltage driver used for droplet motion. The voltage V_{drive} is controlled by the control voltage V_{ctr}. When V_{drive} is applied, the electrode capacitance is charged through the P-DMOS transistor. It is subsequently discharged through the N-DMOS transistor when V_{drive} is switched off. The charge (or discharge) current I_{drive} is directly linked to the capacitance by

$$Q = C \cdot V_{\text{drive}} = \int I_{\text{drive}} \cdot dt = \int (V_{Rw}/Rw) \cdot dt, \qquad (1)$$

where Rw denotes the wire and itanium tin oxide (ITO) glass resistance from the top ITO plate (peptide collector site) to ground (Figure 1(b)) [2]. Its value is around 350 Ω. The transient voltage V_{Rw} across Rw was measured and recorded

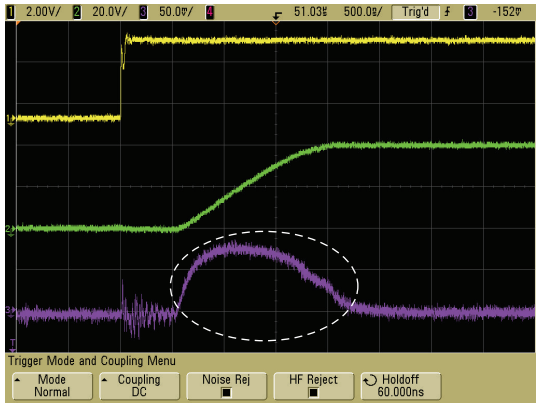


Figure 3: Actual transient measurement: rising edge control voltage V_{ctr} (yellow, 2 V per grid), V_{drive} (green, 20 V per grid), and V_{Rw} (purple, 50 mV per grid) for droplet with pure peptide.

using an oscilloscope in order to deduce the transient of current along the output path of the DMOS driver. The complete schematic of the DMOS-CMOS circuit, which we designed and implemented, is shown in Figure 2(b).

Therefore, our proposed architecture for presence and purity detection is based on the monitoring of the *(dis)charging current*. The latter can be duplicated by using a P-DMOS current mirror, while the discharge equivalent may be copied by an N-CMOS current mirror (red parts in Figure 2(a)).

The discharge current has been converted into a voltage via a transimpedance circuit and subsequently integrated; this result is then converted into a digital word via an 8-bit ADC. These parts have currently been implemented in a field-programmable analog array (FPAA). As for the purity test by impedance measurements later, the digital output value is then compared to the typical values of the pure peptides stored in an SRAM in the SoC.

Figure 3 shows part of the measurement results based on using the control electrodes in the case of only pure peptide droplets, according to Figure 2(a). Similar measurements were carried out with only the impure peptide droplets. These measurements of the transient voltage V_{Rw} have shown indeed that the charge current is linked to the purity of the peptides. Moreover, as the area under the purple curve is different in the case of pure and impure peptides, one can state that the electrode capacitance increases with the peptide purity.

Table 1 provides the results of using the structure in Figure 2 for purity detection, based on measurement data similar to Figure 3. The time interval (X-axis) was about 3 microseconds, and the charge through the top and bottom mirror parts of the driver circuit (Figure 2) at the rising and falling edge of the control voltage was compared for different droplet situations.

Table 1 shows that the top mirror under a rising edge of the control voltage resulted in the largest changes between pure and impure peptides. The results were reproducible and well within 1% tolerance. Presence detection (no solution) is very simple to implement.

Table 1: Percentage differences in measured values compared to pure peptide solution for top mirror (m12, m13) and bottom mirror (m23, m24) for rising and falling edge of the control voltage.

Condition	Top mirror, rising edge	Bottom mirror, falling edge
Pure peptide	0	0
Impure peptide	5,5%	4,1%
TFA solution	8,9%	7,0%
No solution	18,1%	14,3%

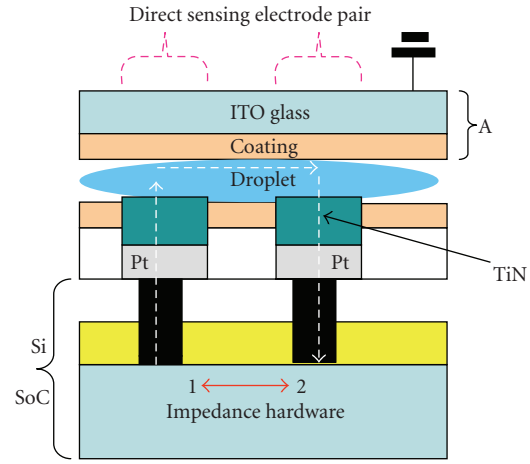


Figure 4: The direct sensing electrode pair infrastructure. The impedance is measured between nodes 1 and 2.

Hence our new structure based on control electrodes and transient current measurements could be used for our purposes. In the remaining part of this paper, we will investigate the merits of *direct sensing* electrodes in this respect.

4.2. *Direct sensing electrode measurements (X-MEF)*

Our second approach for presence and purity detection uses the direct sensor electrode *pair* of the X-MEF (Figure 1). A cross-section of this pair is presented in Figure 4; notice that the fluidic droplet flow, in contrast to Figure 1(b), is in this case perpendicular to the drawing. Impedance measurements have been carried out between the nodes 1 and 2 (Figure 4).

One can model this direct sensing electrode infrastructure as two-interfacial capacitances (C_{EDL}) in series with a solution resistance (R_{SOL}) and a solution capacitance (C_{SOL}) as shown in Figure 5. C_{EDL} represents the electrical double layer in the electrode-electrolyte interface dominating the interfacial impedance; for more details on direct sensing electrode modelling, especially for the MEA, [9] is useful.

The direct sensing electrode tests used a standard impedance setup. The test infrastructure consists of two Pt/TiN electrodes with dimensions of $50 \times 50\,\mu$m, making direct contact with an on-top droplet. Since the sensing

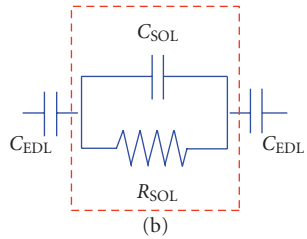


Figure 5: Simple component model of direct sensing electrode pair.

electrodes have direct contact with the droplet, impedance spectroscopy theories using the X-MEF can be applied [6, 7]. Hence we carried out impedance measurements instead of the (dis)charging method as discussed previously.

We used a Wayne Kerr precision impedance analyzer 6500 to analyze the impedance variation of the droplets containing different materials; the sweep frequency range was set from 1 kHz to 50 MHz.

In Figure 6(a), the actual measurement results are shown in case of a *pure* peptide. The top plot shows the impedance (10 Ω–1 MΩ scale), the lower plot depicts the phase (−80 deg–+40 deg scale) versus the frequency (1 kHz–50 MHz). Figure 6(b) presents the results of the impedance in all droplet content cases versus the frequency. If no fluid (e.g., peptide droplet) is present at the direct sensing electrode pair location, an (expected) pure capacitive behavior was observed and hence peptide droplet presence detection is extremely simple. A detailed graph in the case of droplet purity differences derived from Figure 6(b) is shown in Figure 6(c). Note that the frequency range was chosen here on the basis of the value of the phase most close to zero degrees because in that case the *droplet solution* content (Figure 5) is dominating other effects. At a frequency of 33 kHz, only a 1% impedance variation was observed between pure and impure peptides. This is in the range of the measurement tolerance (<1%) and can therefore not be used for purity detection.

Figures 6(d) and 6(e) show the same approach, but now in the case of the phase. The largest variations (17%, at 33 kHz) are found via the phase as compared to the previous impedance test with regard to purity/impurity detection.

This is therefore the preferred approach for impurity tests. The results were reproducible and well within acceptable tolerances (<1%) and hence usable for purity detection using the X-MEF direct sensing method.

An alternative multielectrode layout (now only *two* electrodes are used, Figure 1(a) top (left) is expected to enhance the measurement variations and accuracy even more; it will be investigated in future research work.

4.3. Direct sensing electrode measurements (MEA)

As a first step in that direction, we have also carried out similar tests with regard to a direct sensing electrode infrastructure of the multielectrode array (MEA) which is commercially available [8, 9].

This electrode infrastructure is shown in Figure 1(a) at the bottom. Although our tests are currently confined to two electrodes only, the multielectrode potential is clearly available.

The X-MEF cross-section in Figure 4 is easily converted into a two-electrode MEA infrastructure, by removing both the Si-SoC and A part.

Similar measurements using the same content *fluids* (not droplets!) were carried out on a *direct sensing* electrode *pair* in the MEA [8] (see Figure 1, bottom). The modelling of this infrastructure has been discussed in [9]. This experiment was carried out in order to see whether any similarities exist between the MEA and X-MEF, and in longer term, whether more electrode pairs could provide more reliable data on presence and contents of fluids/droplets.

Although the devices differ in amount of fluid used, distance between electrodes (layout) and used materials and electronics, trends should be similar.

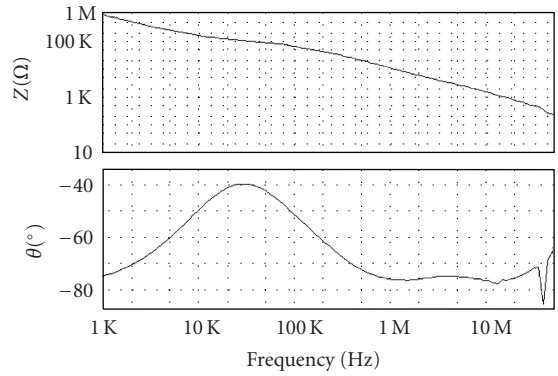
Figure 7(a) presents the measurement screenshot of impedance and phase in the case of a pure peptide *fluid* over a large frequency range. Figure 7(b) shows the measurements of the impedance for all possible fluid cases. It shows that the presence detection for a fluid (e.g., peptide) is very easy. A zoomed in representation of the impedance in Figure 7(c) reveals that the variation in pure and impure peptide contents is around 5.3% in the area of interest. Figure 7(d) shows the phase versus frequency for all fluid contents cases which indicates also a very simple detection of fluid presence. Figure 7(e) presents a zoomed in version of Figure 7(d); calculations show a variation of 20% in phase at 29 kHz between a pure and impure peptide fluid. Clearly, also in the case of the MEA, the largest variations are found via the phase with regard to purity/impurity detection. The results were reproducible and the measurement tolerances less than 1%.

When comparing the data in detail of Figures 6 and 7 of the XMEF and MEA, respectively, one can draw the following conclusions: the MEA performs better in pure and impure detection of peptides in impedance and phase, and the phase is the best parameter to be used. The X-MEF case shows somewhat poorer results, but also the phase is the best choice for contents detection. The difference in test frequencies and absolute values of impedance and phase stems from the difference in structure between the X-MEF and MEA.

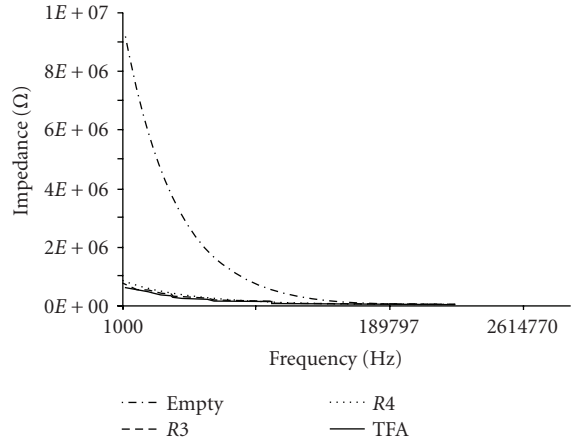
In the next two paragraphs will be elaborated how the previous measurements can be used to increase the dependability of the peptide synthesis process. First, the construction and location (collector) of the sensors are discussed in detail. After that, the results of these measurements are used to start up a new peptide synthesis sequence. This is implemented in software.

5. THE PEPTIDE COLLECTOR SITE

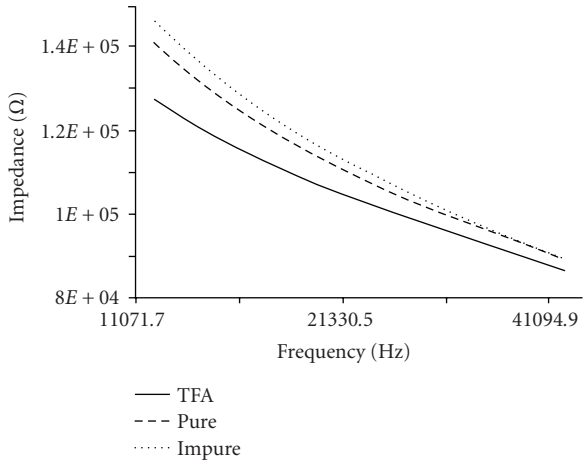
In a previous paper [2], several electrode configurations have been suggested for monitoring droplet presence and contents. The situation in our case is different, as the purity of the peptide has to be determined at a collector site. This collector site consists of a deep-etched trench in the top ITO



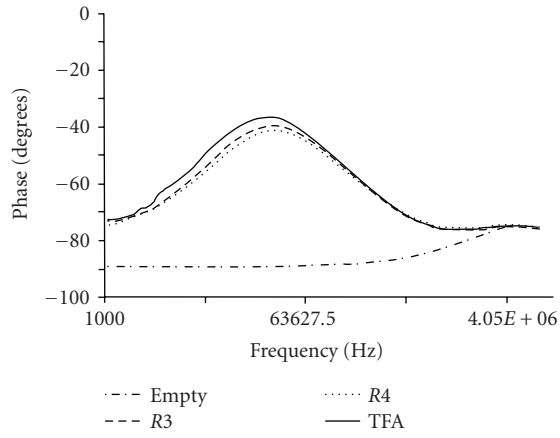
(a) X-MEF direct-sensing electrode pair measurement in the case of a pure peptide droplet. Impedance and phase versus frequency



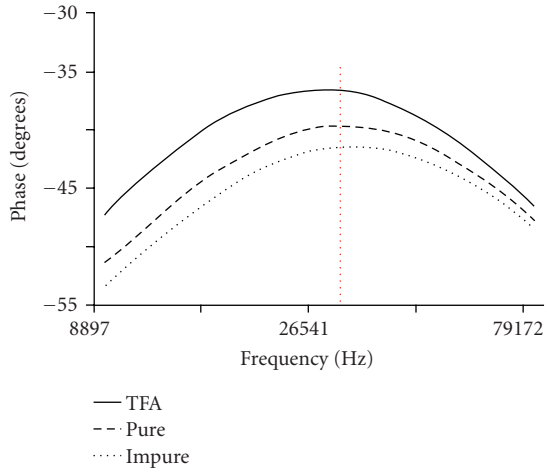
(b) Measured X-MEF direct-sensing electrode pair impedance in the case of droplet absence (empty), TFA, pure (R3), and impure (R4) peptide droplets



(c) Previous measurement zoomed in for the last three droplet cases under phase condition

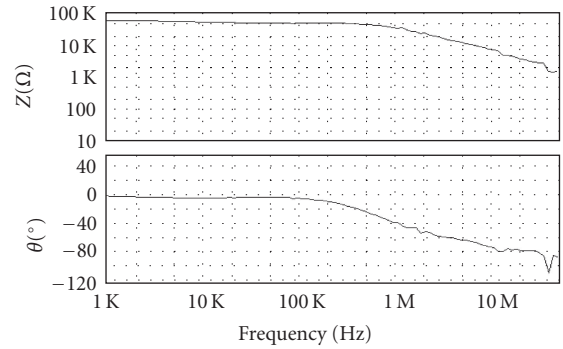


(d) Measurement of X-MEF direct sensing electrode pair phase in the case of droplet absence, TFA, pure (R3) and impure (R4) peptide droplets

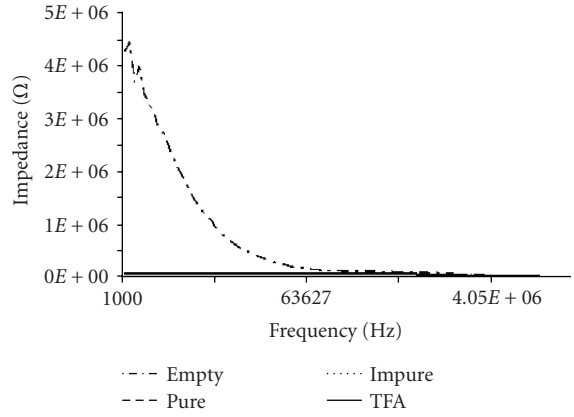


(e) Previous measurement zoomed in for the last three droplet cases under phase condition

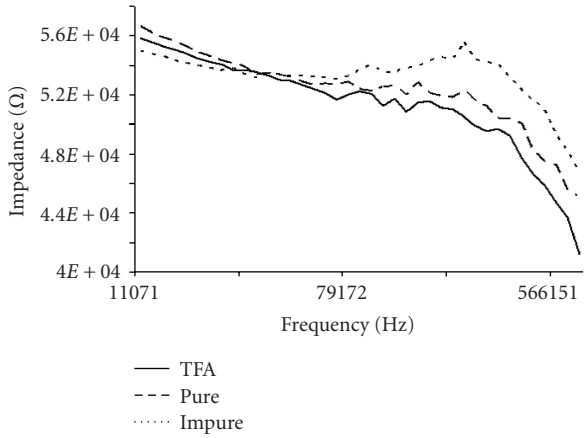
Figure 6: X-MEF measurement results from the direct sensing electrode pair infrastructure.



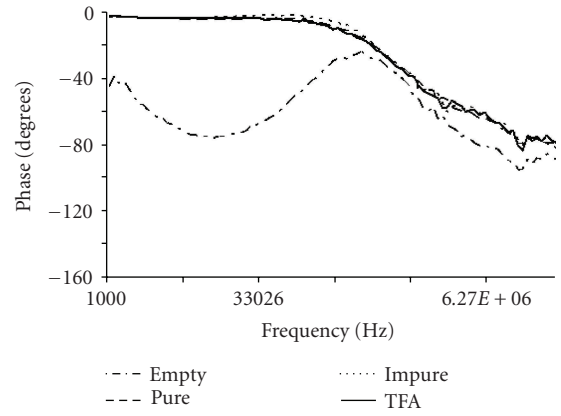
(a) MEA direct sensing electrode pair (62-63) measurement in the case of a pure peptide fluid. Impedance (10 Ω–100 kΩ scale) and phase (−120 deg–40 deg scale) versus frequency (1 kHz–50 MHz scale)



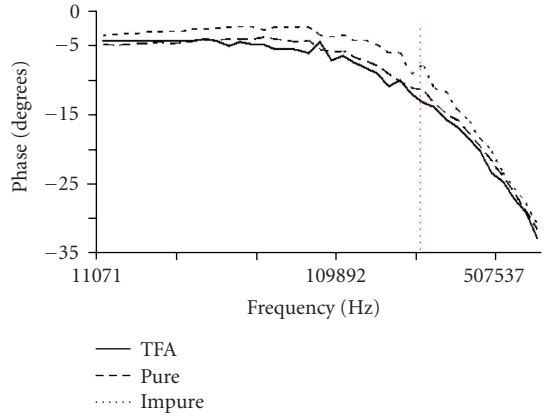
(b) Measured MEA direct sensing electrode pair impedance in the case of droplet absence (empty), TFA, pure, and impure peptide fluids (1 kHz–407 kHz frequency range)



(c) Previous measurements zoomed in for the last three droplet cases in the 11 kHz–70 kHz range



(d) MEA direct sensing electrode pair phase measurements in the case of droplet absence, TFA, pure, and impure peptide droplets (1 kHz–1.2 MHz frequency range)



(e) Previous phase measurements zoomed in for the last three droplet cases in the 11 kHz–70 kHz frequency range

Figure 7: MEA direct sensing electrode pair (electrode # 62 and # 63) measurements of impedance and phase.

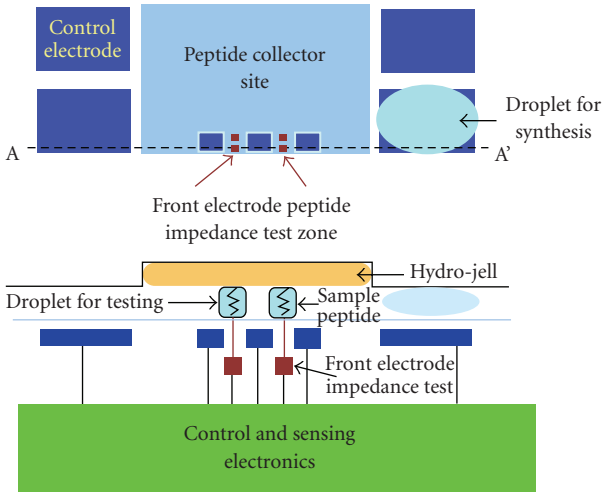


FIGURE 8: The direct sensing electrodes at the peptide collector site. Usage is made of special test droplets for purity detection.

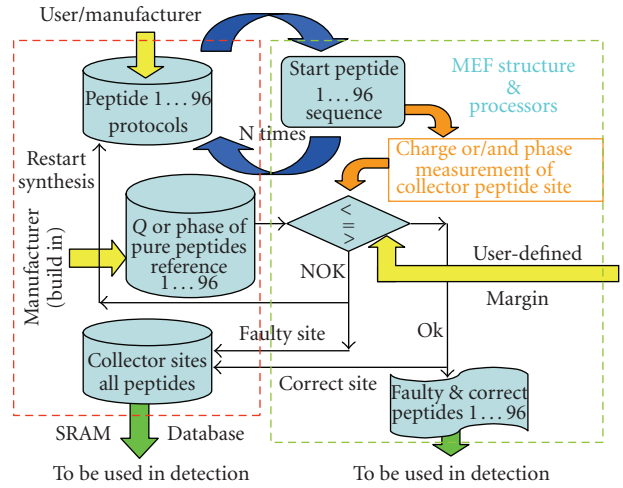


FIGURE 9: The handling of pure and impure peptide collector sites, employing the previous measurement techniques.

glass, and filled with a porous hydro gel. This approach is required to obtain sufficient peptide material for accurate cancer cell detection. Although a single pair of direct sensing electrodes can be used (shown in Figure 8, and used in the previous tests), also other, more complex options are open, as for example, like the ones used in an MEA as employed by QinetiQ [8]. Our current approach is depicted in Figure 8. The lower figure is the cross-section of A-A'.

Our system uses a special test droplet, which is smaller in dimensions than the ones during synthesis and consists of an acid solution, which cuts part of the peptide from the collector site. The droplet now contains the peptide; for enhancing the sensitivity three measurements are taken subsequently. The previously discussed tests at the chosen frequency (e.g., f_{lo} = 33 kHz) can be carried out by for instance a bridge structure [9].

6. FAULT TOLERANT PEPTIDE SYNTHESIS

The electronics in the SoC implementing the previous measurement system will send the droplet presence and contents information (based on control-electrode transient current or/and direct sensing electrode(s) phase) in digital form to our on-chip general processor (ARM), fluidic-specific coprocessor, and embedded RAM (Figure 9). Here, it will be decided if the deviation in measured peptide purity (or in worst-case absence) jeopardizes the correct (cancer or virus) detection. If so, the collector site is flagged and its location stored in the database. The digital information in terms of charge or phase of a specific pure peptide can be loaded in advance by the manufacturer, together with the measurement tolerance band and required boundary conditions (e.g., the frequency).

After flagging, a new round for synthesis will be initiated by the processor of that peptide, at either the *same* location or another site. Which decision is made depends on the measurement results. If no presence of peptides has been detected, probably the original collector site is unreachable or faulty and hence another free site will be allocated. If a large deviation (>10% margin, but software adjustable) from the pure peptide data has been detected, it is also decided to go to another site as the site can only contain a limited volume of fluids and a certain minimum is required for immune response. Only if a slight deviation (<5% margin, but software adjustable) is noticed from pure peptides, the same site will be used to add additional pure peptide via synthesis. This location information is also automatically stored and this means that a direct link exists between the original collector site, and the correct one; this is essential in the next optical step for cancer detection [10]. The simplified procedure is illustrated in Figure 9.

The user (or manufacturer) indicates which peptides have to be synthesized. These are specific to the cancer cells to be potentially detected. Currently, one can maximally provide 96 peptides on a single substrate. Multiple peptides are synthesized in parallel. By using our approach, a *dependable* MEF system results, which is a prerequisite for the application in a biomedical environment. All software has been written in C++ and runs on the on-board processor.

7. CONCLUSIONS

In this paper, two new test techniques have been investigated to determine the presence and purity of synthesized peptide droplets in our MEF and a commercial MEA via measuring the charge and phase of the biomaterial. Use is made of either direct sensing electrode pairs or control electrodes. It has been shown that detection is possible in both cases. The result is used to mark collector sites of insufficient pure peptides which could obscure cancer detection, and relate them to (a) pure site(s). In this way, the quality of cancer detection in this type of device is significantly increased, resulting in a *dependable* point-of-care device. Multielectrodes for sensing and additional DSP are seen as a possibility to further enhance the quality of measurements. A very strong point of our SoC-MEF approach is that the system is scalable in the

future to offer fully automatic dependable diagnosis in life sciences by on-the-fly specific peptide generation depending on previous diagnostic measurement results of the sample.

ACKNOWLEDGMENTS

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