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Contents

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Research Article

Optimal Sizing of a Hybrid Renewable Photovoltaic-Wind System-Based Microgrid Using Harris Hawk Optimizer

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Hybrid renewable energy microgrid has become an attractive solution to electrify urban areas. This research proposes a microgrid design problem including photovoltaic (PV) arrays, wind turbine, diesel, and batteries for which Harris hawk optimization (HHO), a metaheuristic technique, is applied. Based on a long-term techno-economic assessment, the HHO approach is used to determine the best hybrid microgrid size for a community in Saudi Arabia's northern region. The efficacy of HHO is investigated, and its performance was compared with seven metaheuristic techniques, grasshopper optimization algorithm (GOA), cuckoo search optimizer (CSO), genetic algorithm (GA), Big Bang–Big Crunch (BBBC), coyote optimizer, crow search, and butterfly optimization algorithm (BOA), to attain the HRE microgrid optimal sizing based on annualized system cost (ASC) reduction. Some benchmarks (optimum and worst solutions, mean, median, standard deviation, and rate of convergence) are used to distinguish and analyze the performance of these eight metaheuristic-based approaches. The HHO surpassed the other seven metaheuristic techniques in achieving the best HRE microgrid solution with the lowest ASC (USD 149229.9) followed by GOA (USD 149380.5) and CSO (USD 149382.5). The findings revealed that the HHO, GOA, CSO, and coyote have acceptable performance in terms of capturing the global solution and the speed of convergence, with only minimal oscillations. The BBBC, crow search, GA, and BA, on the other hand, have unacceptably poor performance, trapping to the local solution, oscillations, and a long convergence time. In terms of optimal solution and convergence rate, the BBBC and GA both perform poorly when compared to the other metaheuristic techniques.

1. Introduction

Renewable energy is the energy generated from naturally renewed resources. Unlike conventional resources, renewable energy resources are nondepletable energy sources. Renewable and reliable energy supplies are required by the world since they are significantly cleaner and create energy without polluting the environment [1]. Wind turbine (WT) generators, solar photovoltaic (PV), geothermal, biomass, and other renewable energy sources exist. Aside from their benefits like environmental friendliness and sustainability, wind and solar PV became increasingly popular because of lower production costs and increased applications for both commercial and residential [2]. These sources of power can be used independently or in combination to supply the utility grid with electrical power. Furthermore, renewable energy system-based microgrid is utilized to electrify remote locations that are not serviced by the utility grid. Owing to the unreliability and large size of employing a single source to supply electricity to remote sites, hybrid energy technologies have been intended to address these difficulties [3]. PVs, WTs, batteries, diesel generators, and fuel cells (FCs) are examples of hybrid renewable energy resources (HRERs). However, when renewable energy resources are employed to supply the off-grid sites with electricity, a challenge can be increased due to their nonlinear and erratic behavior [4]. Diminished reliability, control complexity, design considerations, instability, and lower energy are only a few of the challenges [5]. These problems are nonlinear and

complicated optimization problems. The action of making the best or most effective use of HRERs with the least cost is known as optimization [6, 7].

On hybrid renewable energy systems, a variety of optimization strategies are applied, including classical techniques and artificial intelligence (AI) techniques [8–10], hybrid techniques [11, 12], and software programs [13–15]. Analytical techniques [16, 17], graphical techniques [18, 19], statistics techniques [20], and numerical-based techniques [21] are examples of classical techniques. Although classical methods are straightforward, they have some constraints for defining the optimization issue. Graphical techniques, for example, rely on solar irradiance and wind speed information to estimate system sizing, which can lead to size issues (oversizing or undersizing) [22]. Analytical techniques are incapable of dealing with a lot of energy sources, and they take longer to compute than AI algorithms. On the other hand, other optimization algorithms like AI, hybrid computing, and software programs do not have the same constraints as classical techniques and can effectively tackle the optimization problems. The researchers are motivated to learn more about technical and economic feasibility difficulties by promoting more use of HRERs to supply the off-grid and on-grid rural remote regions. The HOMER PRO software application in [13–15] was used to conduct a techno-economic analysis. In [13], the authors investigated, assessed, and designed a technical and economic viability of solar PV-diesel-batteries for electrifying a town in Pakistan. Their approach makes use of the national grid's time-constrained availability. The HOMER PRO software tool was used to estimate the system optimal size and assess its techno-economic viability. According to the findings of this study, grid-integrated systems have a lower Cost of Energy (COE) than off-grid systems. The study in [14] used HOMER software program for remodeling and refinancing a rural microgrid on a Thai island. The system was designed to offer the lowest COE. In Benin, a research was conducted to look into the powering of rural villages; the hybrid PV-diesel-batteries was proven to be the most cost-effective [15].

The appropriate HRER sizing is unavoidable since oversizing increases the initial cost while undersizing reduces the shared power from the HRERs and, as a result, reduces system reliability. The use of AI approaches to size HRERs optimally has recently piqued the interest of most experts across the world. Some research examined single-objective models, whereas others investigated multiobjective models [8] [23–25]. To lower the annual cost of a hybrid PV-WT-battery system, the authors utilized a model based on a fuzzy logic [23]. The sizing of storage energy systems in renewable energy networks was optimized using a genetic algorithm (GA) in [8], limiting expected energy not supplied and power losses (PL). In [24], this study proposed an effective sizing technique for the component of the hybrid photovoltaic-WT-battery system according to GA and combined with an energy management strategy. The economic model/predictive control technique [26] was used to develop an energy management technique. The authors in [25] proposed a quasisteady operating approach combined with GA to achieve the best size of a PV-pump storage hydroelectric system according to both the loss of power supply probability (LPSP) and investment cost. In [27], a MATLAB framework for optimal size of a wind-hydro system based on lower COE and CO_2 emissions was developed. In order to reduce the total net present value, the authors implemented a model based on a mixed-integer linear programming modeling framework for attaining technical and economic optimum design of PV and energy storage systems [28]. The authors in [29] employed Particle Swarm Optimization (PSO) to design the best PV-WT-battery system according to reducing the total annual cost (TAC). Based on net present cost (NPC) minimization, GA was employed to address a multiobjective sizing issue for a PV-WT-battery-solar collector [30]. In [9], the authors modified a cuckoo search optimizer (CSO) for sizing PV-battery, WT-battery, and PV-WT-battery systems with the purpose of lowering overall system costs. The results revealed that the CSO generates higher-quality solutions and is faster to convergence than the PSO and GA approaches. The Pareto evolutionary algorithm was used by the authors in [31] to reduce the LCOE and CO_2 life cycle emissions (LCE) for a WT-PV-diesel-battery system. The PV-biogas-pump storage-battery system was designed using the Water Cycle Algorithm (WSA) and Moth-Flame Optimization (MFO) in [32]. The MFO approach and the WSA are assessed and compared to the GA. The differential evolution (DE) was combined with a fuzzy control by the authors in [33] to optimize the design of a PV-WT-diesel-hydrogen-battery system according to the least cost, emission, and unmet load. The authors in [34] proposed an improved Fruit Fly Optimizer (FFO) for designing a hybrid PV-WT-diesel-battery system with the lowest pollutant emission and TAC. The line-up competition algorithm was used in [35] to build an optimal PV-WT-diesel-battery system that minimized TAC and emissions of CO_2. In [36], the author used Grey Wolf Optimization (GWO) to determine the best size for a photovoltaic-WT-biomass system while reducing the TNPC and LPSP. The GWO method's results were compared to those of the GA and Simulated Annealing (SA) methods, demonstrating that the GWO method is superior. For attaining optimal sizing of the PV-WT-battery system, a hybrid Big Bang–Big Crunch (BBBC) was proposed in [37]. To identify the appropriate size for a PV-WT system by reducing the TAC, the authors of [38] employed an Ant Colony Optimization (ACO) algorithm. The authors of [39] applied a hybrid optimizer technique using two well-known metaheuristics: SA and Tabu Search to attain the best size of a small self-contained PV-WT-diesel-biodiesel generator-FC-battery power system to minimize the system's COE. The equilibrium optimizer performed well compared to bat optimizer, and Black Hole (BH) optimization was applied to size the energy systems a microgrid of a photovoltaic with FCs and battery storage energy systems to minimize the COE [40]. In [41], the best size of a PV/WT/battery/diesel microgrid has been attained using Bonobo optimization algorithm based on ASC reduction. The optimal sizing of a microgrid consisting of PV/WT/battery/diesel while satisfying the

LPSP and REF reliability measures was achieved by using an artificial ecosystem-based optimization algorithm [42]. In [43], a modified African vulture optimizer (IAVO) is proposed to identify the optimal configuration for a HRERs. The structure is composed of fuel cell, WT, and PV and its auxiliaries that include the electrolyzer and the storage system. The main target is to find the optimal configuration to minimize the LPSP and TNPC. In [44], a new optimization algorithm called converged krill herd (CKH) has been proposed for optimal size of a HRERs including battery and fuel cell to supply the driving force of a locomotive. The main goal is to minimize the total cost of the system while dealing with various constraints such as the battery capacity constraint and the fuel cell state-of-charge limit.

Based on the previous literature, this article was considered an early attempt to apply the Harris hawk optimization (HHO) technique to tackle the optimal design optimization problem in standalone microgrid. The HHO is applied to a highly constrained objective function that considers several important constraints, including power balancing, generation power capacities, LPSP, and renewable energy fraction (REF) restrictions. The effectiveness of applied HHO was investigated, and its performance was compared to that of seven metaheuristic techniques: grasshopper optimization algorithm (GOA), CSO [9], BBBC [37], coyote [45], crow search [46], GA [8], and butterfly optimization algorithm (BOA) [47] to achieve HRE microgrid optimal sizing with a quick convergence rate and the lowest annualized system cost (ASC). To empirically evaluate this, the following research questions were formulated: Does any algorithm perform significantly better than others for solving the optimal sizing problem? Is there any dependency between algorithm used and the initial population? Some benchmarks are used to distinguish and analyze the performance of these metaheuristic-based techniques. The HHO outperformed the other seven metaheuristic techniques in achieving the best HRE microgrid solution, with the lowest ASC (USD 149229.9) followed by GOA (USD 149380.5) and CSO (USD 149382.5), respectively. The proposed HHO technique could be useful for a wide range of optimization challenges in the power and energy industries. According to the findings, the HHO, GOA, CSO, and coyote have appropriate global solution capture and convergence rates with low oscillations. The BBBC, crow search, GA, and BA, on the other hand, perform poorly, with trapping to the local solution, oscillations, and a long convergence time. The BBBC and GA both perform poorly in terms of optimal solution and convergence rate when compared to other metaheuristic approaches.

The remainder of the paper is organized as follows. The PV, WT, battery, and diesel generators are all mathematically modelled in Section 2. The objective function and constraints of the problem formulation are presented in Section 3. The proposed HHO technique is discussed in Section 4. Section 5 includes the simulation results as well as discussions. The article is finally concluded in Section 6.

2. Proposed Hybrid Photovoltaic-Wind Energy Microgrid

The proposed microgrid configuration is shown in Figure 1. WT and PV arrays are the system's principal energy sources. The AC bus bar is connected to the WTs and diesel generator, while the DC bus bar is interconnected to the PV arrays and battery banks. The bidirectional DC/AC converter serves as both an inverter and a rectification bridge, converting DC to AC power and AC to DC power. When renewable generation sources cannot fully meet the load, the battery banks are used to provide backup power. Diesel generators serve as a backup power source when neither the WTs nor the PV arrays can generate output power, and the batteries are depleted. The load to be supplied is assessed using real-world data collected in an isolated community named Al-Sulaymaniyah (within Arar region in Saudi Arabia), where the load is currently served by diesel generator units. The optimization trend tries to reduce the planned proposed hybrid microgrid net present cost (NPC).

The NPC can be estimated using the following formula:

$$\mathrm{NPC} = \mathrm{ASC}\frac{(1+i)^{Y_{\mathrm{proj}}}-1}{i(1+i)^{Y_{\mathrm{proj}}}}, \tag{1}$$

where i is the interest rate per year and Y_{proj} is the lifetime of the project.

The annualized cost of each unit is equivalent to the annualized costs of its capital investment (C_{acap}), as well as its annualized operating and maintenance cost (C_{amain}) and annualized replacement costs (C_{arep}) as shown in the following equation [48]:

$$\mathrm{ASC} = C_{\mathrm{acap}} + C_{\mathrm{arep}} + C_{\mathrm{amain}}. \tag{2}$$

The capital cost can be expressed as in the following form:

$$C_{\mathrm{acap}} = (C_{\mathrm{ren.}} + C_{\mathrm{Batt}} + C_{\mathrm{DG}})\frac{i(1+i)^{Y_{\mathrm{proj}}}}{(1+i)^{Y_{\mathrm{proj}}}-1}, \tag{3}$$

where $C_{\mathrm{ren.}}$ is the renewable capital costs, C_{Batt} is the battery capital costs, and C_{DG} is the capital costs of the diesel generator.

The mathematical modelling for each of the microgrid components used in this study is described in the subsections below.

2.1. Modeling of the PV Array. The PV array's output power is determined by incident solar radiation, temperature, and the PV array's manufacturer's data as follows [48]:

$$P_{\mathrm{PV}} = P_r f_{\mathrm{PV}}\left(\frac{\overline{G_T}}{\overline{G_{T,\mathrm{STC}}}}\right)(1+\alpha_P(T_c - T_{c,\mathrm{STC}})), \tag{4}$$

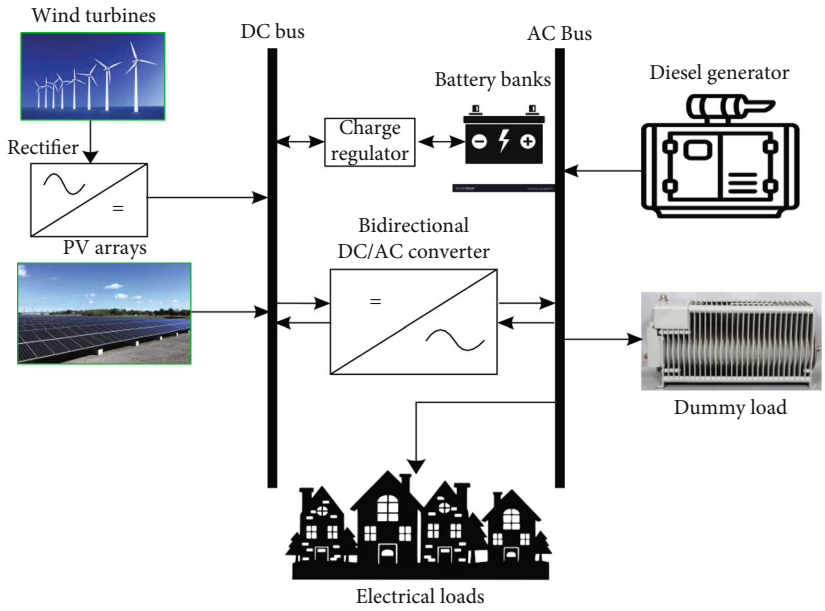

Figure 1: Configuration of the proposed PV-WT-diesel-battery microgrid.

where P_r is the nominal photovoltaic power. $\overline{G_{T,\mathrm{STC}}}$ is the global photovoltaic irradiance under STCs. $\overline{G_T}$ is the global solar irradiance under normal conditions. $T_{c,\mathrm{STC}}$ is the PV temperature under STCs. T_c is the PV temperature under normal conditions. f_{PV} is the derating coefficient. α_P is the temperature coefficient of power.

The PV's steady-state temperature is calculated using the following equation [48]:

$$T_c = \frac{T_a + (\mathrm{NOCT} - T_{a,\mathrm{NOCT}})(1 - 1.11\eta_{\mathrm{MPP}}(1 - \alpha_P T_{c,\mathrm{STC}}))\left(\overline{G_T}/G_{T,\mathrm{NOCT}}\right)}{1 + 1.11\left(\alpha_P \eta_{\mathrm{MPP,STC}}\right)(\mathrm{NOCT} - T_{a,\mathrm{NOCT}})\left(\overline{G_T}/G_{T,\mathrm{NOCT}}\right)}, \tag{5}$$

where T_a is the PV ambient operating cell temperature. NOCT is the PV nominal operating cell temperature. $T_{a,\mathrm{NOCT}}$ is the PV ambient temperature under NOCT. $G_{T,\mathrm{NOCT}}$ is the solar irradiance under NOCT. $\eta_{\mathrm{MPP,STC}}$ is the MPP efficiency of PV under STCs. η_{MPP} is the PV-MPP efficiency.

2.2. Modeling of the Wind Generator. The WTs' output power is determined by the following equation:

$$P_{\mathrm{WT}}(u) = P_r \times \begin{cases} 0, & u < u_c \text{ or } u > u_f, \\ \dfrac{u^2 - u_c^2}{u_r^2 - u_c^2}, & u_c \le u \le u_r, \\ 1, & u_r \le u \le u_f, \end{cases} \tag{6}$$

where P_r is WT rated power, u_c is the starting speed, u_r is the rated speed, and u_f is the furling speed. The power generated by WT is dependent on four parameters: P_r, u_c, u_r, and u_f as shown in Equation (6). The WT power curve based on a nonlinear model is shown in Figure 2. There is no power generated when the wind speed is less than u_c or greater than u_c. The WT generator starts to generate power once the wind speed becomes greater than u_c and reaches to the rated power at the rated speed. The power generated from the WT becomes fixed at the rated power when the wind speed is greater than u_r and less than u_f.

2.3. Modeling of the Battery Bank. All hybrid microgrids require some form of energy storage. This is attributed to the reason that renewable energy resources' output power is uncertain due to their erratic and intermittent climatic conditions. The total amount of energy supplied determines the state of charge (SOC), which can be calculated by the following formula [49, 50]:

$$\mathrm{SOC}(t) = \mathrm{SOC}(t-1)(1-\sigma) + \left(E_{\mathrm{GA}}(t) - \frac{E_L(t)}{\eta_{\mathrm{inv}}}\right)\eta_{\mathrm{battery}}, \tag{7}$$

where σ is the rate of self-discharging; $E(t)$ is the overall output power; $E_L(t)$ is the load demand; and η_{inv} and η are the inverter efficiency and battery's charge efficiency, respectively. The SOC limit cannot be smaller than the battery's minimum permitted level ($\mathrm{SOC}_{\mathrm{min}}$). The SOC cannot exceed

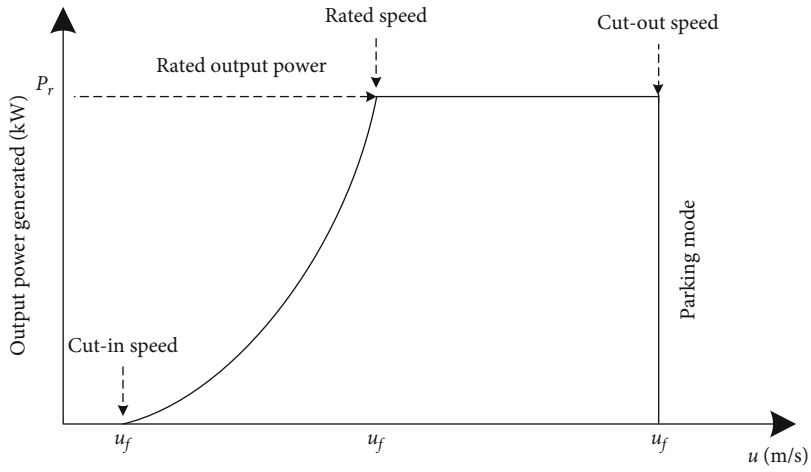

Figure 2: Power characteristic curve of a WT.

the maximum allowable level (SOC_{max}) during a charging process. These SOC constraints can be expressed as follows:

$$SOC(t) = \begin{cases} SOC_{min}, & SOC(t) < SOC_{min}, \\ SOC(t) & SOC_{min} < SOC(t) < SOC_{max}, \\ SOC_{max} & SOC(t) > SOC_{max}. \end{cases} \tag{8}$$

2.4. Modeling of the Diesel Generator. A diesel generator performs the role of the tertiary source in a hybrid microgrid, eliminating the necessity for storing energy. As a result, it is crucial for regional and remote load systems to keep running. It also helps make the system more reliable and cost-effective. The diesel generator is primarily used during periods of peak demand and battery depletion due to its low efficiency load rate. Therefore, when constructing a hybrid microgrid, it is important to keep in mind that the diesel generator should not run under low load or at all. The annual fuel cost and power generated can be estimated using the following equation:

$$C_{DG} = C_F \sum_{t=1}^{8760} AP_{DG}(t) + BP_R, \tag{9}$$

where P_{DG} and P_R are the rated power and power generated of the diesel generator, respectively. The values of A and B in this investigation are 0.246 and 0.08415, respectively.

2.5. Energy Management Strategy. The proposed hybrid microgrid is regulated by the following conditions:

(a) PV and WT are the microgrid's principal sources of power

(b) When the power generated from PV and WT surpasses the capacity demands, the batteries are charged. The excess power is discharged after the battery is fully charged. If the demand is more than the generated power from the renewable energy resources, the load that is not provided is met by the battery if its available energy is more than its minimum capacity

(c) As a last choice, a diesel generator is used, if

(i) the load shortage is less than the diesel generator's minimum permitted power, diesel generator will serve at its minimum permissible power, and the excess power will be dumped

(ii) the load not supplied is delivered by the diesel generator if it is higher than the minimum permissible level and less than its nominal power. If the remaining load is higher than the nominal power, diesel generator will function at that power level, and the load not delivered will come from the battery if the storage capacity is sufficient

Based on these conditions, Algorithm 1 presents the appropriate energy management technique.

3. Problem Formulation

The objective of the microgrid optimization problem is to lower the ASC while maintaining a specific level of reliability, in this case LPSP. In this study, the best microgrid design has been defined as a constrained objective function:

$$\min \text{ ASC}$$
$$\text{subject to : } \begin{cases} LPSP \le LPSP_{desired} \\ REF \le REF_{desired} \\ 0 \le P_{PV} \le P_{PV,max} \\ 0 \le P_{WT} \le P_{WTG,max} \\ 0 \le P_{Batt} \le P_{Batt,max} \\ 0 \le P_{Dsl} \le P_{Dsl,max} \end{cases} \tag{10}$$

```
IF energy generated E(t) is enough to supply load E_L(t), THEN
   Supply the load and charge the battery if possible
ELSE
   IF battery is charged (SOC > SOC_min), THEN
      Use battery banks to supply the load
         IF battery is not enough (SOC < SOC_min), THEN
            Run diesel generator along with battery
         END
      ELSE
         Run diesel generator only to supply the load
      END
END
```

Algorithm 1: Pseudocode of the proposed energy management algorithm.

where $\mathrm{LPSP}_{\mathrm{desired}}$ and $\mathrm{REF}_{\mathrm{desired}}$ are the reliability and REF levels selected by the user. The rated power of the PV, WT, and diesel generator (in kW) is represented by P_{PV}, P_{WTG}, and P_{Dsl}, respectively. The capacity of the battery bank is P_{Bat} (in kWh). The maximum rating of the PV, WTs, batteries, and diesel is represented by $P_{\mathrm{PV,max}}$, $P_{\mathrm{WT,max}}$, $P_{\mathrm{Bat,max}}$, and $P_{\mathrm{Diesel,max}}$. The optimal values of the PV, WT, and nominal power of the diesel generator, as well as battery storage capacity, are determined based on the minimum ASC value as follows:

$$x = [P_{\mathrm{PV}}, P_{\mathrm{WT}}, P_{\mathrm{Diesel}}, P_{\mathrm{Bat}}]. \tag{11}$$

3.1. Modeling of LPSP. The LPSP is a vital aspect in establishing the microgrid's successful reliability. The risk that the microgrid's available power will be insufficient to fulfill the total demand level is specified as the LPSP. The following equation is a representation of the LPSP:

$$\mathrm{LPSP} = \frac{\sum_{t=0}^{T} \mathrm{Power\ outage\ Time}}{T}. \tag{12}$$

A LPSP value of zero means the load has always been delivered, whereas a value of one means the load will not be supplied. The duration of time during which a load demand is not met is known as the power outage time (POT).

3.2. Renewable Energy Fraction. The renewable energy fraction (REF) is a terminology that refers to the total amount of renewable energy delivered to load demand, as seen in the following equation [48]:

$$\mathrm{REF} = \left(1 - \frac{E_{\mathrm{diesel}}}{E_{L,\mathrm{served}}}\right) \times 100, \tag{13}$$

where E_{diesel} is the total amount of power generated by diesel. A classical diesel generator system is equal to 0% of a REF, while a clean system is equal to 100% of a REF. The hybrid energy system is represented by the values ranging from 0% to 100%.

4. Harris Hawk Optimization Technique

The algorithm of HHO's exploitative and exploratory technique is used to solve the hybrid microgrid optimal design [51], which is inspired by the Harris hawk's aggressive attitude. Depending on the appropriate formulation problem, the HHO approach can be utilized to tackle a range of optimization problems. The various phases of HHO are depicted in Figure 3 [51], which are covered in the following subsections.

4.1. Exploratory Phase. Harris' hawks use their strong eyes to follow and detect prey; the prey may not always be easy to spot. As a result, the hawks wait, watch, and monitor the desert for long times in order to track a prey. The Harris' hawks are candidate solutions, and the best solution in each phase is regarded the intended prey or nearly so. Harris' hawks sit at random spots and wait for prey using one of two tactics. They roost in accordance with the positions of other members of the family and the rabbit, as represented in Equation (14) for $q < 0.5$, or roost on tall trees at random within the range, as formulated in Equation (14) for $q \geq 0.5$ [51].

$$X(t+1) = \begin{cases} X_{\mathrm{rand}}(t) - r_1 |X_{\mathrm{rand}}(t) - 2r_2 X(t)|, & q \geq 0.5, \\ (X_{\mathrm{rabbit}}(t) - X_m(t)) - r_3 (LB + r_4(\mathrm{UB} - \mathrm{LB})), & q < 0.5, \end{cases} \tag{14}$$

where $X(t+1)$ is the location of the hawks in the next iteration t. $X_{\mathrm{rabbit}}(t)$ is the location of the rabbit. $X(t)$ is the current location of the hawks, r_1, r_2, r_3, r_4. q is random numbers between $[0, 1]$. LB and UB are upper and lower boundaries. $X_{\mathrm{rand}}(t)$ is a random selection from the current population of hawks. X_m is the average position of hawks in the present population.

4.2. Exploitative Phase. The Harris hawks attack the targeted prey spotted in the prior phase in this phase, which is known as the surprise pounce. Preys, on the other hand, frequently strive to flee perilous situations. As a result, different chasing styles emerge in real-life settings. To represent the tackling stage, the HHO proposes four alternative techniques based on prey escaping performances and Harris' hawk pursuit

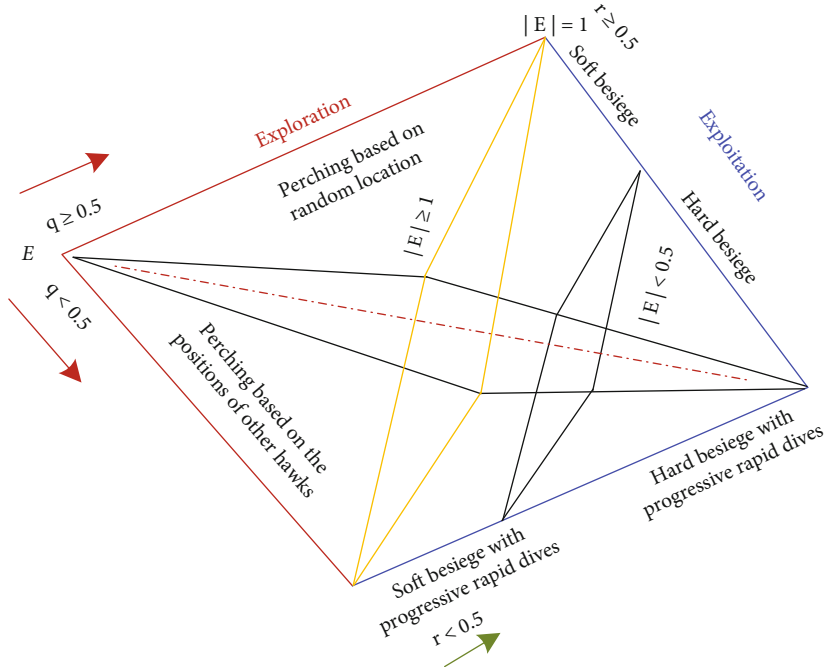

Figure 3: The Harris hawk optimization phases.

tactics. Preys are continually trying to flee from hazardous situations. Assume that r is the probability of a prey successfully fleeing ($r < 0.5$) or failing to flee ($r \geq 0.5$) before a surprise pounce. Hawks will engage in a harsh or soft besiege to capture the prey, regardless of what the prey does. It means they will surround the prey in a variety of ways, softly or forcefully, depending on how much energy the prey has saved. In actual life, the hawks go nearer and nearer to their selected prey to enhance their chances of hunting the rabbit collectively by conducting a surprise pounce. Short time after, the fleeing prey will gradually lose its energy, and the hawks will strengthen the besiege to easily catch the weary prey. The E parameter is used to model this strategy and allow the HHO to flip between soft and harsh besiege processes. When $|E| \geq 0.5$, the soft surround occurs, and when $|E| < 0.5$, the hard surround occurs [51].

5. Simulation Results and Discussions

The proposed Harris hawk optimization (HHO) technique is utilized to attain the best size for a hybrid microgrid system that comprises PV, WT, diesel, and batteries to provide electricity for Al Sulaymaniyah hamlet in Arar, Saudi Arabia. The HHO is compared to seven metaheuristic techniques: GOA, CSO, BBBC, coyote, crow search optimizer, genetic algorithm, and BOA to validate its performance. The optimization issue was implemented using MATLAB R2019b/64-bit/Windows 10 with 500 iterations and 50 runs for all eight metaheuristic-based techniques. In this investigation, the values of average hourly irradiance and wind speed have been used.

Table 1 shows the simulation findings of the HHO with seven recent metaheuristics for tackling the best size of the proposed HES microgrid with a 0% of LPSP in terms of the best solution, worst, average, and standard deviation (STDEV). According to these results, the HHO performed better than any of the other seven metaheuristics tested: GOA, CSO, BBBC, coyote, crow search, genetic algorithm, and BOA in achieving the best size of the HES microgrid with the lowest cost. This is obvious by looking at Figure 4, which compares the optimal ASC calculated using the HHO to the results obtained by employing seven other metaheuristic-based techniques. This figure proved the HHO efficacy to attain the optimal solution followed by GOA, CSO, and coyote.

Figure 4 reveals that crow search and BBBC have the lowest performance among the other metaheuristic-based techniques. Figure 5 depicts the optimum combination of the WT, PV, batteries, and diesel generator for each of the eight metaheuristic algorithms. This figure proves that the renewable energy (PV and WT) participates higher than the diesel where the diesel sizing is minimized, and the renewable sizing is increased as the diesel price increases. Figures 6(a) and 6(b) also illustrate the five-performance metrics that are employed to assess the performance of the eight techniques. Compared to the other seven optimization strategies, HHO has the best performance, whereas the BBBC and genetic algorithm have the worst performance based on these five-performance metrics, as shown in Figure 6. Furthermore, based on these five-performance metrics, it can be revealed that the four metaheuristic-based optimization techniques (HHO, GOA, CSO, and coyote) have an acceptable performance whereas the remaining four metaheuristic-based techniques (BBBC, crow search, genetic algorithm, and BOA) have poor performance. The BBBC has the worst performance compared to the other seven optimization techniques.

Table 1: Results of the HHO compared with seven metaheuristic optimization algorithms.

Algorithm	Performance indicators	P_{PV} (kW)	P_{WT} (kW)	P_{Bat} (kW)	P_{Diesel} (kW)	ASC (USD/year)	REF (%)
HHO	Optimal	358.24	361.80	992.88	224.93	149229.9	86.30694
	Worst	406.5051	339.3375	562.0104	209.5526	151348.5	82.46066
	Mean	356.4754	345.0759	829.1315	216.8645	150209.8	84.1395
	STDEV	39.18455	46.1519	220.7427	9.658326	442.0191	1.652636
GOA	Optimal	358.90	362.95	994.97	223.15	149380.5	86.36665
	Worst	308.8779	383.4638	835.64	216.0318	150243.8	84.52918
	Mean	357.2016	362.815	975.8187	222.7259	149488.7	86.15532
	STDEV	12.37447	5.529344	80.77056	3.248609	193.8246	0.810537
CSO	Optimal	358.87	362.64	995.87	222.95	149382	73.76322
	Worst	351.4298	375.2112	882.0394	232.8948	150037.7	99.06436
	Mean	359.7846	363.0136	985.4449	225.0616	149538.6	84.39674
	STDEV	2.705516	5.21919	20.49994	3.396348	151.2683	10.83353
BBBC	Optimal	397.85	348.4	923.9	229.1	150883.5	64.55
	Worst	293.95	434.95	1436.3	248.06	158884.5	70.52
	Mean	372.75	364.27	844.21	239.71	154138.5	86.67
	STDEV	72.14	69.41	293.67	7.45	2007.99	10.379
Coyote	Optimal	359.59	360.95	1000.00	223.24	149476.7	86.42048
	Worst	338.064	396.3999	919.5867	230.7491	150348.7	86.34566
	Mean	359.1265	363.0383	990.8932	224.8782	149741.2	80.31711
	STDEV	4.173589	7.046377	13.62386	3.152154	157.3429	16.49967
CROW	Optimal	341	404	499	216	151619	82.7
	Worst	359	405.8	498.86	221.7	151833	83.05
	Mean	341.8	405.	499.11	216	151640	82.77
	STDEV	4.57	2.93	0.3925	0.884	50.77	0.098
Genetic algorithm (GA)	Optimal	370.2	311.5	1028	211	15072	85.2
	Worst	496.3	260.5	1356	204.2	15477	88.3
	Mean	375.6	346.9	940.6	219.1	151945	85.6
	STDEV	45.9	52.92	161.4	21.4	927.5	1.627
BOA	Optimal	361.28	373.70	950.01	227.34	150236.4	63.31917
	Worst	352.0645	331.3051	657.5377	228.0661	151968.8	61.28074
	Mean	343.8703	353.6341	850.2741	214.0609	151130.5	66.92574
	STDEV	26.3586	27.9817	161.5311	11.46092	422.1061	6.236738

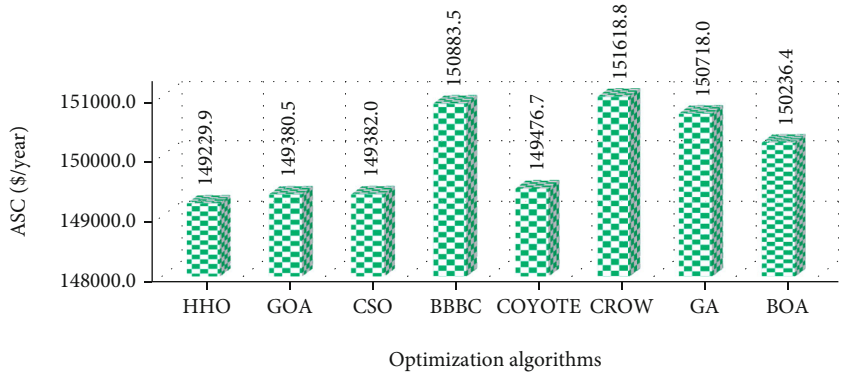

Figure 4: The optimal ASC utilizing HHO when compared to the other seven metaheuristic techniques.

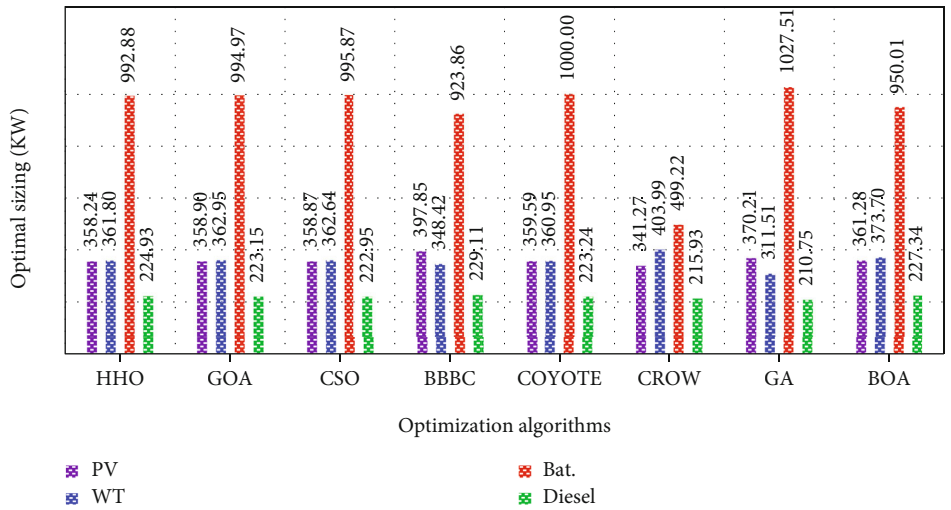

Figure 5: The optimal PV, WT, diesel, and battery sizing of the metaheuristic algorithms.

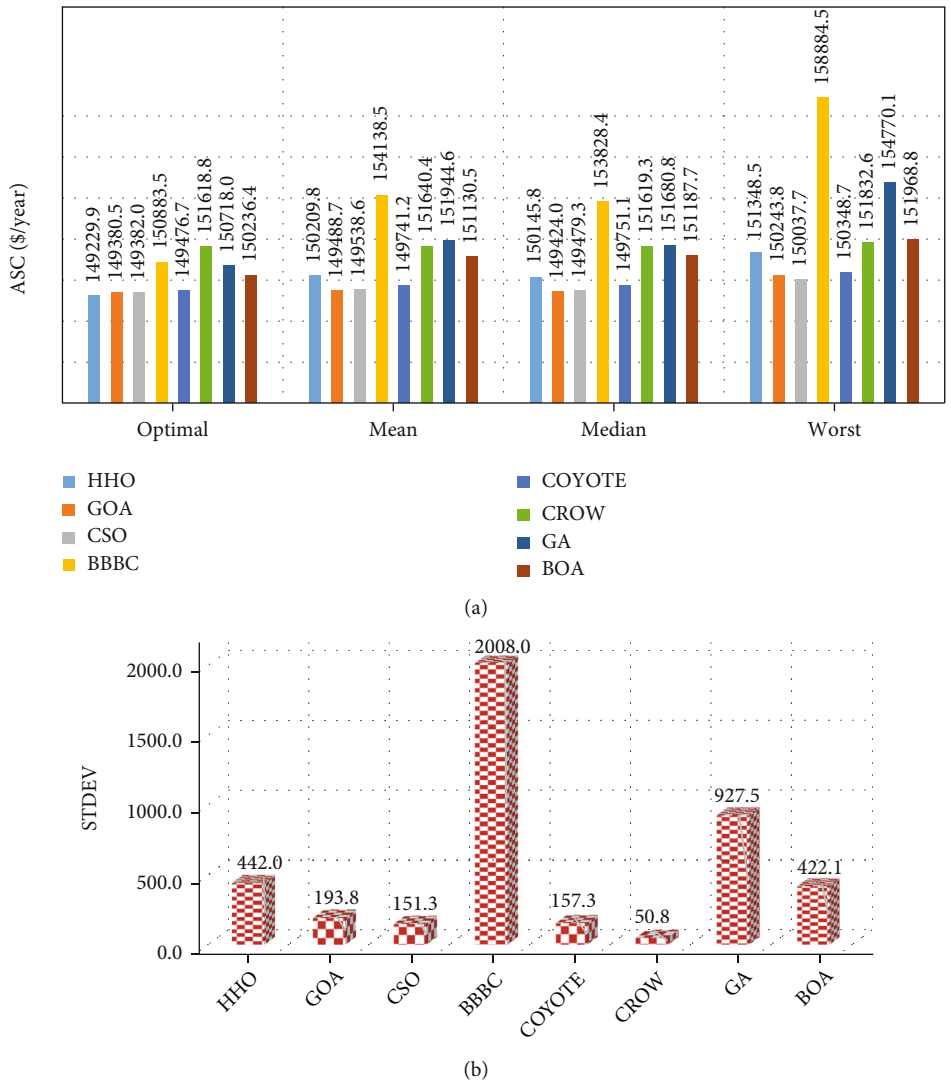

Figure 6: The five-performance metrics: (a) optimal, worst, median, and mean and (b) STDEV.

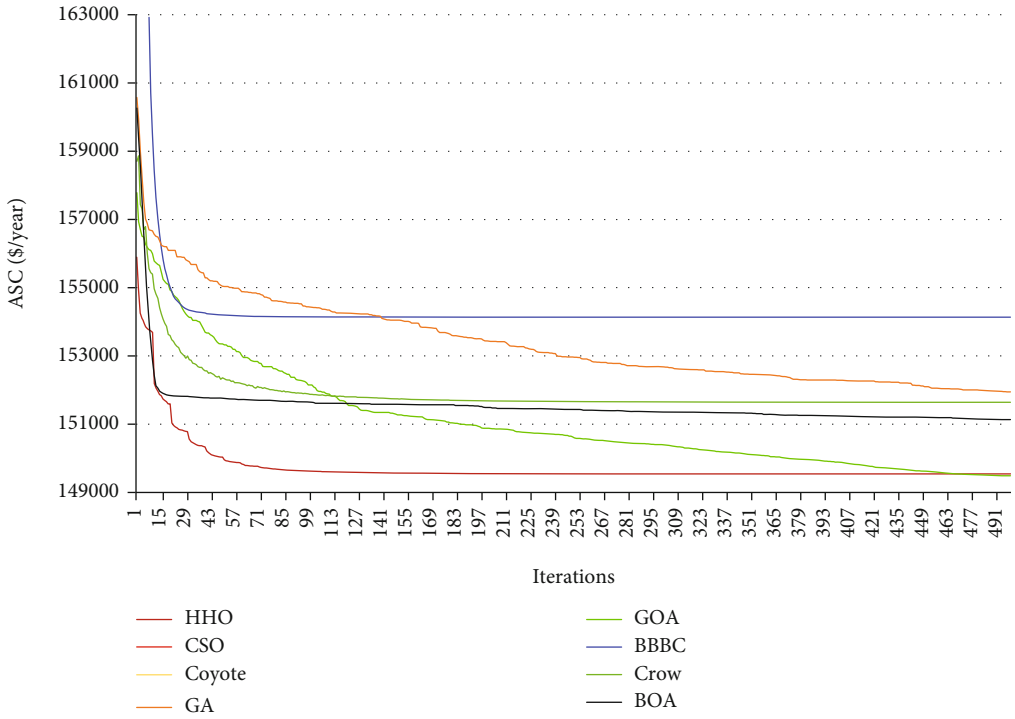

Figure 7: Convergence rate of the HHO compared with the other optimization algorithms.

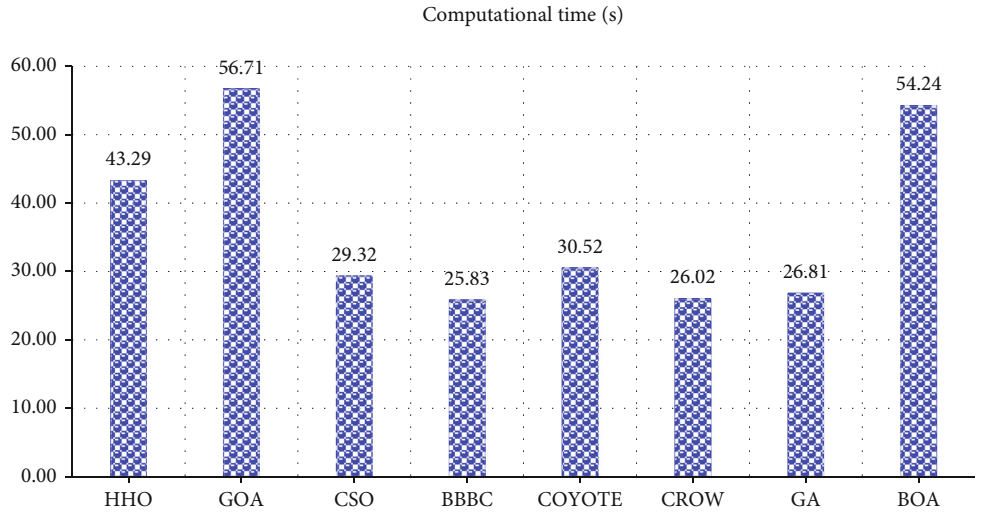

Figure 8: The computational time of the eight metaheuristic algorithms under consideration.

The convergence rate of all metaheuristic techniques: HHO, GOA, CSO, BBBC, coyote, crow search, genetic algorithm (GA), and BOA, is shown in Figure 7. As demonstrated in this figure, the four metaheuristic-based techniques (HHO, GOA, CSO, and coyote) have a higher rate of convergence than the other four metaheuristic-based methods while tracking the global solution. This graph also demonstrates that BBBC and GA have the slowest convergence rates, which implies they might become stuck in a local solution and take a long time to achieve a steady state. This is because BBBC and GA both have a high STDEV. As a result, the best solutions are broadly distributed, and both techniques could end up with a local solution.

The computational time required by each algorithm to obtain the optimum solution is depicted in Figure 8. Although the BBBC, GROW, and GA were the quickest to discover the best solution in almost all experiment runs, one must bear in mind that these algorithms provided the worst findings. As shown in Figure 8, the HHO, GOA, and BOA algorithms have been shown to be nondominant. Although the HHO can find the best optimal solution compared to the seven algorithms, it needs improvement related

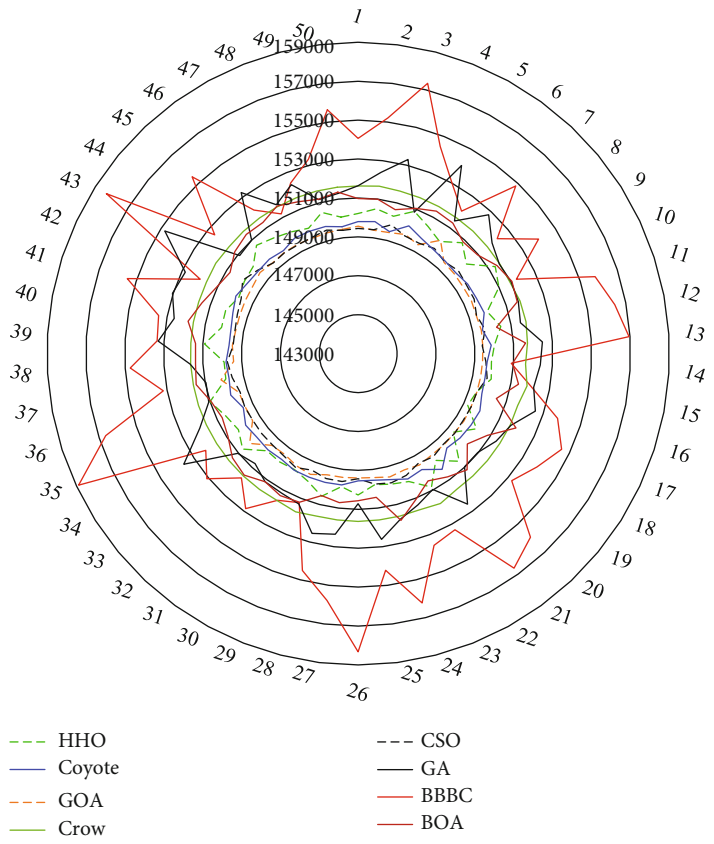

Figure 9: The ASC vs. run number for metaheuristic algorithms.

to the reduction of the computational time. Figure 9 illustrates the ASC versus the run number for the HHO method compared with the other seven metaheuristic-based optimization approaches. The four metaheuristic-based approaches (HHO, GOA, CSO, and coyote) can abide the global solution and attain the optimal design of the HES microgrid with the lowest ASC, less oscillation, and quick convergence, while the four metaheuristic-based optimization approaches (BBBC, crow search, BOA, and genetic algorithm) may be trapped to the local solution and have clear oscillations, as shown in Figure 9. Furthermore, this graph indicates that both BBBC and genetic algorithm are unable to capture the global solution, resulting in noticeable steady-state oscillations.

6. Conclusions

The Harris hawk optimization (HHO) technique has been used to find out the best design for a HRE microgrid, which includes PV, WT, diesel, and batteries to provide electricity for Al Sulaymaniyah hamlet in Arar, Saudi Arabia. The HHO is compared to seven metaheuristic-based techniques for validation: GOA, CSO, BBBC, coyote, crow search, genetic algorithm, and BOA to achieve the best size of the HES microgrid based on minimizing the annualized system cost. To discern and assess the performance of these eight metaheuristic algorithms, five-performance benchmarks (optimal and worst solution, STDEV, mean, and median) are utilized. The HHO surpassed the other seven metaheuristic-based techniques: GOA, CSO, BBBC, coyote, crow search, genetic algorithm, and BOA, in achieving the best size of the HES microgrid with the lowest ASC (USD 149229.9) and convergence rate. The four metaheuristic-based techniques (HHO, GOA, CSO, and coyote) exhibit an acceptable performance in terms of global solution capture with fewer oscillations and convergence rate, whereas the four metaheuristic-based techniques (BBBC, crow search, genetic algorithm, and BOA) have poor and unacceptable performance, resulting in local solution trapping instead of global solution, obvious oscillations to find solution, and a high convergence rate. In terms of optimal solution and convergence rate, the BBBC and GA have bad performance in comparison to other metaheuristic-based optimization approaches. The reason behind this is that both BBBC and GA have a high standard deviation. The high standard deviation indicates that the best solutions are widely dispersed, and both techniques could end up with a local solution. Future work necessitates the improvement of the HHO to increase population diversity in the search space while decreasing consumption time.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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Research Article

Design of Boosted Multilevel DC-DC Converter for Solar Photovoltaic System

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Integration of renewable energy sources to the grid-connected system has influenced scholarly research in recent times to evolve solutions for power electronic conversion. Particularly, solar photovoltaic (SPV), being a resource available throughout the year, demands needful research to meet the demand for industrial applications. To facilitate SPV, multilevel inverters (MLIs) and cascaded H-bridge inverters (CHBIs) are proposed in the literature to meet the power requirement. However, these circuits suffer from efficiency loss, economic aspects of DC sources usage, and switching losses. Hence, in this research, a new power converter topology is projected to improve the overall efficiency of SPV systems. Further, a three-level approach involving (i) SPV Panel-Temperature Reduction (SPV-PTR) Setup, (ii) Boost Multilevel Direct Current Link Converter (BMLDCLC), and (iii) use of effective snubber modules (SM) are effectively handled to promote the industry readiness of the proposed system. From a detailed system investigation, it is seen that the proposed arrangement has minimized the power loss to ensure better quality in output. Furthermore, the software-based results and hardware setup of the planned comprehensive converter have shown promising results in terms of (i) reduced voltage stress, (ii) reduced total harmonic distortion (THD) without filter component, and (iii) reduced power loss. It is observed that the experimental setup has reported a 12.9% of excess heat removal, 5% decrease in harmonics, and 33% switch reduction than the existing MLI schemes. In addition, the proposed setup is suggested to apply for industrial purposes indicate its efficacy to be a solution in real time.

1. Introduction

Alarming environmental concerns and exhaustion of fossil fuels have invoked the necessity of eco-friendly power generation via renewable energy resources [1]. Having the superiority to reduce greenhouse emissions, renewable energy is considered as one of the essential tools to avoid energy import. In particular, SPV systems have gained monumental recognition to emerge as a resource of the decade. Zero maintenance, harmless operation, abundant availability, and easy portability are its inherent merits over other renewable energy resources.

In general, SPV modules are constant voltage sources fed to a load via power conditioning circuits. However, fabricating an efficient and cost-effective converter prototype model is really challenging. Since the power conditioning circuitries are implemented over two or three-level converters, interfacing PV panels for high power application become complex

and uncertain. More importantly, sequential power electronic switching with three-level converters renders excessive voltage stress across the converter. This results in stressed transmission. Therefore, a supplementary snubber circuit at the output is mandated to reduce the transient power loss [2]. In addition, bulky filter components are also used to tap the hassle-free sinusoidal output. However, the system cost is increased beside the additional usage of transformers on the output side [3].

As an alternative to three-level converters, researchers have used multiple topologies with multilevel inverters (MLIs). It is important to note here that the advent of MLIs has enabled the efficient interface with multiple electrical applications such as (i) uninterrupted power supply (UPS) systems, (ii) motor drives, (iii) integration of renewable energy systems, (iv) static compensator, and (v) renewable energy sources [4–8]. Though MLIs have exhibited their significant merits from the end-user side, they are penalized with the necessity of high (i) power-switching components, (ii) regulator units, (iii) power supply units, (iv) gate driver circuits, (v) protection units, and (vi) DC sources to reduce its popularity [9–16]. This certainly increases the manufacturing cost of the system. Out of many configurations in MLI, a few important works in literature are presented as the review in the following. A typical nine-level multilevel inverter for induction motor application is presented in [9]. Also, the importance of high-frequency switches to control uncertainty and voltage diversity factor is critically analyzed in this research. With an objective to reduce power electronic switches, a seven-level MLI with three sources is presented in [10]. Alternatively, a nine-level MLI design with four DC sources is presented in [11]. Notably, usage of limited (twelve) Metal Oxide Semiconductor Field Effective Transistor (MOSFET) switch has gained research interest to reduce THD. However, all the aforementioned works have the drawbacks of (i) design of control circuit, (ii) elimination of lower-order harmonics, and (iii) requirement of high switching devices. Hence, a novel H-bridge-based MLI system has been proposed in [12]. But then, the research necessitates an additional DC source which remains an important downside of the topology. Sequentially to limit the source count with MLI, a seven-level MLI with only three DC sources is proposed in [13]. However, twelve controlled semiconductor switches are used. With a motive to reduce power electronic switches, a similar MLI design with eight controlled semiconductor switches is proposed in [14]. Using only three sources, the same seven-level MLI topologies are presented in [15, 16]. Nevertheless, usage of power semiconductor switches was found high compared to [14].

At the outset, in comparison to various topologies discussed in [13–20], it is seen that the output voltage is achieved either by a series connection of DC sources or using a transformer at the inverter side. Thus, it becomes a nonviable solution for grid-connected systems economically. Note that power losses are also increased due to the usage of the bulky transformer. This invokes a power converter system to maintain the nominal voltage at the DC link, and it is achieved by using appropriate DC to DC power converters. Alternatively, cascaded H-bridge inverters among MLI are also proposed in the literature. Owing to the simpler and lucid circuitry, few research works are reported by using cascaded H-bridge inverters (CHBIs) in [17–20]. In comparison over two or three-level inverters, the use of CHBI offers multiple salient features such as (i) meagre transient across the inverter, (ii) reduced total harmonic distortion (THD) without filter component, and (iii) less significant filter components.

Commencing from the extensive review survey, it is seen that there exist a wide gap in formulating an MLI with the following advantages: (i) limited DC sources, (ii) less stress on the converter, (iii) less THD, and (iv) limited use of power electronic switches. Therefore, a new and novel seven-level stepped DC-link converter is proposed in this research. In addition, the converter is integrated with the PV source to check its viability for industry applications. In order to appreciate the panel temperature within limits, an exclusive prototype testing of PV with an aluminum sheet supported by a DC fan for cooling arrangement is performed. It is important to note here that PV panels are provided with a hydrophobic nano coating (HNC) solution to avoid dust accumulation and stagnant water droplets on PV panels. This helps the PV to shield itself from corrosion, thus increasing the lifetime for its continued quality of operation. The distinguished merits of the proposed research are summarized in the following.

(i) A new seven-level stepped DC-link MLI with reduced stress on the converter is proposed for the first time

(ii) The seven-level stepped DC-link converters are interfaced with the PV module, and their industrial viability is studied

(iii) To subside the panel temperature in real time, the cooling arrangement is provided via aluminum sheet and DC fans

(iv) To enable durability and long sustainability with PV, hydrophobic nano coating (HNC) is used

(v) The use of two PV sources at the input side per phase eliminates the unnecessary stress on the converter

The entire paper is ordered as follows. In Section 2, PV modelling and design of DC-DC boost converter is detailed. In Section 3, the proposed converter design and its design constraints are given. Software-based results and hardware realization are given in Sections 4 and 5, respectively. To contribute to a fair comparative study, the usage of power electronic components and their losses are analyzed and compared in Section 6. Conclusions are addressed as the summary in Section 7.

2. PV Modelling

One-diode PV models are prevalently popular to use for simulation investigations. The representation of the corresponding electrical circuit of one diode PV model is represented in Figure 1 [21–23], and for better understanding,

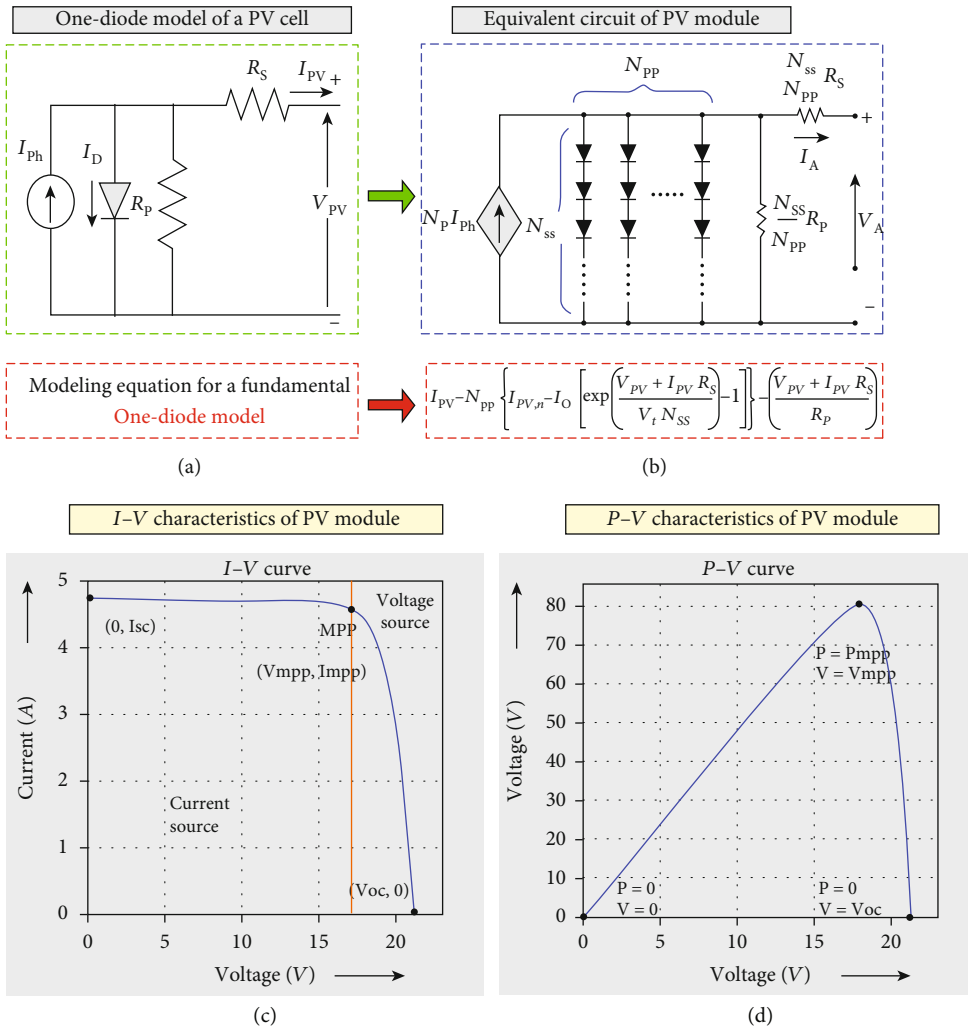


Figure 1: One-diode PV model and its characteristics.

the I-V and P-V distinctiveness of a PV module are also presented in the same figure. From the characteristics, it is seen that PV operates at a unique operating point where maximum power can be extracted. In addition, PV demands a power electronic interface to enable its smoother operation. The PV output current [23] by applying KCL is given by

$$I_{\mathrm{PV}} = I_{Ph} - I_D - \frac{V + I_{\mathrm{PV}} Rs}{Rp}. \tag{1}$$

The ideal diode current equation is mathematically given in Equation (2).

$$I_D = I_O\left(e^{V_D/\alpha V_T} - 1\right), \tag{2}$$

where "I_o" is the reverse saturation current, "a" is the diode ideality factor, and "V_T" is the thermal voltage proportional to temperature changes which is given by

$$V_T = \frac{N_S K T}{q}, \tag{3}$$

where "N_s" is the number of cells connected in series, "K" is the Boltzmann constant, "T" is the temperature at STC, and "Q" is the charge of the electron $1.9 * 10^{-19}$C. On incorporating "I_D" in "I_{PV}," then the output current equation (24) becomes

$$I_{\mathrm{PV}} = N_{pp}\left\{I_{Ph} - I_O\left[\exp\left(\frac{V_{PV}+I_{\mathrm{PV}}R_S}{V_t N_{ss}}\right) - 1\right]\right\} - \left(\frac{V_{\mathrm{PV}} + I_{\mathrm{PV}}R_S}{R_P}\right), \tag{4}$$

where "N_{SS}" and "N_{PP}" are the numbers of cells connected in series and parallel [24, 25].

3. Multilevel Stepped DC-Link Converter

Further, synthesizing sinusoidal voltage with less harmonic using multiple DC sources is its unique characteristic. Note that three-phase multilevel inverters gain more attention since each individual phase requires an "N" number of DC sources to obtain a "$2N+$" voltage output level. However, MLI greatly suffers due to the requirement for an increased

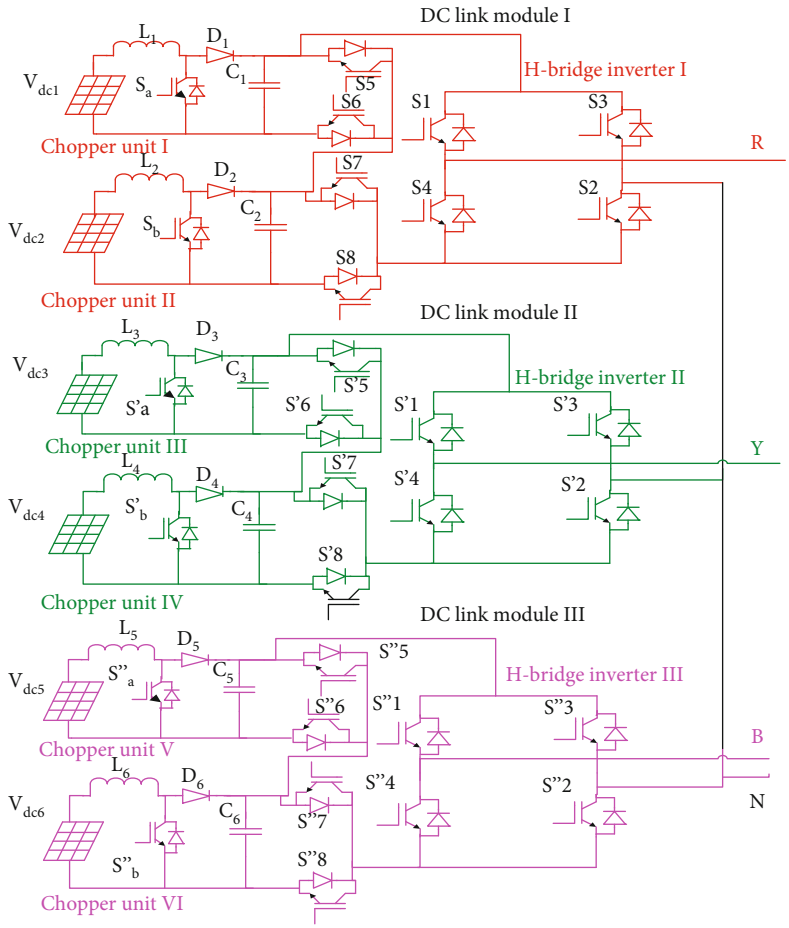


Figure 2: Equivalent circuit of three-phase seven-level BMLDCLC.

number of power electronic components, and this is reduced by using Boosted Multilevel DC Line Converter design. One such configuration with PV as the source is proposed in this research. The operating modes and their analysis on output voltage are discussed in the following.

3.1. Design of Boosted Multilevel DC-Link Converter (BMLDCLC). The schematic of the projected seven-level BMLDCLC circuit is represented in Figure 2. For understanding, each phase is highlighted in different colors and named in the convention as *R* phase, *Y* phase, and *B* phase. Note that each phase is provided with a provision to switch on and off to maintain the output voltage in limits. Further, the boost converter is interfaced among the MLI and PV sources. This eliminates the necessity of a transformer and thus improving the cost efficiency of the converter. Further, the equivalent circuit of BMLDCLC clearly shows that boost chopper takes responsibility to uphold DC-link voltage across each phase. In addition, two power sources are used in each phase reduces the stress on converter is a notable merit of proposed converter. The generalized equations (12–14) to estimate the power components, sources, and level of single-phase BMLDCLC are presented in Equations (5)–(7).

$$N_{\text{switch}} = 2s + 4H + b, \tag{5}$$

$$n = 2(H+1)^s - 1, \tag{6}$$

$$H = n - (n-1), \tag{7}$$

where "*s*" is the DC source count, "*n*" is the number of levels, "*H*" is the number of converter topology at load end, and "*b*" represents boost converter.

3.2. Design of Boosted Multilevel DC-Link Converter (BMLDCLC). The DC-DC boost converter is an integral part of the proposed converter design. Further, it is connected to the inverter via switching circuitry to generate AC waveforms. The schematic of the DC-DC boost converter is presented in Figure 3. Since PV is a constant voltage source, the task of boosting converter becomes much easier to maintain constant DC-link voltage across the inverter. As a known fact that PV is a nonlinear DC source, the system demands a maximum power point controller to track the MPP. To achieve this, each PV panel is provided with a current and voltage sensor to track the unique operating point where the highest accessible power is able to be pulled out. Note that a simple perturb and observe (P&O) algorithm is employed to appreciate simplicity. Besides, the necessity of a metaheuristic algorithm is not required since only one module is used as a DC source [26–30]. For brevity, the flowchart of the P&O algorithm is presented in Figure 4.

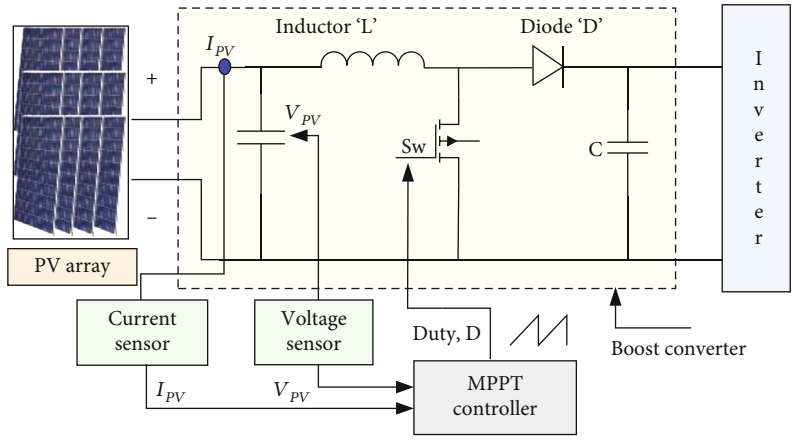


Figure 3: Representation of DC-DC boost converter.

In general, P&O works on the standard that repeated perturbation in voltage is made until the MPP is tracked. Based on the power values, the duty cycle of the boost chopper is altered [11]. Duty cycle equation of the boost chopper is given in the following.

$$D = \frac{V_o - V_s}{V_o}, \tag{8}$$

where "V_o" and "V_s" are the voltage across the load and source voltage, respectively, and "D" is the duty cycle. Further, the design considerations of boost chopper are given in the following. It is always ensured that the boost chopper is worked in continuous conduction mode, and the design of inductor "L" is made by following the equation given in (9).

$$L = \frac{V_o(1-D)}{\Delta i_L f_s}, \tag{9}$$

where "Δi_L" is the inductor current $(i_2 - i_1)$ and "f_s" is the switching frequency. For better output quality, 3% current ripple is considered for designing the inductor. Capacitor design is made by following the equation given in (10).

$$C = \frac{1-D}{8L(\Delta V_o/V_o)f_s^2}, \tag{10}$$

where $f_s = 1/T$ is the switching frequency and "$\Delta V_o/V_o$" is the voltage ripple, and it is approximately considered as 3%.

3.2.1. Modes of Operation of Boosted Multilevel DC-Link Converter (BMLDCLC). The proposed Boosted Multilevel DC-Link Converter (BMLDCLC) is designed for 3-phase load, and each phase constitutes six different operating modes. A detailed discussion on its working is given in the following.

(1) Modes of Operations in "R" Phase. During the first and fourth modes of operation, the source voltage "V_{dc1}"is boosted by turning on the switch S_a. The mathematical expression for "V_{dc1}" is given.

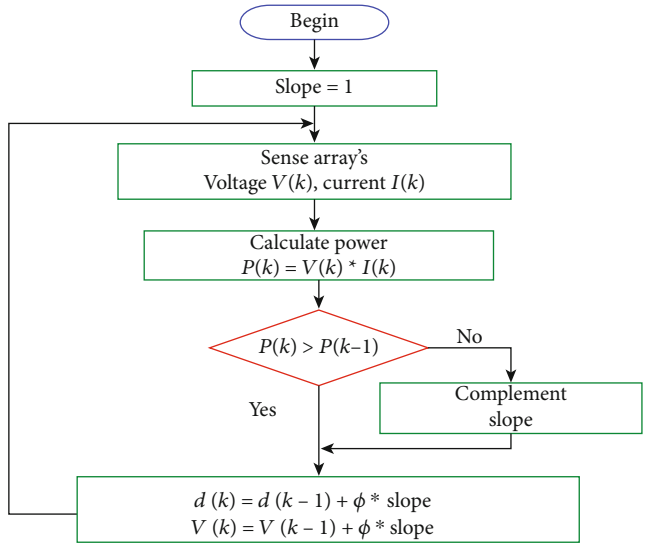


Figure 4: Perturb and observe algorithm for MPP tracking.

In Equations (8) and (9), further, the switches S_6 and S_7 are made to behaviour to attain the voltage level "V_{ob1}" at the inverter side.

$$V_{dc1} = L_1 \frac{I_2 - I_1}{T_{on1}}, \tag{11}$$

$$V_{dc1} = L_1 \frac{dI_1}{dt}. \tag{12}$$

The energy stored in the inductor "E_{i1}" can be calculated by using Equation (6).

$$E_{i1} = V_{dc1}.I_{s1}.T_{on1}. \tag{13}$$

At the time, $t = T_{off1}$, switch S_a is made to switch off, and hence, source current flows through L from I_2

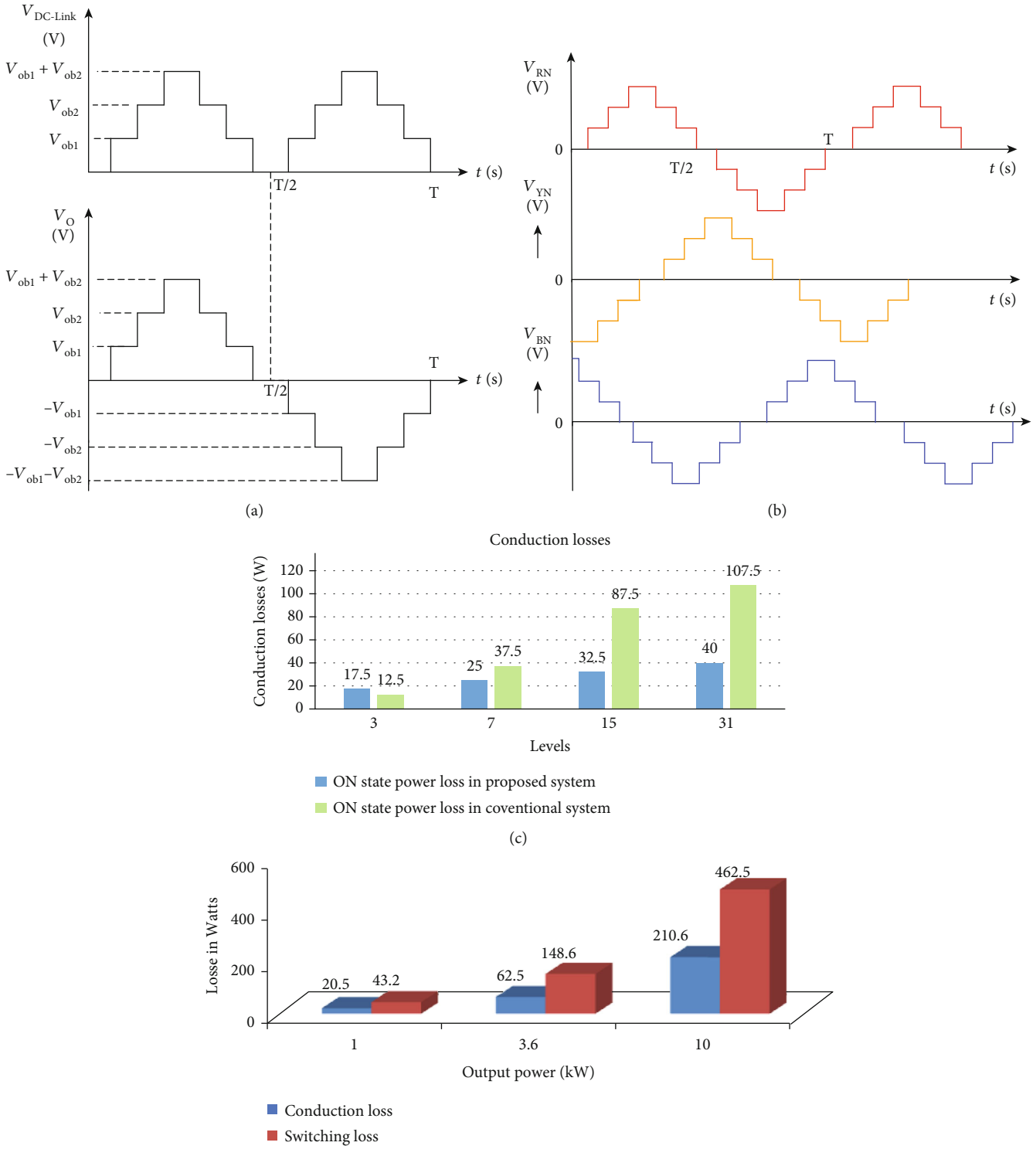
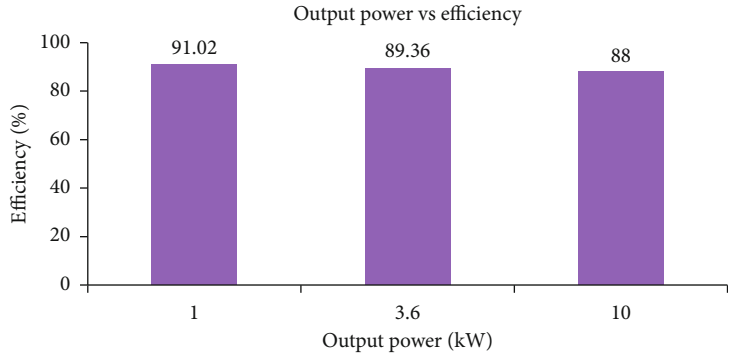


Figure 5: Continued.



(e)

FIGURE 5: (a) Distinctive voltage waveform of 1Φ seven-level BMLDCLC. (b) Characteristic output voltage waveform of 3Φ BMLDCLC. (c) Analysis of conduction loss of BMLDCLC. (e) Losses and efficiency.

to I_1. Therefore, the average output voltage at DC to DC boost converter I can be expressed as Equation (14)

$$V_{ob1} = V_{\mathrm{dc1}} + L_1 \frac{dI_{s1}}{T_{\mathrm{off1}}}. \tag{14}$$

The energy release 'E_{o1}' at this instant can be calculated using Equation (15).

$$E_{o1} = (V_{ob1} - V_{\mathrm{dc1}}) I_{s1}.T_{\mathrm{off1}}. \tag{15}$$

The output voltage of boost converter I of R phase is thus attained as in Equation (16).

$$V_{ob1} = \frac{V_{\mathrm{dc1}}}{1 - K_1}. \tag{16}$$

The change in capacitor voltage can be calculated by using Equation (17).

$$\Delta V_{C1} = I_{o1} * \left[\frac{V_{ob1} - L_1(I_2 - I_1)}{V_{ob1} * f * C_1}\right]. \tag{17}$$

In the second and fifth switching schemes of the chopper unit, the PV source voltage V_{dc2} is boosted to V_{ob2} by turning on the switch S_b in the boost chopper, while S_5 and S_8 are used as a snubber. At this time period, $t = T_{\mathrm{on2}}$; switch S_b of chopper unit-II is turned on to raise the inductor current I_3 and I_4 linearly. The voltage and energy equation corresponding to inductor L_2 is equated in Equations (18) and (19).

$$V_{\mathrm{dc2}} = L_2 \frac{I_4 - I_3}{T_{\mathrm{on2}}}, \tag{18}$$

$$E_{i2} = V_{\mathrm{dc2}}.I_{s2}.T_{\mathrm{on2}}, \tag{19}$$

where I_3 is the current flowing through the inductor during boost operation in boost chopper unit-II and I_2 is the current flowing through the inductor due to S_b in boost chopper unit-II. During $t = T_{\mathrm{off2}}$, switch S_b of the chopper-II unit gets turned off, because of which, the current through L_2 linearly falls from I_4 to I_3. The expression pertaining to the average output voltage and energy stored in the boost chopper IV is given in the following equations:

$$V_{ob2} = V_{\mathrm{dc2}} + L_2 \frac{dI_{s2}}{T_{\mathrm{off2}}}, \tag{20}$$

$$E_{o2} = (V_{ob2} - V_{\mathrm{dc2}}) I_{s2}.T_{\mathrm{off2}}. \tag{21}$$

For schemes 3 and 6, the source voltage V_{dc1} and $V_{\mathrm{dc2}}$are stepped up to obtain V_{ob1} and V_{ob2} by turning on switches S_a and S_b of DC-to-DC boost converter. During conduction, S_6 and S_8 act as a snubber to protect the boost converter switches. During the turn-on period ($t = T_{\mathrm{on3}}$), switches S_a and S_b remain conducting to linearly rise the inductor current L_1 and L_2 from I_1 to I_2 and from I_3 to I_4 respectively. The input energy of inductor L_1 from the source voltage V_{dc1} is given in Equation (22).

$$E_{i3} = (V_{\mathrm{dc1}} + V_{\mathrm{dc2}}).(I_{s1} + I_{s2}).T_{\mathrm{on3}}, \tag{22}$$

The output phase voltage (V_{RN}) of BMLDCLC is given as

$$V_{RN} = (V_{ob1} + V_{ob2}) \sin \omega t. \tag{23}$$

(2) Modes of Operations in Y Phase. Similar to the modes of operation of R phase, Y phase DC-link switches (S_5', S_6', S_7', and S_8'), boost chopper switches (S_a' and S_b'), and converter switches (S_1', S_2', S_3', and S_4') are triggered systematically with the phase shift of 120°. The phase voltage equation pertinent to the "Y" phase is given by (V_{YN}). For Y phase, the scheme of switching the 2nd and 5th DC-DC boost converter is followed. The PV source voltage V_{dc4} is boosted to V_{ob4} by turning on the switch S_b' in the DC-DC boost converter where S_5' and S_8' are used as snubbers. At time period $t = T'_{\mathrm{on2}}$, switch S_b' of DC-DC boost converter is turned on to raise the inductor current I_3' to I_4' linearly. The voltage

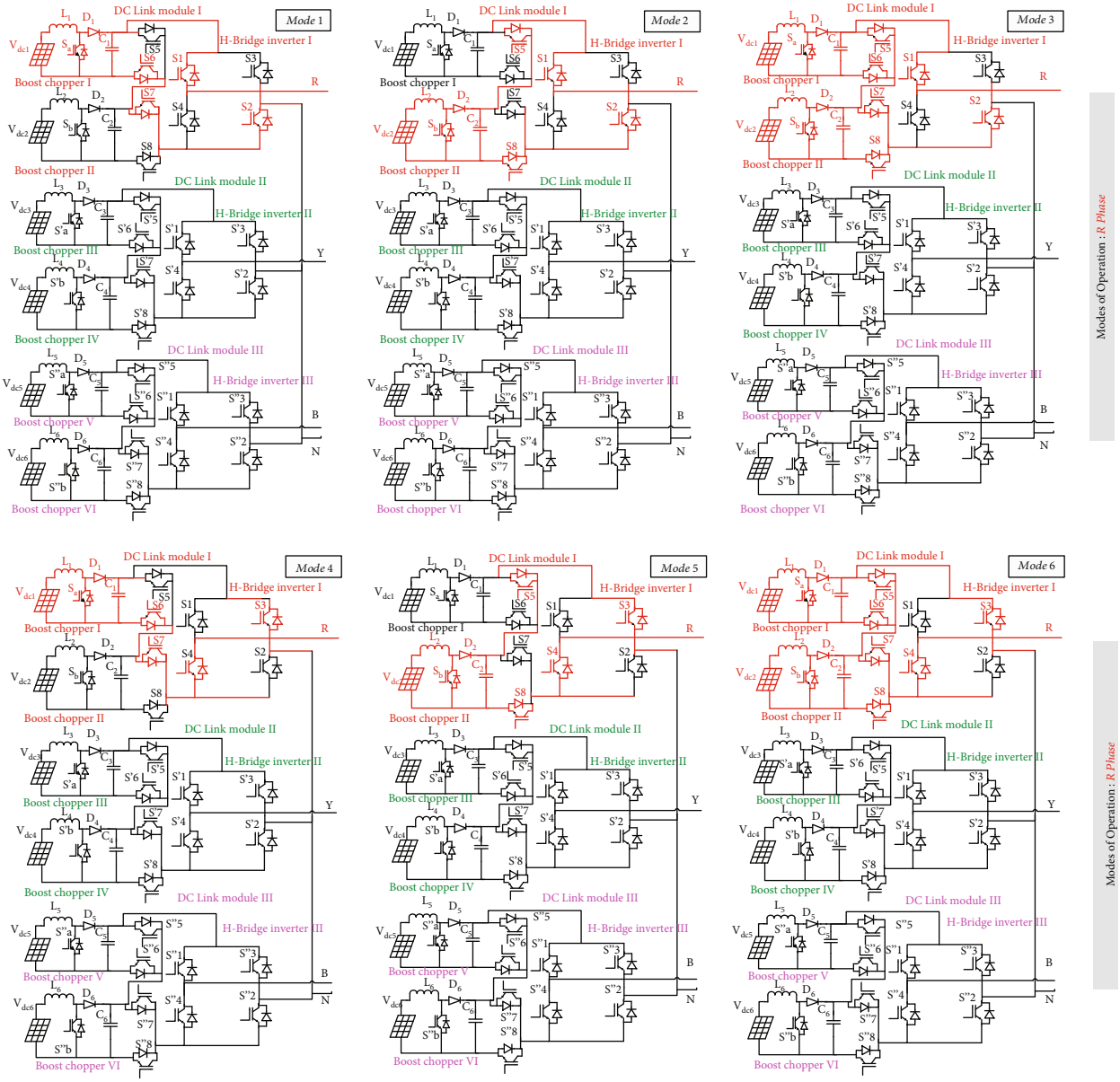


Figure 6: Modes of operation of proposed 3-phase seven-level BMLDCLC.

and energy equation corresponding to inductor L_4 is expressed as

$$V_{\mathrm{dc4}} = L_4 \frac{I'_4 - I'_3}{T'_{\mathrm{on2}}}, \tag{24}$$

$$E_{i4} = V_{\mathrm{dc4}}.I_{s4}.T'_{\mathrm{on2}}. \tag{25}$$

At time $t = T'_{\mathrm{off2}}$, switch S'_b of the DC-DC boost converter is turned OFF where the inductor current linearly falls from I_4 to I_3. The expression pertaining to the average output voltage and energy stored in the DC-DC boost converter IV is given in the following equations:

$$V_{ob4} = V_{\mathrm{dc4}} + L_4 \frac{dI_{s4}}{T'_{\mathrm{off2}}}, \tag{26}$$

Table 1: Specifications of three-phase BMLDLC systems.

Parameters	Range
Source voltage unit I (V_{ob1})	24 V
Source voltage II (V_{ob2})	48 V
H-bridge inverter output voltage (V_{phmax})	72 V
H-bridge inverter output voltage ($V_{L\ \mathrm{max}}$)	120 V
RL load system	218 Ω, 197 mH
Rated power	100 W

$$E_{o4} = (V_{ob4} - V_{\mathrm{dc4}})I_{s4}.T'_{\mathrm{off2}}. \tag{27}$$

The average output voltage of DC-DC boost converter IV

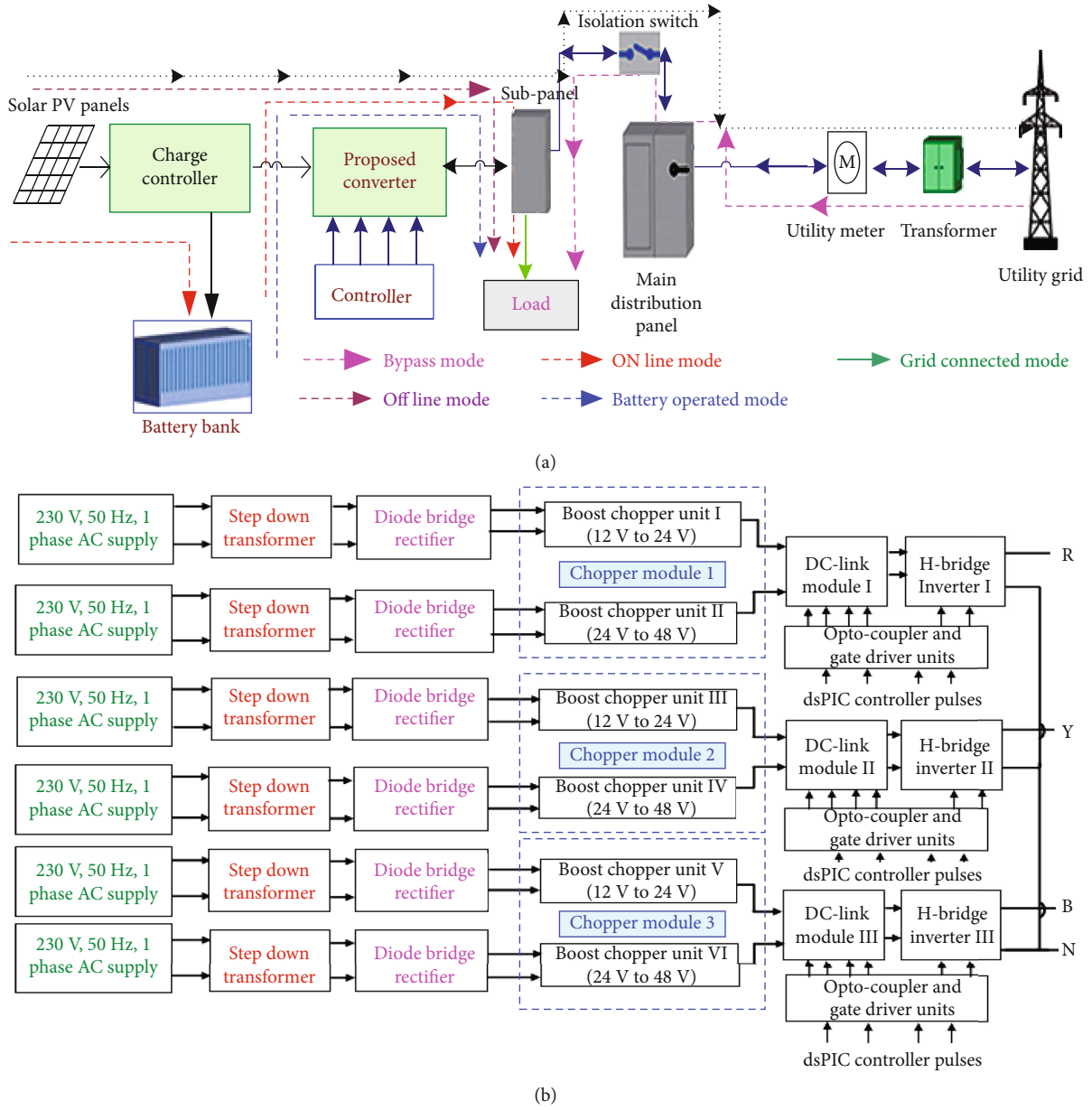


Figure 7: (a) Schematic diagram of BMLDCLC-based UPS system. (b) Block diagram of 3ϕ seven-level BMLDCLC.

under ideal conditions is expressed in Equation (28).

$$V_{ob4} = \frac{V_{dc4}}{1 - K'_2}. \tag{28}$$

The difference in voltage across the capacitor C_4 is articulated by Equation (29).

$$\Delta V_{C4} = I_{o4} * \left[\frac{V_{ob4} - L_4\left(I'_4 - I'_3\right)}{V_{ob4} * f * C_4}\right], \tag{29}$$

where V_{dc4} is the DC source voltage IV, I_{s4} is the DC source current IV, K'_2 is the duty cycle of DC-DC boost converter IV, and V_{ob3} is the output voltage of DC-DC boost converter IV.

$$V_{YN} = (V_{ob3} + V_{ob4}) \sin(\omega t - 120^\circ). \tag{30}$$

(3) Modes of Operations in B Phase. Similar to the modes of operation of R and Y phases, B phase DC-link switches (S''_5, S''_6, S''_7, and S''_8), DC to DC converter II (S''_a and S''_b), and inverter switches (S''_1, S''_2, S''_3, and S''_4) are triggered systematically with the phase shift of 240°. For schemes 3 and 6, the source voltage from PV, V_{dc3}, and V_{dc4} are stepped up to obtain V_{ob3} and V_{ob4} by turning on switches S'_a and S'_b of DC-DC boost converter. During conduction, S'_6 and S'_8 act as a snubber to protect the boost converter switches. During the turn-on period ($t = T'_{on3}$), switches

Table 2: Qualitative study of proposed work with other popular methods in literature.

Parameter	Ref [14]	Ref [15]	Ref [17]	Ref [18]	Ref [19]	Ref [20]	Proposed converter
Number of PV/DC sources required	3	4	3	3	3	3	2
Number of power electronic switches/phase	12	12	12	8	14	18	10
Number of gate drivers	6	6	6	3	6	10	3
TSV	176.3	153.4	No data	No data	No data	162.4	148.6
Voltage level of inverter	7	9	7	7	7	7	7
Series connected DC sources or transformer requirement at inverter	✓	✓	✓	✓	✓	✓	×
Efficiency	85.3	88.4	82.1	No data	No data	86.4	90.9

H: high; L: low; ✓: mandatory; ×: not mandatory.

S_a' and S_b' remain conducting to linearly rise the inductor current L_3 and L_4 from I_1' to I_2' and from I_3' to I_4', respectively. The input energy given to the inductor L_3 from the PV source voltage V_{dc3} is given in Equation (31).

$$E_{i5} = (V_{dc3} + V_{dc4}).(I_{s3} + I_{s4}).T'_{on3}. \quad (31)$$

At time instant $t = T'_{off3}$, the switches S_a' and S_b' are turned off, and the corresponding inductor current L_3 and L_4 current is observed to fall linearly from I_2' to I_1' and I_4' to I_3', respectively. The energy released from the inductors L_3 and L_4 to the snubber module can be estimated as follows:

$$E_{o5} = [(V_{ob3} - V_{dc3})I_{s3} + (V_{ob4} - V_{dc4})I_{s4}].T'_{off3}. \quad (32)$$

The difference in voltage across the capacitors C_3 and C_4 are articulated using Equation (33).

$$\Delta V_{C_3} + \Delta V_{C_4} = I_{o3} * \left[\frac{V_{ob3} - L_3\left(I'_2 - I'_1\right)}{V_{ob3} * f * C_3}\right] + I_{o4} * \left[\frac{V_{ob4} - L_4\left(I'_4 - I'_3\right)}{V_{ob4} * f * C_4}\right]. \quad (33)$$

$$V_{BN} = (V_{ob3} + V_{ob4}) \sin(\omega t + 240). \quad (34)$$

The expected output voltage waveforms for 1Φ and 3Φ inverter systems are represented in Figures 5(a) and 5(b), respectively. The equations for estimating the highest phase and line voltages of 3ϕ BMLDCLC are as follows.

$$V_{RY} = \sqrt{3}(V_{ob1} + V_{ob2} + V_{ob3} + V_{ob4}) \sin\left(\omega t + \frac{\pi}{6}\right), \quad (35)$$

$$V_{YB} = \sqrt{3}(V_{ob3} + V_{ob4} + V_{ob5} + V_{ob6}) \sin\left(\omega t - \frac{\pi}{2}\right), \quad (36)$$

$$V_{BR} = \sqrt{3}(V_{ob5} + V_{ob6} + V_{ob1} + V_{ob2}) \sin\left(\omega t + \frac{\pi}{2}\right). \quad (37)$$

Table 3: Load specifications of three-phase BMLDLC.

RL load		Motor drive load	
Parameter		Parameter	
R	26 Ω	V	440 V
L	30 mH	I	12 A
Z	27.6 Ω	P	5 HP
		R	26 Ω
		L	30 mH
		Z	27.6 Ω
		Inertia	0.0146 kg.m^2

For a better understanding of modes of operation with the proposed BMLDCLC system, six different modes of each phase are presented in Figure 6. Further, the equivalent circuit gives a detailed understanding of the on and off states of the power electronic switch to brief current flow in the proposed converter.

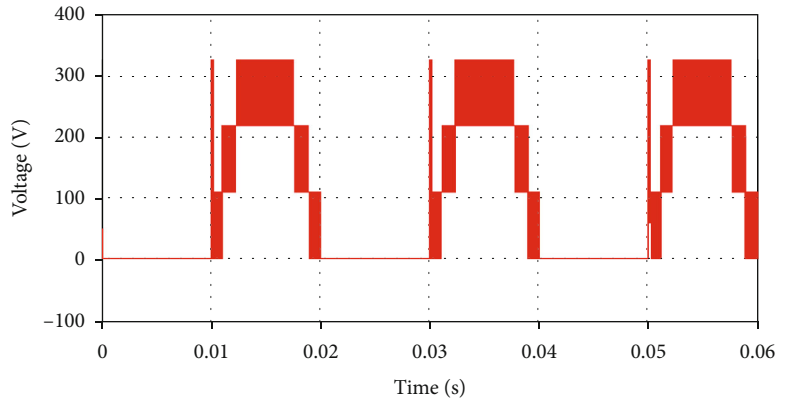
3.2.2. Estimation of Power Losses in BMLDCLC. In general, it is important to estimate the total losses that incur in a MLI. Hence, the mathematical formulations pertinent to various category to calculate losses in the proposed BMLDCLC are given in the following: (i) conduction losses, (ii) switching losses, and (iii) overall standing voltage.

(i) Conduction losses

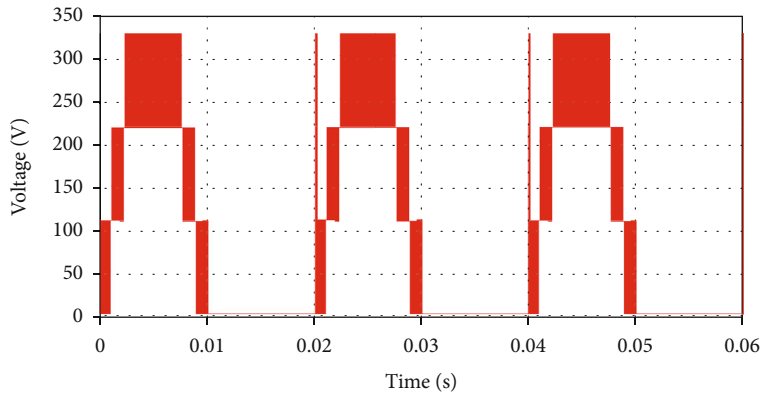
Conduction losses, in general, are associated with the power electronic switch. Nor the proposed BMLDCLC, it is seen that the conduction loss should be calculated for (i) chopper module, (ii) snubber circuit, and (iii) H-bridge inverters at the output. The mathematical equation to estimate the conduction losses of the chopper unit are premeditated in (38).

$$P_B = 3 * \sum_{k=1}^{N\text{switch}} V_{T,k}.i_{sw,k}. \quad (38)$$

Conduction losses of snubber module and H-bridge



(a)



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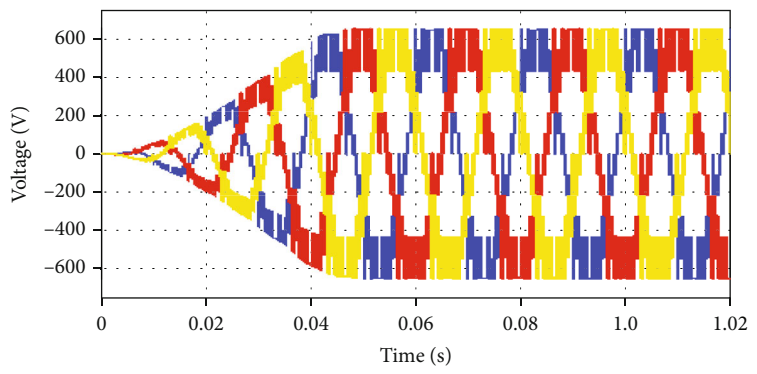
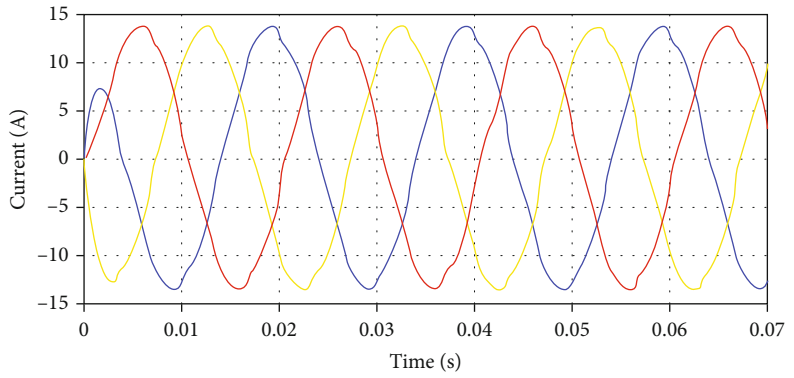


(c)



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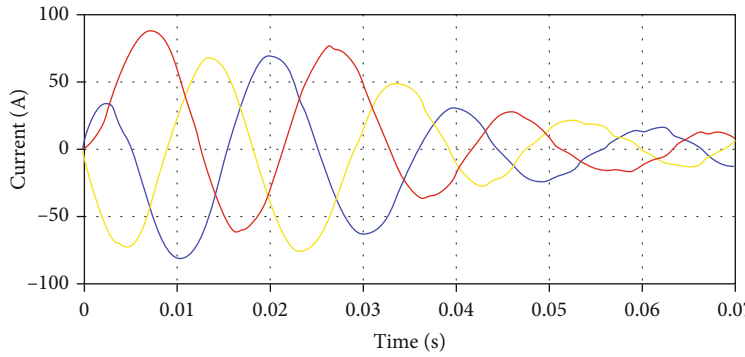

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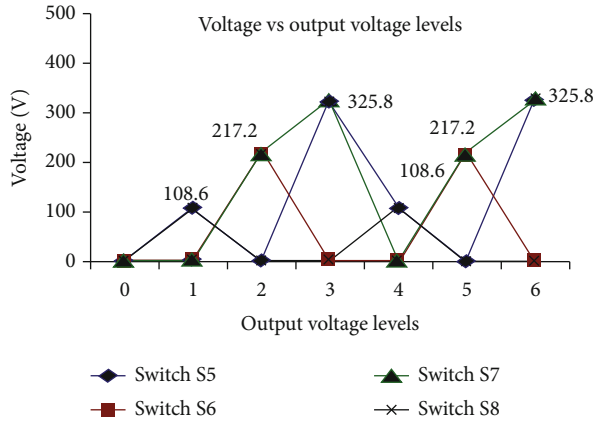


(f)

FIGURE 8: (a) Voltage across H-bridge switches S_1 and S_2. (b) Voltage across H-bridge switches S_3 and S_4. (c) Output line voltage of 3ϕ BMLDCLC. (d) Load current 3-phase BMLDCLC—RL load. (e) Load current 3-phase BMLDCLC—motor drive. (f) Blocking voltage of DC-link switches.

DC to AC converter switches are analyzed as represented in Figure 2(c) and expressed by Equations (39) and (40).

$$P_{\mathrm{DCLM}} = \frac{3}{\pi \int_0^{\pi} p_{\mathrm{DCLM}}(t)\, d\omega t}, \tag{39}$$

$$P_H = \frac{3}{\pi \int_0^{\pi} p_h(t)\, d\omega t}. \tag{40}$$

The power losses of the suggested system are given by

$$P_{\mathrm{BMLDCLC}} = P_B + P_{\mathrm{DCLM}} + P_H. \tag{41}$$

(ii) Switching losses

Similar to conduction losses, switching losses of a power electronic switch are also estimated for (i) boost converter and (ii) snubber module. Switching loss pertinent to the DC-DC boost converter is estimated for both on and off time of the power electronic switch, and it is mathematically given in Equations (42) and (43).

$$E_{\mathrm{on},B} = 3 * \sum_{k=1}^{N\mathrm{switch}} V_{sw,k}.i_{sw,k}.t_{\mathrm{on}}, \tag{42}$$

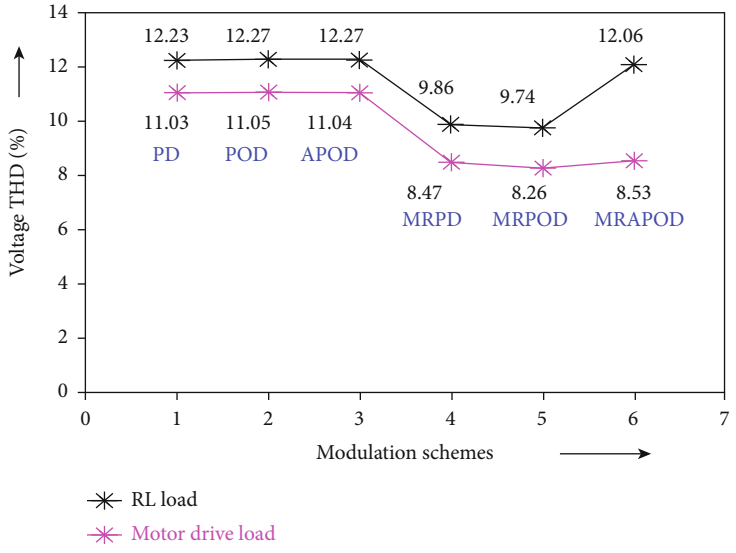
$$E_{\mathrm{off},B} = 3 * \sum_{k=1}^{N\mathrm{switch}} V_{sw,k}.i'_{sw,k}.t_{\mathrm{off}}. \tag{43}$$

The on state and off state loss of a "k^{th}" switch are estimated by using the formulation given in (44) and (45).

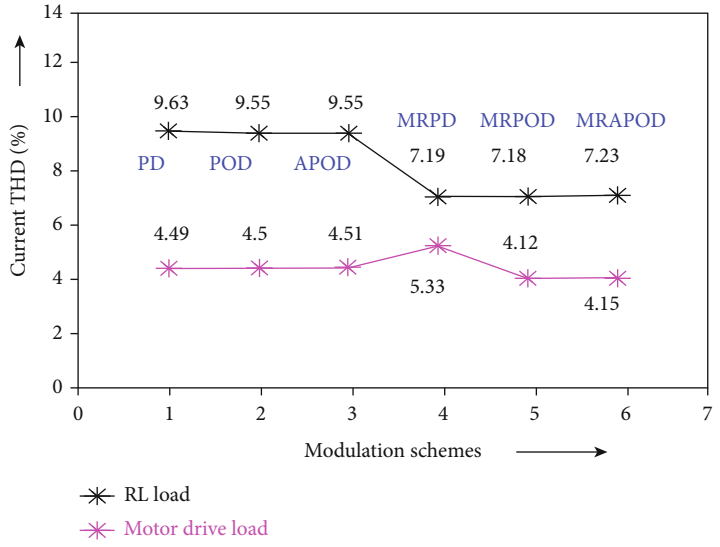
$$E_{\mathrm{on},K} = \frac{(V_{sw,k}.i_{sw,k}.t_{\mathrm{on}})}{6}, \tag{44}$$

$$E_{\mathrm{off},k} = \frac{\left(V_{sw,k}.i'_{sw,k}.t_{\mathrm{off}}\right)}{6}, \tag{45}$$

where $E_{\mathrm{on}-k}$ is the energy loss during the switch on, $E_{\mathrm{off}-k}$ is the energy loss during the switch off, and i_t is the source current flowing all the way through the power semiconductor switch subsequent to turning on. Further, on estimating the losses in a power electronic switch, the total losses in

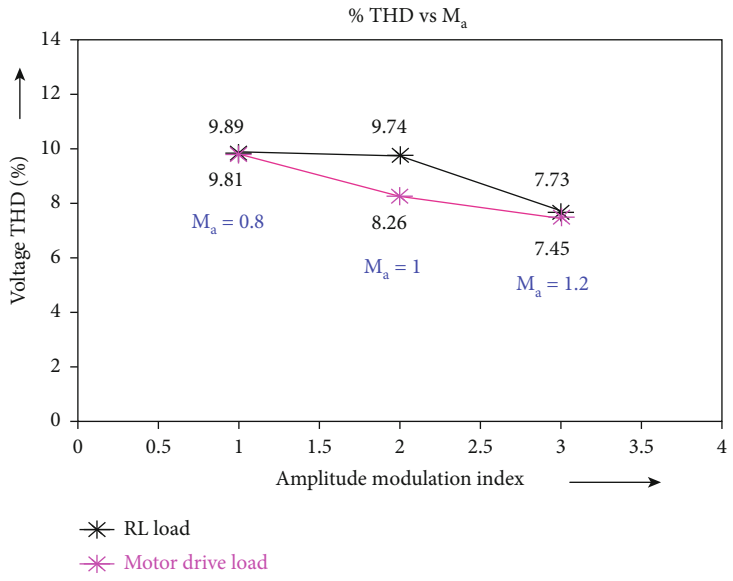


(a)

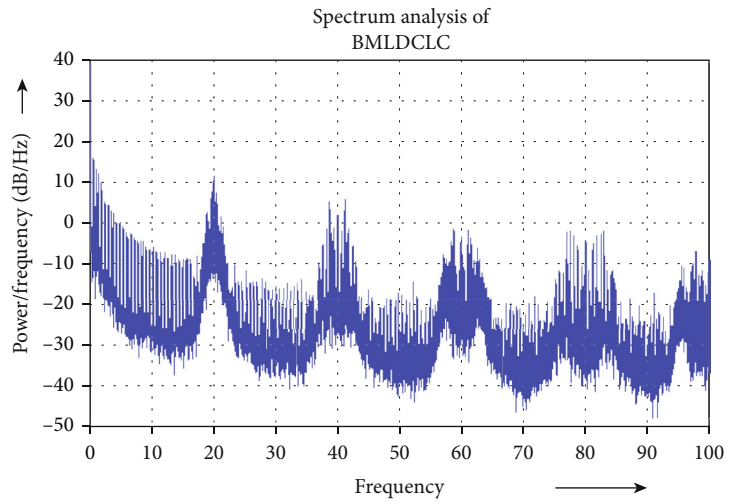


(b)

Figure 9: Continued.



(c)



(d)

Figure 9: THD investigation of the output voltage of 3ϕ BMLDCLC. (b) THD investigation of the load current of 3ϕ BMLDCLC. (c) Power Signal Density analysis for the output voltage of 3ϕ BMLDCLC.

the DC-link module can be calculated. Mathematical formulations to estimate the loss during on and off time are given in Equations (37) and (38), respectively.

$$E_{\text{on,DCLM}} = \sum_{k=1}^{N_{\text{switch}}} E_{\text{on},K}. \tag{46}$$

$$E_{\text{off,DCLM}} = \sum_{k=1}^{N_{\text{switch}}} E_{\text{off},K}. \tag{47}$$

(iii) Overall standing voltage (OSV)

Overall standing voltage (OSV) of the proposed unit is calculated as

$$\text{TSV} = \left(\frac{7s^2 + 5s - 2}{2}\right) V. \tag{48}$$

The average voltage drop at the switching frequency is 19.53 V and 20.68 V for the rated output voltage system. Hence, the average switching loss is considered as 148.6 W. Hence, the efficiency of the proposed converter is 90.9%. Losses and efficiency analysis are represented in Figure 5(e).

3.3. A Comprehensive Analysis on the Operation of BMLDCLC System in Grid-Connected Mode: Case Study.

Table 4: Harmonic investigation of three-phase BMLDCLC fed RL load (rated voltage).

Order of harmonics	$M_a = 0.8$		$M_a = 1$		$M_a = 1.2$	
	Voltage harmonics (%)	Current harmonics (%)	Voltage harmonics (%)	Current harmonics (%)	Voltage harmonics (%)	Current harmonics (%)
3	0.29	0.21	0.22	0.09	0.14	0.06
5	4.69	3.03	4.35	2.92	8.52	4.78
7	4.62	2.37	3.24	2.15	6.72	2.85
9	0.07	0.05	0.15	0.05	0.09	0.03
11	4.58	1.58	2.24	1.06	3.61	1.13
13	3.67	1.38	1.78	0.8	2.79	1.09
15	0.09	0.02	0.1	0.02	0.1	0.03
17	2.34	1.01	1.5	0.25	2.14	0.87
19	1.98	0.89	1.42	0.21	2.02	0.66

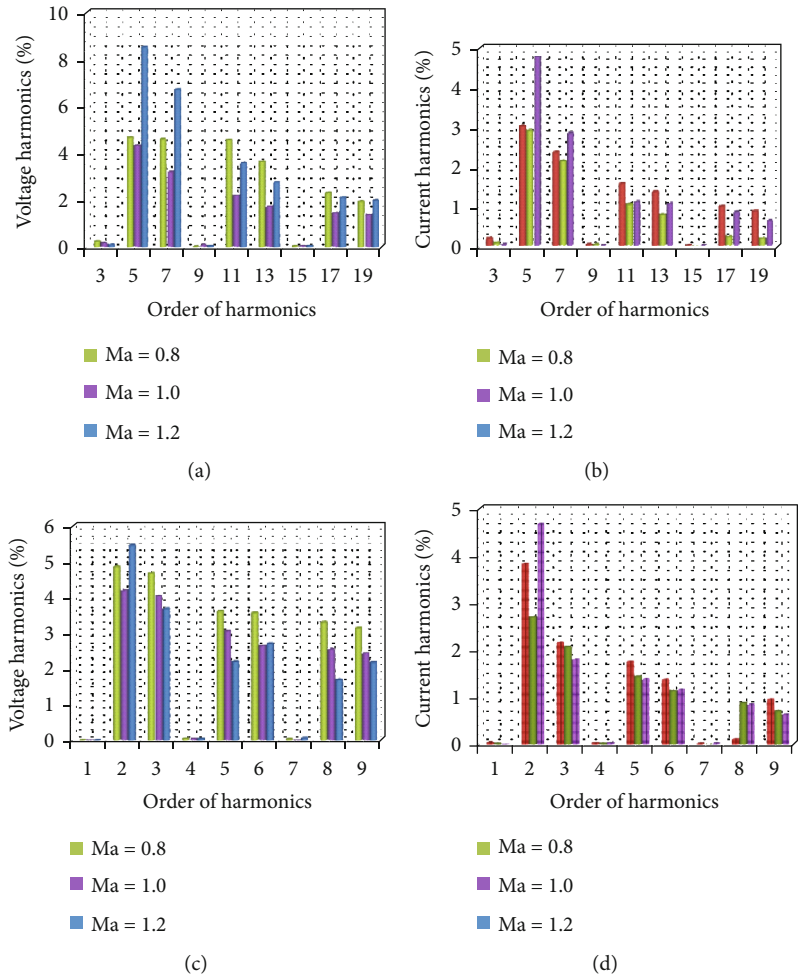


Figure 10: (a) Harmonic analysis of rated output voltage. (b) Harmonic analysis of load current. (c) Harmonic analysis of output voltage of 120 V. (d) Harmonic analysis of load current for 120 V output voltage system.

As the proposed converter arrangement is highly encouraged to get connected for a grid-connected mode, a quantitative case study on its operation to grid-connected modes is presented in this section. Design specifications of the recommended system and the data are related to voltage, and power ratings are represented in Table 1. Also, the schematic of the proposed converter connected to the utility is given in Figure 7(a). From the figure, it is understood that the

Table 5: Harmonic investigation of three-phase BMLDCLC fed RL load (for 120 V).

Order of harmonics	$M_a = 0.8$		$M_a = 1$		$M_a = 1.2$	
	Voltage harmonics (%)	Current harmonics (%)	Voltage harmonics (%)	Current harmonics (%)	Voltage harmonics (%)	Current harmonics (%)
3	0.03	0.05	0.04	0.03	0.02	0.02
5	4.87	3.82	4.21	2.71	5.46	4.67
7	4.69	2.16	4.06	2.08	3.69	1.81
9	0.08	0.04	0.08	0.03	0.07	0.05
11	3.63	1.76	3.08	1.45	2.22	1.39
13	3.58	1.38	2.67	1.15	2.72	1.17
15	0.06	0.03	0.04	0.01	0.09	0.04
17	3.32	0.12	2.57	0.89	1.71	0.86
19	3.16	0.96	2.46	0.72	2.20	0.65

proposed system has a battery bank and an isolation switch. Note that isolation is mandatory to disconnect it from the utility. Further, the proposed seven-level BMLDCLC connected to a three-phase load system offers five operating modes as follows: (i) bypass mode, (ii) off line mode, (iii) on line mode, (iv) battery-operated mode, and (v) grid-connected mode.

The operating characteristics of various modes in the grid-connected system are discussed in detail as follows:

(i) In grid-connected mode, subpanel and isolation switches are activated, and the excess power produced by the solar PV panels is imported to the grid

(ii) In off line mode, the load is operated through a solar fed BMLDCLC system. Note that subpanel and isolation switches are in off state during off line mode

(iii) In on line mode, the load is operated through solar fed battery-operated BMLDCLC system, and in the same mode, the energy storage device is acquired to completely store the energy by the solar panels through the charge controller

(iv) Battery operating mode is activated only for emergency and backup loads

In bypass mode, subpanel and isolation switches are activated, and the load is directly connected to the grid. This mode is activated only when solar power is not competent to attend to the load demand. It is noteworthy to mention here as master control manages the operation of the entire system, including the battery bank and the grid-isolation device.

From the specifications of Table 2, it is anticipated that grid-connected systems need nominal power components and PV panels compared to topologies proposed in [14, 15, 17–20]. Thus, it is confirmed that the proposed converter reduces the overall cost for grid-connected UPS applications. The inductor values of L_1 and L_2 pertinent of boost converters 1 and 2 are calculated using the following equations:

$$L_1 = \frac{V_{\mathrm{dc1}} * (V_{ob1}\text{-}V_{\mathrm{dc1}})}{(I_2 - I_1) * f * V_{ob1}}, \tag{49}$$

Table 6: Properties of various metals.

Material	Specific heat (kJ/kg°C)	Thermal conductivity (W/m°C)
Aluminum	0.99	205
Iron	0.45	79.5
Steel	0.46	50.2
Copper	0.39	385
Brass	0.38	109
Zinc	0.38	112
Water	4.18	0.6
Glass	0.84	0.8
Silver	0.23	406

$$L_2 = \frac{V_{\mathrm{dc2}} * (V_{ob2}\text{-}V_{\mathrm{dc2}})}{(I_4 - I_3) * f * V_{ob2}}. \tag{50}$$

To contribute to a fair comparative study, the BMLDCLC system is also presented in Figure 7(b) with a transformer and single-phase supply. However, the system is extremely complicated, and the use of transformers leads to higher costs. Detailed discussions on a transformerless MLI configuration fed UPS system related to (i) transient analysis, (ii) ripple current analysis, (iii) sliding mode controller analysis, and (iv) robustness and multiport analysis can be referred in [31–34].

4. Simulation Results and Discussion

The converter is tested with two various loads (i) RL load and (ii) motor drive load. Further, software-based system modelling is performed in a MATLAB Simulink environment with a system configuration of 4 GB RAM and an *i3* processor. For simulations, SPV panels are associated in series and parallel approaches to attain the source voltage $V_{\mathrm{dc1}}\text{-}V_{\mathrm{dc6}}$. Note that 250 watts PV sources having open-circuit voltage of 36 V and short circuit current as 8 A are used. Further, battery banks are connected in series and parallel approaches to achieve the source voltage of a stepped DC-link hybrid converter and to achieve an uninterrupted power supply for industrial applications. It is noteworthy to mention here that 12 V batteries having 85 AH capacity

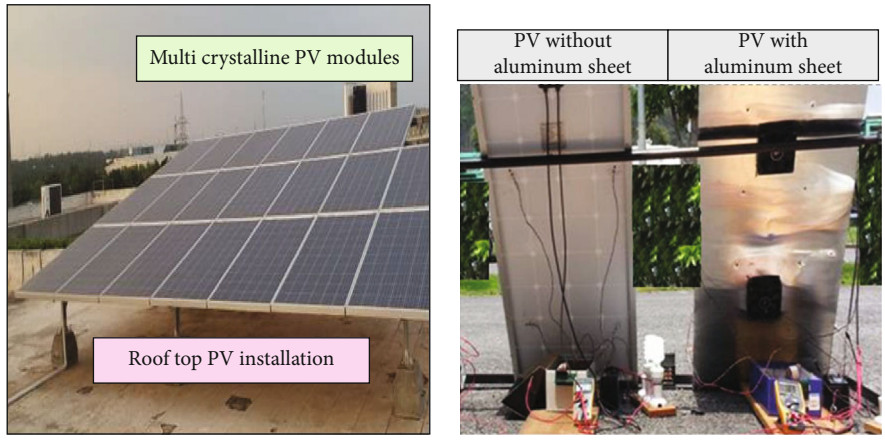


Figure 11: (a) Solar plant; (b) experimental analysis with aluminum metal sheet.

are used as a backup to serve in the absence of PV. BMLDCLC initiates its operation as boost chopper; source voltages of 36 V and 72 V are boosted up to 109 V and 216 V, respectively, to achieve the rated voltage of 415 (V_{rms}). Furthermore, the power electronic switches of the DC-DC boost converter are fed with a 10 kHz switching frequency to maintain the DC-link voltage. Additional grid-powered storage with an inverter system is also provided to run the backup loads for emergency purposes. The load specifications are represented in Table 3.

The simulation results of the snubber-assisted module are presented in Figures 8(a) and 8(b), respectively. From the acquired waveforms, it is incidental that four switch back-end conversions are performed at the zero-crossing points for every 10 ms, as presented in Figure 8(a). Thus, ensuring that switching losses is minimal. In addition, the reproduction of three-phase voltage with definite steps in the waveform gives the judicial validation of the proposed MLI. In order to operate the converter switches efficiently, peak inverse voltage across front-end switches is considered at different levels, as presented in Figures 8(c) and 8(d). Further, the voltages measured at switches give three various DC values to confirm the seven operations of the inverter. Stability analysis has been carried out for the proposed system, and it is inferred that the system is operated in equilibrium with respect to electrical parameters only after 0.05 ms. From Figure 8(c), it is noticed that the steady-state voltage is achieved only after 0.05 ms. To measure the appropriate modulation index with the proposed system, various pulse width modulation (PWM) schemes [35–37] are investigated for both RL load and motor drive load as shown in Figures 9(a) and 9(b), respectively. Over and above, the MCMRPOD-PWM technique is found effective to have reduced THD without filter component, and the same is adopted for the proposed converter topology. Further, the system has also been examined for different modulation indexes (M_a) like 0.8, 1.0, and 1.2, as shown in Figure 9(c). From the results, it is established that the projected system fed RL load and motor drive load systems generate lower THD (without filter component) values of 7.45% and 7.73%, respectively, for $M_a = 1.2$. Also, it is evidenced that hybrid converter generates 40% higher 5^{th} and 7^{th}-order voltage and current harmonics. In order to notice the strength of power signals, spectrum analysis has been conducted, and the results are shown in Figure 9(d).

PSD for the inverter voltage of the recommended inverter topology at 10 kHz, 20 kHz, 30 kHz, and 40 kHz is -6 dB/Hz, 12 dB/Hz, -18 dB/Hz, 8 dB/Hz, and -2 dB/Hz, 14 dB/Hz, -16 dB/Hz, and 4 dB/Hz, respectively. The ratio of output voltage in the recommended seven-level inverter fed RL and motor drive load systems at 10 kHz, 20 kHz, 30 kHz, and 40 kHz is 1.25%, 9.95%, 0.31%, 6.27%, and 1.98%, 12.5%, 0.39%, and 3.96%, respectively. Thus, the efficiency of the proposed converter is estimated as 90.9%, and the proposed three-phase stepped DC-link inverter has improved efficiency of 4.7% and 12.9%, respectively, against two-level and three-level boost chopped fed inverter configurations.

For an inverter, individual order harmonic ensures the converter efficiency. Hence, the voltage and current harmonics of the proposed converter are tested and analyzed for three various modulation index (M_a). The values pertinent to the order of harmonics are numerically presented in Table 4. For better understanding, a bar chart to measure harmonics in output voltage and current is plotted as shown in Figures 10(a) and 10(b). From the figure, it is noticed that 5^{th}-order harmonics get augmented for overmodulation ($M_a = 1.2$) state. In addition, the average voltage ratio for the proposed topology fed RL and motor drive load system is 4.44% and 4.70%, respectively. The system parameters are designed for the inverter output voltage of 600 V (Vm). The average output voltage of boost chopper units are as follows:

Case 1.

$$V_{ob1} = \frac{36}{(1 - 0.67)} \ (\text{assuming } K_1 = 0.67 \text{ for } M_a = 1),$$
$$V_{ob1} = 109\text{V}, \tag{51}$$

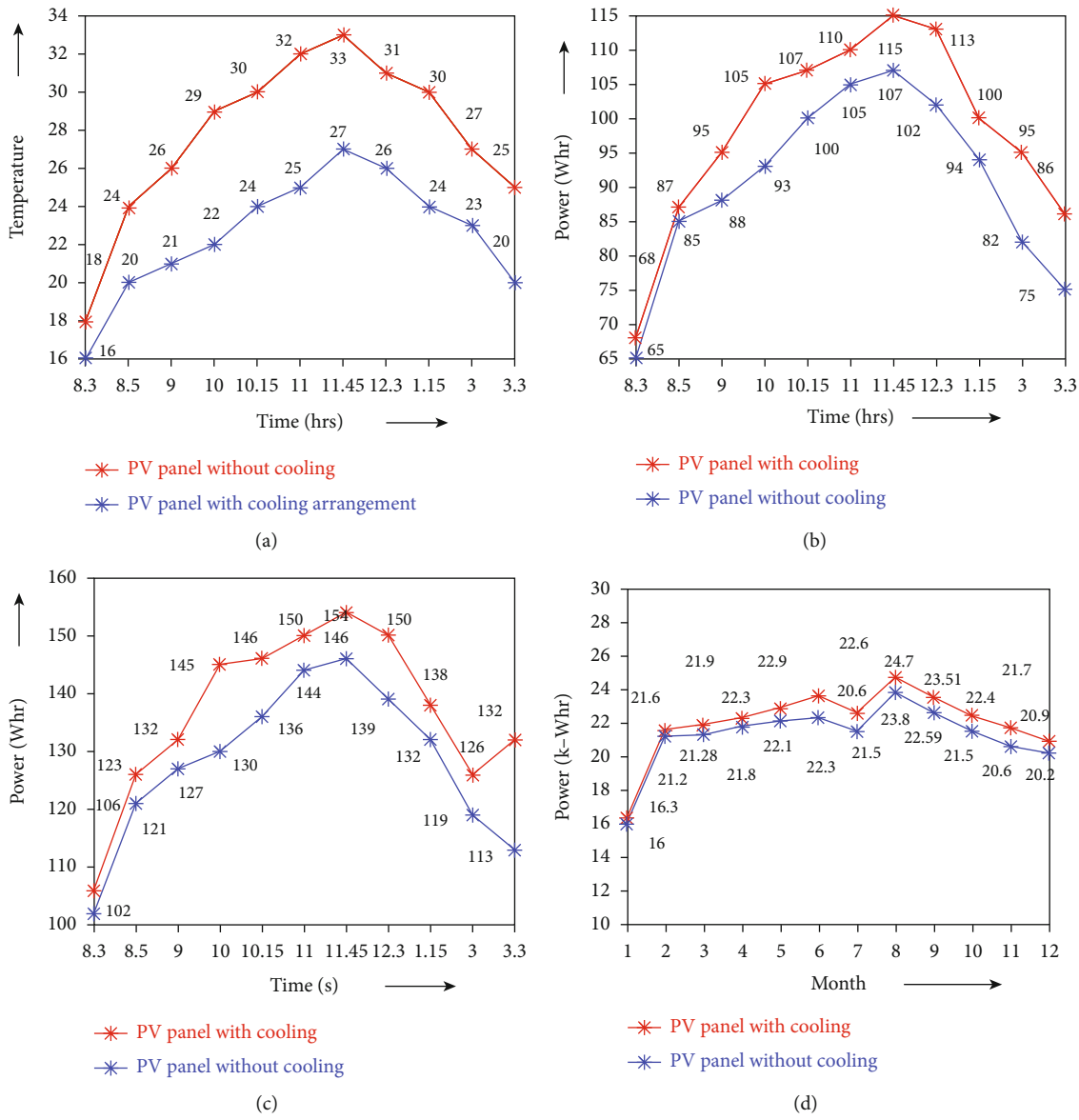


Figure 12: (a) Thermal characteristics of solar panel in the month of August. (b) Power generation in the month of January. (c) Power generation in the month of June. (d) Overall power generation for a year.

$$V_{ob1} = \frac{72}{(1-0.67)} \text{ (assuming } K_1 = 0.67 \text{ for } M_a = 1),$$
$$V_{ob1} = 216\text{V}, \tag{52}$$

Case 2.

$$\text{V}_{ob1} = \frac{36}{(1-0.73)} \text{ (assuming } K_1 = 0.73 \text{ for } M_a = 1.2),$$
$$\text{V}_{ob1} = 140\,\text{V}, \tag{53}$$

$$\text{V}_{ob1} = \frac{72}{(1-0.73)} \text{ (assuming } K_1 = 0.73 \text{ for } M_a = 1.2),$$
$$\text{V}_{ob1} = 280\,\text{V}. \tag{54}$$

Since the provisions to visualize hardware results for rated voltage is not possible, the hardware design is made for 120 V phase voltage. Thus, to validate the proposed system with 120 V as output voltage, the simulation trials of the proposed converter are repeated, and the results pertinent to the modulation index are shown in Figures 10(c) and 10(d). Further, the detailed investigations pertinent to numerical are given in Table 5.

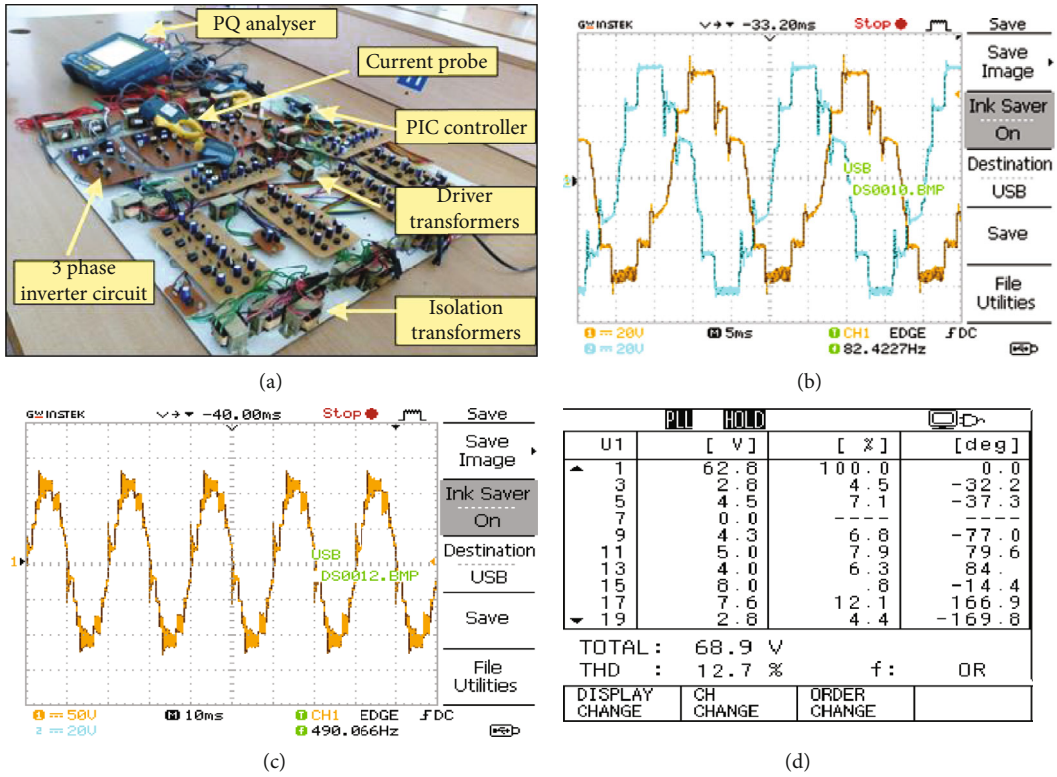


Figure 13: (a) Hardware setup of three-phase seven-level BMLDCLC system. (b) Output phase voltage of three-phase BMLDCLC. (c) Output line voltage of three-phase BMLDCLC. (d) THD spectrum.

5. Hardware Experimentation

To experiment with the proposed converter, a lab-made prototype model is exclusively constructed. Further, 250 watts PV panels installed on the rooftop of the electrical engineering building of KPR Institute of Engineering and Technology is utilized as the source. In general, SPV panels are nonimmune to geographical and seasonal variations. Further, the overall efficiency gets affected negatively by a rise in temperature. Additionally, excessive heat may significantly increase the output current, which may account for power loss up to 10-22 percentage, hence an attempt to cool PV panels with the help of temperature coefficient. In general, PV panel manufacturers provide a "temperature coefficient" (TC) value for each SPV panel, whose value varies based on manufacturing technology and materials used. This parameter can be used to determine the amount of power loss for each one degree Celsius of temperature rise.

5.1. Design of Thin Aluminum Sheet-Based Cooling System. The panel's temperature is one of the key components to drag the overall power; hence, a new method to reduce the panel temperature is explored by using thin aluminum sheet. Aluminum was chosen for its high thermal conductivity (267 watts per metre-kelvin) and low weight per square. For a fair comparative study, the thermal conductivity and specific heat of various metals are presented in Table 6. Further, the implementation cost was also found economical with aluminum metal. The experimental setup of the PV system is shown in Figures 11(a) and 11(b), respectively. From Figure 11(b), it is seen that one of the PV panels was used as it is, while the other one was wrapped with thin aluminum sheet in the rear, and the setup was also braced with two DC-cooling fans to enhance the cooling effect. The cooling fain decreases the panel temperature and helps to extract the maximum available power.

The experimental study for cooling is extended for one year, and the instantaneous voltage and power values are recorded. Further, the measure of PV thermal characteristics (PV panel temperature) is measured for the month of August and presented as shown in Figure 12(a). From the figure, it is seen that aluminum-based cooling arrangement has always maintained the temperature in limits compared to the original. To understand the impact of power generation of PV panels with cooling, the power generated from the PV plant is recorded for the months of January and June which is shown in Figures 12(b) and 12(c), respectively. Further, the total power yield for a year is also presented as in Figure 12(d). In all the aforementioned cases, the cooling effect with PV panels had a major impact to improve the power extraction from PV systems. From Figure 12(a), it is inferred that aluminum-based cooling arrangement system has an average of 5°C to 6°C better hear absorption or removal which is equivalent to 12.9% of total heat removal. As a safety measure to protect PV from dust accumulation, panels were coated with hydrophobic nano coating (HNC)

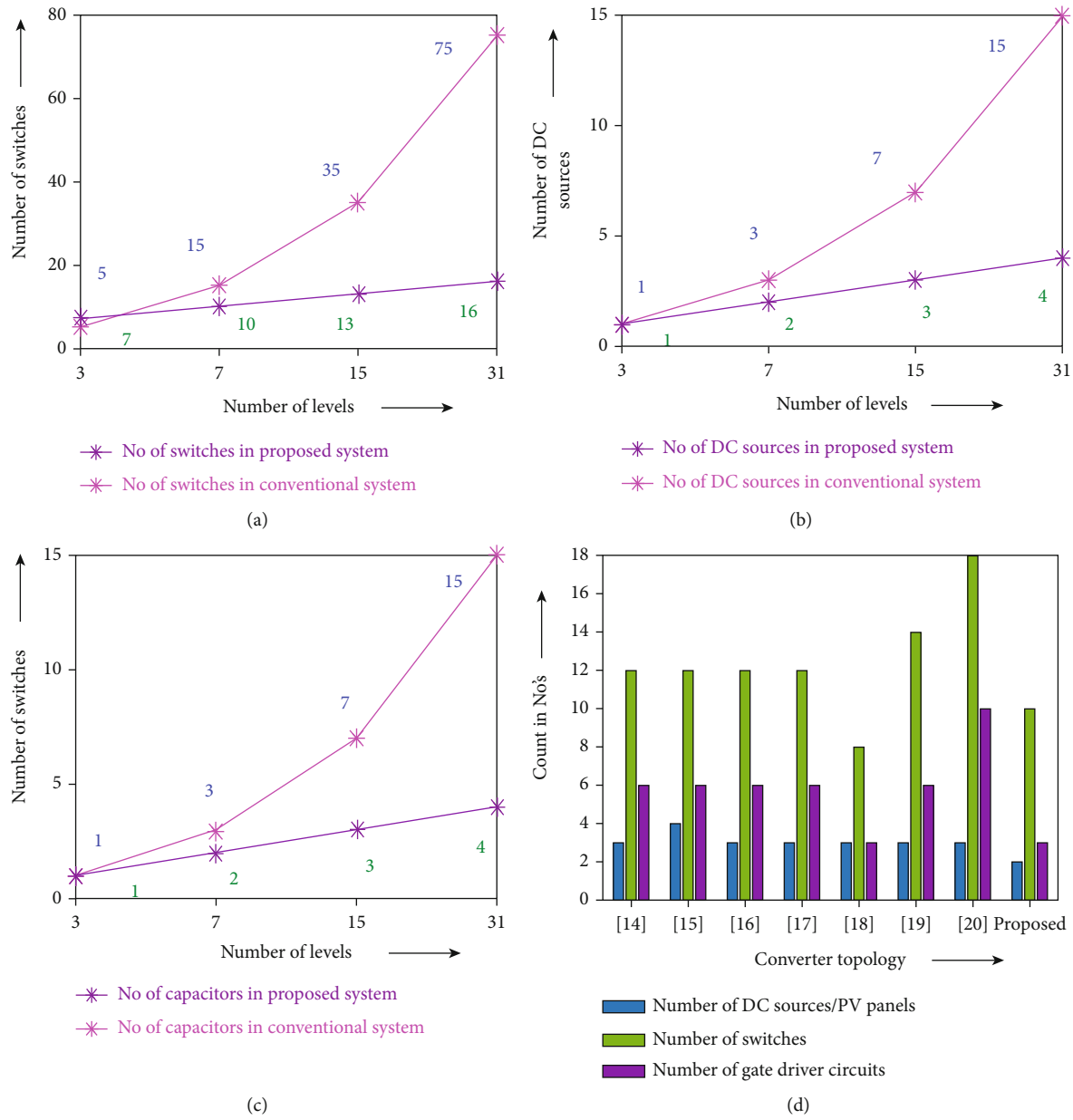


FIGURE 14: Comparative analysis of controlled switches. (b) Comparative analysis of DC sources. (c) Comparative analysis of capacitors. (d) Comparative analysis with different seven-level hybrid converter topologies.

solution. This enabled the PV to prevent from (i) accumulation of water drops, (ii) dust, and (iii) bird droppings over SPV panel surface. In addition, the arrangement has enhanced the surface contact, and the light transfer to the SPV cells was increased, ensuring the higher amount of electricity production. It is noteworthy to mention here that the use of HNN has decreased cleaning of PV panel on average.

5.2. BMLDCLC Setup. The entire system is designed and implemented as prototype model as represented in Figure 13(a). PIC microcontroller is used for providing gating sequence of the converter. Hardware results (i) output phase voltage (V_{RN} and V_{YN}) and (ii) line voltage of the 3ϕ seven-level BMLDCLC scheme are shown in Figures 13(b) and 13(c), respectively. To evaluate the virtues and system performance, the operation of proposed BMLDCLC is tested for diverse modulation indices and its electrical parameters are specified in Table 6. From the table, it is inferred that the individual harmonic is within the limit for the modulation index $M_a = 1.0$. Thus, the same is recommended for real-time operation. From the examination, it is authenticated that the 3rd, 5th, and 7th-order harmonics are mitigated through the switching schemes. Furthermore, to authenticate the simulation results, power quality analysis was conducted experimentally and the results are represented in Figure 13(d). From the investigation, the THD of the recommended system is 12.7%.

6. Comparative Analysis

In order to compare the proposed work comprehensively in a common platform, a qualitative assessment of anticipated BMLDCLC topology is made with other literatures as represented in Table 2. Various parameters considered for comparison are as follows: (i) PV panels/DC sources required, (ii) power semiconductor switches used, (iii) gate drivers used, (iv) levels in voltage stress, (v) output voltage levels, and (vi) series connected DC sources. Also, an interesting comparison related to parameters (i) number of power electronic switches, (ii) number of DC sources, and (iii) number of capacitors are considered for conventional MLI (three, seven, fifteen, and thirteen level), and it is compared with proposed inverter topology. This comparison is benchmarked as bar chart and presented in Figures 14(a)–14(c), respectively. From the comparative study, it is inferred that the proposed seven-level BMLDCLC has comparatively utilized 66.66% less (i) switching components, (ii) DC sources, and (iii) capacitors. Further, the same analysis is extended for various literature works, and it is compared with proposed inverter topology as bar chart in Figure 14(d). Yet, the proposed system topology has emerged as one of the best alternatives for existing seven-level inverter configurations. Thus, on overall, the proposed system has greater scope for real-time implementation towards industrial applications is proved. Also, the experimental findings and simulation results confirm that BMLDCLC has conceived greater interest to be as a suitable replacement for existing three-phase seven-level MLI. It is evident from Table 2 that the proposed system requires lesser number of power switches and DC sources. Analysis on the basis of system requirements has been made for various configurations. Hence, from the abovementioned table and analysis part, the authors have given a clear picture about the cost reduction for the proposed system. The comparative study confirms that the proposed 7-level BMLDCLC system has only utilized 33.33% switches compared to other conventional MLI schemes. Hence, the proposed system has the reduced cost of 175.24 US dollars compared with conventional CMLI.

The proposed BMLDCLC configuration required at least six DC sources for synthesizing 7-level three-phase AC output, which is the main limitation of the proposed system over conventional three-phase voltage source inverter system. Also, the proposed BMLDCLC configuration required three boost chopper units for achieving 7-level three-phase AC output. In future, the above constraints can overcome by integrating all the submultilevel modules with a common H-bridge inverter module.

7. Conclusion

A new BMLDCLC topology is proposed in this research work for industrial applications. Further, effectiveness of converter in real-time operating conditions is analyzed using a prototype model, and the following conclusions are arrived.

(i) The BMLDCLC is effective to reduce stress on the primary DC-DC converter since two DC sources are used to serve the DC-link voltage

(ii) The case study on grid-connected systems reveals the importance of proposed design to serve as a solution for energy management system

(iii) The comparative study confirms that the proposed 7-level BMLDCLC system has only utilized 33.33% switches compared to other conventional MLI schemes

(iv) From the power frequency spectrum analysis and perceived output waveforms, the recommended power converter is proved to reduce 41% voltage stress

(v) From the circuit analysis, it is confirmed that the output voltage is achieved without any series connected DC sources and inverter and transformer. This certainly proves the cost-effectiveness of BMLDCLC compared to conventional MLIs

(vi) A converter efficiency of 90% is recorded in real-time investigation

Abbreviations

APOD: Alternate phase opposition disposition
AC: Alternating current
M_a: Amplitude modulation index
BCMLI: Boost cascaded multilevel inverter
CLSPWM: Carrier level shifted pulse width modulation
CDCLHBI: Cascaded DC-link H-bridge inverter
CMLI: Cascaded multilevel inverter
CSI: Current source inverter
dsPIC: Digital signal peripheral interface controller
DC: Direct current
FCMLI: Flying capacitor multilevel inverter
M_f: Frequency modulation index
IGBT: Insulated gate bipolar transistor
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
MRAPOD: Modified reference alternate phase opposition disposition
MRPD: Modified reference phase disposition
MRPOD: Modified reference phase opposition disposition
MLI: Multilevel inverter
PD: Phase disposition
POD: Phase opposition disposition
PSD: Power spectral density
PWM: Pulse width modulation
SPWM: Sinusoidal pulse width modulation
SVM: Space vector modulation
SVPWM: Space vector pulse width modulation
THD: Total harmonic distortion
UPS: Uninterrupted power supply
VSI: Voltage source inverter
ZVS: Zero voltage switching.

Data Availability

The data used to support the findings of this study are included in the article.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this article.

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Research Article

Design of a High Step-Up DC-DC Converter with Voltage Doubler and Tripler Circuits for Photovoltaic Systems

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In this paper, a high step-up DC-DC interleaved boost converter is proposed for renewable sources with low voltages such as photovoltaic module and fuel cell. The proposed converter uses interleaving method with an additional voltage doubler and tripler circuit. In the proposed converter, the inductor at all phases is operated to gain high voltage through voltage doubler and tripler circuit capacitors with suitable duty cycle. The proposed topology operates in six switching states in one period. The steady-state analysis and operating principle are examined comprehensively which shows numerous improvements over the traditional boost converter. These improvements are high-voltage gain and low-voltage stress across switches. The proposed DC-DC interleaved boost converter has a gain/conversion ratio four times that of the conventional interleaved boost converter and four times less-voltage stress across the main switches. Simulation has been done in Matlab Simulink on a 70% duty cycle, and results are compared with conventional interleaved boost converter. For an input voltage of 15 volts, the proposed converter is able to generate an output voltage of 200 volts at 70% duty cycle with a voltage stress of 50 volts across main switches, whereas traditional interleaved boost converter generates 200 volts from same input voltage at 92.5% duty cycle with voltage stress of 200 volts across switches. From simulation results, it is clear that the proposed converter has better performance as compared to conventional interleaved boost converter for same design parameters.

1. Introduction

Renewable energy generation becomes more popular during the last decade. Renewable energy sources, for example, solar, wind, and fuel cell systems, are most effective sources to reduce the power generation crisis all over the world [1]. Energy resources, for example, coal, natural gas, and oil, have various bad influences on nature, such as pollution and greenhouse impacts; also, there is a massive contradiction among the global energy need and the fossil fuel supply. The key matters for human being development are lack of energy and environmental pollution. Renewable sources such as photovoltaic modules are a clean energy source, and their addition to the power system is constantly rising. It will contribute a huge amount of electricity among all the renewable energy sources [2, 3]. The PV grid-connected power system turns into a fast emergent section in the PV market [4]. Power electronics circuits must be followed for using energy sources (wind cells, solar, and fuel) as a front end of the electrical system [5]. Bidirectional DC-DC converters are also needed in the energy storage systems (ESSs), to store the excess energy during production and release it when needed in peak demand or off peak hours; hence, boost converter is required to step up low voltage of storage system [6]. The full utilization of power is generated through PV module, and to satisfy safety requirements, the latest research trend is to

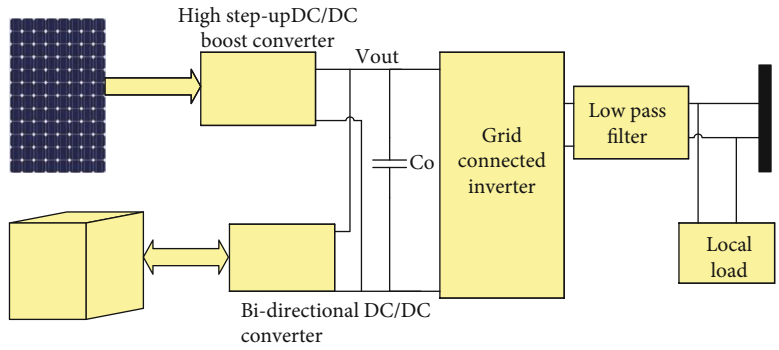

Figure 1: Drawing of the single-phase PV grid-connected power system.

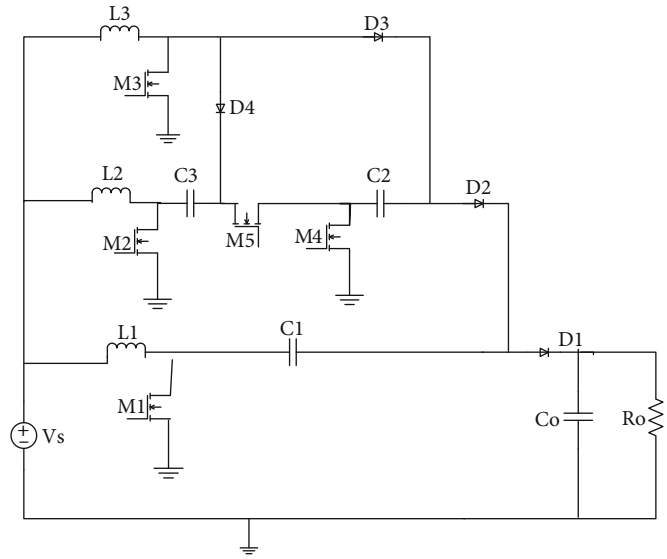

Figure 2: Circuit diagram of the proposed converter.

make parallel arrangement of PV module instead of series. A high DC bus voltage is required for the half-bridge, full-bridge, and multilevel grid inverters. The power in series configuration drops off significantly due to partial shading, particularly in the urban regions and mismatch of modules [7]. In this case, the PV parallel arrangement is more effective than the PV series-connected arrangement due to the functioning of PV modules [8, 9]. H-bridge multilevel inverters or other multilevel configurations are employed to enhance the PV modules output power in grid-connected PV power system [10, 11], but for this, some other power devices are needed, and the cost is increased in these solutions. Renewable sources mostly generate electrical power with small DC voltage. Hence, the electrical power has been produced with low DC voltage, and we know that 1.414 times of AC voltage is needed on the DC side to convert it into the desirable AC voltage. The complete model is shown in Figure 1.

Therefore, DC/DC high step-up converters are required. The conventional boost converters can attain a high gain on a high duty cycle, which causes a reverse recovery problem and high-voltage stress across the switching devices, which decreases the efficiency [12]. A triangle modulation (TRM) scheme decreased circulating current with ZCS behavior for the whole operating range; however, the feasibility of TRM is limited for the operation to gain more than unity [13]. To minimize these issues, it is desirable to plan a DC-DC step-up converter that can attain a high-voltage gain exclusive of high duty cycle, less reverse recovery problem, and improved efficiency with low-voltage stress across the main transistors. Theoretically, boost converter can attain infinite gain, but because of various parasitic in experimental layout, the infinite gain cannot achieve practically. Therefore, to overcome the limitation of such type on gain, different types of solutions have been introduced in the literature. In recent years, switched capacitor voltage boost converter has got more attention because of its exceptional full monolithic integration applications and higher power density as compared with conventional inductor-based voltage boost converters. The multistage switched-capacitor voltage boost converter characteristics can be investigated with no involvement of magnetic components [14, 15]. This particular property allows it to be used in analytical models and estimate the performance of voltage boost converter [16, 17]. Moreover, conventional models by using simple

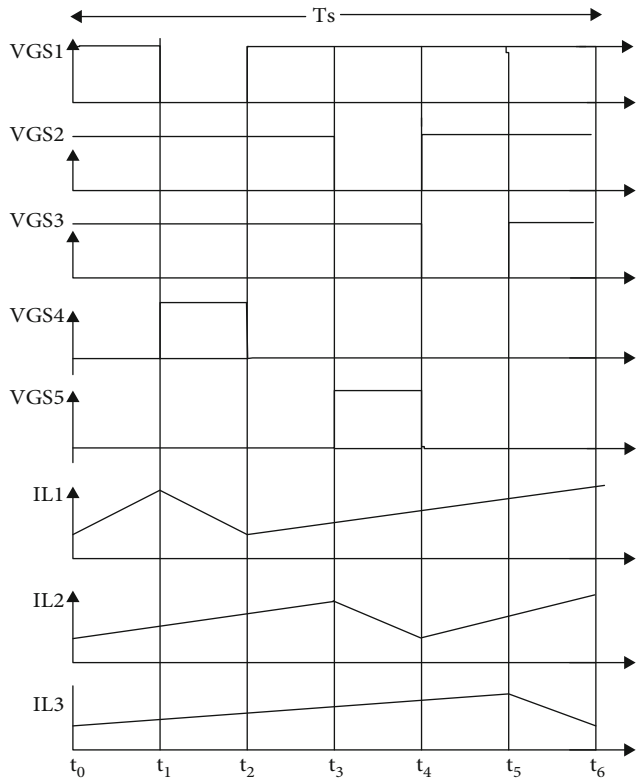

Figure 3: Major waveforms of the proposed converter.

switched-capacitor voltage boost converters have been reviewed in [18]; a small number of reports on a model using the modified switched-capacitor voltage boost converters can be discovered. Furthermore, even though the usual models practice a switching frequency FS and flying capacitance CF to design voltage boost converter, load capacitance CL and complementary switched-capacitor configuration are not taken into account. Hence, the accuracy of the model is not enough and cannot be used in real voltage boost converters. A switched-capacitor voltage boost converter has been used in the power range from monolithic integration to higher power application [19, 20]. Several voltage boost converters have been proposed. Boost converters with switched capacitor are broadly used since they can achieve high-voltage gain by linking voltage boost converters in a cascade [21]. It can generate a high gain, but the overall system efficiency will be reduced because the resultant efficiency will be the product of the efficiencies of the linked converters. Theoretically coupled inductor-based converter increased DC gain, by increasing the turns ratio of the coupled inductor, though the leakage inductance drawback should be thoroughly controlled [22]. Hence, a new interleaved boost converter with voltage doubler and tripler circuit is proposed here which gives improved results in terms of gain and voltage stress across the switching devices on small duty cycle. The circuit diagram of the mentioned topology is presented in Figure 2.

The mentioned topology is a three-phase interleaved circuit which consists of three inductors, voltage doubler and tripler circuits and a basic boost converter circuit. Switching devices M_1, M_2, M_3, M_4, and M_5 are turned on and off by a PWM source with a 120-degree phase shift for switch M_1, M_2, and M_3, while the switch M_4 will be on when the switch M_1 is off and vice versa. The same is the case for switches M_5 and M_2, such as both the switches will not be on or off at the same time. The inductors will charge in the on time of the switch M_1, M_2, and M_3 and will discharge to the capacitors when the switch M_1, M_2, and M_3 are in off state. With the proposed topology, the voltage gain will increase, and voltage stress across the switches, such as voltage drop, will reduce; hence, the losses will decrease.

2. Operating Principle of Proposed Converter

A three-phase interleaved boost converter with voltage doubler and tripler circuit is proposed in this paper. The below-mentioned assumptions were made for the operation of the mentioned converter.

(1) Capacitor C_1, C_2, C_3, and Co are of enough size that the voltage ripple is minor through them compared to their DC values

(2) Each component is considered to be ideal

(3) The operating mode is continuous conduction mode; thus, the current I_1 through inductor L_1, I_2 through inductor L_2, and I_3 through inductor L_3 flow continuously

(4) Inductors L_1, L_2, and L_3 have the same inductance L

All switches are operated by PWM signals. Signals for switchs M_1, M_2, and M_3 are having a phase shift of 120 degrees. The PWM signal for switch M_4 is the inverse of switch M_3, and the signal to switch M_5 is the inverse signal of the switch. V_S is the input voltage, and V_O is the output voltage. The proposed is converter operating with constant switching constant frequency F_S, where $T_S = 1/F_S$. For the proposed converter, there are six switching states such as modes in one complete switching period as shown in Figure 3 and a few major waveforms defining the operating behavior of the mentioned converter. The six switching states are $t_o = 0$ sec, $t_1 = (\mathrm{DTs} - 2\mathrm{Ts}/3)$ sec, $t_2 = (\mathrm{Ts}/3)$ sec, $t_3 = (\mathrm{DTs} - \mathrm{Ts}/3)$ sec,$t_4 = (2\mathrm{Ts}/3)$ sec, $t_5 = \mathrm{DTs}$ sec, and $t_6 = (Ts)$ sec

All the six switching states are described as follows:

(i) State: I, III, V:$(T_0 \le T \le T_1), (T_2 \le T \le T_3, T_4 \le T \le T_5)$

States I, III, and V are the same for the proposed converter. It begins when switches M_1, M_2, and M_3 are set high at starting of time with PWM signals to V_{GS1}, V_{GS2}, and V_{GS3}. Diodes D_1, D_2, D_3, and D_4 are off in these states. The circuit diagram for this state is shown in Figure 4. Inductors L_1, L_2, and L_3 are get charged by DC input voltage, and I_1, I_2, and I_3 through inductors L_1, L_2, and L_3 rise linearly with slopes $VS/L1$, $VS/L2$, and $VS/L3$, respectively. The capacitors C_1, C_2, and C_3 are neither charges nor discharges. In this state, the output capacitor C_O discharges to load, and

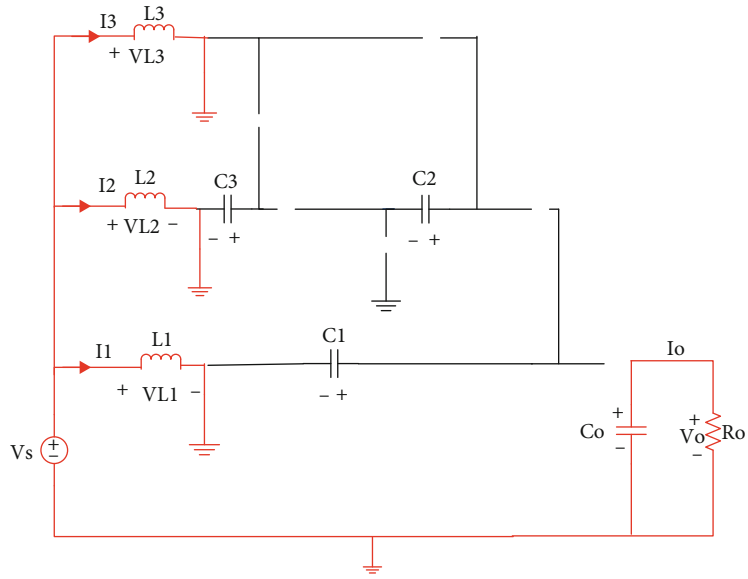

Figure 4: States I, III, and V.

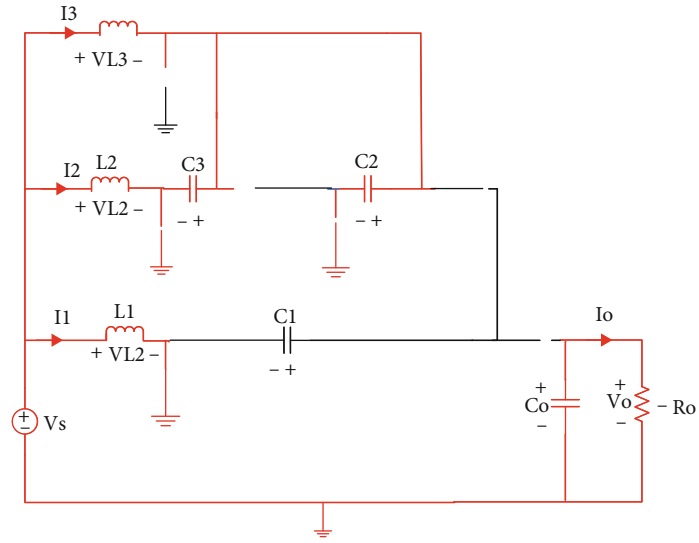

Figure 5: State II.

hence, output voltage Vo through Co decrease linearly with slope of $-VO/(RL * CO)$.

(ii) State: II $(T_1 \le T \le T_2)$

This circuit diagram for this state is shown in Figure 5. The inductor L_1 discharge in this state to capacitors C_2 and C_3, while L_2 and L_3 are still charging, and I_2 and I_3 through inductors L_2 and L_3 constantly rise with a slope of $VS/L2$ and $VS/L3$, respectively. So, in this state, the voltage across capacitors C_2 and C_3 increases because the capacitor is charging. Voltage across capacitor C_1 is still constant because current is not flowing through capacitor C_1. In this state, the output capacitors C_O discharge to load resistance, and hence, the voltage V_O at output across C_O falls linearly with a slope of $-VO/(RL * CO)$.

(iii) State: IV $(T_3 \le T \le T_4)$

The circuit diagram for this state is presented in Figure 6. Inductor L_1 is charging, and I_1 and I_3 through inductors L_1 and L_3 increase linearly with a slope of $VS/L1$ and $VS/L3$, correspondingly, inductor L_2 and capacitors C_2 and C_3 are discharging to capacitor C_1.So, in this state, the voltage across capacitors C_2 and C_3 decreases, and voltage across capacitor C_1 increases. In this state, the output capacitor C_O discharges to load; hence, the voltage at the output V_O through C_O decreases linearly with a slope of $-VO/(RL * Co)$.

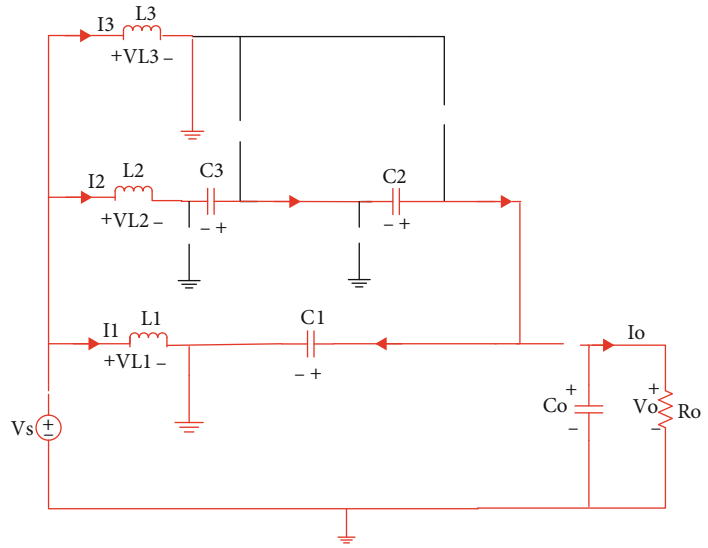

Figure 6: State IV.

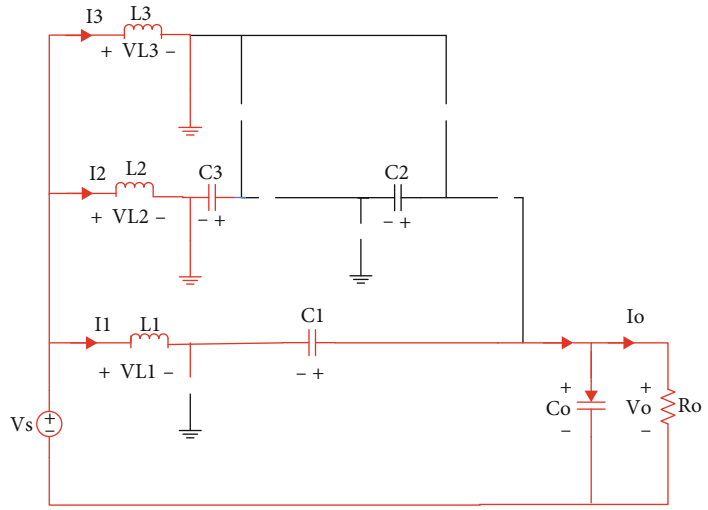

Figure 7: State VI.

Table 1: Converter parameters for simulation.

Name of parameter	Symbol	Value
Voltage at input	V_S	15 [V]
Voltage at output	V_O	200 [V]
Frequency	F_S	10 [kHz]
Load resistance	R_L	1537 [Ω]
Filter inductor in phase #1, 2, and 3	L_1, L_2, L_3	1 [mH]
Intermediate capacitor	C_1	1.75 [uF]
Intermediate capacitor	C_2	5.2 [uF]
Intermediate capacitor	C_3	5.2 [uF]
Output smoothing capacitor	C_O	5 [uF]
Voltage stress across M_1, M_2, M_3	$V_{M1,M2,M3}$ (stress)	50 {V]
Ripple in capacitor voltage V_{CO}	ΔV_{CO}	10 [V]

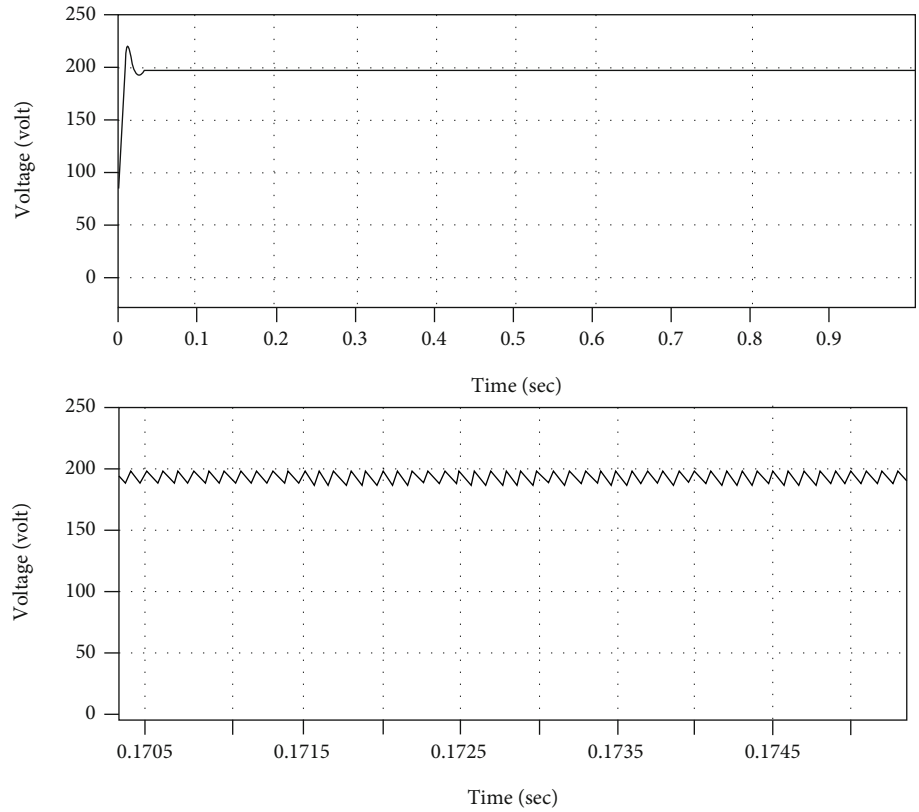

Figure 8: Output voltage waveform on 70% duty cycle.

(iv) State: VI $(T_5 \le T \le T_6)$

The circuit diagram for this interval is presented in Figure 7. Inductors L_2 and L_3 are charging while L_1 is discharging. I_2 and I_3 rise linearly with a slope of $VS/L2$ and $Vs/L3$ correspondingly, and inductor L_1 and capacitor C_1 are discharging to capacitor Co and load Ro. The voltage across capacitor C_1 is decreasing and the output capacitor Co gets charging, and hence, the voltage at output such as V_O across Co increases linearly.

3. Steady-State Analysis

To make an easy and simple assessment of the proposed circuit diagram, the time intervals for switching states put across in terms of switching period TS of duty cycle D as follows: $t_o = 0$ sec, $t_1 = (\mathrm{DTs} - 2\mathrm{Ts}/3)$ sec, $t_2 = (\mathrm{Ts}/3)$ sec, $t_3 = (\mathrm{DTs} - \mathrm{Ts}/3)$ sec, $t_4 = (2\mathrm{Ts}/3)$ sec, $t_5 = \mathrm{DTs}$ sec, and $t_6 = (\mathrm{Ts})$ sec.

3.1. DC Conversion Ratio. Voltage gain can be derived by using volt-second balance principles. Inductor L_3 is charging in states I, III, IV, V, and VI and discharging in state II.

The volt second balance of inductor L_2 gives:

$$\mathrm{VC2} = \frac{\mathrm{VS}}{1-D}, \qquad \mathrm{VC3} = \frac{\mathrm{VS}}{1-D}. \tag{1}$$

Similarly, inductor L_2 is charging during the interval I, II, III, V, and VI and discharging in IV.

The volt second balance of inductor L_2 gives:

$$\mathrm{VC1} = \frac{3\mathrm{VS}}{1-D}. \tag{2}$$

Inductor L_1 gets charged during states I, II, III, IV, and V and discharged during interval VI.

The volt second balance of inductor L_2 gives:

$$\frac{\mathrm{Vo}}{\mathrm{Vs}} = \frac{4}{1-D}. \tag{3}$$

The gain of the proposed converter is obtained as:

$$\mathrm{M} = \frac{4}{1-D}. \tag{4}$$

3.2. Voltage Stress across MOSFETS M_1, M_2, and M_3. When the switch is in an off state, the voltage stress or voltage drop is produced across it. The voltage stress across the MOSFET M_1 can be obtained as

$$\mathrm{VM1} = \mathrm{VCo} - \mathrm{VC1}. \tag{5}$$

The voltage stress through switch M_2 can be obtained as

$$\mathrm{VM2} = \mathrm{VC1} - \mathrm{VC3} - \mathrm{VC2}. \tag{6}$$

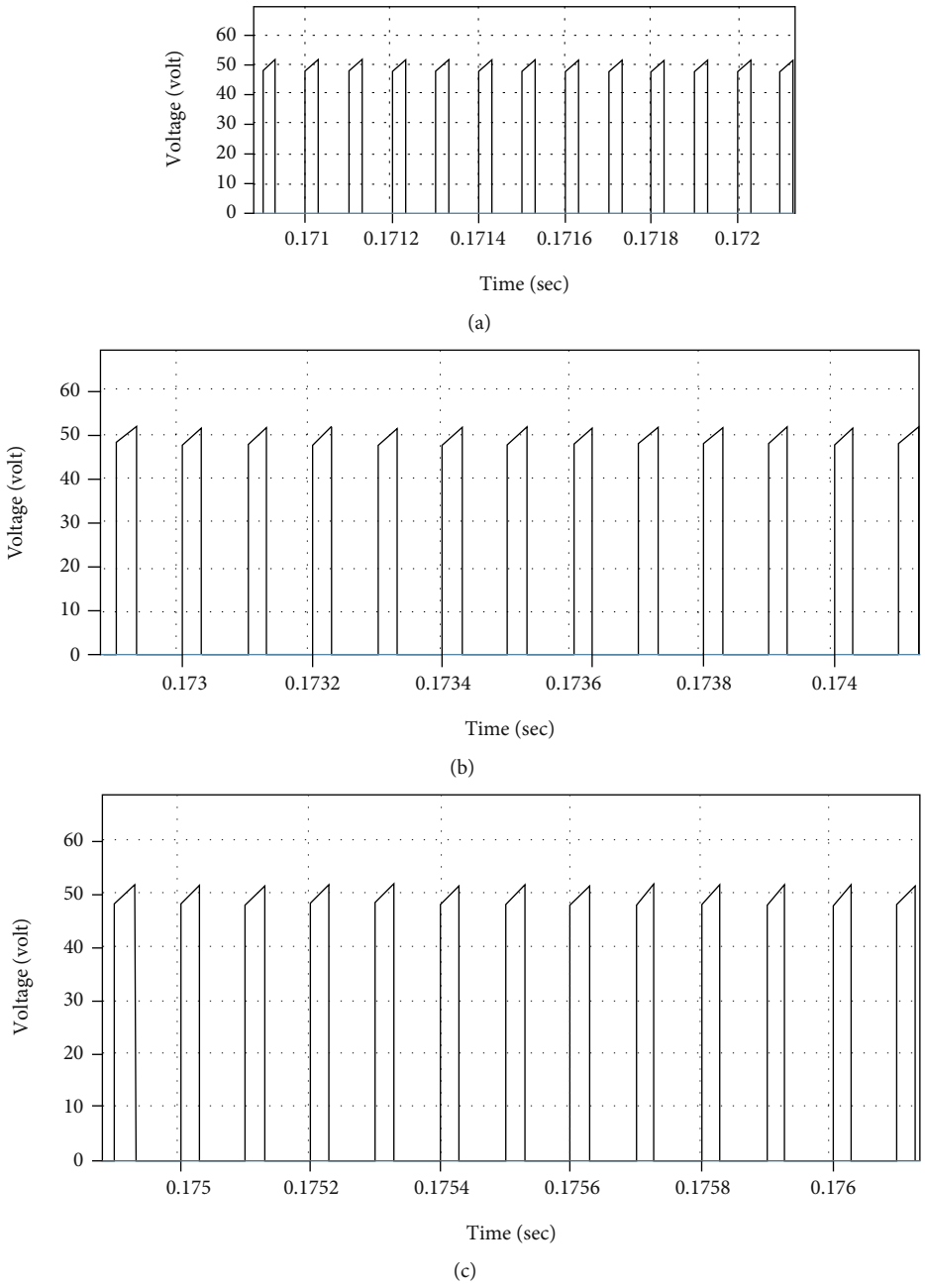

FIGURE 9: (a) Voltage stress across M_1. (b) Voltage stress across M_2. (c) Voltage stress across M_3.

The voltage stress across the switch M_3 can be obtained as

$$\mathrm{VM3} = \mathrm{VC2} = \mathrm{VC3}. \tag{7}$$

3.3. Ripple Current and Ripple Voltage. The $\Delta i1$ is the ripple current in current I_1, $\Delta i2$ in current I_2, and $\Delta i3$ in current I_3. The ripple current through inductors L_1, L_2, and L_3 can be expressed as follows:

$$\Delta I1, 2, 3 = \frac{\mathrm{VsDT}}{\mathrm{L}(1, 2, 3)}. \tag{8}$$

The ΔVco is the ripple voltage in V_{CO}, ΔVc1 in V_{C1}, ΔVc2 in V_{C2}, ΔVc3 in V_{C3}, and ΔVc4 in V_{C4}.

For finding ΔVco, the capacitor CO is discharging to the load. The ΔVco can be expressed as follows:

$$\Delta\mathrm{Vco} = \frac{\mathrm{Vo} * D}{\mathrm{Ro} * \mathrm{Co} * \mathrm{Fs}}. \tag{9}$$

For ΔVc1, capacitor C_1 is discharging to Co and load; ΔVc1 can be expressed as follows:

$$\Delta\mathrm{Vc1} = \frac{I1 * (1 - D)}{\mathrm{C3} * \mathrm{Fs}}. \tag{10}$$

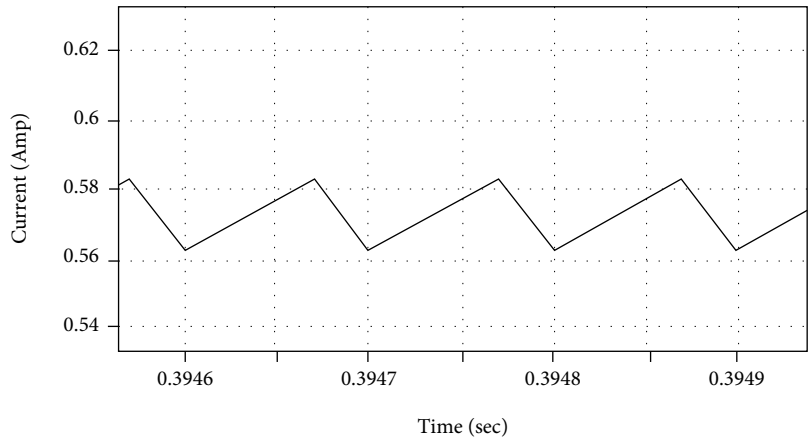

Figure 10: Phase current across L_1, L_2, and L_3.

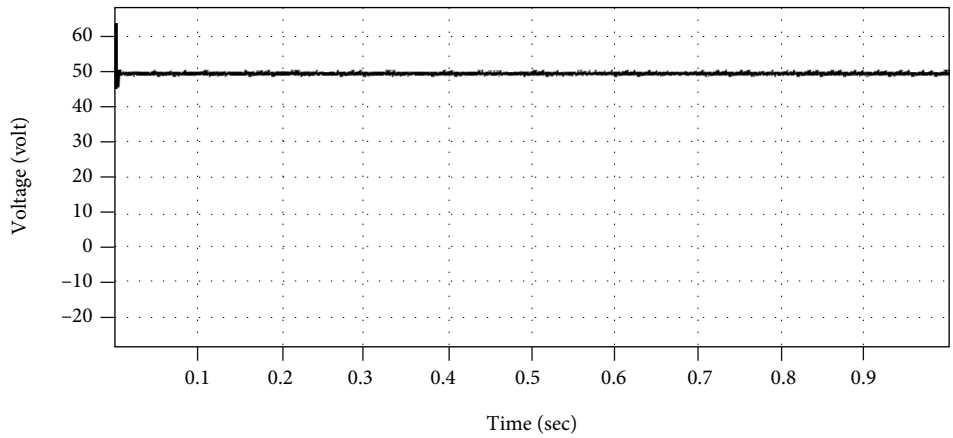

Figure 11: Output voltage waveform of conventional IBC on $D = 0.7$.

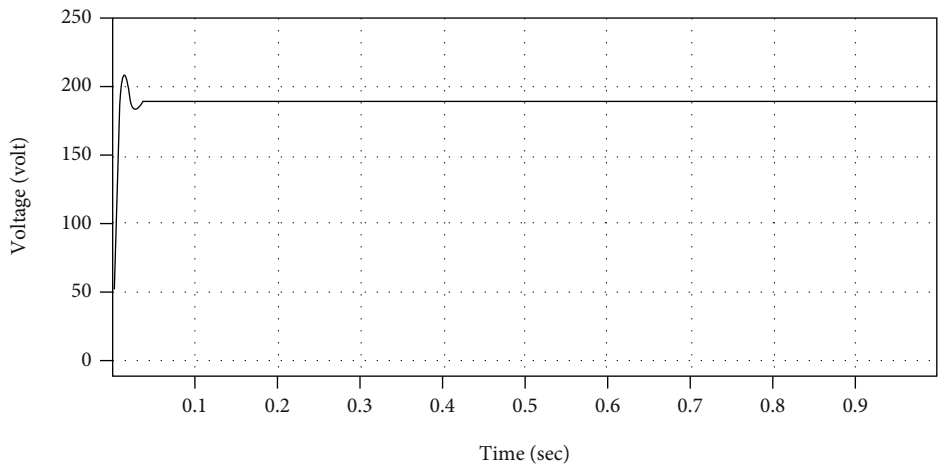

Figure 12: Output voltage waveform of conventional IBC on $D = 0.925$.

Here, $I1$ can be expressed as follows:

$$I1 = \frac{Io}{1 - D}. \tag{11}$$

For finding ΔVc2, capacitor C_2 is discharging to C_1; ΔVc2 can be expressed as follows:

$$\Delta Vc2 = \frac{I1 * 1 - D}{C2 * Fs}. \tag{12}$$

For finding ΔVc3, capacitor C_3 is discharging to C_1; Δ

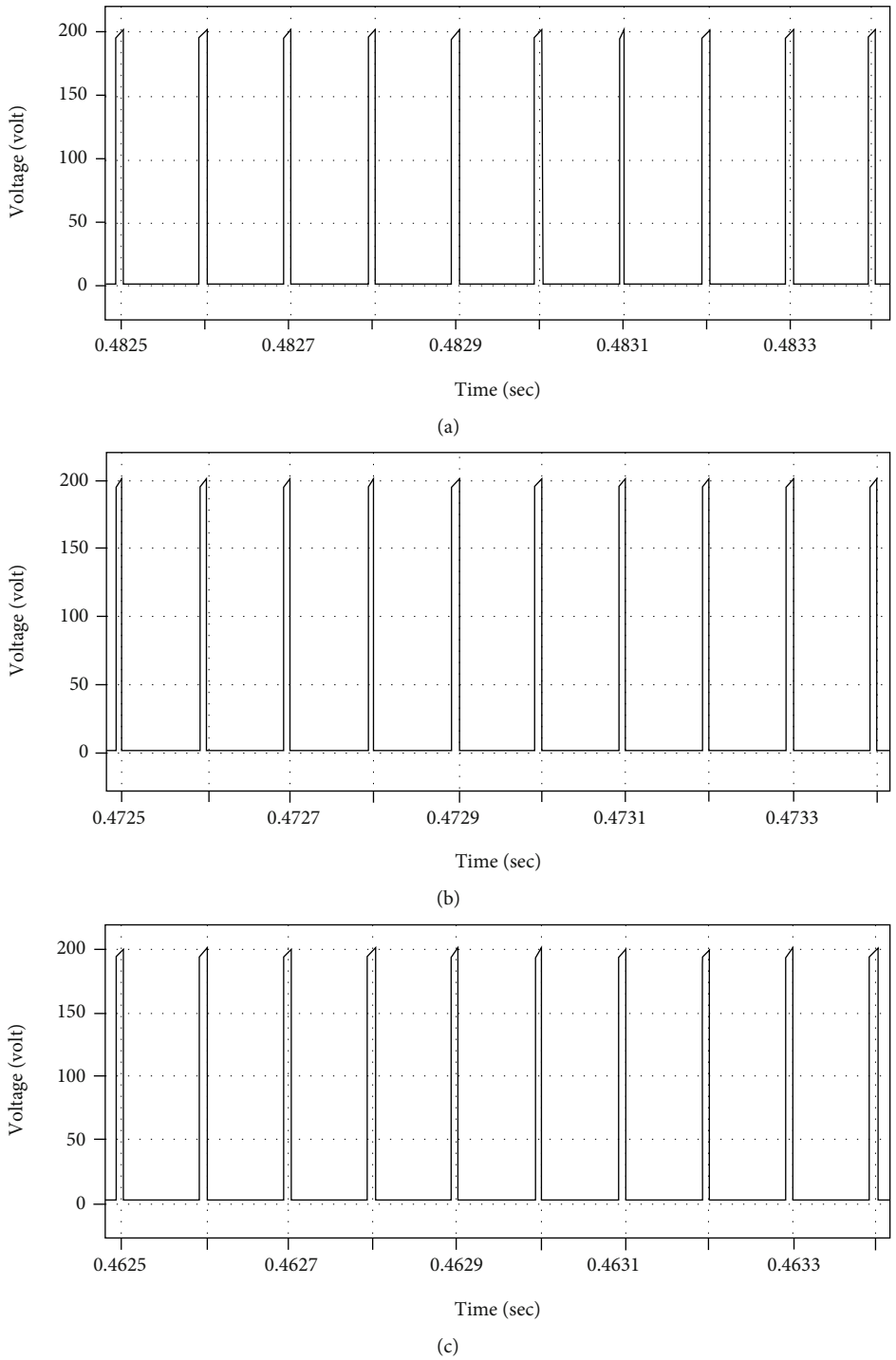

Figure 13: (a) Voltage stress across MOSFET M_1. (b) Voltage stress across MOSFET M_2. (c) Voltage stress across MOSFET M_3.

Vc2 can be expressed as follows:

$$\Delta \mathrm{Vc3} = \frac{I1 * 1 - D}{\mathrm{C3} * \mathrm{Fs}}. \tag{13}$$

3.4. Voltage Stress across the Switches. Voltage stress across the MOSFET M_1 can be expressed as follows:

$$\mathrm{VM1} = \mathrm{VCo} - \mathrm{VC1}. \tag{14}$$

Voltage stress across the MOSFET M_2 can be expressed as follows:

$$\mathrm{VM2} = \mathrm{VC1} - \mathrm{VC3} - \mathrm{VC2}. \tag{15}$$

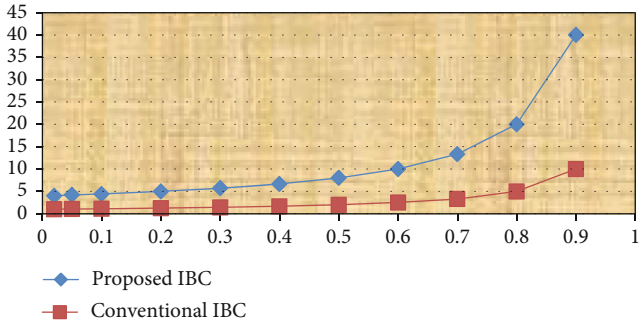

Figure 14: Voltage gain comparison between conventional IBC and proposed IBC.

Voltage stress across the MOSFET M_3 can be expressed as follows:

$$VM3 = VC2 = VC3. \quad (16)$$

4. Results

The simulation has been performed in Matlab Simulink to verify the performance of the proposed interleaved triphase boost converter and conventional DC-DC interleaved boost converter with parameters given in Table 1. The derived mathematical equations have been used up to obtain the theoretical results presented in Table 1.

4.1. Simulation Results. Output voltage waveforms of the proposed boost converter with a 70% duty cycle is 200 V shown in Figure 8

The voltages stress across the MOSFET M_1, M_2, and M_3 is 50 V as shown in Figures 9(a)–9(c); the phase current through inductors L_1, L_2, and L_3 is shown in Figure 10.

The simulation results clearly show that there is no difference between simulation results and theoretical results.

4.2. Comparison. Now, utilizing the parameters given in Table 1, the simulation results of the conventional DC-DC interleaved boost converter are also acquired. The output voltage waveform of the conventional boost converter is given in Figure 11, which is 50 volts with a 70% duty cycle. The conventional interleaved boost converter gives the output voltage 200 volts on a 92.5% duty cycle value such as $D = 0.925$ (as shown in Figure 12). Figures 13(a)–13(c) show that at $D = .925$; the voltage stress across MOSFETS for the usual interleaved DC-DC boost converter is 200 V.

It is clear from the simulation results that the presented converter topology has very good results as compared to the conventional interleaved DC-DC boost converter. As compared with a conventional converter, it is obvious that the proposed boost converter has a four times higher voltage conversion ratio, and the voltage stresses on main switches are approximately four times smaller than the conventional DC-DC interleaved boost converter. In the conventional IBC, the output voltage appears across the main switching devices, while the current is divided into all phases, due to which the inductor size is reduced in both conventional and proposed IBC.

Simulation results are provided for the conventional interleaved DC-DC boost converter and proposed interleaved DC-DC boost converter, which indicates that the proposed converter yields better results as compared with a conventional interleaved boost converter at the expense of only two additional switches (proposed converter uses 5 MOSFETs while conventional uses 3). The comparisons between the gain of the conventional IBC and proposed IBC are shown in Figure 14.

5. Conclusion

Compared with the conventional IBC, the proposed IBC has several good extra characteristics, which comprise a high gain/conversion ratio, and across the main MOSFETs, the low-voltage stress. Voltage doubler plus voltage tripler circuits are used to gain these benefits. The steady-state analysis and working principle of the offered converter of each state are examined clearly with the proposed circuit diagram and mathematical equations. Simulation results in Matlab Simulink show that normal interleaved DC-DC boost converter is affected by operating on extreme value of D (duty cycle) and will be having reverse recovery problem for switching devices for boosting 15-volt input voltage to 200 volts, while it is clear from both the simulation and theoretical outcomes that the presented converter can simply achieve 200 V with the appropriate value of D, and the voltage stress across the switches will also reduce to one-fourth of output voltage. The above-mentioned qualities of high DC-DC conversion ratio and reduced voltage stress across switching devices make the mentioned boost converter an appropriate candidate in case of low voltage renewable sources with low DC output voltages and more other functions where a high step-up conversion ratio is wanted.

Data Availability

Data will be provided on request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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Review Article

Thinking and Prospect of Power Chip Specificity

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The contradiction between the demand of massive intelligent scene caused by the interconnection of things in power system and the bottleneck of the chip itself is becoming more and more serious. How to realize the self-controllable and domestic substitution of power chips has been widely concerned in the power field. Therefore, this paper analyzes the demand for power chips in power system and discusses the scene specificity of power chips. Then, it combs the design architecture of power chips and discusses the application scenarios and research focuses of power chips. Finally, the key scientific problems and major technical bottlenecks of power chips are prospected.

1. Introduction

Chip is the leading foundation of national economic and social development. The development of chip industry is not only an inevitable development trend facing external competitive pressure but also meets the urgent "neck" demand of various industries in China [1]. Now, it has risen to the level of national strategy [2]. Since 2014, the state has successively promulgated such strategic plans and policies, such as the outline for promoting the development of the national integrated circuit industry, the 13th five-year development plan for the national high tech industrial development zone, and several policies for promoting the high-quality development of the integrated circuit industry and software industry [3]. It is aimed at promoting the innovation and breakthrough of integrated circuit and improving the technology level of Chinese chip industry [4]. It can be seen that independent research and development of chips and accelerating the industrialization of chips are the urgent needs and major strategic planning of the country [5].

As the basic energy industry of industrial development, the power industry is closely related to the use of chips in all aspects of power production [6]. In 2010, the State Grid comprehensively promoted the construction of smart grid. At that time, the demand for chips was expected to reach 20 billion pieces. In 2019, State Grid and China Southern Power Grid have put forward strategic measures to build the power Internet of Things (IoT) and digital grid, aiming to realize the coordinated interconnection of all production links of power system [7]. Comprehensive perception of system operation status and efficient processing of massive power information by using new modern information technologies such as advanced sensors, intelligent equipment, artificial intelligence and edge computing [8–10]. In this context, all intelligent scenarios need to use power chips for efficient data analysis and intelligent processing, and the demand for power chips in the power system is growing exponentially.

Under the important national strategic planning and the urgent demand of power system, the research and

development of domestic power chip with self-control have been widely concerned in related fields. Many power chip enterprises, such as Beijing Smart Chip, Fudan Microelectronics, and Datang Microelectronics, have emerged in China, which can realize the localization substitution of some security chips, master chips, and RF chips. However, at present, the high-end chips in the electric power field are still mainly imported chips. Due to the technical bottlenecks in technology, materials, and performance testing system, there is still a big gap between domestic power chip enterprises and foreign enterprises [11]. Relevant scholars have also studied the key technologies involved in power chips, including energy consumption optimization technology based on multicore chips [12], modeling customization for power chips [13], and device development and system integration based on power chips [14]. It is thus clear that the current theoretical research on the chip is mainly based on the general chip architecture and the demand integration and performance optimization of power application scenarios are carried out [15].

However, with the intellectualization and ubiquity of power grid application scenarios under the power IoT, the power system presents an urgent demand trend for diversified power chips [16]. The contradiction between the increasing demand for intelligent scenarios in power system and the technology bottleneck of power chips and the power chip integration mode based on the general chip architecture is intensified. Power core is urgently needed in power application scenarios. The bottleneck technology breakthrough can realize the customization of various application scenarios. For these purposes, this paper analyzes the power chip architecture and the application of power chip and discusses the key problems of power system chip from the perspective of power chip classification and application. The main contributions in this paper can be summarized as follows:

(i) Analyzing the demand for power chips in the power system and discuss the specifics of their scene

(ii) Combining the architecture design of power chips and discussing their application scenarios and research focus

(iii) Exploration of major scientific problems and major technical bottlenecks for power chips

2. Preliminary

2.1. The Particularity of Power Scene. With the development of power system in the direction of digitalization, automation, and interaction, a series of intelligent power equipment, such as intelligent meter and intelligent distribution terminal, are widely used in the power system [17]. These intelligent power devices need to use a large number of power chips. These chips are not only directly related to the demand of intelligent analysis scenarios but also an important link between the user side and the smart grid information exchange. Power chip has become the core force of smart grid development, which is of great significance to the construction of power IoT and the realization of digital transformation of power grid.

At present, power chips have penetrated into all aspects of intelligent power system, such as power generation, transmission, transformation, distribution, power consumption, and dispatching, providing the underlying material support for the development of the power industry [18–20]. There are many intelligent scenarios in the power system inseparable from the use of power chips, but each scenario needs different types of power chips. Power grid data analysis, processing, and control need the master chip to complete; field data acquisition needs sensor chip support; key data protection needs specific security chip; information transmission and interaction rely on communication chip. Identification and storage management of power equipment need radio frequency identification chip; massive intelligent inspection and monitoring terminal need artificial intelligence chip. A large number of intelligent acquisition devices and small and micro sensors are needed for the collection of user electricity information and environmental state perception, as well as corresponding intelligent processing chips [21]. Therefore, diversified scenes, huge volume, and fragmented application are the characteristics of the demand for chips in power system.

In addition, the power chip used in the current power system is highly dependent on foreign imports and the safe and stable operation of the power system is faced with potential risks such as information security and algorithm constraints. Therefore, speeding up the research and replacement of chips needed for power system intellectualization and realizing the security of power grid chips independently and controllable are the fundamental requirements to ensure the security of power grid. At the same time, the power grid integrated with blockchain and other technologies will become an important security technology [22–24].

2.2. Definition and Classification of Power Chips. Chip is the general designation of semiconductor component products, also known as integrated circuit, microcircuit, etc., which is a kind of micro electronic device or component [25]. There are many classification methods for general chips. According to application scenarios, chips can be divided into four categories: civil, industrial, automotive, and military. According to the use or function, chips can be divided into GPU, CPU, FPGA, DSP, ASIC, and SOC. According to the manufacturing process, chips can be divided into 7 nm and 14 nm ac [26].

At present, power chip mainly refers to the chip used in power system. The power chip is classified according to its application function. The commonly used chip mainly includes main control chip, communication chip, security chip, radio frequency identification chip, and sensor chip. However, with the development of the power IoT and the digital transformation of power grid, the new power system not only needs the basic functions of traditional chip such as sensing, measurement, control, and communication but also needs the intelligent chip to realize intelligent perception, analysis, and identification at the terminal and equipment side. Therefore, the meaning and classification of

traditional power chip cannot meet the special needs of power system development and power scene. Therefore, this paper puts forward the concept of power dedicated chip, which is defined as a customized industrial chip that meets the requirements of power system measurement, control, protection, intelligent perception, analysis, and identification. It is the basic device for new energy access and smart grid upgrade and development. In addition to the traditional master control and communication chips, the power dedicated chips should also include power distribution terminal intelligent chips, visual edge intelligent chips, sensor and edge computing fusion chips, and blockchain chips for IoT applications. Figure 1 shows the classification of power dedicated chips.

The intelligent chip of power distribution terminal is mainly used for terminal equipment of power distribution and power consumption. Intelligent integrated distribution terminal (TTU), feeder terminal device (FTU), and station control terminal (DTU) equipped with smart chip of distribution terminal not only can collect and monitor distribution data but also can analyze and identify fault and power types on line, so as to achieve timely fault isolation recovery, voltage, and reactive power adjustment on the distribution terminal side. The intelligent meter and intelligent charging pile equipped with intelligent chip of power distribution terminal can not only complete the measurement, collection, communication, and accounting of power consumption data but also realize the analysis and identification, prediction, and identification of power consumption load.

The vision edge intelligent chip is mainly used in power transmission and transformation link inspection equipment and power operation monitoring system. The inspection unmanned aerial vehicles (UAV) and transmission line online monitoring equipment equipped with video monitoring edge intelligent chip can not only monitor the changes of temperature, inclination, phase, vibration, and wind deflection of transmission lines but also analyze and identify the transmission line fault and transmission channel environment in real time [27]. The electric power operation monitoring equipment equipped with video monitoring edge intelligent chip can identify the behavior and posture of operators on line and timely warn the poor operation, missing operation, and nonoperation according to the specified sequence, so as to realize the safe production of electric power.

The fusion chip of sensor and edge computing is used in sensor terminals of power system. The temperature sensor, photoelectric sensor, vibration sensor, displacement sensor, and other sensor terminals equipped with sensor and edge computing fusion chip can not only realize online monitoring of the operation status of power equipment but also analyze the fault type of equipment according to the data collected by the sensor and assist the operation and maintenance personnel.

The blockchain chip for the application of the IoT is used for all kinds of terminal devices of the power IoT, providing a basic environment for data exchange for the unified management, security identification, and interconnection of all things of the power equipment, realizing the full traceability of the power grid data, and ensuring the safe and stable operation of the smart grid. The combination of blockchain technology and power IoT is conducive to the formation of a new form of decentralized power IoT security protection based on blockchain, which plays an important role in power system security detection, distributed trust mechanism, and power grid data privacy protection.

3. Architecture Systematization of Power Chip

3.1. Power Chip Architecture. There are numerous chip products used in the power industry, but there is no systematic technical standard and architecture for chips in the power industry. The national standards issued by the national integrated circuit standardization subcommittee mainly focus on the basic general requirements of chips, international standard conversion, and other directions, and there are no specific requirements for power specific chips [11]. Traditional power chips are mainly used in power grid sensing, measurement, control, and communication. According to different application scenarios, they can be divided into main control chip, sensor chip, security chip, communication chip, and RFID chip. The typical architecture modules of these chips are shown in Table 1.

The processor module in Table 1 includes the main processor and the coprocessor. The function module refers to the circuits required for the chip to complete specific functions, such as memory and flash memory control circuit of the main control chip, A/D conversion circuit of the sensor chip, safety logic circuit of the security chip, radio frequency circuit, and the radio frequency identification chip. It can be found from Table 1 that these traditional chips have communication module, power management module, function module, and external interface.

In order to make the chip industry be able to serve the power grid construction safely and reliably, it is necessary to clarify the requirements of the power industry on the chip function, performance, reliability, security, and real-time performance and design the power dedicated chip functional architecture of the largest convention under a variety of power intelligent application scenarios, combined with the architecture module of traditional chip, considering that the power special chip also has the ability of intelligent calculation and analysis and needs high-performance processor and high-speed and large-capacity memory. This paper summarizes the general architecture module of power dedicated chip into specific scene processor module, memory module, communication module, power management module, function module, and external interface [28].

3.2. Design Principles and Technical Requirements of Power Chip. When designing the power chip, we should analyze the requirements of different application scenarios of the power system and choose the general architecture module of the chip. At the same time, we should study the intelligent processing and identification algorithm suitable for the power chip with limited resources, build the algorithm library of power dedicated chip, and deploy it in the specific

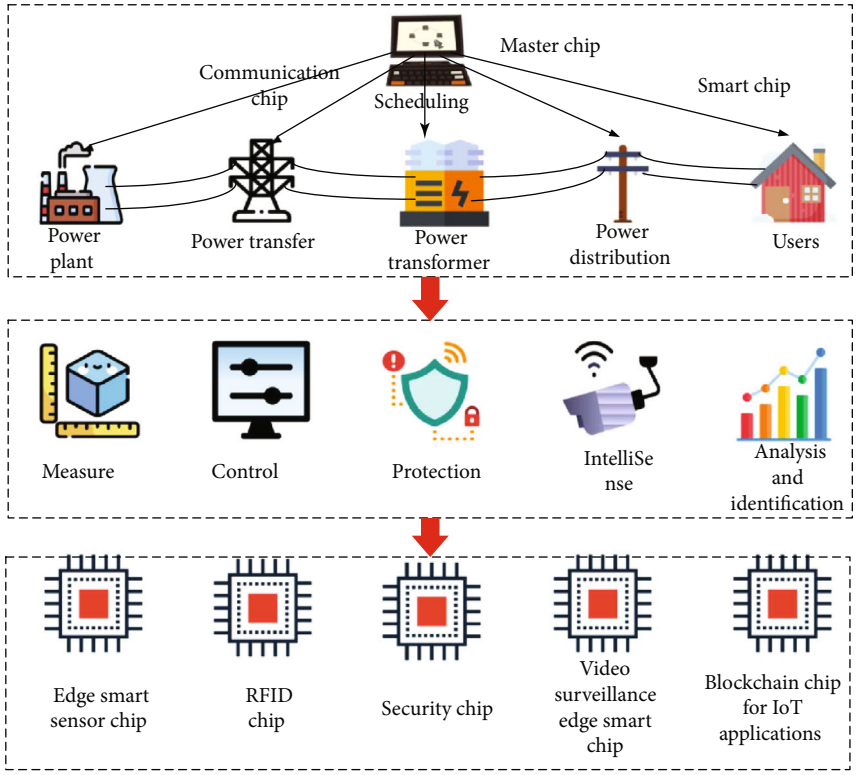

Figure 1: Application and classification of power chips.

Table 1: Traditional power chip architecture modules.

Chip type	Master chip	Sensor chip	Security chip	Communication chip	RFID chip
Processor module	√		√	√	
Memory module	√		√		√
Communication module	√	√	√	√	√
Power management module	√	√	√	√	√
Functional module	√	√	√	√	√
External interface	√	√	√	√	√

scene processor module. The common intelligent algorithms of power chip are shown in Table 2.

The design of power dedicated chip not only needs to meet the scene requirements but also designs the structure and details of the power chip in combination with the technical requirements of power equipment environment, information security, and business real time. At the same time, select a specific scenario processor with appropriate performance and power consumption. The technical principles that should be followed in the power special chip mainly include the following aspects:

(1) Reliability. Most of the power equipment in smart grid is arranged outdoors, facing various severe weather conditions, geomagnetism, radiation, electric field, and other interference, so the power chip must be stable and charged in the environment of wide temperature, high humidity, salt fog, ice and snow, electromagnetic radiation, and so on. In particular, in the EMC (electromagnetic compatibility) design of power special chip, functional test should be done first to check whether the EMC index of the chip can meet the requirements, and then, protective design is needed, which involves filtering and shielding circuit and adjusting the wire layout in the chip [29, 30].

(2) Security. The data carried in the power dedicated chip is related to the national economy and people's living and privacy. In the past, major equipment failures at home and abroad have problems such as data leakage and sending and receiving errors. Therefore, independent information encryption function module should be considered in the design of power dedicated chip, so as to realize encrypted and secure communication between power equipment and cloud [31, 32].

(3) Real Time. The data acquisition, accurate measurement, data transmission, real-time control, and business scheduling

Table 2: Electric power chip algorithm library.

Chip category	Algorithm
Network communication	Message encoding and decoding, repeated message filtering, broadcast storm suppression, information security encryption
Electrical parameter data processing and calculation	Message processing, digital filtering, phase sequence calculation, harmonic calculation
Intelligent perception and analysis recognition	Target detection, target tracking, semantic segmentation, behavior and gesture recognition

of smart grid require very high real-time performance, which not only refers to the real-time data acquisition but also includes the real-time data processing, analysis, and decision-making. If the real-time performance cannot be guaranteed, the state data of power grid may be delayed and the stability of power grid can be misjudged. It is of great significance to design excellent high-performance and low-power power dedicated chips for the construction of real-time power IoT.

4. Key Technology

With the chip and terminal of intelligent processing capacity, more and more power chips will undertake the task of intelligent processing. Moreover, the current intelligent processing algorithm is mainly carried out in the resource-rich cloud platform. How to deploy the existing intelligent processing methods to the power chip is facing a huge challenge. Therefore, this paper focuses on the key technologies involved in the development of power chip intelligence, including lightweight intelligent processing model, cloud-edge-terminal collaboration technology, and security protection technology.

4.1. Lightweight Intelligent Processing Model for Power Chip

4.1.1. Lightweight Model Design. The research on lightweight model design mainly focuses on the construction of lightweight deep learning framework and the design of lightweight intelligent analysis model. (1) The lightweight deep learning framework is designed to provide intelligent analysis environment on power chip. In 2017, Google first proposed a lightweight deep learning algorithm framework for mobile and embedded devices named TensorFlow Lite, which can run deep learning models on low-latency mobile devices, and it takes up less memory space [33]. Jia et al. proposed a lightweight Caffe framework. In April 2017, Facebook added the functions such as recursive neural networks on the basis of Caffe and proposed the Caffe2 framework to make the framework better on mobile terminals. In March 2018, the Caffe2 was incorporated into the PyTorch framework, and the mainstream PyTorch and MXNet frameworks also began to support edge-terminal deep learning models [34]. Each framework including TensorFlow Lite, Caffe2, MXNet, and PyTorch has its own advantages and disadvantages, none of which can perform well in terms of delay, memory occupied, and reasoning effect [35]. (2) Lightweight model design is to consider the limited computing resources of power chips and directly design an intelligent analysis algorithm suitable for resource limited chips, such as SqueezeNet, MobileNet, ShuffleNet, and XceptionNet with faster and smaller network architecture. In addition, some scholars build lightweight intelligent analysis model through neural architecture search (NAS), which commonly uses the neural architecture search (NAS) method to search for lightweight deep learning models suitable for artificial intelligence (AI) chip. In 2016, Google [36] first proposed an architecture search method that uses the reinforcement learning to produce convolutional neural network architectures. Its basic idea is to automatically search out an optimal network architecture for different tasks by defining search space, search strategy, and evaluation prediction. In recent years, the researches on network architecture search (NAS) have mainly focused on the definition of NAS search space, NAS search algorithms, and evaluation of model performance [37]. The definition of search space is to determine the candidate network structures to be searched. At present, there are mainly two types of search space: global search space and local search space [38]. There are three main types of NAS search algorithms including search algorithms based on reinforcement learning, search method based on evolutionary algorithms, and search method based on gradients. The evaluation of model performance is to evaluate the network architecture performance obtained in the process of neural network architecture search. The most direct method is to train the obtained network architecture on the target dataset, get weights to the model, and then the inference effect of the model determined by using the test samples. However, the main problem of this method is that the search efficiency is low, which requires huge computing resources, the selection of network super parameters is difficult, and the network search is easy to fall into local optimum. So this method needs further research and optimization [39].

4.1.2. Compression and Acceleration of Model. The main methods of model compression include model pruning, parameter sharing, and simplified convolution kernel, currently [40]. Parameter pruning is to evaluate importance of structure and parameters of a deep learning model. Under the premise of ensuring accuracy of the models, redundant or less important network structures and parameters are to be cut to achieve the purpose of lightweight the deep network. Wang et al. [41] proposed a channel pruning model compression method based on discriminant force and applied it to the ice thickness monitoring of transmission lines. The ice thickness model after channel pruning was

deployed in the front-end ice monitoring device, so as to realize the front-end identification of ice thickness. Parameter sharing is to share a same quantized value among similar model parameters of the deep learning models to achieve deep learning model compression. Wu et al. [42] studied the influence of two parameter quantization methods of 8-bit computing and floating-point computing on the performance of deep learning models, and the research results show that the two quantization methods perform well for deep learning models. The method of simplifying the convolution kernel is to simplify the convolution kernel of the convolutional neural network, reducing or simplifying the high-dimensional convolution kernel to achieve model compression. MobileNet proposed by Howard et al. [43] is a typical model compression method that simplifies the convolution kernel. MobileNet uses depth wise separable convolution (DSC) to replace the classic 3D convolution in convolution neural network for feature extraction. This model can reduce the redundant information of convolution kernel, greatly reduces the calculation of deep learning network, and is adapted to the terminal with limited resources [44]. But in general, the research of lightweight model is not mature enough, and whether it is successfully applied in power chip for intelligent analysis and processing needs further verification.

4.2. Cloud-Edge-Terminal Collaboration Technology. With the development of edge computing and chip technology, more and more data processing tasks will be completed in terminals with AI chips, but it does not mean that cloud computing will be replaced. Because the memory and computing power of the edge computing devices and chips are relatively small and the computing resources are limited, only some lightweight deep learning networks can be deployed, so the tasks and data that can be processed are limited. Generally, the trained lightweight deep learning model is embedded in the edge computing device or power AI chip. Cloud computing is far away from the data source, there will be a certain delay in obtaining data, so it cannot achieve real-time data analysis and processing. But the cloud computing center is rich in computing resources, which can deploy complex deep learning models with higher accuracy and complete the training work of the model. Therefore, it is the key to promote and apply the power chip and edge intelligent technology to study the cloud-edge-terminal collaboration technology [45].

Cloud-edge-terminal collaboration technology involves storage, communication, task allocation, and model training and so on. According to the different dominant players, there are three modes of cloud-edge-terminal collaboration technology [46]. (1) Cloud-oriented collaboration technology: that is, cloud is responsible for model training and task assignment, and only the specific tasks are distributed to the edge and terminal for execution. (2) Terminal-oriented collaboration technology: the terminal allocates the main tasks according to its own computing power and memory and interacts with the intelligent processing results with the cloud and edge devices. (3) Cloud-edge-terminal collaborative optimization technology: that is to say, the task computing power and communication at the cloud edge are optimized in advance, and then, each link is configured and set according to the optimization results.

In the research of cloud-edge-terminal collaboration technology, Niu et al. [47] constructed a service response framework of power system based on cloud edge collaboration and proposed a load allocation mechanism of power IoT oriented to edge computing to minimize service delay. To solve the problem of task unloading in edge computing, Yao et al. [48] mainly studied the cost optimization of task scheduling in smart grid environment and proposed a task optimization algorithm based on green greedy algorithm, which provides a solution for the real-time power data analysis collected by smart devices in smart grid environment. Edge computing is an important supplement of cloud computing. Huang et al. [49] proposed a cloud edge collaboration framework for smart grid real-time video monitoring and proposed an efficient heuristic algorithm based on simulated annealing strategy for collaborative optimization. Zahoor et al. [50] proposed a smart grid resource management model based on cloud-fog computing. The core idea of the model is to establish the hierarchical structure of cloud-fog computing and provide different types of computing services for smart grid resource management. Aiming at the resource allocation problem of fog computing in ubiquitous smart grid, a dynamic resource allocation framework is proposed by Li et al. [51]. A dynamic differential game model is established, which can help service providers to make the optimal dynamic strategy when users change the strategy, to meet the needs of power grid users while maximizing resource utilization and efficiency. But the current power chip-related collaborative technology is still in its infancy, and cloud-edge-terminal collaborative technology as an important topic in the application of edge computing needs more discussion and research.

4.3. Security Protection Technology of Power Chip. In recent years, there have been many cybersecurity incidents in the power system. As one of the key national facilities, the power system has always been one of the important targets subject to cyberattacks. Security protection of the power system is of great significance to ensure safe and stable operation of the power grid [52–55]. However, with the rise and development of edge intelligence and power chip technology, a large number of user data are processed in the edge intelligent terminal. Although the edge and distributed intelligent processing mode has higher processing efficiency, the security protection ability at the edge end is relatively poor, it is easier to be invaded by attackers, and there are higher potential security risks. Therefore, the research on the security technology of power chip is the key to the application and promotion of power chip.

At present, some scholars have explored the chip security technology. Songlin et al. [56] proposed an edge computing system for smart grid based on the IoT. The system can achieve the connection and management of entity terminals, providing real-time analysis and processing of massive data by edge computing under edge computing. With the help of edge computing paradigm, he realized and proposed a

privacy protection strategy based on edge computing to ensure the security of the smart grid system under edge computing. Aiming at the security requirements in data transmission of smart grid under edge computing, a secure data aggregation (SDA) scheme based on Domino Ferrer additive privacy is proposed by Okay and Ozdemir [57]. The protocol not only ensures low communication and storage overhead but also achieves end-to-end confidentiality. Gai et al. [58] combined the block chain and edge computing technology and proposed a model permissioned blockchain edge model for smart grid network (PBEM-SGN) aiming at two important issues of privacy protection and energy security in smart grid. This model uses group signature and secret channel authorization technology to ensure the legitimacy of users to improve the security of smart grid. Yuan and Li [59] proposed a trust mechanism for IoT edge devices based on multisource feedback information fusion. Since the proposed multisource feedback mechanism is used for global trust computing, it is highly reliable to malicious attacks caused by malicious feedback providers. However, currently, such technologies related to edge computing and power AI chip are not mature enough. The security protection for edge computing and AI chip is an emerging research field, and it still has a long way to go in the future.

4.4. Power Chip Performance Testing Technology. The power chip industry is divided into four parts: design, manufacturing, packaging, and testing. The testing technology of power chip is one of the important supporting technologies for the development of power chip industry and also the key link to ensure the performance and quality of power chip. However, the current research mainly focuses on the performance testing of general-purpose chips. It includes the architecture design of chip test platform, high-speed signal test, and chip test optimization [60, 61]. The current test research on power chip is relatively scarce, and the test technology of power chip is lagging behind; there is no authoritative test system of power chip, which is extremely unfavorable to the development of power chip technology. In particular, the power system is a strong electricity environment; electromagnetic interference has a great impact on the power chip, how to find the special problems of power chip under high voltage and strong electromagnetic environment and form the standard system of EMC research and performance function detection of power chip under strong electromagnetic environment. Therefore, it is urgent to study the performance test technology of power chip and form a comprehensive and complete chip test system.

5. Application Scenarios of Power Chip

5.1. Intelligent Terminal of Power Distribution and Utilization. The distribution and utilization information acquisition system is a system for collecting, monitoring, and processing power distribution and utilization information of power users. The system is logically divided into three levels: master station layer, communication channel layer, and acquisition equipment layer [62, 63]. The main station layer includes marketing acquisition business application, front-end acquisition platform, and database management system; the communication channel layer mainly adopts optical fiber private network, 230 MHz wireless private network, APN wireless private network, micro power wireless, and other networks; the acquisition equipment layer includes concentrator, collector, and watt hour meter. In the operation of the whole system, the acquisition layer equipment obtains the user's measurement information through the distribution network acquisition terminal and transmits the information to the master station through the communication channel layer. The master station records, counts, and analyzes all the data and realizes the automatic collection of power consumption information, abnormal measurement monitoring, power quality monitoring, power consumption analysis and management, relevant information release, distributed energy monitoring, and so on, information interaction and other functions of intelligent electrical equipment [64, 65].

The intelligent chip carried in the distribution and consumption collection terminal realizes the front-end intelligent analysis and processing of the collected data and then builds a cloud edge end collaborative intelligent processing framework for power distribution and utilization data, which avoids the data congestion and response delay caused by the massive distribution and consumption data uploaded to the monitoring center. The architecture of the distribution and utilization collection system based on the intelligent chip is shown in Figure 2. The existing distribution and utilization terminal chip is mainly used for information communication. In comparison, the intelligent chip integrates powerful data processing module, which can intelligently analyze and process the data collected by the power distribution terminal. Moreover, the data processing ability is stronger and the response time is faster. It can better meet the real-time requirements of data processing in distribution network and greatly meet the power distribution chip facing the bottleneck demand.

5.2. Intelligent Inspection of Substation. In recent years, with the rapid development of artificial intelligence technology, robots begin to simulate human thinking and complete complex tasks. The intelligent inspection robot is used in the substation for equipment inspection, taking photos and archiving for key parts and meters, detecting meter scale, and real-time infrared monitoring of equipment temperature. The collected pictures and data are transmitted to the background inspection system in real time through wireless communication (power 4G), so as to complete equipment inspection in high-risk environment instead of staff [66, 67].

Nowadays, most substations are equipped with rail or trackless inspection robots, but the intelligent identification method of inspection images cannot meet the practical requirements, so most of the inspection robots are idle, which means the equipment images collected by the inspection robots and the defect detection are carried out through manual inspection. The test results have a great relationship with the quality of personnel, and the efficiency is low [68, 69]. Substation intelligent inspection chip technology can effectively solve the current dilemma. The topology of substation

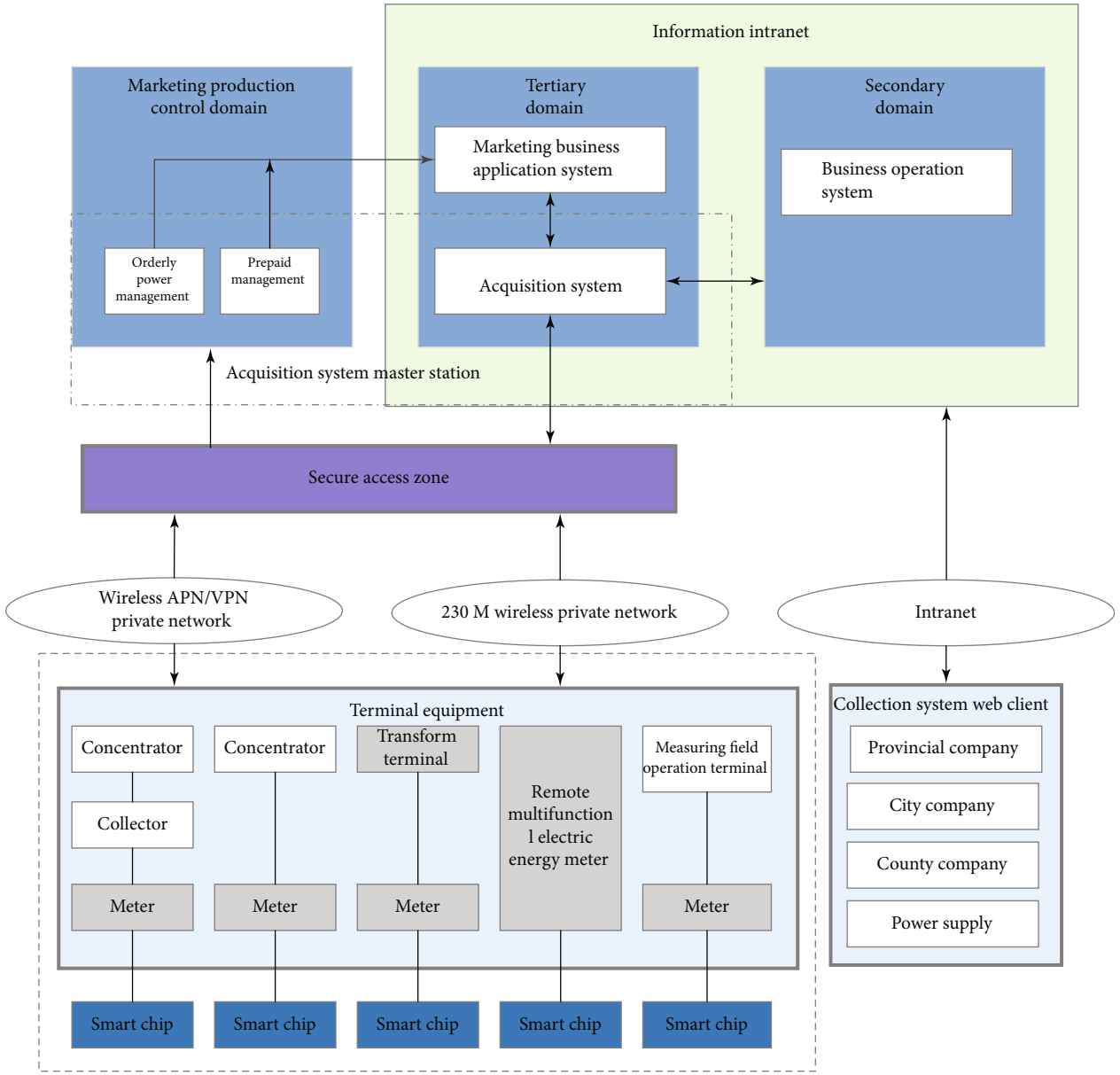

Figure 2: Network topology diagram of electricity collection system based on smart chip.

intelligent inspection system based on intelligent chip is shown in Figure 3.

As shown in Figure 4, through the intelligent chip on the inspection robot, real-time recognition and intelligent analysis of the collected equipment images are carried out, by using big data analysis and artificial intelligence technology, centralized management and control of terminals, automatic discrimination of push abnormal results, traceability of inspection process, acquisition of historical inspection situation, etc., thus forming an intelligent inspection framework of cloud end cooperation, providing technical support for the realization of unmanned inspection of substation.

5.3. Edge Intelligent Video Surveillance. With the continuous development of strong smart grid construction, higher requirements are put forward for video monitoring system, through the installation of network cameras in substations, transmission lines, business halls, and other places to collect onsite analog or digital video signals, access to the power grid through the video transmission network, and display the unified video monitoring platform to complete the daily inspection of substation and video monitoring of business hall. However, due to the large number of monitoring devices in the power grid, if all the video data of power grid security monitoring are uploaded to the cloud server, the amount of video monitoring data is relatively large. The computing capacity of cloud server is limited, and the delay is high, so the real-time performance of video monitoring cannot be guaranteed [70, 71]. The former power system also has power chips for video monitoring, but the image processing capacity of the existing chip technology is limited. So it cannot be applied to the processing requirements of massive video

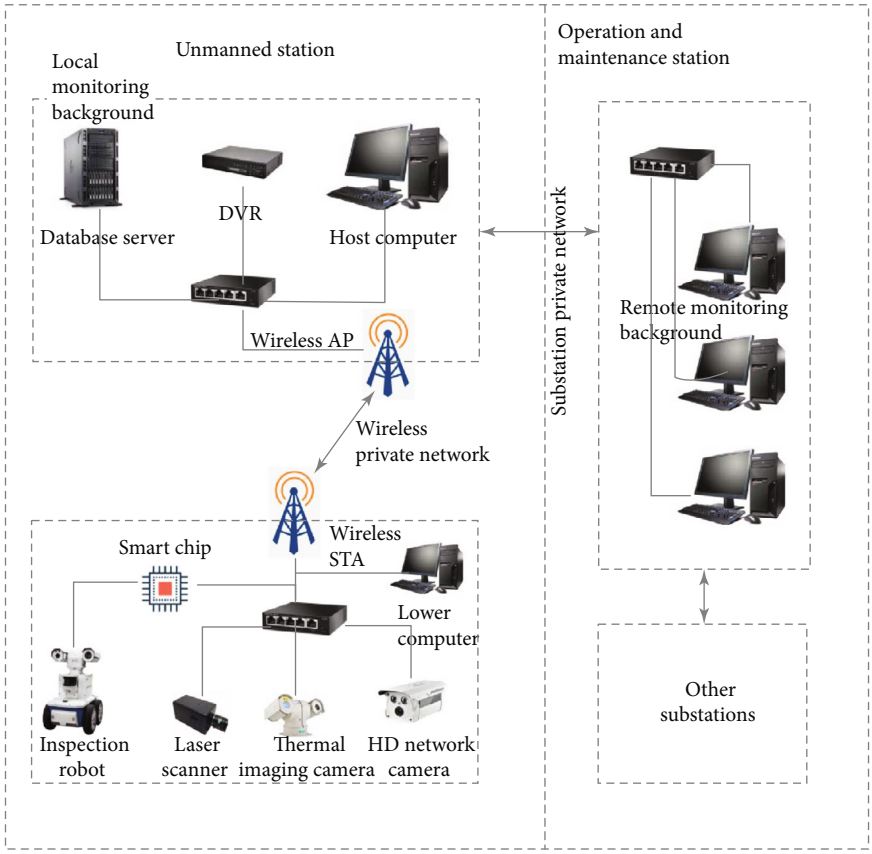

Figure 3: Topology diagram of intelligent inspection robot system for substation based on smart chip.

monitoring images generated under the background of power IoT and energy Internet. Vision intelligent processing chip and edge computing technology provide a solution for massive image visual processing. The topology of video monitoring system based on edge intelligent chip is shown in Figure 4.

As shown in Figure 4, the edge intelligent analysis and processing of power grid video monitoring can be realized by carrying the edge intelligent chip into the video monitoring terminal, which greatly improves the analysis and storage capacity of massive video and meets the demand of power system video monitoring massive power image intelligent analysis.

5.4. Edge Intelligent Sensor. With the continuous development and expansion of power grid scale, the state monitoring of electrical equipment has gradually become an important part of the company's operation and management. Power grid equipment has the characteristics of large number, wide variety, high value, long service cycle, wide distribution, and complex operation environment. The state evaluation and diagnosis ability of relevant equipment and channels is insufficient, which cannot support the rapid growth of the demand for operation and maintenance management of distribution equipment. Therefore, through the IoT technology, using the camera, position sensor, temperature sensor, humidity sensor, smoke sensor, pressure sensor, and other equipment installed on the column, box type and station transformer area, the operation status of the external environment, transformer, and low-voltage distribution box can be monitored. Through public network and private network, the data is transmitted to the back-end monitoring platform. The back-end monitoring platform analyzes the collected data, pushes the early-warning information synchronously, and monitors the onsite operating environment and status of power system equipment in real time [72–75].

However, with the proposal and promotion of the strategic planning of the power IoT, the demand of the power system for sensors with intelligent analysis ability is increasing rapidly. However, the data processing capacity of the existing sensor chips is limited, which cannot meet the processing requirements of the massive power data generated under the background of the power IoT. Therefore, it is urgent to develop "micro" intelligent sensors with strong data processing ability. By carrying the edge intelligent chip in the existing sensors, the intelligent upgrading of the existing commonly used sensors can be realized, so as to realize the edge terminal processing of the collected data, which greatly improves the power grid information collection ability and data analysis ability. The architecture of the environmental monitoring system for electrical equipment based on the edge intelligent sensor is shown in Figure 5.

6. Scientific Problems and Technical Bottlenecks

6.1. Scientific Problems. The research and development of power specific chip is still in its infancy, and the key scientific

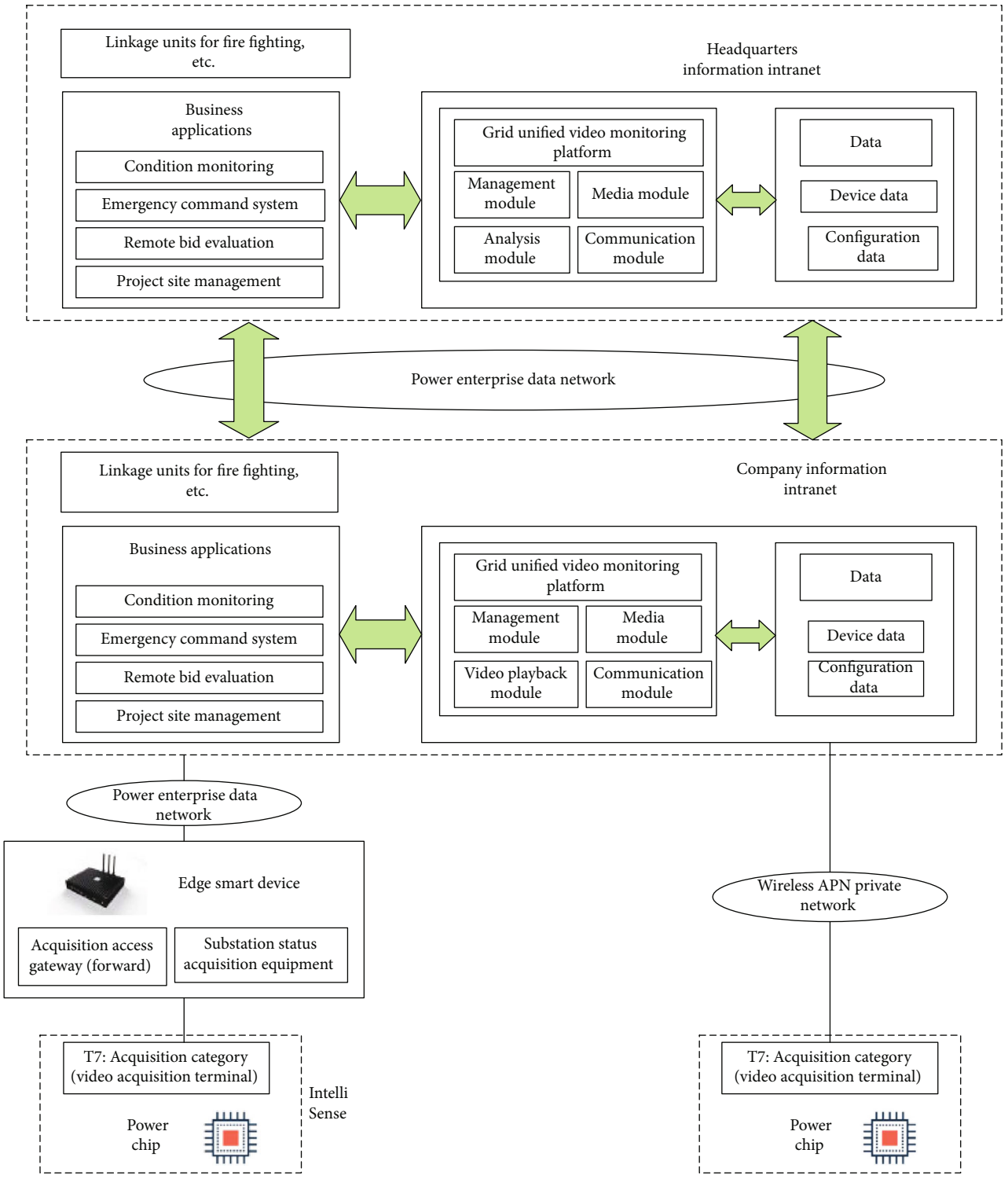

Figure 4: Topology diagram of unified video monitoring platform for power grid based on AI chip.

problem to be solved is how to realize the chip-based intelligent perception and analysis of the power IoT facing the fragmentation of scene and the complex data information. The IoT of power system has caused massive demand for intelligent scenarios and business data to be analyzed, and the computing resources of power chips are limited. Therefore, the research on the chip intelligent perception and efficient analysis architecture model of the power IoT is the focus of the power special chip research and also an important scientific problem to be solved.

In addition, in the practical application of the chip, it is usually faced with the influence of many factors, such as electricity, magnetism, and force, which lead to the degradation or failure of chip performance. Due to the complexity of

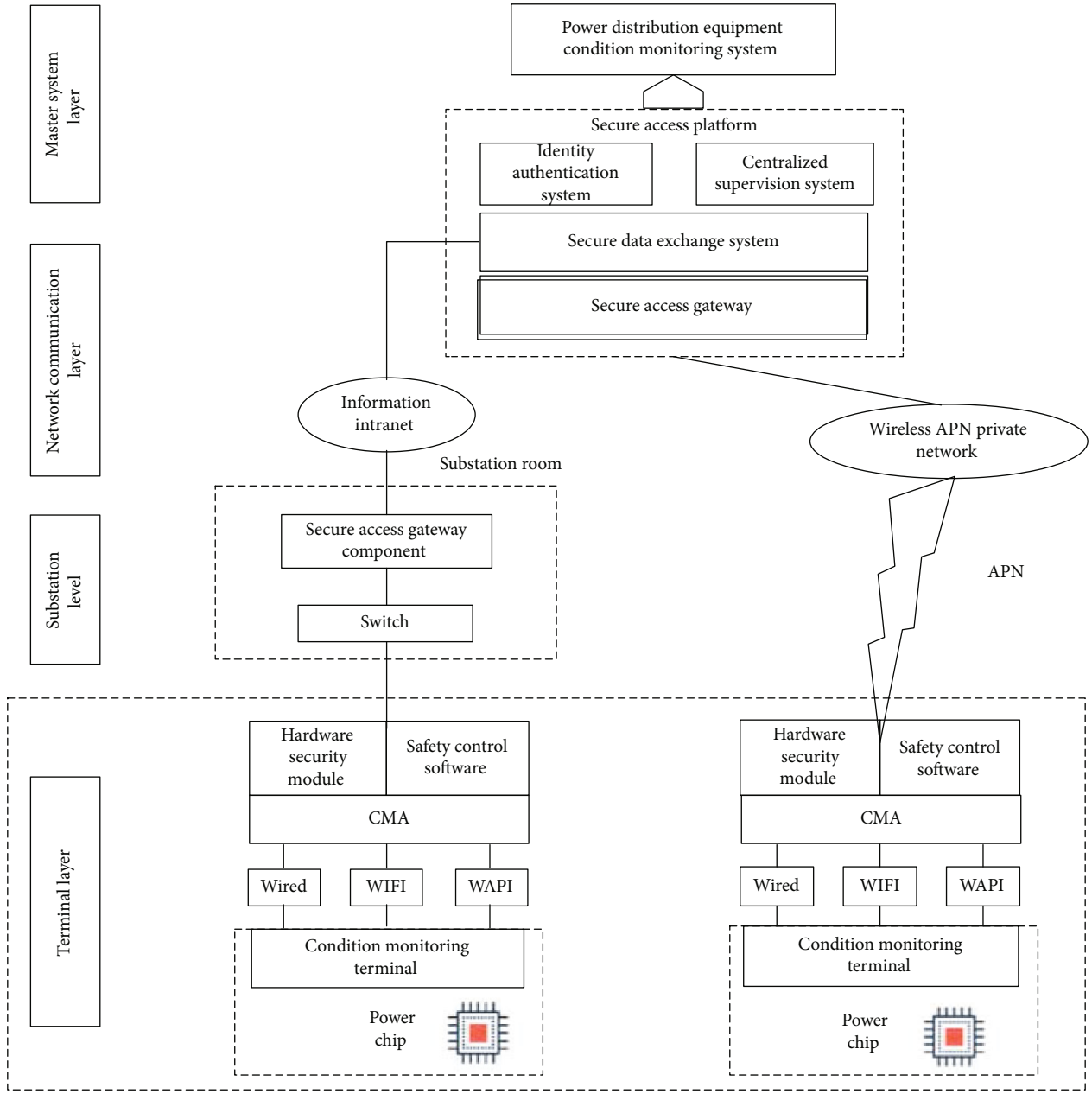

Figure 5: Architecture diagram of the environmental monitoring system for electrical equipment based on power chips.

electromagnetic environment, the diversity of equipment structure, and the small and micro nature of power chips, it is often difficult to find out the physical mechanism of power chip failure, and it is difficult to determine and reproduce the failure causes and processes of power chips. Therefore, it is another scientific problem to study the influence of complex electromagnetic environment on chip performance and qualitative analysis.

6.2. Key Technical Bottlenecks. The key technical bottlenecks in the field of power chips mainly include the following four aspects:

(1) To meet the needs of energy and power industry, the architecture design of power dedicated chip is discussed. Due to the specific industry requirements of the energy and power industry, it is necessary to design and optimize the chip architecture and configuration, rather than simply use the general chip architecture. How to optimize the architecture and redundancy according to the specific needs of the energy and power industry and how to research and optimize the configuration of customized architecture are the key bottlenecks to realize the independent control of power chips

(2) The problem of chip level power intelligent algorithm for protection, measurement, and control and intelligent sensor services is presented. Power protection, measurement and control, environmental monitoring, and other business need high precision, high reliability, small and micro, integration, so the corresponding edge intelligent analysis

algorithm of power chip also needs to be optimized. On how to consider the requirements of protection, measurement, control, and sensing in the field of energy and power, research and verifying various new applicability algorithms in the environment of miniaturization, distribution, and integration is the key to realize the intelligent upgrade of power chip

(3) Performance compatibility and detection of power chip in strong electromagnetic environment: power system is a strong power operation environment; electromagnetic interference has a great impact on power chips. How to find the special problems of power chips in high voltage and strong electromagnetic environment and to form the EMC research and performance function testing standard system of power chips under strong electromagnetic environment is of great significance to the application and promotion of power chips

(4) Intelligent customization of power chip under the demand of power fragmentation scenario: with the development of the power IoT, all scenarios of power system need chips with intelligent analysis function. It is of great significance to study the integrated application problems of power chips, such as easy-to-use requirements, edge intelligent algorithm requirements, large-scale tasks, and information flow collaboration, when applied to different engineering scenarios and specific systems

7. Conclusion

This paper discusses the specificity of power chip, puts forward the definition and research object of power chip, analyzes its typical application scenarios, and looks forward to the scientific problems and main technical bottlenecks of power chip. The main conclusions are as follows:

(1) Power chip is the inevitable product of the development of power IoT, artificial intelligence, and chip and measurement technology. And it is also the priority development field of the power industry in the future. The key to data perception and analysis in the construction of the power IoT is also the basis for the grid to realize full customer state perception and business full penetration

(2) At present, the focus of power chip research is on architecture design, chip level intelligent algorithm, performance test system and method, scene fragmentation application, autonomous chip algorithm and structure framework, etc.; breaking through the bottleneck of chip is the key to solve the problem of independent and controllable power chip

Data Availability

The data presented in this study are available on request from the corresponding author: dr.mohamed.abdelaziz@mu.edu.eg.

Conflicts of Interest

The authors declare no conflict of interest.

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