Journal of Sensors

Smart Sensors and Systems for Ubiquitous Power Internet of Things

Lead Guest Editor: Kai Huang
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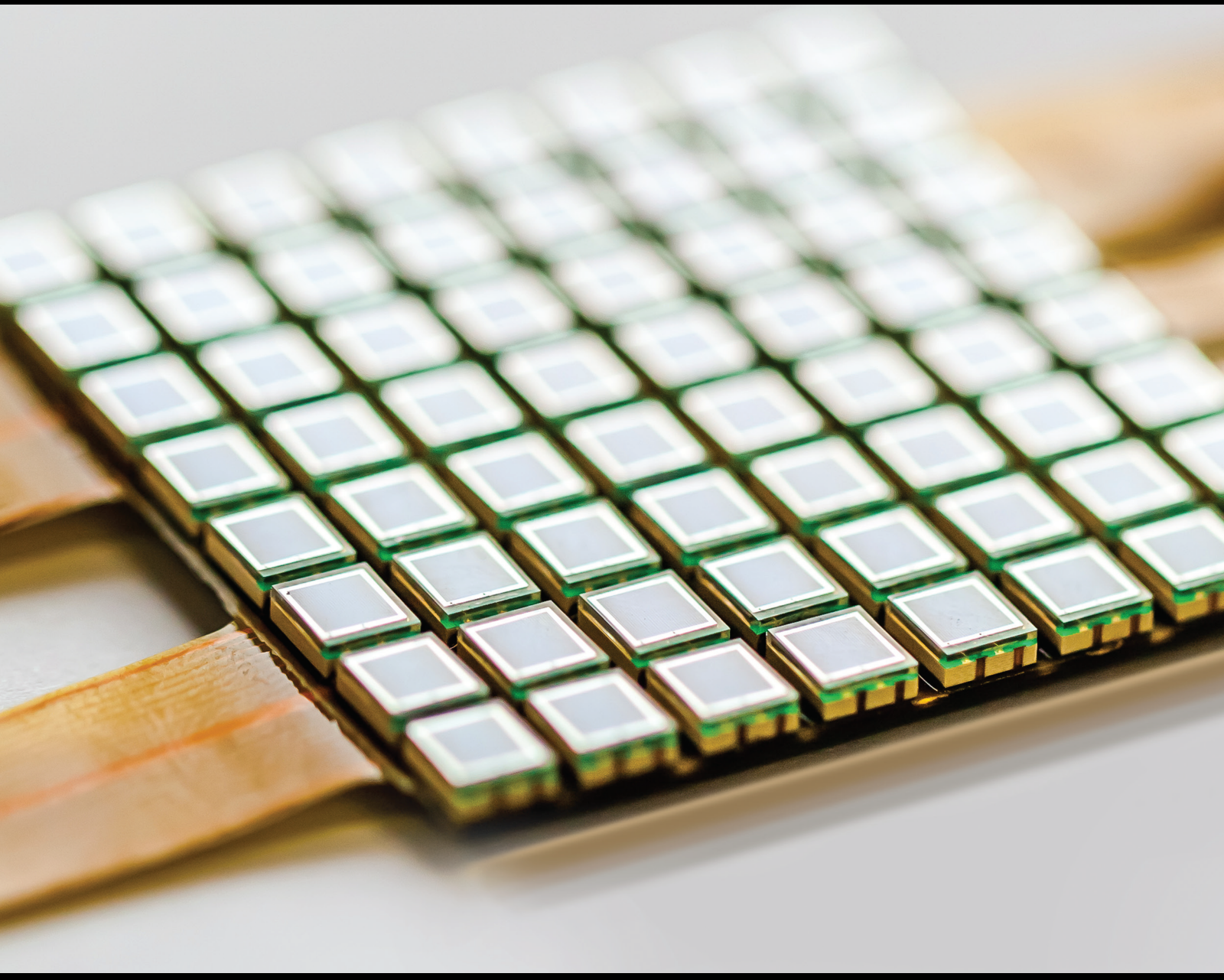

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Contents

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Research Article

Research on Life Extension Method of Transmission Line Intelligent Sensing System Based on Environmental Energy Harvesting

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In this paper, we focus on building and researching the self-power sensor system based on the tiny energy harvesting technology which can be used in the scenario of ubiquitous power Internet of Things (UPIoT) and prove the possibility and efficiency for the life extension of transmission line intelligent sensing system. Large scale of sensor in the smart grid technology application, especially in high-voltage transmission lines, is not convenient; it is worth mentioning that most of all kinds of sensor node equipment using battery power make the life of the equipment or components limited by greatly. Therefore, low power consumption, long life, no battery dependence, free maintenance, and other requirements are increasingly important to solve the difficulties of deployment and maintenance. At the same time, the problem of the battery case electricity use with low efficiency and short life of sensor node has become the bottleneck of further widely deployed wireless sensor node equipment. The power collection technology based on environmental energy can effectively handle with the problems of energy collection efficiency and management that need to be urgently solved in new application scenarios such as zero-standby power consumption devices, remote active tags, battery-free telemetry and remote control, and ultralong life sensing system. By studying various kinds of environmental energy collection technologies and utilizing the conversion and management technologies of available weak environmental energy, such as solar energy and magnetic field energy, into electric energy, this paper establishes an energy conversion test system and configuration model and verifies the feasibility of the assumption of maintenance-free for the intelligent sensing system of transmission lines.

1. Introduction of Transmission Line Intelligent Sensing System and Environmental Microenergy Collection Technology

Smart grid sensing system of the transmission line, conductor temperature, and image conductor is a practical and monitoring system, such as dancing and overhead line transmission tower in the process of forming and ops bolt used in all kinds of intelligence, pressure, and settlement. A huge number of angle sensor mainly depends on the degree of intelligent degree of maintaining the stable working. Therefore, most wireless sensor network nodes are powered by disposable batteries. After being installed, it is very difficult or impossible to replace the equipment maintenance and battery under high voltage and live environment. As a result, energy supply and management of nodes have always been the focus of research in wireless sensor network technology. Although measures of optimizing network structure and reducing node power consumption can reduce energy consumption to a certain extent, they cannot fundamentally solve the problem of node energy depletion. However, the technology of available energy collection which can be collected continuously from the surrounding environment opens up a new direction for solving this problem [1, 2]. At present, the energy collection technologies that have been

applied in the field of power transmission line sensing mainly include solar energy harvesting and magnetic field harvesting.

1.1. Solar Energy. Solar energy extraction mainly converts light energy into electric energy through solar panels to supply power for sensors. Since the energy intensity of light energy varies greatly with time, solar panels are often combined with batteries to form solar power supply systems in practical applications [3]. The principle is shown in Figure 1. The solar power supply system is relatively mature, with high energy conversion efficiency.

The conversion efficiency of mass-produced photovoltaic cells can reach up to 18%, and the energy density is about 3 mW/cm^2. However, the application effect is limited by natural conditions and battery life [4].

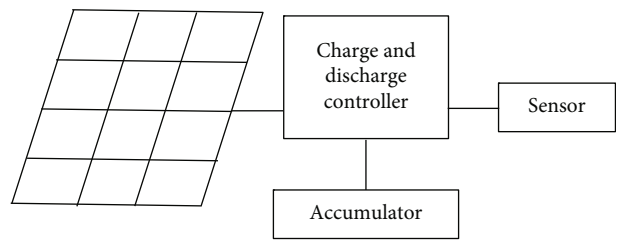

Figure 1: Schematic diagram of solar power supply system.

1.2. Magnetic Field Energy. Magnetic field energy harvesting technology mainly relies on closed coils to generate induced current by induction of the changing magnetic field, so as to realize the conversion of magnetic energy to electric energy [5]. Magnetic field energy capture technology can be divided into invasive and noninvasive according to the deployment mode of energy capture module. Invasive energy harvesting is similar to conventional current transformer (CT) (as shown in Figure 2).

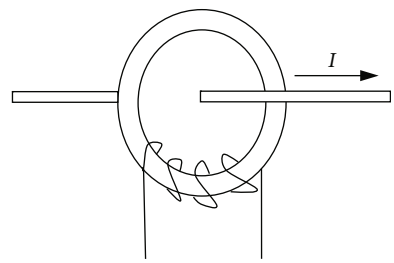

Figure 2: Invasive energy harvesting.

By plugging into the transmission line or AC bus, it generates coupling effect to extract electricity. The coupling effect is good, the energy harvesting power is high, but the operability is poor, and the later maintenance cost is high [6]. Noninvasive energy extraction means that the energy extraction module is placed outside the energy-being extracted device, and energy extraction is carried out through external coupling effect. As shown in Figure 3, the coupling coefficient of noninvasive energy extraction and the power of energy extraction are lower than that of invasive energy extraction.

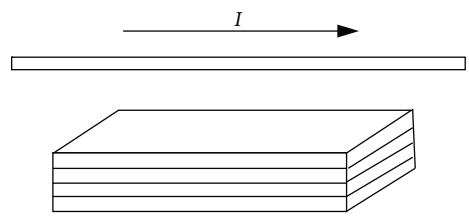

Figure 3: Noninvasive energy harvesting.

The installation of noninvasive energy extraction device does not destroy the structure of the original system and has good operability with low maintenance cost [7]. At present, the invasive magnetic field energy harvesting technology is relatively mature, which can realize the magnetic field energy harvesting under the load of 5A and above lines, and the output power can reach watt level, which has been widely used in power system. Engineering application cases mainly include transmission line temperature sensor based on CT energy extraction, distribution line fault indicator, etc. However, the noninvasive energy capturing technology has few practical applications.

1.3. Laser Power. The main principle of the laser power supply mode [8, 9] is that the laser light source is received at the low potential side. After that, the energy is transmitted to the high potential side through the optical fiber. Then, the light energy is directly converted into electric energy by the photoelectric conversion device, and the stable power output is finally provided after passing through the DC-DC converter. Its advantage [10, 11] is that under relatively stable conditions, a relatively stable power supply voltage can be obtained after conversion; the power supply has small ripple, low noise, and is not easily affected by external factors. This power supply mode also has some disadvantages, such as low photocell conversion efficiency, limited laser output power, and limited power supply.

1.4. Microwave Power. Microwave power supply is a wireless power transmission method [12]. In the process of transmission, the energy loss of microwave is smaller than that of laser power supply, and the transmission energy is larger, which has the characteristics of simple and convenient implementation. However, there are also some shortcomings in the application, such as bringing some interference signals in the microwave transmission process to the normal operation of online equipment, especially in the data transmission and relay protection equipment action.

1.5. Voltage Transformer. The principle of voltage transformer power supply [13, 14] is the same as that of ordinary transformer. A special voltage transformer (PT) is adopted to transform the electric energy from high voltage to low voltage and provide to the electric equipment. It has a stable power output and easy access to electric energy points. The disadvantages are large volume, high cost, and inconvenient installation, which have great influence on operation safety.

Different energy harvesting technologies are suitable for different fields. In response to the needs of large-scale breeding farms for monitoring the ventilation status, a wind-

Table 1: Characteristic of battery and supercapacitor.

Characteristic	Battery	Supercapacitor
Transformation	Chemical–electrical	Electrical
Internal reaction	REDOX chemical reactions	Polarized electrolyte physical reactions
Process reversibility	Charge and discharge process reversible, energy conversion loss	Charge and discharge process reversible
Charging and discharging speed	The general charge and discharge rate is 1-5 times, the maximum discharge rate can be up to 10 times	The higher the charging current, the faster the speed, and within 10 seconds can reach 95% of the rated capacity
Operating temperature	-25°C–+45°C	-40°C–+70°C
Energy density	High, 20-100 wh/kg	Low, 3-15 wh/kg
Charge-discharge efficiency	>95%	>95%
Cycle life	5000-10000	>100000
Environmental protection	Potential pollution	Almost no chemical contamination
Maintenance	Periodic replacement	Maintenance-free

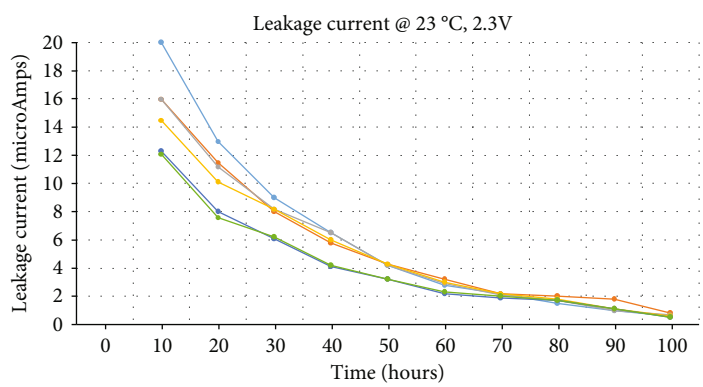

Figure 4: Discharge characteristics of supercapacitor samples.

induced vibration piezoelectric energy capture system can be designed to solve the problem of self-powered monitoring sensors [15]. The sensor self-powered system based on thermoelectric power generation can collect the energy of the temperature difference between the inside and outside of the ventilation pipe to supply power to the sensor monitoring system [16]. For outdoor IoT scenarios, solar energy can be used as an energy source, and the output characteristics of photovoltaic cells can be used for energy harvesting, and the voltage transmission ratio can be improved to realize the system self-powered [17].

2. Selection of System Energy Storage Devices

Rechargeable batteries are commonly used in wireless sensor systems for energy storage. Compared with standard capacitors and batteries, supercapacitors have many advantages, making them as ideal substitutes. These advantages include short charge and discharge times than rechargeable batteries, high efficiency which is up to 98%, lower internal resistance, large power output, better thermal performance, and a better

Table 2: Comparison of supercapacitor charging time.

Super CAP	Super CAP-1	Super CAP-2	Super CAP-3
Parameter			
Beginning voltage	0.7 V	0.7 V	0.7 V
Full voltage	4.48 V	4.48 V	4.48 V
Charging time	11 mins	9 mins	7 mins

Table 3: Comparison of supercapacitor leakage characteristic.

Super CAP	Super CAP-1	Super CAP-2	Super CAP-3
Discharge test result			
	1.5 F, 5 V	1.5 F, 5 V	1.2 F, 5 V
T0	4.48	4.48	4.48
T0+2 hours	3.47	3.384	4.196
T0+4 hours	3.214	3.203	4.119
T0+6 hours	3.019	3.052	4.042

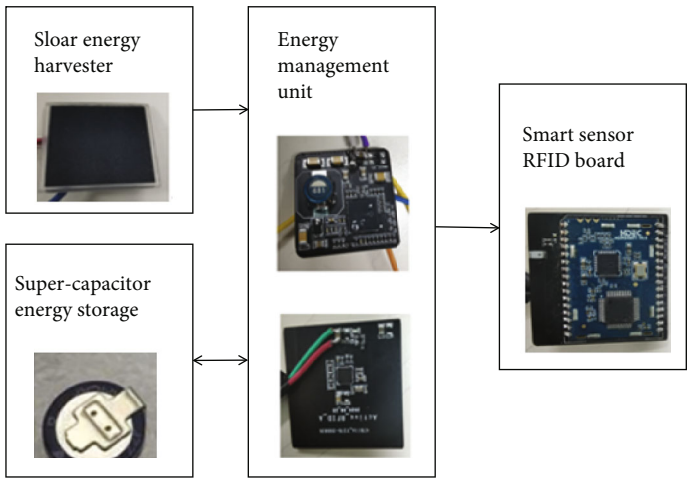

Figure 5: Sensor system diagram.

safety margin than batteries and standard capacitors. More differences between these two kinds of energy storage devices can be found in Table 1.

Supercapacitor is an electrochemical component that uses polarized electrolyte to store energy. It can be used as a power source with special performance between traditional capacitor and battery. Moreover, the energy storage process is reversible, and it can be charged and discharged repeatedly for hundreds of thousands of times. Its outstanding advantages are high power density, short charge and discharge time, long cycle life, and wide operating temperature range. The selection of supercapacitors, power requirements, discharge time, and system voltage variation play a decisive role. There are two factors that will cause the voltage drop of the supercapacitor. One factor is the energy released by the supercapacitor; the other factor is the internal resistance of the supercapacitor. In the very fast pulse, the internal resistance part is the main factor. In contrast, in the long process of discharging, the capacitive part is the main part.

Supercapacitors have recommended operating voltage or optimum operating voltage based on the maximum working time of the capacitor at its highest set temperature. If the applied voltage is higher than the recommended voltage, the life of the capacitor will be shortened. If the overvoltage lasts for a long time, the electrolyte inside the capacitor will decompose and form a gas. When the pressure of the gas increases gradually, the safety hole of the capacitor will break. A short period of overvoltage is tolerable for a capacitor.

When a supercapacitor is discharged, it discharges according to a slope curve. When an application specifies the capacitance and internal resistance requirements of the capacitor, it is most important to understand the influence of resistance and capacitance on discharge characteristics. Resistance is the most important factor in pulse applications, and capacity is the most important factor in small current applications. The calculation formula is as follows:

$$V = I\left(R + \frac{T}{C}\right). \tag{1}$$

Table 4: Sensor system configuration model.

Load parameter		Marks
Vin (V)	3	System operation voltage
T0 (s)	1800.73	Operation period
T1 (s)	0.73	Operation time
Isys (A)	0.015	Operation current
Isleep (A)	0.000014	System-free current
Iavg (A)	0.00001	System average current
c (W/S)	0.001217	System average power

V is the starting work voltage, and as the difference between the working voltage, I is the discharge current, R is the DC resistance, T is the discharge time, and C is the capacitance in pulse application. Because the current is very big, in order to reduce the voltage drop, the low resistance (ESR) of the supercapacitor (R value) is chosen; in small current applications, the large capacity of supercapacitor (C value) needs to be chosen in order to reduce the voltage drop.

Self-discharge and the leakage are essentially the same, in view of the supercapacitor structure, equivalent to inside the capacitance between the positive and negative has a high resistance current path; it means at the time of capacitor charging, there will be an additional current at the same time. When a capacitor is in charge, we can regard this current as leakage current. When the charging voltage is removed and the capacitor is not connected to the load, the current causes the capacitor to be in the discharge state. At this point, the current is regarded as the self-discharge current.

In order to make the measurement of leakage current or discharge current more accurate, we chose the general supercapacitor samples which discharge characteristics are shown in Figure 4. The capacitor must be continuously charged for more than 72 hours to ensure the leakage slope tends to be stable. The leakage is determined by the structure of the capacitor. A supercapacitor is a parallel connection of

Table 5: Calculation results under the condition of 2 mA charging current.

Vmax (V)	4.8	Maxim voltage of output
Vmin (V)	1.8	Minimum voltage of output
Ileakage (A)	0.00001	Leak current of supercapacitor
Icharge (A)	0.002	Charging current under indirect solar conditions
Tdis (hrs)	72	Discharge time (determined by requirement:3 days without solar)
Capacity (F)	4	Capacity of supercapacitor
Tcharge (hrs)	1.65	Charge time

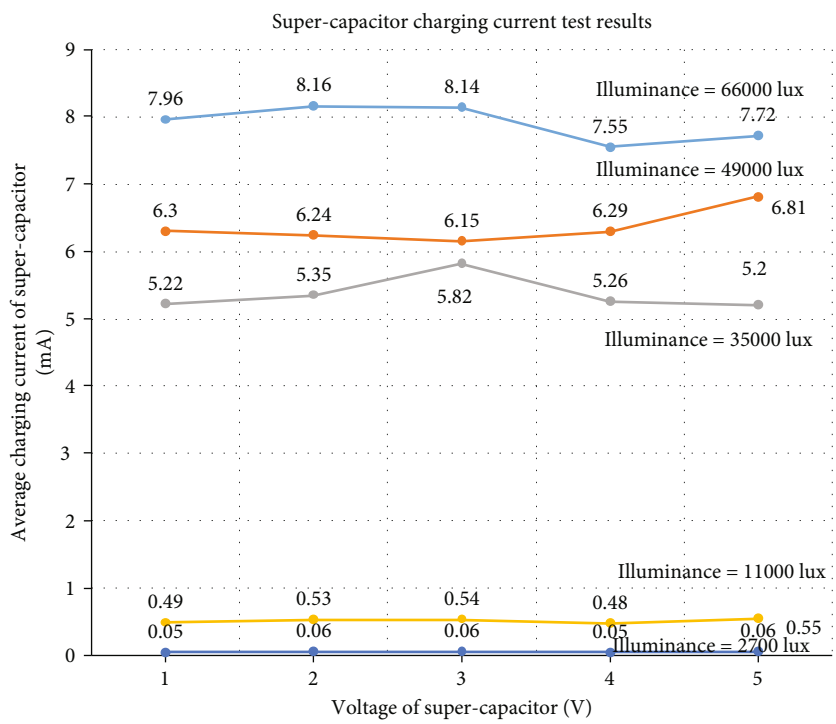

Figure 6: Supercapacitor charging current with the change of illuminance.

several supercapacitors with different internal resistances. When the supercapacitor is charged, the supercapacitor with low internal resistance charges fast, and the voltage can quickly rise to the value of the charging voltage. When the charging voltage of the supercapacitor is removed, if the high internal resistance supercapacitor is not fully charged, the low internal resistance supercapacitor starts to discharge to the parallel high internal resistance supercapacitor, so that the voltage across the capacitor will drop relatively fast. The capacitor is usually considered as a relatively large self-discharge. It must be noted that the larger the capacitance of the capacitor, the longer it takes for the capacitor to be fully charged.

In this paper, three types of supercapacitors are selected to test the actual charge-discharge effect. The system is set with an overvoltage protection of 4.5 V and a discharge threshold of 2.8 V. The test results are as follows:

According to the test data shown in Tables 2 and 3, supercap-3 has excellent performance in terms of the overall charge-discharge effect and self-leakage; supercap-3 is selected as the energy storage element of the system.

3. Verification of Self-Powered Sensor System Based on Microsolar Energy Extraction Sensor

With the development of ubiquitous power Internet of Things, all kinds of wireless smart sensors are gradually widely used. In order to solve the problem of energy acquisition, support the long life cycle, and reduce the cost of manual maintenance of power system, this system focuses on the investigation of the energy demand of passive sensors commonly used in power system and selected the representative smart sensor RFID system as the research object to verify the feasibility.

The system converts solar energy into electric energy through a 2.5 cm ∗ 2.5 cm solar panel suitable for small

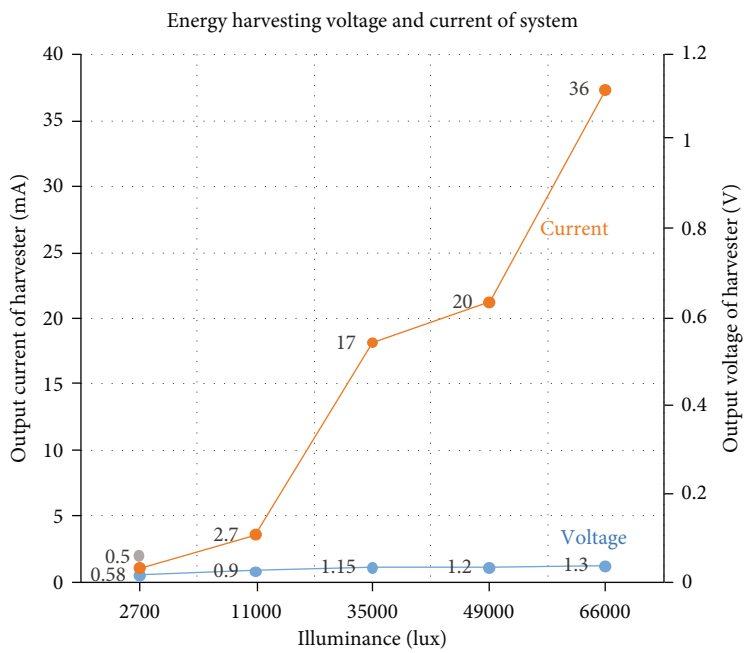

Figure 7: Energy harvesting voltage and current from solar panel.

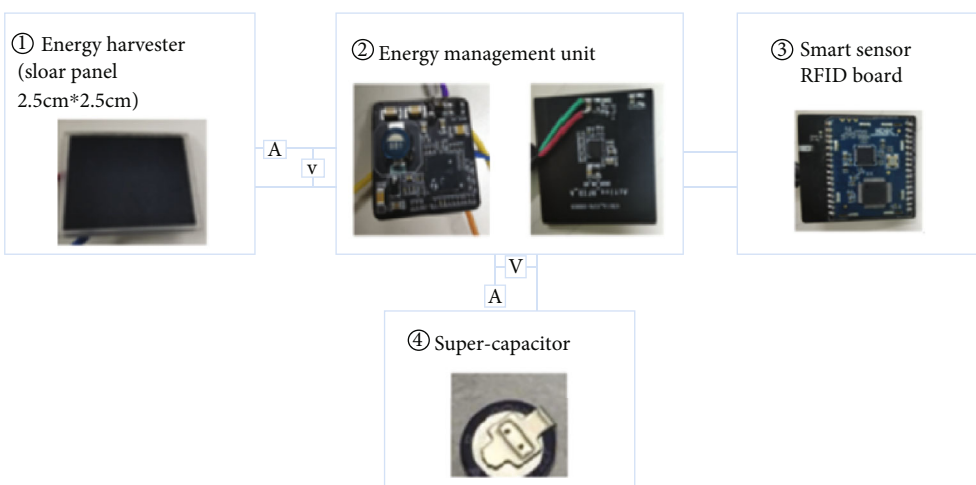

Figure 8: Experimental test platform.

sensor nodes and then converts nanoelectrical energy (only a few hundred milliwatt) into electric energy that can be used for smart sensor RFID system controllers through a power management chip with ultralow voltage start-up characteristics. Current system uses small solar panels as energy input, according to the previous section of the contrast of characteristics between supercapacitors and the ordinary rechargeable batteries; environmental temperature change is big. Considering the characteristics of large environmental temperature variation, different system load energy consumption, and high real-time charging frequency of environmental energy in practical applications, this paper uses the supercapacitor as the energy storage element and connects the back end to a real pressure data reporting sensor.

Based on the above analysis, we built a sensor system that can take a long life without maintenance as shown in Figure 5. The sensing system consists of solar panel energy harvester, microenergy management unit, smart sensor RFID board, and supercapacitor. The system emits a 15 mA current signal every 30 minutes which continues 730 ms. System's free current is 14 μA. Supercapacitor leakage current is 10 μA.

3.1. System Configuration Model. The sensor node power supply system is based on ambient energy collection research output model, through calculation of the load power system based on the need to meet the continuous running time. The configurations of supercapacitors and solar

panels are required to guide the system hardware architecture of the subsequent application design. At the same time, it can be used to evaluate the efficiency of the docking of other energy extraction devices.

Firstly, the average power of the system is calculated through the load power consumption, and the results are shown in Table 4.

$$P(\text{average power}) = \frac{[(\text{Vin} \times \text{Isys} \times T1) + (\text{Vin} \times \text{Isleep} \times T3)]}{T0}, \tag{2}$$

$$\text{Iavg}(\text{average current}) = \frac{[(\text{Isys} \times T1) + (\text{Isleep} \times T3)]}{T0}. \tag{3}$$

According to the system configuration in the previous section, the following data parameters can be obtained. According to the above formula, the average power consumption of the system under the configuration condition of the system is 1.217 mW, which can be used to calculate the supercapacitor configuration of the subsequent system under the condition of no light for 3 days.

The requirements of working voltage threshold, load current, the self-leakage, and working time of the supercapacitor are important, and the factors also were analyzed in the previous section; the capacitance required by the system can be calculated according to the average leakage of current, and the formula is shown as follows:

$$\begin{aligned}\text{Capacity}(F) &= (V\ \max + V\ \min) \times I \times \frac{t}{V\ \max^2 - V\ \min^2} \\ &= \frac{(V\ \max + V\ \min) \times \text{Ileakage} \times 60 \times 60}{(V\ \max\ 2 - V\ \min\ 2)},\end{aligned} \tag{4}$$

$$\text{Tcharge}(\text{Charge time}) = \frac{[C \times (\text{Vmax} - \text{Vmin})/\text{Icharge}]}{3600}. \tag{5}$$

Table 5 shows the calculation results according to the charging efficiency after the output current of solar panels under solar indirect conditions converted by the power management system, and the charging current is 2 mA.

Finally, the result obtained through the data model simulation is that when the ultralow power management system is configured with the upper limit of the charging voltage of the supercapacitor is 4.8 V, and the discharge is as low as 1.8 V; the size of the supercapacitor required for the system to maintain no light for 3 days is 4 Farad.

3.2. Experimental Test Platform and Results. In order to evaluate the system feasibility, we developed an experimental test platform, as shown in Figure 5, which is comprised of energy harvester, energy management element, supercapacitor, and smart sensor RFID board as load. One supercapacitor was chosen as an electric storage element to be evaluated considering the situation for nonlight. Two ammeters (A) and voltmeters (V) are used for measurements of current and voltage, respectively.

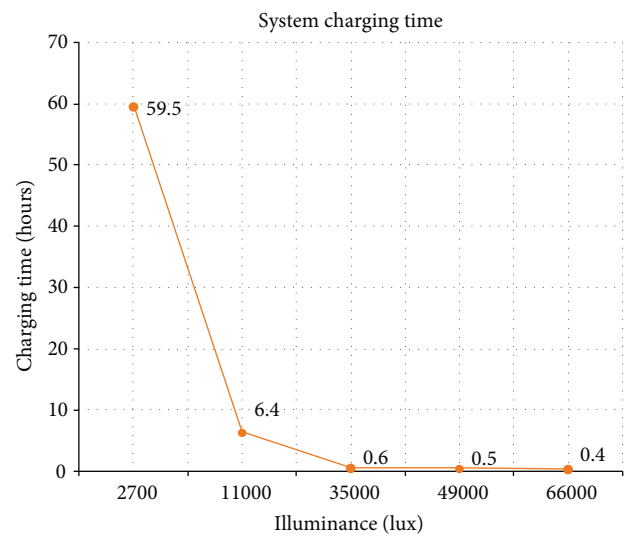

Figure 9: System charging time.

It is very meaningful to test system charging current under the real different lighting conditions. Figure 6 shows the test results of supercapacitor charging current under the change of illuminance, the stronger the light, the greater the charging current. If the illuminance is 66000 lux, the charging current of system can reach 7.55 mA with the 4-Farad supercapacitor.

The energy provided by the energy harvester almost determines the available power of the system. Figure 7 shows the energy harvesting voltage and current test results.

To ensure the system normal operating, supercapacitor's voltage range should be 1.8 V~4.8 V; this experiment tested the charging time of supercapacitor from 1.8 V~4.8 V. As shown in Figure 8, the charging time is 0.42 hours when the system works under the condition of illuminance = 66000 lux which is shown in Figure 9. This light intensity is consistent with sunny day.

Considering the application model as shown in Table 4, the discharging time is tested under the condition of no input power. If we choose the 4-Farad supercapacitor, the system can work continuously for 73.3 hours without interruption (as shown in Figure 10).

As all the research above, the sensing system we built emits a 15 mA current signal every 30 minutes which continues 730 ms. By calculation, the average current consumption of the system is 0.006 mA. System's free current is 14 μA, and the supercapacitor leakage current is 10 μA. We can get that the total system power consumption is 30 μA. When the load voltage and charging voltage are the same, as long as the charging current of the supercapacitor is greater than 30 μA, it can ensure uninterrupted operation of the sensor node system. As shown in Figure 6, under the condition of illuminance greater than 11000 lux, the charging current is about 500 μA. Two hours of the same light intensity can meet the consumption of the system 24 hours a day.

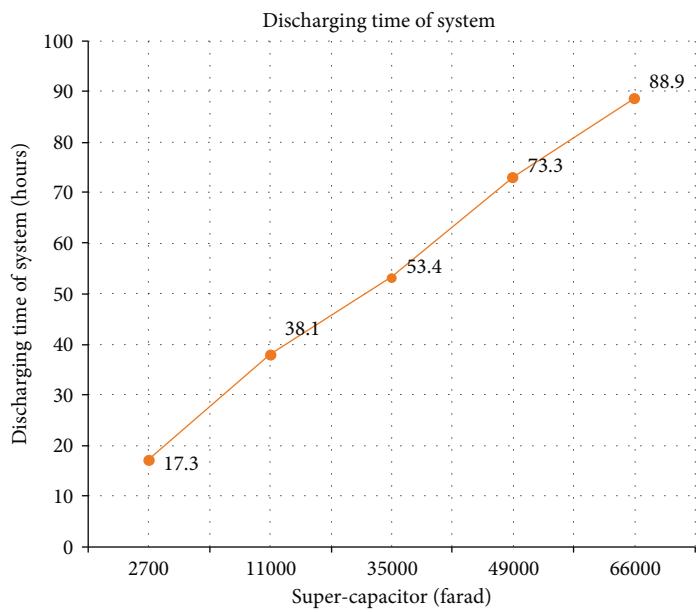

Figure 10: Discharging time of system test results, under the condition of no input power.

4. Conclusions

This work proposes a sensor micropower energy collection system and an effective detection method according to the energy utilization in the working environment of the electric energy sensor. The experimental results confirmed the feasibility of using environmental energy to supply power to the sensor system. The system can realize the self-powering of the low-power sensor nodes and ensure the long-term stable operation of the sensor node. By analyzing the current status of microenergy harvesting technology and the general characteristics of wireless sensors, a theoretical model of sensor energy supply-demand relationship is created. In practice, it is equipped with a microenergy harvesting management system model based on low-sensitivity sensor sensors. The actual test results demonstrate in theory and practice that the use of a microenergy harvester, a low-power ultralow voltage start-up power management chip, and a supercapacitor system architecture can provide the daily energy required by the wireless sensor system. In this way, small solid-state batteries can be added to prevent the system from inadequate energy supply accidents, extending the working life of the sensor and the maintenance-free period. So, the energy harvesting system solves the problem of uninterrupted self-supply of sensor nodes without nonrechargeable battery. The experimental results show that the self-powered system can solve the energy supply problem of low-power smart sensors, save manpower maintenance costs, use environmental energy to obtain energy, reduce environmental pollution, and improve the reliability of sensor detection devices. The experimental results also show that it is feasible to obtain energy from the natural environment to supply a low-power sensor system. At the same time, this solution would rely on and be restricted by the development of energy harvester technology, so we use the most mature energy harvesting equipment to do the research; in order to improve energy utilization efficiency, further research on energy harvesting technology and energy storage technology is needed, including energy harvesting materials, methods, and shapes.

The study also for the integration of intelligent sensor and transmission line tower label provides a possibility and can solve common problems of transmission tower label, because the passive label communication distance is very short; it must be hanged on the low part of the tower, but it is not convenient for human check. So, the minimized power system would make it possible to hang on the top of the tower; also, the combination of smart sensor and RFID system will further promote development of power transmission lines in intelligent monitoring scenarios of the system integration process. It provides important and reliable technical support for its intelligentization, miniaturization, and integration.

Self-powered sensors based on environmental energy harvesting have the advantages of long life and maintenance-free. This technology will become a hot spot and development trend in the research of low-power active systems in the future, especially for the use of energy resources in the working environment of electric power sensors under typical application scenarios of electric power. In order to solve the power supply problem of the power transmission and transformation status monitoring sensors, the abundant magnetic field energy around the transmission cable can be used to develop a self-powered system based on magnetic field energy for the transmission cable and converter valve application scenarios to improve the reliability and stability of the monitoring sensors. With the construction and development of ubiquitous power Internet of Things, wireless sensing technology has broad application prospects in the fields of power equipment status monitoring, power system fault diagnosis, and fault early warning and location of transmission lines. Transmission lines are

an important part of the power grid. Regular inspections of transmission lines are the main means to ensure the normal operation of the power grid. Regular inspections waste manpower, financial resources, and material resources, so state inspections are used. As temperature sensor, humidity sensor, or strain clamp sensor that detect important states of transmission lines, its power supply cannot meet the long-term and reliable operation of the sensor. The multiparameter energy harvesting system can solve the power supply problem of a variety of wireless sensor devices.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

There is no conflict of interest regarding the publication of this paper.

Acknowledgments

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Research Article

A Small-Area, Low-Power Delta-Sigma DAC Applied to a Power-Specific Chip

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This paper introduces a small-area, low-power delta-sigma DAC that can support power line carrier communication. In order to achieve the oversampling ratio of 128, a three-stage cascaded half-band filter is utilized. An optimized sturdy MASH $\Delta\Sigma$ modulator was used to avoid instability caused by high-order shaping and reduce the area at the same time. The postanalog reconstruction includes a switched-capacitor DAC (SC DAC) and a 4-tap FIR/IIR hybrid filter, which not only meets the requirements of low power but also promotes the out-of-band SNR. The final chip is fabricated in a 55 nm CMOS process, occupies 0.08 mm^2, and consumes 1.5 mW of analog power at 2.5 V supply. The simulation results show that the dynamic range is 85.7 dB, while the out-of-band SNR is 40.5 dB.

1. Introduction

The smart grid is a new type of grid based on the physical grid, combined with modern advanced computer technology, information technology, sensor measurement, and other technologies. Different from the traditional power grids in the past, today's power grids are not limited to one-way collection and have their own networking function, which can realize the interconnection of everything and the smart life of smart electricity. For example, in power line carrier communication (PLC) technology, wires can be used to distribute power to consumers and transmit data. In the PLC analog front-end transmitter, the digital-to-analog converter (DAC) is responsible for converting the digital baseband signal into an analog signal and loading it into the power grid. Low power and high resolution are required for DAC in PLC.

While increasing the function and reducing the size, extending the service life of the battery has been the focus of smart device design engineers for many years [1]. Low power consumption, small area, and high integration are the keys to the design of Very Large Scale Integration (VLSI). $\Delta\Sigma$ DAC is widely used in portable devices and smart grid equipment because of its low-speed, high-precision, high-integration, and low-cost characteristics.

The delta-sigma DAC introduced in this article has made a comprehensive consideration of performance, power consumption, and area in the digital and analog design. In the digital difference filter part, a three-stage half-band filter (HBF) cascade is used to reduce the number of filter stages. At the same time, an optimized sturdy MASH $\Delta\Sigma$ modulator is used to achieve the same signal-to-noise ratio while avoiding redundant matching circuits and further reducing the area. In addition, in the subsequent analog reconstruction part, the SC DAC is used to integrate the 4-tap FIR/IIR hybrid filter structure, which not only meets the requirements of low power consumption but also improves the out-of-band signal-to-noise ratio [2].

2. Materials and Methods

2.1. Proposed $\Delta\Sigma$ DAC Architecture. The $\Delta\Sigma$ DAC is composed of a digital front-end module and an analog reconstruction one. The digital front-end module includes a 128x interpolation filter, sturdy MASH 2-1 delta-sigma modulator

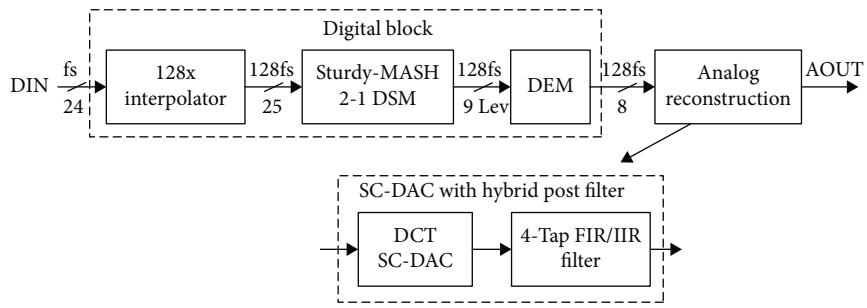

Figure 1: Delta-sigma DAC diagram.

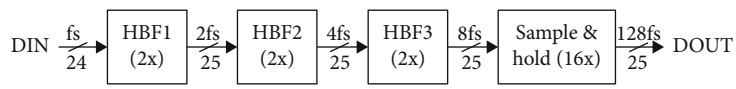

Figure 2: Interpolation filter diagram.

(DSM), and dynamic element matching (DEM); the analog reconstruction module includes a SC DAC and a 4-tap FIR-IIR hybrid postfilter. Figure 1 is the architecture diagram of the $\Delta\Sigma$ DAC. The input is a 24-bit PCM digital signal, and its sampling frequency is fs = 44.1 kHz. First, the signal is oversampled by using an interpolation filter by 128 times; then, an optimized MASH 2-1 DSM performs noise shaping on the signal, pushing the noise to high frequency and at the same time converting the high-bit digital stream into low-bit (4-bit) 9th-order digital flow; then, the DEM algorithm disrupts its thermometer coding bits to reduce the unit capacitance mismatch of the subsequent SC DAC; finally, the SC DAC realizes the digital-to-analog function, and the subsequent filter filters out-of-band noise.

2.1.1. Interpolation Filter. Considering the linear phase, a finite impulse response (FIR) filter is utilized instead of an infinite impulse response (IIR) filter [3]. The former has the virtues of simplicity and high feasibility. In order to further shrink the area, this design uses a half-band filter (HBF), a type of FIR, which has the characteristics of small filter coefficient multiplication and coefficient symmetry, and half of the coefficient is 0.

Figure 2 shows the diagram of the interpolation filter. The interpolation filter adopts a three-stage HBF cascade structure. The first two stages achieve the OSR (oversampling ratio) of 8, and the last stage is a sample-and-hold circuit, which increases the oversampling rate to 128 times. Table 1 summarizes the technical indicators of the three-level HBF.

2.1.2. Sturdy MASH Delta-Sigma Modulator. This design adopts sturdy MASH DSM. The input is 25 bits, while the output is the 9th order. Generally speaking, it is an effective way to improve the signal-to-noise ratio (SNR) with high-order loop filters in DSM. However, the higher the order, the worse the stability and the more difficult the engineering realization [4]. The authors [5] proposed the Multistage Noise Shaping Modulator (MASH DSM). It eliminates the stability problem of high-order modulators through measurement and subtraction between multiple levels. However,

Table 1: Technical indicators of the three-level HBF.

	Orders	Passband frequency (normalized)	Passband ripples (dB)
HBF1	70	0.4535	0.02
HBF2	10	0.2268	0.016
HBF3	6	0.1134	0.01

in terms of $\Delta\Sigma$ ADC, the MASH structure has a matching problem between analog and digital parts [6]. Considering $\Delta\Sigma$ DAC, there is also a trade-off between the accuracy and area. To solve the aforementioned shortcomings, scholars have successively proposed and studied the sturdy MASH $\Delta\Sigma$ modulator [6–9]. In short, compared with the single-stage structure, sturdy MASH DSM is more stable and suitable for multibit quantization. Furthermore, compared with the MASH structure, the output of the second stage is coupled back into the first loop without additional cancellation logic, thereby reducing the area.

Figure 3 shows the architecture of sturdy MASH 2-1 DSM. As the name implies, the DSM is divided into two stages. The loop filter of the first stage adopts a second-order cascade-of-resonators feedback form (CRFB) and optimizes the in-band zero to produce two complex zeros located at 20 kHz [2], which further improves SNR; the second stage is a first-order function. The signal transfer function (STF) and noise transfer function (NTF) of the first stage are as follows:

$$\mathrm{STF}_1 = \frac{z^{-1}}{1 + g \bullet z^{-1}}, \tag{1}$$

$$\mathrm{NTF}_1 = \frac{1 + (g-2) \bullet z^{-1} + z^{-2}}{1 + g \bullet z^{-1}}. \tag{2}$$

The STF and NTF of the second stage are as follows:

$$\mathrm{STF}_2 = 1, \tag{3}$$

$$\mathrm{NTF}_2 = 1 + z^{-1}. \tag{4}$$

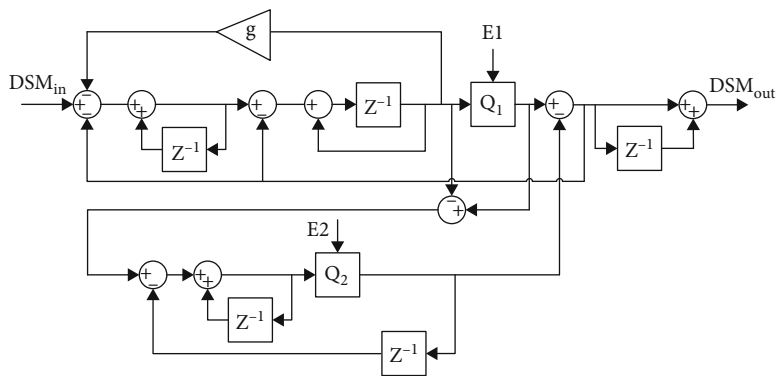

Figure 3: Sturdy MASH 2-1 DSM architecture.

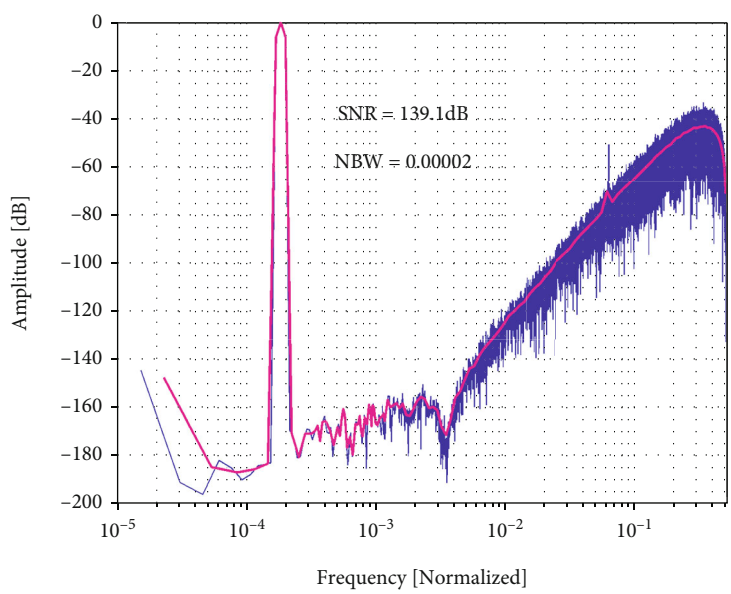

Figure 4: DSM simulation spectrum.

The equation of the overall DSM is as follows:

$$\mathrm{DSM_{out}} = \mathrm{DSM_{in}} \bullet \mathrm{STF_1} + E_1 \bullet \mathrm{NTF_1} \bullet (1 - \mathrm{STF_2}) - E_2 \bullet \mathrm{NTF_1} \bullet \mathrm{NTF_2}. \tag{5}$$

$\mathrm{DSM_{in}}$ and $\mathrm{DSM_{out}}$ are the input and the output of DSM, respectively. STF_i, NTF_i, and E_i are the STF, NTF, and quantization error of the i-th stage, respectively, and g is the feedback coefficient in the first stage (the actual value is 2^{-11}).

By incorporating Equations (1)–(4) into Equation (5), the first-level quantization noise (E1) can be eliminated, leaving only the second-level quantization noise (E2), so that the overall DSM STF and NTF formulas are as follows:

$$\begin{aligned} \mathrm{STF_{top}} &= \frac{z^{-1}}{1 + g \bullet z^{-1}}, \\ \mathrm{NTF_{top}} &= \frac{\left(1 - z^{-1}\right) \bullet \left[1 + (g - 2) \bullet z^{-1} + z^{-2}\right]}{1 + g \bullet z^{-1}}. \end{aligned} \tag{6}$$

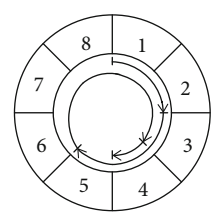

Figure 5: DWA algorithm diagram $\{2, 3, 6, 1\}$.

The last module of DSM, i.e., $1 + z^{-1}$, induces a pole at fs/2 to attenuate high-frequency noise and idle sounds [10]. MATLAB's SIMULINK tool was used to simulate DSM, and the input signal is 1 kHz, which was sampled at 128×44.1 kHz. Figure 4 shows the DSM simulation spectrum.

It shows that there is a notch at fs/2 (normalized = 1) and 20 kHz (normalized = $3.543e^{-3}$). The former is due to the function of $(1 + z^{-1})$ followed by DSM, while the latter is caused by the zero optimization of the first stage in DSM. The simulation results are consistent with the previous theory.

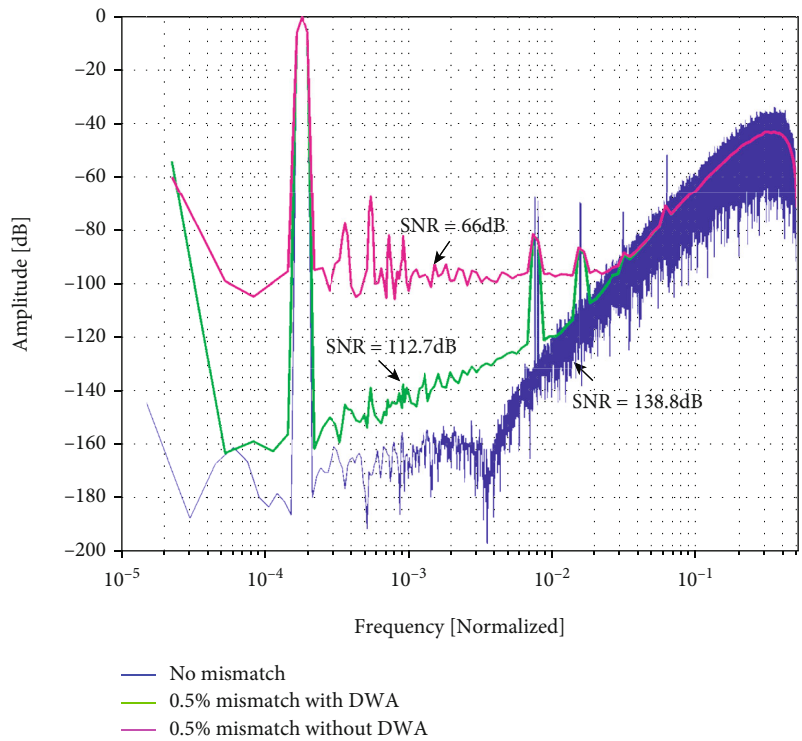

Figure 6: Digital front-end output spectrum, with no mismatch, 0.5% mismatch without DWA, and 0.5% mismatch with DWA.

2.1.3. DEM. Since the DSM uses multibit quantization, a subsequent multibit DAC is required for digital-to-analog conversion. Due to process limitations, the unit capacitance cannot be perfectly matched; that is, there are inevitable nonlinear problems. In addition to factory calibration (such as laser fine-tuning) and analog calibration [4], a more cost-effective way is digital correction. The DEM algorithm is commonly applied in digital correction. DEM uses a random selection algorithm to make unit devices as equally probable as possible and converts mismatch errors into white noise [11]. Data Weighted Average (DWA) is the first-order error shaping algorithm of DEM, and its working mechanism is rotation selection.

An example of the 8-element DWA algorithm is illustrated in Figure 5. Assume that the selection sequence is 2, 3, 6, 1, and each element is selected cyclically. Under the high-frequency clock, the cumulative average of the error is close to 0. That is, the low-frequency adaptation error is pushed to the high frequency. In addition to the first-order error shaping algorithm, many researchers have proposed second-order or even higher-order shaping algorithms, such as vector-based error shaping [12–14] and tree structure-based error high-order shaping [15]. Owing to its complicated circuit structure and stability issues, high-order shaping is not taken into our consideration, although it has a better noise shaping performance than the first-order one.

The digital front-end output spectrum, with no mismatch, 0.5% mismatch without DWA, and 0.5% mismatch with DWA, is shown in Figure 6. The simulation tool is MATLAB SIMULINK. In order to better distinguish between different curves, the 0.5% mismatched curve has been processed by a log smooth function to average the power and reduce the variance [4]. Under a 0.5% mismatch, SNR is 65 dB without DWA, while SNR with DWA is only 20 dB lower than the ideal SNR, which meets the design requirements.

2.1.4. Analog Reconstruction Module. As mentioned earlier, the final output of the DSM is a 9th-order bit stream; therefore, a low-bit DAC is needed to realize the digital-to-analog function. At the same time, because DSM introduces a lot of high-frequency noise, a poststage filter is included to purify the signal. The main purpose of this design is low power consumption and small area, so the direct charge transfer switch capacitor DAC (DCT-SC DAC) is adopted [11, 16]. Compared with current steering DAC, DCT-SC DAC is more insensitive to clock jitter and has lower power consumption. Furthermore, this structure allows hybrid filtering of FIR and IIR, which can significantly reduce out-of-band noise. In order to obtain a larger out-of-band SNR (SNR_{out}), the authors in [2] extended the FIR tap on the basis of [16]. The analog reconstruction module of this design is SCT-SC DAC, integrating a 4-tap FIR/IIR hybrid filtering function.

Figure 7 is a block diagram of the analog reconstruction module. There are 4 groups of different unit capacitor arrays. The input is the thermometer code after DEM scrambled a total of 16 bits (of which 8 bits are logical NOT), controlling different switches (SW). The input code is sequentially delayed by a unit clock, controlling the switches of different

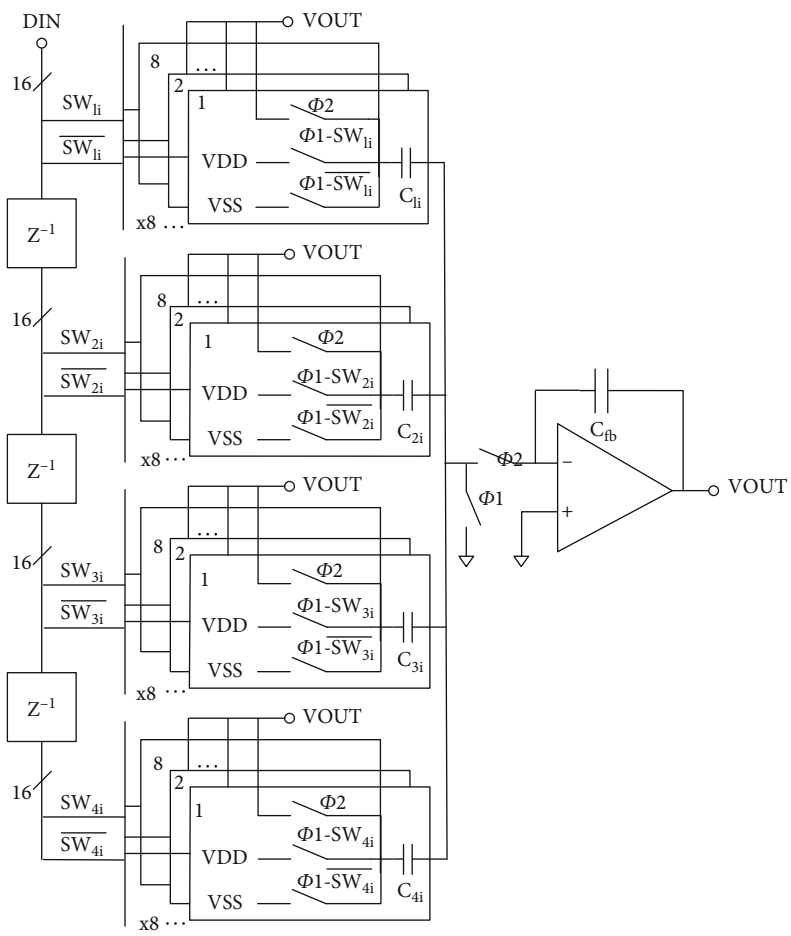

Figure 7: Block diagram of the analog reconstruction module.

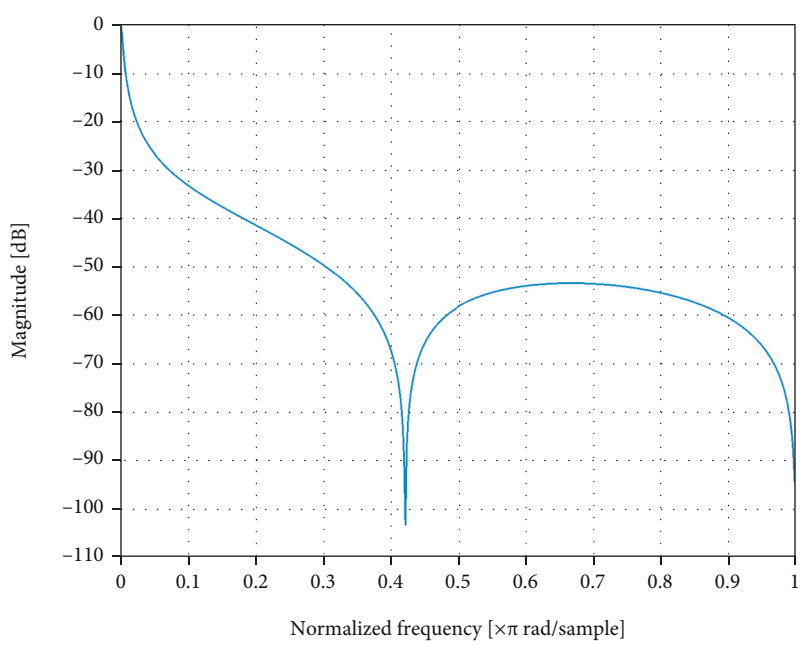

Figure 8: 4-tap FIR/IIR frequency response curve.

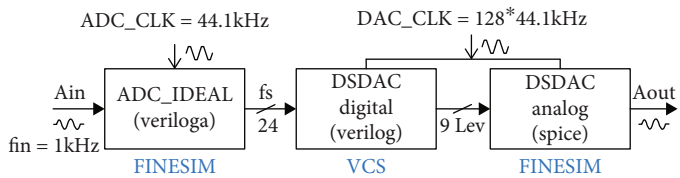

Figure 9: DSDAC hybrid simulation structure.

groups to function the 4-tap FIR filtering [2]. During phase 1 ($\Phi 1$), all unit capacitors (C_{1i}, C_{2i}, C_{3i}, and C_{4i}) are sampled (charged or discharged). During phase 2 ($\Phi 2$), all potential capacitors are connected in parallel with C_{fb} and direct charge transfer occurs. Since the amplifier does not provide driving current, the power consumption is greatly reduced, and the design of the amplifier will not be tricky. An operational amplifier with fully differential input and single-ended output is used for the sake of the small area. The transmission equation of the hybrid 4-tap FIR/IIR is as follows:

$$H(z^{-1}) = \frac{C_1 + C_2 \bullet z^{-1} + C_3 \bullet z^{-2} + C_4 \bullet z^{-4}}{C_{fb} + C_1 + C_2 + C_3 + C_4 - C_{fb} \bullet z^{-1}},$$
$$C_1 = \sum_{i=1}^{8} C_{1i}, C_2 = \sum_{i=1}^{8} C_{2i}, C_3 = \sum_{i=1}^{8} C_{3i}, C_4 = \sum_{i=1}^{8} C_{4i}. \quad (7)$$

In this design, $C_{fb} = 16$ pF, $C_{1i} = 40$ fF, $C_{2i} = 20$fF, $C_{3i} = 20$ fF, and $C_{4i} = 40$ fF. With MATLAB simulation, the frequency response curve of the hybrid 4-tap FIR/IIR transfer function is shown in Figure 8. It can be seen from the figure that the curve has notches at fs/2 and $0.42 \cdot$ fs/2, and its cut-off frequency is about $0.018 \cdot$ fs/2 = 50 kHz, which greatly reduces SNR_{out} while not compromising the in-band signal.

2.2. Simulation and Results. This design adopts a simulation method called digital-analog hybrid simulation, with VCS (digital front-end part) and FINESIM (ideal ADC and analog part) tools, verifying and analyzing the entire DAC system. A block diagram of the DSDAC hybrid simulation structure is shown in Figure 9. The input analog signal frequency is 1.03359 kHz (the number of FFT points is 216, and the signal frequency is perfectly located at one of the bins of the FFT, which can effectively avoid spectrum leakage [4]), and the sampling frequency is 44.1 kHz. We use the Verilog language to construct an ideal 24-bit ADC to assist simulation. The synthesizable behavioral Verilog is used as a simulation model for the digital front-end part, and the XRC Spice netlist is used as the analog simulation model.

The data of the transient simulation is output to a file at 1/fs time interval. Then, we import the file into MATLAB for spectrum analysis, with the number of FFT points being 216. Figure 10 presents an in-band output spectrum of 1 kHz full amplitude input signal. And the SNR is 63.2 dB. An in-band output spectrum of 1 kHz -6 dB input signal

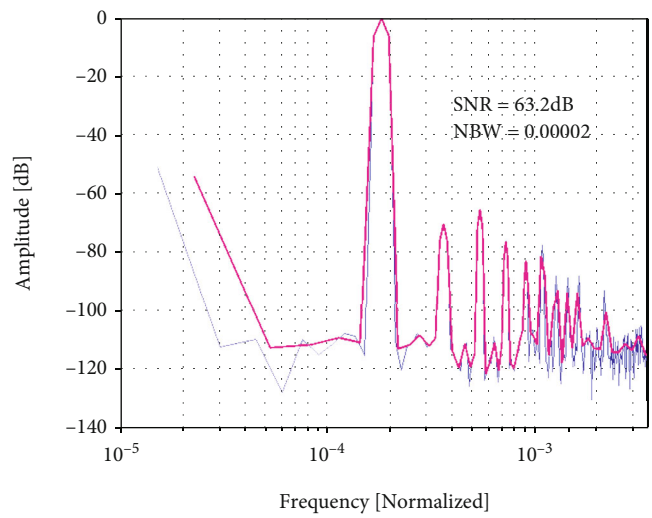

Figure 10: In-band output spectrum of 1 kHz 0 dBFS input signal.

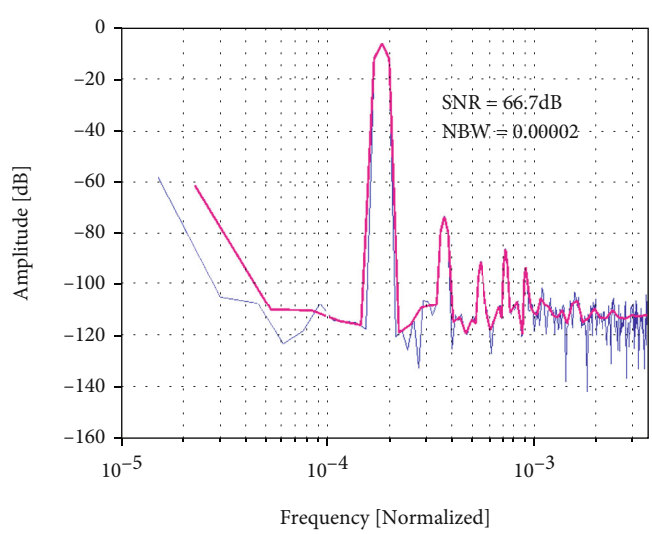

Figure 11: In-band output spectrum of 1 kHz -6 dBFS input signal.

(-6 dBFS) is shown in Figure 11, and the SNR is 66.7 dB. Figure 12 is an in-band output spectrum of 1 kHz -60 dBFS input signal, and the SNR is 25.7 dB. For audio equipment, the dynamic range (DR) is usually calculated as SNR of 1 kHz at -60 dBFS [16]. Therefore, the dynamic range is

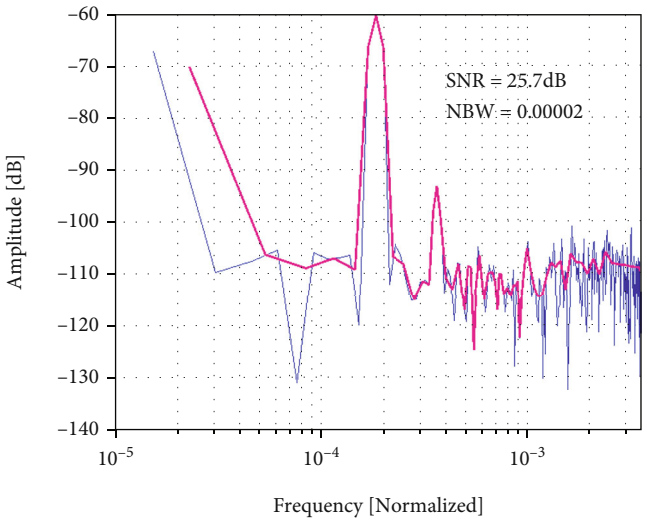

Figure 12: In-band output spectrum of 1 kHz -60 dBFS input signal.

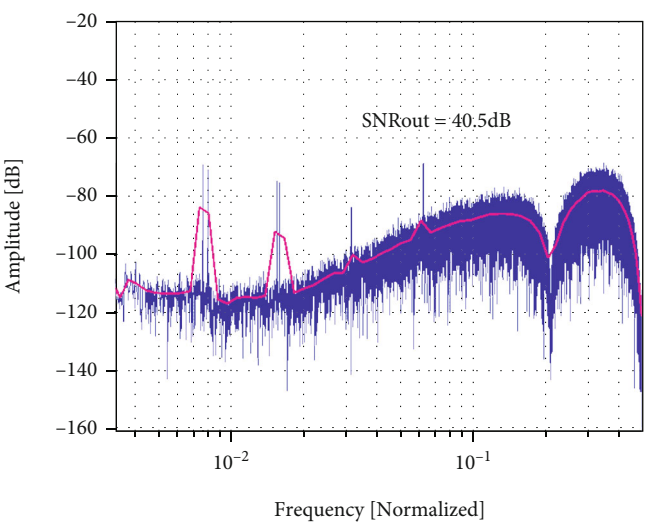

Figure 13: Out-of-band output spectrum of 1 kHz 0 dBFS input signal.

85.7 dB. Figure 13 shows the out-of-band output spectrum when the input signal is 1 kHz with 0 dBFS. It can be seen from the figure that the SNR_{out} is 40.5 dB. And the signal has two notches probably at fs/2 and 0.21 fs, which is consistent with the previous 4-tap FIR/IIR hybrid filter transfer function spectrum response results.

Table 2 summarizes the simulation performance of DSDAC. Due to the limitation of harmonics, the performance of the actual peak SNR is not ideal. A jitter can be added to DSM to avoid the interference of idle tones in subsequent experiments [2, 3].

The chip is based on 55 nm CMOS technology. The digital and analog parts are powered by 1.2 V and 2.5 V, respectively. Finally, DSDAC is integrated into SoC (System on Chip), and the AXI-Lite bus is used for interactive control.

Table 2: DSDAC performance summary.

	This work	[2]	[3]
Types of results	Postlayout simulation	Experiment	Experiment
Process	55 nm	0.13 μm	0.35 μm
Supply (V)	1.2*/2.5**	1.2*/3.3**	0.8
Power (mW)	1.5**	14.5	2.6
Output swing	0.48 Vpp	0.9 Vrms	0.56 Vpp
SNR (dB)	66.7	88	69
DR (dB)	85.7	97	88
SNR_{out} (dB)	40.5	39	—
Area (mm^2)	0.05*/0.03**	0.44	3.52***

*Digital part; **analog part; ***including a headphone driver.

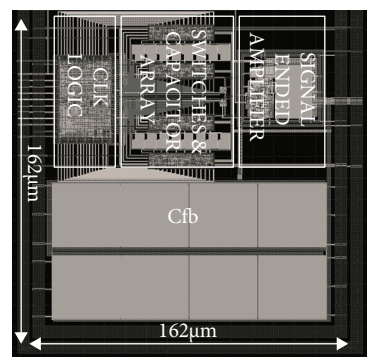

Figure 14: Analog part layout.

Figure 14 shows the layout of the analog part. The total area of the analog part is 160 μm × 160 μm.

3. Conclusions

Considering the endurance and integration of applications such as smart grids and portable electronic devices, this article designs and implements a small-area, low-power $\Delta\Sigma$ DAC. In terms of small area, we focus on the digital front-end part, using a three-level cascade HBF and an optimized sturdy MASH structure for the DSM; in terms of low power consumption, the main optimization of the analog reconstruction part is to use SC DAC and 4-tap FIR/IIR hybrid postfiltering. It not only improves the SNR_{out} but also reduces power consumption. The analog area is only 0.08 mm^2 in the 55 nm CMOS process. Circuit simulation shows that DR is 85.7 dB, the SNR_{out} is 40.5 dB, and the analog power consumption is 1.5 mW. It is suitable for high-efficiency and low-cost information transmission systems in the power field.

Data Availability

The raw/processed data required to reproduce the results obtained in this study cannot be shared at this time because they are used in an ongoing study.

Conflicts of Interest

The authors declare no conflict of interest.

Acknowledgments

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Research Article

A Power Management IC Used for Monitoring and Protection of Li-Ion Battery Packs

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A power management system is a critical component of the system which needs Li-ion battery packs for power supply. This paper proposes a fully integrated, high-precision, and high-reliability Integrated Circuit (IC) for the power management system of Li-ion battery packs. It has full protection circuits including overvoltage, overtemperature, and overcurrent circuits with measuring voltage accuracy of 0.2 mV and a 15-bit internal Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). This IC is designed to protect the system automatically and measure the battery cells' voltage, temperature, and charging or discharging current with high precision. It also provides an I^2C interface to communicate with an external Microcontroller Unit (MCU), making it achievable to perform battery cells' voltage balancing and SOC estimation with 0.1% estimation accuracy in an hour.

1. Introduction

To ensure efficient and secure operation of the system with Li-ion battery packs, a system which can intelligently monitor and protect the battery system in real time is necessary [1]. As battery manufacturing technology matures, a battery's volume and voltage are getting increasingly precise, which asks a much more precise and stable management system. Also, for the large equipment, the Li-ion battery pack always contains a huge number of cells, meaning that the system must have high voltage tolerance. The requirements including higher precision, higher stability, and higher voltage tolerance put forward a great challenge for the design of power management system IC. There are many relevant ICs available nowadays [2]. However, these ICs are generally too expensive and can hardly meet all the possible requirements, such as high precision, high stability, high voltage tolerance, and high integration level. For example, [3] presents an IC which has a 16-bit delta-sigma ADC, achieving 2.2 mV total measurement accuracy. [4] presents an IC which can also achieve highly accurate cell voltage measurements. These products cannot drive the power MOSFET, which means they cannot cut off the charging or discharging path without extra devices. Thus, when an abnormal condition occurs, they need the external MCU to perform protection actions, which makes the application circuit much more complicated. Some other modern products also have some deficiencies.

In this paper, a fully integrated, high-reliability, and high-precision power management system IC for the electric system with Li-ion battery packs is proposed. It contains protection circuits, internal Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC), power MOSFETs' driving circuit, and I^2C interface. The IC can sample battery cells' voltage, temperature signals, and current's magnitude with 0.2 mV accuracy. It can also detect abnormal conditions including overvoltage, overtemperature, and charging or discharging overcurrent. Besides, the IC can drive the power MOSFETs in the charging and discharging path, thus controlling whether the system is connected to

the charger or the load. With the I^2C interface, this IC can work with external MCU, achieving functions like cell balancing and SOC estimation.

This paper is divided into six sections. Section 2 provides an overview of the IC's architecture. Sections 3 demonstrates some considerations in the design of high-precision sampling circuit to ensure the accuracy of controlling. Section 4 gives general descriptions of protection circuit design and the algorithms of the Li-ion battery pack management system with this IC in application. Section 5 provides some test results. Section 6 summarizes the IC's functions and innovations and gives the prospects.

We note that a shorter conference version of this paper appeared in Hao et al. [5]. Our initial conference paper focused on the protection and security of the system and did not address the detailed realization of the high-precision sampling of battery voltages and current amplitude. This manuscript addresses the realization of sampling methods using an internal high-precision SAR ADC and shows more experimental results.

The detailed performance specifications are shown in Table 1. The given numbers are default values, and users can choose other values by writing the registers.

2. Chip Architecture

The IC contains protection circuits, internal SAR ADC, power MOSFETs' driving circuit, and I^2C interface, as shown in Figure 1. It can be directly used in the power management systems, providing cell voltage input and power MOSFET drive output. It also has some other signal input pins like external temperature sampling, wake-up sensor, and output pins like cell balance control output CBN. Figure 2 shows the diagram of the complete IC. The IC is designed to monitor series connected cells with high voltage tolerance. All the battery cells are connected to the input of level shifters inside the IC, so the voltage intervals at a high level will be shifted into an interval of 0~5 V. Then, these voltages are divided by two, turning into the voltage interval of 0~2.5 V. After the above operation, the obtained voltage can be directly processed by the ADC and some other internal circuits, such as overvoltage protection circuit. The IC has some other voltages to be detected, such as the voltage generated by an external thermistor and a fixed resistor, the voltage generated by an internal bipolar transistor, and the voltage generated by a detecting resistor connected in series in the charge and discharge path. These voltages are separately used to detect the external temperature, the internal temperature, and the charging or discharging current magnitude. The IC detects abnormal conditions using these voltages and responds rapidly, thus ensuring the safety of the whole system in operation. The IC contains a 15-bit SAR ADC, which can operate self-calibration when the IC powers on. Cooperating with a multiplexer, this internal SAR ADC can choose the certain signal channel to monitor cell voltages, current magnitudes, and external or internal temperature. MCU obtains data from this IC and uses this to perform required algorithms. In order to guarantee the balance of the battery pack and extend the battery's life, balancing circuitry is designed to perform passive cell voltage balancing, as shown in Figure 3. Besides, the IC has some digital blocks, including cell balancing control logic, power MOSFET control logic, registers, and abnormal conditions detecting logic including overcurrent, overvoltage, and overtemperature. Most modules of the IC are powered by a 5 V voltage generated inside by LDO, while a 12 V voltage is generated to drive the power MOSFETs which control the ON-OFF of the charging and discharging path. The 3.3 V DC regulator output RGO and RGC are connected to an external power device to supply for MCU, thus making the MCU's current drawn from battery cells instead of this IC.

3. Signal Sampling Circuit Design

There are various voltage signals in which users may want to obtain. Thus, the ADC's input must have the ability to switch among these different voltage signal channels. As shown in Figure 1, different voltages can be chosen by a multiplexer, which is controlled by the I^2C interface. When a certain voltage is selected to perform analog-digital conversion, the ADC is activated. After conversion is finished, the ADC's digital output is read by the I^2C interface, and a multiplexer selects the next voltage signal automatically to start the next conversion cycle, thus achieving continuous conversion of all the voltage signals. There are three types of signals which need to be converted: battery cells' voltage, charging and discharging current, and temperature.

3.1. Battery Cells' Voltage Sampling. As shown in Figure 4, the Nth battery cell is taken as an example. The voltage of this cell's anode is $V_{\text{cell}}(N)$, and the voltage of this cell's cathode is equal to the anode of the next cell $N-1$, which is $V_{\text{cell}}(N-1)$. An op-amp is used to make $V_X = V_{\text{cell}}(N-1)$, thus generating a current in $2R$:

$$I = \frac{V_{\text{cell}}(N) - V_{\text{cell}}(N-1)}{2R}. \tag{1}$$

This current flows in the resistor "R," generating a voltage which represents the battery cell "N" voltage:

$$V(N) = I \cdot R = \frac{V_{\text{cell}}(N) - V_{\text{cell}}(N-1)}{2}. \tag{2}$$

The input range of the ADC is 0~2.5 V, but the voltage of battery cells is usually around 4 V. As mentioned before, cell voltages must be divided by two before being connected to the input of ADC. The voltage $V(N)$ can be converted directly by the internal SAR ADC.

However, these operational amplifiers used in the sampling circuit will extract a current I_b from battery cells.

If there are 16 cells in total, when sampling the 16th battery cell's voltage, considering that the op-amp in Figure 4 uses NMOS as input pairs, it takes $V_{\text{cell}}(15)$ as the power net and $V_{\text{cell}}(14)$ as the ground net. As shown in Figure 5, every battery cell is connected to the IC. However, parasitic resistance exists in every net. Considering the 14th cell's anode, there is a current I_b extracted from the 15th cell's

Table 1: Detailed design target.

Design target	Default
Maximum battery cells	16
Total voltage range	0~85 V
Overvoltage threshold	4.25 V
Overcurrent threshold	1.25 V (500 mΩ sensing resistor recommended)
Protection time out	200 μs

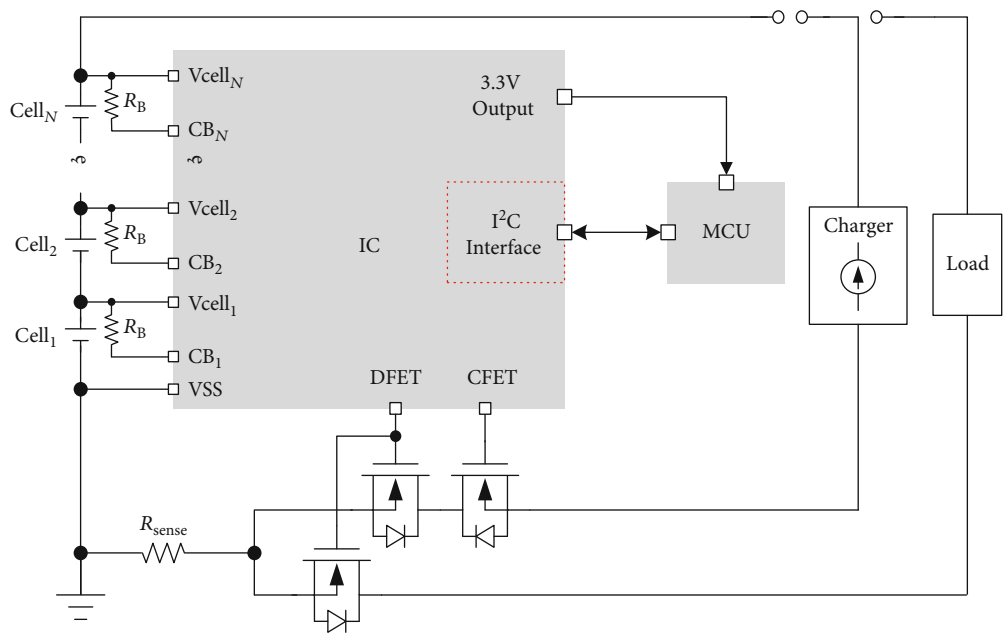

Figure 1: Diagram of the Li-ion battery pack management system.

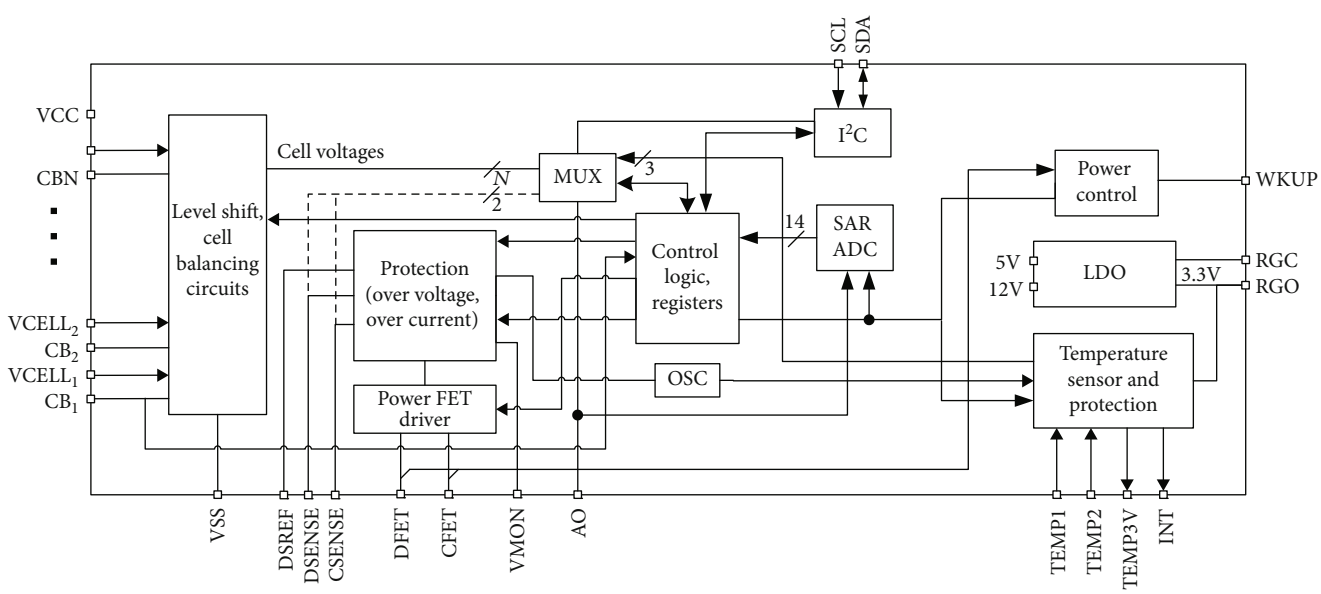

Figure 2: Diagram of the complete IC for the Li-ion battery management system.

sampling op-amp and a current I_b injected by the 16th cell's sampling op-amp, which can almost counterbalance. Yet, considering the 15th cell's anode, there is only a current extracted by the 16th cell's sampling op-amp. As shown by the black arrows in Figure 5, cell 1~cell 14's anode is extracted and injected a current I_b simultaneously, which

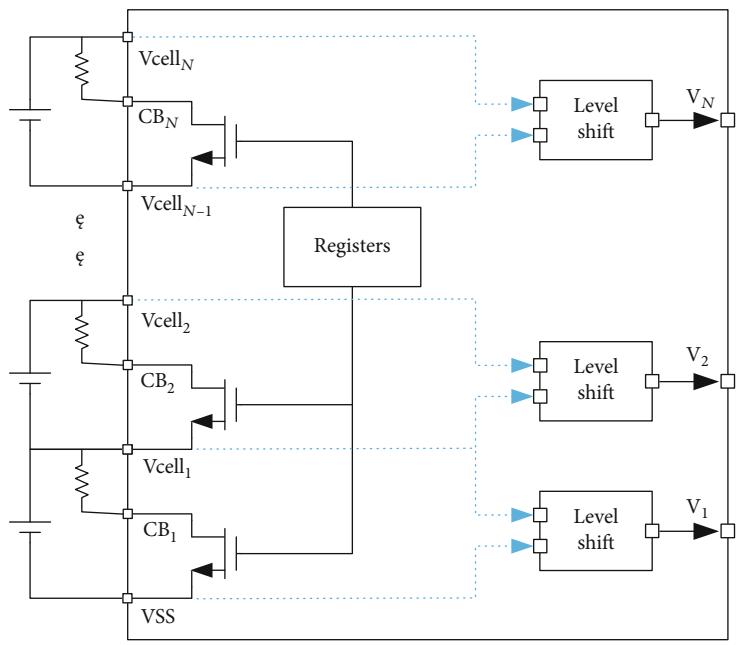

Figure 3: Cell balancing and batteries' voltage level shift circuits.

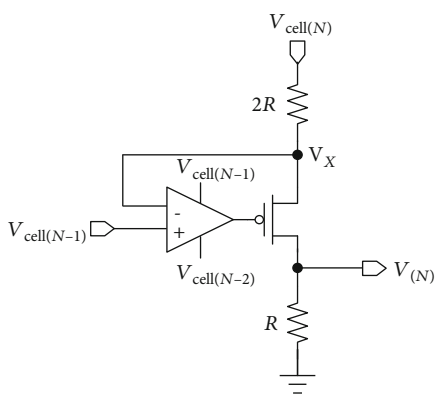

Figure 4: Battery cell voltage sampling circuit.

means that there is no actual current flowing from this node. Therefore, parasitic resistor R_P will not have an effect on the sampling accuracy. However, cell 15's anode has a current I_b flowing from it, generating a voltage drop $I_b R_P$ in this parasitic resistor, which makes the sampling of cell 15 and cell 16 not accurate. In order to cancel this current, a dummy op-amp is added, as shown in Figure 6. Using these methods, the current consumed by those op-amps in sampling circuits will not affect the precision of battery cells' voltage sampling.

3.2. Charging and Discharging Current Sampling. As shown in Figure 7, a sensing resistor R_{sense} is put in the charging and discharging path. When charger or load is connected to the battery pack, there is a current flowing through the resistor, generating a voltage which can be sampled by the IC's pin "current sense." This voltage signal can be selected to the internal SAR ADC and be converted, and the digital code of current amplitude is obtained. The R_{sense} is normally set as 500 mΩ. With 0.2 mV ADC resolution, the effective current sensing accuracy can be 0.4 mA.

3.3. Temperature Sampling. A constant current generated by a bandgap flows through a diode-connected PNP bipolar transistor. Since the base-emitter voltage has a negative temperature coefficient, we can use this V_{be} to detect internal temperature. As shown in Figure 8, a bipolar transistor's base-emitter voltage is directly connected to a comparator, which can output a warning flag when internal temperature is higher than the set threshold for a certain time. In addition, this V_{be} can also be selected to the input of internal SAR ADC to be converted, and a digital output of internal temperature can be obtained.

Furthermore, this IC has inputs prepared to detect external temperature. Users can connect a thermal resistor with a constant resistor to generate a voltage which represents the external temperature.

3.4. 15-Bit Self-Calibrated SAR ADC. In modern application, high-precision control becomes increasingly important. Therefore, it is necessary that the IC provides an internal analog-to-digital converter to detect required signal. Some previous works [2] provide several integrated parallel ADCs so that the measurements can be synchronized. The measurements can be faster in this way, but it occupies too much area of the IC. In this work, therefore, a communal SAR ADC is provided to detect all the voltages in sequence.

The reference voltage of ADC is 2.5 V, which means that the ADC needs to achieve a resolution of 0.2 mV/2.5 V = 1/12500 at least. It is true that a 14-bit SAR ADC can already achieve a resolution of $1/2^{14} = 1/16384$. However, considering the deviation between simulation and tests, a 15-bit SAR ADC is selected. The structure of 15-bit SAR ADC is shown in Figure 9. The actual circuit of SAR ADC has

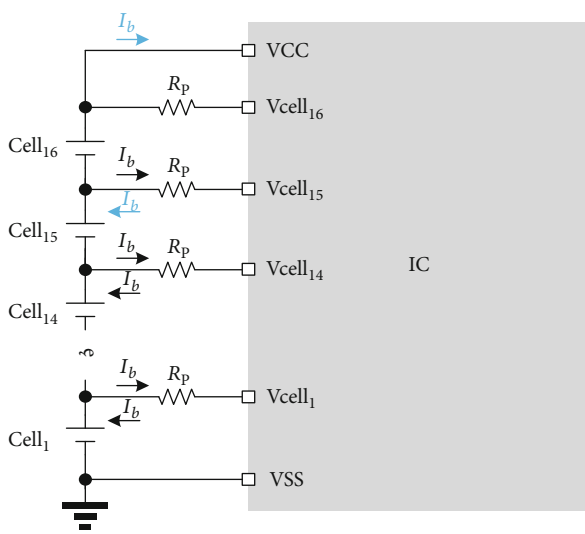

Figure 5: Current extracted by the amplifiers in the sampling circuit.

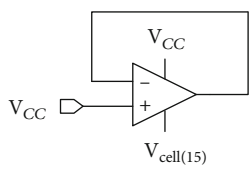

Figure 6: Dummy op-amp.

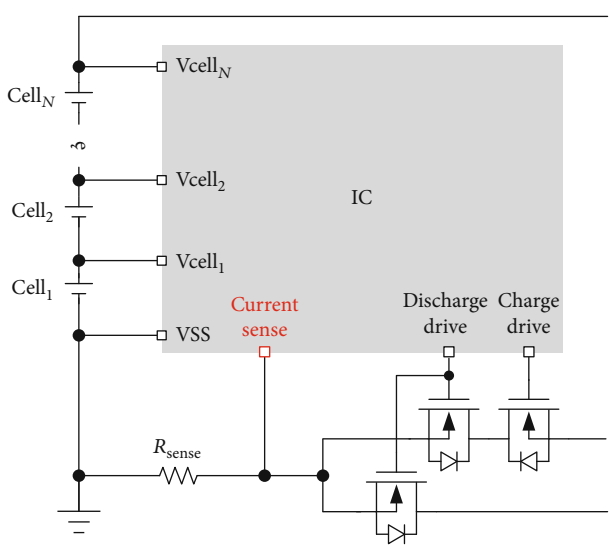

Figure 7: Current sampling circuit.

differential structure. For the convenience of description, this paper only gives the demonstration of a single side. In the practice of the battery management system, it is possible that negative voltage needs to be measured. For example, charging current is detected by a sampling resistor. Under this circumstance, the current flows from the negative electrode of the battery cell. One side of the sampling resistor is connected to the negative electrode of the lowest battery, and the voltage of another end is used to calculate the current. Therefore, a negative voltage needs to be converted. Under this circumstance, an extra capacitor is connected in shunt with the capacitor array, whose value is half of the capacitor of MSB. During the tracking mode, a lower plate of the extra capacitor is connected to ground and is switched to V_{REF} once ADC enters holding mode. Since the voltage at the positive input of the comparator is equal between the beginning and the end of the hold mode, the electric charge contributed by the extra capacitor will make the detected voltage higher than the real value by $1/4V_{REF}$. Thus, when processing negative voltage, the ADC will perform the above operation and obtain a digital code whose corresponding value equals the original voltage plus $1/4V_{REF}$. Through this method, the largest charging current $I_{Charge,max}$ that the IC can handle is $1/(4V_{REF}R_{sense})$. With a 500 mΩ sensing resistor, $I_{Charge,max}$ is 1.25 A. In practice, users can use a smaller sensing resistor to support a larger charging current.

In order to achieve the goal of high precision, a self-calibration algorithm is proposed, realized by an auxiliary 13-bit capacitor array shown in Figure 9. This auxiliary capacitor array can be used to calibrate the input offset voltage of a comparator and mismatches of capacitors in the main array. The calibration process is completed automatically when ADC powers on. First, during the calibration of input offset voltage of a comparator, the bottom plate of the main capacitor array is connected to a constant voltage, and the auxiliary array samples a 0 V differential input voltage to operate a SAR conversion, thus achieving a 13-bit digital output, which can represent the input offset voltage of a comparator. Second, during the calibration of the capacitors' mismatch, what is wanted to obtain is the error of every bit's actual weight w_i and its ideal weight. However, the ideal weight of the ith bit can be seen as 2^{i-1}, which is theoretical and cannot be represented in the practical circuit. In practice, the deviation of the ith bit's w_i weight and the sum of those lower bits' weight $\sum_{j=1}^{i-1} w_j$ are obtained first; then, the error code is calculated by an iteration algorithm. All the calibration code is stored in internal registers. During conversion, these codes are read in real time, controlling the auxiliary array to operate correspondingly to calibrate the error charge of the main array. Hence, the internal SAR ADC can achieve a high resolution.

4. Other Circuits and Designed Algorithms

4.1. Protection Circuit Design. Another highly significant function of a power management system is protection. In this work, the IC can detect different abnormal conditions and respond correspondingly. Possible abnormal conditions include the following: charging or discharging overcurrent, battery cells' overvoltage, and internal and external overtemperature. Protection circuitry is shown in Figure 10. For example, during charging operation, if the IC detects that discharging current magnitude exceeds the set threshold for a time long enough, it can be considered that the discharging overcurrent occurs. Consequently, the IC will shut down the discharging MOSFET to cut off the discharging path.

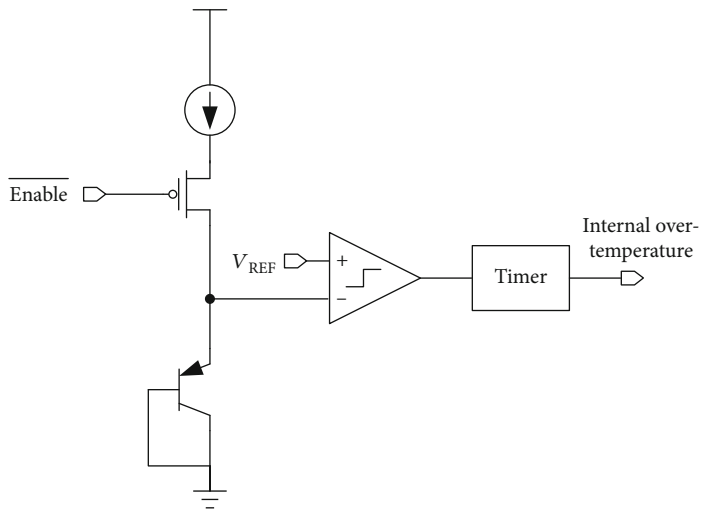

Figure 8: Internal temperature sampling circuit.

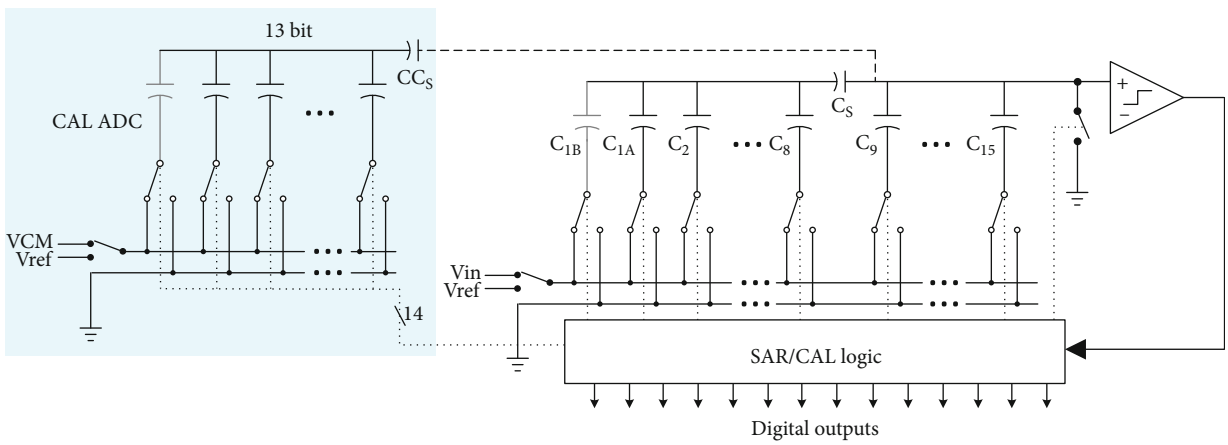

Figure 9: Internal 15-bit self-calibrated SAR ADC.

The delay time (±10% accuracy) and judgement voltage thresholds (0.2 mV accuracy) of every abnormal condition can be adjusted through the I^2C interface. Those circuitries to provide the reference clock and reference voltage are trimmed, thus guaranteeing the accuracy of delay time and threshold voltage.

As shown in Figure 10, there are two back-to-back N-MOSFETs in the charging path and a single MOSFET in the discharging path. The back-to-back N-MOSFETs are necessary. If there is only one FET in the charging path, as shown in Figure 11, when the voltage of battery cells V_{Battery} is lower than the charger's voltage V_{Charger}, the voltage of FET's source is $V_{\text{Battery}} - V_{\text{Charger}}$, which is negative. Then, the FET cannot be turned off even if the gate's voltage "CFET" is set to zero.

On the contrary, in Figure 10, the pin DFET controls M1 and M2, while CFET controls M3. DFET can provide both the pull-up and pull-down capability, while CFET can only provide pull-up capability. Thus, when a user needs to cut off both the charging and discharging paths, CFET is set to ground, which means that the gate to source voltage V_{GS} of M1 and M2 is zero. Since the CFET has no pull-down capability, it is disconnected from M3, making the V_{GS} of M3 discharged form R_g. Even if the voltage of M3's source is negative, the V_{GS} of M3 can still be discharged to zero. This guarantees reliable cut-off of the charging and discharging path.

4.2. Cell Voltage Balancing. During the processing of the battery pack, due to variance of physical volume, internal impendence, and thermal situation, the individual cells' voltages may drift apart over time [6]. Without the function of cell balancing, some battery cells' voltage can be higher than others; thus, there can be a situation where some cells are already fully charged or even over charged, while others are still not fully charged. However, the charger will be cut off only if all the cells are fully charged, which means that some cells will be charged continuously after being fully charged, which can cause an irreversible damage to a Li-on battery. As a result, the algorithm of battery cells' balancing is introduced, which maximizes the effective energy stored in the battery pack and extends the battery's life.

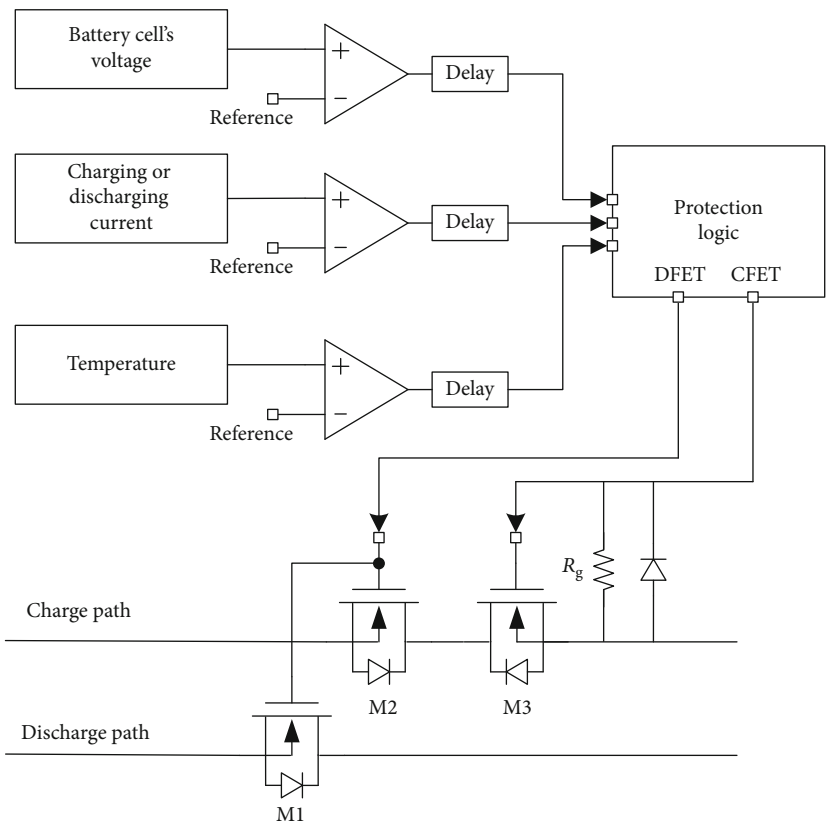

Figure 10: Protection circuit diagram of battery cells' voltage, charging and discharging current, and temperature.

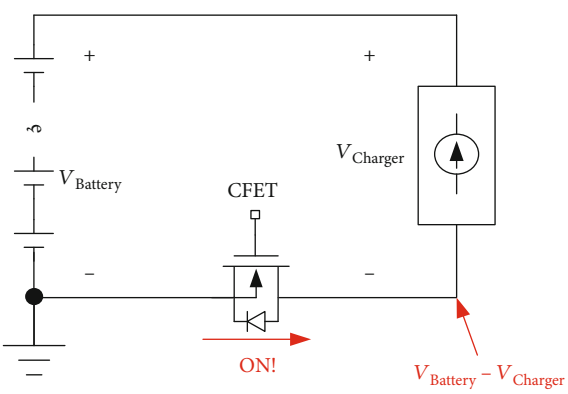

Figure 11: The simplified circuit if one FET is applied in the charging path.

In this work, the IC controls an external dissipative shunting resistor to consume the energy of those battery cells whose voltages are too high. Firstly, the IC gets the magnitude of all the battery cells' voltages from SAR ADC: $V_n = \{V_1, V_2, \cdots, V_N\}$. Then, the maximum value V_{max} and minimum value V_{min} are picked out. If the value of $V_{max} - V_{min}$ is bigger than the set threshold (100 mV), the battery pack can be considered scrapped. Otherwise, for four battery cells with the highest voltage, the corresponding CBN pins output high level to turn on the MOSFET, which connects the external resistor to the specific cells. Thus, the resistor will consume extra energy from those cells whose voltages are higher. With the charging or discharging going on, after a period of time, the energy consumed by the external resistor can make those cells' voltages drop faster or increase more slowly, thus bringing all the cells back to balance by repeating the above step.

4.3. SOC Estimation. It is indispensable to estimate the available energy left in the battery pack accurately in the practical use, since the system's tolerance range is needed to make corresponding arrangements. The most widely used metrics to measure that is State of Charge (SOC), which is normally defined as the ratio of its current capacity $Q(t)$ to the nominal capacity Q_n [7]. Q_n represents the maximum charge which can be stored in the battery. Accordingly, SOC can be formulated as

$$\mathrm{SOC}(t) = \frac{Q(t)}{Q_n}. \tag{3}$$

4.3.1. Conventional Methods. The commonly used methods to estimate SOC include the following: Open Circuit Voltage (OCV) method, Coulomb counting method, internal impedance measurement method [8, 9], and intelligent algorithms, etc. [10]. The Coulomb counting method is easy to conduct, thus being widely embedded in BMS ICs. It suffers, however, from inaccurate initial SOC value and accumulated errors. Meanwhile, although the OCV method's algorithm is very simple, the accurate relationship between SOC and OCV remains difficult to measure. Besides, the intelligent

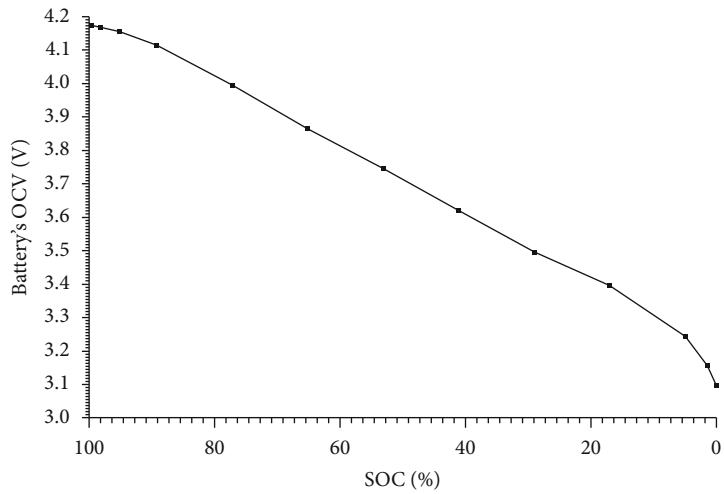

Figure 12: Test result curve of the battery's OCV vs. SOC.

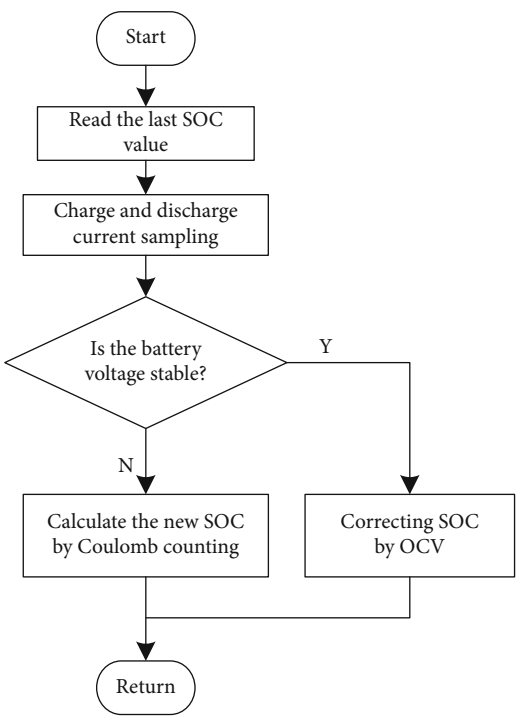

Figure 13: Flowchart of the SOC estimation algorithm.

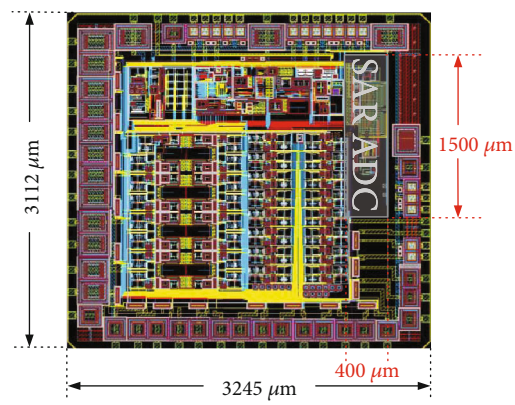

Figure 14: Layout of the complete IC.

algorithms include artificial neural networks, machine learning, etc. These intelligent algorithms need extensive test data and high-performance computing unit, which is not available in some applications.

(1) OCV Method. There is a relationship between SOC and OCV of a battery [10], which can be derived from experimental data. Taking the 18650 Li-ion battery as an example, we used a constant current source to charge it from empty to full. Every ten-minute charging must be followed with a rest time period of two hours, ensuring that the battery's voltage was stable. Repeat this operation until the battery is fully charged. The procedure is just the same in the discharging test. After multiple experiments and averaging, the relationship between SOC and OCV can be demonstrated in Figure 12 according to our test data. As a result, the value of SOC can be adjusted by curve fitting using premeasured data, with error not exceeding 0.1% in the experiment. However, the voltage across the battery is not necessarily equal to the actual OCV during operation; instead, it varies with the working current's variation. Also, the battery needs a long time to stabilize after charging or discharging operation, which can be an hour or even longer. As a consequence, the OCV method is inaccurate in most cases and cannot acquire data in real time.

(2) Coulomb Counting Method. If the battery's current is constant during a time period Δt, the change of $Q(t)$ can be calculated by

$$\Delta Q(t) = I \cdot \Delta t. \tag{4}$$

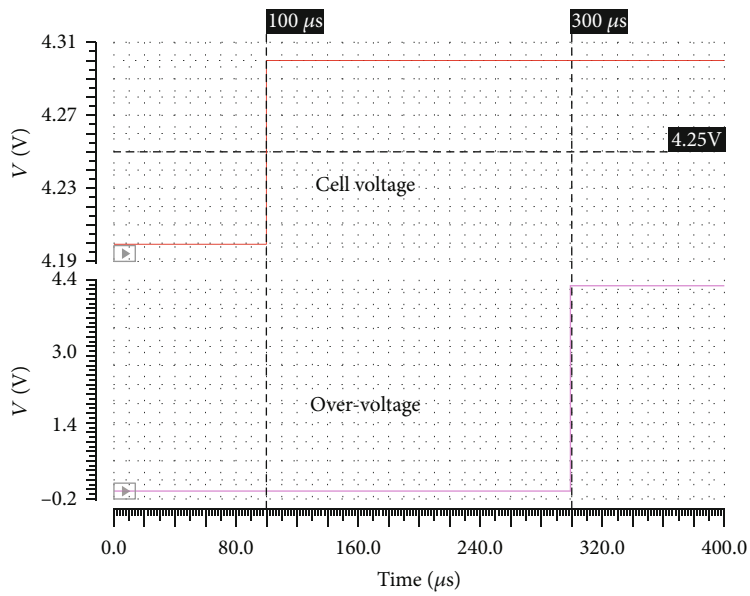

Figure 15: Waveform of battery cell overvoltage.

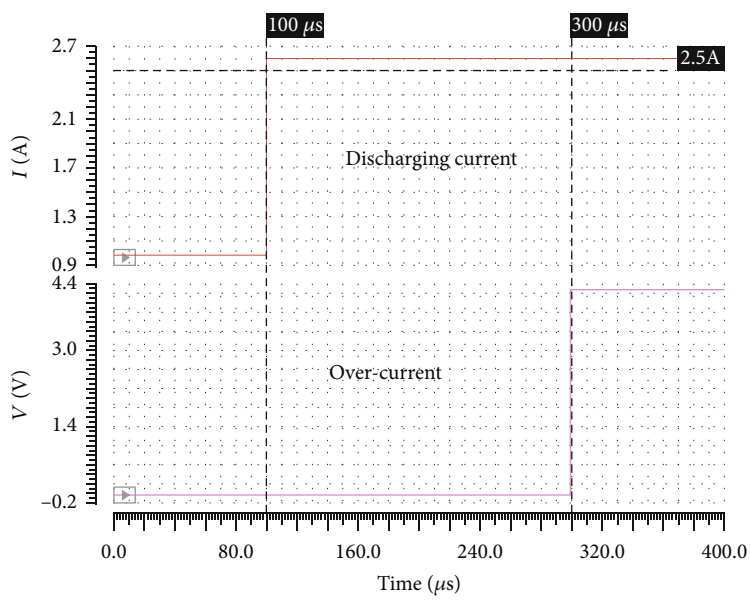

Figure 16: Waveform of discharging overcurrent.

Furthermore, (5) can be derived:

$$Q(t) = \int I\,dt. \tag{5}$$

This is the so-called Coulomb counting method.

In order to facilitate the algorithm's operation, the Coulomb counting method can be modified by the following equation:

$$\mathrm{SOC}(t) = \mathrm{SOC}(t-1) + \frac{I(t)}{Q_n} \cdot \Delta t. \tag{6}$$

In a word, during continuous operation of the battery system, current magnitude can be estimated periodically through ADC, which is used to update the SOC value regularly.

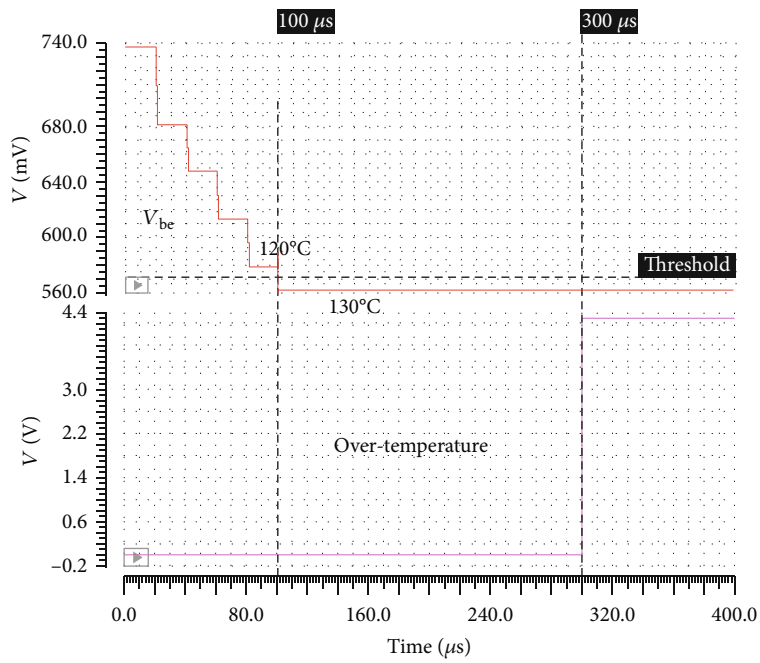

Figure 17: Waveform of overtemperature.

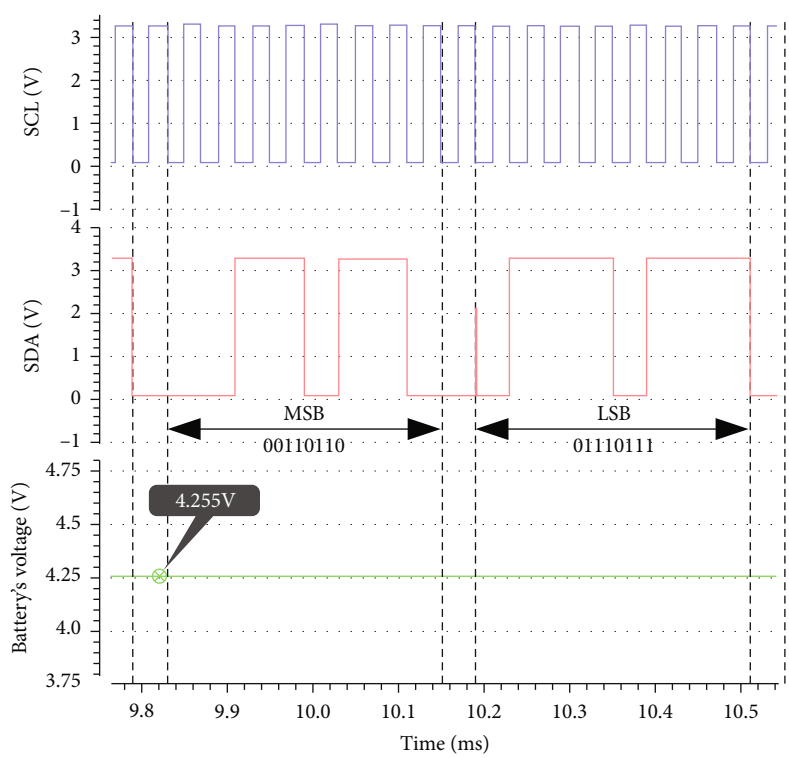

Figure 18: Waveform of I^2C when reading codes from ADC.

4.3.2. Proposed Method. In this work, OCV and Coulomb counting methods are synthesized, which combines the advantages of both methods. Therefore, this IC is able to estimate the SOC value in real time with high precision.

The magnitude of battery cells' voltage (OCV) is available directly through SAR ADC. At the same time, charging or discharging current magnitude used for Coulomb counting can be detected by a sampling resistor in the charging and discharging path. Voltage drop through the sampling resistor is processed by ADC to calculate the current's magnitude.

During operation, the IC reads the last SOC value at the beginning of each calculation cycle and updates the SOC

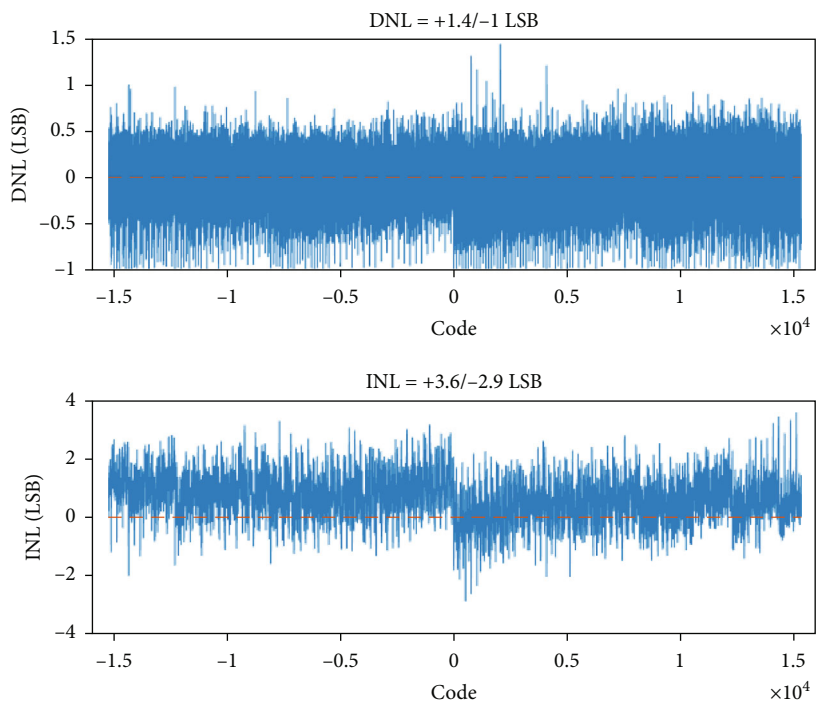

Figure 19: Static characteristics of ADC.

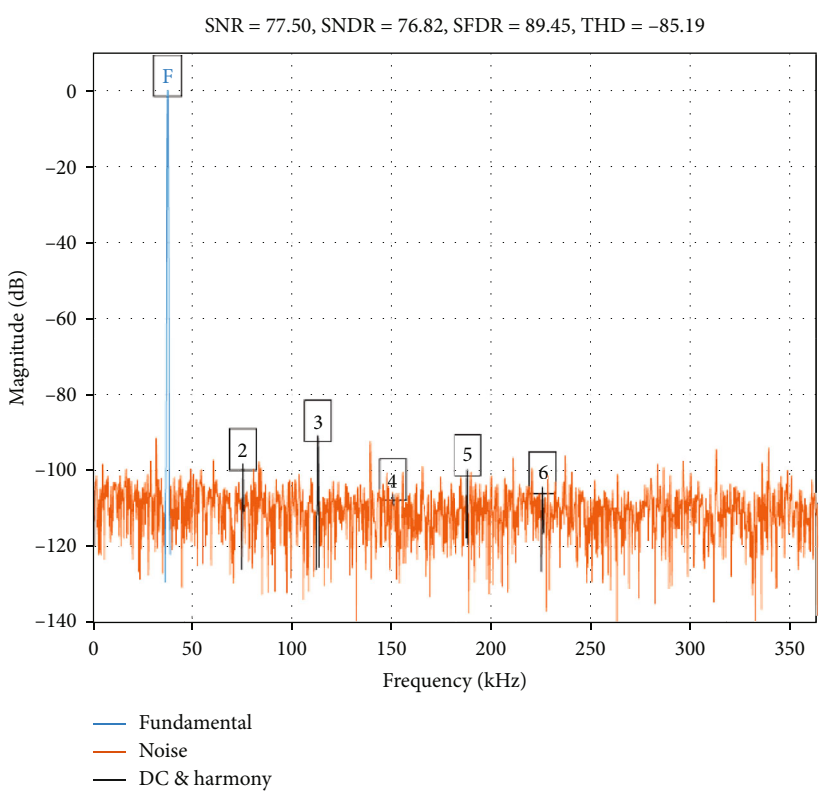

Figure 20: Dynamic characteristics of ADC.

value by the Coulomb counting method in real time. Besides, it can identify whether the system is working or not and has a time counter recording the period when the system is powered down. If this time is long enough, which presents that the batteries' terminal voltage is stable and nearly equal to OCV, the IC will adapt the OCV method to adjust the SOC

Table 2: Comparison of this work with previous ICs.

Property	This work	[3]	[4]
Quiescent current	800 μA*	950 μA	2 mA
ADC resolution	<0.2 mV	Total error < 2.2 mV	<1.1 mV
Comm.	No external components	External MOS drivers	External MOS drivers

*The quiescent current is estimated via simulations.

Table 3: Breakdown of the quiescent current.

Module	Quiescent current
SAR ADC	310 μA
Reference	120 μA
Sampling circuit	260 μA
Others	110 μA

Table 4: Performance summary of the prototype.

Parameter	Value
Process	180 nm CMOS process
LDO 1 (for internal use)	5 V
LDO 2 (for internal use)	12 V
LDO 3 (for external use)	3.3 V
SAR ADC	15 bit
Sampling precision	0.21 mV
SOC precision	±0.1%/h
Protection functions	Overvoltage Overcurrent Overtemperature
Temperature range	-40°C~125°C*

*The temperature range is just for functionality.

value using curve fitting, based on obtained data shown in Figure 12. After being restarted, the IC carries on the Coulomb counting operation. Thus, the system can obtain accurate SOC value in real time and avoid cumulative error caused by Coulomb counting. However, the data in Figure 12 is just a reference. The relationship between SOC and OCV will vary with time going on. That is to say if an accurate SOC value is demanded, the curve of SOC and OCV must be adjusted according to using time and environment. In order to verify this method by experiment, we selected an existing ADC chip with 15-bit accuracy to build a testing system. The OCV is tested using the same way in which the curve of the battery's OCV vs. SOC is obtained, and current is also detected to calculate the SOC value. By comparing the results of several experiments, the total estimation error will not exceed 0.1% within an hour. The algorithm's flowchart is shown in Figure 13.

5. Results

The IC was designed in a 0.18 μm Bi-CMOS process: "DongBu-181aBD18BA," and the layout is shown in Figure 14. This IC's size is 3245μm × 3112μm.

The IC's overall functions are only verified by postsimulation. Postsimulation results demonstrate that the IC can detect all the abnormal situations and respond rapidly, generally by turning off the corresponding charging or discharging MOSFET. For example, the overvoltage time delay is set to 200 μs, and the cell's voltage exceeds the threshold of 4.25 V at 100 μs. Then, at 300 μs, the overvoltage warning bit is set high; meanwhile, the IC automatically cuts off the discharging path, as shown in Figure 15. Similarly, the discharging current exceeds the threshold of 2.5 A at 100 μs; then, at 300 μs, the overcurrent warning bit is set high, as shown in Figure 16.

Make the temperature vary with time, as shown in Figure 17. The overtemperature time delay is also set to 200 μs. When the temperature exceeds the threshold 125°C for 200 μs, the overtemperature indicator is set high and the IC will cut off the charging and discharging path.

Figure 18 shows the result when the IC chooses a battery's voltage of 4.255 V to perform analog-to-digital conversion and reads the obtained code from it. Considering the reference voltage of 2.5 V of ADC, the obtained digital result is 2.1275 V. This value is half of the chosen battery cell's voltage, indicating that it represents the actual magnitude of 4.255 V. The accuracy of ADC is verified.

The proposed self-calibrated SAR ADC has been fabricated and tested separately. The static characteristics and dynamic characteristics are given in Figures 19 and 20. The DNL is -1 to 1.4 LSB, and the INL is -2.9 to 3.6 LSB. The dynamic characteristics are tested in the 720 KSPS sampling rate and 37 kHz input signal frequency. When input is half of the magnitude, SNDR is 76.82 dB, from which we can deduce that in full input magnitude, SNDR is 82.84 dB and ENOB (effective number of bits) is 13.5 bit.

Table 2 provides a comparison of this work with similar ICs from industry. Table 3 provides the breakdown of the quiescent current. Table 4 provides a general summary of this work.

6. Conclusion and Prospect

In summary, a complete power management system IC with full integration, high precision, and high reliability for a battery pack which can monitor and protect the system is demonstrated, achieving lower application costs. The IC protects the battery from overvoltage, overcurrent, and overtemperature when charging and discharging with 0.2 mV discrimination accuracy. With a SAR ADC integrated, the IC can get precise magnitude of each battery cell's voltage, the internal or external temperature, and charging or discharging current with 0.2 mV voltage accuracy. The IC works with an external

MCU, being able to perform battery cell voltages' balancing and to help users to get the SOC value with 0.1% estimation accuracy. After verification, the IC ensures safe operation of the system with the Li-ion battery pack. In following work, the MCU will be integrated with an analog front end, making it a fully integrated power management IC with intelligent self-control for the Li-ion battery pack.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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Research Article

Hardware Decoding Accelerator of (73, 37, 13) QR Code for Power Line Carrier in UPIoT

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The proposal of the ubiquitous power Internet of Things (UPIoT) has increased the demand for communication coverage and data collection of smart grid; the quantity and quality of communication networks are facing greater challenges. This brief applies (73, 37, 13) quadratic residue (QR) codes to power line carrier technology to improve the quality of local data communication in UPIoT. In order to improve the decoding performance of the QR codes, an induction method for the error pattern is proposed, which can divide the originally coupled error pattern into six parts and reuse the same module for decoding. This method greatly reduces the resource requirements, so that (73, 37, 13) QR code can be implemented on FPGA hardware. Notably, the hardware architecture is a modular framework, which can fit into an FPGA with different sizes. As an example (73, 37, 13), QR code is implemented on Intel Arria10 FPGA; the experimental result shows that the maximum decoding frequency of this architecture is 21.7 M Hz, which achieves 4121x speedup compared to CPU. Moreover, the proposed architecture benefits from high flexibility, such as modular design and decoding framework in the form of the pipeline which can be seen as an alternative scheme for decoding long-length QR codes.

1. Introduction

With the development of power systems, the types and quantities of electrical equipment are increasing rapidly, for example, Energy Storage (ES) is being widely adopted in the grid to meet the needs of intermittent power generation [1]. This brings a growing demand for information sharing [2] and analysing [3] between all nodes in the power grid system. Ubiquitous power Internet of Things (UPIoT) is proposed as an advanced technology in the construction of smart grids. It can integrate the combination of the Internet of Things (IoT) and the power business, efficiently integrate IoT and power system, and improve the information transparency of the power system. The "Ubiquitous" of UPIoT is embodied in the various nodes of the power system (transmission, transformation, distribution, and consumption), that means the real-time interconnection of people, machinery, power networks, and platforms can be achieved at any time [4].

UPIoT is proposed based on IoT, so it has a structure similar to the traditional IoT, including perception layer, network layer, platform layer, and application layer [5]. The perception layer is composed of sensors with different functions in each link and node of the power network. The network layer is mainly composed of the internet or the dedicated network, which is responsible for a large amount of information transmission. The platform layer is the data sharing and publishing center. The application layer provides users with data display and control signal transmission function. It is recognized that UPIoT mainly includes three parts [6] of communication, local communication, edge IoT gateway, and remote communication. As an intermediate carrier between the perception layer and the platform layer, the edge IoT gateway assumes the function of gathering data and the local edge fast computing. The remote network is usually implemented by 4G/5G and dedicated networks, while the local communication network can choose wired or microwave wireless networks due

to its short distance. The types and quantities of data measured by local sensors in UPIoT will increase greatly with the development of power networks. Therefore, the local transmission network should have the following characteristics:

(i) Two-way real-time communication capability

(ii) Low power consumption and low cost

(iii) Strong data compatibility

Power line carrier communication (PLC) technology, as a local communication technology, can carry both power and data and has been widely used for high-speed data transmission, even in relatively remote areas [7]. The good characteristics of PLC, such as direct application of power line transmission data, no need to modify the wiring layout, easy implementation, and two-way communication, can meet the basic characteristics of the local transmission network. However, using power carrier line leads to a relatively large attenuation of carrier signal, and the damage to performance from multiple noises is still a challenge. In order to deal with the shortcomings, some researches have proposed Reed-Solomon (RS), Low Density Parity Check (LDPC) [8, 9], Convolution Code (CC), and other advanced codes [10, 11]. In addition, using modulation techniques such as Quadrature Frequency Shift keying (QFSK) and Orthogonal Frequency Division Multiplexing (OFDM) [12] can improve the reliability of the system.

The LDPC codes are selected as the channel coding schemes for the data channels in 5G new radios because of its excellent long code error correction performance. In local communication, most of the transmitted signals between the sensors and the IoT gateway are expected to be power status data and control signals, which can be regard as short data; the advantages of Low-Density Parity Check (LDPC) codes cannot reflect due to the dense and short communication data [8]. In recent years, with continuous development, the root-protograph (RP) LDPC code appeared to solve the interruption limitation of the BF channel due to its nontraversal characteristics [9]. The CC decoding has high computational complexity due to the Viterbi algorithm and the use of interleave causes significant end-to-end delay. Reed-Solomon (RS) codes, which are used in many PLCs, will cause a huge amount of calculation when the redundancy is large. Due to the insufficient error correction capability of the channel encoder, the performance of the receiver still cannot achieve satisfactory performance [10]. Therefore, we propose to use quadratic residue (QR) codes [13] to encode data and control signals in front of the PLC channel, and still can use more commonly used modulation methods such as OFDM; it can obtain the following advantages:

(i) The requirement of transmission power can be reduced in the same environment

(ii) Improve the reliability of communication and thereby improve communication efficiency

The QR code gains powerful error correction capabilities by increasing the complexity of decoding; although the QR code decoding algorithm has been improved several times, it is still difficult to make a stand out in practical applications due to its unsatisfactory decoding speed. Based on the existing decoding algorithm, difference syndrome (DS) algorithm [14], and optimized decoding algorithm cyclic weight (OCW) [15], we propose a method suitable for digital circuit hardware implementation, which is named as error pattern induction (EPI). By using EPI, we reduce the (73, 37, 13) QR code into 6 parts so that it can use same pipeline processor, and (73,37, 13) QR code can be realized on limited hardware resources. At the same time, we implemented the hardware decoding architecture of (73, 37, 13) QR code on the Intel Arria10 10AX115-U4F45I1SG FPGA platform, achieving a maximum clock frequency (fmax) of 260.42 MHz, which is equivalent to 21.7 MHz decoding frequency.

2. QR Code and Decoding Algorithm

The QR code was proposed by E. Prange in 1958 and has excellent error detection and correction capability due to its large minimum Hamming distance [3]. The QR code is defined on the finite field $GF(2^m)$, and $GF(2^m)$ is a finite field containing 2^m elements. The (73, 37, 13) QR code is constructed over $GF(2^9)$, and its quadratic residue set is given by

$$Q_{73} = \left\{ l \mid l \equiv x^2 \mod 73, 1 \le x \le \left[\frac{73}{2}\right] \right\},$$
$$= \left\{ \begin{array}{c} 1, 2, 3, 4, 6, 8, 9, 12, 16, 18, 19, 23, 24, 25, \\ 27, 32, 35, 36, 37, 38, 41, 46, 48, 49, 50, \\ 54, 55, 57, 61, 64, 65, 67, 69, 70, 71, 72 \end{array} \right\}. \quad (1)$$

Let m be the smallest positive integer which makes $(2^m \mod n) = 1$, and for (73, 37, 13) QR code, $m = 9$. Let $\alpha \in GF(2^9)$ be a root of the primitive polynomial $p(x) = x^9 + x^4 + 1$, then α generates all nonzero elements in the finite field $GF(2^9)$. Obviously, $(2^9 - 1)/73 = 7$, so $\beta = \alpha^7$ is the 73rd root of unity in $GF(2^9)$, and the generator polynomial of the (73, 37, 13) QR code is given by

$$\begin{aligned} g(x) = \prod_{i \in Q_{73}} \left(x - \beta^i\right) &= x^{36} + x^{34} + x^{32} + x^{31} \\ &+ x^{30} + x^{28} + x^{25} + x^{24} + x^{22} + x^{21} + x^{20} \\ &+ x^{19} + x^{18} + x^{17} + x^{16} + x^{15} + x^{14} + x^{12} \\ &+ x^{11} + x^8 + x^6 + x^5 + x^4 + x^2 + x + 1. \end{aligned} \quad (2)$$

The message part of the (73, 37, 13) QR code is a vector of length 37 and can be expressed by a polynomial as $m(x) = \sum_{i=0}^{36} m_i x^i$. Then, the codeword can be expressed as

$$c(x) = m(x) \cdot x^{36} + m(x) \cdot x^{36} \bmod g(x) = \sum_{i=0}^{72} c_i x^i, \quad (3)$$

by using systematic coding, where high 37 bits are message bits, expressed as $m(x) \cdot x^{36}$, and lower 36 bits are parity bits, expressed as $m(x) \cdot x^{36} \bmod g(x)$. If the codeword is passed

through an additive white Gaussian noise (AWGN) channel, the noise can be expressed as $e(x) = \sum_{i=0}^{72} e_i x^i$, then the received codeword can be expressed as

$$r(x) = c(x) + e(x) = \sum_{i=0}^{72} r_i x^i, \tag{4}$$

let $s(x) = r(x) \bmod g(x) = \sum_{i=0}^{35} s_i x^i$, and the $s(x)$ is called syndrome polynomial.

We will describe the decoding algorithms by integrating DS algorithm and OCW algorithm; of course, there are other decoding algorithms such as Berlekamp-Massey (BM) [16], Fast Algebraic Decoding Algorithm (ADA) [17], Syndrome and Syndrome Difference Decoding Algorithm (SSDDA) [18, 19], all of them are implemented in software.

For simplicity, split codeword r to a message part r_m and a parity part r_p, and split decoded codeword d_r to a message part dr_m and a parity part dr_p. Let e_i be an error in the ith bit of r_m, and the syndrome corresponds to e_i is expressed as s_i. The syndromes $s_i (0 \le i \le 36)$ is shown in Table 1.

For a received codeword r, the syndrome s_r of r is first calculated, then the weight $W(s_r)$ of the s_r is calculated, and the codeword can be decoded by the following steps.

Step 1. If $W(s_r) \le 6$, all errors of the received codeword r are in r_p. Then, the decoded message part $dr_m = r_m$, and the decoding is completed at this time. If $W(s_r) > 6$, there is at least one error existing in the message part r_m.

Step 2. Calculate $s_{ri} = s_r \wedge s_i (0 \le i \le 36)$ where '$\wedge$' means the bit operation XOR, and calculate the weight $W(s_{ri})$ of s_{ri}. If i exists in the range of $0 \le i \le 36$ such that $W(s_{ri}) \le 5$, there is only one error in r_m, and we can obtain the decoded message part $dr_m = r_m \wedge e_i$. Then, the decoding is completed at this time, and the calculation complexity of this step is C_{37}^1. If i does not exist such that $W(s_{ri} \le 5)$, there are at least two errors in the message part r_m.

Step 3. Calculate $s_{rij} = s_r \wedge s_i \wedge s_j (0 \le i < j \le 36)$, and calculate the weight $W(s_{rij})$ of s_{rij}. If i, j exist in the range of $0 \le i < j \le 36$ such that $W(s_{rij}) \le 4$, there are two errors in r_m, and we can obtain decoded message part $dr_m = r_m \wedge e_i \wedge e_j$. Then, the decoding is completed at this time, and the calculation complexity of this step is C_{37}^2. If i, j does not exist which makes $W(s_{rij} \le 4)$, there are at least three errors in r_m.

Step 4. Calculate $s_{rijk} = s_r \wedge s_i \wedge s_j \wedge s_k (0 \le i < j < k \le 36)$, and calculate the weight $W(s_{rijk})$ of s_{rijk}. If i, j, k exist in the range of $0 \le i < j < k \le 36$ such that $W(s_{rijk} \le 3)$, there are three errors in r_m, and we can obtain decoded message part $dr_m = r_m \wedge e_i \wedge e_j \wedge e_k$. Then, the decoding is completed at this time, and the calculation complexity of this step is c_{37}^3. If i, j, k does not exist which makes $W(s_{rijk} \le 3)$, there are at least four errors r_m.

Table 1: Syndromes and error patterns.

s_i	Error pattern
s_0	1000_1111_0010_0010_1110_1000_1001_1110_0011
s_1	1001_0001_0110_0111_0011_1001_1010_0010_0101
s_2	1010_1101_1110_1100_1001_1011_1101_1010_1001
s_3	1101_0100_1111_1011_1101_1111_0010_1011_0001
s_4	0010_0110_1101_0101_0101_0110_1100_1000_0001
s_5	0100_1101_1010_1010_1010_1101_1001_0000_0010
s_6	1001_1011_0101_0101_0101_1011_0010_0000_0100
s_7	1011_1001_1000_1000_0101_1110_1101_1110_1011
s_8	1111_1100_0011_0010_0101_0101_0010_0011_0101
s_9	0111_0111_0100_0110_0100_0010_1101_1000_1001
s_{10}	1110_1110_1000_1100_1000_0101_1011_0001_0010
s_{11}	0101_0010_0011_1011_1110_0011_1111_1100_0111
s_{12}	1010_0100_0111_0111_1100_0111_1111_1000_1110
s_{13}	1100_0111_1100_1101_0110_0111_0110_1111_1111
s_{14}	0000_0000_1011_1000_0010_0110_0100_0001_1101
s_{15}	0000_0001_0111_0000_0100_1100_1000_0011_1010
s_{16}	0000_0010_1110_0000_1001_1001_0000_0111_0100
s_{17}	0000_0101_1100_0001_0011_0010_0000_1110_1000
s_{18}	0000_1011_1000_0010_0110_0100_0001_1101_0000
s_{19}	0001_0111_0000_0100_1100_1000_0011_1010_0000
s_{20}	0010_1110_0000_1001_1001_0000_0111_0100_0000
s_{21}	0101_1100_0001_0011_0010_0000_1110_1000_0000
s_{22}	1011_1000_0010_0110_0100_0001_1101_0000_0000
s_{23}	1111_1111_0110_1110_0110_1011_0011_1110_0011
s_{24}	0111_0001_1111_1110_0011_1110_1110_0010_0101
s_{25}	1110_0011_1111_1100_0111_1101_1100_0100_1010
s_{26}	0100_1000_1101_1010_0001_0011_0001_0111_0111
s_{27}	1001_0001_1011_0100_0010_0110_0010_1110_1110
s_{28}	1010_1100_0100_1010_1010_0100_1100_0011_1111
s_{29}	1101_0111_1011_0111_1010_0001_0001_1001_1101
s_{30}	0010_0000_0100_1101_1010_1010_1010_1101_1001
s_{31}	0100_0000_1001_1011_0101_0101_0101_1011_0010
s_{32}	1000_0001_0011_0110_1010_1010_1011_0110_0100
s_{33}	1000_1101_0100_1111_1011_1101_1111_0010_1011
s_{34}	1001_0101_1011_1101_1001_0011_0111_1011_0101
s_{35}	1010_0100_0101_1001_1100_1110_0110_1000_1001
s_{36}	1100_0111_1001_0001_0111_0100_0100_1111_0001

Step 5. Cyclic shift r by 36 bits to left, the result of shifting is expressed as r'. Then, calculate the syndrome $s_r{}'$ of r', and calculate the weight $W(s_r{}')$ of $s_r{}'$. Repeat steps 1~4, then 4~6 errors in r_m can be correct. After these, the decoding is completed. We can infer that the total computational complexity of the DS algorithm is $(C_{37}^1 + C_{37}^2 + C_{37}^3) * 2$.

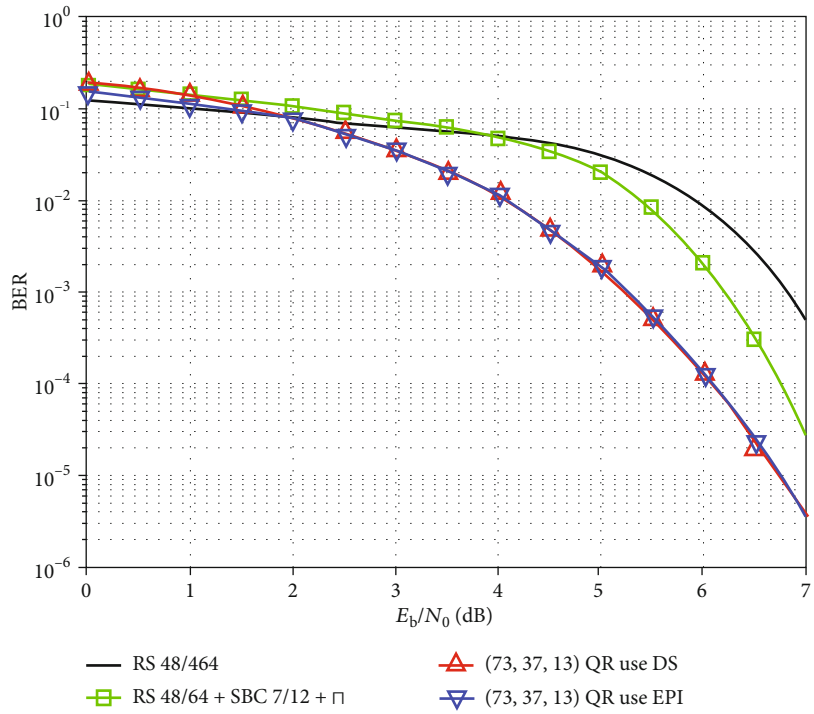


Figure 1: BER performance of the two RS codes, the (73, 37, 13) QR algorithm use DS algorithm in [10] and use EPI in this paper.

The simulation of QR code is indispensable, 37-bit random message is generated and encoded by (73, 37, 13) QR code. Then, calculate the decoding performance after mixing the encoded signal with Gaussian white noise. The simulation results of different bit error rate (BER) performance are shown in Figure 1. We also show the curves of the two RS codes in [20] and the EPI algorithm proposed in this paper. From Figure 1, we can see that QR codes have better performance than RS codes, and QR codes will also have better performance in practical applications. The specific EPI algorithm will be explained in Section 3.

3. Error Pattern Induction Method

In order to improve the decoding speed and ensure the controllability of the decoding time, it is necessary to calculate all the decoding possibilities, then the decoding could be completed within a fixed time. However, the long codeword length of (73, 37, 13) QR code leads to high decoding complexity, and decoding with a full parallel module will result in a great amount of resource consumption. This decoding framework summarizes the error patterns to implement module multiplexing based on DS algorithm; then, we can reduce resource consumption and hardware burden, and we can make it possible to implement in low-cost hardware.

3.1. Error Pattern Induction and Classification. Section 2 shows that when there are three errors in r_m, the decoding complexity is the highest, so we consider to optimize it firstly.

3.1.1. Three-Error Patterns. The number of three-error patterns is c_{37}^3, a total of 7770 kinds, which can be decomposed into several parts, and we call them as inductive error patterns; the inductive error patterns are shown in Table 2.

Table 2: Three-error inductive error patterns.

Inductive error patterns	Numbers
$e_0e_1e_n(2 \le n \le 35)$	34
$e_0e_2e_n(4 \le n \le 34)$	31
$e_0e_3e_n(6 \le n \le 33)$	28
$e_0e_4e_n(8 \le n \le 32)$	25
$e_0e_5e_n(10 \le n \le 31)$	22
$e_0e_6e_n(12 \le n \le 30)$	19
$e_0e_7e_n(14 \le n \le 29)$	16
$e_0e_8e_n(16 \le n \le 28)$	13
$e_0e_9e_n(18 \le n \le 27)$	10
$e_0e_{10}e_n(20 \le n \le 26)$	7
$e_0e_{11}e_n(22 \le n \le 25)$	4
$e_0e_{12}e_n(n = 24)$	1
Total numbers	210

From Table 2, there are 210 kinds of inductive error pattern. Cyclic shift each pattern to the left by $m(1 \le m \le 36)$ bits so that we can obtain all $210 * 37$ kinds of three-error patterns, and these patterns are further decomposed to the form of 7770.

At this point, the first decomposition is completed, but due to the uneven distribution of the number of errors, the hardware implementation will result in different pipeline lengths, so we need to process the inductive error patterns.

Table 3: Three-error combination.

Group	Three-error combination patterns	Numbers
1	$e_0e_1e_n(2 \le n \le 35), e_0e_{12}e_n(n = 24)$	$34 + 1 = 35$
2	$e_0e_2e_n(4 \le n \le 34), e_0e_{11}e_n(22 \le n \le 25)$	$31 + 4 = 35$
3	$e_0e_3e_n(6 \le n \le 33), e_0e_9e_n(18 \le n \le 27)$	$28 + 7 = 35$
4	$e_0e_4e_n(8 \le n \le 32), e_0e_9e_n(18 \le n \le 27)$	$25 + 10 = 35$
5	$e_0e_5e_n(10 \le n \le 31), e_0e_8e_n(16 \le n \le 28)$	$22 + 13 = 35$
6	$e_0e_6e_n(12 \le n \le 30), e_0e_7e_n(14 \le n \le 29)$	$19 + 16 = 35$

As is shown in Table 3, we combine the inductive error patterns and divide them into 6 groups to make the patterns evenly distributed, and each combination pattern group has 35 inductive error patterns.

We call the inductive patterns in the same group as combination patterns and implement them in same pipeline. Then, the three-error patterns are decomposed into the form as $C_{37}^3 = 7770 = 6 * 35 * 37$.

3.1.2. Two-Error Patterns. The number of two-error patterns is $d\_flag\_\text{in} = 0$, a total of 666 kinds can be decomposed into the 18 kinds of inductive patterns, expressed as $e_0e_n(1 \le n \le 18)$. Then, we cyclically shift each pattern to the left by m $(1 \le m \le 36)$ bits so that we can get all $18 * 36$ kinds of two-error patterns.

Since the three-error patterns are divided into 6 groups, we also combine two-error patterns into 6 groups to maintain the consistency of the pipeline, and each group has 3 two-error inductive patterns. The two-error combination patterns are shown in Table 4.

At this point, the two-error patterns are decomposed into the form as $C_{37}^2 = 6 * 3 * 37$.

3.1.3. Single-Error Pattern. The number of single-error patterns is C_{37}^1, a total of 37 kinds. It is the minimum error correction unit and can be grouped without decomposing. Since the number 37 cannot be evenly divided, the single-error patterns are divided into 6 groups. Each group has 7 single-error patterns, and no operation is performed in redundant part to ensure the consistency of the pipeline. The single-error division groups are shown in Table 5.

3.2. Error Pattern Traversal and Decoding Framework. Unlike the DS algorithm, the priority of the memory footprint optimization in the FPGA application is not high. Therefore, we propose a decoding framework that separates decoding operation into an error pattern traversal part and a codeword decoding part. We use memory cells to reduce register consumption, which is feasible in FPGA designs.

The specific operation of this decoding framework is shown in Section 4. After the preprocessing operation, the codeword r/r' and the flag bit are stored in First Input First Output (FIFO) memory. Then, the codeword r/r' is calculated to obtain the initial syndrome s_r, and we can traversal of all error patterns by s_r. When traversing, if the corresponding condition is met (see Section 4 for details), the decoding flag bit denoting as '*d_flag*' will be set to 1, and the current error pattern denoting as '*ep1*', '*ep2*', and '*ep3*' will be recorded to the register '*e_reg_out1*', '*e_reg_out2*', and '*e_reg_out3*'. When the error pattern traversal is completed, decoding will be performed according to the decoding flag bit, the recorded error pattern positions, and the original codeword stored in FIFO.

Table 4: Two-error combination patterns.

Group	Two-error combination patterns	Numbers
1	e_0e_1, e_0e_2, e_0e_3	3
2	e_0e_4, e_0e_5, e_0e_6	3
3	e_0e_7, e_0e_8, e_0e_9	3
4	$e_0e_{10}, e_0e_{11}, e_0e_{12}$	3
5	$e_0e_{13}, e_0e_{14}, e_0e_{15}$	3
6	$e_0e_{16}, e_0e_{17}, e_0e_{18}$	3

Table 5: Single-error combination patterns.

Group	Single-error combination patterns	Numbers
1	$e_n(0 \le n \le 6)$	7
2	$e_n(7 \le n \le 13)$	7
3	$e_n(14 \le n \le 20)$	7
4	$e_n(21 \le n \le 27)$	7
5	$e_n(28 \le n \le 34)$	7
6	$e_n(n = 35)$	1

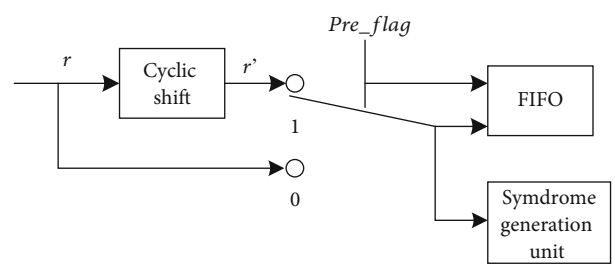


Figure 2: Preprocessing unit.

This framework reduces the register consumption of each stage of the pipeline from store 73 bits of entire codeword to store 18 bits of the three error pattern positions (each error pattern position is 6 bits), which greatly reduces the register consumption. The registers saved here can be used for other intermediate amounts of storage to increase the speed of the entire framework.

4. Hardware Architecture Design

According to Section 3, the operations before and after the cyclic shift are the same, so we can implement these two operations in same hardware framework by preprocessing and postprocessing of the received codeword, then we can realize pipeline multiplexing to improve resource utilization and reduce resource consumption. All the error patterns are summarized and divided into 6 parts, then the decoding

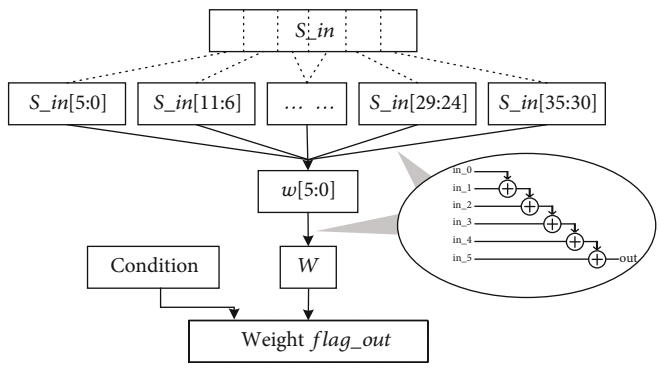


Figure 3: Weight calculation unit.

modules can be multiplexed. We traverse one part each clock, and all the error patterns are traversed by six clocks. The specific modules are as follows.

4.1. Code Words Preprocessing Module. Preprocess the input codeword r by the cyclic shift operation, the original codeword r, and the cyclic shifted codeword r' are given by

$$\begin{aligned} r &= \left(r_{m36}, r_{m35}, \cdots, r_{m0}, r_{p35}, r_{p34}, \cdots, r_{p1}, r_{p0}\right), \\ r' &= \left(r_{m0}, r_{p35}, r_{p34}, \cdots, r_{p0}, r_{m36}, r_{m35}, \cdots, r_{m1}\right). \end{aligned} \tag{5}$$

The specific structure is shown in Figure 2; the current data is determined according to the state of preprocessing flag denoted as 'pre_flag'(0/1); when $pre\_flag = 0$, the current data is original codeword r; when $pre\_flag = 1$, the current data is cyclic shifted codeword r'. Then, the data sequence r, r' are input into initial syndrome generation unit one by one. Note that in order to make the figures clear, the clock signal is not shown in the figures below.

4.2. Weight Calculation Unit. The weight calculation unit can accumulate the sum of $s_i(\sum_{i=0}^{35} s_i)$ (as shown in Figure 3). In order to reduce the path delay and increase the operation frequency, we divide the *S_in* into 6 parts and complete the sum operation in 2 steps.

In addition, a module identification signal named "Condition" is introduced to make the weight calculation unit to adapt to different modules.

In initial syndrome generation module, "flag_out" will be enabled when $W(S_{\text{in}}) \le 6$.

In single-error traversal module, "flag_out" will be enabled when $W(S_{\text{in}}) \le 5$.

In two-error traversal module, "flag_out" will be enabled when $W(S_{\text{in}}) \le 4$.

In three-error traversal module, "flag_out" will be enabled when $W(S_{\text{in}}) \le 3$.

4.3. Syndrome Generation Unit. The syndrome generation unit has two kinds of units, one for s_r and another for s_{ri}, s_{rij}, s_{rijk}.

The calculation of initial syndrome is given by

$$s_r = r_p \wedge (r_{m0} \cdot s_0) \wedge (r_{m1} \cdot s_1) \wedge \cdots \wedge (r_{m36} \cdot s_{36}). \tag{6}$$

Other syndrome calculations are given by

$$\begin{aligned} s_{r,i} &= s_r \wedge s_i (0 \le i \le 36), \\ s_{rij} &= s_r \wedge s_i \wedge s_j (0 \le i < j \le 36), \\ s_{rijk} &= s_r \wedge s_i \wedge s_j \wedge s_k (0 \le i < j < k \le 36), \end{aligned} \tag{7}$$

where i, j, k are the error positions of r_m.

The specific structure is shown in Figure 4. The initial syndrome s_r is calculated by formula (6) according to r_m, r_p and syndromes $s_0 \sim s_{36}$. Then, the other syndromes s_{ri}, s_{rij}, and s_{rijk} can be calculated by s_r, s_i, s_j, and s_k.

According to the algorithm, when the calculation of initial syndrome s_r is completed, the weight $W(s_r)$ of the initial syndrome s_r is calculated firstly. If $W(s_r) \le 6$, the decoding flag bit '*d_flag_init*' is set to 1, the register '*e_reg_out3*' of the current error pattern is assigned to "40", which can provide an indication for postprocessing unit to decoding.

4.4. Error Traversal Units. The error traversal units are divided into three types according to the number of errors in r_m, which are single-error traversal units, two-error traversal units, and three-error traversal units. In order to reduce the consumption of registers in this design, after each traversal unit calculates the weight of the new syndrome, only the current decoding flag bit 'd_flag_out', and the current error pattern 'ep1', 'ep2', 'ep3' are recorded instead of direct decoding. After all pattern traversal is completed, decoding is performed by decoding flag bit and the recorded error patterns.

4.4.1. Single-Error Traversal Units. The specific structure is shown in Figure 5. According to the input error pattern position 'ep1', calculate $s_{r,ep1} = s_r \wedge s_{ep1}$, and calculate the weight $W(s_{r,ep1})$ of $s_{r,ep1}$, then the flag bit 'd_flag_out' will be given according to $W(s_{r,ep1})$. Regardless of whether the current error pattern meets the decoding condition, the current error pattern position 'ep1' is recorded to 'ep1_out', which simplifies the logic and accurately records the error pattern.

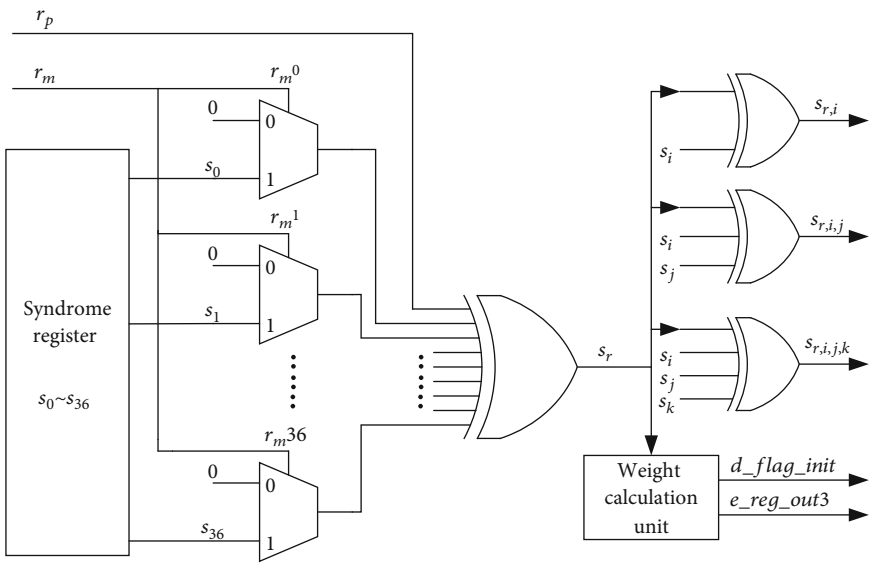


Figure 4: Syndrome generation unit.

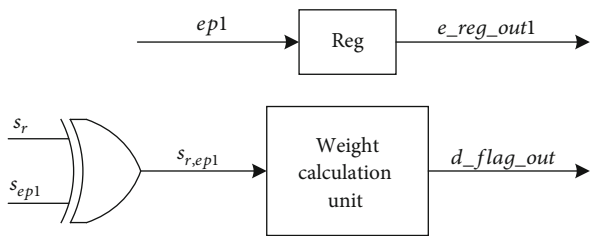


Figure 5: Single-error traversal unit.

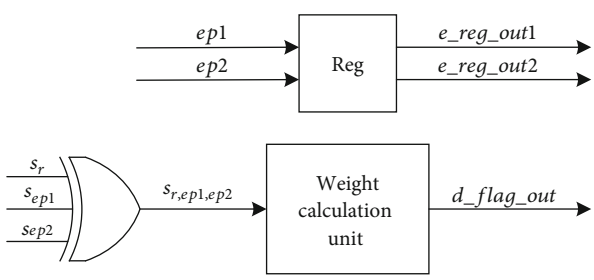


Figure 6: Two-error traversal unit.

4.4.2. Two-Error Traversal Units. The specific structure is shown in Figure 6. According to the input error pattern positions 'ep1', 'ep2', calculates$s_{r,ep1,ep2} = s_r \wedge s_{ep1} \wedge s_{ep2}$, and calculate the weight $W(s_{r,ep1,ep2})$ of $s_{r,ep1,ep2}$. Then, the flag bit 'd_flag_out' will be given according to $W(s_{r,ep1,ep2})$. At the same time, the current error pattern positions 'ep1', 'ep2' are recorded to 'e_reg_out1', 'e_reg_out2'.

4.4.3. Three-Error Traversal Units. The specific structure is shown in Figure 7. According to the input error pattern positions '*ep1*', '*ep2*', '*ep3*', calculate $s_{r,ep1,ep2,ep3} = s_r \wedge s_{ep1} \wedge s_{ep2} \wedge s_{ep3}$, and calculate the weight $W(s_{r,ep1,ep2,ep3})$ of $s_{r,ep1,ep2,ep3}$. Then, the flag bit '*d_flag_out*' will be given according to $W(s_{r,ep1,ep2,ep3})$. At the same time, the current error pattern

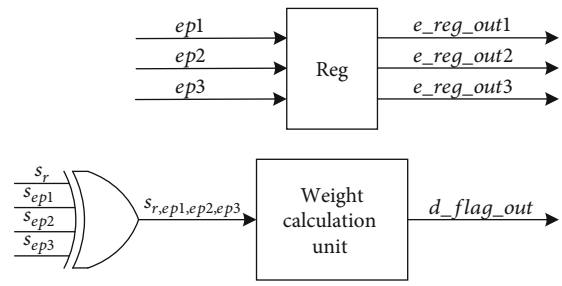


Figure 7: Three-error traversal unit.

Table 6: Traversal the error patterns.

pctr	Three-error combination patterns	Two-error combination patterns	Single-error combination patterns
1	$e_0e_1e_n(2 \le n \le 35)$ $e_0e_{12}e_n(n = 24)$	e_0e_1, e_0e_2, e_0e_3	$e_n(0 \le n \le 6)$
2	$e_0e_2e_n(4 \le n \le 34)$ $e_0e_{11}e_n(22 \le n \le 25)$	e_0e_4, e_0e_5, e_0e_6	$e_n(7 \le n \le 13)$
3	$e_0e_3e_n(6 \le n \le 33)$ $e_0e_9e_n(18 \le n \le 27)$	e_0e_7, e_0e_8, e_0e_9	$e_n(14 \le n \le 20)$
4	$e_0e_4e_n(8 \le n \le 32)$ $e_0e_9e_n(18 \le n \le 27)$	$e_0e_{10}, e_0e_{11}, e_0e_{12}$	$e_n(21 \le n \le 27)$
5	$e_0e_5e_n(10 \le n \le 31)$ $e_0e_8e_n(16 \le n \le 28)$	$e_0e_{13}, e_0e_{14}, e_0e_{15}$	$e_n(28 \le n \le 34)$
6	$e_0e_6e_n(12 \le n \le 30)$ $e_0e_7e_n(14 \le n \le 29)$	$e_0e_{16}, e_0e_{17}, e_0e_{18}$	$e_n(n = 35)$

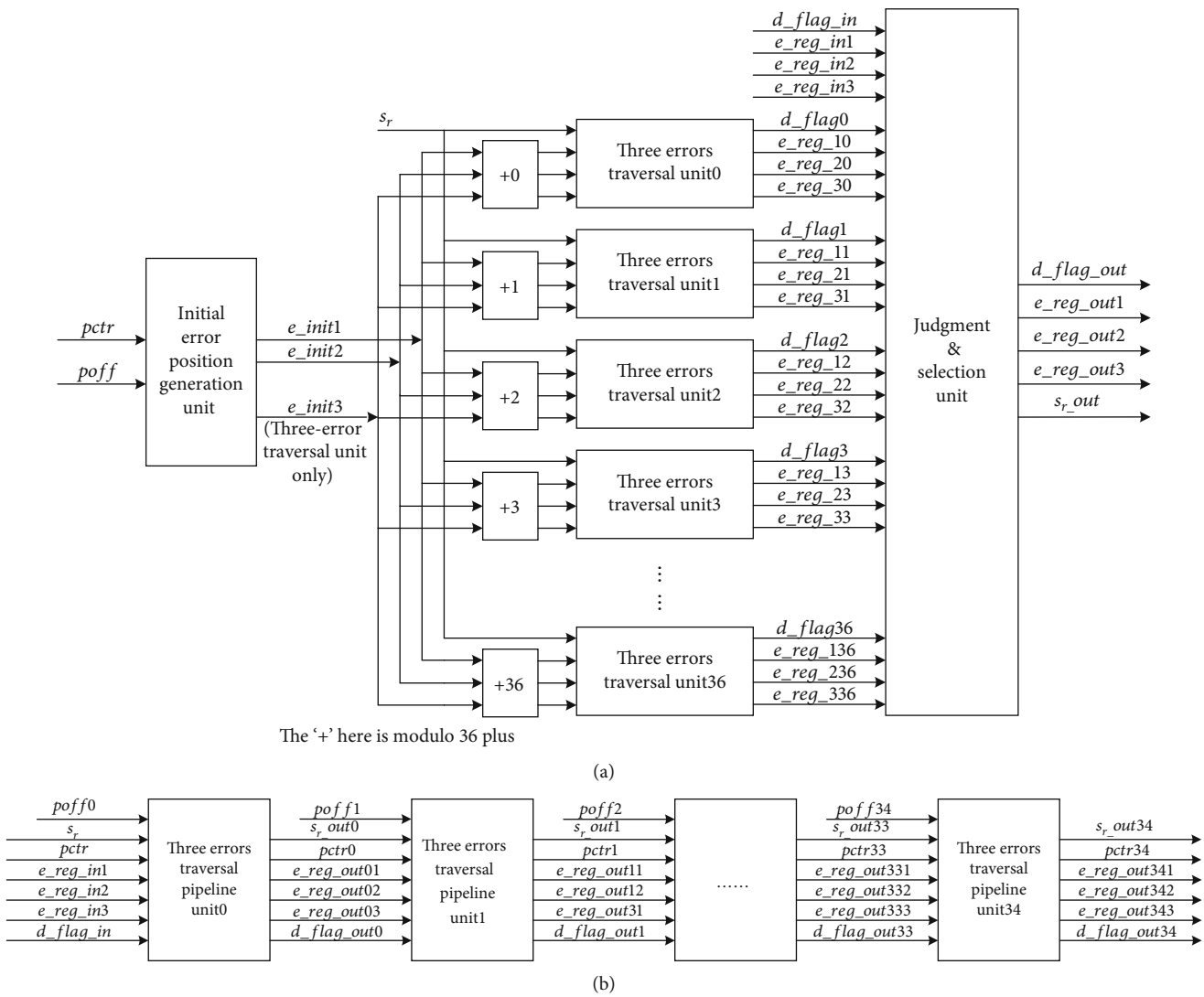


Figure 8: (a) Three-error traversal pipeline unit; (b) three-error traversal module.

positions '*ep1*', '*ep2*', '*ep3*' are recorded to '*e_reg_out1*', '*e_reg_out2*', '*e_reg_out3*'.

4.5. Error Traversal Modules. Each error traversal module can complete one kind of error traversal. To facilitate pipeline implementation, the error traversal units need to be integrated. An appropriate integration method can improve resource utilization and improve the running speed of the entire system.

4.5.1. Three-Error Traversal Module. The inductive error patterns are combined according to Table 3. After combining, the number of each combination pattern is 35. At this time, module multiplexing can be performed by controlling the value of the input parameter '*pctr*'. In each clock, we traverse 35 kinds of inductive error patterns; all three-error patterns will be finished in 6 clocks (as is shown in Table 6).

Change the input parameter '*pctr*' $(1 \le pctr \le 6)$ to control the switching of the combination patterns, and according to the offset parameter '*poff*' $(0 \le poff \le 34)$, we can determine the initialization pattern $e_{init1}e_{init2}e_{init3}$ to construct the basic pipeline unit. The calculation method of the initialization parameter is given by

$$init1 = 0,$$
$$init2 = \begin{cases} 13 - pctr, \text{when } (pctr * 2 + poff) > (36 - pctr), \\ pctr, \text{when } (pctr * 2 + poff) < (36 - pctr), \end{cases}$$
$$init3 = \begin{cases} pctr + poff - 11, \text{when } pctr * 2 + poff > 36 - pctr, \\ pctr * 2 + poff, \text{when } pctr * 2 + poff < 36 - pctr. \end{cases} \tag{8}$$

According to the input decoding flag bit '*d_flag_in*', if $d\_flag\_\text{in} = 1$, the error pattern of the previous stage traversal unit has met the decoding condition, set '*d_flag_out*' to 1, and register '*e_reg_in1*', '*e_reg_in2*', '*e_reg_in3*' directly to '*e_reg_out1*', '*e_reg_out2*', '*e_reg_out3*'; if $d\_flag\_\text{in} = 0$, the

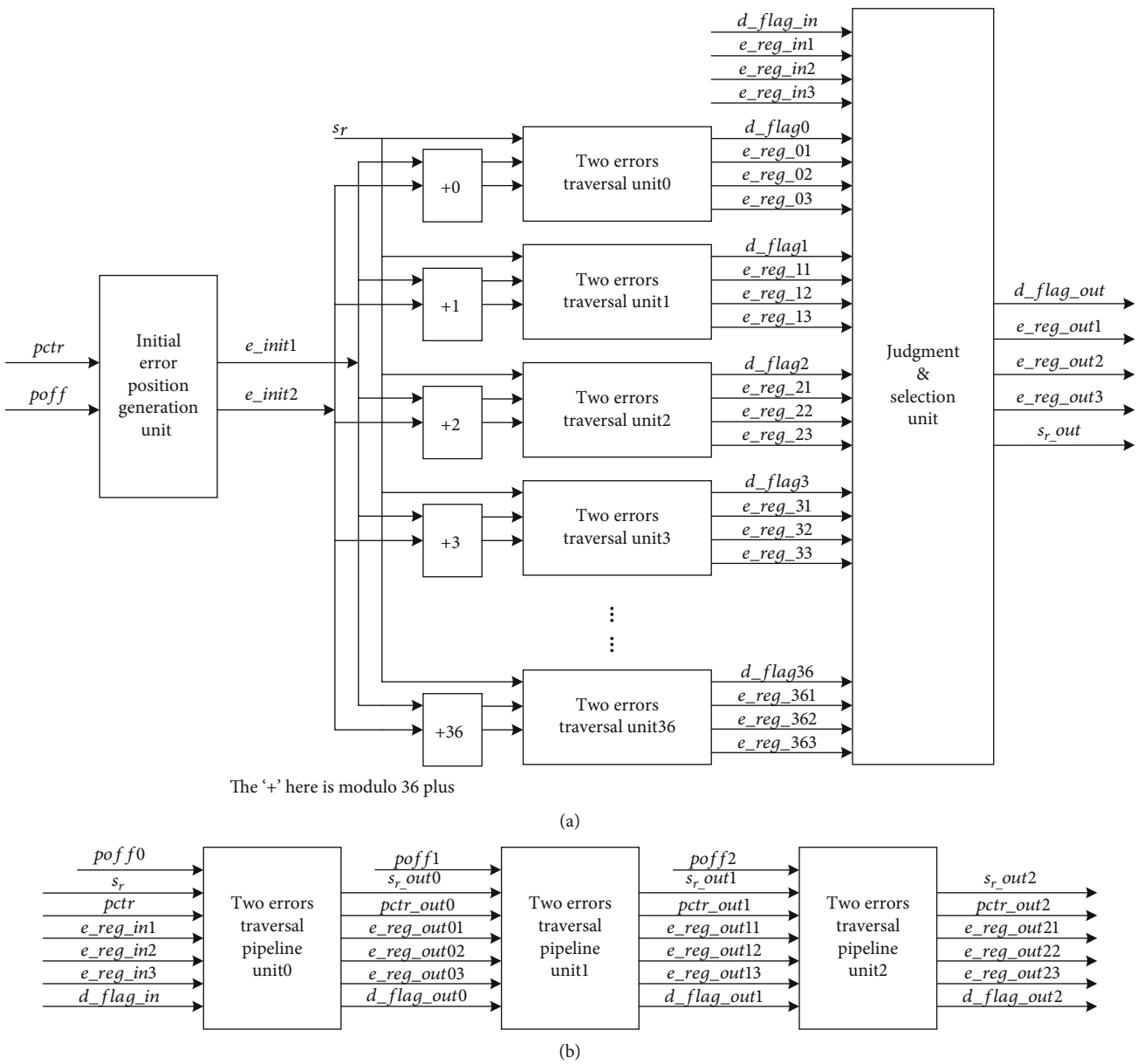


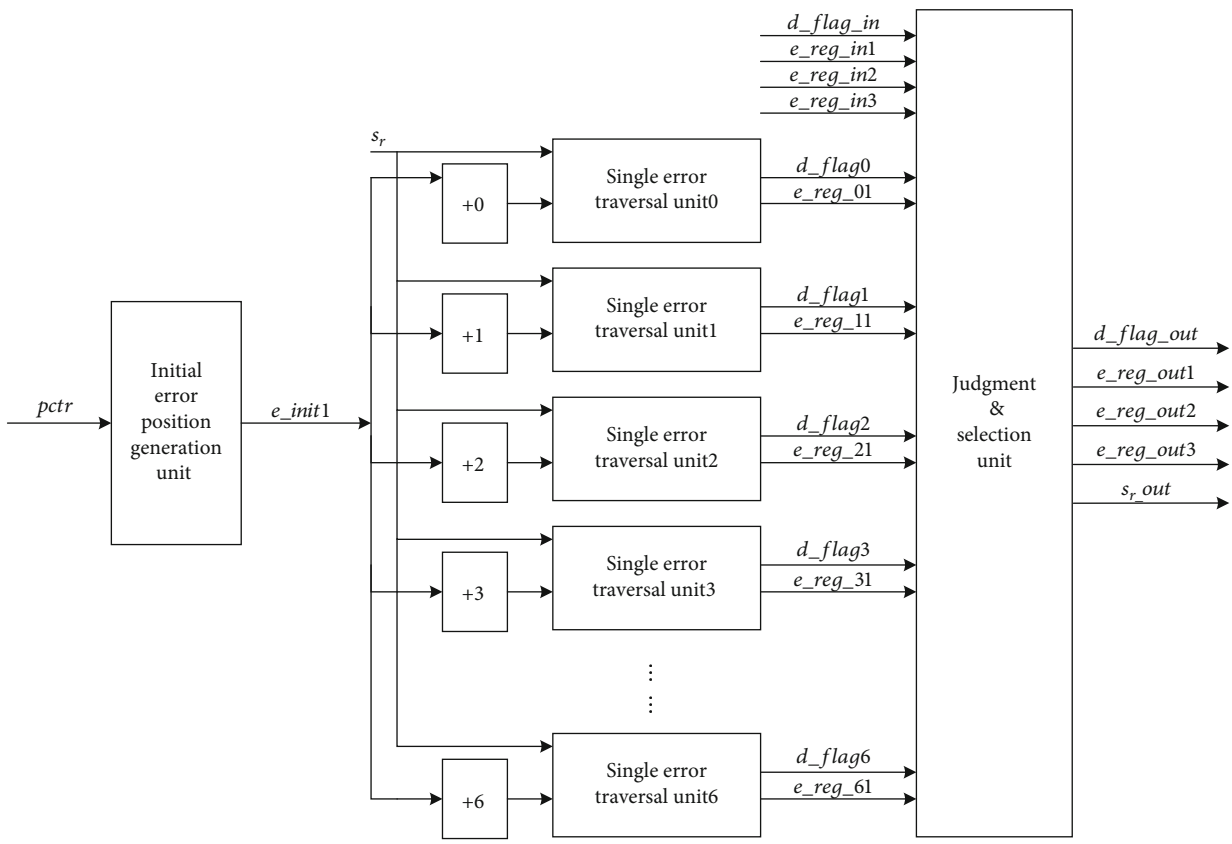
Figure 9: (a) Two-error traversal pipeline unit; (b) three-error traversal module.

error pattern of the previous stage traversal unit does not meet the decoding condition, and the error pattern traversal result of this level is considered.

The specific structure of the basic pipeline unit is shown in Figure 8(a). The initial error positions '*e_init1*', '*e_init2*', '*e_init3*' are determined according to the parameters '*pctr*' and '*poff*'. Then, modulo 36 plus $l(0 \le l \le 36)$ bits, respectively, with initial error positions to obtain new error patterns for traversal. Combined with the input initial syndrome s_r, 37 error traversal units are obtained to form a basic pipeline unit. After traversing these error patterns, the 37 results of traversal are judged and selected. If the error patterns in this unit satisfy the decoding condition, the '*d_flag_out*' is assigned to 1, and the current error positions are output to the error pattern record registers '*e_reg_out1*', '*e_reg_out2*', '*e_reg_out3*'. Then, the input initial syndrome s_r is passed to the next level for traversal.

35 three-error traversal pipeline units are connected step by step to form a complete three-error traversal module. The specific structure is shown in Figure 8(b). The initial syndrome s_r, parameter '*pctr*', decoding flag '*d_flag_out*' and error pattern record register '*e_reg_out1*', '*e_reg_out2*', '*e_reg_out3*' are passed in stages to ensure the integrity of the error pattern traversal and the stability of the data.

4.5.2. Two-Error Traversal Module. In the three-error traversal pipeline unit, all three-error patterns have been distributed by 6 clocks, so we also distribute all two-error patterns into 6 clocks. In each clock, we traverse 3 inductive two-



The '+' here is modulo 36 plus

Figure 10: Single-error traversal pipeline unit.

error patterns, all two-error patterns will be finished in 6 clocks (as shown in Table 6).

Change the input parameter '*pctr*' $(1 \le pctr \le 6)$ to control the switching of the combination patterns, and according to the offset parameter '*poff*' $(0 \le poff \le 3)$, we can determine the initialization pattern $e_{init1}e_{init2}$ to construct the basic pipeline unit. The calculation method of the initialization pattern is given by

$$\begin{aligned} init1 &= 0, \\ init2 &= pctr * 3 + poff - 3. \end{aligned} \tag{9}$$

Table 7: Decoding operations.

e_reg_out3	m_decode	p_decode
40	m_delay	$p\_delay \wedge s\_delay$
41	$m\_delay \wedge e_{e\_reg1}$	$p\_delay \wedge s\_delay \wedge s_{e\_reg1}$
42	$m\_delay \wedge e_{e\_reg1} \wedge e_{e\_reg2}$	$p\_delay \wedge s\_delay \wedge s_{e\_reg1} \wedge s_{e\_reg2}$
0~36	$m\_delay \wedge e_{e\_reg1} \wedge e_{e\_reg2} \wedge e_{e\_reg3}$	$p\_delay \wedge s\_delay \wedge s_{e\_reg1} \wedge s_{e\_reg2} \wedge s_{e\_reg3}$

According to the input decoding flag bit '*d_flag_in*', if $d\_flag\_\text{in} = 1$, the error pattern of the previous stage traversal unit has met the decoding condition, set '*d_flag_out*' to 1, and register '*e_reg_in1*', '*e_reg_in2*', '*e_reg_in3*' directly to '*e_reg_out1*', '*e_reg_out2*', '*e_reg_out3*'; if $d\_flag\_\text{in} = 0$, the error pattern of the previous stage traversal unit does not meet the decoding condition, and the error pattern traversal result of this level is considered.

The specific structure is as shown in Figure 9(a), and the initial error positions 'e_init1', 'e_init2' are determined according to the parameters 'pctr' and '*poff*'. Then, modulo 36 plus $l(0 \le l \le 36)$ bits, respectively, with initial error positions to obtain new error patterns for traversal. Combined with the input initial syndrome s_r, 37 error traversal units are obtained to form a basic pipeline unit. After traversing these error patterns, the 37 results of traversal are judged and selected. If the error patterns in this module satisfy the decoding condition, the 'd_flag_out' is assigned to 1, the current error positions are output to the error pattern record registers 'e_reg_out1', 'e_reg_out2', and the value of 'e_reg_out3' is set to 42, providing an indication for the postprocessing unit. Then, the input initial syndrome is passed to the next level for traversal.

Three two-error traversal pipeline units are connected step by step to form a complete two-error traversal module. The specific structure is shown in Figure 9(b). The initial syndrome, parameters 'pctr', 'poff', decoding flag 'd_flag_out', and error pattern record registers 'e_reg_out1', 'e_reg_

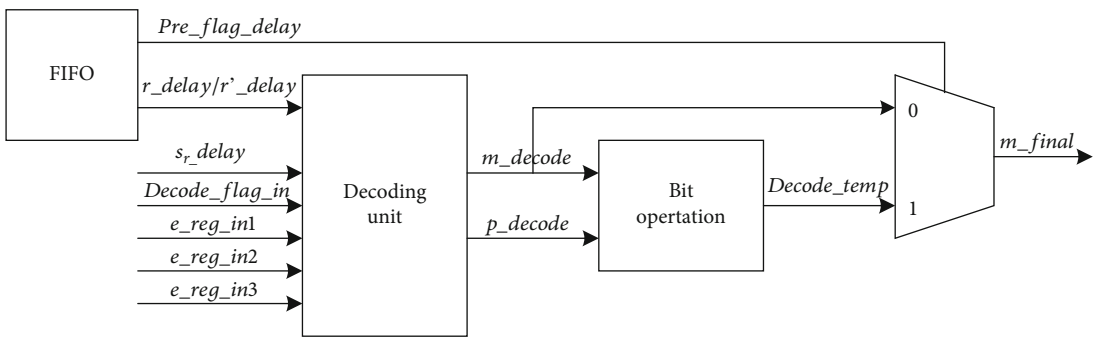


Figure 11: Decoding and postprocessing unit.

out2', 'e_reg_out3' are passed in stages to ensure the integrity of the error pattern traversal and the stability of the data.

4.5.3. Single-Error Traversal Module. The same as three-error and two-error traversal pipeline unit, all the single-error traversal units are distributed to 6 clocks (as shown in Table 6).

Change the input parameter 'pctr' $(1 \le pctr \le 6)$ to control the switching of the combination patterns, we can determine the initialization pattern e_{init1} to construct the basic pipeline unit. The calculation method of the initialization pattern is given by

$$init1 = (para\_ctrl - 1) * 7. \tag{10}$$

According to the input decoding flag bit 'd_flag_in', if $d\_flag\_\text{in} = 1$, the error pattern of the previous stage traversal unit has met the decoding condition, set 'd_flag_out' to 1, and register 'e_reg_in1', 'e_reg_in2', 'e_reg_in3' directly to 'e_reg_out1', 'e_reg_out2', 'e_reg_out3'; if $d\_flag\_\text{in} = 0$, the error pattern of the previous stage traversal unit does not meet the decoding condition, and the error pattern traversal result of this level is considered.

The specific structure is as shown in Figure 10, and the initial error position 'e_init1' is determined according to the parameter 'pctr'. Then, modulo 36 plus $l(0 \le l \le 36)$ bits, respectively, with initial error position to obtain new error patterns for traversal. Combined with the input initial syndrome s_r, 7 single-error traversal units are obtained to form a complete single-error traversal module.

After traversing the error patterns, the 7 results of traversal are judged and selected. If the error patterns satisfy the decoding condition in this module, the 'd_flag_out' is set to 1, the current error positions are output to the error pattern record registers 'err_reg_out1'. And 'err_reg_out2' is set to 0, 'err_reg_out3' is set to 41, which provide indications for postprocessing unit. Then, the input initial syndrome s_r is passed for final decoding.

4.6. Decoding and Postprocessing Unit. Read the data stored in the FIFO, denoted as 'r_delay' and 'pre_flag_delay', and 'r_delay' contains a message part 'm_delay' and a parity part 'p_delay'. According to the decoding status flag bit 'd_flag1', error pattern record registers 'e_reg_out11', 'e_reg_out12', 'e_reg_out13', preprocessing status flag bit 'pre_flag_delay' and the pipeline passed syndrome 's_delay', the decoding can be completed. Denote the decoded codeword message part as 'm_decode' and denote decoded codeword parity part 'p_decode'. The operations of decoding are shown in Table 7.

After the decoding is completed, postprocessing is required to restore the original codeword order. The decoded codeword is cyclically shifted and restored according to the preprocessing status register '*pre_flag_delay*', thereby we can obtain the final decoded codeword '*m_final*' as

$$m\_final = \begin{cases} m\_decode, \text{when } pre\_flag\_delay = 0, \\ \{p\_decode, m\_decode[36]\}, \text{when } pre\_flag\_delay = 1. \end{cases} \tag{11}$$

At this time, the decoding is completed, 'm_final' is the final decoded codeword, and the specific structure is as shown in Figure 11.

4.7. Pipeline Architecture. The preprocessing module, the initial syndrome generation module, the three-error traversal module, the two-error traversal module, the single-error traversal module, and the decoding and postprocessing module are connected step by step to form a 42-stage pipeline. The specific architecture is shown in Figure 12.

4.8. Hardware Implementation Results. The experiment and verification are divided into two parts, software verification and hardware verification. Software verification tests the performance of QR codes while hardware verification tests the acceleration effects of QR codes. Software verification part is carried out on the Personal Computer (PC), which is also mentioned in Section 2. The verification software runs in VS2019, Intel core I5-6500, windows 10 environment, and the decoding time is shown in Table 8. In order to show the difference between various decoding algorithms, we have recorded the decoding error correction time of various decoding algorithms under different number of errors. There is no doubt that the more errors an encoded message has, the longer decoding time cost, and the unstable decoding delay will have an impact on the real-time performance of the IOT device. In addition, the software experiment content also included the average decoding time of various decoding algorithms by calculating average based on the probability distribution of the number of errors, the results can be used as a

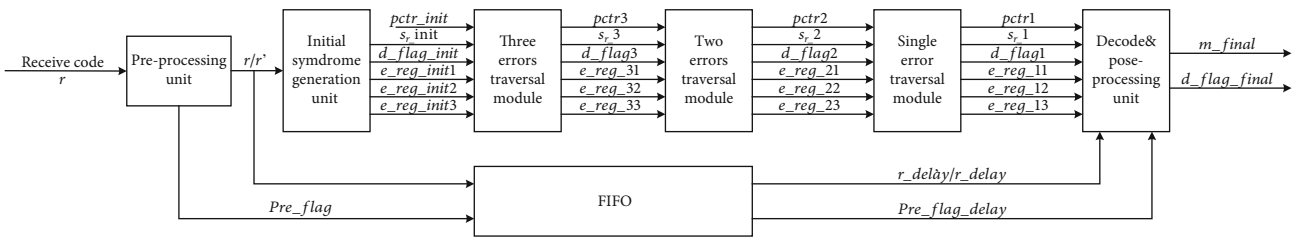


Figure 12: Pipeline architecture.

Table 8: Decoding time under various conditions.

Environment	Works	Error numbers (us) 1	2	3	4	5	6	Average 1	Average 2
PC	*DS in this paper*	1.12	2.16	4.24	19.76	48.36	203.66	190.00	3.863
	IFBM in [17]	205.5	142.7	219.3	2955.9	3104.6	11824	11065.57	378.42
	ADA in [18]	1.8771	17.412	71.391	269.36	536.31	5954.5	5482.66	49.97
	SSDDA in [19]	1.7002	2.5378	22.863	286.47	482.94	701.54	681.27	26.4
	Algorithm in [20]	1134	1848	2611	6822	11417	30915	29193.32	2089
	DS in [14]	0.854	5.69	38.3	95.8	198	245	240.2691	16.02
Arria10	*Hardware implemented in this paper*	0.0461	0.0461	0.0461	0.0461	0.0461	0.0461	0.0461	0.0461

Note that the average decoding time 1 is calculated by supposing all error patterns have the same probability of occurrence. And the average decoding time 2 is calculated by supposing there must be 1~5 errors in the received code and is under the environment of 7 dB SNR, where the occurring probability is 41.27% of one error, 36.49% of two errors, 15.92% of three errors, 5.03% of four errors, 1.1% of five errors, and 0.2% of six errors.

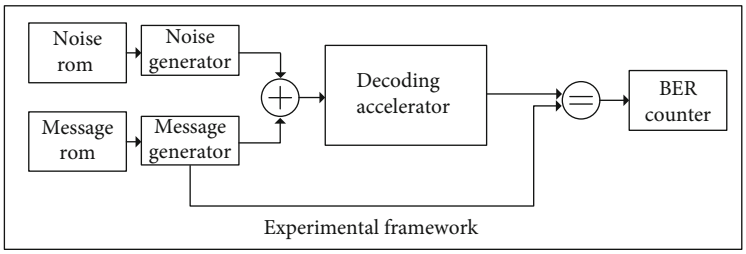


Figure 13: Hardware experimental framework.

reference for the real-time performance of decoding algorithms.

The hardware verification framework is shown in Figure 13. Random messages and noise are generated by ROM lookup table. The sum of encoded message and noise will input into the decoding accelerator. The BER counter records the error rate by comparing the decoding result with the original message.

The decoding accelerator is deployed in Intel Arria10 10AX115U4F45I1SG FPGA; the results is given in the Table 9.

In this decoding framework, all error patterns are evenly distributed into the pipeline, so the decoding time is fixed. A complete decoding requires 125 clocks, the traverse modules cost 12 clocks, 6 clocks to traverse all patterns, and 6 clocks repeated after shifting. Therefore, after 12 clocks of pipeline processing, a valid decoding result can be obtained. At the operation frequency of 260.42 M Hz, every 12 clock outputs can be equivalent to a decoding speed of 21.7 M Hz, the decoding time is 46.07 ns, and the decoding time required of each condition is shown in Table 8. Compared with PC, hardware decoding acceleration can obtain 4121 times of decoding speed increase and can maintain a constant decoding time.

Table 9: Results of accelerator.

	Available	Result
ALMs	43.72 k	12.7 k
Block RAM	55.6 Mbit	0.15 Mbit
Max clock freq.	—	260.42 MHz
Latency	—	46.07 ns

5. Conclusion

This article introduces the feasibility and advantages of QR code in power carrier technology based on the concept of

UPIoT, and according to its shortcomings (decoding complexity and defects with long decoding time) proposed a solution. By improving the DS decoding algorithm, the error pattern is split according to the characteristics of the inductive combination of error patterns, the proposed Error Pattern Induction method has been simulated to prove that the performance is not lost and is better than RS code. This article also analyses the hardware feasibility of separating error pattern traversal and decoding operations and implements an FPGA-based hardware decoding architecture on this basis, on the Intel Arria10 10AX115U4F45I1SG FPGA platform, an equivalent decoding frequency of up to 21.7 MHz is realized, which is 4121 times the decoding speed of software. To our best knowledge, the hardware decoding architecture proposed in this paper is the first hardware implementation of (73, 37, 13) QR code decoding architecture.

While providing a new implementation scheme for PLC error correction coding based on UPIoT, this architecture also shows that QR codes with longer codewords can also be quickly decoded by our hardware frame.

Data Availability

Our data is not public because of confidentiality, readers can contact hjynet@hdu.edu.cn for available data.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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Research Article

14-Bit Fully Differential SAR ADC with PGA Used in Readout Circuit of CMOS Image Sensor

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This paper proposes a 14-bit fully differential Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) with a programmable gain amplifier (PGA) used in the readout circuit of CMOS image sensor (CIS). SAR ADC adopts two-step scaled-reference voltages to realize 14-bit conversion, aimed at reducing the scale of capacitor array and avoiding using calibration to mitigate the impact of offset and mismatch. However, the reference voltage self-calibration algorithm is applied on the design to guarantee the precision of reference voltages, which affects the results of conversion. The three-way PGA provides three types of gains: 3x, 4x, and 6x, and samples at the same time to get three columns of pixel signal and increase the system speed. The pixel array of the mentioned CIS is 1026×1024, and the pixel pitch is $12.5\,\mu m \times 12.5\,\mu m$. The prototype chip is fabricated in the 180 nm CMOS process, and both digital and analog voltages are 3.3 V. The total area of the chip is $6.25 \times 18.38\,mm^2$. At 150 kS/s sampling rate, the SNR of SAR ADC is 71.72 dB and the SFDR is 82.91 dB. What is more, the single SAR ADC consumes 477.2 uW with the 4.8 V_{PP} differential input signal and the total power consumption of the CIS is about 613 mW.

1. Introduction

An image sensor is a device that converts light signals into electrical signals. In recent years, the demand for an image sensor is continuously increasing, which is widely used in mobile phones, SLR digital cameras, automotive electronics, and security industry fields [1]. Mainstream image sensor technologies are roughly divided into two types: CCD image sensor and CMOS image sensor (CIS). With the advantages of high resolution and low noise, CIS gradually becomes the first choice of sophisticated and important fields. Readout circuit is the core part of CIS, whose continuous speed is normally between 50 fps and 10 Mfps while ADC is the important module in readout circuit [2, 3]. Based on the number of ADCs used in a circuit, column ADC may be the most suitable ADC applied in the large pixel array, keeping a good balance between area, power, and speed while the other types are chip ADC and pixel ADC. With the size of pixel array increasing, the mutual interference between signals will increase the complexity of the system when the pixel array studied in most researches is less than 1000 H ∗ 1000 V [4–6]. Combined with the above situation, SAR ADC is employed widely when the scale of pixel array increases. Compared with other types of ADC, the balance between power consumption and speed is always the advantage of SAR ADC. In order to maximize the dynamic range of SAR ADC, a programmable gain amplifier (PGA) is the necessary part used in weak-light conditions, though it usually consumes a substantial amount of power. The performance of SAR ADC and PGA directly affects the quality of the images captured by the image sensor while the bits of SAR ADC decide the resolution and the PGA determines the dynamic range.

The pixel array of CIS presented in this paper is 1026×1024, and the pixel size is $12.5\,\mu m \times 12.5\,\mu m$, which is larger than normal CIS. In order to read signal as fast as possible, column readout circuit is adopted. The resolution of SAR ADC is 14 bits, which is relatively high. Usually, a calibration algorithm is adopted in this situation while the SAR ADC used in this paper do not follow the mainstream practice, considering the power, area, and complexity. However, a reference voltage precision optimization algorithm is used to

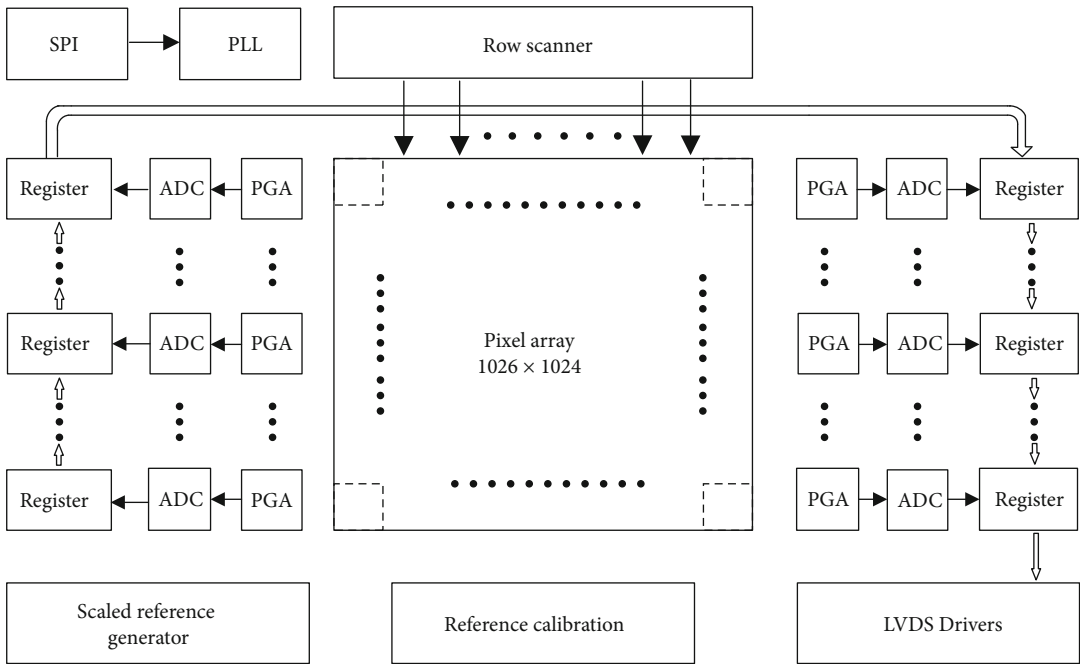


Figure 1: System architecture of the proposed CIS.

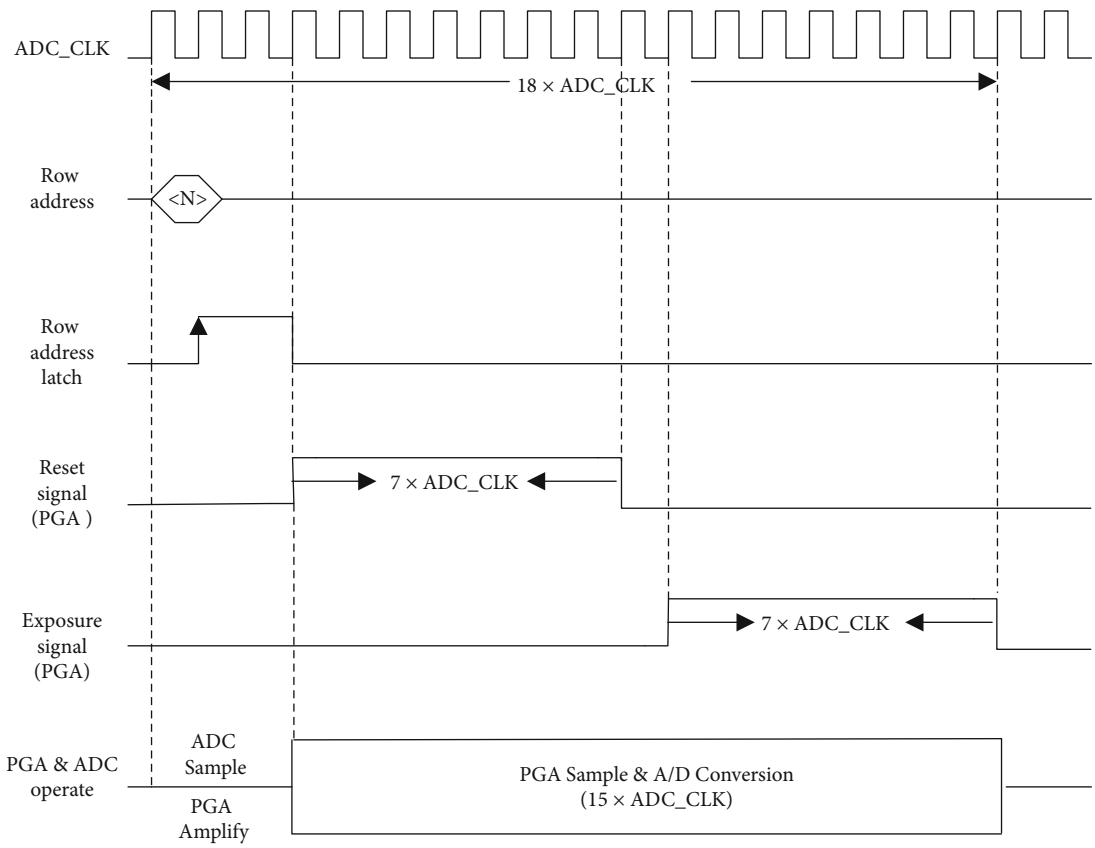


Figure 2: System timing of the proposed CIS.

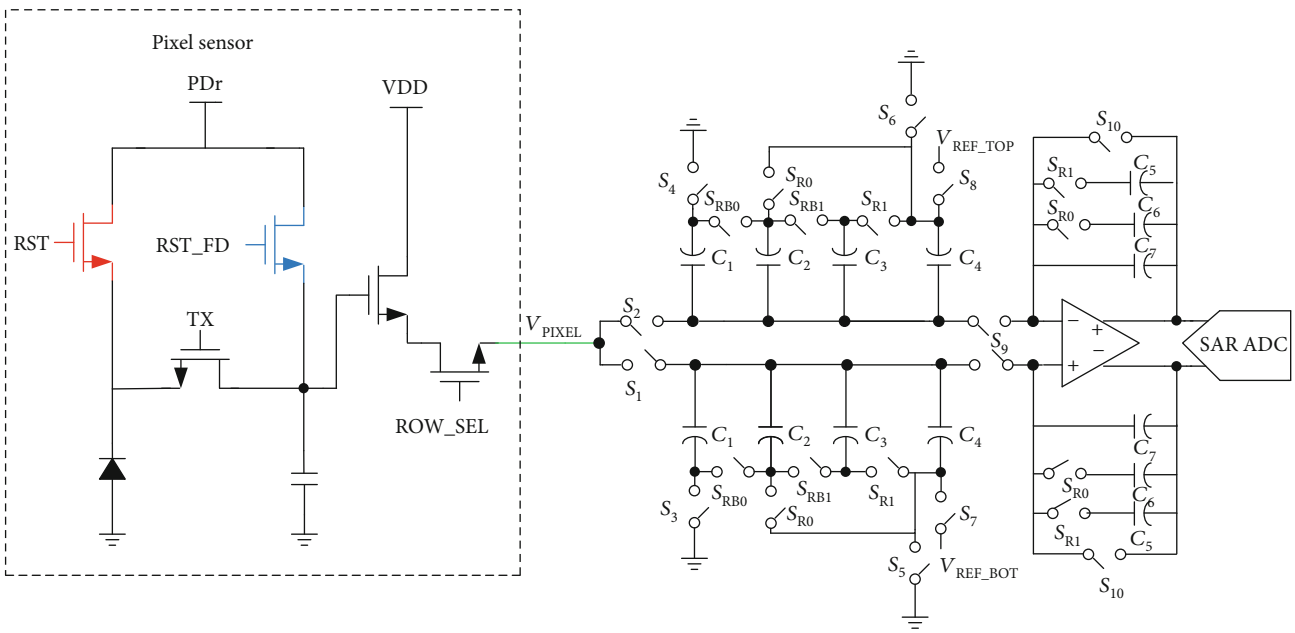


Figure 3: The proposed architecture of PGA samples the signal from the 5-T pixel sensor.

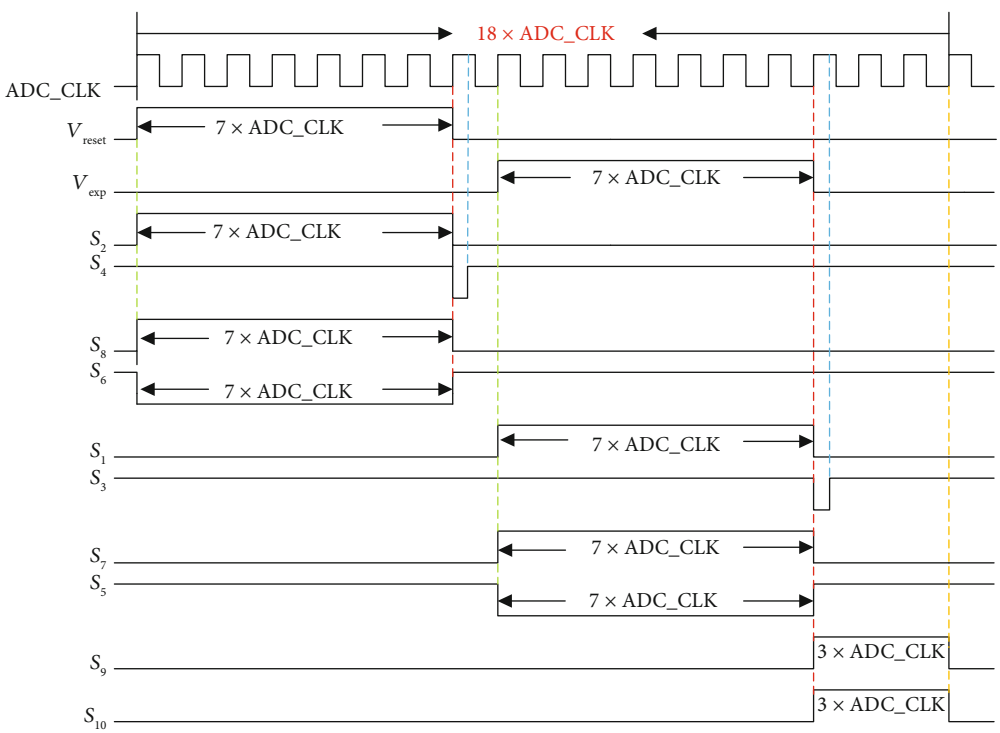


Figure 4: Timing diagram for the PGA.

improve the performance of SAR ADC. What is more, PGA provides the gain of 3x, 4x, and 6x, based on the input signal.

The initial shorter conference paper introduces the working principle and results of the CIS chip briefly [7]. Based on the initial paper, this paper is organized as follows, which shows more details of the CIS chip. Section 2 describes the architecture of the system. The operation principle of different modules is discussed in Section 3, including implementation details of ADC and PGA. The simulated and experimental results of the prototype are illustrated in Section 4. Section 5 concludes this paper.

2. System Architecture

Figure 1 shows the architecture of the proposed CIS, which includes pixel array, PGA, ADC, register, row scanner,

reference generator, reference calibration, Low-Voltage Differential Signaling (LVDS) drivers, and auxiliary circuits. Considering more than one million pixels and the frame rate (50 fps), a column readout circuit is used when a row scanner is applied on selecting a specific row. When the row is determined by a row scanner, a column readout circuit begins to work. The small signal is amplified by PGA and then converted into a digital signal by ADC, which is shifted into register. Finally, the LVDS driver takes on the role of output signal. The proposed CIS works at the speed of 150 KS/s, and the reference clock signal is 2.7 MHz.

During the whole process, the function of PGA is to sample exposure signal, reset signal, and provide three gains: 3x, 4x, and 6x. Owing to exposure signal lower than reset signal, which means that the calculated signal for the difference between exposure signal and reset signal is single-ended, the fixed deviation is added to the system for converting a single-ended signal into differential forms, which is consistent with SAR ADC input. What is more, in order to speed the upsampling process, three-way PGA corresponding to three columns of pixel array is adopted instead of sampling signal one by one. The gain of PGA is decided by the size of signal, which should be distinguished before transferred into SAR ADC.

14-bit fully differential SAR ADC is necessary for the proposed CIS, which directly affects the image. The high-precision reference voltage is the guarantee of SAR ADC. As a result, a scaled reference generator is used with a reference calibration module.

The system timing of the proposed CIS is shown in Figure 2. The working cycle of the chip is 18 ADC_CLKs (reference clock signal). During the first 3 ADC_CLKs, a specific row is chosen when SAR ADC samples the signal amplified by PGA. The remained 15 ADC_CLKs mainly include the following work: the conversion of SAR ADC, the signal sampling of PGA, and the data reading. During the sampling process of PGA, the reset signal is sampled first and the exposure signal follows.

3. Operation Principle and Circuit Implementation

In this section, the operation principle and circuit implementation of CIS are introduced, which consist of PGA, SAR ADC, and reference voltage self-correction algorithm. Referring to SAR ADC, principle and timing are described. What is more, the core parts of SAR ADC are presented in detail, including comparator and DAC.

3.1. PGA. In the CMOS image sensor system, a pixel sensor which demonstrates the brightness of the outside light depends on the difference between reset signal and exposure signal. The form of reset and exposure signal is voltage, which needed to be sampled and amplified into a suitable size. In order to increase the speed of the readout circuit, reset and exposure signals are sampled by different capacitors and amplified by a differential amplifier.

Based on the principle of pixel array, the reset signal is always higher than the exposure signal, which results in the unipolar difference all the time. The proposed architecture of PGA shown in Figure 3 aims at solving the problem by introducing a fixed deviation. V_{PIXEL} represents the reset and exposure signals, which is the output signal of the 5-T pixel sensor. With the help of a combination of capacitors C_1, C_2, C_3, and C_4, the unipolar difference between them is converted into bipolar form and averaged over the positive and negative half axes. The single-ended signal is transferred to a differential signal, which is more convenient for SAR ADC. The control action of switches S_{RB} and S_{R} is the opposite, which decides the gain of PGA. The switching of S_{R1} and S_{R0} changes the magnitude of the gain from 3x to 4x or 6x. What is more, $V_{\mathrm{REF\_TOP}}$ and $V_{\mathrm{REF\_BOT}}$ are the reference voltage of SAR ADC, which is applied on PGA as well. The purpose of adopting different reference voltages is to generate the needed deviation.

Table 1: The value of capacitors from C_1 to C_7.

C_1	C_2	C_3	C_4	C_5	C_6	C_7
$33C_u$	$4C_u$	$4C_u$	$7C_u$	$4C_u$	$4C_u$	$8C_u$

The working cycle of PGA is 18 ADC_CLKs, which is the same as the system and ADC working cycle. The following analysis of operation principle of PGA is based on the charge. The change on charge represents the switch of working status.

As shown in Figure 4, reset signal which is called V_{reset} is got by PGA. During the first 7 ADCs, switches S_2, S_4, and S_8 are on while S_6 is off on the upper capacitor array part. What is more, switches S_{RB0} and S_{R1} are on when the lower plates of capacitors C_1 and C_2 are connected to the ground and the lower plates of capacitors C_3 and C_4 are connected to the $V_{\mathrm{REF\_TOP}}$. The total charge Q_{UP} stored in capacitors C_1, C_2, C_3, and C_4 on the upper part is calculated as follows:

$$Q_{\mathrm{UP}} = (C_1 + C_2)\bullet(V_{\mathrm{reset}} - V_{\mathrm{GND}}) + (C_3 + C_4)\bullet\left(V_{\mathrm{reset}} - V_{\mathrm{REF_{TOP}}}\right). \tag{1}$$

At the 8th ADC_CLK, all switches on the upper part begin to change. The switches S_2 and S_8 turn off while the switch S_6 turns on. What is more, S_4 turns off first and turns on again in the half of ADC_CLK. The lower plates of C_3 and C_4 are connected from $V_{\mathrm{REF\_TOP}}$ to the ground. However, the capacitors are not connected to new power and the total charge keeps on. Considering the switch S_2 is open, the upper plate voltages of capacitors are not regular. Based on the charge conservation and the ignoration of offset, the voltage of the upper plate can be achieved by

$$Q_{\mathrm{UP}} = (C_1 + C_2 + C_3 + C_4)(V_{\mathrm{UP}} - V_{\mathrm{GND}}), \tag{2}$$

$$V_{\mathrm{UP}} = V_{\mathrm{reset}} - \frac{C_3 + C_4}{C_1 + C_2 + C_3 + C_4}\left(V_{\mathrm{REF\_TOP}} - V_{\mathrm{GND}}\right). \tag{3}$$

The latter 7 ADC_CLKs are from 9 to 15 ADC_CLKs. In this period, the exposure signal is sampled by the lower part

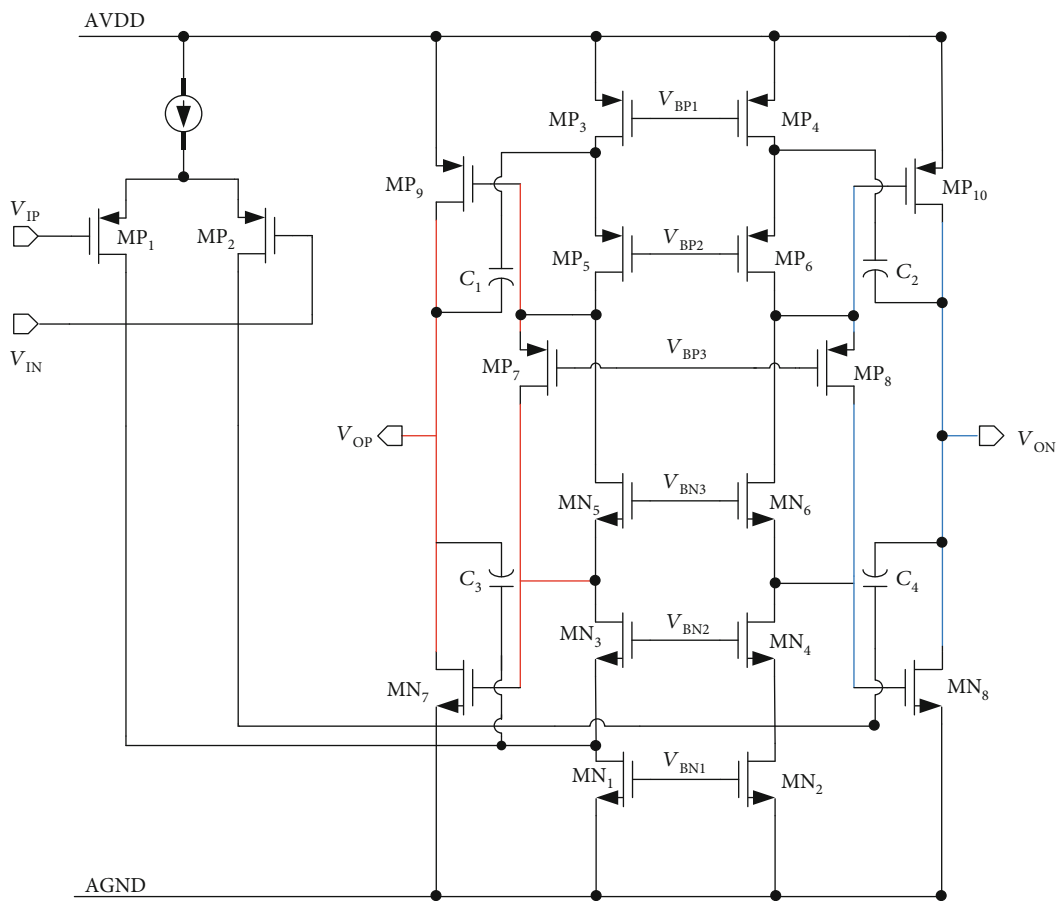


Figure 5: Architecture of operational amplifier.

of a circuit. The principle and process of sampling are the same as the reset signal. At the beginning, the switches S_1, S_3, and S_7 are closed and S_5 is open. The charge Q_{DN} sampled in this procedure is

$$Q_{DN} = (C_1 + C_2)\bullet(V_{exp} - V_{GND}) + (C_3 + C_4)\bullet(V_{exp} - V_{REF\_TOP}). \tag{4}$$

And then, the switch S_5 turns on and S_1, S_3, and S_7 turn off. Finally, S_1 and S_7 keep off and S_3 and S_5 keep on, where the state of S_3 is from open to closed. Through this process, the following equations can be obtained:

$$Q_{DN} = (C_1 + C_2 + C_3 + C_4)(V_{DN} - V_{GND}), \tag{5}$$

$$V_{DN} = V_{reset} - \frac{C_3 + C_4}{C_1 + C_2 + C_3 + C_4}(V_{REF\_BOT} - V_{GND}). \tag{6}$$

Combining equations (1)–(6), the differential signal sent into the amplifier is described by the following equations:

$$V_{IN} = V_{DN} - V_{UP}, \tag{7}$$

$$V_{IN} = (V_{exp} - V_{reset}) + \frac{C_3 + C_4}{C_1 + C_2 + C_3 + C_4}(V_{REF\_TOP} - V_{GND}). \tag{8}$$

According to equation (8), apart from the difference between V_{exp} and V_{reset}, the fixed deviation is introduced as expected, which realizes the goal of making the signal spread uniformly. After sampling is finished, switches S_9 and S_{10} turn on, which lasts 3 ADC_CLK.

During the phase, the function of S_{R0} and S_{R1} is to choose different gains which is called amplify phase as well. The value of capacitors used in the PGA is shown in Table 1. The calculation formula of gain is

$$V_{IN} = \frac{C_1 + C_2 + C_3 + C_4}{C_5 + C_6 + C_7}. \tag{9}$$

If switches S_{R0} and S_{R1} both turn on, the gain of PGA is 6x. While if one of them turns off, the gain of PGA is 4x. Once both are closed, the smallest gain 3x is achieved under this situation.

As a significant part of PGA, the operational amplifier needs to be paid enough attention to. Figure 5 shows the architecture of amplifier, which needs high gain, enough bandwidth, strong driving capability, and low noise. The

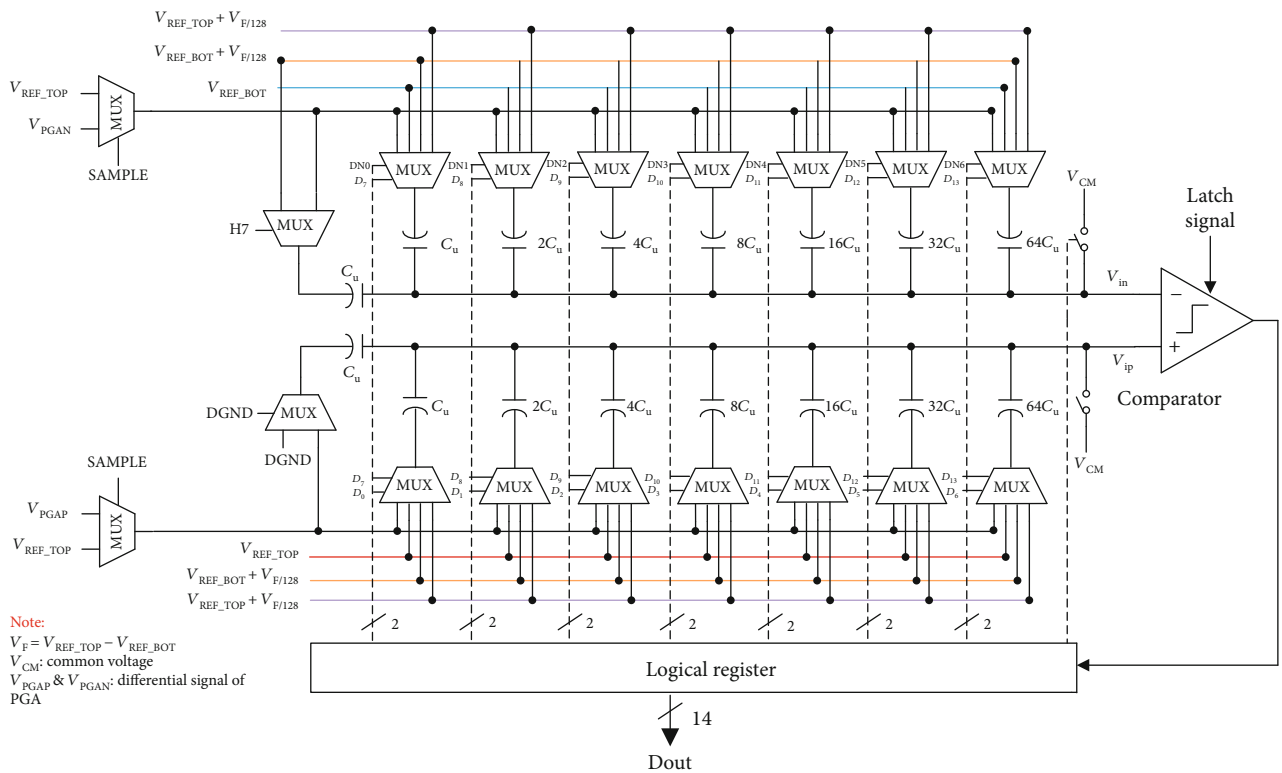


Figure 6: The architecture of the proposed SAR ADC.

proposed amplifier contains two stages: amplifying stage and driving stage, aimed at providing enough gain and increasing the ability of driving. Compared with other architectures of amplifier, the wider input common mode range and larger output swing are the advantages of folding cascode operational amplifier, which is applied in this situation and provides major gain. The cascode stage makes the R_{out} increase, which leads to high gain.

The driving stage is the floating-biased class AB output stage, having a strong driving ability. The size of following-up capacitor arrays used in the SAR ADC is large, which puts forward higher requirements for the driver of the input stage. Considering the high power consumption of folding cascode amplifier, the floating biased transistors MN_5, MN_6, MP_7, and MP_8 are utilized to decrease and stabilize quiescent current of the output stage as analyzed in [8]. The overall gain of the two-stage amplifier is

$$A_{op} = g_{MP1} \bullet ((g_{MN3} \bullet r_{o,MN3} \bullet (r_{o,MN1} \| r_{o,MP1})) \| (g_{MP5} \bullet r_{o,MP3} \bullet r_{o,MP5})) \bullet (g_{MN7} + g_{MP9}) \bullet (r_{o,MN7} \| r_{o,MP9}). \quad (10)$$

When it comes to noise, the high noise is always the drawback of folding cascode amplifier, as depicted in [9]. However, the operational amplifier of this structure meets design requirements. In order to improve the performance of noise, PMOS is adopted as input, which is better than NMOS on noise. What is more, larger value of g_{MP1} and smaller value of g_{MN1} and g_{MP3} are chosen to reduce the noise. Under the circumstance, the value of W/L needs to be weighed carefully, which is important for improving the SNR of SAR ADC.

3.2. SAR ADC. The most important module of CIS is SAR ADC, which is placed after PGA. The function of SAR ADC is to convert the analog signal amplified by PGA into the digital signal.

The sampling speed of SAR ADC required by the system is 150 KS/s, and the resolution of SAR ADC is 14 bits. Normally, the differential input method is selected to suppress the interference of common mode factors and the charge redistribution theory is applied on SAR ADC, which was first proposed by McCreary and Gray [10]. Combing the above two points, the architecture of double reference voltage SAR ADC is widely used. If the resolution of SAR ADC is beyond 10 bits, the capacitor array will be very large, taking up unexpected area in the situation. In order to avoid a huge capacitor array, the two-step scaled-reference SAR ADC is put forward, which is based on the charge redistribution theory as well. This structure was first proposed by South Korea's Shin for CMOS image sensor applications [11]. Two-step scaled reference contains four reference voltages, and the increased reference voltage is to reduce the area of the capacitor array.

3.2.1. Principle and Timing. The architecture of the proposed SAR ADC is shown in Figure 6, containing DAC, comparator, and SAR Logic. Compared with double reference voltages, two-step scaled reference keeps on the size of

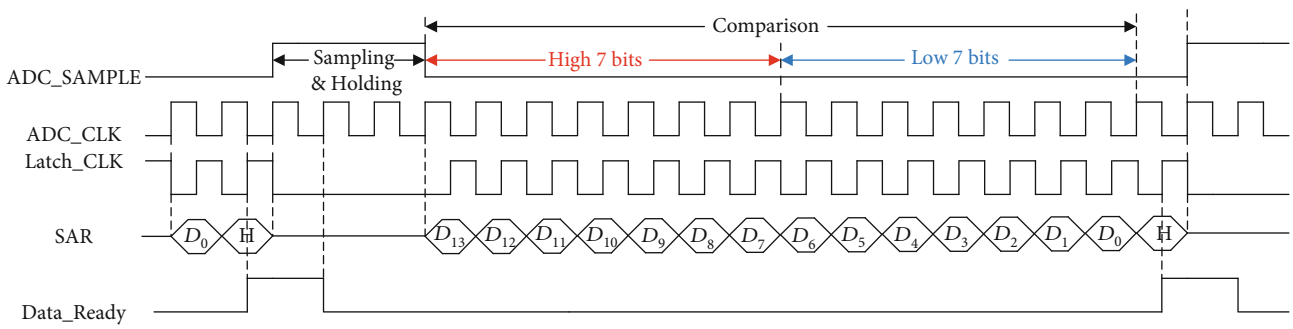


Figure 7: Timing diagram of SAR ADC.

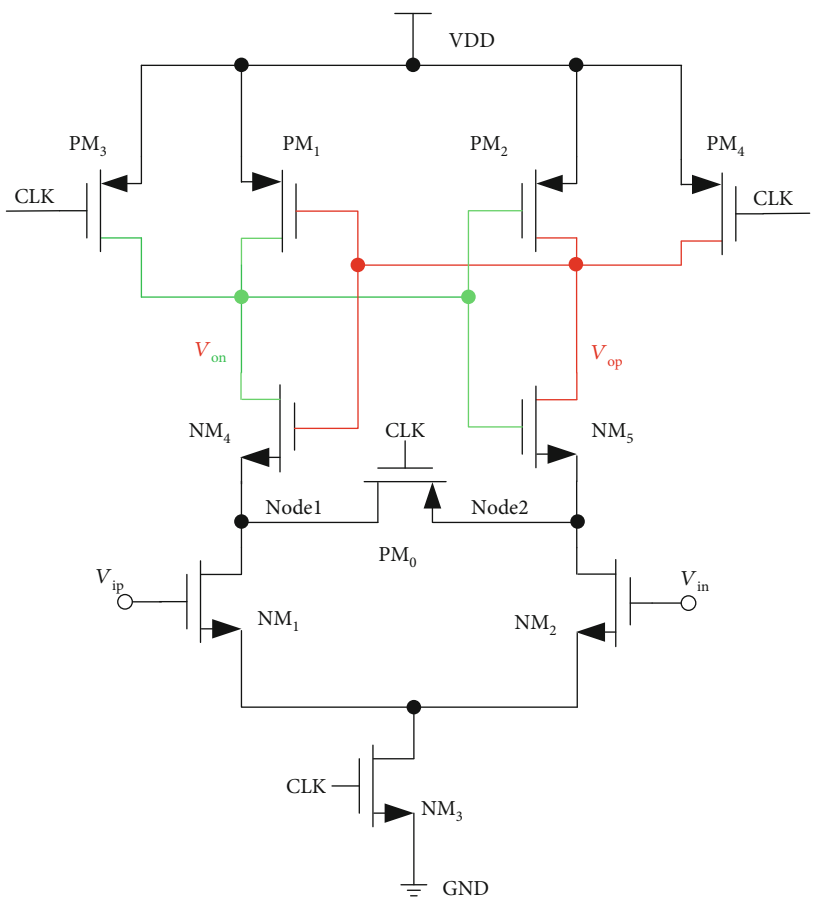


Figure 8: StrongARM latch topology.

capacitor array with the complex conversion process. Use the same size capacitor array, but the resolution has changed from the previous 7 bits to 14 bits, which is the core advantage of the architecture. On the other hand, the requirement of precision of reference voltage is increasing. The added reference voltages $V_{\text{REF\_TOP}} + V_F/128$ and $V_{\text{REF\_BOT}} + V_F/128$ need higher accuracy compared with $V_{\text{REF\_TOP}}$ and $V_{\text{REF\_BOT}}$. $V_{\text{REF\_TOP}}$ and $V_{\text{REF\_BOT}}$ are the reference voltages used in the first stage while the $V_{\text{REF\_TOP}} + V_F/128$ and $V_{\text{REF\_BOT}} + V_F/128$ are applied on the second stage. The value of V_F is

$$V_F = V_{\text{RFF\_TOP}} - V_{\text{RFF\_BOT}}. \tag{11}$$

V_{PGAP} and V_{PGAN} are the output signals of PGA, which are the same as V_{OP} and V_{ON} shown in Figure 5. V_{CM} is the common voltage of the input signal of SAR ADC.

The whole process includes four parts: sampling, holding, comparison, and output. The architecture adopts lower plates of capacitors to sample. During the sampling phase,

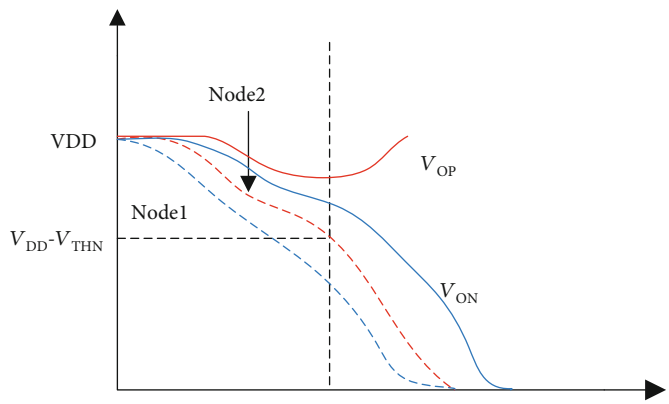


Figure 9: The voltage change of the whole process.

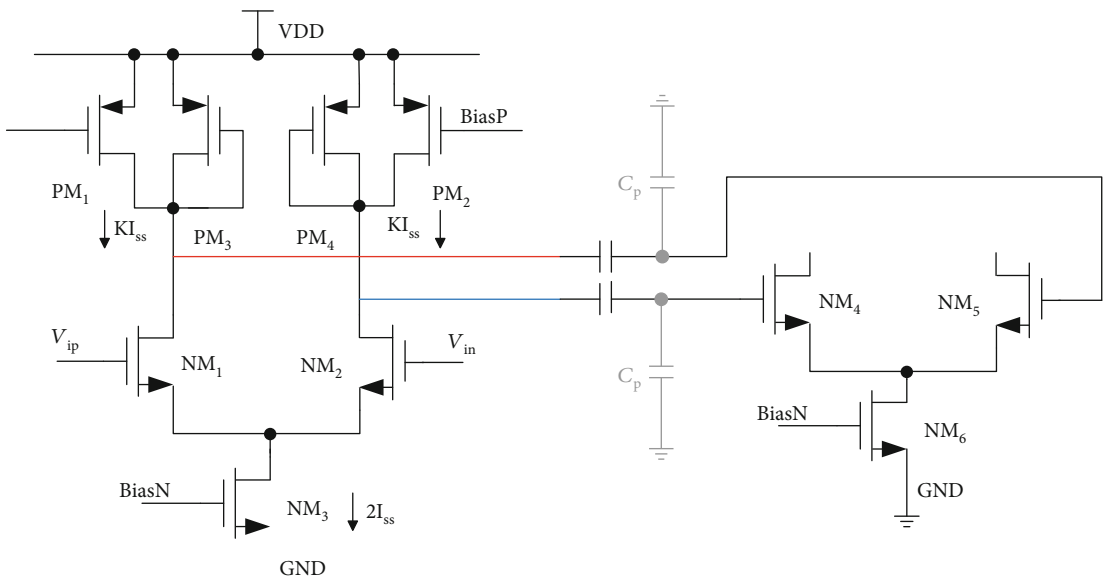


Figure 10: The architecture of preamplifier.

V_{PGAP} and V_{PGAN} are chosen by MUX when all upper plates of capacitors are connected to V_{CM}. The signal V_{PGAP} and V_{PGAN} are sampled by the capacitor array because all lower plates of capacitors are connected to V_{PGAP} and V_{PGAN}. The charge Q_s stored in all capacitors is calculated as

$$Q_s = -(V_{PGAP} - V_{PGAN}) * 2^7 C_u. \tag{12}$$

Converting the input voltage into the form of charge is the principle of sampling. In order to hold the sampled charge, the upper plates of capacitors do not connect to the V_{CM}. The lower plates of capacitors in the negative part are connected to the V_{REF_TOP} when the lower plates of capacitors in the positive part are connected to the V_{REF_BOT}. After finishing the procedure, according to the charge conservation theory, the following equations are obtained:

$$Q_{HP} = \left(V_{ip} - V_{REF_{BOT}}\right) * 2^7 C_u, \tag{13}$$

$$Q_{HN} = \left(V_{in} - V_{REF_{TOP}}\right) * 2^7 C_u, \tag{14}$$

$$Q_H = Q_{HP} - Q_{HN}. \tag{15}$$

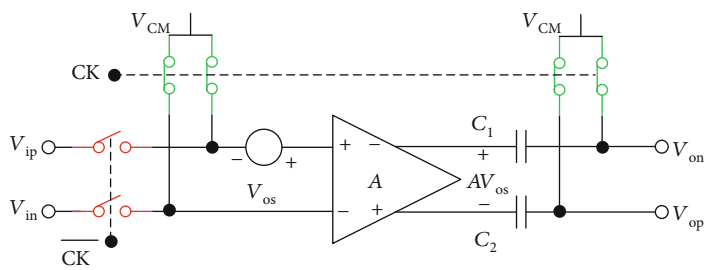
Combining equations (12)–(15), the input signal of comparator is achieved:

$$V_{ip} = V_{REF\_BOT} - V_{PGAP}, \tag{16}$$

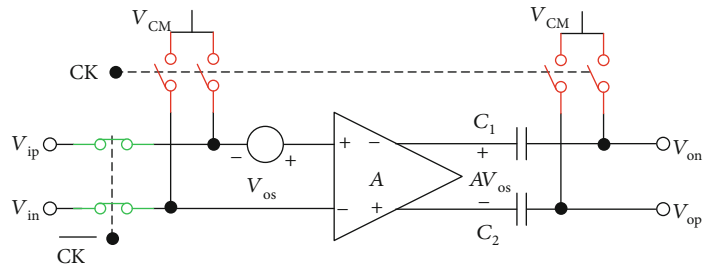
$$V_{in} = V_{REF\_TOP} - V_{PGAN}, \tag{17}$$

$$V_{IN} = V_{ip} - V_{in} = V_{REF\_BOT} - V_{PGAP} - \left(V_{REF\_TOP} - V_{PGAN}\right). \tag{18}$$

Once the holding phase is finished, SAR ADC enters the comparison phase, which contains two parts: high 7-bit conversion and low 7-bit conversion. The reference voltages of high 7-bit conversion are V_{REF_TOP} and V_{REF_BOT} while $V_{REF\_TOP} + V_F/128$ and $V_{REF\_BOT} + V_F/128$ are the reference voltages of low 7-bit conversion. Controlling the connection of lower plates of capacitor array to adjust the input signal of comparator and then get the corresponding code according



(a) Reset phase



(b) Amplification phase

Figure 11: Offset cancellation circuit.

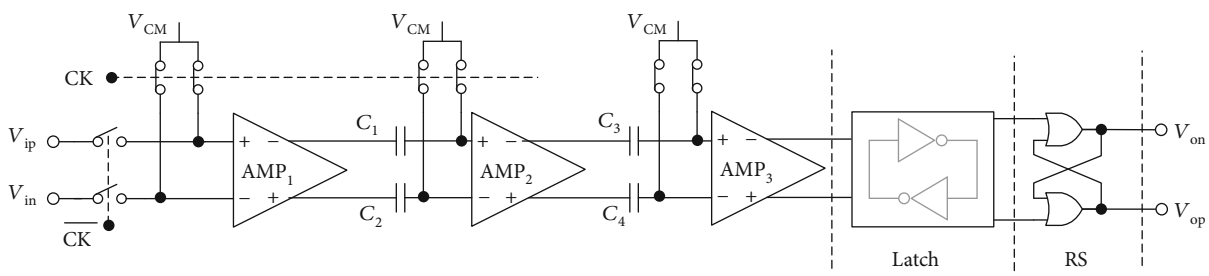


Figure 12: The complete structure of comparator.

to the comparison result is the core working principle of comparison.

During the high 7-bit conversion, the MSB (D_{13}) is taken for example and the others are the same working process. At the beginning, the lower plate of highest capacitance ($64C_u$) in the positive side is connected from $V_{\text{REF\_BOT}}$ to $V_{\text{REF\_TOP}}$ and the lower plate of the highest capacitor ($64C_u$) in the negative side is connected to $V_{\text{REF\_BOT}}$. The other plates of capacitance keep on the current states. The change of charge Q_c stored in the capacitor array is calculated as follows:

$$\begin{aligned} Q_c &= \left(V_{\text{REF}_{\text{TOP}}} - V_{\text{REF}_{\text{BOT}}}\right) * 2^6 C_u - \left(V_{\text{REF}_{\text{BOT}}} - V_{\text{REF}_{\text{TOP}}}\right) \\ &\quad * 2^6 C_u = 2 * \left(V_{\text{REF}_{\text{TOP}}} - V_{\text{REF}_{\text{BOT}}}\right) * 2^6 C_u \\ &= \left(V_{\text{REF}_{\text{TOP}}} - V_{\text{REF}_{\text{BOT}}}\right) * 2^7 C_u. \end{aligned} \tag{19}$$

The input signal of comparator V_{IN} follows with Q_c:

$$V_{\text{IN}} = -\left(V_{\text{PGAP}} - V_{\text{PGAN}}\right). \tag{20}$$

If the V_{IN} is negative, the result of comparator is 0, which means V_{PGAP} is larger than V_{PGAN} and the SAR Logic should control the switch to keep on. Otherwise, the result of comparator is 1. The lower plate of highest capacitance ($64C_u$) in the positive side is connected to $V_{\text{REF\_BOT}}$ instead of $V_{\text{REF\_TOP}}$, and the negative side is the opposite, which also represents V_{PGAP} which is smaller than V_{PGAN}. The rest 6 bits work in the same way.

The conversion of low 7 bits is different from high 7 bits. When the conversion of the 7th bit is finished, the lower plate of dummy capacitor in the negative side is connected to $V_{\text{REF\_BOT}} + V_F/128$ and the lower plates of other capacitors are connected to $V_{\text{REF\_BOT}} + V_F/128$ or $V_{\text{REF\_TOP}} + V_F/128$, which are determined by the original state and increases by $V_F/128$. The purpose of the switch action is to keep the value of V_{IN} on with the increasement of connected voltages of capacitors in the negative side and decrease of connected voltage of dummy capacitor. The decreased charge Q_{DEC} and Q_{INC} can be expressed as

$$Q_{\text{DEC}} = \left(V_{\text{REF\_TOP}} - \left(V_{\text{REF}_{\text{BOT}}} - \frac{V_F}{128}\right)\bullet C_u = \left(V_F - \frac{V_F}{128}\right)\bullet C_u, \tag{21}$$

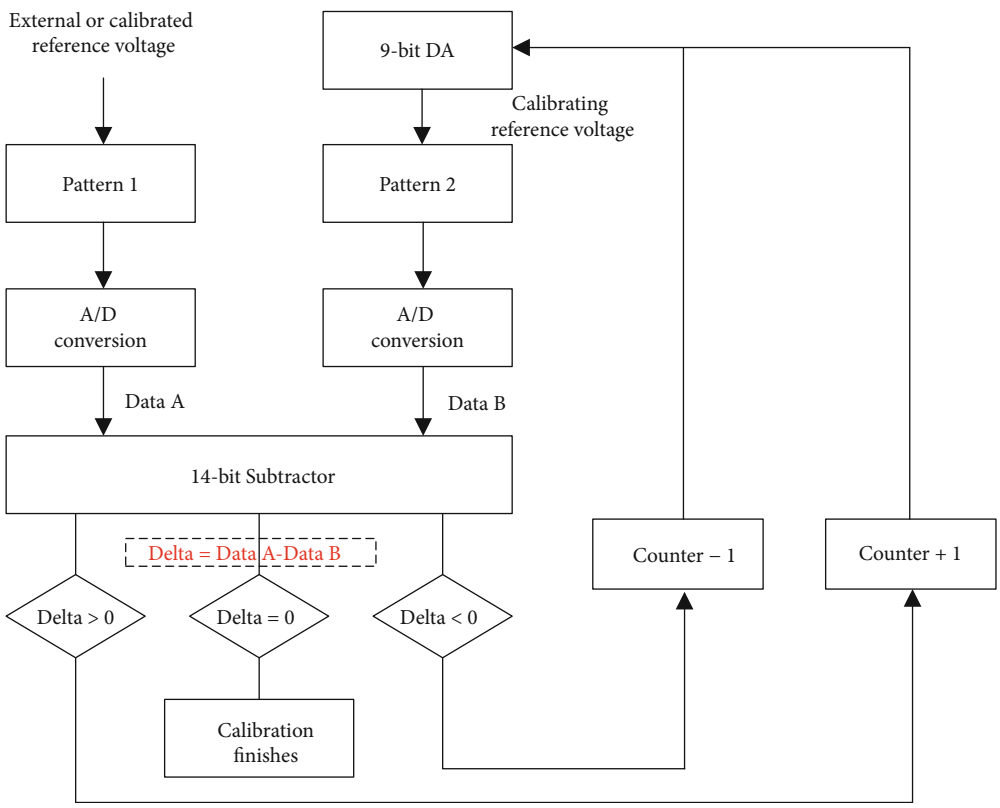


Figure 13: Flowchart of the self-calibration algorithm.

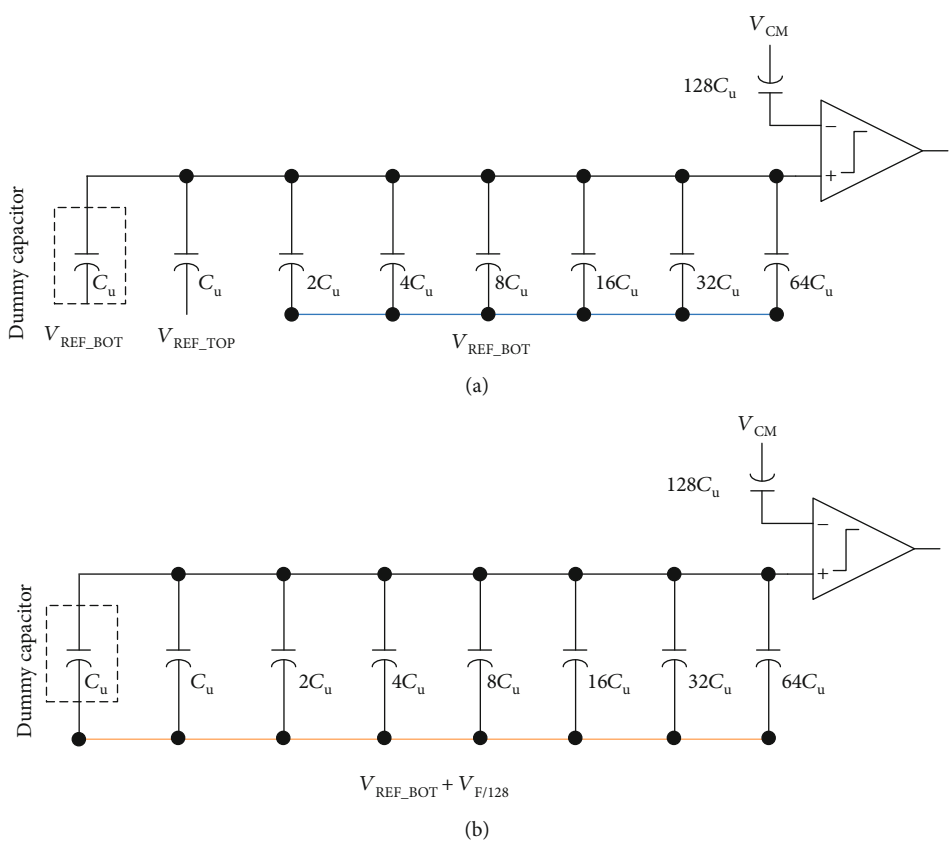


Figure 14: (a) $V_{REF\_BOT} + V_F/128$ calibration pattern 1 and (b) $V_{REF\_BOT} + V_F/128$ calibration pattern 2.

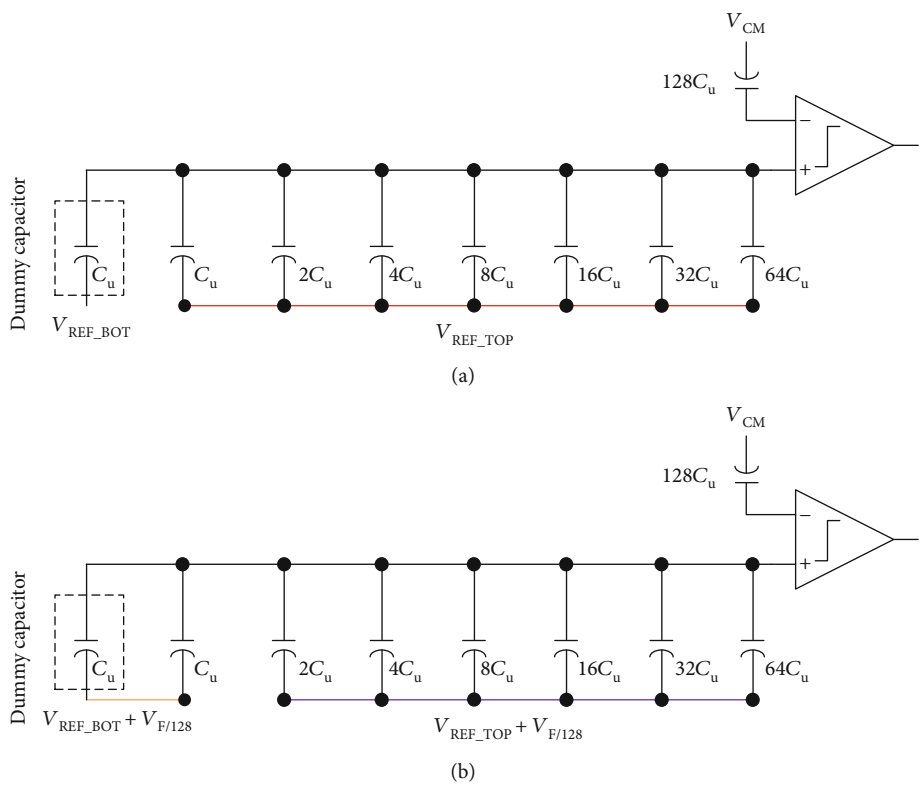


Figure 15: (a) $V_{REF\_TOP} + V_F/128$ calibration pattern 1 and (b) $V_{REF\_TOP} + V_F/128$ calibration pattern 2.

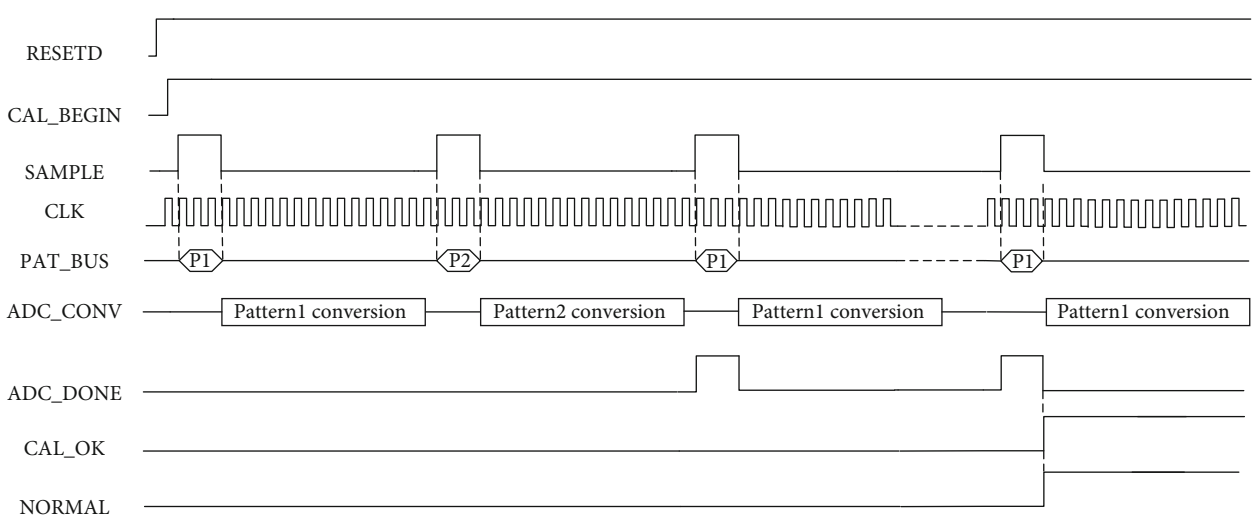


Figure 16: The timing block of calibration.

$$Q_{INC} = \frac{V_F}{128} \bullet \left(\sum_{n=6}^{0} \frac{1}{2^n} \bullet C_u \right) = \left(V_F - \frac{V_F}{128} \right) \bullet C_u. \quad (22)$$

According to equations (21) and (22), Q_{DEC} and Q_{INC} are equal, which means the value of V_{IN} does not change. At this time, the requirements of low 7-bit conversion are met. In order to explain the process, the comparison of 6th bit is taken for example. Because the low 7-bit conversion and high 7-bit conversion use the same capacitor array, the procedure is similar. What is more, the switch action of lower 7 bits is based on the high 7 bits. For instance, the conversion of 6th bit is related to 13th bit. If D_{13} is 0, which means the lower plate of the highest capacitance ($64C_u$) in the positive side is connected to V_{REF_BOT} and the lower plate of the highest capacitance ($64C_u$) in the negative side is connected to $V_{REF\_TOP} + V_F/128$, the connection voltage of lower plate of the highest capacitance ($64C_u$) in the positive side will increase by $V_F/128$ and the connection voltage in the negative side will decrease by $V_F/128$. The increased charge

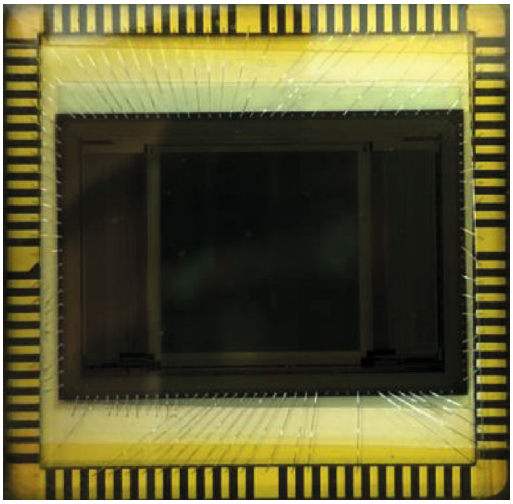


Figure 17: The photograph of the chip.

Q_{INC} and increased voltage of input signal ΔV are achieved:

$$Q_{\mathrm{INC}} = \left(\frac{V_F}{128} - \left(-\frac{V_F}{128}\right)\right) \bullet 64C_u = C_u \bullet V_F, \tag{23}$$

$$\Delta V = \frac{V_F}{128}. \tag{24}$$

If D_{13} is 1, which means the lower plate of the highest capacitance ($64C_u$) in the positive side is connected to $V_{\mathrm{REF\_TOP}}$ and the lower plate of the highest capacitance ($64C_u$) in the negative side is connected to $V_{\mathrm{REF\_BOT}} + V_F/128$. The process is similar to the situation of $D_{13} = 1$. The change on charge and the input signal are the same as well. The result of comparison determines the switch actions, which has been explained above. The voltage V_{D6} represented by the capacitor array during the process is calculated:

$$V_{D6} = -V_{\mathrm{IN}} + \left(-1 + \sum_{n=13}^{6} \frac{1}{2^{D_n}}\right) \bullet \left(V_{\mathrm{REF_{TOP}}} - V_{\mathrm{REF_{BOT}}}\right). \tag{25}$$

The last six bits adopts the same working process. Combining the conversion of high 7 bits and low 7 bits, the analog signal sampled by PGA is converted into 14-bit digital code.

The timing diagram of SAR ADC is shown in Figure 7. The reference clock is still ADC_CLK. The whole procedure occupies 18 ADC_CLKs. The 3 ADC_CLKs are used for sampling while 14 ADC_CLKs are adopted for comparison and the function of the last ADC_CLK is to output the results. During the comparison, the comparator begins to compare at the rising edge of ADC_CLK and latch the signal at the following edge of ADC_CLK. After latching the last comparison, the signal DATA_Ready turns to a high level and keeps on before the first ADC_CLK finishes.

3.2.2. Comparator. The comparator almost decides the speed of SAR ADC. In order to speed up the comparison, the StrongARM Latch topology is used, which is explained in [12]. The StrongARM latch topology is not only good at speed but also expert in saving power. The circuit is shown in Figure 8.

The StrongARM latch is based on positive feedback, which includes two working stages: reset phase and regeneration phase. At the beginning, the CLK is low. NM_1 and NM_2 are off while Node1 and Node2 are connected together to keep the same voltage for resetting. The output V_{op} and V_{on} are reset to the power supply voltage by PM_3 and PM_4, respectively. What is more, PM_1, PM_2, NM_4, and NM_5 are off. When in the regeneration stage, CLK is high and the current flows through NM_1 and NM_2. Assuming that $V_{\mathrm{ip}} > V_{\mathrm{in}}$, the current flowing through NM_1 is larger than NM_2, causing the voltage of Node1 to drop faster than Node2. When the voltages of Node1 and Node2 arrive at $V_{\mathrm{DD}} - V_{\mathrm{THN}}$, NM_4 and NM_5 turn on. Because Node1 first reaches $V_{\mathrm{DD}} - V_{\mathrm{THN}}$, V_{op} begins to drop, which also leads to the dropping speed of V_{op} slow down. Positive feedback is formed and V_{op} becomes V_{DD} finally. The loop gain A_p of the positive feedback loop is

$$A_p = \left(g_{\mathrm{mn4}} + g_{\mathrm{mp1}}\right) \bullet \left(r_{\mathrm{on4}} \| r_{\mathrm{op1}}\right) \bullet \left(g_{\mathrm{mn5}} + g_{\mathrm{mp2}}\right) \bullet \left(r_{\mathrm{on5}} \| r_{\mathrm{op2}}\right). \tag{26}$$

The voltage change of the whole process is shown in Figure 9.

In order to reduce the impact of input offset voltage and kickback noise, the preamplifier is adopted, the architecture of which is shown in Figure 10. The preamplifier uses Current Starving Technical [13] to increase the gain instead of using cascode structure. The small signal gain is calculated as follows:

$$A_v = \frac{g_{\mathrm{mn2}}}{g_{\mathrm{mp4}}} = \frac{\sqrt{2\mu_n C_{\mathrm{ox}} (w/L)_2 I_{dn2}}}{\sqrt{2\mu_p C_{\mathrm{ox}} (w/L)_4 I_{dp4}}} = \frac{\sqrt{\mu_n (w/L)_2}}{\sqrt{\mu_p (w/L)_4}} \bullet \frac{1}{\sqrt{1-K}}. \tag{27}$$

K represents the ratio coefficient of the current flowing through the NM_4 or NM_5, which determines the gain of amplifier. Aimed at making the resolution of latch shown in Figure 8 reach 0.5LSB, the gain of the amplifier requires at least

$$A_v = \frac{V_{\mathrm{OS,Latch}}}{1/2\mathrm{LSB}}. \tag{28}$$

The gain is related to $V_{\mathrm{OS,Latch}}$ closely. Based on the requirement of resolution and process characteristics, the three-stage operational amplifier is adopted.

The amplifier itself owns offset voltage, requiring the gain of the input stage maximized. The input offset voltage of the last two stages can be ignored when it is equivalent to the input. However, the offset voltages are still needed to be eliminated as much as possible, which is depicted in Figure 11.

The work of amplifier contains two phases: reset phase and amplification phase. In the reset phase, both input terminals are short to the common mode voltage V_{CM} through the

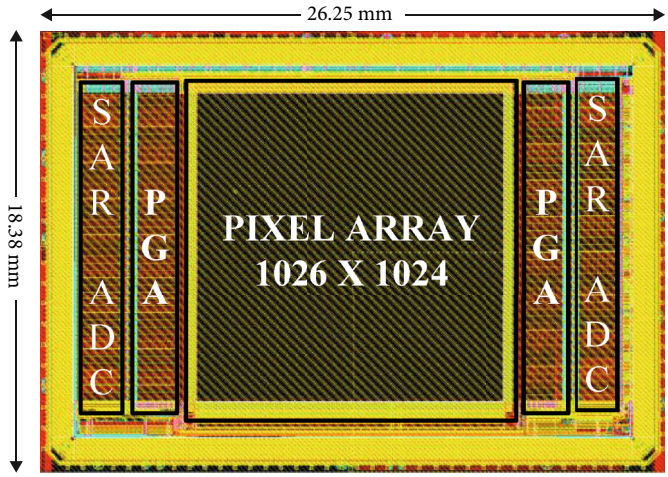


Figure 18: The layout of the chip.

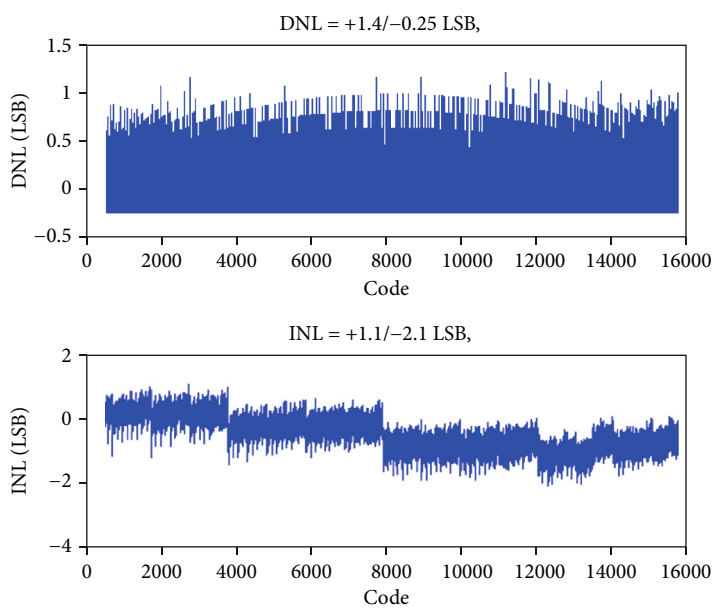


Figure 19: Static performance of SAR ADC.

switch when the two output terminals are also short to the V_{CM}. The output offset is stored in capacitor C_1 and C_2, which is the opposite to the input offset:

$$V_{os,out} = -A \bullet V_{os,in}. \tag{29}$$

When the amplifier enters the amplification stage, the switches connected to V_{CM} do not keep on and input signals V_{ip} and V_{in} connect to the input of amplifier. At this time, the output signal of amplifier can be obtained:

$$V_{out} = \left(V_{ip} - V_{in} + V_{os,in}\right) \bullet A - A \bullet V_{os,in} = \left(V_{ip} - V_{in}\right) \bullet A. \tag{30}$$

According to equation (30), the output does not contain V_{os}, which means the effect of offset voltage is eliminated. The complete comparator design is shown in Figure 12, including amplifiers, latch, and RS flip-flop. The three-stage preamplifier amplifies the input signal, and then, the amplified signal is compared by StrongARM latch quickly. The function of RS flip-flop is to output the results to the logic register.

3.3. Reference Voltage Self-Calibration Algorithm. The proposed architecture adopts a two-step scaled reference. The resolution of two reference voltages $V_{REF\_TOP} + V_F/128$ and $V_{REF\_BOT} + V_F/128$ is up to $V_F/128$, which is difficult for design. Once the accuracy of the reference voltage is far from the target value, the results of SAR ADC are greatly affected. The reference voltage self-calibration algorithm is applied to guarantee the required accuracy.

The proposed reference voltage self-calibration algorithm is based on the split capacitor linearity on-chip self-

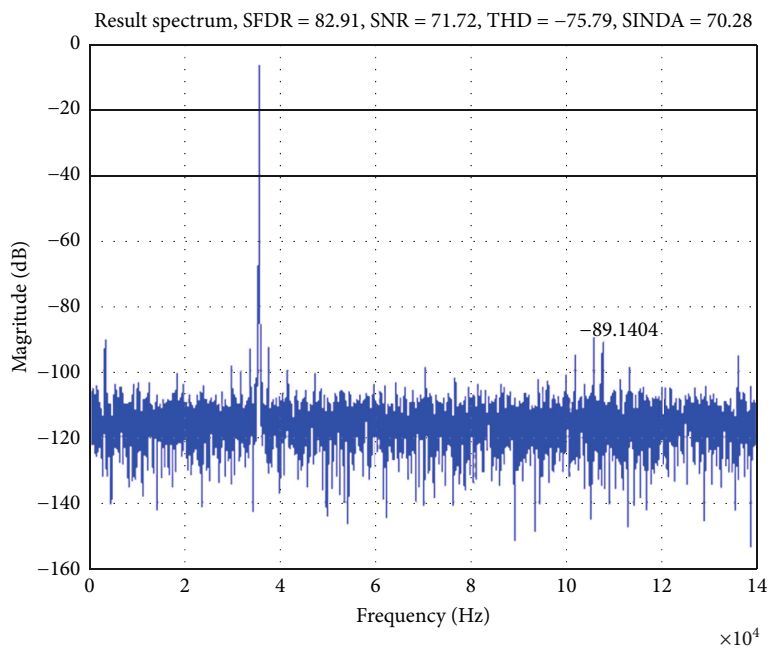


Figure 20: Dynamic performance of SAR ADC.

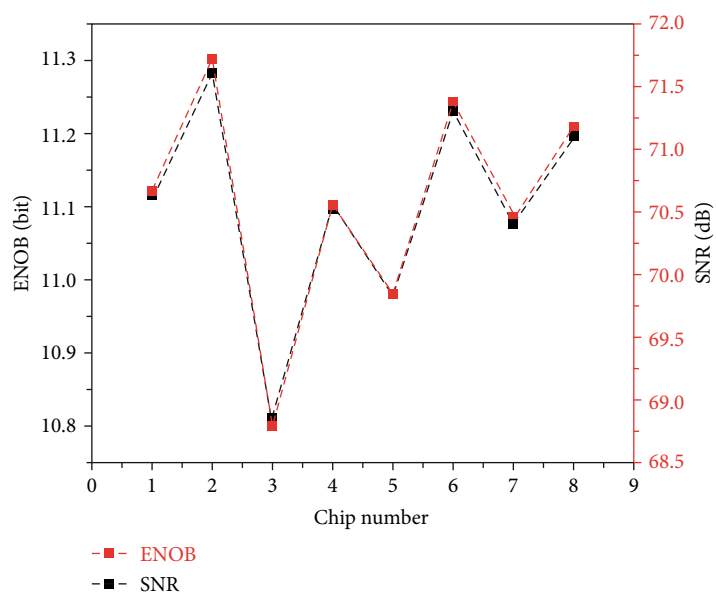


Figure 21: The measured SNR and ENOB of different chips.

calibration method proposed by Yoshioka et al. [14], which is to correct the output code by comparing the certain capacitors and the rest of all low capacitors. When the certain capacitance is consistent with the rest of all low capacitors, the calibration is finished.

Combining the correlated double sampling circuit technology and the above self-calibration method, the reference voltage self-calibration algorithm is proposed and the flowchart is shown in Figure 13.

The algorithm includes two patterns. Pattern 1 provides the relatively accurate target value when pattern 2 represents the value to be corrected. Two-step scaled reference is used in the process. The reference voltages $V_{\text{REF\_TOP}}$ and $V_{\text{REF\_BOT}}$ are the precise voltages, which generate $V_{\text{REF\_TOP}} + V_F/128$ or $V_{\text{REF\_BOT}} + V_F/128$ by DAC. The $V_{\text{REF\_TOP}} + V_F/128$ or $V_{\text{REF\_BOT}} + V_F/128$ in pattern 2 is the internally generated voltage, which is a rough value and needs to be corrected.

The precise voltages and rough voltages are converted into digital code through ADC. The difference between precise voltages and rough voltages determines the action of counter. Once the difference is equal to zero, the calibration is finished. If the difference is not equal to zero, the counter

(a) (b)

Figure 22: Captured photos by the CIS.

Table 2: Performance summary of the prototype.

Parameter	Value
Process	180 nm CMOS process
Analog supply	3.3 V
Digital supply	3.3 V
ADC	
Resolution	14 bits
Sample rate	150 kSps
Input range	-2.4 V ~ +2.4 V
DNL	+1.4/-0.25LSB
INL	+1.1/-2.1LSB
SNR	71.7 dB
SFDR	82.91 dB
SINAD	70.28 dB
Power consumption	477.2 uW
PGA	
Gain	3x, 4x, 6x
CIS	
Frame rate	50 fps
Pixel number	1026 × 1024
Pixel pitch	12.5 μm × 12.5 μm
Temporal noise	13.6 e_{rms}
Total power	613 mW

will add one or minus one and the output of DAC will get closer to the target value.

The capacitor array of $V_{REF\_BOT} + V_F/128$ calibration pattern is shown in Figure 14 when the capacitor array of $V_{REF\_TOP} + V_F/128$ calibration pattern is shown in Figure 15. Both work on the same principle, but the output of DAC in the $V_{REF\_TOP} + V_F/128$ calibration is limited. For a differential ADC, the single-ended voltage can only reach V_{REF_TOP}. If the lower plates of capacitors are connected to the $V_{REF\_TOP} + V_F/128$, the results of ADC will exceed the conversion range, which is not accurate.

Assuming that the error of A/D conversion is ±1LSB, the digital code D_1 in pattern 1 is equal to 00000010000000 when correcting $V_{REF\_BOT} + V_F/128$. If the reference voltage is provided from a relatively small value by pattern 2, the digital code will keep on the 00000010000000, which is not consistent with the real value. However, the D_1 is equal to D_2, which means the calibration has finished. During the process, the reference voltage self-calibration algorithm does not take on the job, so the reference voltages should change from a large value and the calibration of $V_{REF\_TOP} + V_F/128$ is the same as well.

Figure 16 shows the timing block of calibration. PAT_BUS is the bus signal that controls the DAC capacitance switch. When the system is powered on, the signal RESETD resets the digital circuit and then the signal CAL_BEGIN jumps to the high level, which means the calibration module begins to work. The timing of A/D conversion is the same as SAR ADC. A single complete calibration cycle includes 2 settings of switch mode and 2 A/D conversions. Once the second conversion is finished, the signal ADC_DONE will turn to a high level. The compared results of two conversions determine the state of calibration.

If the calibration is over, the signal CAL_OK becomes a high level, which represents the work of one reference voltage calibration has been finished. If the signal CLK_OKs of two references are high level, the whole calibration will be finished and the signal NORMAL will turn to a high level as well.

4. Experimental Results

The CMOS image sensor is fabricated in the 180 nm CMOS process, which is used in remote sensing. Referring to the capacitor array, MIM capacitors are chosen, which have a better match and less affected by temperature compared with others. The pixel array is 1026 × 1024, and the pixel pitch is

Table 3: The comparison of previous work.

Parameter	This work	JSSC 16 [15]	TED 16 [16]	ISSCC 18 [17]	JSSC 19 [18]
Process (nm)	180	180	90	90	65
ADC type	SAR	SAR	SAR	SAR	SAR
Supply voltage (V)	3.3	2.8/1.8	2.8/1.2	1.8/1	3.4
Number of pixel	1026 × 1024	160 × 120	1696 × 1212	2560 × 1536	792 × 528
Pixel pitch (μm)	12.5	4.4	1.12	1.5	1.5
Frame rate (fps)	50	100	60	60	170
Resolution (bit)	14	10	12	10	10

12.5 μm × 12.5 μm. The photography of the chip is shown in Figure 17 and the layout of the chip is shown in Figure 18, which are consistent. The pixel array is put in the center of the chip while the readout circuits are placed on the left and right sides. The whole area of the chip is 26.25 × 18.38 mm^2, where the pixel array occupies the main area.

When it comes to SAR ADC, the performance contains static performance and dynamic performance. Due to the combination of PGA and SAR ADC, the performance of SAR ADC is affected by PGA and the following presentation includes the effect of PGA. The static performance is shown in Figure 19. The DNL is +1.4/-0.25 LSB and the INL is +1.1/-2.1 LSB, which reflects the transient noise. At the sampling speed of 150 kS/s, the SNR and SFDR of the SAR ADC are 71.72 dB and 82.91 dB, respectively, when the frequency of the input signal is 33.3 kHz, which is shown in Figure 20. What is more, the THD of SAR ADC is -75.79 dB and the SINAD is 70.28 dB. In order to verify the stability performance of the proposed prototype, eight chips are tested to get the data, which is presented in Figure 21. The SNR of SAR ADC is from 68.78 dB to 71.71 dB when the ENOB is from 10.8 bits to 11.3 bits, whose performance is relatively stable. The single SAR ADC consumes 477.2 uW.

Figure 22 shows the photos captured by the proposed CIS chips, in which the edge of the subjects can be clearly recognized. What is more, the depth of the background color can be clearly identified, which means the CIS have a good resolution. The performance summary of the prototype is listed in Table 2, including SAR ADC, PGA, and the CIS. The total power consumption of the CIS is about 613 mW.

Compared with the previous works, which are depicted in Table 3, this work adopts the large pixel array and the resolution of SAR ADC is comparatively high without the help of complex calibration and the advanced technology. The proposed CIS chip keeps a balance between the area, resolution, and speed.

5. Conclusions

The 14-bit fully differential SAR ADC with PGA is proposed to apply on CIS. In this paper, the scale of pixel array is large when the three-way PGA is used to sample at the same time to increase the speed. What is more, it also provides three types of gain: 3x, 4x, and 6x. Considering the reset and exposure signal, the fixed deviation is added into the PGA, which makes the input signal distributed evenly on the positive and negative sides. When it comes to SAR ADC, the two-step scaled-reference voltages are adopted to realize the goal of 14-bit A/D conversion with a 7-bit complementary capacitor array, which is aimed at reducing the number and the area of capacitors. In order to make the precision of reference voltage meet the requirement, the reference voltage self-calibration algorithm is used. During the whole process, the offset and matching accuracy needs to be considered as well. By finishing the above design, the readout circuit realizes the function well and the proposed CIS achieves the goal of high resolution for remote sensing, which are verified in the manufactured chips.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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Research Article

Design of a CMOS Lineal Hall Sensor Front-End Working in Current Mode with Programmable Gain Stage for Power Specific Chip

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With the continuous intelligentization of power systems, the demand for the integration of digital chips and sensor chips such as the Internet of Things is also increasing. A CMOS lineal magnetic Hall sensor front-end working in current mode with programmable gain stage is designed and implemented with SMIC 55 nm standard CMOS technology. By using a spinning-current technique, chopper technique, and digital calibration technique to eliminate the offset voltage and nonlinearity, this magnetic Hall sensor can be easily integrated into digital systems like SoCs. This work has already finished the circuit simulation and layout design, and all simulation indicators basically reach the expected value. The maximum gain of proposed sensor systems can be up to 33.9 dB. The total power is less than 4 mW. And the total area is less than 0.113 μm^2. The magnetic Hall sensor can be easily integrated into chips such as the power Internet of Things to form a single-chip-level SoC design, which is mainly used in applications such as circuit breakers and electric energy measurement.

1. Introduction

With the rapid development of very large-scale integrated circuits, various new types of equipment and various digital chips used in power grids and related digital-analog hybrid sensor chips are also emerging. Commonly used special control chips for power Internet of Things generally have an integration level only to the digital-analog/analog-to-digital converter level, and the corresponding sensor part still needs to be connected to an off-chip chip. Considering the realization of the overall function of the system and the realization of sufficient performance at a relatively low cost, SoC (System on Chip) design has gradually become the mainstream. On the premise of meeting standard CMOS silicon process manufacturing, many of the off-chip sensor circuit parts have already been integrated into the SoC to form a single-chip-level design. Hall sensor is one of which is easy to integrate with standard CMOS process. As a part of the special chip for the power Internet of Things, it can measure the current inside the line without contact by measuring the magnetic induction near the power line, which can be applied to various occasions such as circuit breakers and energy measurement.

Hall sensors are widely used in automotive and industrial applications such as current measurement, angle detection, and position detection. Hall sensors are preferred because of their low cost, low power, wide range, high sensitiveness, and great compatibility to standard CMOS. As the sensors are not fabricated in dedicated technology, they also suffer from sensitivity drift and offset in Hall plate. Usually, offset can be eliminated by spinning-current and chopper techniques. The sensitivity drift can be compensated by a look-up table, analog compensation technique, or digital calibration technique. The look-up table is the simplest way for sensitivity drift compensation, but the performance is poor. The analog compensation technique can have better performance

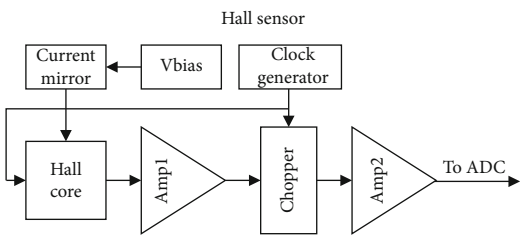


Figure 1: Main structure of Hall sensor front-end.

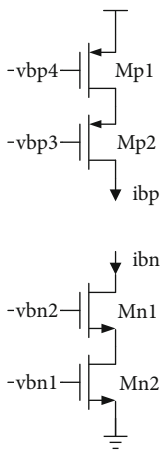


Figure 2: A pair of wide swing cascade current mirrors.

but leads to higher complexity and implementation cost. The digital calibration technique is preferred because it outperforms the look-up table and it is easy to implement in a digital domain with an elaborately designed calibration algorithm.

2. Materials and Methods

The main structure of the proposed Hall sensor system is presented in Figure 1. It consists of a Hall core, a current mirror and its bias, two stages of a differential amplifier, a chopper circuit, and a clock generator.

In this design, the Hall device is biased by a pair of current mirrors to produce a pair of differential Hall voltage. The differential Hall voltage is amplified by a differential amplifier Amp1 with constant gain. Then, the output of Amp1 goes through the chopper circuit to eliminate the offset voltage of the Hall plate. After the amplification of Amp2 with programmable gain, the final output is sampled and measured by a 16-bit 1MSps ADC, then processed in a digital domain. The clock generator produces different clocks for the Hall core to realize the spinning-current technique and for chopper to reduce Hall offset voltage. The detail of each block will be discussed below.

2.1. Current Mirror and Vbias. The Hall core is biased with 100 μA constant current to produce a stable Hall voltage. To get lower common-mode voltage of Hall voltage, a pair of current mirrors is implemented separately by PMOS and NMOS using a wide swing cascade structure. Figure 2 shows the details of current mirrors where nodes vbp4 to vbn1 come from Vbias circuit.

The Vbias circuit provides nodes from vbp4 to vnb1 for current mirrors. That is, it is basically a constant-Gm structure which can provide satisfying immunity to power supply [1].

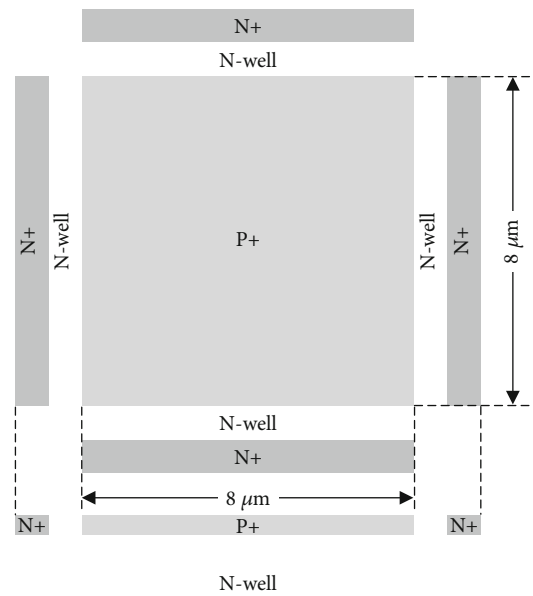


Figure 3: An N-well Hall device with geometry of 8 μm.

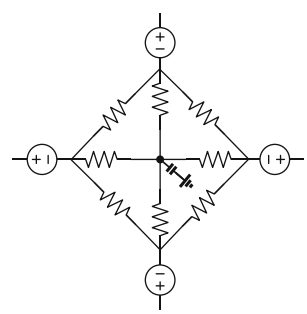


Figure 4: Simulation model of Hall device.

2.2. Hall Core. The Hall core consists of a Hall device or so-called Hall plate and 8 switches. The Hall device is implemented with an N-type semiconductor, to be more explicit, the N-well region. Figure 3 demonstrates the typical geometry of the Hall device. Common types of Hall plate include rectangle, bridge, and cross. In this design, a cross type is chosen, and a P+ region is added on the top of N-well to get rid of the effect from the upper circuit.

Figure 4 shows a Hall plate model for circuit simulation. And its basic framework still adopts the most basic Wheatstone bridge structure [2, 3]. The four resistors on the arm represent the N-well diffusion resistance of the four interdigital regions. The four resistors in the middle represent the resistance in the central region of the Hall plate. The capacitor serves as the parasitic capacitance at the contact hole to simulate the transient response of the Hall plate. And the

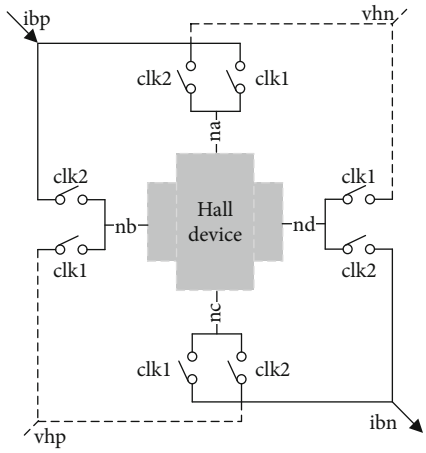


Figure 5: Structure of Hall core using spinning-current.

four current controlled voltage sources are used to simulate the Hall effect and controlled by the current flowing through the contact hole. The output voltage of this model varies from magnetic field intensity dynamically. For example, it can produce a pair of 84 μV differential Hall voltage, accompanied with 96 μV offset voltage under 10 mT@20 kHz. The circuit of this model is shown.

To eliminate the Hall offset voltage introduced by geometry asymmetry, we employ the spinning-current technique in the Hall core circuit by using 8 switches [4–8]. Figure 5 presents the basic structure. The clocks of 8 switches are 50% duty cycle square wave and can be up to 50 MHz. The phase between clk1 and clk2 is 180°. The current direction is from ibp to ibn. It works in 2 different phases.

In the first phase, the bias current flows from node na to node nc; thus, differential Hall voltage V_{sensor} is generated from node nb and node nd:

$$V_{\text{sensor}[1]} = V_{\text{Hall}[1]} + V_{\text{off}[1]}. \quad (1)$$

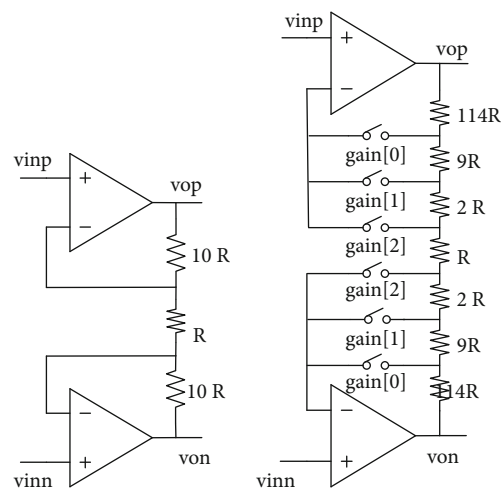
In the second phase, the bias current flows from node nb to node nd; thus, differential Hall voltage V_{sensor} is generated from node nc and node na:

$$V_{\text{sensor}[2]} = V_{\text{Hall}[2]} - V_{\text{off}[2]}. \quad (2)$$

If the switching frequency of the current direction is far greater than the change frequency of the magnetic field, then the magnetic field is approximately unchanged in these two phases. By subtracting the voltage obtained from these two phases, the differential Hall voltage becomes

$$V_{\text{sensor}} = V_{\text{sensor}[1]} + V_{\text{sensor}[2]} = 2V_{\text{Hall}} + \Delta V_{\text{off}}. \quad (3)$$

Using the rotating current technology with n ports and n phases can further reduce the offset voltage, but it will increase the complexity of the system and limit the working speed of the system. It is necessary to coordinate the relationship between the system speed and the offset voltage.



(a) Structure of Amp1 (b) Structure of Amp2

Figure 6: The structure of adopted differential amplifier.

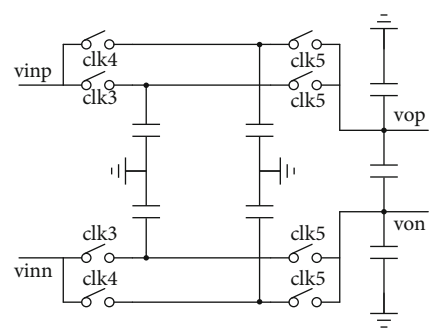


Figure 7: Chopper circuit structure.

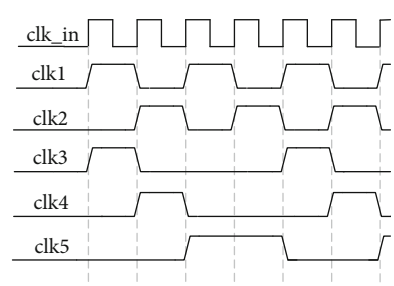


Figure 8: Phase diagram of the clock generator.

2.3. Differential Amplifier. The Hall effect is very weak. And the output Hall voltage of the modulation module is very small, which is in the order of μV~mV. Therefore, it must be amplified before demodulation. The differential amplifier consists of two single-ended operational amplifiers and several resistances. Since the output signal of the Hall disk is weak, the first stage of the gain adjustable amplifier needs low noise and high input impedance. For Amp1, a two-stage folded-cascode optional amplifier with Miller compensated is used in this design. For Amp2, three switches are used to obtain programmable gain. The detailed structure of Amp1 and Amp2 is shown in Figures 6(a) and 6(b). With such implementation,

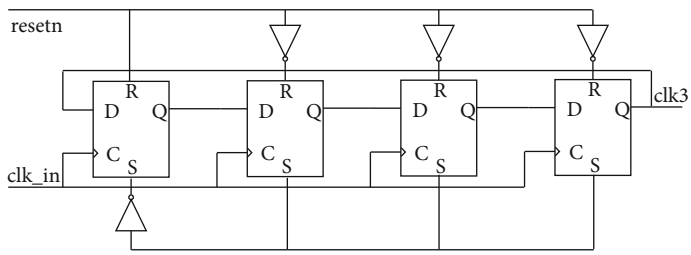


Figure 9: Ring D flip-flop structure.

Table 1: Parameters of 5 clocks.

	T_{rise}/ps	T_{fall}/ps	Duty	T (min)/ns
clk1	27.1	28.9	50 ± 0.1%	20 ± 0.02
clk2	27.9	28.8	50 ± 0.1%	20 ± 0.02
clk3	24.8	27.1	25 ± 0.1%	40 ± 0.04
clk4	24.5	27.2	25 ± 0.1%	40 ± 0.04
clk5	27.4	28.8	50 ± 0.1%	40 ± 0.04

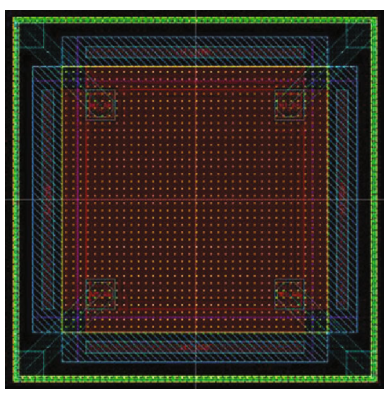


Figure 10: Layout design of Hall device.

Amp1 can provide a gain of 20, and Amp2 can provide a gain of 250/49.2/9.1 when gain[2]/gain[1]/gain[0] are enabled separately. The power supply of the operational amplifier implemented is 2.5 V, and the static power consumption is 370 μA. The open-loop gain is up to 80 dB. And the open-loop cutoff frequency is 200 MHz [9–11].

2.4. Chopper. The chopper circuit is designed between Amp1 and Amp2 to reduce the offset voltage of the Hall device by integrating Hall voltage vhp and vhn in two clock phases [12]. The chopper circuit is implemented with several capacitors. The detailed structure is shown in Figure 7. And clocks clk3 to clk5 are also generated by the clock generator. In the clk3 phase, $V_{sensor[1]}$ is stored on the capacitor. Then, in the clk4 phase, $V_{sensor[2]}$ is stored on the capacitor. In the clk5 phase, $V_{sensor[1]}$ and $V_{sensor[2]}$ are integrated on the output capacitor. As long as the ratio of input capacitance and output capacitance is controlled to be 2 : 1, the value of output capacitance is V_{Hall}.

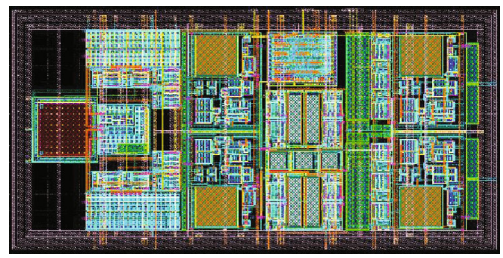


Figure 11: Layout design of the proposed Hall sensor system.

2.5. Clock Generator. The clock generator generates 5 clocks for the Hall core and chopper circuit [13]. The phase diagram of these clocks is presented in Figure 8. The parameters of these clocks are of vital importance. Thus, with ring D flip-flop structure and digital synthesis technique, these parameters can be strictly precise. Figure 9 shows the ring D flip-flop structure of the clock generator (for example, clk3), and Table 1 lists the parameters of these clocks.

3. Results and Discussion

This work has already finished the circuit simulation and layout design. The layout design of the proposed Hall plate is shown in Figure 10. And the layout design of the entire system is shown in Figure 11. The simulation results show that the proposed Hall sensor system can amplify a 168 μv (Vpp) Hall voltage (with 96 μv offset) to 414 mv (with -27 mv offset). By using the proposed Hall sensor system, the Hall voltage is amplified by 2460 times.

The performance summary is given in Table 2 (*The sensitivity is related to the Hall device model).

4. Conclusions

The simulation results show that the Hall sensor system front-end is capable of amplifying Hall voltage and reducing offset voltage. While integrated with ADC, the Hall voltage data can be easily processed with CPU or DSP. At the same time, since the design of the sensor system is based on the standard SMIC 55 nm process, with the necessary digital control logic and ADC part, the design is easy to integrate into the corresponding power specific SoC chips. The advantage of our Hall sensor system is small area consumption and easily integrated with SoC chips. And due to very high frequency spinning current technique, this Hall sensor system

Table 2: Main parameter compared with related work.

	This	[14]	[15]	[16]	Unit
Tech	55	180	350	180	nm
Plate size	8×8	8×8	/	/	μm^2
Num of plates	1	2	4	4	
Spinning frequency	50M	250k	20k	1k	Hz
Area	0.113	1.16	11.55	/	μm^2
Power	4	0.12	3.3	1.6	mW
Sensitivity	4.14 V/m*	1.6 V/A/T	50 mA/T	50 mV/T	
Nonlinearity	*	0.2%	0.8%	/	%
Offset	65 μT	50 μT	40 μT	25 μT	μT

can process up to 100 kHz alternating magnetic field with no more than -3 dB attenuation.

In this paper, a lot of work has been carried out on CMOS Hall device design optimization, offset elimination, and signal amplification circuit technology, as well as Hall device simulation modeling and other aspects. Though we have obtained some meaningful results, there are still some deficiencies. The future plan involves the following directions.

We have mainly adopted the dynamic offset elimination technology of two-phase spinning-current. However, the residual offset is still high, which is due to the sensitivity of the Hall device to the fluctuation of the manufacturing process and junction field effect. We will use the four-phase spinning-current technology combined with the fully symmetrical structure of the Hall device design to improve the ability of eliminating the Hall device offset and obtaining lower residual offset. In addition, the negative feedback technology will be applied to the signal conditioning circuit to reduce the residual offset caused by the signal conditioning circuit itself. The mechanical stress compensation technology in a chip will also be explored to eliminate offset caused by mechanical stress after packaging.

Data Availability

The raw/processed data required to reproduce the results obtained in this study cannot be shared at this time because they are used in an ongoing study.

Conflicts of Interest

The authors declare no conflict of interest.

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Research Article

Power Management in Low-Power MCUs for Energy IoT Applications

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In this paper, we identify and address the problems of designing effective power management schemes in low-power MCU design. Firstly, this paper proposes an application-based multipower domain architecture along with a variety of working modes to effectively realize the hierarchical control of power consumption. Furthermore, devices in energy IoT (eIoT) do not always work under the main power supply. When the main power supply is unavailable, the standby power supply (usually the battery) needs to maintain the operation and save the data. In order to ensure the complete isolation between these two power sources, it is always necessary to insert a diode in both select-conduction paths, respectively. In this paper, we built a stable and smooth power switching circuit into the chip, which can effectively avoid the diode voltage loss and reduce the BoM cost. In addition, in the sleep mode, considering the relaxed output voltage range and a limited driving capability requirement, an ultra-low-power standby power circuit is proposed, which can autonomously replace the internal LDO when in sleep, further reducing the sleep power consumption under the main power supply. Fabricated in a standard 0.11 μm CMOS process, our comparative analysis demonstrates substantial reduction in power consumption from 1 μA to 0.1 μA.

1. Introduction

The rapid growth of the energy Internet of Things (eIoT) has driven the vigorous development of microcontrol units (MCUs) [1–3]. In order to provide a lower cost solution, more and more functions are integrated in MCUs: networking, high-efficiency sensor interfaces, etc., which makes the low-power design challenging. Moreover, the application scenarios of eIoT are more complex due to multiple power domains, making low-power design a complex task.

The eIoT is an intelligent system integrating distributed and scalable renewable energy sources and Internet technology with the existing smart grid [4–6]. By controlling the energy flow through the information flow, an overall information transmission and exchange platform is built. The platform connects end users and power supply station, realizing information sharing and transparency and therefore forming an energy ecosystem. The development trend of eIoT is inseparable from the MCU market. Whether it is a small node for connection or a sensor hub for collecting and recording data, it is mainly based on the MCU platform [7, 8].

As the one of the key parts, power management in an MCU for the eIoT is quite challenging [9, 10]. Firstly, the MCU for the eIoT usually has multiple supply domains. For example, apart from the normal supply source, MCUs for smart meters also have a battery supply. Furthermore, the real-time clock (RTC) block is required in the MCU for energy metering. It needs to be working uninterrupted when the meter is in storage or under the power outage. The power dissipation becomes critical for the RTC powered by a battery. Sometimes, the MCU is even required by utility regulations to have a separate RTC power domain. Due to the multiple supply domains, the MCU for eIoT should be compatible with a large supply voltage range of 2.2 V to 5.5 V. Switching among different supply domains with high reliability is also challenging for power management in the MCU. In addition, to extend the battery life, traditional

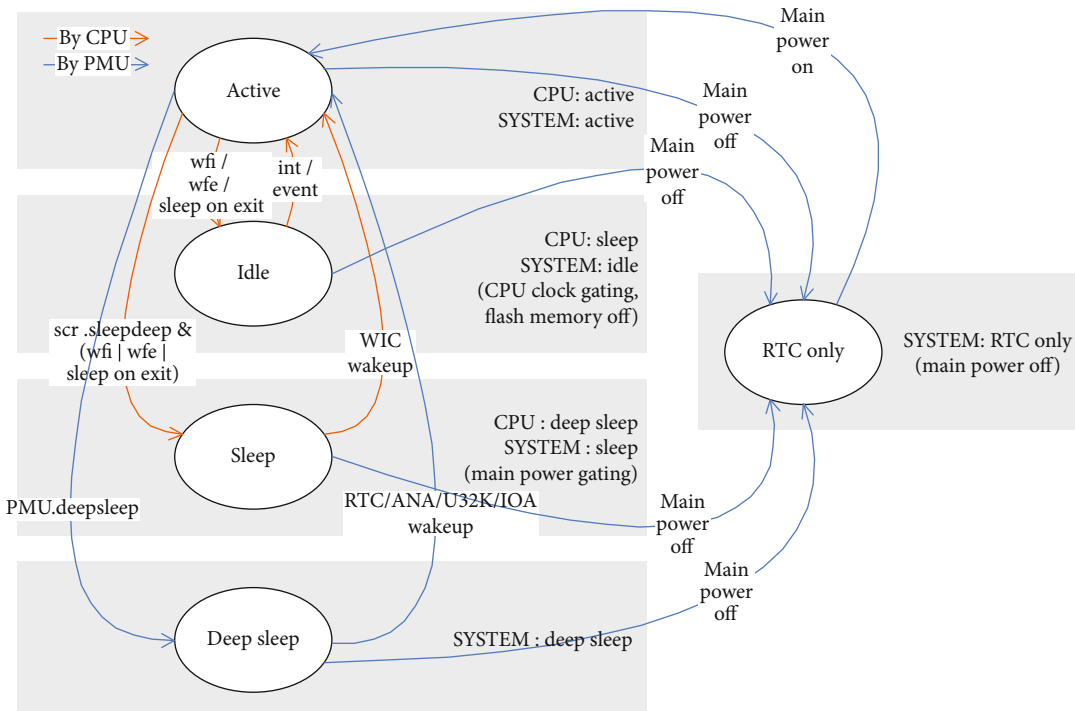


Figure 1: Power state flow chart of the low-power MCU.

techniques such as clock gating and power gating [11] can be used to reduce the power consumption of the digital and analog cores; however, the power consumption of the always-on power management circuits, such as low-dropout regulator (LDO), should be minimized to extend the battery life. At the same time, they should be able to provide a large load current up to 30 mA for the normal working mode.

State-of-the-art ultra-low-power MCUs on the market can achieve submicrowatt power consumption in low-power mode; however, they can only supply a single standard 3.3-V supply voltage [12], which requires additional power switching circuit on-board, increasing the design cost for eIoT applications. As for the LDO in the MCU with large load current as well as low quiescent current, a digitally adaptive LDO scheme is proposed in [13]; however, the driving ability of 2.56 mA is not enough for MCUs in eIoTs and its 650 nA quiescent current also limits the further reduction of the power consumption.

To solve the above issue, the paper proposes several techniques for power management in the low-power MCU for eIoT with low cost and high reliability. Firstly, the application-based multimode switch scheme along with a multipower domain strategy is proposed to optimize the power consumption through a hierarchical control. In addition, we integrate the traditional power switch function into the chip, effectively reducing the system cost and extending the battery life. In order to further reduce the power consumption in the sleep mode, we design an ultra-low-power backup power supply circuit in lieu of the traditional LDO in the sleep mode, reducing the power to 0.1 μA.

The paper is organized as follows. Section 2 introduces the architecture of the power management system in the MCU for the eIoT. Section 3 describes the proposed ultra-low-power backup LDO circuit design, followed by measurement results in Section 4. Section 5 concludes the work.

2. Design of Low-Power Supply System with High Reliability

In order to effectively simplify the peripheral circuit design and prolong the battery life, the independent power supply mechanism of the RTC and the corresponding main power supply, battery power supply, RTC power supply, and other multipower domain switching strategies and multiple low-power operation modes are designed.

2.1. Application-Based Multimode Switching Scheme. In view of the complexity characteristics of the of eIoT applications, five working modes are designed according to the different applications of the MCU, namely, active, idle, sleep, deep sleep, and RTC-only, to reduce the power consumption of the chip. Take the energy meter as an example [14]: the active mode is applied when the meter is running normally; the sleep mode is used in scenarios where the meter is powered by battery supplies during a power outage; the deep sleep mode can further reduce power consumption of the sleep mode shutting down more functions; and the RTC-only mode is suitable for extremely low power running when the meter is placed in the warehouse and not yet mounted [15]. The switching of these five working modes is shown in Figure 1.

The idle and sleep modes are directly controlled by the MCU core, and users only need to execute specific instructions to enter in or out of these modes. The control of the

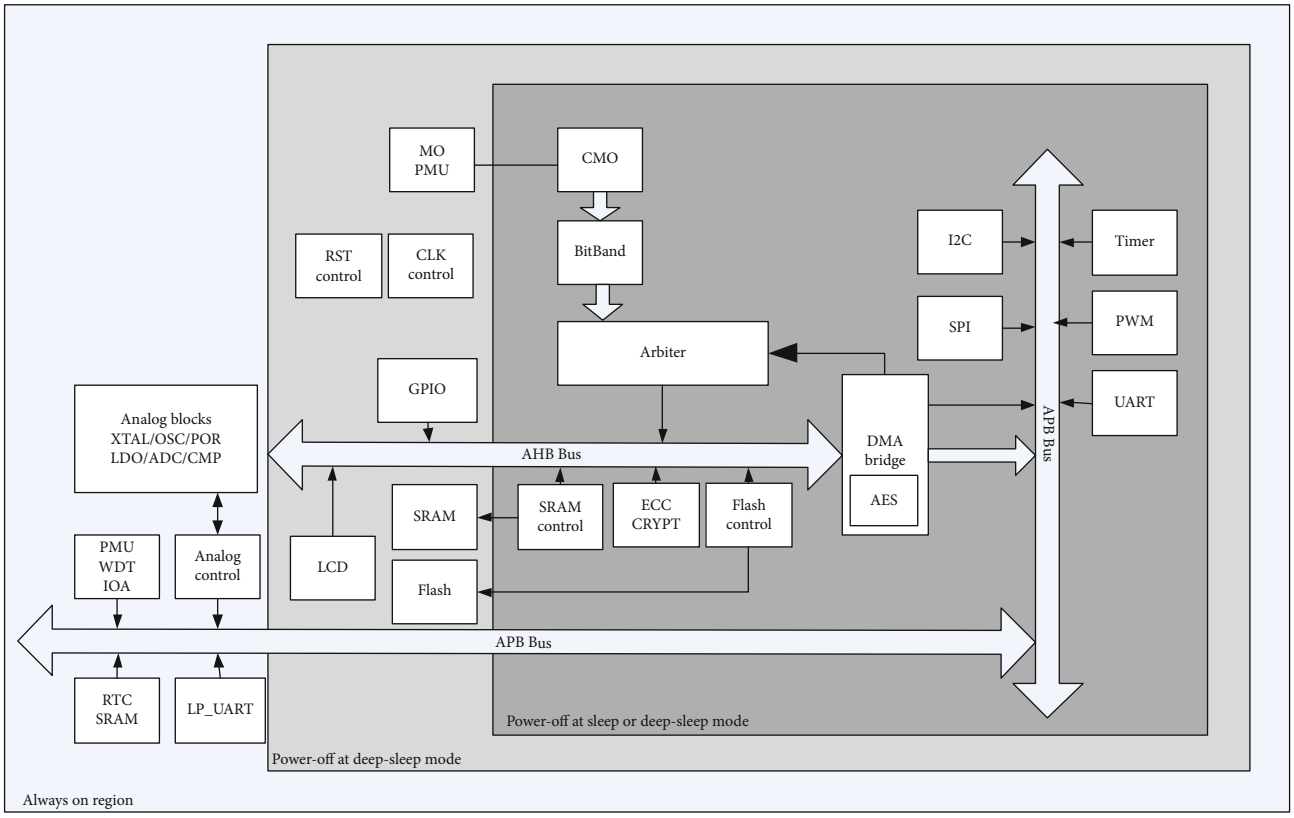


Figure 2: System functional block diagram.

deep sleep and RTC-only modes is realized through the power management unit (PMU). By reading the value of the control register written by the software, the PMU controls the hardware state machine to switch between different modes. The involved operations include the power gating and clock gating of the corresponding modules [16, 17] and the isolation of different power domains. To explain different modes, we show the system functional block diagram in Figure 2 with power domains. The specific working status of different modes is as follows:

(1) Active

This mode is the normal working mode of the MCU. In this mode, the chip works at the PLL clock or internal high-frequency RC clock, the CPU core is turned on, and the functional modules, interfaces, and peripherals can all be turned on and configured through the software.

(2) Idle

In this mode, the CPU is stopped, but the high-speed peripherals remain monitoring and can be quickly awakened by any interruption.

(3) Sleep

In this mode, the CPU and most functional modules are turned off. Only SRAM, PMU, GPIO, etc. are working. As shown in Figure 2, the dark gray part is powered off. The high-frequency clock is turned off. The chip works using the low-frequency clock RTCCLK.

Table 1: Power supply in different modes of the chip.

MODE	Main power domain		RTC domain
	VDD	BATVDD	BATRTC
Active	V		
Idle	V		
Sleep		V	
Deep sleep		V	
RTC-only			V

(4) Deep sleep

In this mode, the CPU and all peripherals are powered down, and only the interrupting IOs, RTC, PMU, and UART32K (low-power UART module) modules are active. As shown in Figure 2, the light gray part is also powered off.

(5) RTC-only

All main power supplies are powered down, and only the RTC circuit powered by BATRTC maintains operation in this mode, as shown in the blue part in Figure 2.

For energy meters, the power supplies in different modes are also different, as shown in Table 1. In normal mode, the chip uses the main power supply VDD. It is usually supplied by a rectifier bridge and an LDO. In this power supply

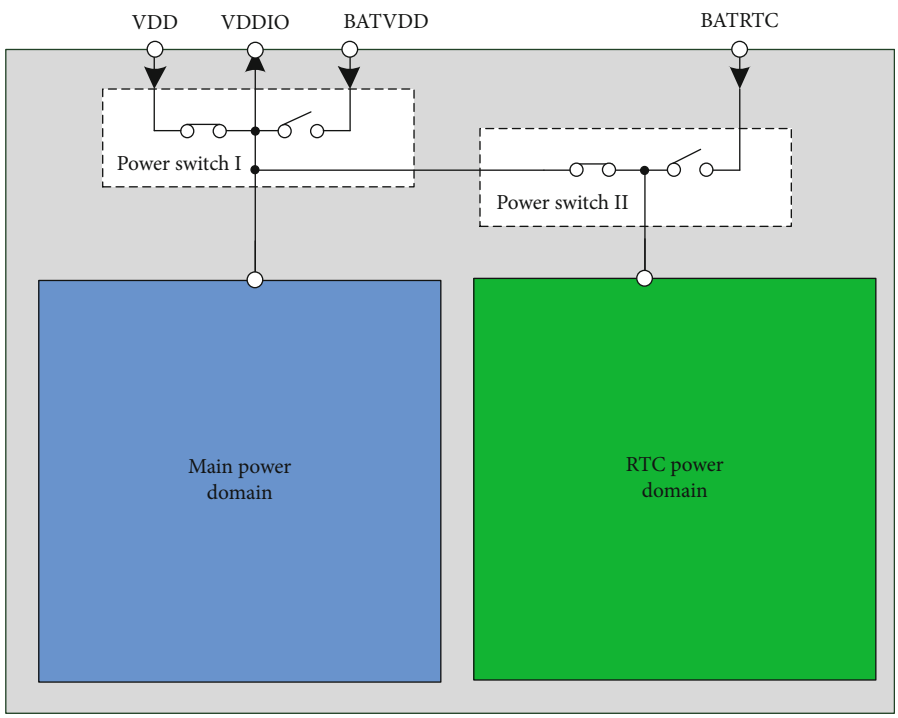


Figure 3: Independent power supplies for multiple power domains.

situation, the chip can also enter the idle mode to save energy. When the main power is off, such as in the case of storage or power outage, the battery will be activated as a backup power source to maintain the basic function of the chip. The chip then transitions into the sleep or deep sleep mode. The RTC must be accurate under all conditions. Therefore, a special RTC power domain is designed. It is powered by another separate battery and kept always on. When the main power domain is completely powered off, the chip enters the RTC-only mode.

2.2. Built-In Power Switching with High Reliability. As shown in Figure 3, the power architecture of the chip is divided into two parts. One is the main power domain, under which most functional modules such as the CPU, memory, and peripherals are placed. The other is the RTC power domain. This domain has the always-on circuits such as the crystal oscillator clock and RTC module. Except for in the RTC-only mode, the main power domain is always on. When the utility power is present, it is powered by the utility power, and during a power outage, it switches to the battery power. Usually, this switching is done off-chip. As shown in Figure 4(a), in order to prevent the reverse current, the regulated main power and the battery are, respectively, connected in series with a diode and then supplied to the chip's supply input VDD. Generally, the voltage of the regulated utility power is higher than that of the battery, so the chip is powered by the utility power. In addition to the BOM cost of the diode, this scheme also has a disadvantage of the diode voltage drop. The diode voltage drop can reduce the battery usage range.

To solve this issue, this work proposed a built-in power switching with high reliability. In this design, the main power domain is changed from the traditional single-power input (VDD in Figure 4(a)) structure to a three-power structure, including the main power input VDD, battery input BATVDD, and IO power (the main power supply of the chip generated after the power selection). When implemented, as shown in Figure 4(b), VDD and BATVDD are connected to VDDIO through a MOSFET switch, respectively, and the control logic ensures that only one switch is turned on at a given time. VDDIO is connected to VDD by default. VDD is divided by a series of resistors and then connected to the hysteresis comparator for the voltage detection. When VDD is lower than the switch threshold, VDDIO is switched to the battery. To address potential reliability issues during usage, the switching circuit is designed carefully as follows.

In most cases, the VDDIO voltage is close to the higher of these two inputs. Considering that the voltage of VDD may be 3.3 V or 5.0 V, while that of BATVDD is usually 3.6 V (at full capacity), the bulk of the two switch MOSFETs is connected to VDDIO to ensure that the source and drain of the MOSFETs are reverse biased to the bulk parasitic diode. BATVDD, as a backup power supply, does not provide current to circuit to prolong the life of the battery unless the main power is off. Therefore, the power supply switching is only controlled by detecting VDD. Generally, the switching threshold for 5 V (main supply voltage) applications is 3.6 V, and for 3.3 V application is 3.0 V.

As shown in Figure 5, the output of the detection circuit is connected to the power switch circuit to generate two-phase nonoverlapping clocks [18, 19]. One of the clock signals passes through a buffer and is used to control the switch of VDD. Because PM0 is usually kept on during the normal application, the driving capacity of PM0 should be large

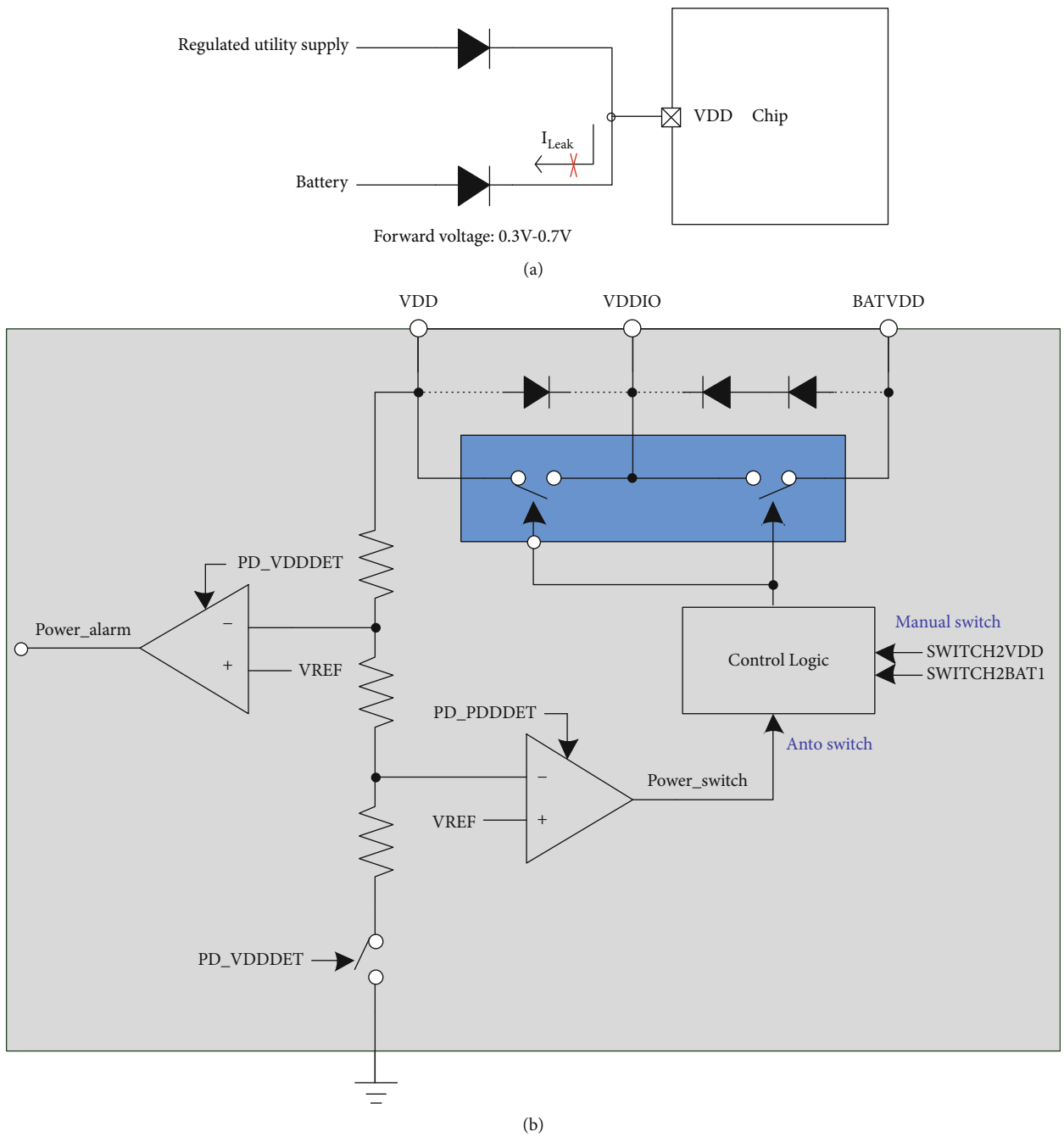


Figure 4: (a) Traditional external switching scheme; (b) proposed internal switching scheme.

enough. In order to reduce the area, a low-voltage PMOS with a larger current density per unit area is used. But meanwhile, it is necessary to control the gate-source voltage V_{GS} of PM0 to avoid breakdown. In this design, a voltage drop close to 1.5 V is generated through two diode-connected MOS transistors through a fixed bias current. When PM0 is turned on, PM7 and PM8 produce a voltage drop. When PM0 needs to be turned off, PM9 connects the gate of PM0 directly to the source. The other clock signal is used to generate the switch control signal of PM1. In order to ensure that PM1 can be completely shut down, it is necessary to ensure that the gate voltage of PM1 follows the source voltage (the source is of a higher voltage than the drain). Therefore, the gate voltage of PM1 needs to be at the higher voltage of VDDIO and BATVDD to prevent the reverse current to the battery when VDDIO = VDD = 5 V. The detailed circuit is shown in Figure 5. When PM0 is turned on, S2 is low. PM3 and PM4 are on, and NM0 and NM1 are off. PM5 and PM6 are gate-source connected transistors that act like parasitic diodes. Since there is no conduction current, the voltage drop is much smaller than a threshold voltage V_{TH}, so that the voltage of the gate of PM1 is almost equal to the higher voltage of

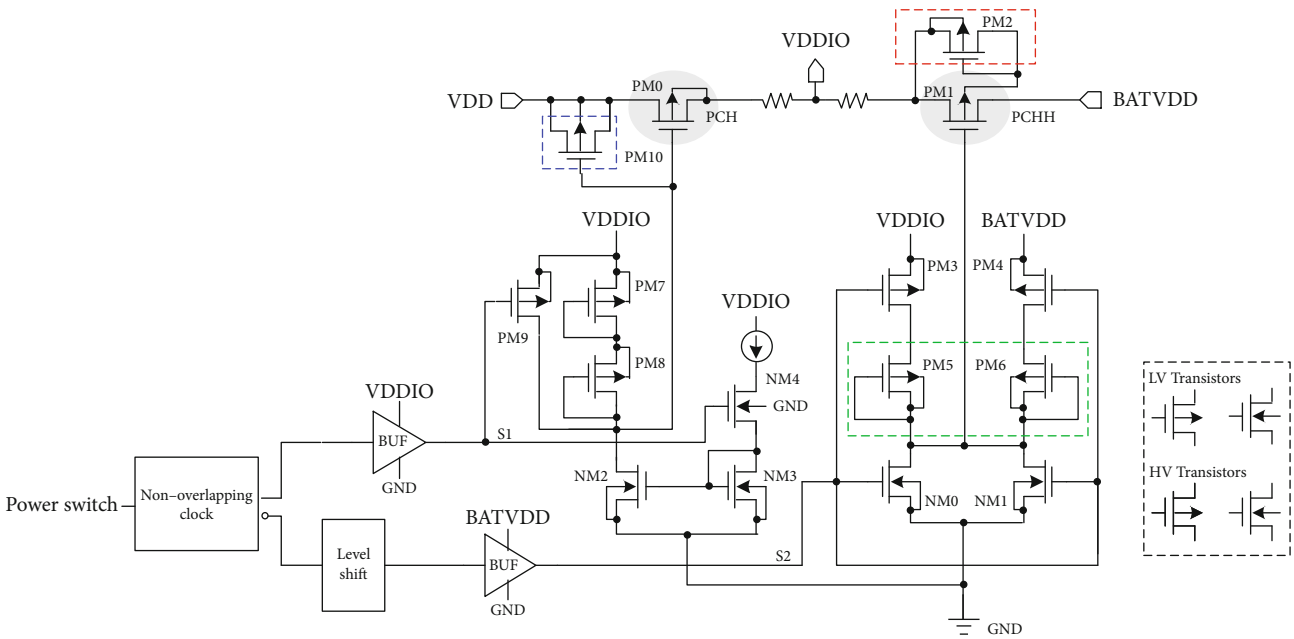


Figure 5: Power supply switching circuit.

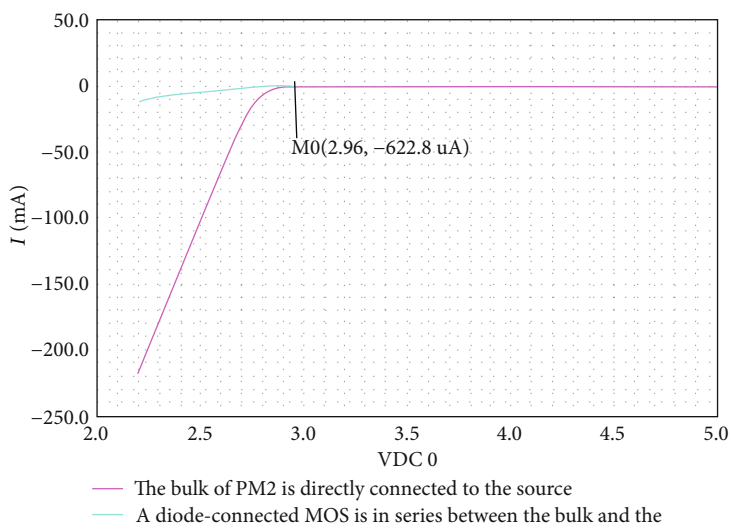


Figure 6: BAT leakage current with and without PM2.

VDDIO and BATVDD. With PM5 and PM6, the two power supplies can also be isolated from each other to prevent the inverse current.

An additional transistor PM2 is connected on the bulk of PM1 to avoid drawing current from the battery. For 3.3 V applications, the threshold of the power switch is set at 3.0 V ± 10%. It may happen that PM1 remains off, but the parasitic diode of its drain and bulk is forward biased and starts to draw current from BATVDD without PM2 [20]. The effect is similar to doubling the threshold voltage from BATVDD to VDDIO, as shown in Figure 4(b), which improves the reliability of the power supply switching circuit. The comparison is shown in Figure 6. When VDDIO is lower than 3.0 V, BATVDD starts to leak current to VDDIO, and the modified circuit has significantly smaller leakage than the original circuit.

The transistor PM10 is also connected in series at the drain and gate of PM0 to solve the breakdown problem that may be caused by the rapid rise of VDD with the cold start. Through the MOS CAP formed by PM10, the instantaneous voltage difference between the drain and the gate of PM0 is limited. It also improves the reliability of the circuit [21].

To ensure that bulk parasitic diodes of these two power switches PM0 and PM1 are always reverse biased, the conduction voltage drop of both should be small enough. Under the condition that the maximum load current is 30 mA, the selected conduction impedance is less than 8 Ω over process corners.

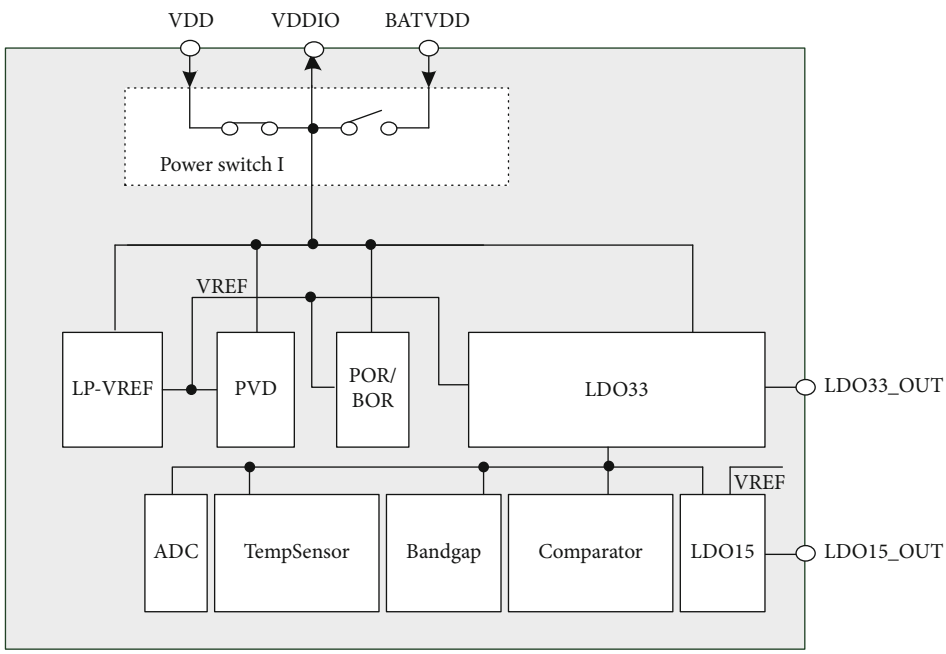


Figure 7: BAT leakage current with and without PM2.

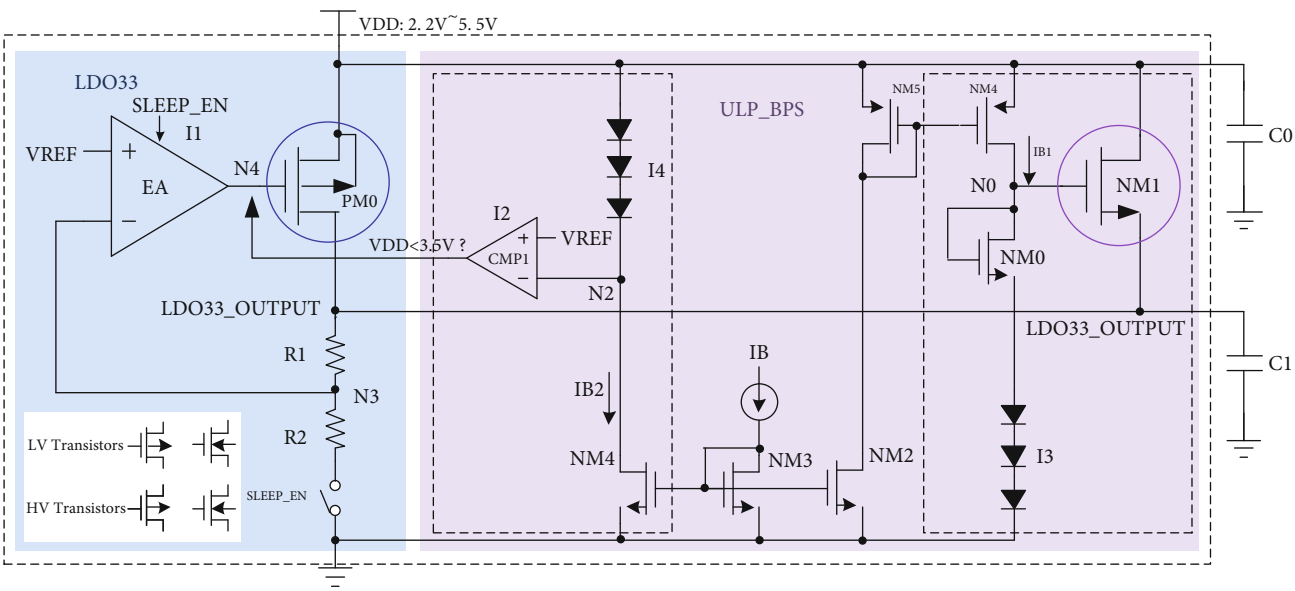


Figure 8: Ultra-low-power backup power supply (ULP_BPS).

As for the power switch in the RTC power domain (power switch I in Figure 3), because the RTC power domain continues to work at low power consumption (such as 1 μA), the design of the switch is similar, but it will be much simpler.

3. Ultra-Low-Power Backup Power Supply Design

MCUs usually have multiple power supplies from different sources, such as from an off-chip LDO output, by an ultracapacitor, or from a battery, depending on the applications. To ensure that the key modules have a stable power supply voltage, as shown in Figure 7, MCUs with a 5 V main supply voltage usually regulate the supply voltage to 3.3 V through an internal LDO (referred to as LDO33 below) to supply analog modules such as the bandgap, the temperature sensor, and ADC. It is also used to supply current for low-power-consuming blocks such as the LDO15 and comparators. In the sleep mode with the main power on, the LDO33 is still active because some of the analog blocks are still working. To achieve lower power consumption in the sleep mode, the quiescent current of the LDO33 needs to be minimized.

The traditional LDO33 is shown in Figure 8. The output voltage is divided by the sampling resistor and fed back to the error amplifier (EA) to generate a stable voltage LDO33_OUT. To design a low-power LDO, in addition to reducing

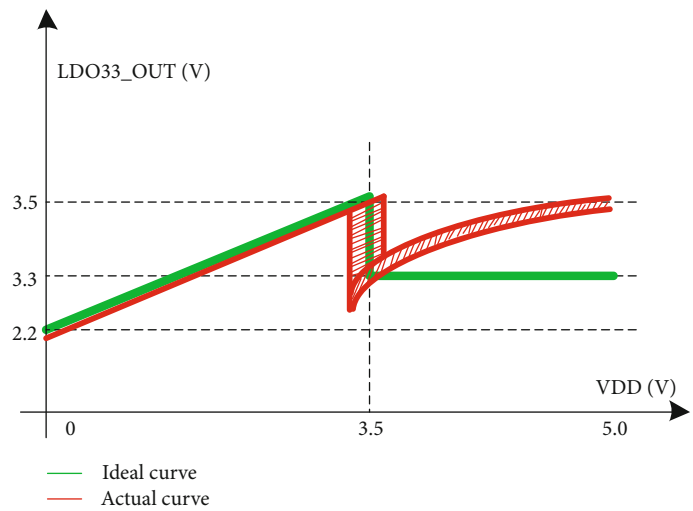


Figure 9: Ideal output vs. output considering nonideal effects.

the power consumption of the EA block, it is also necessary to minimize the current on the sampling resistors. Because the voltage drop of the resistor is fixed, the current can only be reduced by increasing the resistance. A larger resistance leads to a larger area. Suppose we want to reduce the power consumption of the LDO33 to 0.1 μA, using the traditional scheme, the resistance needs to be increased to 33 M ohms even without considering the power consumption of the EA. A 33 M ohm resistance in a CMOS process is usually area consuming. As for the digital LDO, it can work at a very low supply voltage, but it usually has the problem of large output ripple and it is still challenging to achieve absolute low power consumption [22], which is not suitable for the target applications.

In the sleep mode, the most functional modules are turned off; the load of LDO33 usually does not exceed 100 μA. The accuracy of the output voltage is also greatly relaxed. The paper proposes to add an ultra-low-power backup power supply (ULP_BPS) to the traditional LDO33. In the sleep mode, the main LDO is shut down and the ULP_BPS kicks in to reduce the power consumption.

As shown in Figure 8, LDO33_OUTPUT (the output voltage) is generated by passing a fixed voltage through a source follower. The required voltage is generated by adding a bias current to the diode string. The bias current can be limited to 10 nA and provided by anther low-power reference and bias generation circuit, which consumes about 300 nA and can also provide the reference voltage VREF for LDO33 in the normal working mode. It is powered by the main supply voltage VDD to avoid start-up problems. Due to the use of the source follower structure, there is no need for a resistor string to form a feedback loop and no need to worry about the stability.

In this implementation, the P-type bias current flows thru a diode-connected transistor NM0 and a diode string I3 to the ground. If the gate-source voltage V_{GS} of NM0 is close to that of the driver transistor NM1, the output LDO33_OUT (the source of NM1) is almost equal to the voltage across I3. Therefore, the output voltage can be adjusted by adjusting the number of diodes in I3. When VDD is small (less than $V_{I3} + V_{GS,NM0}$), the transistor NM4 enters the linear region, and the output voltage is about $V_{DD} - V_{GS,NM1}$.

Since the battery voltage changes in its lifetime, the MCU is usually required to have a wide operating voltage range, such as 2.2 V~5.5 V. But the analog blocks supplied by LDO33 have a minimum voltage requirement, say 2.2 V. When the voltage is lower than this, the analog blocks will work abnormally, and the chip will also trigger power on reset (POR) and exit the sleep mode. In this case, LDO33 will follow VDD directly, regardless of the level of VREF. VREF is calibrated to guarantee the accuracy of the supply detection result. In summary, ULP_BPS block needs to meet the requirements of 2.2 V~3.8 V output under 2.2 V~5.5 V input. The 3.8 V output is due to the requirement of the device breakdown voltage.

When the input is low, say below 3.0 V, the output $V_{DD} - V_{GS,NM1}$ will be difficult to maintain above 2.2 V. We add a power detection mechanism to address this. When a low-power supply voltage is detected, the driver transistor PM0 is turned on such that the output of LDO33_OUT follows VDD to maximize power utilization. The driver transistor of the main LDO can be reused to ensure a low voltage drop while avoiding additional area cost. In the implementation, a fixed bias current flows through the diode string I4 connected to VDD to generate a voltage drop $V_{DD} - V_{I4}$ that is compared with the low-power reference voltage VREF through a comparator. For example, if the voltage drop across I4 is designed to be 2.3 V, the output will follow VDD when VDD is lower than 3.5 V (VREF is about 1.2 V).

In CMOS processes, diodes are generally realized by diode-connected MOS transistors. In order to ensure that the output is controlled within the demand range for different loads, power supply sources, temperatures, and process deviations, it is necessary to minimize the variation of the device to achieve bias in the design with respect to the above

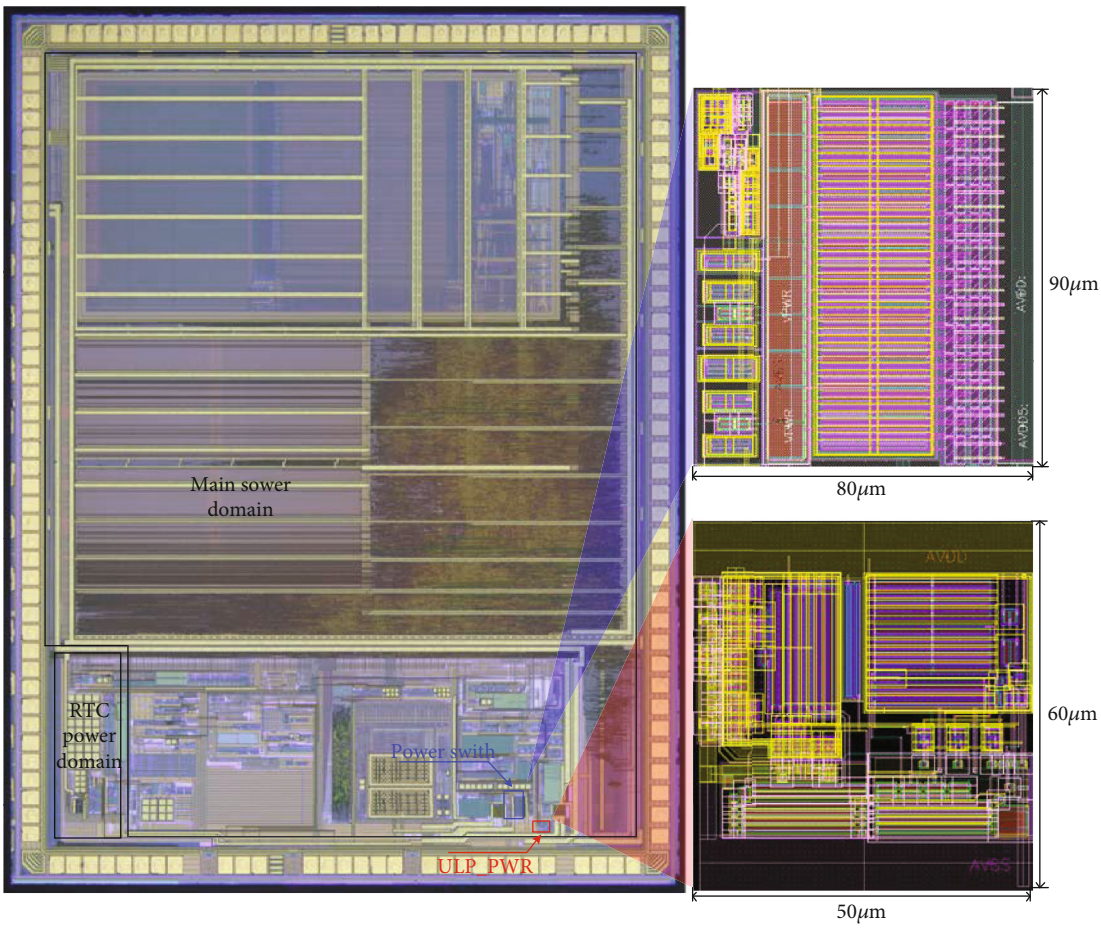


Figure 10: Die microphoto.

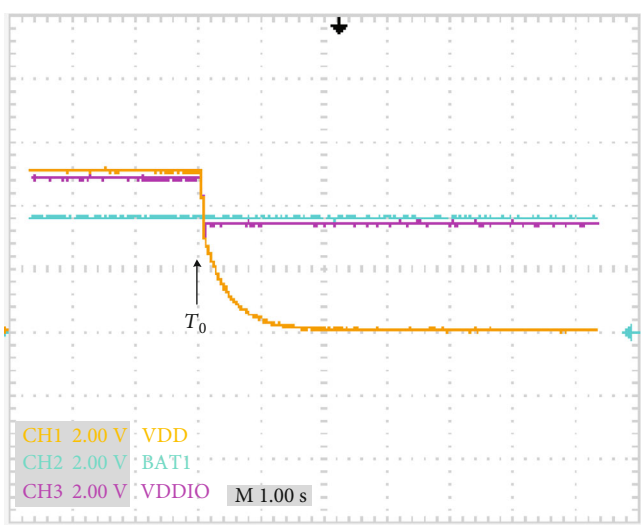


Figure 11: Oscilloscope results of power switch scheme.

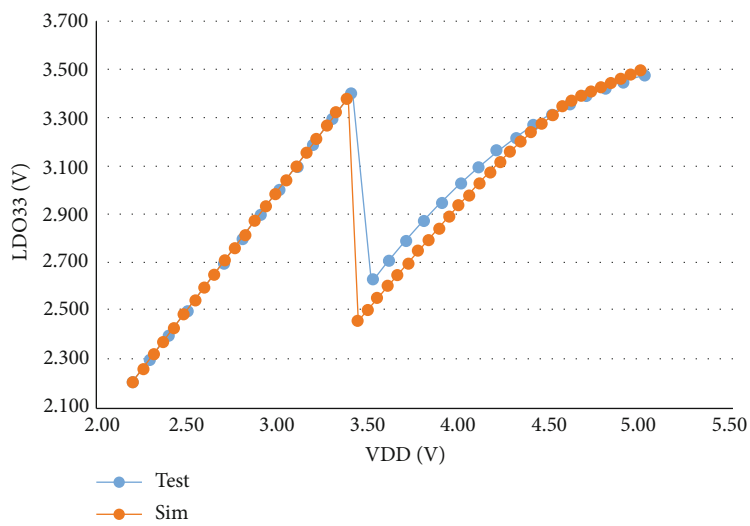
variables [23]. Figure 9 shows the simulated output voltage vs. the VDD. Detailed design considerations for high reliability are list below.

The typical voltage drop at I4 is $V_{DD} - V_{REF} = 2.3\,V$, lower than the breakdown voltage of the low-voltage transistor. It is realized by using three low-voltage (LV) PMOS in series. For the diode string I3, a high-voltage (HV) IO PMOS is used to avoid breakdown of LV devices. However, the threshold voltage of HV PMOS is relatively high, and it cannot match 3.3 V well if two or three are connected in series, so a small LV core NMOS is used at the end of series closest to GND. A MOS transistor of the same type as NM1 is used to implement NM0 so that the gate-source voltage VGS is as close as possible. However, due to the difference in current flow, variations will still be introduced. The body of the HV PMOS is connected to VDD. When the input is over 3.6 V, the actual output is a curve that increases with VDD but the slope gradually decreases as shown in Figure 9. The output is shown in the red curve in Figure 9. The turning point and the output at high VDD have a certain offset range, but it does not exceed the target window of 2.2 V-3.5 V.

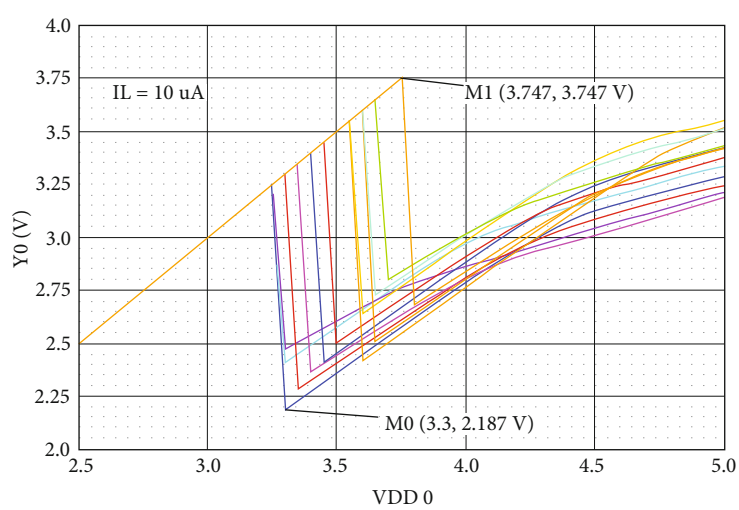
In the design, the bulks of all PMOS transistors are not connected to the source to eliminate the body effect. The main consideration is that the branch bias current is very small so the impedance is high. During reliability tests such as latch-up, if there is substrate leakage, it may cause abnormal bias, so the bodies of transistors are connected to a low-resistance power supply or ground.

Table 2: Comparison of results between traditional LDOs and the improved structure.

Module	Technology (μm)	Input voltage (V)	Output voltage (V)	Max output current (mA)	Quiescent current (μA)	Size (mm^2)	Stability consideration
LDO33 (this work)	0.11	2.2-5.5	2.2-3.6	30	1	0.026	Yes
ULP_BPS (this work)	0.11	2.2-5.5	2.2-3.8	0.1	0.1	0.003	No
Adaptive LDO [13]	0.13	1.9-3.6	1.52	2.56	0.65-17.7	0.016	Yes
DLDO [22]	0.65	0.5	0.45	0.2	2.7	0.042	Yes



(a)



(b)

Figure 12: (a) Simulation result vs. test result; (b) impact of PVT on turning point.

4. Simulation and Test Results

The design is implemented in a standard 0.11 μm CMOS process. As shown in Figure 10, the area of the power supply switching circuit and the low-power backup power supply is 0.0072 mm^2 and 0.003 mm^2, respectively, accounting for less than 1% of the whole chip area.

To test the power switching circuit for an actual energy application, we connect BATVDD to 3.6 V and VDD to 5.0 V DC sources, respectively. Enable the automatic

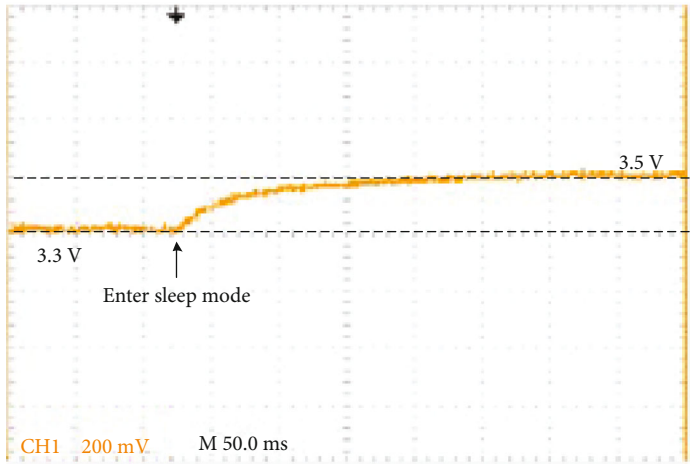


Figure 13: Measurement results of LDO33_OUT using an oscilloscope when switching from the normal operating mode to the sleep mode.

switching mode, and set the switching voltage to 3.6 V through software configuration, then disconnect VDD from the DC source at T_0, and observe the entire switching process through an oscilloscope. In Figure 11, the yellow line and the blue line are the two input power supplies, VDD and BATVDD, respectively, and the purple line is the output VDDIO. It can be seen that after disconnecting from the DC source, VDD drops slowly, and VDDIO still follows VDD at the beginning. But when it drops to about 3.6 V, VDD continues to drop, and VDDIO remains near the battery voltage. The realization of the entire power switch is stable and reliable.

Test results show that the power consumption of the proposed ULP_BPS module is about 0.1 μA, which is an order of magnitude lower than the power consumption of the traditional low-power LDO33. Due to the open loop structure, it does not have stability problem. Compared to single adaptive LDO design in [13], this work can achieve lower quiescent current and support larger load current (30 mA) by combining the traditional LDO33 and the proposed ULP_BPS. Comparison of results is shown in Table 2.

Set the output current of LDO33_OUT to 5 μA, and perform a DC swept on VDD from 5 V to 2.2 V. Both the simulation and test results are shown in Figure 12(a), meeting the design spec. Figure 12(b) shows the influence of Process-Voltage-Temperature (PVT) on the output. It can be seen that the output is 2.2 V~3.75 V under the full input range of 2.2 V~5.5 V meeting the design spec.

In practical applications, when the energy meter enters the sleep mode from the normal operating mode, the output of LDO33_OUT is observed through the oscilloscope, as shown in Figure 13. Because LDO33 has a large decoupling capacitor off-chip, e.g., 10 μF, LDO33_OUT will slowly switch to the output of ULP_BPS.

5. Conclusions

To address the low-power design issue for MCU, we proposed several power management techniques. Firstly, the application-based multimode switch scheme along with a multipower domain strategy is proposed to optimize power consumption through hierarchical control. In addition, we integrated the traditional power switching function into the chip and designed a safe and reliable power switch circuit, which can effectively reduce system costs and extend battery life. To further reduce the power consumption in the sleep mode, we also designed an ultra-low-power backup power supply circuit to replace the low-power LDO reducing the power to 0.1 μA, an order of magnitude lower than the original circuit. The techniques have been used in energy metering chips that have been sold in millions.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

There is no conflict of interest regarding the publication of this paper.

Acknowledgments

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