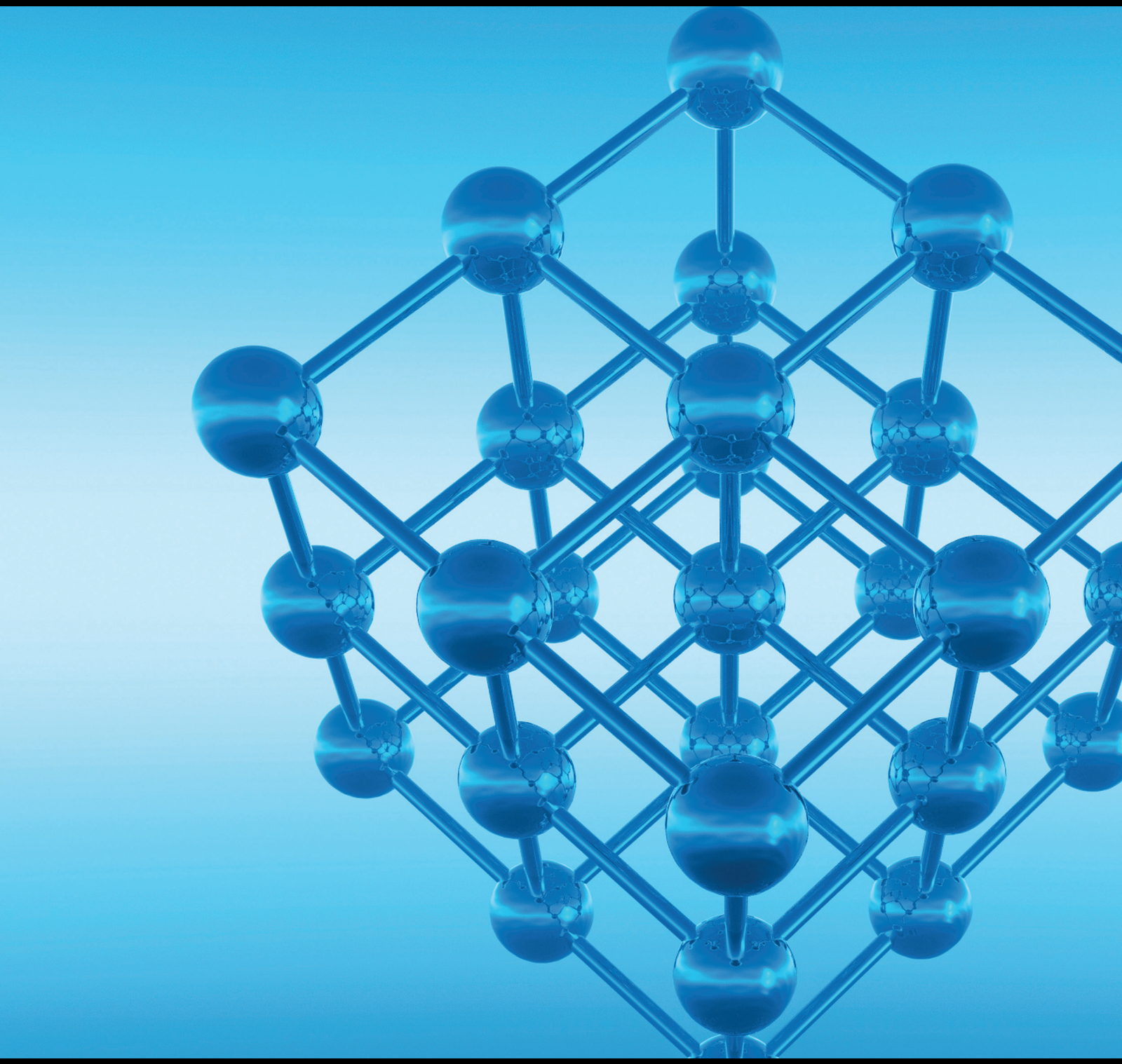
Advances in Condensed Matter Physics

Si- and Ge-Based Electronic Devices

Guest Editors: Yi Zhao, Wenfeng Zhang, Rui Zhang, and Jiwu Lu



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Editorial Board

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Editorial
Si- and Ge-Based Electronic Devices

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In the past few decades, silicon (Si) complementary metal-oxide-semiconductor (CMOS) field-effect transistors have been scaled exponentially over time for the demand of drive current enhancement and cost reduction. As the technology node advances into sub-20 nm regimes, Si CMOS encounters immense challenges from both processing and theoretical perspectives. To maintain or further improve the transistor performance, Ge-based electronic transistors are explored as Ge exhibits higher hole and electron mobilities. As compared with the Si CMOS process, the process for fabricating high performance Ge-based transistors is still under development. This special issue aims to address some of the challenges encountered in the state-of-the-art technology, for both the Si- and Ge-based electronic transistors.

For Ge MOSFETs, interface engineering and gate dielectric engineering are necessary to reduce the electrical active defects in the Ge surface and the high-κ/Ge interface. Other than Ge, SiGe is another possible channel material for the future CMOS technology. SiGe could be obtained by directly growing on Si substrate and therefore it has better compatibility with Si CMOS technologies. Besides the research works on Ge-based transistors, this special issue also includes some papers on the Si lateral diffused MOS (LDMOS). Novel structural designs were demonstrated to improve the performance and reliability of the Si LDMOS. Last but not least, this issue also reports a work on increasing the responsivity of the Si n-MOSFET photodetectors.

We hope that readers of this special issue will find not only the accurate and most updated data in the papers, but also important solutions for the existing issues in the theory and fabrication of Si- and Ge-based electronic transistors.

Yi Zhao
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Jiwu Lu
Wenfeng Zhang

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Research Article

Characteristics and Breakdown Behaviors of Polysilicon Resistors for High Voltage Applications

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With the rapid development of the power integrated circuit technology, polysilicon resistors have been widely used not only in traditional CMOS circuits, but also in the high voltage applications. However, there have been few detailed reports about the polysilicon resistors' characteristics, like voltage and temperature coefficients and breakdown behaviors which are critical parameters of high voltage applications. In this study, we experimentally find that the resistance of the polysilicon resistor with a relatively low doping concentration shows negative voltage and temperature coefficients, while that of the polysilicon resistor with a high doping concentration has positive voltage and temperature coefficients. Moreover, from the experimental results of breakdown voltages of the polysilicon resistors, it could be deduced that the breakdown of polysilicon resistors is thermally rather than electrically induced. We also proposed to add an N-type well underneath the oxide to increase the breakdown voltage in the vertical direction when the substrate is P-type doped.

1. Introduction

With the booming market of power integrated circuits for the smart power management [1–4] and automotive and green energy, BCD [5, 6] (Bipolar-CMOS-DMOS) technology has been proved to be the best solution for these applications. People tend to integrate as much active and passive devices, including resistors, for different voltages' applications as possible on single chip. As a resistor, polysilicon [7] is supposed to be the best choice for integrated circuits technology due to its good and stable voltage and temperature coefficients. However, in the high voltage application, although the polysilicon resistor is still acting as an important device, there are few detailed reports about its properties, especially the voltage and temperature coefficients, under high voltages. It has been experimentally observed that different doping concentrations in the polysilicon could lead to different voltage and temperature coefficients of the resistor [8–10]. However, there is no enough physical explanation or further analysis for this phenomenon, which is very important for guiding the mass production. On the other hand, circuits for DC-DC and AC-DC applications in the smart power management system require the resistor to behave robustly under high voltages. This topic is not experimentally studied yet.

In this study, we investigate the voltage and temperature coefficients of polysilicon resistors with different doping concentrations. Secondly, the breakdown voltages (V_{BD}) of the resistors with different sizes are discussed. Also, the impacts of the high and low voltage stresses on the resistance of the polysilicon are experimentally studied. The results show that the voltage and temperature coefficients strongly depend on the doping concentration. After the high voltage stress, the resistance of the polysilicon could be degraded.

2. Experimental

The polysilicon resistors with different doping concentrations were prepared at 1 μm BCD standard process platform. The doping concentrations and corresponding square resistances are summarized in Table 1. Except for the doping concentration, all other processes were the same for all the resistors. The test structure for measurements in this study is shown in Figure 1.

Table 1: Doping concentrations and corresponding square resistances at room temperature.

	High	Medium	Low
N-type doping concentration (cm^{-3})	2*E*20	1.9*E*19	1.5*E*19
Resistance at room temperature (ohm/sq)	350 ± 70	2000 ± 400	10000 ± 4000

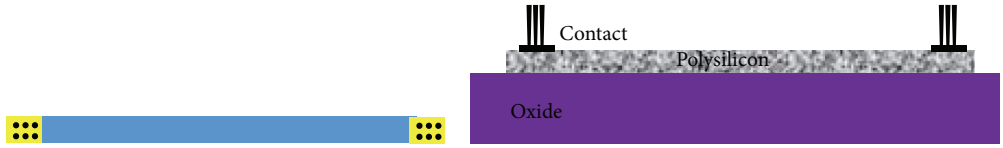

Figure 1: (a) Layout and (b) cross section of the resistor (color online).

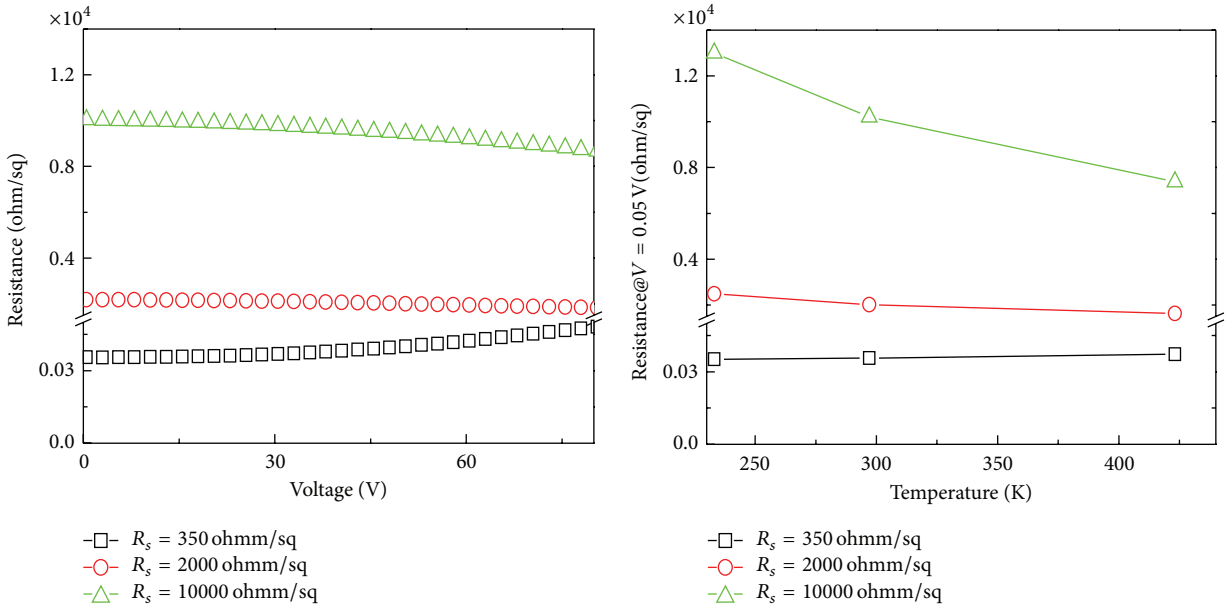

Figure 2: (a) Resistance-voltage and (b) resistance-temperature curves of three resistors with different resistances (color online).

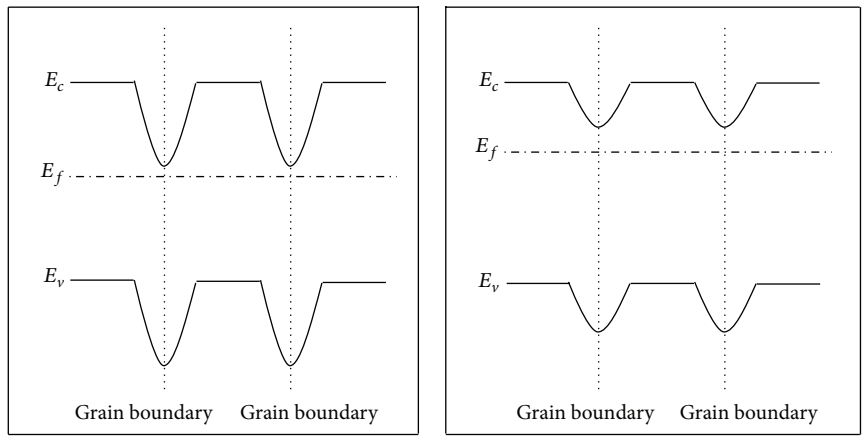

Figure 3: Illustration of the energy band of (a) low doping and (b) high doping concentrations.

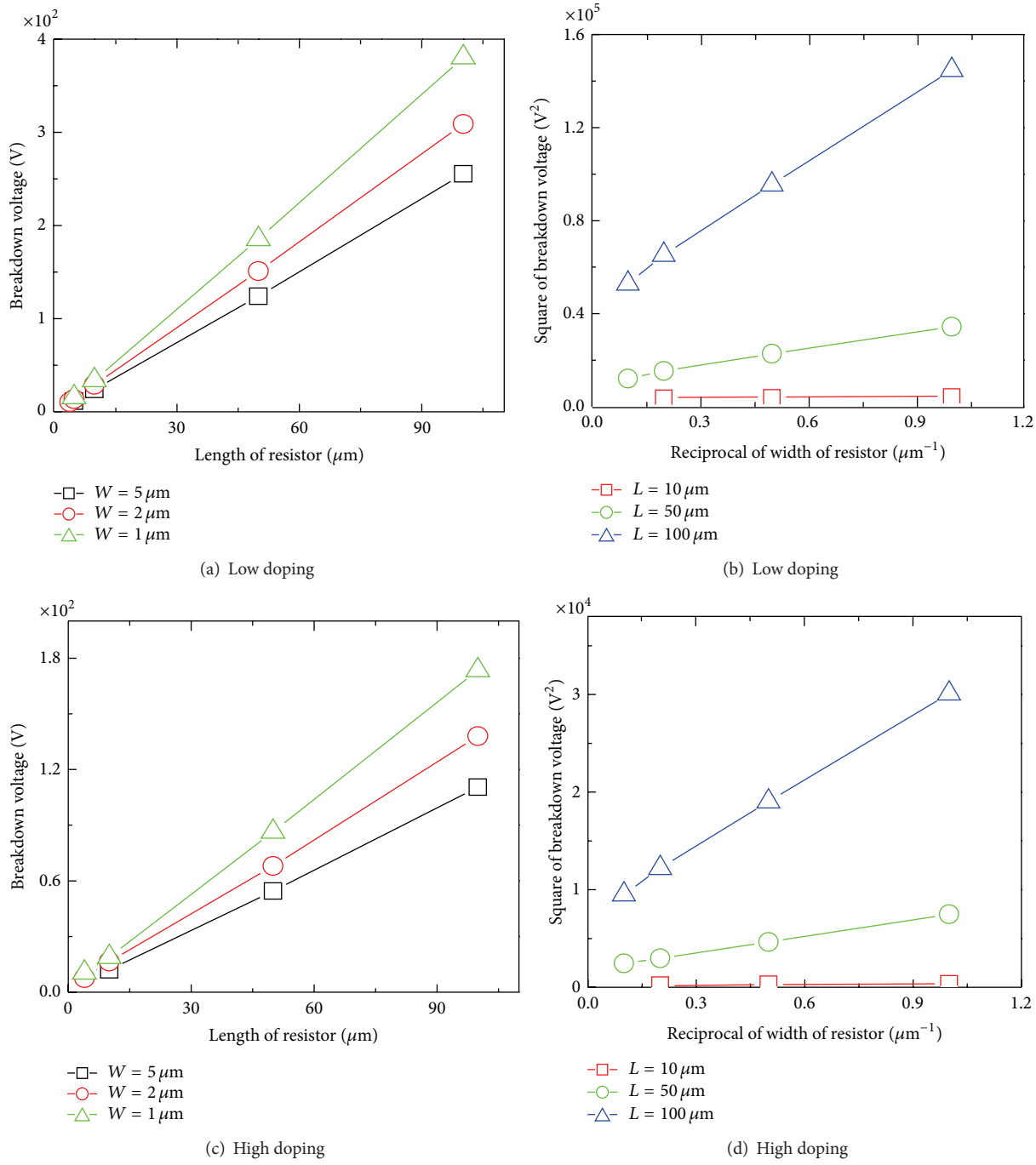

FIGURE 4: V_{BD} versus length of the resistor ((a) and (c)) and square of V_{BD} versus the inversed width of the resistor ((b) and (d)) (color online). (a) and (b) come from lightly doped resistors while (c) and (d) come from highly doped ones.

The voltage and temperature coefficients were extracted in the high voltage (<80 V) region and under the temperature varied from −40°C to 150°C.

V_{BD} of the polysilicon resistors with different widths (W) and lengths (L) were measured. Some polysilicon resistors were electrically stressed with a low voltage (6 V) or a high voltage (80 V) for some time.

3. Results and Discussion

3.1. Resistor Characteristics. Figure 2 shows the voltage and temperature coefficients of the polysilicon resistors with different doping concentrations. All the resistances in Figure 2(b) are obtained with applied voltage of 0.05 V. It could be found from the figure that the resistor with a

relative high doping concentration shows a positive voltage coefficient and a positive temperature coefficient while the other two resistors with much lower doping concentrations have negative voltage and temperature coefficients.

The possible reason for this phenomenon might be as follows. Polysilicon consists of many large grains, which are surrounded by grain boundaries. When the polysilicon is doped with a low impurity concentration, most of the carriers are absorbed by the grain boundaries, resulting in potential barriers around the boundary which could prevent the carriers moving (Figure 3). When a voltage is applied to the resistor, the carriers own a high energy and could more easily travel across the barrier, generating larger current and lower resistance. Similarly, a high temperature could help the carriers across the grain-boundary-induced barriers. Thus, the polysilicon resistor with a lower doping concentration has negative voltage and temperature coefficients. When the polysilicon is heavily doped, the grain boundaries have been full of constrained carriers while there are still many carriers remaining in grains. In this case, there will be little or even no grain-boundary-induced potential barriers around the boundary, while the high voltage and high temperature could cause large scattering within the crystalline grain, resulting in a larger resistance. Thus, the polysilicon resistor with a relative high doping concentration has positive voltage and temperature coefficients.

Therefore, it could be possible for us to make the voltage and temperature coefficients as small as we want if we tune the doping concentration carefully.

3.2. Reliability Behaviors of Polysilicon Resistors. Breakdown voltages of polysilicon resistors with different sizes (W and L) are shown in Figure 4. We can see that the breakdown voltage is proportional to the length of the resistor, while the square of the breakdown voltage is reversely proportional to the width of the resistor. This result is in good agreement to Scafft's research [11] on thermal conductance of a rectangular resistance on an oxide film over a Si substrate. The breakdown voltage decreases with the increase of the width of the resistor in Figure 4, showing that the polysilicon resistor is thermally breakdown, instead of electrically breakdown.

Furthermore, to study the reliability behaviors of the polysilicon resistors under high voltage applications, the same resistors with high doping concentrations were electrically stressed at 6 V and 80 V. As shown in Figure 5, the stress of 6 V has no significant effect on the resistance, while the 80 V stress leads to a quick decrease and then a smooth increase in the resistance of the resistor. We think that the resistance decrease is due to the charge release from the grain boundaries while the increase could be attributed to self-heating of the polysilicon.

The above results suggest that, in order to ensure that the resistor behaves robustly in the circuits, the study on the breakdown voltage of the resistor with different sizes is required. Besides, the voltage stress should be a necessary item for the reliability evaluation including both self-heating and electromigration effects of polysilicon resistors [12–16].

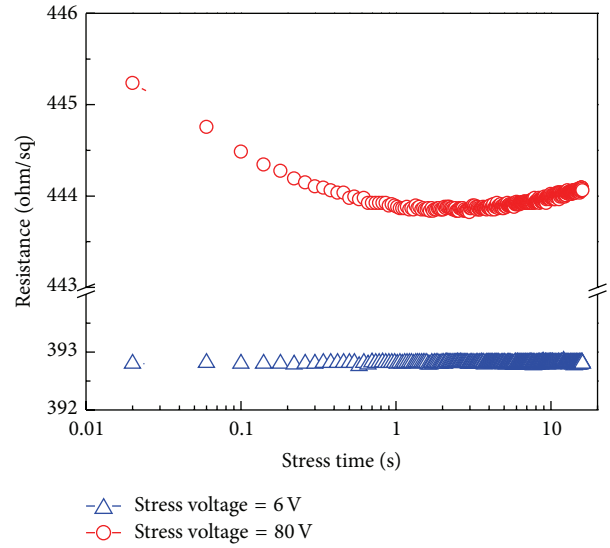

Figure 5: Normalized resistance under 6 V and 80 V stress (color online).

3.3. New Structure Proposal for Resistor due to Oxide Consideration. According to the structure of resistor in Figure 1, we can see that if the voltage application of the resistor comes up to several hundred volts, the voltage across the oxide is several hundred volts and the electrical field density is above the critical density of breakdown of silicon dioxide (Figure 6(a)). On the other hand, a high voltage on the resistor has a simultaneous vertical electrical field which may lead to a lot of reliability problems of the oxide for isolation. Thus, oxide breakdown becomes another shortcoming for high voltage application of resistor. A new structure in Figure 6(b) is suggested for the resistor to add a lightly doped N-type well under the oxide if the substrate is P-type doped. In this way, a PN diode is formed below the oxide. When high voltage is stressed on the resistor, the diode is reversed biased and undertakes parts of the voltage. The whole structure can be summarized as an oxide capacitance and a diode in series in Figure 6(c). We can see that the breakdown voltage of the vertical structure [11, 12] can be increased and the voltage stressed on the resistor can be increased.

4. Conclusions

We have experimentally investigated the voltage and temperature coefficients of polysilicon resistors for high voltage applications. The experimental results show that ultralow voltage and temperature coefficients (~0) could be achieved according to carefully tuned doping concentrations. We also found that the breakdown of the polysilicon resistors under a high voltage is a thermal-dominant process, rather than an electrical process. Furthermore, the high voltage stress can degrade the performance of the polysilicon.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

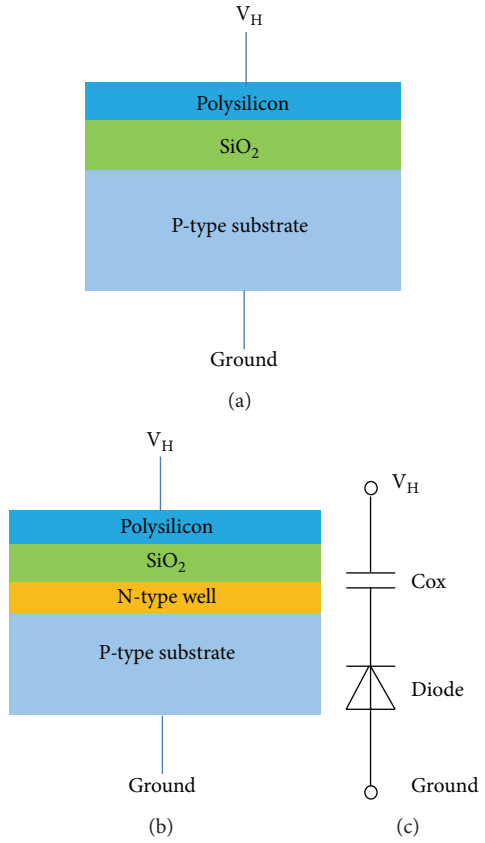

FIGURE 6: (color online) (a) Simplified vertical structure for resistor (b) added Nwell beneath the oxide to raise the breakdown voltage of the vertical structure.

Acknowledgments

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References

[1] R. Rudolf et al., IEEE International Symposium on Power Semiconductor Devices and ICs, 2011.

[2] K. Sam, N. A. Rahim, and H. Mokhlis, "Smart power management algorithm in microgrid consisting of photovoltaic, diesel, and battery storage plants considering variations in sunlight, temperature, and load," *Energy Conversion and Management*, vol. 84, pp. 562–582, 2014.

[3] T. Nitta, S. Yanagi, T. Igarashi et al., "Necessity of pulse hot carrier evaluation in suppressing self-heating effect for SOI smart power," in *Proceedings of the 21st International Symposium on Power Semiconductor Devices and IC's (ISPSD '09)*, pp. 84–87, Barcelona, Spain, June 2009.

[4] D. Y. Zai, Y. Zhao, C. Yin-Fei et al., "Effect of the trench shape on the electrical properties of silicon based trench barrier schottky diode," *Acta Physica Sinica*, vol. 63, Article ID 127201, 2014.

[5] I.-Y. Park, Y.-K. Choi, K.-Y. Ko et al., "BD180—a new 0.18 μm BCD (Bipolar-CMOS-DMOS) technology from 7V to 60V," in *Proceedings of the 20th International Symposium on Power Semiconductor Devices and IC's (ISPSD '08)*, pp. 64–67, Orlando, Fla, USA, May 2008.

[6] A. Andreni, C. Claudio, and P. Galbiati, "A new integrated silicon gate technology combining bipolar linear, CMOS logic, and DMOS power parts," *IEEE Transactions on Electron Devices*, vol. 33, pp. 2025–2030, 1986.

[7] N. C.-C. Lu, L. Gerzberg, C.-Y. Lu, and J. D. Meindl, "Modeling and optimization of monolithic polycrystalline silicon resistors," *IEEE Transactions on Electron Devices*, vol. 28, p. 818, 1981.

[8] G. Baccarani, B. Riccò, and G. Spadini, "Transport properties of polycrystalline silicon films," *Journal of Applied Physics*, vol. 49, no. 11, pp. 5565–5570, 1978.

[9] J. Y. W. Seto, "The electrical properties of polycrystalline silicon films," *Journal of Applied Physics*, vol. 46, no. 12, pp. 5247–5254, 1975.

[10] P. J. French, "Polysilicon: a versatile material for microsystems," *Sensors and Actuators A: Physical*, vol. 99, no. 1-2, pp. 3–12, 2002.

[11] H. Scafft, "Thermal analysis of electromigration test structures," *IEEE Transactions on Electron Devices*, vol. 34, pp. 664–672, 1987.

[12] O. Semenov, A. Vassighi, and M. Sachdev, "Impact of self-heating effect on long-term reliability and performance degradation in CMOS circuits," *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 1, pp. 17–27, 2006.

[13] J. C. Doan, J. C. Bravman, P. A. Flinn, and T. N. Marieb, "The evolution of the resistance of aluminum interconnects during electromigration," *Microelectronics Reliability*, vol. 40, no. 6, pp. 981–990, 1999.

[14] L. He, L. Du, Y. Q. Zhuang et al., "A new model for electromigration grain boundary noise based on free volume," *Chinese Physics B*, vol. 19, Article ID 097202, 2010.

[15] H. Sheng-Dong, Z. Bo, L. Zhao-Ji, and L. Xiao-Rong, "A new structure and its analytical model for the vertical interface electric field of a partial-SOI high voltage device," *Chinese Physics B*, vol. 19, no. 3, Article ID 037303, 2010.

[16] Y. G. Wang, X. R. Luo, R. Ge et al., "Compound buried layer SOI high voltage device with a step buried oxide," *Chinese Physics B*, vol. 20, Article ID 077304, 2011.

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Research Article

Transformation of Holes Emission Paths under Negative Bias Temperature Stress in Deeply Scaled pMOSFETs

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We examine the impact of negative bias temperature (NBT) stress on the fluctuations in I_D and I_G for deeply scaled pMOSFETs and find that the relative high NBT stress triggers I_G-RTN and I_D-step. Through the analysis of the field dependence of emission constant and the carrier separation measurement, it is found that under the relative high NBT stress some traps keep charged state for very long time, as observing step-like behaviors in I_D, while other traps emit charged holes to the gate side through TAT process, which originate both I_D-step and ID-RTN.

1. Introduction

Negative bias temperature instability (NBTI) degradation is one of the most important reliability issues in modern complementary metal-oxide-semiconductor (CMOS) technologies [1–7]. Recently, much attention has been paid to NBTS generated oxide traps, which could significantly increase the failure probability in deeply scaled pMOSFETs. Furthermore, these traps are currently considered to not only cause the V_{th} degradation but also increase the gate leakage current (I_G) [8–10]. However, someone considers the I_G fluctuations are probably not to be explained as the results of NBT induced switching traps [11–13]. Tsujikawa reported that the observed transient I_G and I_D signal simultaneously in small size pMOS devices are not linked directly with each other [11]. Wagner et al. [12] pointed out that the increases of I_G fluctuation are probably caused by the beginning of oxide breakdown which should not be explained as the results of NBT induced switching trap while Gao et al. [14] have reported that I_G increases only when part of the switching hole traps transform to the permanent bulk traps with increasing NBT stress or stressing time. To date, the impact of negative bias temperature stress condition on I_D and I_G fluctuation has not been systematically evaluated yet.

In this paper, we examine the impact of stress on the I_G-RTN and I_D-RTN for deeply scaled pMOSFETs, using carrier separation measurement to identify the type of I_G-RTN. The characteristic of time constants and amplitude in RTN under the various stress regions is investigated and a trap-assisted tunneling model through NBT stress-induced switching traps is proposed to explain the mechanism of I_G-RTN. The results illustrate that, under the relative high NBT stress, at least some of the holes are discharged from the traps to the gate side.

2. Experiment

Plasma nitric oxide (PNO) pMOSFETs used in this study were fabricated with a standard CMOS process technology. The devices size ($L \times W$) is 30 nm × 70 nm and dielectric thickness is about 2.6 nm. And the I_D-V_G curve of this device is shown in the inset of Figure 1. The measurements were conducted using a Keithley 4200 semiconductor characterization

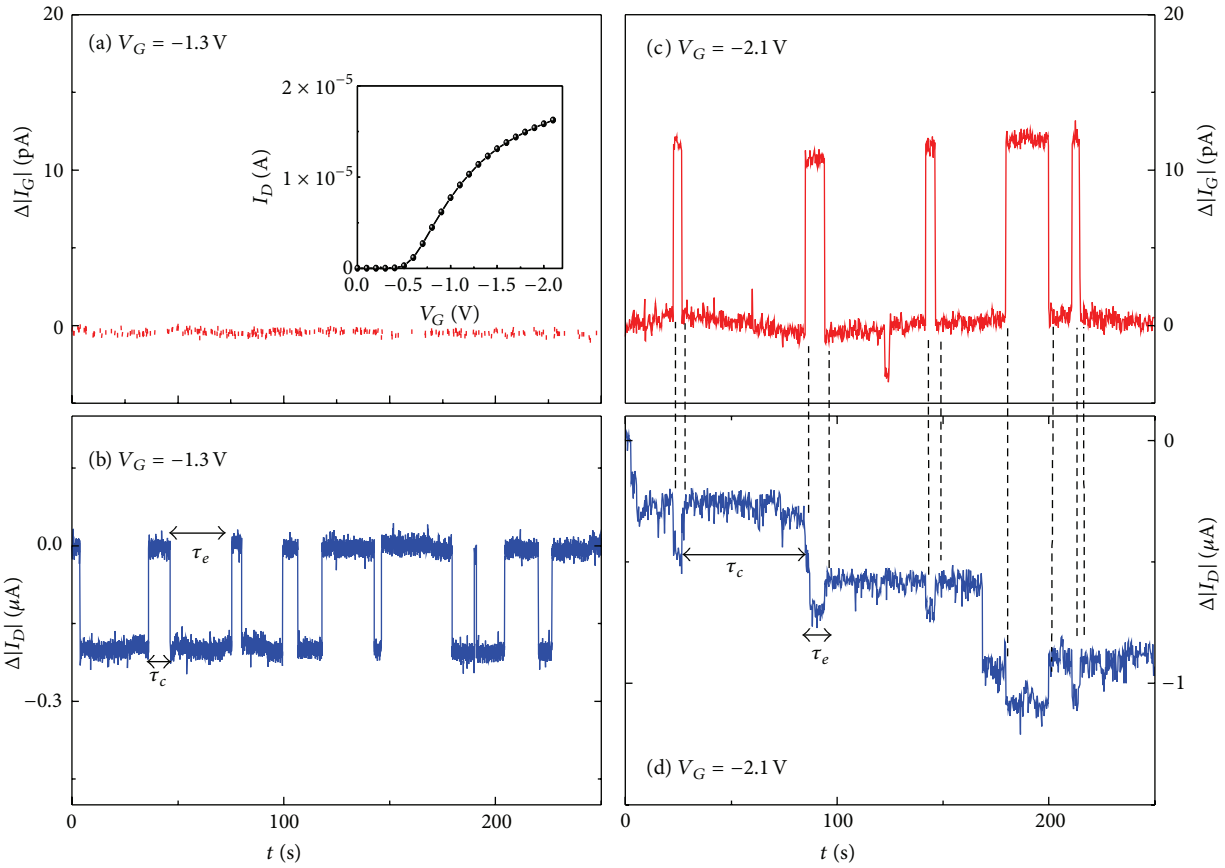

FIGURE 1: The time trace of I_G and I_D fluctuation under the gate voltage V_G of −1.3 V and −1.9 V with V_{DS} of 50 mV. The inset shows the I_D-V_G curve of the experimental device.

system and a Cascade Summit 12000 probe station with a built-in temperature controller.

3. Result and Discussion

Figure 1 shows the time traces of I_G and I_D monitored simultaneously under the relative low (V_G = −1.3 V, E_{ox} = 3.1 MV/cm) and high (V_G = −2.1 V, E_{ox} = 6.2 MV/cm) NBT with V_{DS} of 50 mV at room temperature stress for pMOSFETs. I_D-RTN is clearly detected in both cases, which should be contributed by the traps in the gate oxide layer. But there are two major differences between the two stress conditions. One is that the higher stress voltage triggers I_G-RTN, which has the strong reverse correlation with I_D-RTN; for example, the low drain current RTN level corresponds to the high gate current RTN level. The correlation suggests that I_G-RTN and I_D-RTN share the same traps induced by NBT stress, or a trapped hole results in the simultaneous increase in I_G and decrease in I_D under the relatively high NBT stress condition.

By using the carrier separation measurement as shown in Figure 2, the drain and source electrodes were connected together and the gate electrode was biased under the stress condition [15–17]. In that case, the I_G current could be divided into hole (source/drain) part and electron (substrate) part. The hole current, electron current, and I_G components could

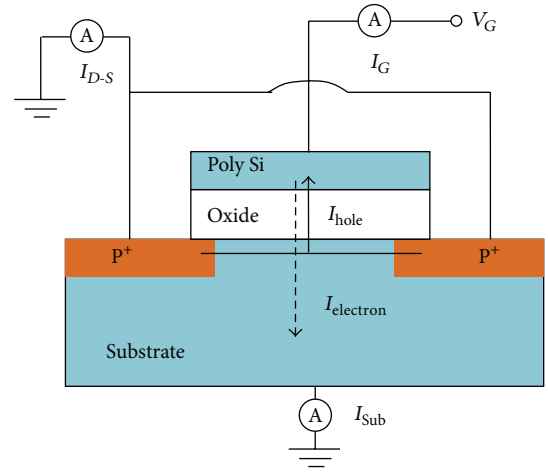

FIGURE 2: Configuration of the circuit diagram in carrier separation measurements. The gate electrode is biased for the stress condition, and drain and source electrodes are connected together.

be monitored simultaneously with the stress time. We could find several RTN fluctuations in the traces of I_{Hole} and I_G and no obvious RTN fluctuations in the $I_{electron}$ trace as shown in Figure 3. Moreover, it could be seen that the RTN fluctuations in the traces of I_{Hole} have almost same amplitude

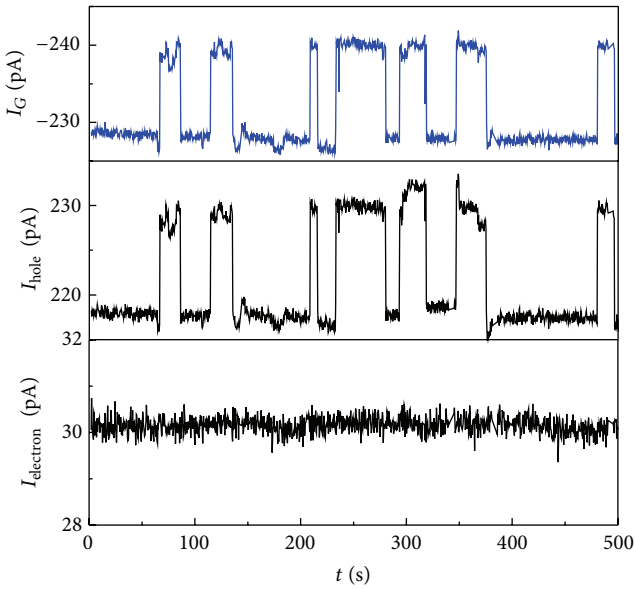

FIGURE 3: The time traces of gate current, electron current, and hole current under NBT stress (−1.9 V) at $T = 320$ K by using carrier separation technique.

and synchronize with that in the I_G trace. Therefore, holes are the major contributors to I_G-RTN. To conclude, the switching hole trap generated in high NBT stress could induce a larger amount of hole from channel to gate.

Another major difference for the two stress conditions is the electrical behaviors of I_D-RTN. Figure 4 shows the field dependence of the average value of capture time (τ_c) and emission time (τ_e) for the I_D-RTN within the gate voltage of (−1.0 V~ −1.3 V) and (−1.8 V~ −2.1 V). The average values of τ_c and τ_e are obtained from the exponential distribution of the single τ_c and τ_e. As shown in Figure 4(a), for the low stress range, τ_c and τ_e are found to exponentially decrease and increase with V_G, respectively. As shown in Figure 4(b), for the high stress range, τ_e keeps weakly dependent with the field even though τ_c exhibits similar behaviours as these observed in the low stress. The strong field dependence of both τ_c and τ_e in I_D-RTN under low stress could be explained by the extended nonradiative multiphonon (eNMP) theory [18–22]. In this theory, when the negative gate bias is applied for pMOSFETs, the switching trap states can be created from Si-Si precursors in the oxide state by capturing a hole via a multiphonon emission (MPE) process [18, 20]. The increase of the gate field results in a lower MPE barrier. The latter enhances the charge transfer reaction, leading to the dramatic reduction of hole capture time, which could be described as follows [23–25]:

$$\tau\left(\Delta E_B, F_{\mathrm{OX}}, F_C\right) = \tau_0 \cdot \exp\left(\frac{\Delta E_B}{KT}\right) \cdot \exp\left(-\frac{F_{\mathrm{ox}}^2}{F_c^2}\right). \quad (1)$$

Here ΔE_B is the multiphonon emission (MPE) barrier for hole capture, F_{ox} is the applied field in the oxide layer, and F_c is the characteristic field in MPFAT process. The red solid lines in Figure 4(a) present the fitting results with F_c being about 2.5 MV/cm which is analogous to that measured in NBTI [20, 26]. On the other hand, increasing the stress field will raise the hole traps' energy level and prevent the hole back to channel, which finally increases the emission time of RTN which is corresponding to the result in the low stress range.

However the electrical behaviour of τ_e in the high stress range is hard to be explained by this theory. One possible explanation is that the hole emission from trap is not to the Si substrate side but to the gate side by tunneling [27, 28]. In this case, increasing the stress field not only could prevent the hole back to channel but also will encourage it to be emitted to gate, which finally results in a weakly field dependence. Therefore, these switching traps behave as hole current path from channel to gate at high gate bias, which is consistent with the reverse correlation of I_D and I_G-RTN.

For verifying the current path induced by switching traps under high gate bias, the field and temperature dependence of the I_G-RTN is measured. As shown in the inset of Figure 5, the extremely weak temperature dependence was observed in ΔI_G, which is the typical behavior of elastic tunneling. In one-step elastic TAT model, channel charges could tunnel to gate side with the assistance of a trap in oxide. And the TAT probability in the model is described as [27, 29]

$$I_{\mathrm{TAT}} = AF_{\mathrm{OX}}^2 \cdot \left(\frac{\Phi_T}{xF_{\mathrm{OX}}}\right) \cdot \left(\frac{2\Phi_T}{xF_{\mathrm{OX}}} - 1\right) \cdot \exp\left(-\frac{8\pi\sqrt{2m_{\mathrm{OX}}}\Phi_T^{3/2}}{3hqF_{\mathrm{OX}}} \cdot \left[1 - \left(1 - \frac{xF_{\mathrm{OX}}}{\Phi_T}\right)^{3/2}\right]\right). \quad (2)$$

Here Φ_T is the energy depth of the trap from the valence band of dielectric, m_{ox} is the hole effective mass in dielectric, F_{ox} is electric field in oxide, and x is the trap's distance from the interface of gate and oxide. When $x = 1.5$ nm and $\Phi_T = 4$ V, it is observed that it provides a good description of the experimental data in Figure 5, which verifies that these switching traps could perform as hole tunneling paths.

Finally, the step-like fluctuations detected in Figure 1(b) are investigated. To avoid the mixture of several fluctuations, we selected the device which has only one active trap under the measurement condition. The gate voltage dependence of Id fluctuation of this trap is measured. Under the high bias of −1.7 V, the emission of the carriers from the trap is not detected until the end of measurement time of 300 s. Therefore the step-like behavior at −1.7 V is presented. When the gate bias is reduced from −1.7 V to −1.5 V, the emission of carriers from the trap occurs at about 210 s and the emission time (τ_e) is about 170 s. Further decreasing the gate bias reduces the emission time to about 70 s at $V_G = -1.4$ V and about 10 s at $V_G = -1.2$ V (Figure 6). The voltage dependence of the emission time observed here is consistent with the field behaviors of I_D-RTN in Figure 4(a). The results clearly inform that I_D-RTN transforms to I_D-step when the gate bias is increased. In other words, both I_D-step and I_D-RTN are originated from the switching traps.

According to the above analyses, I_G-RTN, I_D-RTN, and I_D-step observed in NBTI degradation are due to the generated NBT traps. Under the relatively low NBT stress, the

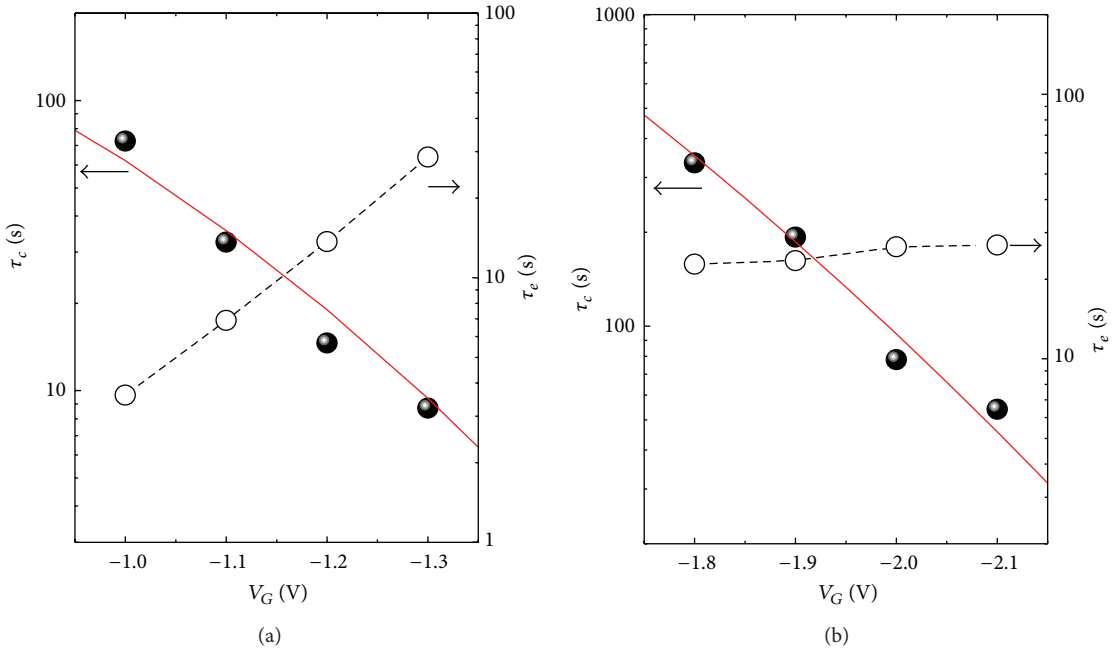

FIGURE 4: Field dependence of the average value of τ_c and τ_e of the RTN under (a) higher and (b) lower gate bias regions. The red lines present MPFAT simulation results for τ_c.

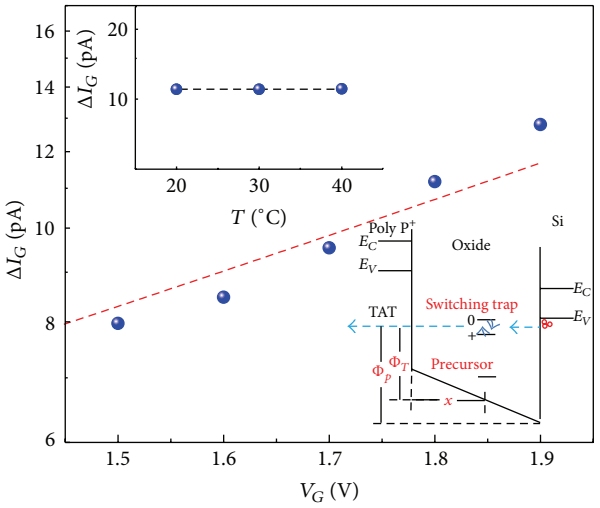

FIGURE 5: The field dependence of ΔI_G amplitude. The red dash line presents the simulation results by trap-assisted tunneling (TAT) modeling. The inset shows temperature behaviors of ΔI_G.

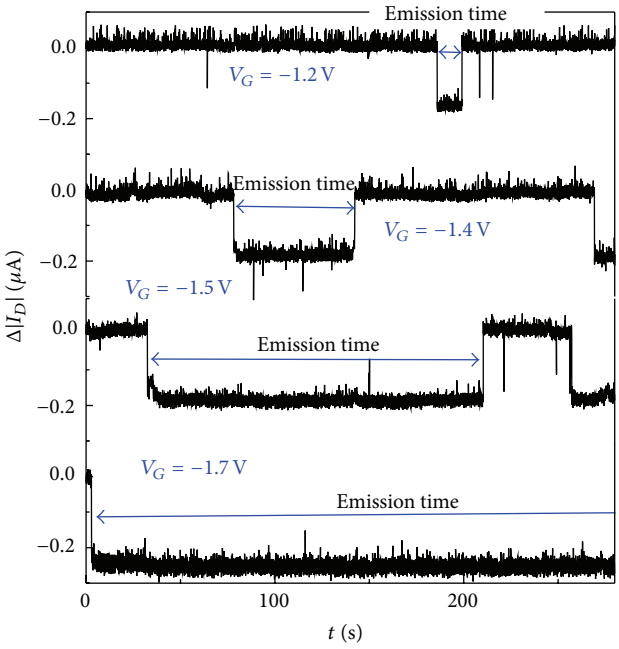

FIGURE 6: The transformation of transience signal from I_D-Step to I_D-RTN could be seen by decreasing the gate bias from −1.7 V to −1.5 V. And the emission time of this trap is obviously decreased from larger than 300 s to about 10 s when gate bias is decreased from −1.7 V to −1.2 V.

generated traps exchange holes with channel as shown in Figure 7(a), which induces the RTN fluctuations in I_D. Under the high NBT stress, larger oxide field raises the hole traps' energy level and prevents the hole back to channel. Some traps keep charged state for very long time, as observing step-like behaviors in I_D, while the other traps emit charged holes to the gate side through TAT process as shown in Figure 7(b). In the latter case, the hole current path from channel to gate is formed. As a result, RTN fluctuations in I_G are detected.

4. Conclusions

In this paper, the fluctuations including I_G-RTN, I_D-RTN, and I_D-step are studied under various NBT stress. Note

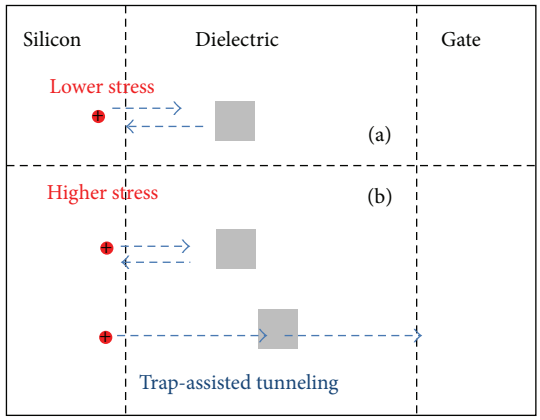

FIGURE 7: Schematic view of the switching traps in pMOSFETs. Under low gate bias, the switching traps in oxide layer could only be recovered by exchanging hole with channel and induce only I_D-RTN. Under the high gate bias, part of generated switching traps can capture and hold the hole while some others transform the hole from the channel to gate by TAT mechanism.

that, under the relative low NBT stress, only I_D-RTN could be detected while under the relative high NBT stress the I_D-RTN, I_G-RTN, and I_D-step are observed. Through the analysis of the field dependence of emission constant and the carrier separation measurement, it is found that under the relative high NBT stress some traps keep charged state for very long time, as observing step-like behaviors in I_D, while other traps emit charged holes to the gate side through TAT process, which originate both I_D-step and I_D-RTN.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

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References

[1] K. O. Jeppson and C. Svennson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," *Journal of Applied Physics*, vol. 48, no. 5, pp. 2004–2014, 2004.

[2] S. Ogawa and N. Shiono, "Generalized diffusion-reaction model for the low-field charge-buildup instability at the Si-SiO_2 interface," *Physical Review B*, vol. 51, p. 4218, 1995.

[3] C. R. Parthasarathy, M. Denais, V. Huard et al., "Designing in reliability in advanced CMOS technologies," *Microelectronics Reliability*, vol. 46, no. 9-11, pp. 1464–1471, 2006.

[4] H. C. Ma, J. P. Chiu, C. J. Tang, T. Wang, and C. S. Chang, in *Proceedings of the International Reliability Physics Symposium*, 2009.

[5] D. K. Schroder, "Negative bias temperature instability: what do we understand?" *Microelectronics Reliability*, vol. 47, no. 6, pp. 841–852, 2007.

[6] V. Huard, C. Parthasarathy, C. Guerin et al., "NBTI degradation: from transistor to SRAM arrays," in *Proceedings of the 46th IEEE International Reliability Physics Symposium*, pp. 289–300, May 2008.

[7] B. Kaczer, T. Grasser, P. J. Roussel et al., "Origin of NBTI variability in deeply scaled pFETs," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 26–32, May 2010.

[8] M. Toledano-Luque, B. Kaczer, E. Simoen et al., "Correlation of single trapping and detrapping effects in drain and gate currents of nanoscaled nFETs and pFETs," in *Proceedings of the IEEE International Reliability Physics Symposium (IRPS '12)*, pp. XT.5.1–XT.5.6, IEEE, Anaheim, Calif, USA, April 2012.

[9] X. Ji, Y. Liao, C. Zhu et al., "The physical mechanisms of IG random telegraph noise in deeply scaled pMOSFETs," in *Proceedings of the IEEE International Reliability Physics Symposium (RPS '13)*, pp. XT.7.1–XT.7.5, Anaheim, Calif, USA, April 2013.

[10] R. Degraeve, T. Kauerauf, M. Cho et al., "Degradation and breakdown of 0.9 nm EOT SiO_2 ALD HfO_2 metal gate stacks under positive constant voltage stress," in *Proceedings of the IEEE International on Electron Devices Meeting, IEDM Technical Digest*, pp. 408–411, Washington, DC, USA, December 2005.

[11] S. Tsujikawa, "SILC and NBTI in pMOSFETs with ultrathin SiON gate dielectrics," *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 524–530, 2007.

[12] P.-J. Wagner, B. Kaczer, A. Scholten et al., "On the correlation between NBTI, SILC, and flicker noise," in *Proceedings of the IEEE International Integrated Reliability Workshop (IIRW '12)*, pp. 60–64, October 2012.

[13] S. Tsujikawa and J. Yugami, "Evidence for bulk trap generation during NBTI phenomenon in pMOSFETs with ultrathin SiON gate dielectrics," *IEEE Transactions on Electron Devices*, vol. 53, no. 1, pp. 51–55, 2006.

[14] Y. Gao, D. S. Ang, C. D. Young, and G. Bersuker, "Evidence for the transformation of switching hole traps into permanent bulk traps under negative-bias temperature stressing of high-k P-MOSFETs," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 5A.5.1–5A.5.5, April 2012.

[15] W. Mizubayashi, N. Yasuda, H. Ota et al., "Carrier separation analysis for clarifying leakage mechanism in unstressed and stressed $HfAlO_x/SiO_2$ stack dielectric layers," in *Proceedings of the 42nd Annual IEEE International Reliability Physics Symposium*, Phoenix, Ariz, USA, April 2004.

[16] Y. Shi, T. P. Ma, S. Prasad, and S. Dhanda, "Polarity dependent gate tunneling currents in dual-gate CMOSFETs," *IEEE Transactions on Electron Devices*, vol. 45, no. 11, pp. 2355–2360, 1998.

[17] S.-I. Takagi, N. Yasuda, and A. Toriumi, "Expérimental evidence of inelastic tunneling in stress-induced leakage current," *IEEE Transactions on Electron Devices*, vol. 46, no. 2, pp. 335–341, 1999.

[18] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "A two-stage model for negative bias temperature instability," in *Proceedings of the IEEE International Reliability Physics Symposium (IRPS '09)*, pp. 33–44, IEEE, Montreal, Canada, April 2009.

[19] C. H. Henry and D. V. Lang, "Nonradiative capture and recombination by multiphonon emission in GaAs and GaP," *Physical Review B*, vol. 15, no. 2, p. 989, 1977.

[20] V. Huard, in *Proceedings of the International Reliability Physics Symposium*, 2010.

[21] G. Richard, B. William, B. Kaczer, and T. Grasser, "On the thermal activation of negative bias temperature instability," IIRW Final Report 36, 2009.

[22] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, in *Proceedings of the IEEE International Reliability Physics Symposium*, 2010.

[23] T. Grasser, H. Reisinger, W. Goes et al., "Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise," in *IEEE International Electron Devices Meeting*, pp. 1–4, 2009.

[24] S. Makram-Ebeid and M. Lannoo, "Quantum model for phonon-assisted tunnel ionization of deep levels in a semiconductor," *Physical Review B*, vol. 25, no. 10, pp. 6406–6424, 1982.

[25] S. D. Ganichev, W. Prettl, and I. N. Yassievich, "Deep impurity-center ionization by far-infrared radiation," *Physics of the Solid State*, vol. 39, no. 11, pp. 1703–1726, 1997.

[26] X. Ji, Y. Liao, F. Yan, Y. Shi, G. Zhang, and Q. Guo, "The energy distribution of NBTI-induced hole traps in the Si band gap in PNO pMOSFETs," in *Proceedings of the IEEE International Reliability Physics Symposium (IRPS '12)*, XT.12.5, p. XT.12.1, Anaheim, Calif, USA, April 2012.

[27] F. Schuler, R. Degraeve, P. Hendrickx, and D. Wellekens, "Physical charge transport models for anomalous leakage current in floating gate-based nonvolatile memory cells," *IEEE Transactions on Device and Materials Reliability*, vol. 2, no. 4, pp. 80–88, 2002.

[28] M. O. Andersson, Z. Xiao, S. Norrman, and O. Engström, "Model based on trap-assisted tunneling for two-level current fluctuations in submicrometer metalsilicon-dioxidesilicon diodes," *Physical Review B*, vol. 41, no. 14, pp. 9836–9842, 1990.

[29] R. Degraeve, F. Schuler, B. Kaczer et al., "Analytical percolation model for predicting anomalous charge loss in flash memories," *IEEE Transactions on Electron Devices*, vol. 51, no. 9, pp. 1392–1400, 2004.

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Research Article

DC Characteristics Optimization of a Double G-Shield 50 V RF LDMOS

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An N-type 50 V RF LDMOS with a RESURF (reduced surface field) structure of dual field plates (grounded shield, or G-shield) was investigated. The effect of the two field plates and N-drift region, including the junction depth and dopant concentration, on the DC characteristics was analyzed by employing the Taurus TCAD device simulator. A high BV (breakdown voltage) can be achieved while keeping a low R_{DSON} (on-resistance). The simulation results show that the N-drift region dopant concentration has an obvious effect on the BV and R_{DSON} and the junction depth affected these values less. There is an optimized length for the second field plate for a given dopant concentration of the N-drift region. Both factors should be optimized together to determine the best DC characteristics. Meanwhile, the effect of the first field plate on the BV and R_{DSON} can be ignored. According to the simulation results, 50 V RF LDMOS with an optimized RESURF structure of a double G-shield was fabricated using 0.35 μm technologies. The measurement data show the same trend as the TCAD simulation, where a BV of 118 V and R_{DSON} of 26 ohm·mm were achieved.

1. Introduction

A RF LDMOS (radio frequency lateral double diffused metal oxide silicon) device is a competitive power device. It was initially used to displace the bipolar transistor for cellular infrastructure applications [1, 2]. It achieves good linearity, high gain, high breakdown voltage, high output power, high efficiency, good thermal stability, and good broadband match characteristics and is easy to integrate with the MOS process [3, 4]. It is also much cheaper than GaAs devices. It can cover a frequency range of 1 MHz to 4 GHz [5, 6]. Because of these merits, it is widely used as a power amplifier in GSM, PCS, and W-CDMA cellular infrastructure, wireless broadcast, industry, science, medical ISM, and radar [7, 8]. Among them, a 50 V RFLDMOS device is mainly used in wireless broadcast, ISM, and radar, which require a higher breakdown voltage and power density [9, 10].

For a 50 V operation voltage device, the breakdown voltage must be higher than 110 V to guarantee reliable operation. To obtain a high breakdown voltage and maintain a low on-resistance, it is compulsory to adopt the RESURF structure. In RESULF technology, the vertical PN junction depletion layer between the diffusion layer and substrate and its interaction with the lateral PN junction depletion region between the channel and diffusion layer are used to reduce the peak value of the surface electrical field to obtain a higher breakdown voltage. For a 50 V device with a fixed diffusion length, to obtain a high breakdown voltage and low on-resistance, it is not sufficient to only adjust the electrical field distribution of the vertical and lateral PN junction. Introducing a field plate on top of the gate can reduce the feedback capacitance of the C_{GD} and increase the breakdown voltage of the device. The lateral and vertical PN junction distribution of the N-type diffusion region is primarily determined by the N-type implant energy and dose. The field-plate profile and the N-type diffusion region underneath further adjust the electrical field distribution. The impact of the breakdown voltage and on-resistance from the N-type diffusion region

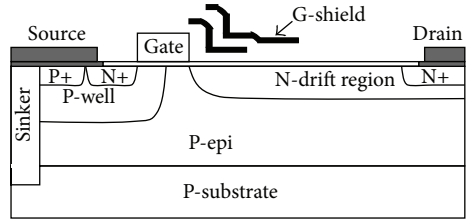

Figure 1: Diagram of the 50 V RFLDMOS device.

implant energy and dose and the length of dual field plate are investigated here. The best RESURF effect is achieved and confirmed by experiment. The device is optimized.

2. Device Structure Analysis

The breakdown voltage of 50 V operation voltage RLDMOS is determined both laterally and vertically. The vertical breakdown voltage is determined by the diffusion region depth and dopant concentration with the epitaxy layer thickness and dopant concentration. Apart from these factors, the lateral breakdown voltage is directly related to the N-type drift region length and surface electrical field distribution of the drift region. The thickness of a P-type epitaxy layer under an N-type drift region is normally sufficiently high that the device breakdown voltage is determined by the lateral breakdown. Figure 1 shows a structural illustration of the 50 V RFLDMOS device. Under the N-drift region is the P-epitaxy layer, which has a lower dopant concentration. Under a high drain voltage, the N-drift region is fully depleted until the edge of the drain under a lateral and vertical electrical field. The dual field plate is used to adjust the N-drift region surface electrical field distribution.

3. Results and Discussion

Device simulation is performed using the TCAD software Taurus. The device structure of the 50 V RFLDMOS is analyzed in detail, including the dual field-plate length, N-type lightly doped drift-region dopant concentration, and junction depth. The effect of the device DC characteristics is simulated. Based on this simulation, the device is fabricated using 0.35 μm technologies; silicon data are collected and compared to confirm the accuracy of the simulation. Finally, the optimized device DC performance is obtained.

The breakdown voltage of the LDMOS device is primarily determined by the length and dopant concentration of the N-type lightly doped drift region. When the vertical breakdown voltage is sufficiently high, the longer N-type lightly doped drift-region length results in a higher breakdown voltage and on-resistance. To reduce the on-resistance, the N-type lightly doped drift-region dopant concentration must be increased; however, in that case, the N-type lightly doped drift region is difficult to be fully depleted, which reduces the breakdown voltage. Thus, there is a tradeoff between the breakdown voltage and on-resistance. It is obvious that obtaining better device DC performance requires considering the length and dopant concentration and junction depth of the N-type lightly doped drift-region all together. For convenience in this study, the drift-region length of the device is fixed at 5 μm. This paper focuses on the impact of the field-plate profile and N-type lightly doped drift-region dopant concentration on the electrical field distribution and main device DC characteristics.

3.1. The Impact of the N-Type Lightly Doped Drift-Region Concentration and Junction Depth on the Breakdown Voltage and On-Resistance. The N-type lightly doped drift-region dopant concentration and junction depth are determined by the N-type implant dosage and energy, respectively. When the length of dual field plate is fixed, the relationship of the implant dosage and energy to the breakdown voltage and on-resistance can be obtained using the TCAD simulation, as illustrated in Figure 2.

As illustrated in Figure 2(a), when the field-plate structure is fixed, there is a peak value of the breakdown voltage BV versus N-type implant dose. The implant dose corresponds to a peak BV which is $1.6e12\,\mathrm{cm}^{-2}$. As the implant dose increases, the breakdown voltage BV decreases. This finding indicates that, for a fixed field-plate structure, there is an optimized implant dose or, in other words, an optimized N-type lightly doped drift-region dopant concentration. This result can be explained by the change in the surface electrical field distribution of the drift region. Figure 3 gives the electrical field distribution curves near the breakdown for different dopant concentrations. A few peaks appear on the surface electrical field of the drift region. Three peaks appear at the two field-plate edges and the boundary of the drift region to the drain terminal. When the dopant concentration is high, the field plate has a stronger effect on the electrical field. The peak electrical field is under the field plate, where the avalanche breakdown occurs. When the dopant concentration is low, the peak electrical field is at the boundary of the drift region to drain terminal. The area under the electrical field curve is indicative of the breakdown voltage BV. To obtain the largest breakdown voltage BV, which corresponds to the largest area under the electrical curve, the dopant concentration should be selected properly to obtain three electrical field peaks that are more uniformly distributed. Dopant concentrations that are either too high or too low are detrimental to the final device breakdown voltage. In Figure 2(a), the breakdown voltage slightly increased when the N-type implant energy increased. When the implant energy increased, the junction depth of

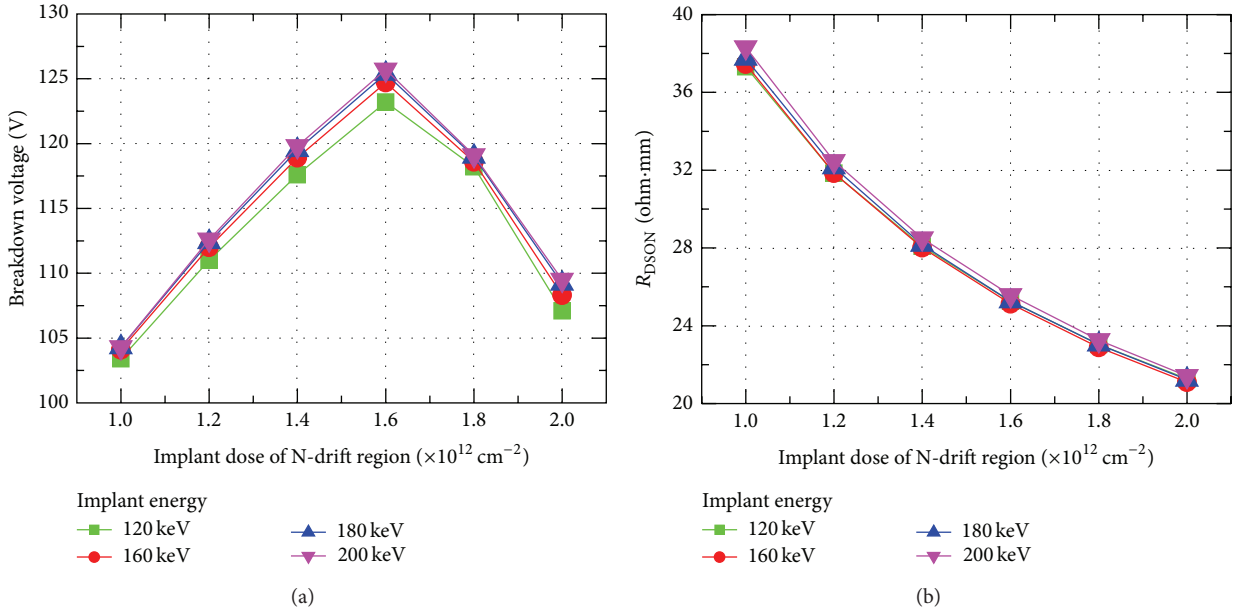

FIGURE 2: Relationship of the (a) breakdown voltage and (b) on-resistance (R_{DSON}) to the implant dose and energy of the N-drift region.

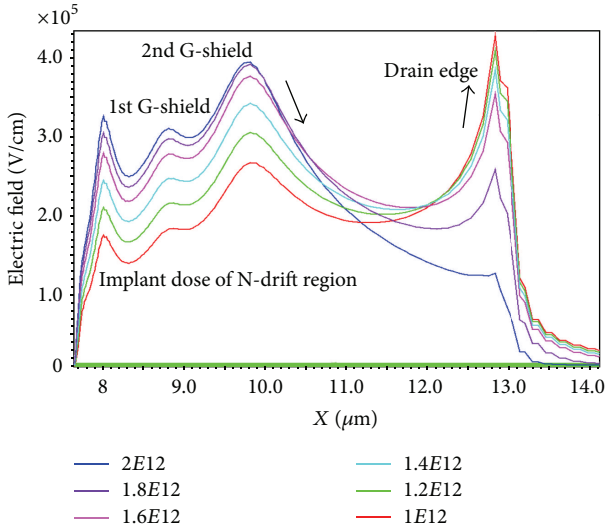

FIGURE 3: Crucial electric field distribution along the surface of N-drift region when breakdown occurs for different given implant energies of the N-drift region.

the N-type lightly doped drift region increased, and the surface dopant concentration decreased. This makes the electrical field distribution at the drift region surface more uniform, which helps increase the breakdown voltage.

The device on-resistance R_{DSON} decreases as the implant dose increases, as illustrated in Figure 2(b). They are inversely proportional because the on-resistance R_{DSON} is primarily determined by the dopant concentration of the N-type lightly doped drift region. From Figure 2(b), we can also observe that the on-resistance R_{DSON} is less impacted by the implant energy because the carrier goes through a wide conduction path. Even if the implant energy increases, there is less change in the overall dopant concentration of the drift region.

3.2. Impact of the Double G-Shield Structure on the Breakdown Voltage and RDSON. The field plate of the RFLDMOS is initially used to block the gate to reduce the feedback capacitance C_{GD} between the drain and gate to improve the RF performance of the device. When the vertical distance of the field plate to the N-type lightly doped drift region decreases, its impact on the surface electrical field distribution of the drift region becomes stronger. Thus, the field plate is also a very important factor to the device breakdown voltage. For the 50 V RFLDMOS device, dual field plates are adopted to obtain good RESURF effect. The profile of the dual field plate, particularly the length, determines the device breakdown voltage. The relation of the breakdown voltage to the length of the field plate is analyzed in detail for a fixed implant dose of the N-type drift region by the TCAD simulation. The optimized field-plate dimension is obtained.

Figure 4 shows the device breakdown voltage versus the second field-plate length with the first field-plate length fixed at 0.8 μm. The impact of the first field plate on the device breakdown voltage will be explained later. For a fixed N-type implant dose that corresponds to a fixed drift-region dopant concentration, the breakdown voltage BV first increases, then reaches a peak value, and finally decreases as the length further increases when the second field plate increases from 1 μm to 2.5 μm.

The optimized length of the second field plate corresponding to the peak breakdown voltage BV is not the same for different dopant concentrations of drift region. As shown in Figure 4, the length of the second field plate corresponding to the peak breakdown voltage is longer for a high implant dose or higher concentration of the N-type lightly doped drift

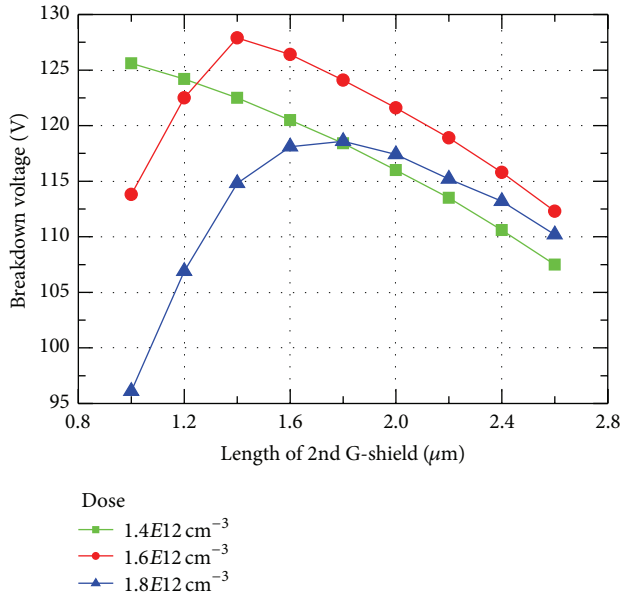

FIGURE 4: Relationship between the breakdown voltage and length of the 2nd G-shield with respect to different implant doses for a given implant energy of the N-drift region.

region. If the concentration of the N-type lightly doped drift region is low, for example, at an implant dose of $1.4e12\ \text{cm}^{-2}$, then the length of second field plate corresponding to the peak breakdown voltage is shorter, which is close to that of the first field plate.

Figure 5(a) illustrates the lateral electrical field distribution of the N-type drift region at the voltage near breakdown when the N-type implant dose is relatively high (= $1.8e12\ \text{cm}^{-2}$). There are three obvious peaks at the edge of the drain and dual field plate. Because the drift region has a high dopant concentration, the peak electrical field at the second field plate is higher than the drain edge. Considering an extreme case when the second field plate is short (L_2 = 1 um) and close to the first field plate, the second field plate is blocked by the first field plate because of the small distance of the first field plate to the drift region, so a very high peak electrical field exists under the field plate and very low electrical field at the drain edge. Overall, the electrical field curve is very steep, which is detrimental to obtaining a high breakdown voltage. When the length of second field plate further increases, the two peak positions of the electrical field corresponding to the two field plates gradually detach. When the second field plate is closer to the drain, it has more control over the electrical field. Its electrical field peak value is always higher than the first field plate. The strongest point of impact ionization, that is, the breakdown point, always exists under the second field plate. When the length of the second field plate gradually increases, dragged by the electrical field under the second field plate, the electrical field at the drain edge also gradually increases. When the length of the second field plate is long (i.e., L_2 = 2.6 um), both the electrical fields under the second field plate and at the drain edge have high peak values. This will block the first field plate and reduce its control over the drift region. The peak value of the electrical field under the first field plate is low, and the distribution is not smooth, which corresponds to a low breakdown voltage BV. Therefore, when the length of second field plate is 1.8 μm, the corresponding electrical field curve is the smoothest; the highest breakdown voltage of 118 V can be achieved at this dopant concentration.

Figure 5(b) shows the lateral electrical field distribution of the drift region at different second field-plate lengths when the N-type implant dose is $1.4e12\ \text{cm}^{-2}$. The trend is similar to that observed for the higher drift-region dopant concentration. The biggest difference is that the highest peak always occurs at the drain edge. The breakdown point is also at this point because the whole drift region is fully depleted and the depletion region extends to the very high doped $n+$ region at high applied voltage. When all of the electrical lines terminate at the drain region, the drain terminal has the highest electrical field and thus breaks down first. In that case, shorter lengths of the second field plates result in higher areas under the electrical field curve and higher breakdown voltages. In such cases, there is less difference between the electrical field distribution of the dual field plates and that of single field plate.

The impact of the first field plate is not considered when discussing the impact of the profile of the dual field plates to breakdown voltage As illustrated in Figure 6, this impact of first field-plate length to breakdown voltage is minor when the second field-plate length is fixed, based on silicon data. The most obvious impact on the device characteristics is the hot carrier injection because the electrical field underneath the gate becomes stronger when the first field plate gets closer to the gate.

It is beneficial to maintain a low drift-region dopant concentration to obtain a higher breakdown voltage. However, the device on-resistance R_{DSON} is inversely proportional to the N-type drift-region dopant concentration. Considering both the breakdown voltage BV and on-resistance R_{DSON}, it is imperative to maintain a higher N-type drift-region dopant concentration. Thus, in order to maintain a lower on-resistance R_{DSON}, device is optimized by utilizing the RESURF effect of dual field plate; a high breakdown voltage can be obtained by adopting an optimized field-plate dimension. It is also helpful to increase the device saturation current Idsat by keeping a higher N-type drift-region dopant concentration.

A 50 V RFLDMOS dual field plate device is fabricated using 0.35 μm technologies. For a fixed implant energy, the silicon data of device breakdown voltage versus the second field-plate length and N-type drift-region dopant concentration is illustrated in Figure 7. Compared with simulation data of Figure 4, the trend observed for the measured data matches the simulation data well. There is an optimized value of the drift-region concentration and second field-plate length. The simulation data predicts the device characteristics well.

Finally, based on the simulation and experiment data, device is optimized by using the following conditions: the N-type drift-region implant dose is $1.6e12\ \text{cm}^{-2}$, and the second field-plate length is 1.8 μm, which achieves a compromise of

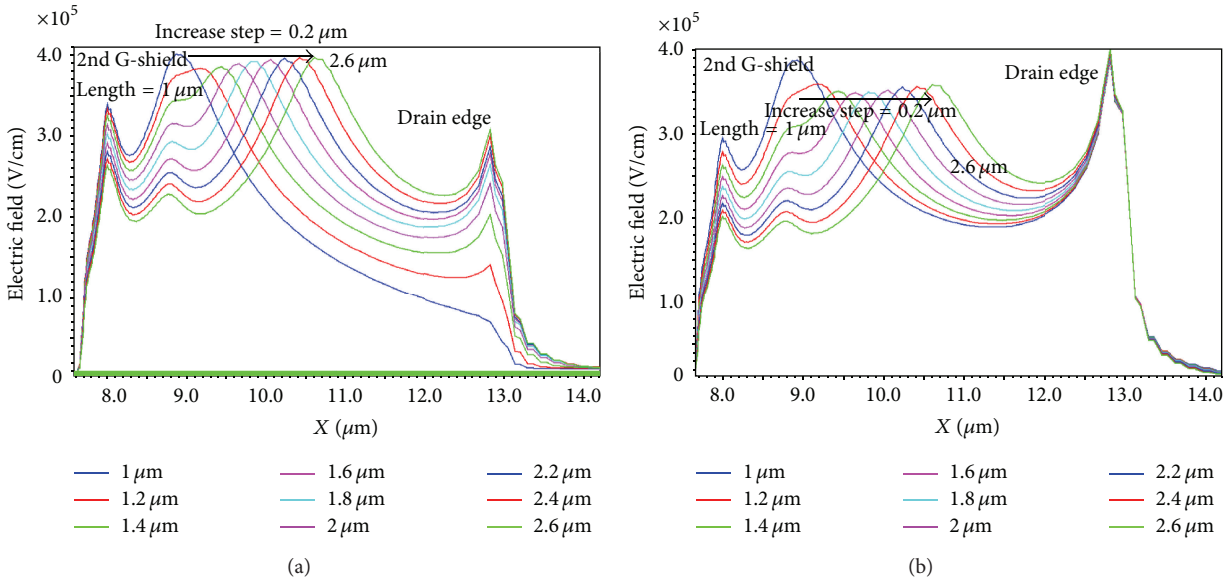

FIGURE 5: For (a) a high implant dose of 1.8e12 cm^{-2} and (b) a low implant dose of 1.4e12 cm^{-2}, the crucial electric field distribution along the surface of the N-drift region is determined by the length of the 2nd G-shield.

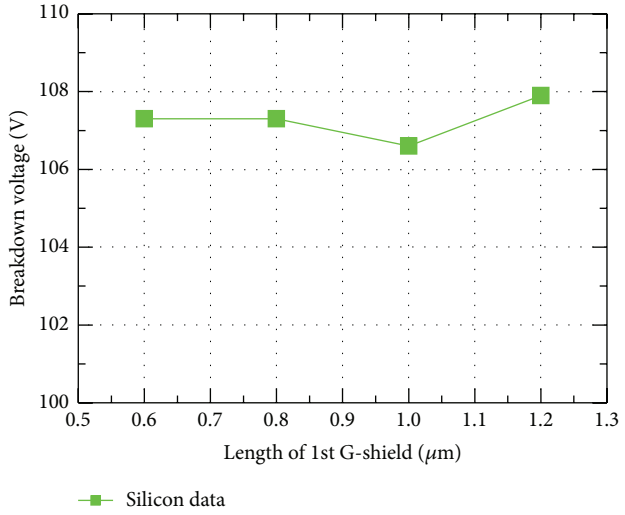

FIGURE 6: Relationship between first G-shield length and the breakdown voltage for a fixed length of 2nd G-shield and other conditions.

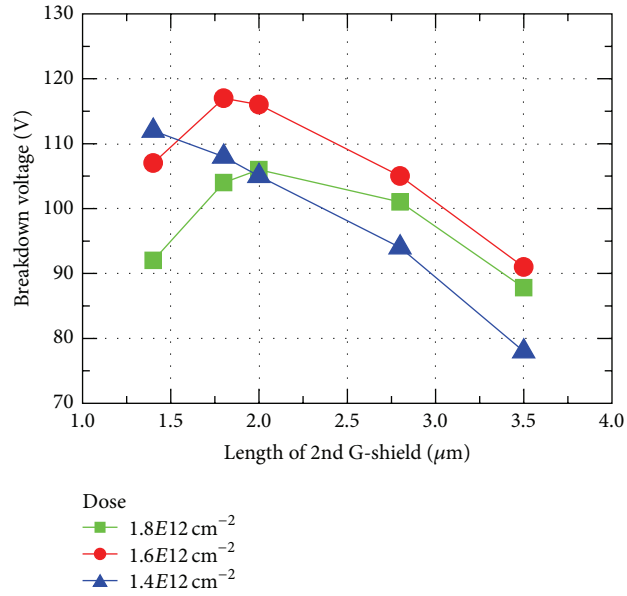

FIGURE 7: Silicon data of the effect of the 2nd G-shield length on the breakdown voltage.

the breakdown voltage and on-resistance. The competitive device performance of breakdown voltage 118 V and the on-resistance 26 ohm·mm is achieved. Figure 8 gives the device I_d-V_g and I_d-V_d curve. The cross-section view of the device TEM is illustrated in Figure 9.

4. Conclusion

The factors that affect the 50 V RFLDMOS DC characteristics are reviewed by performing device simulation using the TCAD software Taurus. The effects of the N-type drift-region dopant concentration, junction depth, and dimension of dual field plates on the breakdown voltage BV and on-resistance R_{DSON} are analyzed. The real silicon data show the same trend as that of the simulation results. The junction depth of the N-type drift region has less effect on the DC characteristics. A high N-type drift-region dopant concentration is beneficial to obtain a lower on-resistance R_{DSON}. However, a low N-type drift-region dopant concentration allows for a higher breakdown voltage. There are optimum field-plate dimensions for different N-type drift-region dopant concentrations, particularly for the second field plate. Based on simulation

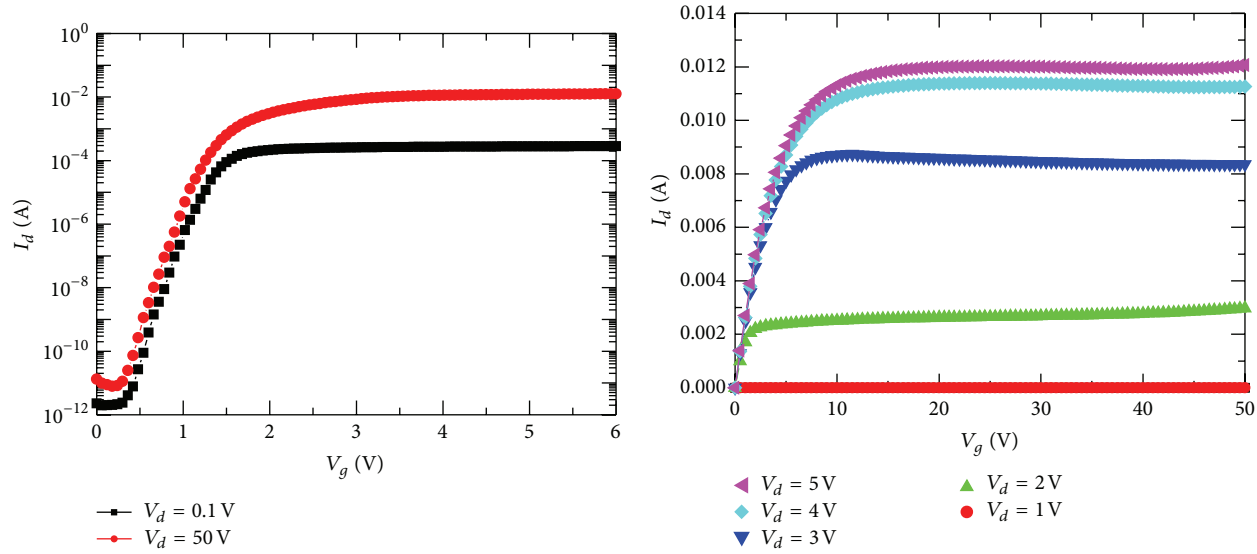

FIGURE 8: Optimized device characteristics (a) I_d-V_g curve and (2) I_d-V_d curve.

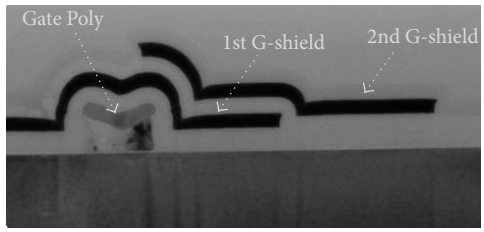

FIGURE 9: TEM picture of the optimized double G-shield RFLDMOS cross-section.

data, an experiment is performed to determine the relationship of the BV to the second field-plate length and N-type drift-region dopant concentration. The trend from the real silicon data matches the simulation well. The device is optimized by choosing an N-type drift-region implant dose of $1.6e12\ \text{cm}^{-2}$ and a second field-plate length of 1.8 μm, which results in an excellent balance between the breakdown voltage BV and on-resistance R_{DSON}. The breakdown voltage is 118 V, and the on-resistance is 26 ohm·mm. Based on this result, if other factors such as the dielectrics under the field plate are also considered, the device DC characteristics can be further improved. In summary, the device structure applies the RESURF effect, and good device optimization is achieved without additional process steps. This is very useful for real applications.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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References

[1] A. Wood, C. Dragon, and W. Burger, "High performance silicon LDMOS technology for 2 GHz RF power amplifier applications," in *Proceedings of the IEEE International Electron Devices Meeting*, pp. 87–90, December 1996.

[2] H. F. F. Jos, "Novel LDMOS structure for 2 GHz high power basestation application," in *Proceedings of the European Microwave Conference*, pp. 739–744, 1998.

[3] H. Brech, W. Brakensiek, D. Burdeaux et al., "Record efficiency and gain at 2.1 GHz of high power RF transistors for cellular and 3G base stations," in *Proceedings of the IEEE International Electron Devices Meeting, Technical Digest (IEDM '03)*, pp. 15.1.1–15.1.4, Washington, DC, USA, December 2003.

[4] F. Van Rijs and S. J. C. H. Theeuwen, "Efficiency improvement of LDMOS transistors for base stations: towards the theoretical limit," in *Proceedings of the International Electron Devices Meeting (IEDM '06)*, pp. 205–208, December 2006.

[5] F. van Rijs, "Status and trends of silicon LDMOS base station PA technologies to go beyond 2.5 GHz applications," in *Proceedings of the IEEE Radio and Wireless Symposium (RWS '08)*, pp. 69–72, Orlando, Fla, USA, January 2008.

[6] S. J. C. H. Theeuwen and H. Mollee, "*S*-band radar LDMOS transistors," in *Proceedings of the 4th IEEE European Microwave Integrated Circuits Conference (EUMIC '09)*, pp. 53–56, 2009.

[7] D. Vye, L. Pelletier, S. Theeuwen et al., "The new power brokers: high voltage RF devices," *Microwave Journal*, vol. 7, pp. 22–40, 2009.

[8] K. Werner and S. Theeuwen, "RF driven plasma lighting—the next revolution in light sources are powered by solid state RF technology," *Microwave Journal*, vol. 53, no. 12, pp. 68–74, 2010.

[9] S. J. C. H. Theeuwen, W. J. A. M. Sneijers, J. G. E. Klappe, and J. A. M. de Boet, "High voltage RF LDMOS technology for broadcast applications," in *Proceedings of the 3rd European Microwave Integrated Circuits Conference (EuMIC '08)*, pp. 24–27, 2008.

[10] P. Piel, W. Burger, D. Burdeaux, and W. Brakensiek, "50 VRFLDMOS: an ideal RF power technology for ISM, broadcast, and radar applications," White Paper, Freescale Seminconductor, Tempe, Ariz, USA, 2011.

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Research Article

Design of a Novel W-Sinker RF LDMOS

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A novel RF LDMOS device structure and corresponding manufacturing process are presented in this paper. Deep trench W-sinker (tungsten sinker) is employed in this technology to replace the traditional heavily doped diffusion sinker which can shrink chip size of the LDMOS transistor by more than 30% and improve power density. Furthermore, the W-sinker structure reduces the parasitic resistance and inductance and improves thermal conductivity of the device as well. Combined with the adoption of the techniques, like grounded shield, step gate oxide, LDD optimization, and so forth, an advanced technology for RF LDMOS based on conventional 0.35 μm CMOS technology is well established. An $F + A$ power amplifier product with frequency range of 1.8–2.1 GHz is developed for the application of 4G LTE base station and industry leading performance is achieved. The qualification results show that the device reliability and ruggedness can also meet requirement of the application.

1. Introduction

Laterally diffused metal-oxide-semiconductor (LDMOS) technologies have been the first choice in wireless base station applications for nearly the last 20 years due to their high gain, high efficiency, superior linearity [1, 2], and being easy to integrate with CMOS technology [3, 4]. RFLDMOS provides the most cost-effective solution for the base station system applications because it can be fabricated with low-cost and mature Si process compared with GaAs and GaN technology. Moreover, LDMOS transistors can be used at high frequencies to achieve a high continuous peak power [5, 6]. Because of these merits, RF LDMOS can also be used in a wide range of applications requiring radio frequency power amplifier like broadcast, pulsed radar, ISM (industrial, scientific, and medical) applications, and so forth [7–9].

In this study, a novel RF LDMOS device structure and corresponding manufacturing process are proposed and developed based on conventional 0.35 μm CMOS technology, and deep trench W-sinker (tungsten sinker) is employed in this technology to replace the traditional heavily doped diffusion sinker to realize an effective connection from source to the back side of the substrate, which reduces chip size and also improves power density of the device greatly. Combined with the adoption of the techniques like G-shield (grounded shield), step gate oxide, LDD optimization, and so forth, an advanced technology for RF LDMOS is well established. An $F + A$ power amplifier product with frequency range of 1.8–2.1 GHz is developed for the application of 4G LTE base station. Both DC and RF performance of the device are evaluated and the results show that industry leading performance is achieved. Besides, the qualification results show the device reliability and ruggedness can also meet requirement of the application.

This paper is organized as follows. Section 2 describes the design of the proposed W-sinker RF LDMOS device structure and corresponding manufacturing process. In Section 3, device measurement results are presented including DC, RF, and ruggedness. In Section 4, conclusion is given.

2. The Proposed Device Structure and Process Features

The cross-sectional view of the proposed device, shown in Figure 1, is based on conventional 0.35 μm CMOS technology, which consists of drain, source, gate, N-LDD (lightly doped

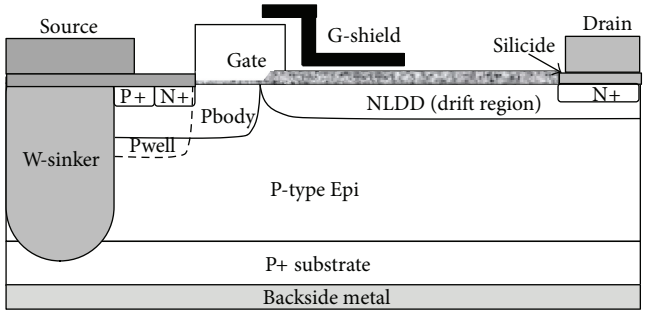

Figure 1: The proposed W-sinker RF LDMOS device structure.

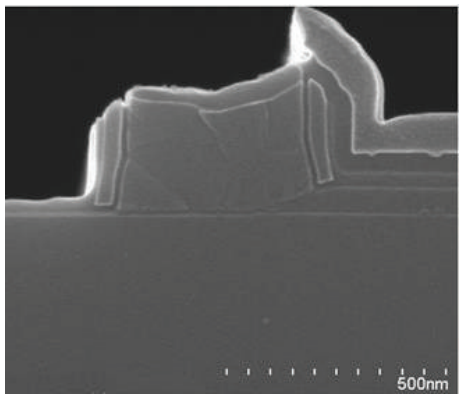

Figure 2: Cross-sectional SEM view of fabricated step gate oxide structure.

drain extension), G-shield (grounded shield), and sinker. A lightly doped epitaxial layer with certain thickness is grown on the highly doped Si substrate to meet the requirement of breakdown voltage for the transistor. A tungsten G-shield plate formed between gate and drain not only reduces the feedback capacitance Cgd but also improves the reliability of the device by reducing the peak electric field at the gate-edge and the drift region. By optimizing the dopant and length of the N-LDD, high breakdown voltage, low on-resistance, and low HCI (hot carrier injection) could be realized. Gate is formed by Ti-salicided polysilicon with sheet resistance lower than 1.5 ohm, which could ensure power swing under high frequency and low power loss of the large power device composed of multifinger; hence both efficiency and power density could be improved. The back-end which consists of three metal layers and total 10 μm thick interlayer dielectric helps to reduce the output capacitance, and 3 μm thick top metal further makes the device low parasitic metal resistance, good electromigration (EM) reliability. Step gate oxide structure is adopted as shown in Figure 2, and the thermal gate oxide is thin at the source side and is tapered to a thicker oxide at the drain side, which not only reduces input capacitance Ciss, output capacitance Coss, and feedback capacitance Cgd, but also improves power gain and reliability of the device [10]. Furthermore, self-align channel is formed by the lateral diffusion of boron ions which is implanted self-aligned to the gate, and extremely short and uniform channel can be achieved

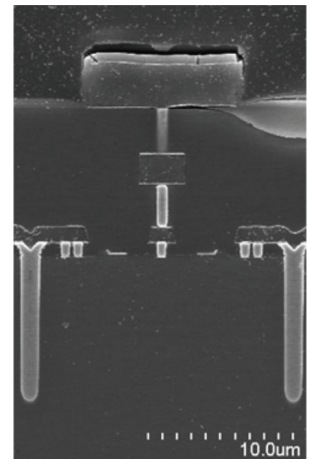

Figure 3: Cross-sectional SEM view of the fabricated RF LDMOS.

even without high resolution photolithograph process and thus also enhances the gain and reliability of device.

Many techniques have been used to improve power density of RF LDMOS device. For example, RESURF (reduced surface field) method and triple G-shield have been adopted in [10]. In this study, a novel W-sinker (tungsten sinker) is employed in the RF LDMOS device to replace the traditional heavily doped diffusion sinker to realize ultralow resistance connection from source to the back side of the substrate; the W-sinker is formed by deep trenching to the P+ substrate and filling it with chemical vapor deposited tungsten, and then the trench is planarized by CMP (chemical mechanical polishing). Compared with the conventional diffusion sinker, by adopting W-sinker, the chip size of RF LDMOS device can be reduced by more than 30% and power density of the device can also be greatly improved. Although trenched sinker LDMOSFET (TS-LDMOS) structure has been proposed in [11] in which the trench is filled with highly doped polysilicon, the W-sinker proposed in this study still has many advantages over the trenched poly sinker. Firstly, the resistivity of tungsten material is normally 2 orders lower than that of polysilicon even if it is heavily doped. For example, at room temperature (20°C), the resistivity of tungsten is about 5.48×10^{-6} ohm-cm while the resistivity of heavily doped silicon is about 1.17×10^{-3} ohm-cm under boron dosage of 1×10^{20} cm^{-3}. Secondly, the trench filling capability of tungsten is better than polysilicon; in particular, it is shown to be more beneficial when it comes to high aspect ratio of the trench. For a RF LDMOS device of 50 V operating voltage, the EPI thickness reaches around 9-10 μm, the trench depth is required to be even higher, and W-sinker is more adoptable. Thirdly, polysilicon is apt to yield stress on the wafer compared with tungsten due to different material properties; in the followed up high temperature processes, drastic stress changes caused by poly recrystallization may lead to dislocation, device leakage, and reliability failure of the power device.

The cross-sectional SEM view of the fabricated W-sinker RF LDMOS is shown in Figure 3, where the W-sinker has depth of 10 μm and width of 1 μm, respectively.

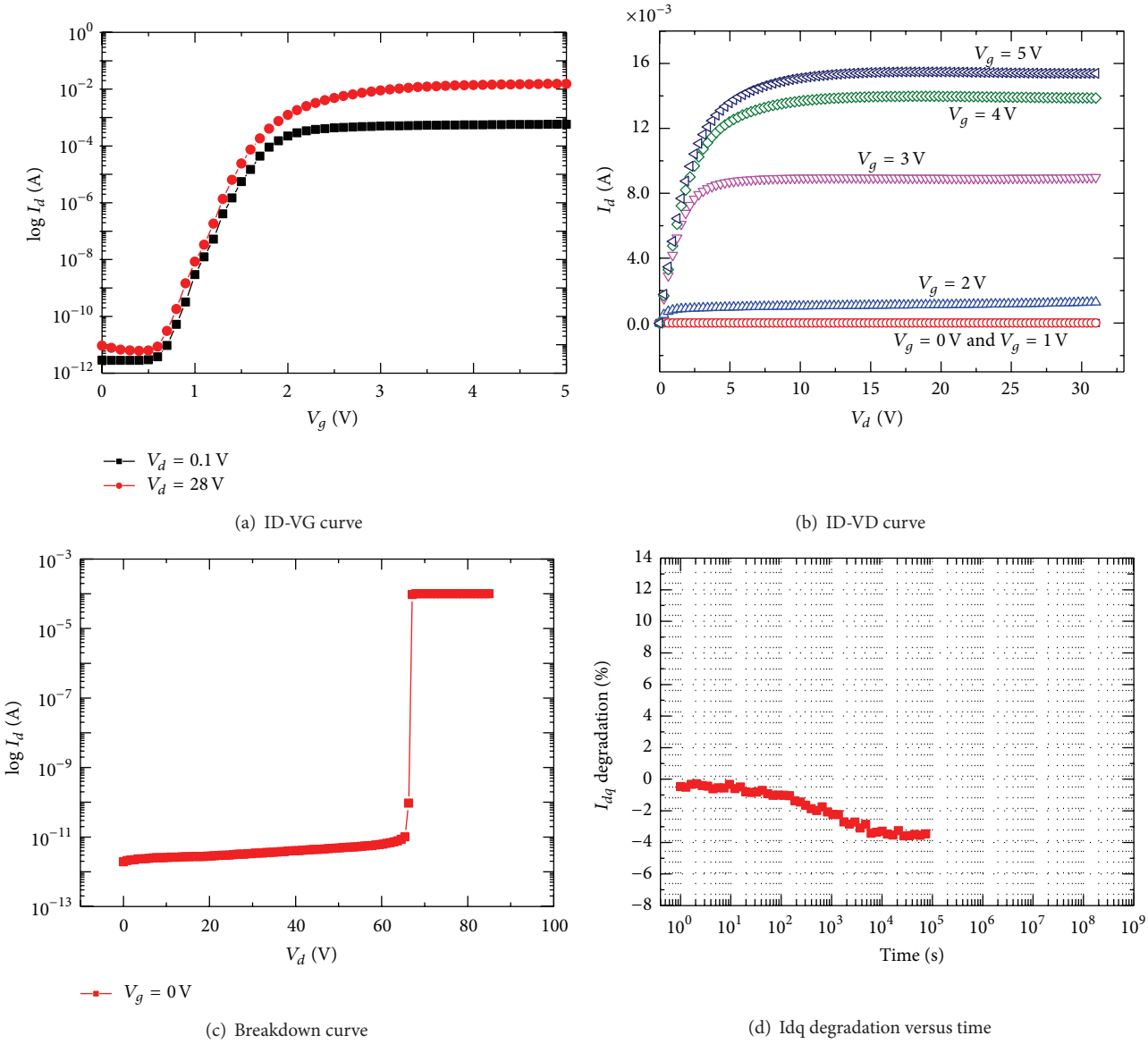

FIGURE 4: DC characteristics of W-sinker RF LDMOS device (W = 80 um).

3. Test Results of the Fabricated RF LDMOS Device

Based on the W-sinker RF LDMOS device structure and technology described in Section 2, a 30 V/100-Watt $F + A$ power amplifier (PA) product for the application of 4G LTE base station is developed; DC characteristics of a single transistor device (width = 80 μm), RF performance, and ruggedness of the $F + A$ power amplifier product are evaluated, and the results are shown as follows.

3.1. DC Characteristics. Instead of the $F + A$ PA product, DC characteristics of the single transistor device (width = 80 um) are measured due to the ability of Agilent 1500A tester. Test results are shown in Figure 4(a) ID-VG curve, Figure 4(b) ID-VD curve, and Figure 4(c) breakdown curve, and the device achieves a breakdown voltage of 67 V, threshold voltage of 1.2 V, and saturation current (Idsat) of 204 μA/μm with gate and drain biased on 5 V and 28 V, respectively.

Furthermore, the degradation experiments of quiescent current (Idq) are conducted to investigate HCI concern. During the test, the RF LDMOS device is stressed under Vd = 28 V and Id = 5 μA/μm which is a typical DC bias for class AB amplifier of base station application. The measurement results of Idq degradation are shown in Figure 4(d), and Idq degradation is concluded to be less than 5% in 20 years, which meets the requirements of various applications of the industry.

3.2. RF Performance. The RF performance of the $F + A$ PA product is characterized by focus load pull measurement system (Figure 5(a): the picture of the system; Figure 5(b): its

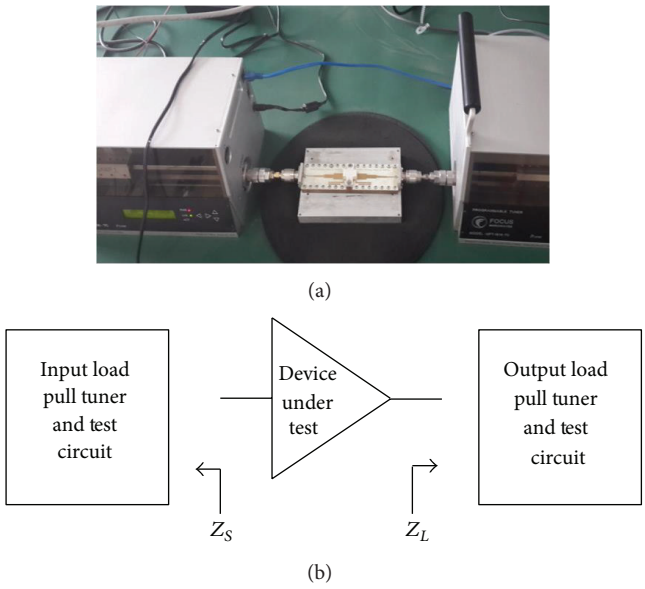

Figure 5: (a) Focus load pull system and (b) its schematic diagram.

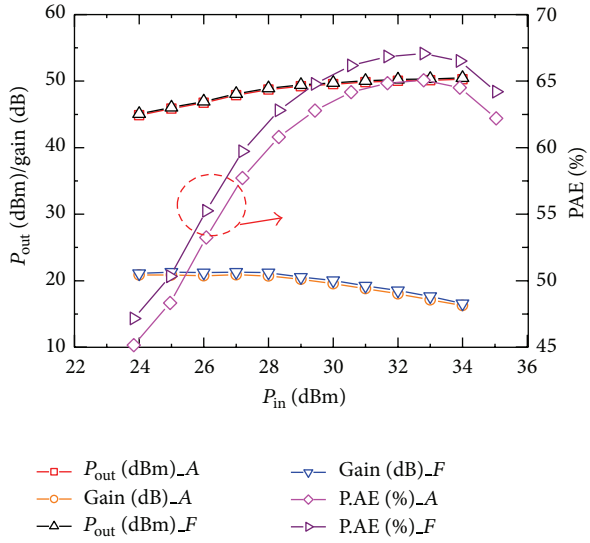

Figure 6: Output power, gain, and PAE versus input power for the 100-Watt $F + A$ product.

Table 1: RF performance of the W-sinker RF LDMOS product.

(a)

Frequency	Zsource	
	Real	Imag.
1880 MHz	11.604	9.494
2025 MHz	2.354	−3.706

(b)

Frequency	Zpwr				
	Real	Imag.	Gain (dB)	PAE (%)	P3dB (dBm)
1880 MHz	1.6	−3.001	18.66	57.8	50.22
2025 MHz	1.447	−3.22	18.42	58.3	50.03

(c)

Frequency	Zeff				
	Real	Imag.	Gain (dB)	PAE (%)	P3dB (dBm)
1880 MHz	1.081	−1.971	21.3	67.7	48.79
2025 MHz	0.813	−2.325	20.81	65.1	48.11

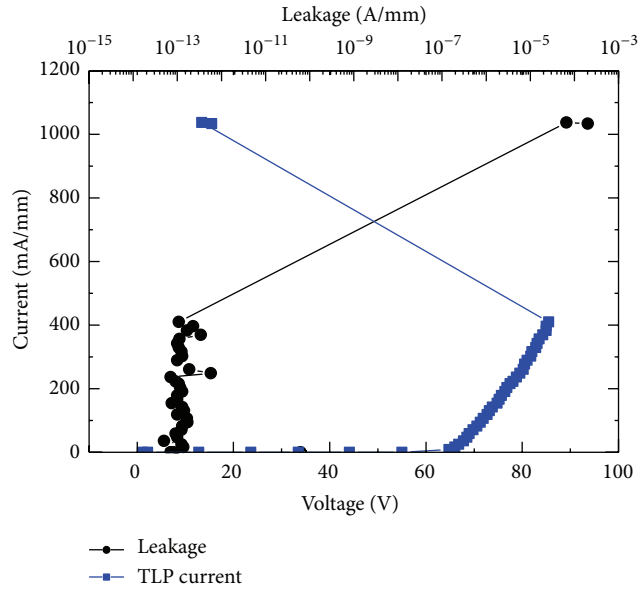

Figure 7: TLP result of the 100-Watt $F + A$ PA product.

schematic diagram). The device is stressed under Vd = 28 V and Id = 5 mA/mm which is the same as actual operating conditions of base station application, and the RF input is pulsed CW (continuous wave) signal with 40 μs pulse width and 4% duty cycle. Test results are shown in Table 1; the RF linear gain is 21 dB, the PAE (power added efficiency) is near 68% with the frequency of 1880 MHz at F band, output power at 3 dB gain compression point (P3dB) reaches 50.2 dBm, and power density is over 1.16 W/mm. And the performance only shows a slight drop with the frequency of 2025 MHz at A band. The detailed output power, gain, and PAE versus input power for 100-Watt $F + A$ product are shown in Figure 6. Industry advanced performance is achieved [10].

3.3. Ruggedness. The device ruggedness is one of the important intrinsic reliability factors for RF LDMOS as challenging electrical and thermal environments are presented for the device in RF power applications. The most common ruggedness failure mechanism for LDMOS devices is the catastrophic failure resulting from the snapback of a parasitic bipolar junction transistor of the device [12]. TLP (transmission line pulse) measurement can be used to characterize the device's breakdown behavior and evaluate the ruggedness performance. Due to the ability of TLP measurement tool Barth 4002, test is conducted on the single transistor device (width = 80 um). The result is shown in Figure 7. I_{t2} (secondary breakdown current) reached 400 mA/mm which indicates that the device has very good ruggedness.

For the high power PA devices, the ruggedness can be measured by the VSWR (voltage standing wave ratio) load mismatch test using the same system as RF test (Figure 5). Test results show that the $F + A$ PA product passes P10dB conditions at the drain voltage of 32 V with the VSWR 20 : 1 load terminal mismatch. In 20 : 1 VSWR output mismatch, 82% of the output power is reflected from the load back to the devices and only 18% is transmitted to the load. The device shows very good device ruggedness.

4. Conclusion

A novel W-sinker RF LDMOS device structure is proposed and corresponding manufacturing process is developed based on conventional 0.35 μm CMOS technology, and deep trench W-sinker is used to realize effective connection from source to the back side of the substrate. Compared to the conventional diffusion sinker, chip size can be reduced and power density of the device can be improved greatly. And the W-sinker proposed in this study also has advantages over the trenched poly sinker proposed by other works regarding the aspects of resistance, process adaptability, and stress. Combined with the adoption of the techniques like G-shield, step gate oxide, LDD optimization, and so forth, an advanced technology for RF LDMOS is well established. An $F + A$ power amplifier product is developed for the application of 4G LTE base station on this technology. Test results show that BV of 67 V and Idsat of 204 mA/mm are achieved. RF linear gain is 21 dB and the PAE is near 68% with the frequency of 1880 MHz at F band, output power at 3 dB gain compression point (P3dB) reaches 50.2 dBm, and power density is over 1.16 W/mm. All the parameters advance in the industry currently. Besides, the qualification results show the device reliability and ruggedness can also meet requirement of the application.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

The authors would like to gratefully acknowledge the contributions of many Huahong Grace colleagues for process and module development, device simulation and characterization, and helpful discussions. The authors would also like to give great thanks to Dajie Zeng and Nan Liu from Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, for supporting RF measurement and ruggedness evaluation. This study is financially supported by the Chinese National Key Project (no. 2012ZX02502).

References

[1] A. Wood, C. Dragon, and W. Burger, "High performance silicon LDMOS technology for 2GHz RF power amplifier applications," in *Proceedings of the IEEE International Electron Devices Meeting*, pp. 87–90, December 1996.

[2] H. F. F. Jos, "Novel LDMOS structure for 2 GHz high power basestation application," in *Proceedings of the 28th European Microwave Conference*, pp. 739–744, 1998.

[3] H. Brech, W. Brakensiek, D. Burdeaux et al., "Record efficiency and gain at 2.1 GHz of high power RF transistors for cellular and 3G base stations," in *Proceedings of the IEEE International Electron Devices Meeting—Technical Digest*, pp. 359–362, December 2003.

[4] F. van Rijs and S. J. C. H. Theeuwen, "Efficiency improvement of LDMOS transistors for base stations: towards the theoretical limit," in *Proceedings of the International Electron Devices Meeting (IEDM '06)*, pp. 1–4, San Francisco, Calif, USA, December 2006.

[5] F. van Rijs, "Status and trends of silicon LDMOS base station PA technologies to go beyond 2.5 GHz applications," in *Proceedings of the IEEE Radio and Wireless Symposium (RWS '08)*, pp. 69–72, Orlando, Fla, USA, January 2008.

[6] S. J. C. H. Theeuwen and H. Mollee, "S-band radar LDMOS transistors," in *Proceedings of the 4th European Microwave Integrated Circut Conference (EuMIC '09)*, pp. 53–56, 2009.

[7] R. Pengelly, D. Vye, L. Pelletier et al., "The new power brokers: high voltage RF devices," *Microwave Journal*, vol. 52, no. 6, pp. 22–40, 2009.

[8] K. Werner and S. Theeuwen, "RF driven plasma lighting—the next revolution in light sources are powered by solid state RF technology," *Microwave Journal*, vol. 12, pp. 68–74, 2010.

[9] P. H. Aaen, *Modeling and Characterization of RF and Microwave Power FETs*, chapter 1, 2007.

[10] S. J. C. H. Theeuwen and J. H. Qureshi, "LDMOS technology for RF power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1755–1763, 2012.

[11] C. S. Kim, J.-W. Park, and H. K. Yu, *Trenched Sinker LDMOSFET (TS-LDMOS) Structure for High Power Amplifier Application above 2 GHz*, IEDM 01-887, IEEE, 2001.

[12] D. Burdeaux and W. Burger, "Intrinsic Reliability of RF Power LDMOS FETs," IRPS11-435~443, 2011.

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Research Article

High-Electron-Mobility SiGe on Sapphire Substrate for Fast Chipsets

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High-quality strain-relaxed SiGe films with a low twin defect density, high electron mobility, and smooth surface are critical for device fabrication to achieve designed performance. The mobilities of SiGe can be a few times higher than those of silicon due to the content of high carrier mobilities of germanium (p-type Si: 430 $cm^2/V{\cdot}s$, p-type Ge: 2200 $cm^2/V{\cdot}s$, n-type Si: 1300 $cm^2/V{\cdot}s$, and n-type Ge: 3000 $cm^2/V{\cdot}s$ at 10^{16} per cm^3 doping density). Therefore, radio frequency devices which are made with rhombohedral SiGe on *c*-plane sapphire can potentially run a few times faster than RF devices on SOS wafers. NASA Langley has successfully grown highly ordered single crystal rhombohedral epitaxy using an atomic alignment of the [111] direction of cubic SiGe on top of the [0001] direction of the sapphire basal plane. Several samples of rhombohedrally grown SiGe on *c*-plane sapphire show high percentage of a single crystalline over 95% to 99.5%. The electron mobilities of the tested samples are between those of single crystals Si and Ge. The measured electron mobility of 95% single crystal SiGe was 1538 $cm^2/V{\cdot}s$ which is between 350 $cm^2/V{\cdot}s$ (Si) and 1550 $cm^2/V{\cdot}s$ (Ge) at $6 \times 10^{17}/cm^3$ doping concentration.

1. Introduction

The clock frequency of conventional silicon based chipset has achieved several gigahertz' levels by increasing line resolution of microcircuit. Time after time, critics have claimed that silicon transistors of smaller dimensions will soon come to the end of shrinking. Also, further speed enhancement faces intrinsic limit by the material properties, such as electron charge mobility. Pure single crystal of silicon has electron charge mobility slightly above 1000 $cm^2/V{\cdot}s$. To build fast chipsets, a different kind of materials that exhibit higher electron charge mobility than silicon's but is still compatible with silicon based fab technology is clearly required. In this regard, previously, many efforts had been carried out to develop single crystal SiGe which is compatible with the current silicon based fab lines and offers higher mobility, but without success [1]. We developed a rhombohedrally aligned silicon-germanium (SiGe) on *c*-plane sapphire substrate. This lattice-matched SiGe widely opens a possibility of chipset speed improvement without the costly efforts to reduce feature size. A lattice-matched SiGe has its own oxide as an insulator, SiO_2, unlike the arsenide, antimonide, or other compound semiconductors. Such an oxide with a proper insulator existing, SiGe, allows mass fabrication of several hundreds of chips on wafer basis.

The attainable speed of silicon-germanium chipsets is based on the gate length and the charge mobility which is related to a defect pattern such as twin population and crystal structure. Lattice-matched SiGe has very high mobility for a possibility of chipset speed improvement. The film surface morphology, number of twins, and dislocations will directly affect the wafer surface topography which sets the limits on yielding rate through device fabrication process. The surface roughness of wafers affects submicron photolithography, wafer bonding [2], edge loss [3, 4], and overall yielding rate. For CPU and memory, the generally known required root

mean square (rms) surface roughness is 0.5 nm~1 nm. The most tolerant case of surface roughness is for the solar cell fabrication requirement which varies from 1 nm to 100 nm. The defect densities on wafer are the key issue for sustaining high yield of nanofab devices [5]. To keep manufacturing costs low, the amount of epitaxy should be kept minimum both for lower consumption or source materials and for increased throughput.

SiGe on sapphire is one of the most important approaches to build silicon-germanium on insulator (SGOI) devices such as a high mobility transistor for K-band and higher frequency applications up to 116 GHz [6–8]. Because sapphire is one of the best insulators, the high frequency parasitic capacitance between the semiconductor layer and the substrate can be alleviated for better performance at high frequency. Many epitaxial growths in this regard utilize silicon on sapphire (SOS) and silicon-germanium on sapphire (SGOS, SGOI) technologies to take advantage of the rectangular r-plane of sapphire aligned with the square-faced (001) plane or rectangle-faced (110) plane of the Si and Ge diamond structure. However, it was reported that this approach often shows 90° rotated twin defects [9]. On the other hand, growth of SiGe layers on the trigonal (0001) plane, that is, c-plane of sapphire, has not been utilized for device fabrication so far due to the formation of 60° rotated twin defects.

In this paper, we present a possibility that rhombohedrally oriented single crystal SiGe could be a candidate material of next generation chipset by showing that electron mobilities of SiGe grown on c-plane sapphire substrate are higher than those of Si. And we investigated the effect of twin density on room temperature (RT) electron mobilities in SiGe grown on c-plane sapphire substrate. Also, our report includes the results of crystalline defects with chemical etching of SiGe film in order to determine the failure analysis required to produce useful SiGe layer for device.

2. Experimental

2.1. Film Growth. The epitaxial layer growth of SiGe was carried out in a magnetron sputtering system. The 2-inch sapphire substrate was cleaned with acetone, isopropanol, and deionized water before being placed onto the wafer holder within vacuum chamber. The back sides of the sapphire substrates were coated with carbon for effective heating of sapphire substrate to a desired level of epigrowth temperature. The sapphire wafer is transparent to infrared (IR) and visible light, and most of the heating due to IR light passes directly through the sapphire wafer without heating it up. Therefore, the actual temperature of the sapphire wafer surface was much lower than the temperature measured by the thermocouple of the substrate heater. In order to solve this problem, backside carbon coated sapphire wafers were prepared before the actual SiGe growth. The substrates were then baked under infrared heat at 200°C for 1 hour. The chamber temperature was then increased to 1000°C for a short time to remove any volatile contaminants. 95% single crystal SiGe film was grown at 890°C growth temperature, a 5-sccm of high-purity argon gas, and 5 mTorr chamber pressure. The rhombohedral alignment of cubic SiGe depends on the growth conditions, especially the growth temperature and the surface termination of the c-plane sapphire wafer. The number of twins was controlled by film deposition temperature during the SiGe deposition and sapphire wafer treatment before the SiGe deposition.

2.2. Film Characterization. The epilayer grown on sapphire substrate was characterized by several XRD methods developed by NASA Langley. The vertical atomic alignment was measured with a symmetric 2θ-Ω scan, which probes the surface normal direction. The prominent SiGe (111) peak at $2\theta \sim 27.5^\circ$, which appears next to the sapphire (0006) and (00012) peaks, shows [111] oriented SiGe. The horizontal atomic alignment is measured with phi (ϕ) scan of the SiGe (220) peaks. Three strong peaks in the ϕ scan indicate the majority single crystalline SiGe and three small peaks indicate the 60° rotated SiGe twin crystal.

Phi (ϕ) Scan Method [10]. When the sample is tilted by angle χ, the sample normal n is tilted by angle χ with respect to the z-axis of the XRD goniometer. This situation is indicated in Figure 1. For example, when we grow SiGe (111) on c-plane sapphire (0001), the growth direction is aligned to [111] = n, while the asymmetric SiGe (220) planes are contained on the green plane with the angle $\chi = \beta = 35.264^\circ$, which is the interplanar angle between (111) and (220) planes of SiGe. If we consider all of the {220} planes of the single crystal SiGe, there will be a total of 12 planes. However, 6 of these are located at the backside of the substrate, while the three planes, (02-2), (20-2), and (2-20), are oriented 90° with respect to the sample normal [111] and hence do not diffract X-rays. Only the three planes, (022), (202), and (220), strongly diffract. When SiGe layer contains twin defects comprised of both bulk domain and microtwin defects, the defects align as the 60° rotated twin crystal along [111]-axis. Therefore, the {220} reflections of twin crystal will be 60° off in the ϕ plane from the original crystal's {220} reflections. The twin crystal's {220} reflections are now shown as blue dots in Figure 1. Therefore, the ϕ scan with the angle $\chi = \beta = 35.264^\circ$ shows the {220} peaks from both the original crystal and the 60° rotated twin crystal.

The y-axis is plotted in a log-scale and the twin crystal's peak is very weak compared with the majority single crystal's peak. And the untilted symmetric phi scan of SiGe {440} reflections shows three strong single crystal peaks and three weak twin defect peaks. By setting the sample's azimuthal ϕ angle to the desired peak (one of the strong single crystal peaks or one of the weak twin defect peaks) and translating the wafer in the X and Y directions, we obtain the X-Y mapping image of the SiGe film on c-plane sapphire wafer. The majority single crystal map shows a uniformly strong signal over the entire wafer surface with a small concentrated region of twin defects at the edge. The twin defects on edge were developed due to both the shadow by the wafer holder and the temperature gradient at the edge.

Atomic force microscope (AFM) measurements show the surface topographic variation and root mean square (rms) roughness of the SiGe layer. The crystal structure and layer thickness of the SiGe thin film were characterized using TEM

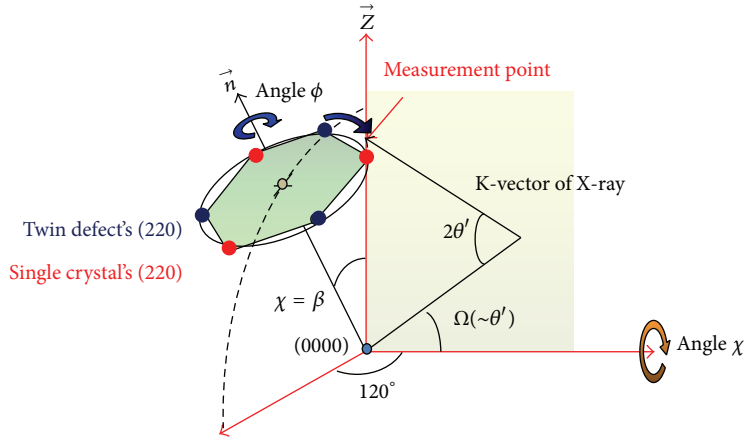

FIGURE 1: Phi (ϕ) scan with tilted χ for twin crystal detection.

TABLE 1: Etchant composition for etch-pit density tests and its effects.

Etch	Composition (Mol %)			Results on {100}	
	Solvent*	HF	Oxidizer**	Line defects	"Point" defects
Secco	67.6	32.2	0.17	Pits	Shallow pits or hillocks
Sirtl	71.2	26.3	2.5	Pits or mounds	—
Wright	78.5	16.1	5.4	Pits	Shallow pits
Seiter	78.5	5.9	15.6	Mounds	Mounds

*H_2O + CH_3COOH (HAc); **CrO_3 + HNO_3.

(FEI, Tecnai G2 F30, 300 KV). The room temperature electron mobilities and carrier densities of the SiGe films were measured using the Hall effect measurement system. To obtain reproducible results, the films were cut into several pieces of a standard sized square. Each corner of the square-cut SiGe film with specific doping concentration was soldered onto the four arms of the sample test platform to ensure ohmic contacts. The ohmic contacts can be also checked during the measurement process of Hall mobility.

To reveal the crystalline defects on fab silicon wafer, some chemical etching methods such as Wright [11], SECCO [12], Sirtl [13], and Dash [14] etches have been widely used in failure analysis of semiconductor. SECCO etch is a very useful chemical etching method for the characterization of defects on surface of bare silicon wafer [15].

SECCO etch uses an etchant composition of solvent, hydrofluoric acid (HF), and $K_2Cr_2O_7$ oxidizer as tabulated in Table 1. SECCO etch compositions are as follows [12]: hydrofluoric acid (HF), 67% by volume, and 0.15 M $K_2Cr_2O_7$ in H_2O, 33% by volume. When mixing the solution, 14.52 g of $K_2Cr_2O_7$ should be dissolved in 330 mL of H_2O. Then, the $K_2Cr_2O_7$ solution is poured into 670 mL of HF. After mixing, the total volume of the solution is kept in plastic chemical bottle. The defect area is under higher stress; hence, it will etch more quickly in SECCO etchant than the bulk semiconductor. In most of the cases, the result appears as an elliptical pit on substrate at the location of the defect. Optical microscopy is performed to inspect the crystalline defects pitted by SEC-CO etch.

3. Results and Discussion

Figure 2 shows the quality of crystalline SiGe film on *c*-plane sapphire through TEM and XRD. XRD normal scan data shows very strong SiGe (111) peak (Figure 2(a)). In order to check the distribution of SiGe crystal in azimuthal in-plane angles, we used the phi scan method for SiGe {220} peaks and sapphire {10–14} peaks. The phi scan of SiGe {220} peaks shows a large difference in alignment and ratio of majority single crystal. The majority peaks and minority primary-twin peaks that are rotated by 60° are noted as (i) and (ii) in Figure 2(b), respectively. The area ratio of the peaks is 95 : 5. In the mapping, a point X-ray source with a 5 nm beam mask was used: (c) shows that almost complete single crystalline SiGe layer was fabricated on the basal plane of trigonal sapphire. Three {10–14} peaks show the trigonal space symmetry of a sapphire crystal (Figure 2(d)). From the SAED pattern in the upper inset of Figure 2(e), the epitaxial relationship between majority SiGe film and sapphire substrate was found to be $(111)_{SiGe}//(0001)_{sapphire}$ and $[-112]_{SiGe}//[01\text{-}10]_{sapphire}$. These results demonstrate that the [111]-oriented rhombohedral heterostructure epitaxy of a cubic single crystalline SiGe layer on trigonal *c*-plane sapphire has been achieved. The SiGe layer was grown in layer-by-layer mode with few micrometers of thicknesses and a smooth interface (Figure 2(f)).

The charge mobility in semiconductor materials is determined and limited by several factors, such as alloy composition, interface roughness, interface charge scattering, lattice

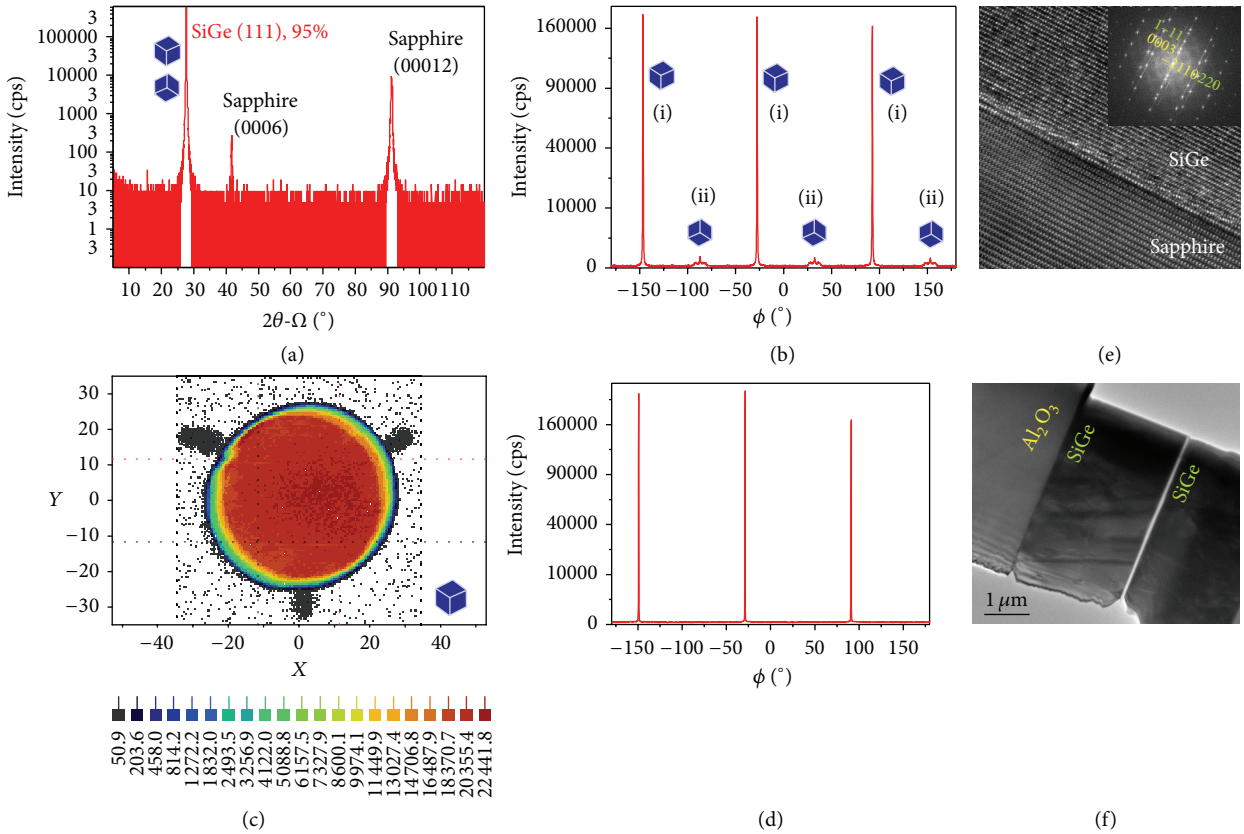

FIGURE 2: Analysis of the 95% single crystal SiGe film. Plot (a) shows θ-2θ scan in the direction normal to the surface, graph (b) shows phi scan of SiGe peaks for the relative atomic alignment, (c) X-Y wafer mapping with majority {440} peak shows the distribution of a single crystal, (d) shows phi scan of sapphire {10–14} peaks for relative atomic alignment, (e) shows HRTEM and its SAED result of the SiGe (green)/sapphire (yellow) interface, and (f) shows low magnification TEM image after the ion milling process.

mismatch or segregation, and strain relaxation of strained SiGe layers with large Ge content and layer width, as discussed in a recent review by Whall and Parker (2000) [18]. The results by Hall effect measurements indicate that the density of twin lattices is correlated with the electron mobility in the SiGe films. Figure 3(a) shows the calculated electron mobility for relaxed SiGe alloys as a function of their Ge content. As shown in Figure 3(a), relaxed SiGe alloys exhibit drastic decline in mobility mainly due to alloy interface scattering in dislocation populated polycrystal region, except for varying high Ge content (>0.85), where they start behaving like Ge [16, 17]. In Figure 3(a), the left side y-axis indicates the pure Si with $\mu_{n,\mathrm{Si}} = 1{,}400\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ and the right side y-axis the pure Ge with $\mu_{n,\mathrm{Ge}} = 4{,}000\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ [19, 20]. When epitaxial layer is grown on Si or Ge substrate, in either case alloy composition from pure Si or pure Ge lowers the electron carrier mobility rapidly and they often become polycrystal with many defects in the middle SiGe composition. In spite of the high mobility of Ge, the mobility of SiGe layer is substantially lowered due to the formation of strain caused dislocation defects. The strain caused dislocation defects occur mainly due to the lattice mismatch between Si whose lattice constant is 5.431 Å and Ge with 6.657 Å [21]. However, if a substrate allows growing a lattice-matched SiGe layer on it, these defect formation problems can be avoided and the mobility can be drastically enhanced beyond that of Si. Of course, not only is the growth of lattice-matched SiGe layer guaranteed by the crystal symmetry of substrate, but also the growth conditions, such as epilayer speed, substrate temperature, and pressure of processing gases, will dictate the formation of lattice-matched crystalline structures. We observed that the electron mobility is also strongly correlated with the dopant electron density. In Figure 3(b), we figured out the dependence of room temperature electron mobilities on defect density and dopant density in SiGe films. The measured dopant electron densities in three SiGe films are $2.21 \times 10^{17}/\mathrm{cm}^3$, $6.02 \times 10^{17}/\mathrm{cm}^3$, and $1.46 \times 10^{18}/\mathrm{cm}^3$. On the other hand, the defect density measurements were made by the XRD phi scan. The electron mobilities of the tested samples are between those of single crystal Si ($\mu_{n,\mathrm{Si}} = 1{,}400\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$) and Ge ($\mu_{n,\mathrm{Ge}} = 4{,}000\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$). The measured electron mobility of a 95% single crystal SiGe was $1538\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ which is between $350\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ (Si) and $1550\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ (Ge) at $6.02 \times 10^{17}/\mathrm{cm}^3$ dopant concentration. And the electron mobility of 99.5% single crystal SiGe is $1552\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ at the $6.02 \times 10^{17}/\mathrm{cm}^3$ dopant concentration. Figure 3(a) shows that the room

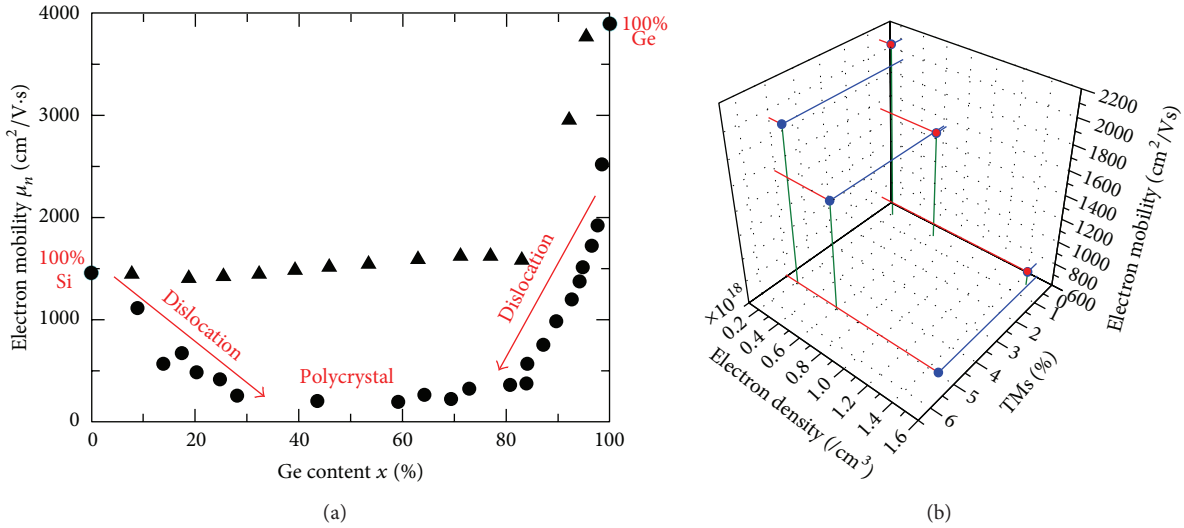

FIGURE 3: (a) Calculated phonon-limited 300 K electron low-field mobility in relaxed $Si_{1-x}Ge_x$ alloys. Results with (circle) and without (triangle) the inclusion of alloy scattering are shown [16, 17]. (b) Three pairs in three-dimensional (3D) plot for room temperature electron mobilities in SiGe films as a function of twin density (TM) and dopant concentration. Red and blue dots show the data points for 99.5% and 95% single crystal SiGe samples grown on c-plane sapphire substrates, respectively.

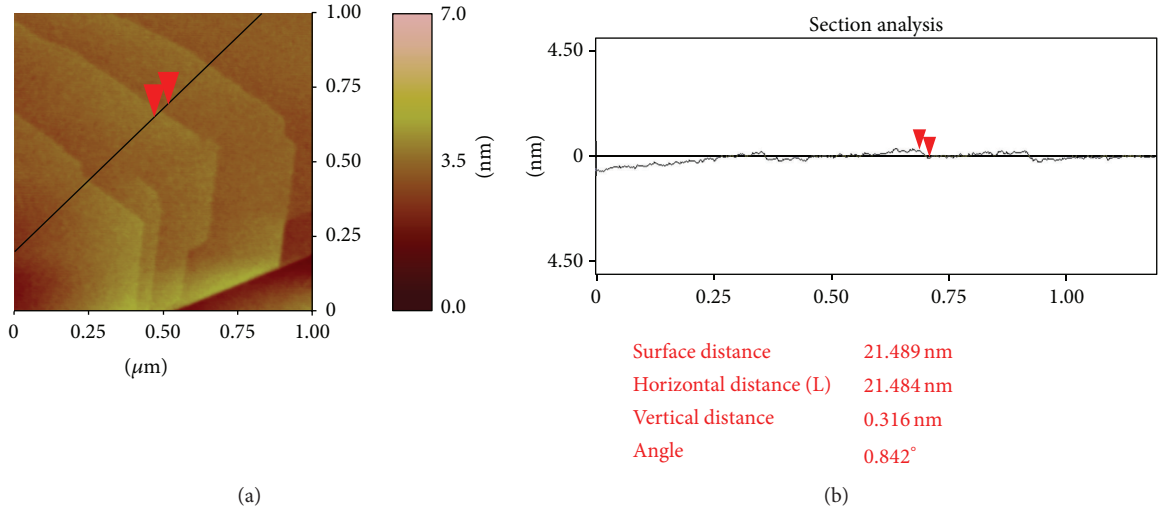

FIGURE 4: AFM image of SiGe layer on c-plane sapphire: (a) 1 μm × 1 μm area of a SiGe and (b) line profile of cross-section measured along the dark line in (a).

temperature electron mobility in the SiGe films grown on sapphire substrates becomes slightly higher as defect densities are decreased.

Since the topographical and morphological properties of the layer directly influence the charge carrier properties and the channel carrier transport characteristic of the device, the layer needs to be flat in atomic level. The SiGe layer shows a root mean square (rms) roughness of 2 nm for 1×1 μm^2 scan. The AFM analysis shows that the epitaxial layer grows in a layer-by-layer growth mode [22, 23], as shown in Figure 4(a). Figure 4(b) shows a line scan profile along the line indicated, which was selected to pass through a step. It is important to control the SiGe composition to reduce the lattice mismatch with the c-plane sapphire, maintain an appropriate molecular beam flux rate to ensure flat smooth layer-by-layer growth, and have 2D layer-by-layer growth in electronic microdevice fabrication.

Fine and delicate growth control of SiGe epitaxy to alleviate crystalline defects is a serious matter that directly affects yield in device fabrication. In particular, the collective effect of threading dislocations (TDs) attributed to performance degradation has been observed when other types of crystal defects exist individually [24]. In MOSFET, interface misfit dislocations (MDs) which extend between the source and

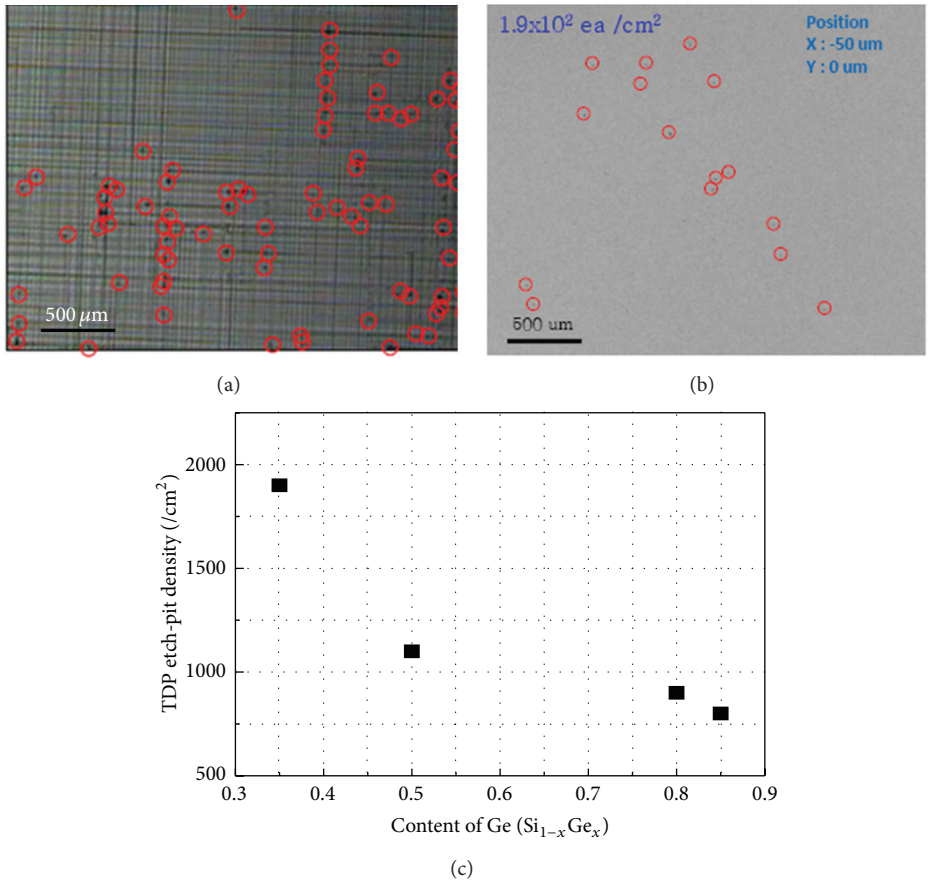

FIGURE 5: Etch-pit test results of (a) typical SiGe on Si(100) wafer with Ge content = 35% and of (b) rhombohedral SiGe on *c*-plane sapphire with Ge content = 35% (c) threading dislocation etch-pit density of $Si_{1-x}Ge_x$ on sapphire substrate based on the Ge content.

the drain may become electrically active, resulting in increased off-state leakage [25]. The electrical impact of stacking faults (SFs) on device operation can be seen as a combination of the individual effects of misfit and TDs. A single SF in the strained Si channel can degrade the device operation at both off- and on-state conditions [26]. SECCO etch is a chemical etching method used to delineath crystalline defects on silicon substrate and SiGe film. When SECCO etch is used directly, crystalline defects are revealed on silicon substrate or SiGe film after 2 minutes at some areas. Industry standard SECCO etch-pit density measurements were performed on a conventional SiGe layer on Si and 95% single crystalline SiGe layers with 35% Ge content on *c*-plane sapphire. A typical SiGe layer with 35% Ge content on a Si(100) wafer shows a high density of dislocation line and etch pits (see Figure 5(a)). On the other hand, the rhombohedral SiGe grown on *c*-plane sapphire with 35% Ge composition ratio shows two orders of magnitude less etch pits and no dislocation lines after performing the SECCO etching (see Figure 5). The conventional SiGe on a Si(100) wafer reveals a threading dislocation pit (TDP) density of $3.9 \times 10^4/cm^2$, line defect density of $1.73 \times 10^4/cm^2$, and a lot of cross-hatch patterns as shown in Figure 5(a). The rhombohedral SiGe grown on *c*-plane sapphire has only a TD etch-pit density of $1.9 \times 10^2/cm^2$, no visible line defects, and no cross-hatch patterns as shown in Figure 5(b). Therefore, the rhombohedral SiGe shows a 200 times less defect density than conventional SiGe on Si(100) wafer under the SECCO etching tests. Conclusively, we confirmed that a new SiGe film growth technique of fully relaxed SiGe alloy layers yields low TD density epitaxially grown on sapphire substrate [27]. The TD etch-pit density of SiGe on sapphire decreases to $800/cm^2$ as Ge content increases (see Figure 5(c)). The SiGe films with low TDP density, high electron mobility based on the high Ge content like 85%, and smooth surface were grown on *c*-plane sapphire substrate. These kinds of films are sufficiently qualified for the fabrication of the ultrafast chipsets like bipolar junction transistors.

The SGOI structures are currently fabricated mainly by two methods, layer transfer [28] and Ge condensation [29, 30]. In the layer transfer method, hydrogen implantation is employed in order to separate a thin SiGe layer from graded SiGe substrates. In the Ge condensation method, a SiGe layer with a low Ge concentration grown on a silicon-on-insulator (SOI) substrate is thermally oxidized, where Ge atoms in the SiGe layer are ejected from the oxide interface resulting in a SiGe layer with a high Ge concentration. However, these methods require complex processing routines and do not always

Table 2: Comparison of Si, SOI, and SiGe on Si and LM-SGOI technologies.

Technology	Si	SOI/SGOI	SiGe on Si	SiGe on sapphire (NASA LaRC)
Fabrication	Single crystal ingot	Hydrogen crack	Gradient layer, super lattice	**Lattice-matched growth**
Growth method	Czochralski	Wafer bonding	Epitaxial growth	**Epitaxial growth**
Lattice-matched Ge content	0%	0%	0%	**85% with sapphire substrate**
Ge content in strained layer before defects	0%	Usually 0~8%	Usually 0~8%	**85% achieved**
Ge content in relaxed layer	0% (not available)	Up to 25% with severe defects	Up to 25% with severe defects	**85% achieved with 0.2% defects**
Parasitic capacitance reduction	No	Yes	No	**Yes**
Device	Bipolar junction transistor (BJT), CMOS	BJT, CMOS/heterojunction bipolar transistor (HBT), CMOS	HBT	**HBT, CMOS**
Improvement	Conventional technology	High speed with insulating substrate	High speed (ultrathin SiGe lower collector voltage of HBT)	**High speed with thick and thin SiGe layer with insulating substrate, higher device yield with lower defects**

produce high-quality fully relaxed SiGe layer [31]. A different approach reported is an amorphous SiGe layer deposited on SOI substrate and then annealed above the melting point of SiGe after the formation of the SiO_2 capping layer [32]. This process has the advantage of simplicity. However, it is difficult to obtain the SiGe layer with high Ge concentration by this process, because the annealing temperature must be reduced below the melting point, resulting in the unusually long annealing time. Rapid thermal annealing (RTA) was also proposed in order to obtain the homogeneous SiGe layer [16]. However, high-quality and uniform SiGe layers were not obtained in the previous study.

We demonstrated the fabrication of high-quality SiGe layers on sapphire substrate by sputtering. The ideal of this process is that a fundamental governing relationship exists in rhombohedral epitaxy process, that is, the growth of ⟨111⟩-oriented cubic crystals on the basal *c*-plane of trigonal sapphire crystals [33–35]. One of the concerns with this epitaxy relationship is that two crystal structures tend to be formed which exhibit a twin lattice structure. This atomic alignment allows polytype crystalline structures with stacking faults on the (111) plane. Rhombohedral alignment, that is, aligning the [111] direction of a cubic structure to the [0001] direction of a trigonal structure, can have two possible azimuthal configurations. Two crystals are twin to each other and they can be formed by a stacking fault during the crystal growth process. We gained an experience to control the amount of the twins based on the growth conditions, especially the growth temperature and deposition power. Our process enables the forming of the SiGe layer of high Ge concentration (85%). For semiconductor device applications, high carrier mobility SiGe layers can be made by reducing stacking faults and microtwin defects. The measurement and control of stacking faults and twin crystals are, therefore, important in the microelectronics applications.

Table 2 illustrates the key features of lattice-matched SiGe on insulator (LM-SGOI) currently under development at NASA Langley [36–42] compared to existing products or technologies. The far right column of Table 2 shows the NASA Langley developed SiGe material that is compatible with the conventional insulator silicon oxide. The new rhombohedral epitaxy allows new lattice matching condition of SiGe on sapphire insulator with 85% Ge content and 0.5% defects. While the carrier mobilities of silicon-on-insulator (SOI) are limited by the silicon material, the mobilities of SiGe on *c*-plane sapphire can be a few times higher than those of silicon due to the high carrier mobilities of germanium. The silicon-on-sapphire (SOS) became crucial in devices using SOI wafers because sapphire is one of the best insulators. The SOS wafer provides electrically separated regions because of the insulating properties of the sapphire itself, as opposed to other typical devices where the regions are electrically separated using reverse bias between the substrate and device area. The space charge region (carrier depletion region) in the reverse bias case is very thin, in the micrometer range, and the capacitance between a device and the substrate is high and causes the device to have a leakage current at high frequency operating speeds. On the contrary, sapphire is very thick and has an ultrasmall capacitance, thereby reducing parasitic capacitance and leakage currents at high operating frequencies. The lattice-matched SiGe is also complemented by silicon oxide as an insulator and stable gate oxide with SiO_2 can make short gate length for RF device. Therefore, RF devices like heterojunction bipolar transistor (HBT) that

are made with rhombohedral SiGe on *c*-plane sapphire can potentially run a few times faster than RF devices on SOS wafers at high frequencies up to several hundred GHz.

4. Summary and Conclusions

In summary, we have experimentally demonstrated the fabrication of high-quality SiGe layers with a high Ge concentration of more than 85% on sapphire wafer by sputtering. We also report that the defect dependence of the electron mobility by the twinning of SiGe thin films on sapphire (0001) substrates was measured. Currently, a standard SiGe technology uses only ultrathin (30~100 nm) layer of SiGe for base layer of heterojunction bipolar transistor (HBT) to avoid dislocation defects. With the lattice-matched SiGe layer we developed, a thin or thick SiGe layer can be also fabricated for any designated applications, since the lattice-matched materials do not have a critical thickness limit. In rhombohedral SiGe on *c*-plane (0001) sapphire, the SiGe layer can be also grown in layer-by-layer mode from sub-100 nm to few micrometers of thicknesses. Therefore, thin rhombohedral SiGe on *c*-plane sapphire has many commercial application potentials as do SOI wafers in addition to solar cell applications. Typically, a rhombohedral single crystal SiGe has 2 or 3 times higher carrier mobility than monocrystalline silicon. The high Ge-content SiGe film shows high mobility, low cost, and simple structure when grown directly on sapphire substrate with sputtering process. If the defects in SiGe can be removed, transistors with higher operational frequencies can be fabricated for a new generation of ultrafast chipsets because of the high mobility of SiGe film.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References

[1] D. L. Harame and B. S. Meyerson, "The early history of IBM's SiGe mixed signal technology," *IEEE Transactions on Electron Devices*, vol. 48, no. 11, pp. 2555–2567, 2001.

[2] C. Gui, M. Elwenspoek, N. Tas, and J. G. E. Gardeniers, "The effect of surface roughness on direct wafer bonding," *Journal of Applied Physics*, vol. 85, no. 10, pp. 7448–7454, 1999.

[3] "Semiconductor Wafer edge analysis," Chapman Technical Note TW-1, 1998.

[4] H. Ahmataku and K. Kipli, in *Proceedings of the IEEE International Conference on Semiconductor Electronics (ICSE '10)*, Melaka, Malaysia, June 2010.

[5] I. McMackin, W. Martin, J. Perez et al., "Patterned wafer defect density analysis of step and flash imprint lithography," *Journal of Vacuum Science & Technology B*, vol. 26, no. 1, pp. 151–155, 2008.

[6] S. A. Alterovitz, C. H. Mueller, and E. T. Croke, "High mobility SiGe/Si transistor structures on sapphire substrates using ion implantation," *Journal of Vacuum Science & Technology B*, vol. 22, p. 1776, 2004.

[7] K. Ismail, M. Arafa, K. L. Saenger, J. O. Chu, and B. S. Meyerson, "Extremely high electron mobility in Si/SiGe modulation-doped heterostructures," *Applied Physics Letters*, vol. 66, no. 9, pp. 1077–1079, 1995.

[8] S. J. Koester, R. Hammond, J. O. Chu et al., "SiGe pMODFETs on silicon-on-sapphire substrates with 116 GHz fmax," *IEEE Electron Device Letters*, vol. 22, no. 2, pp. 92–94, 2001.

[9] W. B. Dubbelday and K. L. Kavanagh, "Growth of SiGe on sapphire using rapid thermal chemical vapor deposition," *Journal of Crystal Growth*, vol. 222, no. 1-2, pp. 20–28, 2001.

[10] Y. Park, H. J. Kim, G. C. King, and S. H. Choi, "X-ray diffraction wafer mapping method for SiGe twin defects characterization," in *Nanosensors, Biosensors, and Info-Tech Sensors and Systems*, vol. 7980 of *Proceedings of SPIE*, April 2011.

[11] M. W. Jenkins, "A new preferential etch for defects in silicon crystals," *Journal of the Electrochemical Society: Solid-State Science and Technology*, vol. 124, no. 5, pp. 757–762, 1977.

[12] F. Secco d'Aragona, "Dislocation etch for (100) planes in silicon," *Journal of The Electrochemical Society*, vol. 119, no. 7, pp. 948–951, 1972.

[13] E. Sirtl and A. Adler, "Chromic acid-hydrofluoric acid as specific reagents for the development of etching pits in silicon," *Zeitschrift für Metallkunde*, vol. 52, pp. 529–534, 1961.

[14] W. C. Dash, "Copper precipitation on dislocations in silicon," *Journal of Applied Physics*, vol. 27, no. 10, pp. 1193–1195, 1956.

[15] H. Rauh, *Wacker's Atlas for Characterization of Defects in Silicon*, A Part of the Wacker Tutorial Series, 1986.

[16] M. Glicksman, "Mobility of Electrons in Germanium-Silicon Alloys," *Physical Review*, vol. 111, no. 1, pp. 125–128, 1958.

[17] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *Journal of Applied Physics*, vol. 80, no. 4, pp. 2234–2252, 1996.

[18] T. E. Whall and E. H. C. Parker, "Si/SiGe/Si pMOS performance—alloy scattering and other considerations," *Thin Solid Films*, vol. 368, pp. 297–305, 2000.

[19] C. Jacoboni, C. Canali, G. Ottaviani, and A. Alberigi Quaranta, "A review of some charge transport properties of silicon," *Solid State Electronics*, vol. 20, no. 2, pp. 77–89, 1977.

[20] V. I. Fistul, M. I. Iglitsyn, and E. M. Omelyanovskii, "Mobility of electrons in germanium strongly doped with arsenic," *Soviet Physics, Solid State*, vol. 4, no. 4, pp. 784–785, 1962.

[21] *Landolt-Börnstein, New Series Group III*, vol. 17a, Springer, Berlin, Germany, 1982.

[22] F. C. Frank and J. H. van de Merwe, "One-dimensional dislocations. I. Static theory," *Proceedings of the Royal Society of London: Series A*, vol. 198, no. 1053, pp. 205–216, 1949.

[23] F. C. Frank and J. H. van de Merwe, "One-dimensional dislocations. IV. Dynamics," *Proceedings of the Royal Society of London A*, vol. 201, no. 1065, pp. 261–268, 1950.

[24] E. Escobedo-Cousin, S. H. Olsen, A. G. O'Neill, and H. Coulson, "Defect identification in strained Si/SiGe heterolayers for device applications," *Journal of Physics D: Applied Physics*, vol. 42, no. 17, Article ID 175306, 2009.

[25] J. G. Fiorenza, G. Braithwaite, C. W. Leitz et al., "Film thickness constraints for manufacturable strained silicon CMOS," *Semiconductor Science and Technology*, vol. 19, no. 1, article L4, 2004.

[26] J. N. Yang, G. W. Neudeck, and J. P. Denton, "Electrical effects of a single stacking fault on fully depleted thin-film silicon-on-insulator P-channel metal-oxide-semiconductor field-effect

transistors," *Journal of Applied Physics*, vol. 91, no. 1, pp. 420–426, 2002.

[27] P. I. Gaiduk, A. Nylandsted Larsen, and J. Lundsgaard Hansen, "Strain-relaxed SiGe/Si heteroepitaxial structures of low threading-dislocation density," *Thin Solid Films*, vol. 367, no. 1-2, pp. 120–125, 2000.

[28] L. J. Huang, J. O. Chu, D. F. Canaperi et al., "SiGe-on-insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors," *Applied Physics Letters*, vol. 78, no. 9, pp. 1267–1269, 2001.

[29] T. Tezuka, N. Sugiyama, T. Mizuno, M. Suzuki, and S. Takagi, "A novel fabrication technique of ultrathin and relaxed SiGe buffer layers with high Ge fraction for Sub-100 nm strained silicon-on-insulator MOSFETs," *Japanese Journal of Applied Physics*, vol. 40, part 1, no. 4B, pp. 2866–2874, 2001.

[30] S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S.-I. Takagi, "Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique," *Applied Physics Letters*, vol. 83, no. 17, pp. 3516–3518, 2003.

[31] T. Shimura, K. Kawamura, M. Asakawa et al., "Characterization of strained Si wafers by X-ray diffraction techniques," *Journal of Materials Science: Materials in Electronics*, vol. 19, no. 1, supplement, pp. S189–S193, 2008.

[32] N. Sugii, S. Yamaguchi, and K. Washio, "SiGe-on-insulator substrate fabricated by melt solidification for a strained-silicon complementary metal–oxide–semiconductor," *Journal of Vacuum Science & Technology B*, vol. 20, no. 5, pp. 1891–1896, 2002.

[33] H.-J. Kim, H.-B. Bae, Y. Park, K. Lee, and S. H. Choi, "Temperature dependence of crystalline SiGe growth on sapphire (0001) substrates by sputtering," *Journal of Crystal Growth*, vol. 353, no. 1, pp. 124–128, 2012.

[34] Y. Park, G. C. King, and S. H. Choi, "Rhombohedral epitaxy of cubic SiGe on trigonal c-plane sapphire," *Journal of Crystal Growth*, vol. 310, no. 11, pp. 2724–2731, 2008.

[35] H. J. Kim, H. B. Bae, Y. Park, and S. H. Choi, "Defect-engineered $Si_{1-x}Ge_x$ alloy under electron beam irradiation for thermoelectrics," *RSC Advances*, vol. 2, no. 33, pp. 12670–12674, 2012.

[36] Y. Park, S. H. Choi, and G. C. King, "Silicon germanium semiconductive alloy and method of fabricating same," US Patent no. 7,341,883, 2008.

[37] Y. Park, S. H. Choi, G. C. King, J. R. Elliott Jr., and D. M. Stoakley, "Graded index silicon geranium on lattice matched silicon geranium semiconductor alloy," US Patent No. 7514726 B2, 2009.

[38] Y. Park, S. Hyouk Choi, G. C. King, and J. R. Elliott, "Method of generating X-ray diffraction data for integral detection of twin defects in super-hetero-epitaxial materials," US Patent no. 7,558,371 B2, 2009.

[39] Y. Park, S. H. Choi, and G. C. King, "Epitaxial growth of cubic crystalline semiconductor alloys on basal plane of trigonal or hexagonal crystal," US Patent no. 7,906,358 B2, 2011.

[40] T. Maniwa, "Steering apparatus," US Patent No. 8,826,767, 2012.

[41] Y. Park, S. H. Choi, G. C. King, and J. R. Elliott, "Rhombohedral cubic semiconductor materials on trigonal substrate with single crystal properties and devices based on such materials," US Patent no. 8,257,491 B2, 2012.

[42] Y. Park, S. H. Choi, G. C. King, J. R. Elliott, and A. L. Dimarcantonio, "X-ray diffraction wafer mapping method for rhombohedral super-hetero-epitaxy," US Patent No. 7769135 B2, 2010.

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Research Article

The Investigation of Field Plate Design in 500 V High Voltage NLDMOS

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This paper presents a 500 V high voltage NLDMOS with breakdown voltage (V_{BD}) improved by field plate technology. Effect of metal field plate (MFP) and polysilicon field plate (PFP) on breakdown voltage improvement of high voltage NLDMOS is studied. The coeffect of MFP and PFP on drain side has also been investigated. A 500 V NLDMOS is demonstrated with a 37 μm drift length and optimized MFP and PFP design. Finally the breakdown voltage 590 V and excellent on-resistance performance (R_{sp} = 7.88 ohm $*$ mm^2) are achieved.

1. Introduction

For the high voltage NLDMOS in BCD (Bipolar, CMOS, and DMOS) platform implicated in 500 V and even higher voltage, RESURF (reduced surface field) technology has been widely adopted [1, 2]. The major purpose of this method is to increase the breakdown voltage (V_{BD}) and improve the on resistance (R_{sp}) of NLDMOS through the reduction of the surface electric field of drift region. It not only helps to reduce the NLDMOS device size and R_{sp}, but also can meet breakdown requirement. For NLDMOS, one well-known technical approach is to introduce a p-type doped layer into n-type doped drift region and then realize the double RESURF or triple RESURF effect [3, 4]. This approach also has been extensively studied by many researchers [5, 6].

MFP or gate shield (Gshield) is a common method employed in RFLDMOS. One or two (even three) metal field plates cover on gate and part of adjacent drift region [7]. The function of this Gshield is to shield the impact from drain and reduce the miller capacitance, which is the feedback capacitance between gate and drain (C_{ds}). It improves the frequency characteristics of RFLDMOS and extends the application to higher frequency [8]. This metal field plate will change the electric field distribution of drift region and affect the breakdown voltage of the device.

In the published research results for 500 V and higher voltage NLDMOS, some researches refer to the devices structure with field plate [9–11]. However, in-depth study of metal and polysilicon field plate on such high voltage NLDMOS is still needed for further investigation. This paper presents a detailed study of MFP and PFP and their effect on 500 V high voltage NLDMOS. A 500 V NLDMOS optimized by MFP and PFP design has been demonstrated with smaller drift size and higher enough breakdown voltage. This research result also can be adopted as a good reference for other high voltage NLDMOS developments.

2. Device Structure

The schematic cross section of 500 V NLDMOS device is showed in Figure 1. When drain terminal is biased at operation voltage (V_{dd}), the voltage sustained in lateral direction and vertical direction is the same. The breakdown voltage of both directions needs to be higher than the operation voltage and at least has 10% margin. Figure 1 shows that the drift region of NLDMOS embraces deep n-type well (DNW) and p-type buried layer (PBL). The voltage drop of V_{dd} in the vertical direction mostly is allocated to the PN diode formed by DNW and p-type substrate (PSUB). Its breakdown

Table 1: Key reference sizes of this NLDMOS.

Item	Description	Size
PFP1	Polysilicon field plate, source side	7
PFP2	Polysilicon field plate, drain side	10
MFP1	Metal field plate, source side	22
MFP2	Metal field plate, middle	3
MFP3	Metal field plate, drain side	25
$E1$	MFP3 extending PFP2 (left side)	8

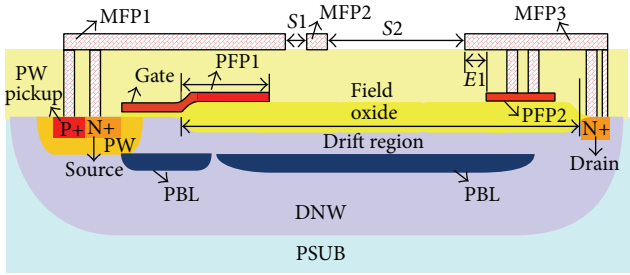

Figure 1: Schematic cross section of high voltage NLDMOS.

is higher than 1000 V and can be used in the application of 500 V NLDMOS. The drift region with DNW and PBL is designed considering RESURF effect. Drift region is fully depleted and sustains the lateral voltage when drain is biased. The doping condition of the drift region is determinate due to the technology platform and will not be discussed here. P-type well (PW) and p-type heavily doped region (P+) form the channel region. N-type heavily doped region (N+) forms the source and drain. Above the silicon, there are polygate, polysilicon field plate 1 (PFP1, close to source side), polysilicon field plate 2 (PFP2, close to drain side), metal field plate 1 (MFP1, source side), metal field plate 2 (MFP2, middle), and metal field plate 3 (MFP3, drain side). $S1$ is the space between MFP1 and MFP2. $S2$ is the space of MFP2 and MFP3. $E1$ represents the extension size of MFP3 over PFP2.

The effect of metal filed plate and polysilicon field plate on high voltage NLDMOS is investigated in this paper. Table 1 summarizes the key reference sizes of the device in Figure 1, which is a high voltage NLDMOS with V_{BD} = 772 V and drift region length = 67 μm.

The depth of DNW is 8 μm and the thickness of gate oxide is 43 nm. The field oxide thickness of PFP and MFP is 630 nm and 1 μm, respectively.

3. Experiment Results and Discussion

The breakdown voltage of high voltage device depends on the length of drift region if the drift region can be fully depleted. When the bias voltage of drain keeps on a rise, the electric field intensity will reach the critical value of silicon (E_c) and device breakdown occurs. Field plate does not change the critical electric field of silicon but reduces the peak value of electric field at a certain bias of drain and thus improves the device breakdown voltage. In an ideal case, when the device breaks down at off-state, the surface electric field is lower than E_c, which means the breakdown happens in the internal region of drift instead of on the surface of silicon. The breakdown of NLDMOS with field plate may not really occur in the internal region of drift, but the field plate can help to move the breakdown point away from the weak gate oxide region to field plate edge.

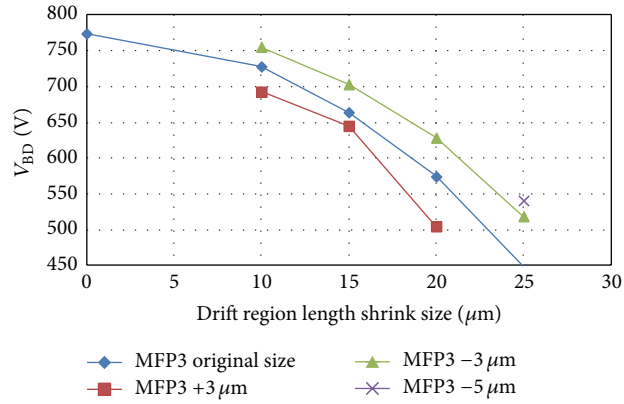

Figure 2: Breakdown voltage related to different drift length.

With the aid of process and device TCAD software, the different MFP and PFP designs and their effects on the breakdown voltage of 500 V NLDMOS have been simulated. The effect of different drift lengths also has been studied. In order to get a 500 V NLDMOS with shortest drift length and without scarifying breakdown voltage, the breakdown voltage drop caused by drift length shortening needs to be compensated by a dedicated field plate design.

Finally, a 500 V NLDMOS with small size and high breakdown voltage is obtained. The experiment result got from silicon matches the simulation data well and proves the correctness of study in this paper. This demonstrated 500 V high voltage NLDMOS meets the application requirement (higher than the 550 V, as least 10% tolerance) and shows excellent on-resistance performance.

4. The Impact of Metal Field Plate on Breakdown Voltage of NLDMOS

4.1. Effect of Metal Field Plate (Drain Side, MFP3) on V_{BD}. Figure 2 shows how the breakdown voltage changes NLDMOS as drift length shrinks at different MFP3 sizes. In this figure, the drift length shrink means shorter drift length. The reduction of MFP3 size means the increase of space $S2$ between MFP2 and MFP3. With the same MFP3, the breakdown voltage drops as drift region becomes shorter. When drift length shrinks 10 μm, the breakdown voltage drops from 774 V to 728 V and decreases by 46 V. If the drift length is determined, the breakdown voltage increases with smaller MFP3 size. When MFP3 is shortened by 3 μm, the breakdown voltage has an increase of 39 V and 51 V, respectively, for drift length reduction of 15 μm and 20 μm. It reveals that the breakdown voltage can be improved more effectively by MFP3 with shorter drift length.

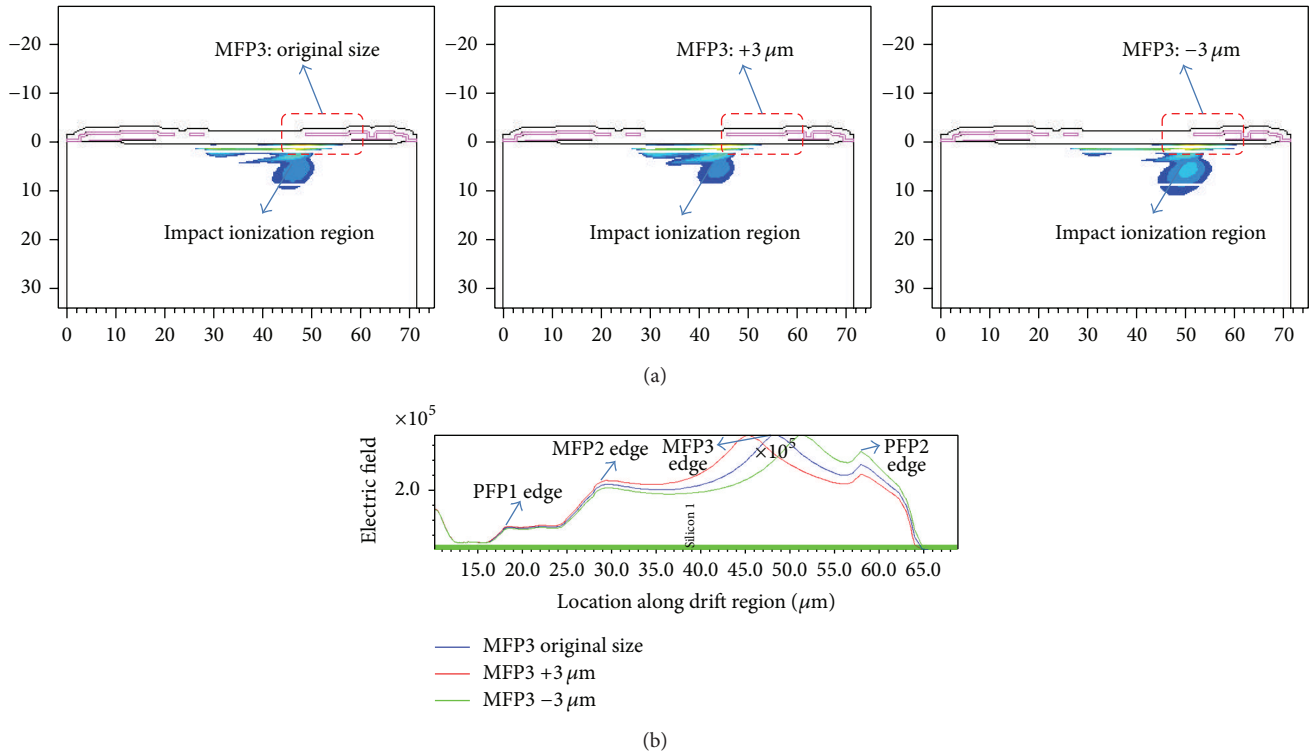

FIGURE 3: (a) Simulated impact ionization at breakdown voltage; (b) lateral electric field distribution of drift region from source to drain.

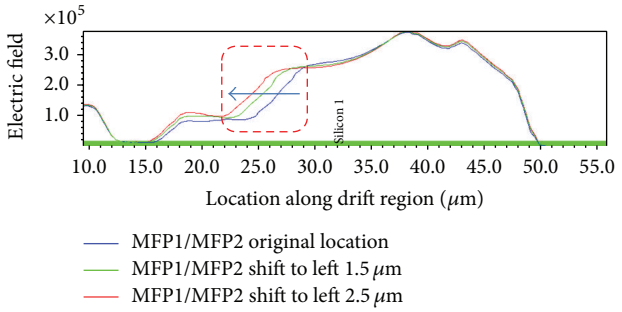

FIGURE 4: Lateral electric field distribution of different MFP2 location.

Figure 3(a) gives the impact ionization intensity pictures of 3 different MFP3 conditions: the length is changed 0 μm, +3 μm, and −3 μm. Based on the location of impact ionization, breakdown occurs at surface of drift region close to the left edge of MFP3. Figure 3(b) presents the lateral electric field distribution in the drift region from source to drain. It shows the electric field peaks locate at the right side edge of MFP2, the left side edges of MFP3 and PFP2. The highest one is peak at MFP3 edge and the breakdown also happens in this location. The electric field peak shifts to the drain side and breakdown voltage becomes higher when MFP3 size is reduced.

4.2. Effect of Metal Field Plate Location (Source Side) on V_{BD}. Figure 4 shows the simulation result of lateral electric field distribution with different MFP2 and MFP1 locations while keeping MFP3 size and space of MFP1 and MFP2 ($S1$) unchanged. According to the lateral electric field distribution shown in Figure 4, the electric field peak close to MFP2 right edge shifts to the left side as MFP1 and MFP2 shift to the left. Breakdown voltage increases by 44 V when the location changes by 2.5 μm. This reveals that the MFP2 location has effective impact on NLDMOS breakdown voltage. MFP2 moving to the left side helps to raise the breakdown voltage of the device.

TABLE 2: V_{BD} of different PFP1 experiment.

PFP size experiment	V_{BD}
0	728
PFP1 −2 μm	728.1
PFP1 +2 μm	727.1

5. The Impact of Polyfield Plate on the Breakdown Voltage of NLDMOS

Table 2 gives the simulation results of breakdown voltage for device with different PFP1 sizes. It shows that different PFP1 sizes have no obvious effect on breakdown voltage. The change of V_{BD} is less than 1 V when PFP1 increases or decreases by 2 μm.

Figure 5 is the lateral electric field distribution of PFP1 experiment. It shows the location of related electric field peak

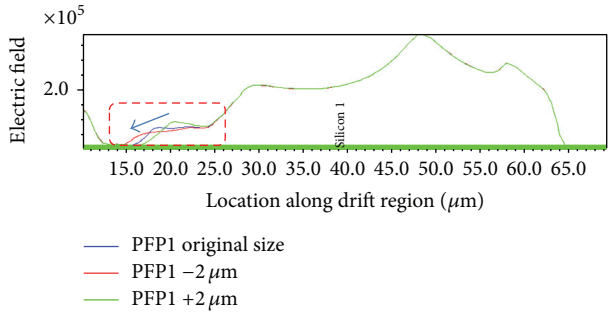

FIGURE 5: Lateral electric field distribution of different PFP1 size.

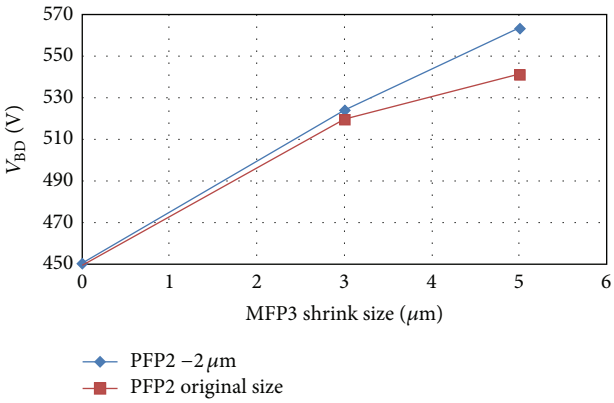

FIGURE 6: NLDMOS breakdown voltage related to MFP3 reducing sizes for different PFP2 length.

will shift as PFP1 edge location changes. The peak value in the left side is smaller than the right side.

6. Coeffect of Metal Field Gate (MFP3) and Polyfield Gate (PFP2) on the Breakdown Voltage of NLDMOS

From the above analysis, device with shorter MFP length shows higher breakdown voltage. Figure 6 tells that, at different PFP2 sizes, the improved level of breakdown voltage with the same MFP3 shrink is different. When MFP3 is reduced 3 μm, breakdown voltage is increased 70 V and 74 V, respectively, for PFP2 without change and with 2 μm reduction. The difference is 4 V and shorter PFP2 has higher breakdown voltage. When MFP3 continuously reduces by 5 μm, breakdown voltage increases by 92 V and 113 V. Their difference is enlarged to 21 V and the shorter PFP2 still has higher V_{BD}. The reason is that the highest electric field peak is changed from MFP3 left edge to PFP2 left edge as illustrated by Figure 7.

In further analysis of the NLDMOS breakdown voltage considering more MFP3 and PFP2 splits as shown in Figure 8, every PFP2 size has an optimized value of the MFP3 extending over PFP2 ($E1$). NLDMOS with this optimized $E1$ value has highest breakdown voltage. For different PFP2 size, the suitable $E1$ is between 2 μm and 5 μm. In the case of PFP2 original size, device with $E1 = 4$ μm shows highest breakdown

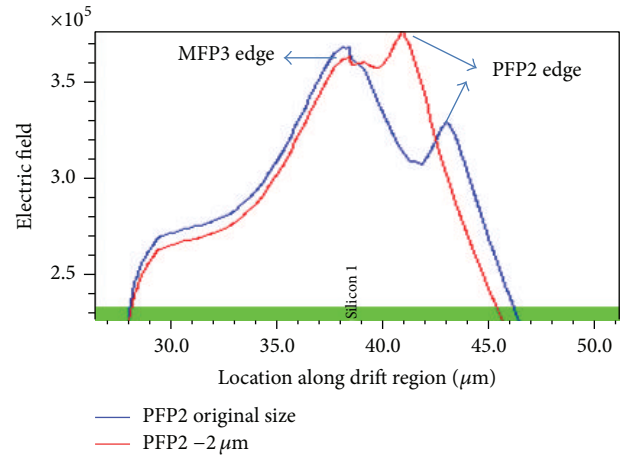

FIGURE 7: Lateral electric field distribution of MFP shrunk 5 μm for PFP2 no change and with 2 μm shrink.

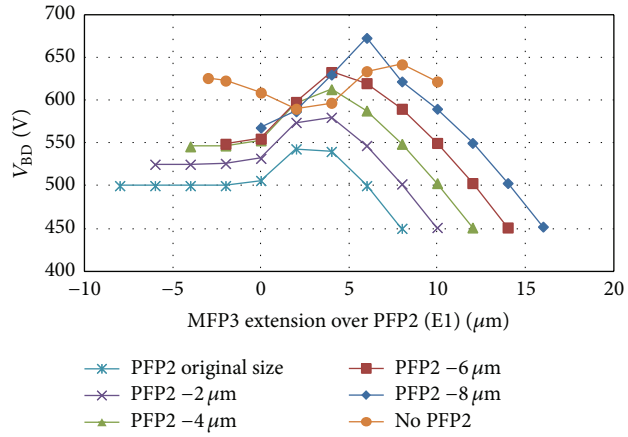

FIGURE 8: Breakdown voltage related to MFP3 extension over PFP2 ($E1$) for different PFP2 sizes.

voltage and V_{BD} starts to drop if $E1$ becomes smaller than this value. When MFP3 is shrunk 5 μm, the $E1$ is changed from 8 μm to 3 μm and the increase of breakdown voltage becomes less as Figure 6 shows.

7. Experiment Results

Based on the above study, a 500 V NLDMOS is designed with 30 μm drift length shrunk as well as metal and polysilicon field plate optimized. The breakdown voltage of simulated result and measurement data are 594 V and 590 V, respectively, as Figure 9 shows, and both results match well. The breakdown voltage meets the requirement of 500 V high voltage device.

Idvg characteristics curve of this device measured on silicon is in Figure 10. The R_{sp} calculated based on measured linear current of drain in Figure 10 is 7.88 ohm $*$ mm^2 and is about 25% less than the released data from another commercial company.

Table 3: Comparison of reference NLDMOS and this work.

Item	Reference	This work	Difference
Length of drift region (μm)	67	37	45%
V_{BD} (V)	772	590	24%

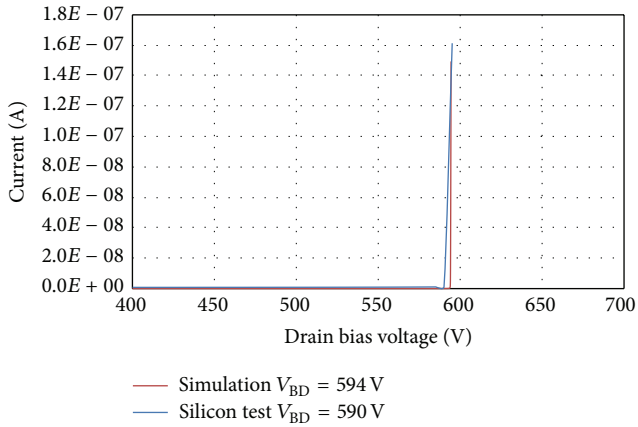

Figure 9: Breakdown voltage comparison of simulation and silicon data.

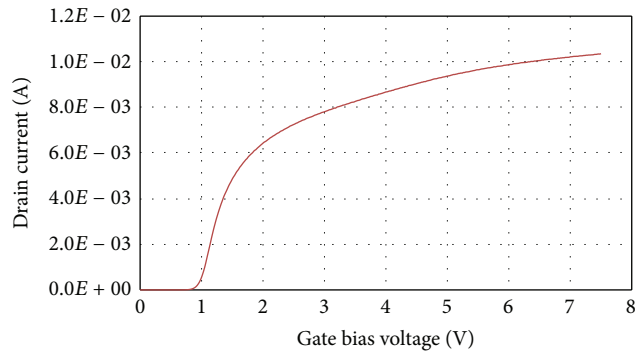

Figure 10: Idvg curve of this 500 V NLDMOS with area = 0.816 mm^2 at V_{dd} = 0.1 V. The R_{sp} is 7.88 ohm $*$ mm^2.

Compared with the referenced NLDMOS with 67 μm drift region length, the drift region of new device is shrunk by 47%. However, the V_{BD} of optimized 500 V NLDMOS is 590 V and only decreases by 24% compared to the V_{BD} of the reference one. It means that the breakdown voltage of the 500 V NLDMOS is improved a lot by this MFP and PFP design discussed in this paper. The result is summarized in Table 3.

8. Conclusion

Study of a 500 V high voltage NLDMOS and related field plate designs have been presented in this paper. The effect of metal and polysilicon field plate on the breakdown voltage has been investigated and the coeffect between MFP3 and PFP2 has also been studied. With the aid of research result, a demonstrated 500 V NLDMOS with 37 μm drift length and optimized field plate design achieves breakdown voltage of 590 V and R_{sp} of 7.88 ohm $*$ mm^2. This excellent on-resistance performance is about 25% less than the released data from another commercial company. The simulation and silicon data match well. The breakdown voltage has been greatly improved by proper field plate design. So the research result of MFP and PFP in this paper can be selected as a good reference for other high voltage designs. But the study on field plate presented in this paper does not consider the doping RESURF of drift region. It will be a direction in the further research of 500 V high voltage NLDMOS.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References

[1] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM '79)*, vol. 25, pp. 238–241, 1979.

[2] A. W. Ludikhuize, "A review of RESURF technology," in *Proceedings of the IEEE 12th International Symposium on Power Semiconductor Devices and ICs (ISPSD '00)*, pp. 11–18, 2000.

[3] D. R. Disney, A. K. Paul, M. Darwish, R. Basecki, and V. Rumennik, "A new 800 V lateral MOSFET with dual conduction paths," in *Proceedings of the 13th International Symposium on Power Semiconductor Devices and ICs (ISPSD '01)*, pp. 399–402, Osaka, Japan, June 2001.

[4] M. Qiao, Y. F. Li, X. Zhou, Z. J. Li, and B. Zhang, "A 700-V junction-isolated triple RESURF LDMOS with N-type top layer," *IEEE Electron Device Letters*, vol. 35, no. 7, pp. 774–776, 2014.

[5] S. Banerjee, V. Parthasarathy, and M. Manley, "Design of stable 700 V lateral MOSFET for new generation, low-cost off-line SMPS," in *Proceedings of the 22nd International Symposium on Power Semiconductor Devices and IC's (ISPSD '10)*, pp. 269–272, IEEE, June 2010.

[6] M. Venturato, G. Cantone, F. Ronchi, and F. Toia, "A novel 0.35 μm 800V BCD technology platform for offline applications," in *Proceedings of the 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD '12)*, pp. 397–400, June 2012.

[7] A. Wood, C. Dragon, and W. Burger, "High performance silicon LDMOS technology for 2 GHz RF power amplifier applications," in *Proceedings of the IEEE International Electron Devices Meeting*, pp. 87–90, December 1996.

[8] D. C. Burdeaux and W. R. Burger, "Intrinsic reliability of RF power LDMOS FETs," in *Proceedings of the IEEE International Reliability Physics Symposium (IRPS '11)*, pp. 435–443, April 2011.

[9] T. Miyoshi, T. Tominari, Y. Hayashi et al., "Reliability improvement in field-MOS FETs with thick gate oxide for 300-V applications," in *Proceedings of the 25th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD '13)*, pp. 393–396, 2013.

[10] K. Mao, M. Qiao, L. Jiang et al., "A 0.35 μm 700 v BCD technology with self-isolated and non-isolated ultra-low specific on-resistance DB-nLDMOS," in *Proceedings of the 25th International Symposium on Power Semiconductor Devices and IC's (ISPSD '13)*, pp. 397–400, Kanazawa, Japan, May 2013.

[11] Z. Hossain, "Determination of manufacturing RESURF process window for a robust 700V double RESURF LDMOS transistor," in *Proceedings of the 20th International Symposium on Power Semiconductor Devices and IC's (ISPSD '08)*, pp. 133–136, Orlando, Fla, USA, May 2008.

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Research Article

Responsivity Enhanced NMOSFET Photodetector Fabricated by Standard CMOS Technology

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Increasing the responsivity is one of the important issues for a photodetector. In this paper, we demonstrate an improved NMOSFET photodetector by using deep-n-well (DNW) structure which can improve the responsivity of the photodetector significantly. The experimental results show that the responsivity can be enhanced greatly by the DNW structure and is much larger than the previous work when DNW is biased with 0.5 V, while the dark current exhibits almost no increase. Further characterization indicates that the diode formed by the bulk and DNW can efficiently absorb photons and has a large gain factor of the photocurrent especially under low light condition, which gives a more promising application for the detector to detect the weak light.

1. Introduction

Image sensors based on standard CMOS technology have obtained great success in the market of mobile phones, digital cameras, and other consumer electronics, because of its low cost, low power consumption, and design flexibility [1–3]. However, in the application field with low illumination, such as biological florescence detection, weak light imaging, and astronomical observation, photodetectors with high sensitivity are necessary [4, 5]. Previously, lateral BJT-based photodetectors have been reported, in which the source, drain, and bulk of a MOSFET form a bipolar transistor to amplify the photocurrent and enhance the responsivity [6]. Based on the same operation mode, Zhang reported a high gain gate-bulk tied NMOSFET photodetector on SOI substrate. In this photodetector, the drain/bulk junction diode absorbs photons and generates electron-hole pairs. The electrons are swept to the drain while the holes accumulate in the bulk which increases the bulk potential. Because of the gate-bulk tied structure, it is then fed back to the gate. The positive feedback leads to further turn-on of the MOSFET, supplying an amplified drain/bulk diode photocurrent to the outputs [7]. But because of the low photon-absorbing efficiency and the high cost of SOI substrate, this idea is extended to bulk structure of MOSFET by us. Here, a gate-bulk tied NMOSFET transistor on deep-n-well is fabricated by standard CMOS technology. Its photoelectric characteristics are investigated. The experimental results show that the DNW/bulk diode can absorb photons efficiently and improve the responsivity significantly when DNW is positively biased while the dark current keeps almost no change.

2. Experiment

Figure 1(a) shows the cross-section of the proposed NMOSFET photodetector. It is formed by a gate-bulk tied (GB tied) NMOSFET transistor on the deep-n-well. The detector is fabricated in standard CMOS process. The size ($W \times L$) of NMOSFET is 10 μm × 0.55 μm and the gate oxide thickness is 12 nm in this study. The depth of source and drain is about 0.2 um. And the depth of the DNW is about 0.8 um. The electrical characteristics of the photodetectors are measured using Keithley 4200 semiconductor characterization system in Cascade Summit 12000 probe station employing a 150 W Xe lamp as the illumination source to emit white light. During photodetecting, the gate and bulk are tied together and left floating, the source is grounded, and the drain and DNW are biased with a positive voltage. The output current is measured in the drain side.

As shown in Figure 1(a), because the NMOSFET is fabricated on a DNW, two photodiodes are formed by the

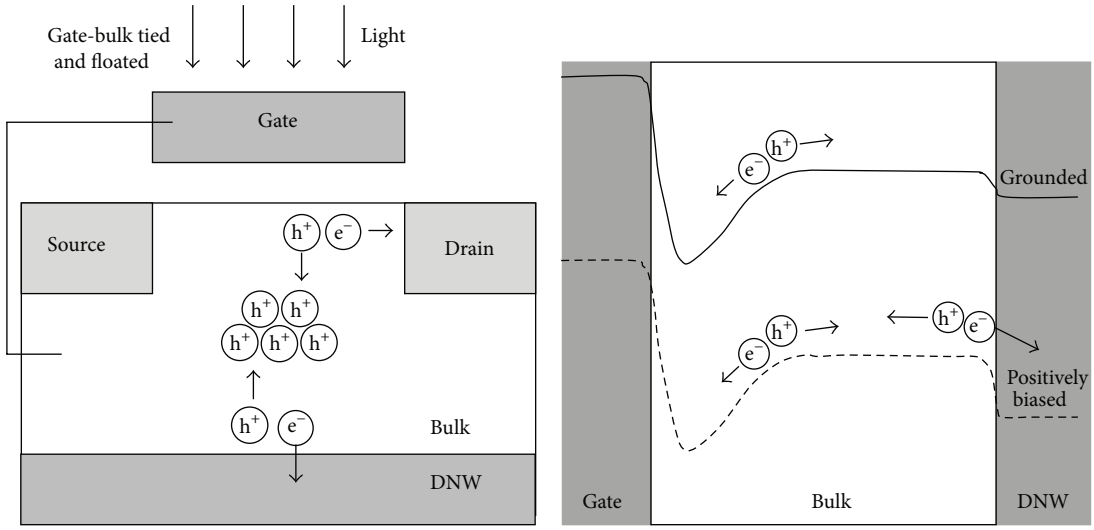

FIGURE 1: (a) The cross-section view of the responsivity enhanced NMOSFET photodetector under light condition. (b) The band diagram of the photodetector with different DNW voltages under light condition.

drain/bulk junction diode (J_1) and the DNW/bulk junction diode (J_2) during detecting. As discussed in [7], the J_1 can absorb photons during detecting and an amplified J_1 photocurrent is obtained in the drain side because of the GB tied structure. Meanwhile, J_2 can become the second source of the outputs when J_2 is reverse biased with a positive DNW voltage. Photons are absorbed in J_2 and the photogenerated holes are then injected into the bulk, which provides an additional increase of the gate potential as shown in Figure 1(b). As a result, the output photocurrent can be further increased.

Therefore, when DNW is grounded, the output current of the GB tied NMOSFET photodetector comes from the amplification of the J_1 photocurrent. When DNW is positively biased, the output current equals the sum of the amplification of the J_1 photocurrent and the amplification of the J_2 photocurrent. So the responsivity of the GB tied NMOSFET photodetector can be enhanced by the DNW structure.

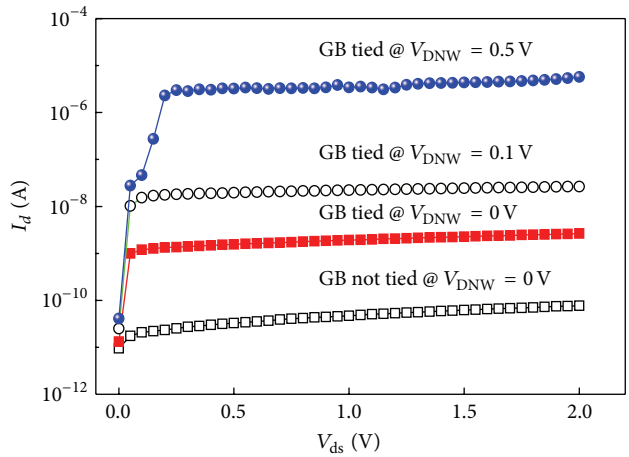

FIGURE 2: Output drain current characteristics of the photodetector under the same illumination of 2.0 μW/cm^2. Four conditions are included: (1) GB not tied with V_{DNW} = 0 V; (2) GB tied with V_{DNW} = 0 V; (3) GB tied with V_{DNW} = 0.1 V; and (4) GB tied with V_{DNW} = 0.5 V.

3. Results and Discussion

Figure 2 shows the output current (I_d) characteristics of the detector with V_{ds} under the same illumination of 2.0 μW/cm^2. Four electrical measure conditions are included: (1) GB not tied with V_{DNW} = 0 V; (2) GB tied with V_{DNW} = 0 V; (3) GB tied with V_{DNW} = 0.1 V; and (4) GB tied with V_{DNW} = 0.5 V. It can be seen that the output drain current of GB tied NMOSFET with V_{DNW} = 0 V is two orders of magnitude higher than that of GB not tied NMOSFET. This result is in agreement with previous result [7] that the output current increase comes from the amplification of photocurrent of J_1 diode due to the gate-bulk tied structure. Compared to that of V_{DNW} = 0 V, the output current of the GB tied NMOSFET photodetector can be further increased one order of magnitude when V_{DNW} = 0.1 V and nearly four orders of magnitude when V_{DNW} = 0.5 V, informing that V_{DNW} can greatly increase the output current.

We also characterize the relationship between the output current of the GB tied NMOSFET photodetector and the light intensity at V_{ds} = 0.5 V as shown in Figure 3. The output current is increased in the whole range of light intensity when DNW is positively biased. The inset picture of Figure 3 shows V_{DNW} dependence of the output dark current and photocurrent under light condition of 2.0 μW/cm^2. It is found that the output photocurrent increases exponentially with V_{DNW} before 0.5 V. Then, it remains essentially the same

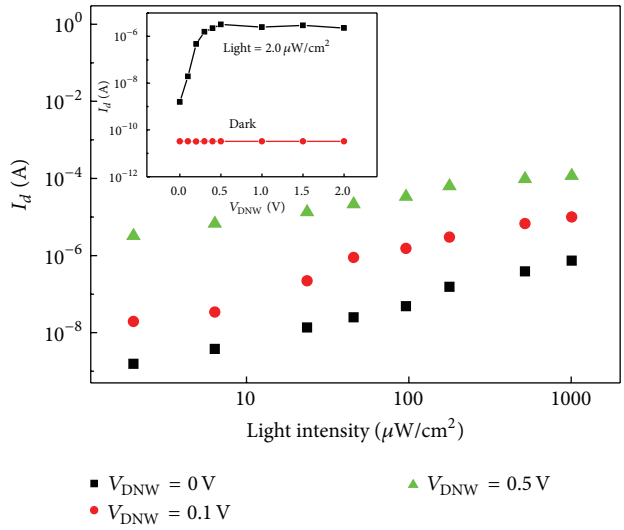

FIGURE 3: The relationship between output drain current and light intensity under different DNW voltages of the GB tied NMOSFET photodetector. The inset picture shows the V_{DNW} dependence of the output dark current and photocurrent under light condition of 2.0 μW/cm^2. The output current is measured at V_{ds} = 0.5 V.

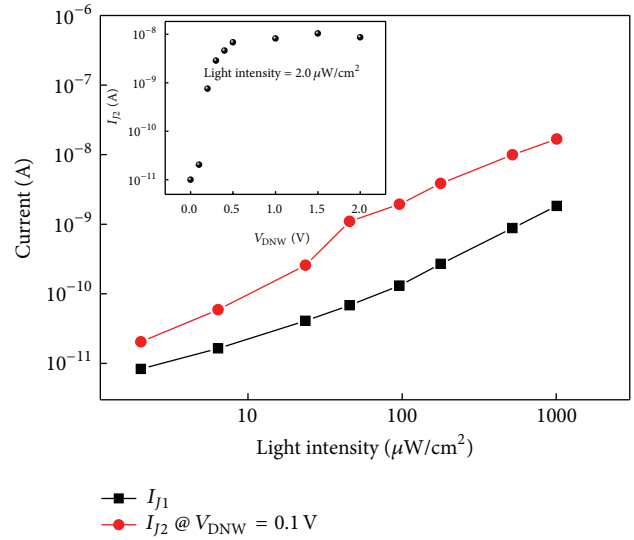

FIGURE 4: The light intensity dependence of the photocurrent of J_1 and J_2 diodes at V_{DNW} = 0.1 V. The inset picture shows the relationship between I_{J2} and V_{DNW} under light condition of 2.0 μW/cm^2.

TABLE 1: Performance comparison of published detector [7] and our detector (V_{ds} = 0.5 V and light intensity = 1 mW/cm^2).

	Published detector [7]	Calculated result according to [7]	Our detector (V_{DNW} = 0.5 V)
Photocurrent	0.1 μA (5 μm × 2 μm)	1.3 μA (10 μm × 0.55 μm)	110 μA (10 μm × 0.55 μm)
Dark current	2.9 pA (5 μm × 2 μm)	38 pA (10 μm × 0.55 μm)	32 pA (10 μm × 0.55 μm)

when DNW voltage is beyond 0.5 V. On the other hand, the dark current almost exhibits no change with the increased DNW voltage.

Table 1 lists the performance comparison of published detector [7] and our detector. We can see that the output photocurrent of our detector at V_{DNW} = 0.5 V is about 2 orders of magnitude higher than the previous work under the same light intensity and the dark current almost does not change. It is therefore concluded that our photodetectors can be greatly improved by the DNW structure and have a larger responsivity than the previous work, while the dark current almost does not change. As analyzed above, the additional increase of output photocurrent of the photodetector when DNW is positively biased comes from the amplification of the photocurrent of J_2 diode.

To further analyze the characteristics of the responsivity enhanced photodetector, the photocurrents of J_1 and J_2 diodes before amplification are measured. Figure 4 shows the light intensity dependence of measured photocurrents of J_1 and J_2 at V_{DNW} = 0.1 V. The optically generated current of J_1 diode before amplification is achieved by operating the NMOSFET in the diode mode. Note that the measured photocurrent I_{J1} has to be halved to get the J_1 diode current before amplification [7]. The photocurrent I_{J2} of J_2 diode is measured at the DNW terminal with V_{ds} = 0.5 V and V_{DNW} = 0.1 V during photodetection. It can be seen that the photocurrent of J_2 diode is nearly one order higher than that of J_1 in the whole range of light intensity, which indicates that most of the holes accumulated in the bulk come from J_2. It is because the area of J_2 is very large and can absorb photons more efficiently than J_1. Therefore, the J_2 diode can greatly increase the gate potential of the NMOSFET and contributes much more to the output photocurrent of the photodetector than J_1 as the measured results shown in Figure 2.

The inset picture of Figure 4 shows the relationship between I_{J2} and V_{DNW} under the light condition of 2.0 μW/cm^2. It can be seen that I_{J2} increases exponentially with V_{DNW} and then it is saturated when V_{DNW} exceeds 0.5 V, which can explain the relationship between the output drain photocurrent and V_{DNW} as shown in the inset picture of Figure 3.

As discussed above, the output current of the GB tied NMOSFET photodetector comes from the amplification of I_{J1} when DNW is grounded, and it equals the sum of the amplification of I_{J1} and I_{J2} when DNW is positively biased. So we can calculate the gain factors of the two photodiodes, respectively.

The gain factor of I_{J1} is calculated using the following equation:

$$\text{Gain}_{J1} = \frac{I_d\left(V_{\text{DNW}0}\right)}{0.5 I_{J1}}, \tag{1}$$

where Gain_{J1} is the gain factor of the J_1 diode photocurrent and $I_d(V_{\text{DNW}0})$ is the output current measured with V_{DNW} = 0 V.

The gain factor of I_{J2} is calculated using the following equation:

$$\text{Gain}_{J2} = \frac{I_d\left(V_{\text{DNW}}\right) - I_d\left(V_{\text{DNW0}}\right)}{I_{J2}}, \quad (2)$$

where Gain_{J2} is the gain factor of the J_2 diode photocurrent and $I_d(V_{\text{DNW}})$ is the output current measured when DNW is positively biased with V_{DNW}.

Figure 5 shows the calculated gain factor of the photocurrent of J_1 and J_2 diodes under different light intensity with $V_{\text{DNW}} = 0.1$ V. We can see that the gain factor of I_{J2} is larger than that of I_{J1} under low light condition. So our proposed new structure can efficiently enhance the responsivity of the photodetector under low light condition. It can also be found that the gain factor of I_{J1} increases at first and then decreases with illumination, while the gain factor of I_{J2} is very large under low light condition and then decreases with illumination. It is because of that that the J_1 photocurrent is very small under low light condition and little holes are accumulated in the bulk. So the NMOSFET stays in depletion region and the channel surface potential increases quickly with the increased gate potential (induced by the accumulated holes). Therefore, the gain factor of I_{J1} increases with the light intensity at first. But when the light intensity becomes large, the output drain current increases and the NMOSFET enters into strong inversion gradually. The surface potential of the NMOSFET changes very little when the gate potential continued increase [8]. So the gain factor of I_{J1} decreases when the light intensity continues to increase. On the other hand, for J_2 diode, because of the large gain factor and the large photon-absorbing efficiency of J_2 when $V_{\text{DNW}} = 0.1$ V, the NMOSFET has entered into inversion region under low light condition. So the surface potential of the NMOSFET changes very little when the light intensity continues to increase and the gain factor of J_2 decreases with the light intensity as shown in Figure 5.

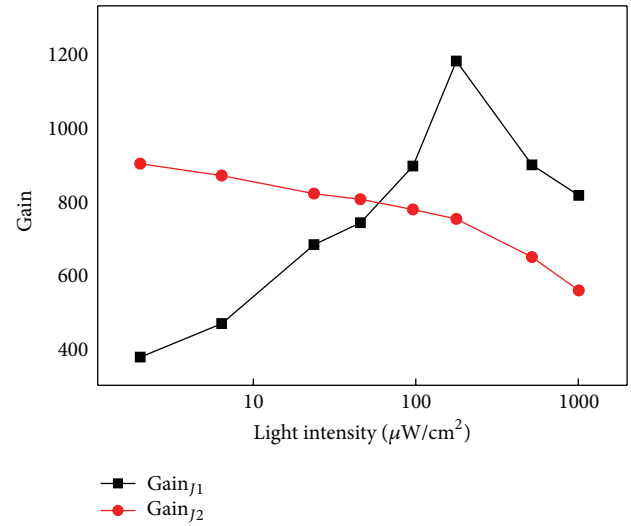

Figure 5: The gain factors of the photocurrent of J_1 and J_2 diodes under different light conditions with $V_{\text{DNW}} = 0.1$ V.

4. Conclusion

In this paper, one responsivity enhanced NMOSFET photodetector on a DNW is studied. Because of the DNW structure, the output photocurrent of the enhanced photodetector comes from two parts. One is from the amplification of the drain/bulk diode photocurrent and the other is from the amplification of the DNW/bulk diode photocurrent. Studies indicate that the photon-absorbing efficiency of the DNW/bulk diode is very high and most of the holes accumulated in the bulk come from the DNW/bulk diode. So the DNW/bulk diode contributes most of the output optical current and can greatly improve the responsivity. The experimental results show that the responsivity of our detector can be enhanced greatly by the DNW structure and the photocurrent is nearly 2 orders of magnitude higher than the previous work when DNW is biased with 0.5 V under the illumination of 1 mW/cm^2, while the dark current exhibits almost no increase. Meanwhile, the gain factor of the photocurrent of DNW/bulk diode is very large under low light condition, which can efficiently enhance the responsivity of the detector under low light condition and makes it very suitable for low light detecting.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

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References

[1] Z. Ignjatovic, D. Maricic, and M. F. Bocko, "Low power, high dynamic range CMOS image sensor employing pixel-level oversampling ΣΔ Analog-to-digital conversion," *IEEE Sensors Journal*, vol. 12, no. 4, pp. 737–746, 2012.

[2] M. Bigas, E. Cabruja, J. Forest, and J. Salvi, "Review of CMOS image sensors," *Microelectronics Journal*, vol. 37, no. 5, pp. 433–451, 2006.

[3] N. Faramarzpour, M. El-Desouki, M. J. Deen, Q. Fang, S. Shirani, and L. W. C. Liu, "CMOS imaging for biomedical applications," *IEEE Potentials*, vol. 27, no. 3, pp. 31–36, 2008.

[4] K. B. Mogensen, H. Klank, and J. P. Kutter, "Recent developments in detection for microfluidic systems," *Electrophoresis*, vol. 25, no. 21-22, pp. 3498–3512, 2004.

[5] O. Tigli, L. Bivona, P. Berg, and M. E. Zaghloul, "Fabrication and characterization of a surface-acoustic-wave biosensor in CMOS technology for cancer biomarker detection," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 1, pp. 62–73, 2010.

[6] H. Yamamoto, K. Taniguchi, and C. Hamaguchi, "High-sensitivity SOI MOS photodetector with self-amplification," *Japanese Journal of Applied Physics*, vol. 35, part 1, no. 2B, pp. 1382–1386, 1996.

[7] W. Zhang, M. Chan, and P. K. Ko, "Performance of the floating gate/body tied NMOSFET photodetector on SOI substrate,"

IEEE Transactions on Electron Devices, vol. 47, no. 7, pp. 1375–1384, 2000.

[8] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, Hoboken, NJ, USA, 3rd edition, 2007.

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Review Article

Interface Engineering and Gate Dielectric Engineering for High Performance Ge MOSFETs

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In recent years, germanium has attracted intensive interests for its promising applications in the microelectronics industry. However, to achieve high performance Ge channel devices, several critical issues still have to be addressed. Amongst them, a high quality gate stack, that is, a low defect interface layer and a dielectric layer, is of crucial importance. In this work, we first review the existing methods of interface engineering and gate dielectric engineering and then in more detail we discuss and compare three promising approaches (i.e., plasma postoxidation, high pressure oxidation, and ozone postoxidation). It has been confirmed that these approaches all can significantly improve the overall performance of the metal-oxide-semiconductor field effect transistor (MOSFET) device.

1. Introduction

After continuously pursuing higher performance complementary metal-oxide-semiconductor field effect transistor (MOSFET) devices for more than four decades, it is becoming increasingly difficult for Si-based MOSFET to enhance performance through traditional device scaling [1–5]. Recently, Ge has attracted intensive interests as the most promising channel material for next generation MOSFET because of the intrinsic higher carrier mobility in Ge than that in Si (2x higher mobility for electrons and 4x for holes) [6–14]. In order to realize high performance Ge p-type MOSFETs, advanced high-k/Ge gate stacks with scaled EOT and superior MOS interfaces are mandatory [15, 16]. Electrically active defects on the Ge surface and Ge/oxide interfaces are suspected as the probable cause of the mobility degradation of performance characteristics in MOSFETs. Hence, high quality MOS interfaces are not guaranteed due to the large amount of defects at direct high-k/Ge interfaces [17]. To solve this problem, an interfacial layer (IL) is introduced between the high-k layer and the Ge substrate, which can provide effective electrical passivation of the Ge surface. Among a variety of ILs, high quality GeO_2 has been considered as the most promising choice due to its extremely low interface defect density D_{it} ($\sim 6 \times 10^{10}\,cm^{-2}eV^{-1}$) [18] and its potential to enable high performance Ge n-MOSFETs [19]. But there is a problem: the formation of volatile GeO either during growth or at elevated temperatures around 550°C–600°C, which are often used in MOSFET processing. Initially it was believed that GeO is formed at the interface between GeO_2 and Ge. More experimental evidences though suggest that GeO is formed at the top surface of GeO_2 and desorbs at high enough temperature [20–22]. In addition, the relative dielectric constant (k-value) of GeO_2 is much lower than that of Hf- and La-based high-k gate dielectrics used for advanced Si technology [23–30]. This means that gate stacks containing thick interfacial GeO_2 layers are difficult to scale below 1 nm EOT as required for future technology nodes. Therefore, a high-k/GeO_2 IL/Ge gate stack with a high quality and ultrathin GeO_2 interfacial layer is obviously required to achieve subnanometer overall EOT in high performance Ge MOSFETs. The biggest challenge at present is how to manufacture, in a controlled manner, an ultrathin GeO_2 passivation layer without compromising its electrical quality.

The most promising route is to use well-controlled oxidation method to introduce the GeO_2 IL of very good quality. Recently, it has been reported that high quality GeO_2/Ge interfaces have been fabricated by thermal oxidation [31],

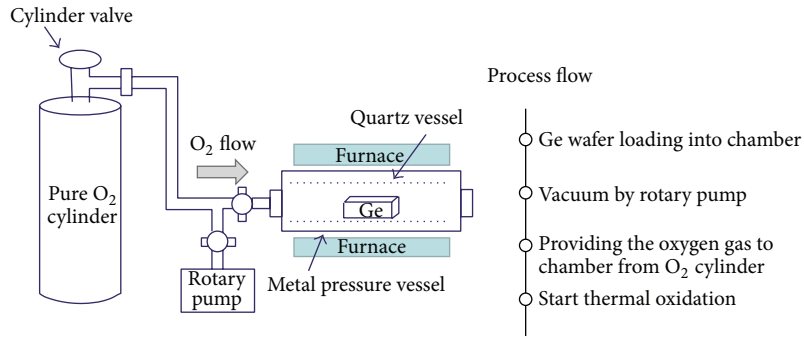

Figure 1: Schematic illustration of HPO system and process flow [35].

ozone oxidation [32], plasma oxidation [33], and so forth. Among them, high-temperature thermal oxidation [34] and ozone oxidation [35] can realize superior GeO_2/Ge MOS interfaces with a D_{it} value less than 5×10^{11} $cm^{-2}eV^{-1}$. Plasma postoxidation enables the formation of ultrathin GeO_x interfacial layer between high-k dielectrics and Ge, suitable for equivalent oxide thickness (EOT) scaling while keeping low D_{it} (~5×10^{10} $cm^{-2}eV^{-1}$) [33]. In this review, the three effective oxidation methods will be discussed in detail.

2. Ge/Dielectric Interface Passivation Methods

2.1. High-Pressure Oxidation. Many approaches were investigated to form a stable and desirable GeO_2 IL in high-k/Ge gate stack. One of the most effective methods was high-pressure oxidation. Lee et al. recently reported that the high-pressure oxidation (HPO) of germanium (Ge) for improving electrical properties of Ge/dielectric stacks was investigated [11, 34–39]. Figure 1 shows the schematic illustration of HPO system and the process flow used in their work. The system mainly composes of an oxygen cylinder, a vacuum pump, and a tube furnace. The furnace consists of a quartz oxidation tube enclosed in a steel pressure vessel.

During the process, the HPO system is evacuated to approximately 1 Pa by rotary pump after the cleaned Ge wafers are placed into quartz oxidation tube. Then, the furnace chamber surrounding the steel pressure vessel is heated to a thermal oxidation temperature. Temperature calibration of HPO furnace was carried out in the temperature range from 200°C to 600°C for precise measurements [35].

By applying the HPO method followed by low-temperature oxygen annealing (LOA), the interface state density was reduced to less than 10^{11} $cm^{-2}eV^{-1}$ near the midgap, as shown in Figure 2. Moreover, the refractive index of thermally oxidized GeO_2 was increased by HPO which is indicating higher density of GeO_2 grown by HPO, as shown in Figure 3. It was also revealed that the dielectric constant of GeO_2 increases from 5.2 in the case of atmospheric-pressure oxidation (APO) to 5.8 in the case of HPO. With HPO method followed by LOA, Lee et al. also obtained the highest hole mobility of 725 cm^2/Vs in Ge/GeO_2 gate stack which is 3.5 times higher than (100) Si universal mobility. With this method, they also demonstrated the highest electron mobility

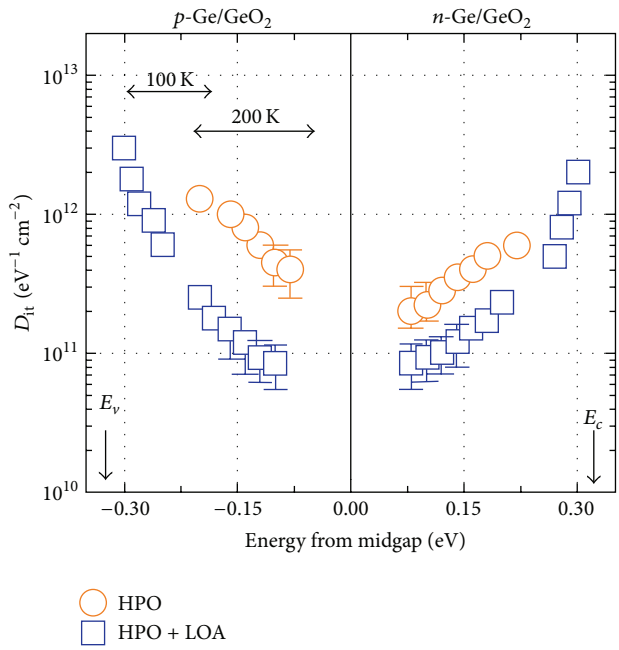

Figure 2: Energy distribution of the interface states density (D_{it}) estimated by the conductance method at 100 and 200 K. [37].

of 1920 cm^2/Vs in Ge/GeO_2/Y_2O_3 gate stack, as shown in Figure 4. Both are the record-high values of Ge MOSFETs, and this is a strong evidence that high quality Ge interface from conduction to valence band edge is possible by the Ge surface passivation. Discussed from a thermodynamic point of view, the GeO desorption from Ge/GeO_2 stacks could be efficiently suppressed by HPO.

Furthermore, by applying the combination of Y_2O_3 and low-temperature high-pressure oxidation (LT-HPO) method, Lee et al. also have demonstrated the peak mobility of 787 cm^2/Vs and high-N_s mobility (at $N_s = 1 \times 10^{13}$ cm^{-2}) of 429 cm^2/Vs in Ge n-MOSFET with sub-nm EOT, which are the highest ones to date among scaled Si and Ge MOSFETs [38]. It is expected that electrical properties of GeO_2 metal-insulator-semiconductor capacitor (MISCAP) can be further improved by optimizing the oxidation temperature and oxygen pressure of HPO.

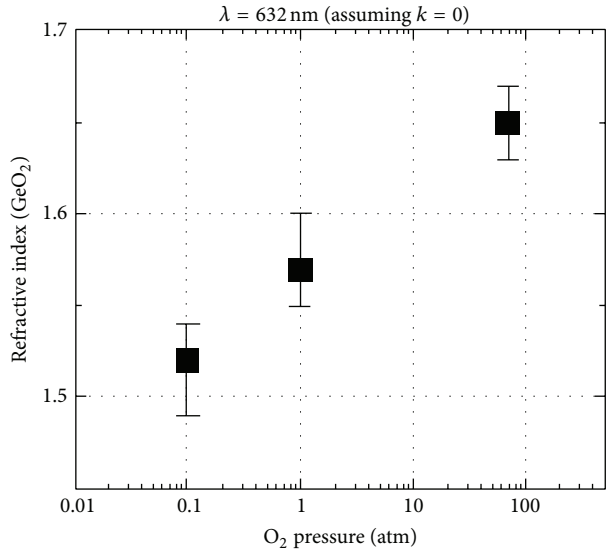

FIGURE 3: Refractive index (n) of GeO_2 films estimated by spectroscopic ellipsometry at λ of 632.8 nm under the assumption that the extinction coefficient is zero [35].

2.2. Plasma Postoxidation. O_2 plasma treatment is a very effective approach to form low defect GeO_2/Ge interfaces and GeO_2 IL at low substrate temperatures, due to the highly reactive O radicals [48, 49]. Zhang et al. have proposed a novel GeO_2 IL formation process by applying the electron cyclotron resonance (ECR) oxygen plasma to form high quality GeO_x ILs through a thin Al_2O_3 oxygen barrier, which can realize a low D_{it} and a thin EOT of around 1 nm at the same time [33]. The basic process flow is shown in Figure 5. In this plasma postoxidation method, a thin GeO_x IL is formed by oxidizing the Ge surface beneath a thin Al_2O_3 layer. The Al_2O_3 serves as a sufficient oxygen barrier which suppresses the growth of unnecessarily thick GeO_x IL. In more detail, an ultrathin (1–1.5 nm) Al_2O_3 layer is first deposited on Ge by atomic layer deposition, followed by oxygen plasma treatment to oxidize the Ge substrate. The Al_2O_3 layer then acts as a barrier layer of oxygen and effectively protects Ge surfaces from direct exposure of ECR oxygen plasma and any damages during the fabrication processes. In addition, low processing temperature provided by the ECR plasma oxidation is expected to minimize the thermal degradation of the GeO_x/Ge interface. They have improved this process to realize EOT less than 1 nm by employing this plasma postoxidation (PPO) process to HfO_2-based gate stacks [45].

A plasma postoxidation time of 10 s is sufficient to reduce D_{it} while maintaining the equivalent oxide thickness (EOT). The D_{it} of Au/Al_2O_3/GeO_x/Ge MOS capacitors is found to be significantly suppressed down to a value lower than 10^{11} $cm^{-2}eV^{-1}$. As shown in Figure 6, they can achieve the minimum D_{it} of 5×10^{10} $cm^{-2}eV^{-1}$ and 6×10^{10} $cm^{-2}eV^{-1}$ for pMOS (1.67 nm EOT) and nMOS (1.83 nm) capacitors, respectively.

High performance Ge MOSFETs with 0.98 nm (EOT) Al_2O_3/GeO_x/Ge gate stack have also been demonstrated by Zhang et al. [12]. The Ge n-MOSFETs have a record-high peak mobility of 937 cm^2/Vs as shown in Figure 7, and the Ge pMOSFETs with EOTs of 1.18, 1.06, and 0.98 nm have provided peak mobility values of 515, 466, and 401 cm^2/Vs, respectively. The Ge pMOSFET with an EOT of 0.98 nm has been found to provide around 1.8 times mobility enhancement against the previously reported values at this EOT value.

Figure 8 shows the mobility benchmark of Ge pMOSFETs in the ultrathin EOT range. From the comparison among the data record so far, a record-high peak mobility (596 cm^2/Vs) has been achieved in EOT of ~0.8 nm for HfO_2/Al_2O_3/GeO_x/Ge pMOSFETs, which is 5.1 times large as the previous value. This proves the novel gate stack structure and plasma postoxidation method can provide sufficient MOS interface passivation. In the same work, a high quality gate stack (HfO_2/Al_2O_3 (0.2 nm)/GeO_x/Ge) with a record 0.7 nm EOT was also successfully demonstrated. The D_{it} of this 0.7 nm gate stack is in the order of 10^{11} $cm^{-2}eV^{-1}$, which leads to a record 546 cm^2/Vs peak mobility.

So, we can conclude that, by applying the PPO method, one can realize both ultrathin EOT less than 1 nm and low D_{it} value at the same time. As a result, the ECR plasma postoxidation method is a promising solution for fabricating advanced high-k/GeO_x/Ge gate stacks with superior MOS interfaces and thin EOT.

2.3. Ozone Postoxidation. Ozone oxidation provides an alternative method to form a high quality GeO_2 IL. The minimum D_{it} of 3×10^{11} $cm^{-2}eV^{-1}$ was demonstrated by using ozone oxidation at 400°C [32]. In previous experimental investigation, Kuzum et al. demonstrated a ~1.5 times higher mobility than universal Si mobility, where a GeO_2 passivation layer was first formed by ozone oxidation and an Al_2O_3 dielectric was followed by ALD [50]. Considering the promising aspect of this ozone-based surface passivation, in the remainder of this review, the research of ozone postoxidation for Ge surface passivation will be discussed in more detail.

Aiming at realizing Ge surface passivation and thin EOTs at the same time, Sun et al. proposed a new ozone postoxidation (OPO) method for Al_2O_3/Ge MOS devices [46]. The OPO treatment performed on Al_2O_3/Ge gate stack is schematically shown in Figures 9 and 10 comparing the C-V characteristics of Al_2O_3/Ge MOS capacitors with different OPO times. It could be found that the sample without the OPO treatment process exhibits very poor C-V behaviors, and the C-V properties were significantly improved with the increase of the OPO time. The inset shows the EOT value of the capacitors decreases from ~2.39 nm to ~1.79 nm with the increasing time of OPO.

In order to investigate the impact of OPO treatment on the interface features of Al_2O_3/Ge gate stack, the high-resolution cross-sectional transmission electron microscopy (HR-TEM) images were taken and shown in Figure 11. It can be seen that the as-deposited sample is uniform and amorphous with a sharp interface. The physical thickness of the Al_2O_3 layer is deduced to be 3.6 nm. Furthermore, there was no GeO_2 interfacial layer (IL) growth between Al_2O_3

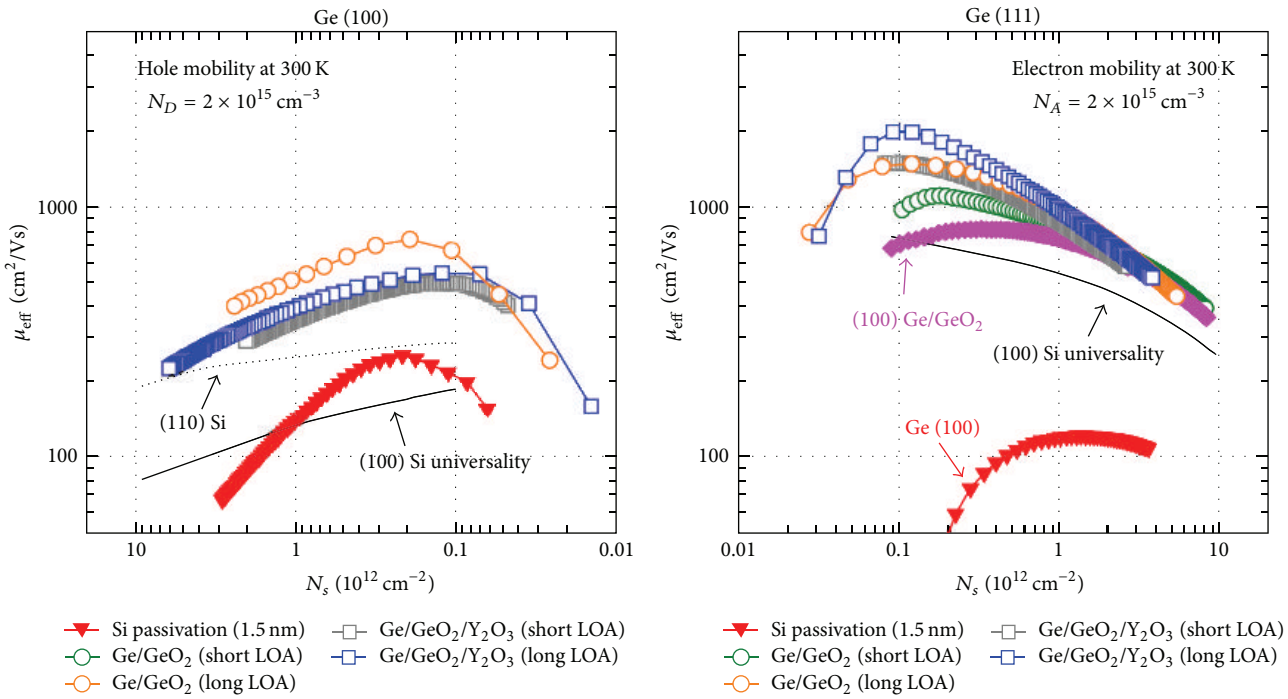

FIGURE 4: A hole mobility of 725 cm^2/Vs was achieved in Ge/GeO$_2$ gate stack with long LOA, which is 3.5 times higher than Si universal mobility. In case of electron mobility, Ge/GeO$_2$/Y$_2$O$_3$ gate stack shows the highest electron mobility of 1920 cm^2/Vs. Both are record-high values of Ge MOSFETs [11].

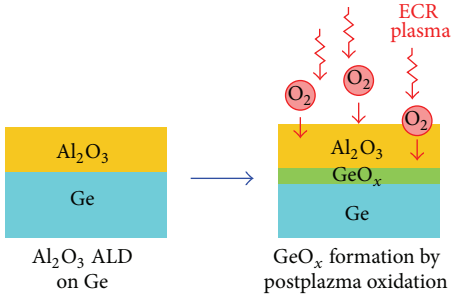

FIGURE 5: Al$_2$O$_3$/GeO$_x$/Ge gate stack formation process by using oxygen plasma through a thin ALD Al$_2$O$_3$ layer [40].

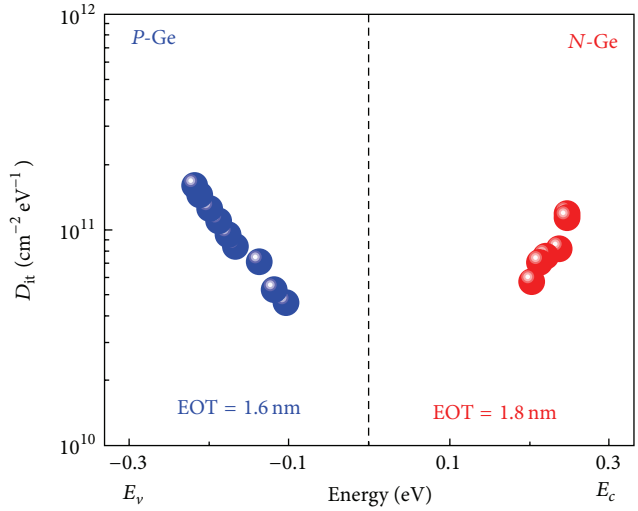

FIGURE 6: D_{it} distribution of the Au/Al$_2$O$_3$/GeO$_x$/Ge MOS capacitors versus energy [33].

films and Ge substrates even after the OPO treatment for 3 and 5 min.

To further understand the impact of the OPO treatment on Al$_2$O$_3$/Ge gate stack, the chemical components of Al$_2$O$_3$ films and the interfacial stoichiometry of all samples were examined by X-ray photoelectron spectroscopy (XPS) measurement. As shown in Figure 12, except the Ge^0 component, no germanium-related peak signals could be observed in the XPS spectrum of both as-deposited and OPO treated samples. This indicates that the Ge substrate was not oxidized after the OPO treatment even for 5 min or the amount of the GeO$_x$ at the interface is under the XPS's detection limit. It could also be found that the Al 2p spectrum of as-deposited sample exhibits two split peaks of Al–Al bonding at 73.0 eV and Al–O bonding at 74.1 eV, indicating the coexistence of the oxygen-deficient composition and the stoichiometric composition in the Al$_2$O$_3$ film. From the OPO treated samples' XPS spectra, we could find that the Al–Al bonding feature intensity rapidly decreases, while the Al–O bonding feature intensity continues to increase with the increase in the OPO time. It indicates that the OPO treatment could cure the oxygen deficiency in the Al$_2$O$_3$ film and finally enhance the average oxygen content of the film.

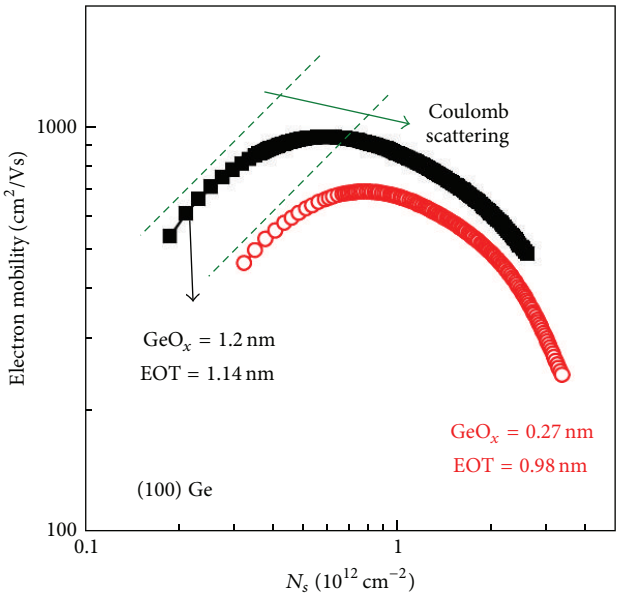

FIGURE 7: Mobilities of Ge n-MOSFETs with an $Al_2O_3/GeO_x/Ge$ gate stack having different GeO_x IL thickness [12].

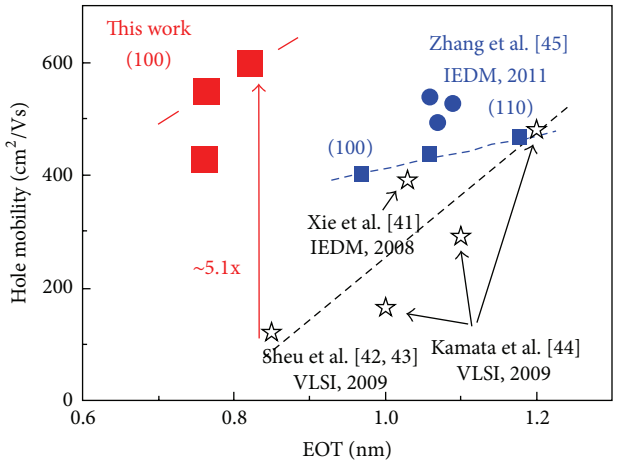

FIGURE 8: Peak mobility of Ge (100) pMOSFETs in Zhang et al.'s work versus EOT, compared with the results reported so far [41–45].

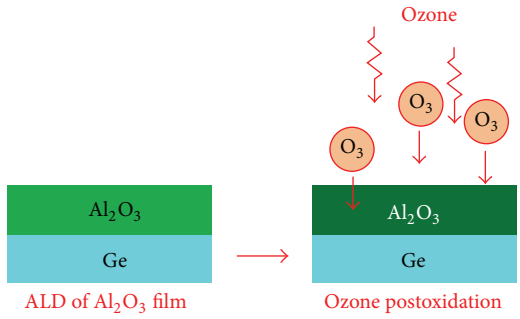

FIGURE 9: Process flow of the OPO treatment on Al_2O_3/Ge gate stack [46].

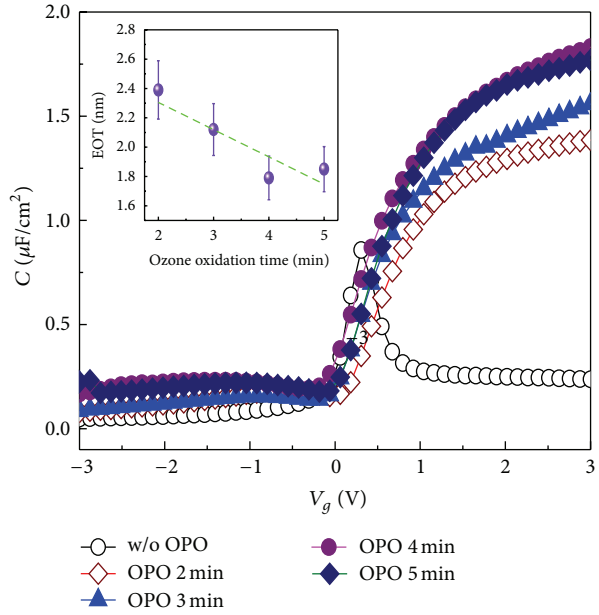

FIGURE 10: C-V characteristics (1 MHz) of Al_2O_3/Ge MOScap improved significantly with the OPO treatment. The inset shows the reduction of EOT versus the OPO treatment time [46].

The EOT value of the MOS capacitor, extracted from the C-V characterizations, decreases from ~2.39 nm to ~1.79 nm, which may be attributed to the continuous improvement in the permittivity of the ALD-Al_2O_3 film with the increase in the OPO time. After a careful process optimization with the OPO technology, sub-1 nm EOT and surface passivation could be achievable at the same time in Ge MOSFETs.

Just recently, Yang et al. have introduced the cycling ozone oxidation (COO) method into the ALD process to form a high quality $Al_2O_3/GeO_x/Ge$ stack [47]. Figure 13 shows the process flow of COO method used in their work. This COO method is proved to be effective in repairing the defects like OH-related groups to suppress the gate leakage current. The minimum D_{it} value of 1.9×10^{11} cm^{-2}eV^{-1} is obtained by inserting GeO_x passivation layer with the COO treatment, as shown in Figure 14 [47].

3. Conclusion and Further Outlook

In order to realize high-mobility Ge CMOS device, different interface control and gate dielectric enhancement methods of Ge were systematically investigated. In this review, we have summarized and discussed various interface control technologies which are effective in obtaining high quality Ge MOSFETs. For reducing the interface state density and enhancing the mobility in Ge MOSFETs, the high-pressure oxidation, plasma postoxidation, and ozone postoxidation have been proven to be very effective based on the formation of good quality Ge oxide. For high-pressure oxidation and plasma postoxidation techniques, both of them can obtain a relatively low minimum value of D_{it} in the order of 10^{11} cm^{-2}eV^{-1} even at a thin EOT of subnanometer [12, 38].

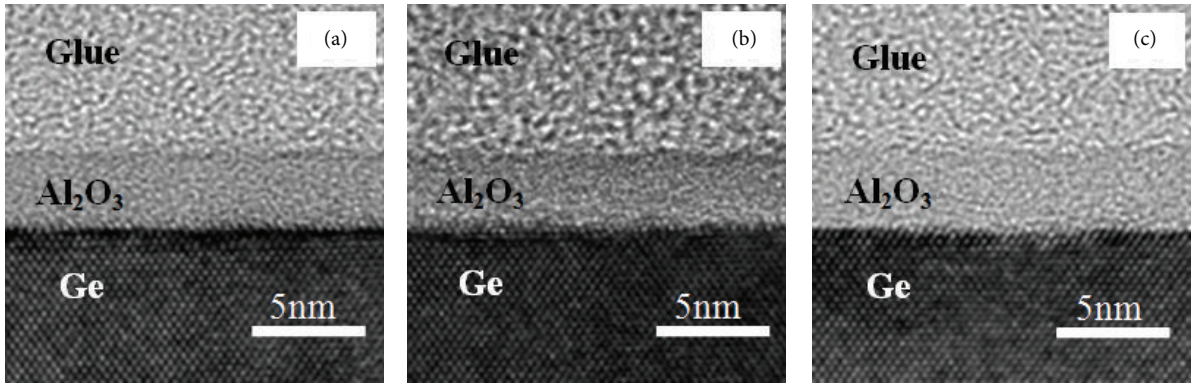

FIGURE 11: High-resolution cross-sectional transmission electron microscopy (HR-TEM) image of ALD-Al_2O_3 on Ge structure: (a) without OPO treatment; (b) OPO treatment for 3 min; and (c) OPO treatment for 5 min [46].

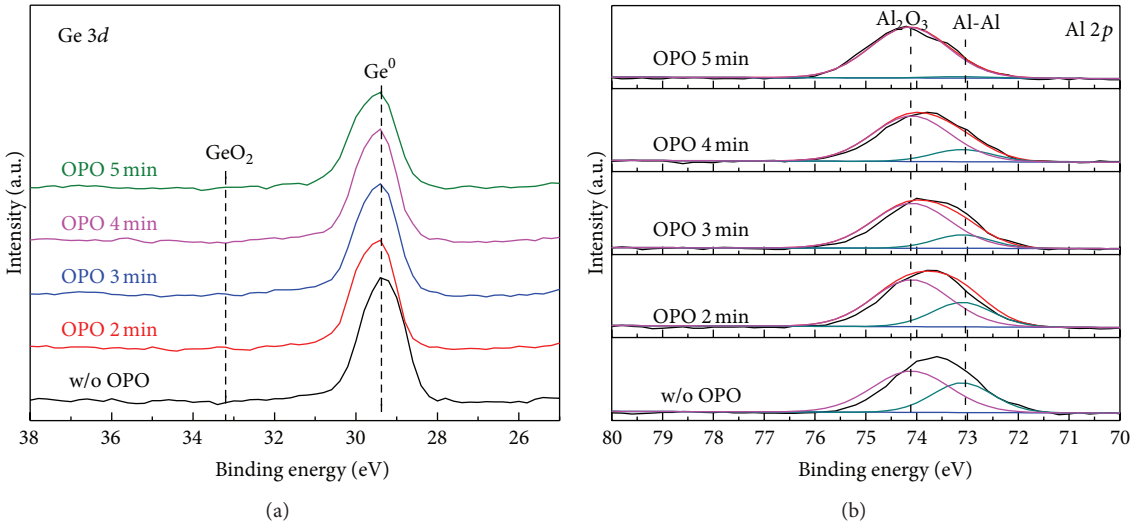

FIGURE 12: (a) Ge 3*d* and (b) Al 2*p* XPS spectra of Al_2O_3/Ge structure before and after an OPO treatment [46].

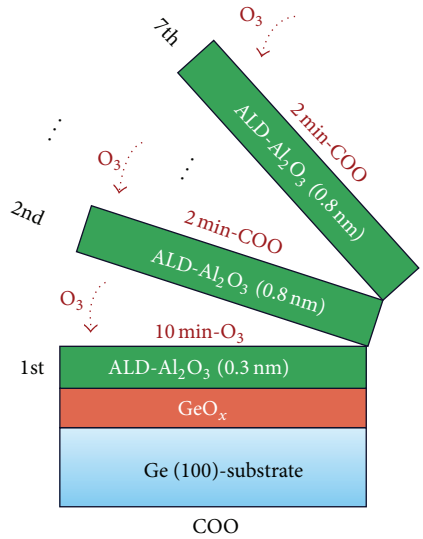

FIGURE 13: Schematic of fabrication procedure of Ge MOS gate stacks for samples with cycling ozone oxidation (COO) treatment [47].

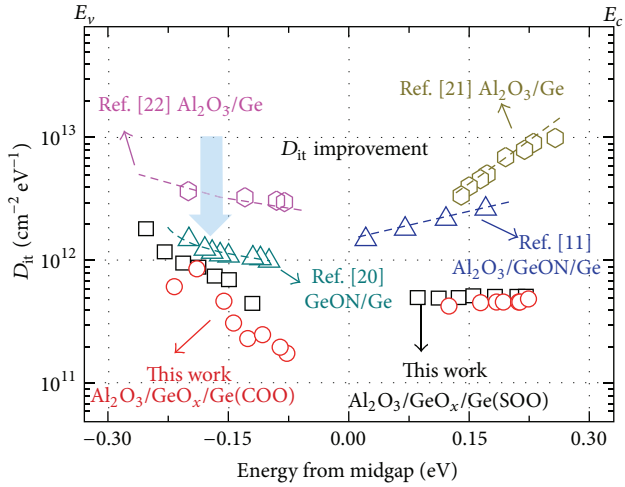

FIGURE 14: Energy distribution of D_{it} of Al_2O_3/GeO_x/Ge MOS capacitors with cycling ozone oxidation (COO) and single ozone oxidation (SOO) treatments, in comparison with previously reported data by other groups [47].

For ozone postoxidation technique, a relatively low minimum value of D_{it} of 1.9×10^{11} $cm^{-2}eV^{-1}$ was also obtained under a relatively thick EOT (definite data not given in their report) [47]. Thus, these three techniques are all potential methods to improve the interfacial properties of Ge/dielectric gate stack in Ge MOSFETs.

It is noted that there are still several challenges for this Ge MOS interface passivation technique. The high-pressure oxidation technique has to be performed under a high pressure of ~70 atm, and thus its applicability to integrate with the current Si CMOS technology is still not clear. On the other hand, the plasma postoxidation technique is well approved in planar Ge MOSFETs. However, its applicability in 3D channel device, especially the gate-all-around (GAA) device, is not investigated yet. For ozone postoxidation, it is still desired to examine the scalability of Ge gate stacks. Due to the drawbacks or limits of each technique, further optimization is still needed to improve the mobility and to scale down the EOT in Ge MOSFETs. The compatibility with existing integrated circuit technology platform is also an important issue.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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References

[1] K. Mistry, C. Allen, C. Auth et al., "A 45 nm logic technology with high-k$^+$metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM '07)*, Technical Digest, pp. 247–250, Washington, DC, USA, December 2007.

[2] Y. Kamata, "High-k/Ge MOSFETs for future nanoelectronics," *Materials Today*, vol. 11, no. 1-2, pp. 30–38, 2008.

[3] M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM '11)*, Technical Digest, pp. 1.1.1–1.1.6, Washington, DC, USA, 2011.

[4] E. J. Nowak, "Advanced CMOS scaling and FinFET technology," *ECS Transactions*, vol. 50, no. 9, pp. 3–16, 2012.

[5] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Transactions on Electron Devices*, vol. 59, no. 7, pp. 1813–1828, 2012.

[6] S. Takagi, T. Mizun, T. Tezuka et al., "Channel structure design, fabrication and carrier transport properties of strained-Si/SiGe-On-Insulator (strained-SOI) MOSFETs," in *Proceedings of the International Electron Devices Meeting (IEDM '03)*, Technical Digest, pp. 3.3.1–33.3.4, Washington, DC, USA, December 2003.

[7] K. Kita, K. Kyuno, and A. Toriumi, "Growth mechanism difference of sputtered HfO_2 on Ge and on Si," *Applied Physics Letters*, vol. 85, no. 1, pp. 52–54, 2004.

[8] T. Krishnamohan, D. Kim, T. V. Dinh et al., "Comparison of (001), (110) and (111) uniaxial- and biaxial- strained-Ge and strained-Si PMOS DGFETs for all channel orientations: mobility enhancement, drive current, delay and off-state Leakage," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM '08)*, Technical Digest, pp. 899–892, San Francisco, Calif, USA, December 2008.

[9] M. Caymax, G. Eneman, F. Bellenger et al., "Germanium for advanced CMOS anno 2009: a SWOT analysis," in *Proceedings of the International Electron Devices Meeting (IEDM '09)*, Technical Digest, pp. 461–464, Baltimore, Md, USA, December 2009.

[10] R. Pillarisetty, B. Chu-Kung, S. Corcoran et al., "High mobility strained germanium quantum well field effect transistor as the P-channel device option for low power (Vcc = 0. 5 V) III-V CMOS architecture," in *Proceedings of the International Electron Devices Meeting (IEDM '10)*, Technical Digest, pp. 150–153, 2010.

[11] C. H. Lee, T. Nishimura, T. Tabata et al., "Ge MOSFETs performance: impact of Ge interface passivation," in *Proceedings of the International Electron Device Meeting (IEDM '10)*, Technical Digest, pp. 416–419, Washington, DC, USA, 2010.

[12] R. Zhang, N. Taoka, P. Huang, M. Takenaka, and S. Takagi, "1-nm-thick EOT high mobility Ge n- and p-MOSFETs with ultrathin GeOx/Ge MOS interfaces fabricated by plasma post oxidation," in *Proceedings of the International Electron Devices Meeting (IEDM '11)*, Technical Digest, pp. 642–645, Washington, DC, USA, December 2011.

[13] R. Zhang, P.-C. Huang, J.-C. Lin, M. Takenaka, and S. Takagi, "Physical mechanism determining Ge p- and n-MOSFETs mobility in high Ns region and mobility improvement by atomically Flat GeOx/Ge interfaces," in *Proceedings of the International Electron Devices Meeting (IEDM '12)*, Technical Digest, pp. 371–374, Washington, DC, USA, 2012.

[14] B. Duriez, G. Vellianitis, M. J. H. van Dal et al., "Scaled *p*-channel Ge FinFET with optimized gate stack and record performance integrated on 300 mm Si wafers," in *Proceedings of the International Electron Devices Meeting (IEDM '13)*, Technical Digest, pp. 20.1.1–20.1.4, Washington, DC, USA, December 2013.

[15] S. Takagi, T. Maeda, N. Taoka et al., "Gate dielectric formation and MIS interface characterization on Ge," *Microelectronic Engineering*, vol. 84, no. 9-10, pp. 2314–2319, 2007.

[16] A. Toriumi, T. Tabata, C. Hyun Lee, T. Nishimura, K. Kita, and K. Nagashio, "Opportunities and challenges for Ge CMOS—control of interfacing field on Ge is a key," *Microelectronic Engineering*, vol. 86, no. 7–9, pp. 1571–1576, 2009.

[17] C. Lin, H. Chang, Y. Chen et al., "Interfacial layer-free ZrO_2 on Ge with 0.39-nm EOT, κ ~43, ~2×10^{-3} A/cm^2 gate leakage, SS =85 mV/dec, Ion/Ioff =6×10^5, and high strain response," in *Proceedings of the International Electron Devices Meeting (IEDM '12)*, Technical Digest, pp. 23.2.1–23.1.4, San Francisco, Calif, USA, December 2012.

[18] Y. Fukuda, T. Ueno, S. Hirono, and S. Hashimoto, "Bend-mode liquid crystal cells stabilized by aligned polymer walls," *Japanese Journal of Applied Physics*, vol. 44, no. 2, p. 981, 2005.

[19] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi, "Proof of Ge-interfacing concepts for metal/high-k/Ge CMOS, Ge-intimate material selection and interface conscious process flow," in *Proceedings of the International Electron Devices Meeting (IEDM '07)*, Technical Digest, pp. 697–700, December 2007.

[20] K. Kita, S. K. Wang, M. Yoshida et al., "Comprehensive study of GeO_2 oxidation, GeO desorption and GeO_2-metal interaction. Understanding of Ge processing kinetics for perfect interface control," in *Proceedings of the International Electron Device Meeting (IEDM '09)*, Technical Digest, pp. 693–696, Baltimore, Md, USA, December 2009.

[21] S. K. Wang, K. Kita, C. H. Lee et al., "Desorption kinetics of GeO from GeO_2/Ge structure," *Journal of Applied Physics*, vol. 108, Article ID 054104, 2010.

[22] S. K. Wang, K. Kita, T. Nishimura, K. Nagashio, and A. Toriumi, "Isotope tracing study of GeO desorption mechanism from GeO_2/Ge stack using ^{73}Ge and ^{18}O," *Japanese Journal of Applied Physics*, vol. 50, Article ID 04DA01, 2011.

[23] E. P. Gusev, D. A. Buchanan, E. Cartier et al., "Ultrathin high-K gate stacks for advanced CMOS devices," in *Proceedings of the International Electron Devices Meeting (IEDM '01)*, Technical Digest, pp. 451–454, December 2001.

[24] C. Choi, C.-Y. Kang, S. J. Rhee et al., "Aggressively scaled ultrathin undoped HfO_2 gate dielectric (EOT < 0.7 nm) with tan gate electrode using engineered interface layer," *IEEE Electron Device Letters*, vol. 26, no. 7, pp. 454–457, 2005.

[25] R. Puthenkovilakam, M. Sawkar, and J. P. Changa, "Electrical characteristics of postdeposition annealed HfO_2 on silicon," *Applied Physics Letters*, vol. 86, no. 20, Article ID 202902, 2005.

[26] Y. Zhao, M. Toyama, K. Kita, K. Kyuno, and A. Toriumi, "Moisture-absorption-induced permittivity deterioration and surface roughness enhancement of lanthanum oxide films on silicon," *Applied Physics Letters*, vol. 88, no. 7, Article ID 072904, 2006.

[27] Y. Zhao, K. Kita, K. Kyuno, and A. Toriumi, "Higher-k $LaYO_x$ films with strong moisture resistance," *Applied Physics Letters*, vol. 89, Article ID 252905, 2006.

[28] Y. Zhao, K. Kita, K. Kyuno, and A. Toriumi, "Band gap enhancement and electrical properties of La_2O_3 films doped with Y_2O_3 as high-k gate insulators," *Applied Physics Letters*, vol. 94, no. 4, Article ID 042901, 3 pages, 2009.

[29] Y. Zhao, K. Kita, K. Kyuno, and A. Toriumi, "Dielectric and electrical properties of amorphous La_{1-x} Ta_x O_y films as higher-k gate insulators," *Journal of Applied Physics*, vol. 105, no. 3, Article ID 034103, 2009.

[30] Y. Zhao, "Design of higher-k and more stable rare earth oxides as gate dielectrics for advanced CMOS devices," *Materials*, vol. 5, no. 8, pp. 1413–1438, 2012.

[31] H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, "Evidence of low interface trap density in GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *Applied Physics Letters*, vol. 93, no. 3, Article ID 032104, 2008.

[32] D. Kuzum, T. Krishnamohan, A. J. Pethe et al., "Ge-interface engineering with ozone oxidation for low interface-state density," *IEEE Electron Device Letters*, vol. 29, no. 4, pp. 328–330, 2008.

[33] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "Al_2O_3/GeO_x/Ge gate stacks with low interface trap density fabricated by electron cyclotron resonance plasma postoxidation," *Applied Physics Letters*, vol. 98, no. 11, Article ID 112902, 2011.

[34] C. H. Lee, T. Tabata, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "Ge/GeO_2 interface control with high-pressure oxidation for improving electrical characteristics," *Applied Physics Express*, vol. 2, no. 7, Article ID 071404, 2009.

[35] C. H. Lee, T. Tabata, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "Ge/GeO_2 interface control with high pressure oxidation for improving electrical characteristics," *ECS Transactions*, vol. 19, no. 1, pp. 165–173, 2009.

[36] T. Nishimura, C. H. Lee, T. Tabata et al., "High-electron-mobility Ge n-channel metal-oxide-semiconductor field-effect transistors with high-pressure oxidized Y_2O_3," *Applied Physics Express*, vol. 4, no. 6, Article ID 064201, 2011.

[37] C. H. Lee, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "High-electron-mobility Ge/GeO2 n-MOSFETs with two-step oxidation," *IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp. 1295–1301, 2011.

[38] C. H. Lee, C. Lu, T. Tabata, T. Nishimura, K. Nagashio, and A. Toriumi, "Enhancement of high-Ns electron mobility in sub-nm EOT Ge n-MOSFETs," in *Proceedings of the Symposium on VLSI Technology Digest of Technical*, T29, p. T28, Kyoto, Japan, June 2013.

[39] C. H. Lee, T. Nishimura, C. Lu, W. Zhang, K. Nagashio, and A. Toriumi, "Significant enhancement of high-N-s electron mobility in Ge n-MOSFETs with atomically flat Ge/GeO_2 interface," *ECS Transactions*, vol. 61, pp. 147–156, 2014.

[40] S. Takagi, R. Zhang, and M. Takenaka, "Ge gate stacks based on Ge oxide interfacial layers and the impact on MOS device properties," *Microelectronic Engineering*, vol. 109, pp. 389–395, 2013.

[41] R. Xie, T. H. Phung, W. He et al., "High mobility high-π/Ge pMOSFETs with 1 nm EOT-new concept on interface engineering and interface characterization," in *Proceedings of the IEDM Technical Digest*, pp. 1–4, San Francisco, Calif, USA, 2008.

[42] S.-S. Sheu, P.-C. Chiang, W.-P. Lin et al., "A 5ns fast write multi-level non-volatile 1Kb its RRAM memory with advance write scheme," in *Proceedings of the IEEE Symposium on VLSI Technology. Digest of Technical Papers*, pp. 82–83, 2009.

[43] S.-S. Sheu, P.-C. Chiang, W.-P. Lin et al., "A 5ns fast write multi-level non-volatile 1Kbits RRAM memory with advance write scheme," in *Proceedings of the IEEE VLSI Symposium Technical Digest*, pp. 82–83, 2009.

[44] Y. Kamata, A. Takashima, Y. Kamimuta, and T. Tezuka, "New approach to form EOT-scalable gate stack with strontium germanide interlayer for high-k/Ge MISFETs," in *Proceedings of the IEEE Symposium on VLSI Technology. Digest of Technical Papers*, pp. 78–79, 2009.

[45] R. Zhang, P. C. Huang, N. Taoka, M. Takenaka, and S. Takagi, "High mobility Ge pMOSFETs with 0.7 nm ultrathin EOT using HfO_2/Al_2O_3/GeO_x/Ge gate stacks fabricated by plasma post oxidation," in *Proceedings of the Symposium on VLSI Technology (VLSIT '12)*, pp. 161–162, June 2012.

[46] J. Sun, Z. Yang, Y. Geng et al., "Equivalent oxide thickness scaling of Al_2O_3/Ge metal—oxide—semiconductor capacitors with ozone post oxidation," *Chinese Physics B*, vol. 22, no. 6, Article ID 067701, 2013.

[47] X. Yang, S. Wang, X. Zhang et al., "Al_2O_3/GeO_x gate stack on germanium substrate fabricated by in situ cycling ozone oxidation method," *Applied Physics Letters*, vol. 105, no. 9, Article ID 092101, 2014.

[48] Y. Fukuda, Y. Yazaki, Y. Otani, T. Sato, H. Toyota, and T. Ono, "Low-temperature formation of high-quality GeO_2 interlayer

for high-κ gate dielectrics/Ge by electron-cyclotron-resonance plasma techniques," *IEEE Transactions on Electron Devices*, vol. 57, no. 1, pp. 282–287, 2010.

[49] Q. Xie, D. Deduytsche, M. Schaekers et al., "Effective electrical passivation of Ge(100) for HfO_2 gate dielectric layers using O_2 plasma," *Electrochemical and Solid-State Letters*, vol. 14, no. 5, pp. G20–G22, 2011.

[50] D. Kuzum, T. Krishnamohan, A. Nainani et al., "Experimental demonstration of high mobility Ge NMOS," in *Proceedings of the International Electron Devices Meeting (IEDM '09)*, Technical Digest, pp. 1–4, Baltimore, Md, USA, December 2009.

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Research Article

Ozone Treatment Improved the Resistive Switching Uniformity of $HfAlO_2$ Based RRAM Devices

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$HfAlO_2$ based resistive random access memory (RRAM) devices were fabricated using atomic layer deposition by modulating deposition cycles for HfO_2 and Al_2O_3. Effect of ozone treatment on the resistive switching uniformity of $HfAlO_2$ based RRAM devices was investigated. Compared to the as-fabricated devices, the resistive switching uniformity of $HfAlO_2$ based RRAM devices with the ozone treatment is significantly improved. The uniformity improvement of $HfAlO_2$ based RRAM devices is related to changes in compositional and structural properties of the $HfAlO_2$ resistive switching film with the ozone treatment.

1. Introduction

Resistive switching phenomena in transitional metal oxide, such as HfO_x, TaO_x, are actively studied in order to apply them to the resistive random access memory (RRAM) [1–3]. RRAM is one of the most promising candidates for next generation of nonvolatile memory owing to its excellent performance, such as simple structure, low power consumption, fast switching speed, long retention time, and CMOS technology compatibility [4–6]. However, the key electrical characteristics of oxide-based RRAM devices still have random dispersion, such as operation voltage and high/low resistance values [7–12]. One of the main challenges that hinder RRAM devices from practical device application is exploring effective ways to suppress the fluctuations of key switching parameters, thus improving the resistive switching uniformity. Some technological methods have been presented to improve uniformity in oxide-based RRAM, such as using ion doping technical approach, specific top electrode materials, inserting interface layer between oxide and electrode, and applying certain operation model [9–12].

Ozone (O_3) treatment can change the compositional and structural properties of the oxide films which may have an effect on the resistance switching behavior of RRAM [13, 14]. In this paper, we investigated the electrical characteristics of $HfAlO_2$ based RRAM devices under different treatment processes and observed that the resistive switching uniformity of $HfAlO_2$ based RRAM devices can be significantly improved under the ozone treatment condition. The improvement of resistive switching uniformity is discussed.

2. Experiment

A 5 nm thick $HfAlO_2$ layer was fabricated on the Pt/Ti/SiO_2/Si substrate using atomic layer deposition by modulating deposition cycles for HfO_2 (derived from $Hf[N(CH_3)(C_2H_5)]_4$ and H_2O precursors) and Al_2O_3 (derived from $Al(CH_3)_3$ and H_2O precursors) at 250°C. The deposition cycle ratio of $HfO_2 : Al_2O_3$ was set 9 : 1. After the $HfAlO_2$ film deposition, some samples were treated in O_3 ambient at 100°C for 30 minutes; other samples without O_3 treatment were kept as control samples. Subsequently, a TaN top electrode with an area of 100 μm × 100 μm was fabricated by magnetron sputtering through a liftoff process. Cross-sectional RRAM stacks are schematically shown in Figure 1. The electrical characteristics of the fabricated RRAM devices were measured using a Keithley 4200 semiconductor parameter analyzer with biased voltage top and grounded bottom electrodes at room temperature. Scanning electron microscopy (SEM) and X-ray photoelectron spectroscopy (XPS) were used to evaluate the structure and compositional characteristics of the $HfAlO_2$ film.

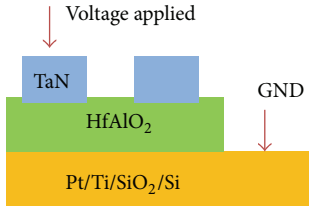


FIGURE 1: Schematic of the fabricated Pt/$HfAlO_2$/TaN memory device.

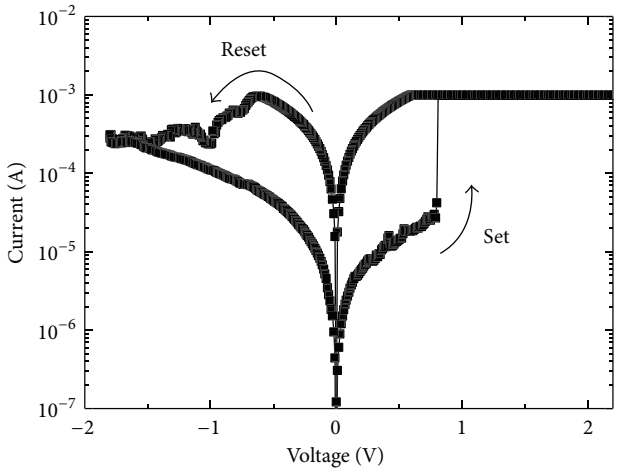


FIGURE 2: The typical current-voltage characteristic of the as-deposited $HfAlO_2$ based RRAM devices.

3. Results and Discussion

All the fresh $HfAlO_2$ based RRAM devices show high resistance state (HRS). An electric forming process with a high voltage was needed to realize reversible resistive switching, which is a precondition for activation of the soft breakdown of the $HfAlO_2$ film. After the electric forming process, stable reversible resistive switching between HRS and low resistance state (LRS) could be achieved in the $HfAlO_2$ based RRAM devices. Figure 2 shows the typical current-voltage (I-V) characteristics of as-deposited $HfAlO_2$ based RRAM devices without the ozone treatment. Typical bipolar resistive switching behaviors were observed in the RRAM devices. A current compliance (CC) during set process is necessary to protect the devices from damage. It can be seen from Figure 2 that the sharp set process from high resistance state (HRS) to low resistance state (LRS) takes place under positive voltage sweep and gradual reset process from LRS to HRS takes place under negative sweep.

The statistical distributions of key memory parameters of the $HfAlO_2$ based RRAM devices were measured by direct current (DC) voltage sweeping mode. Figures 3(a) and 3(b) compared the statistical distributions of HRS resistance (R_{HRS}) and LRS resistance (R_{LRS}) and set voltage (V_{set}) and reset voltage (V_{reset}) from cycle to cycle separately between the $HfAlO_2$ based RRAM devices with and without the ozone treatment. Significantly reduced dispersions of both R_{LRS} and R_{HRS} and V_{set} and V_{reset} are observed in the devices with ozone treatment. The resistance ratios of HRS to LRS in the $HfAlO_2$ based RRAM devices with the ozone treatment are more than 10 during the 512 cycles of DC resistive switching test, as shown in Figure 4.

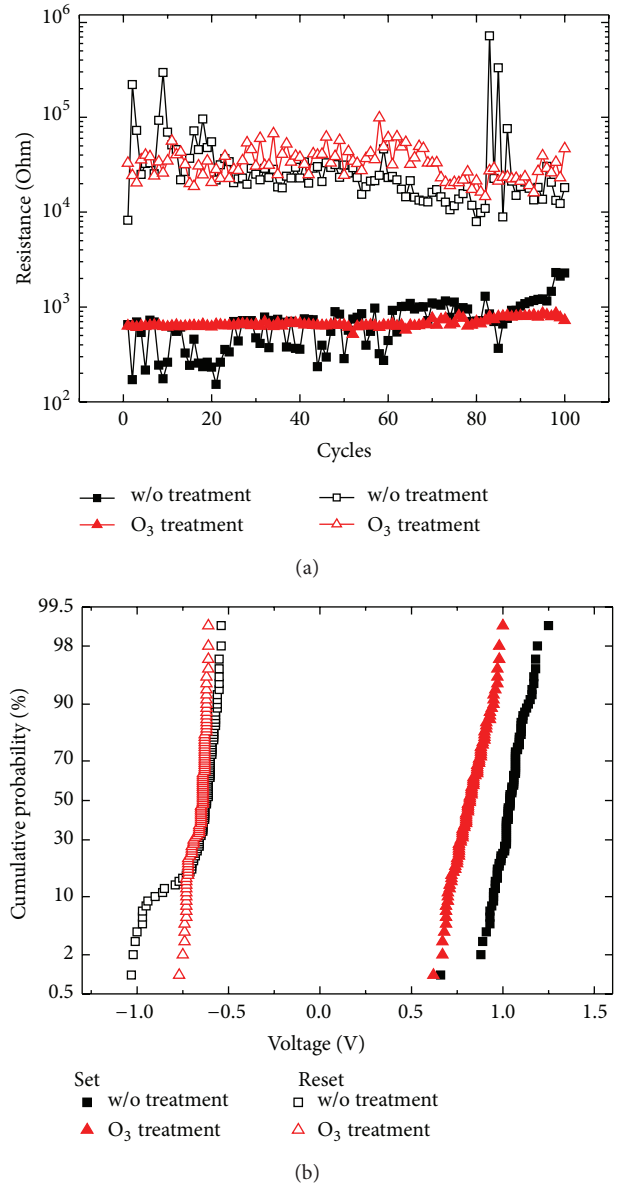


FIGURE 3: Measurement of devices for continuous 100 cycles in DC sweeping mode on different treatment conditions: (a) distribution of the R_{HRS} and R_{LRS} as a function of switching cycles, (b) V_{set} and V_{reset} voltage distribution.

Figure 5 shows the SEM images of the $HfAlO_2$ films with and without the ozone treatment. SEM measurement results revealed that surfaces of the as-deposited $HfAlO_2$ films were featureless and smooth. The nanoparticles' size of as-deposited $HfAlO_2$ films is about 25 nm while it became larger to 30 nm after the ozone treatment. Figure 6 shows the X-ray photoelectron spectroscopy (XPS) of the O 1s and Hf 4f orbitals of argon sputtered $HfAlO_2$ films with spectrum aligned to C 1s on different treatment conditions. XPS depth analysis on the samples with and without the ozone treatment

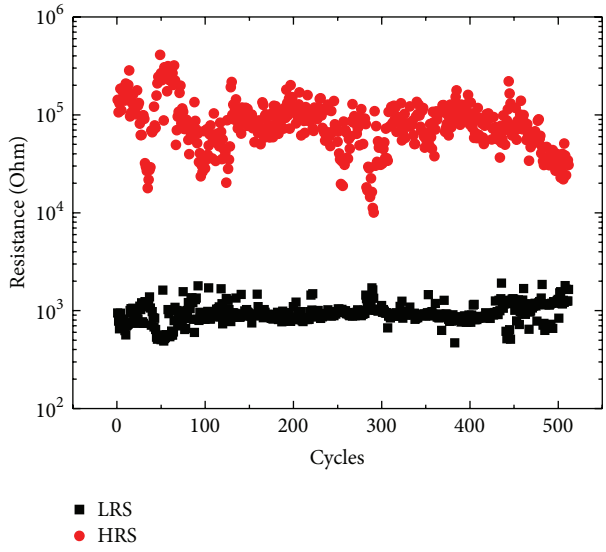
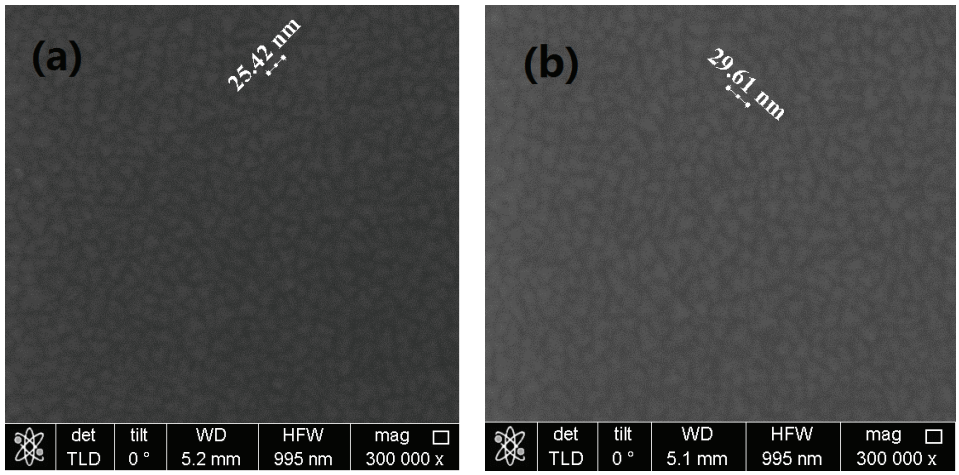


Figure 4: The variation of resistance ratios of HRS to LRS in the $HfAlO_2$ RRAM devices with the ozone treatment.



(a) (b)

Figure 5: SEM images of $HfAlO_2$ film (a) as-deposited (b) with the ozone treatment.

were also carried out. For the as-deposited $HfAlO_2$ film, the banding energy of Hf $4f_{7/2}$ and Hf $4f_{5/2}$ was around 16 and 18 eV, respectively, and O 1s was around 530 eV, consistent with the HfO_2 composition [4]. After the ozone treatment, the two distinct peaks corresponding to the Hf $4f_{7/2}$ and $4f_{5/2}$ of the Hf-O merged into one and the banding energy of O1s and Al 2s also increased, which could be attributed to the partial formation of new Hf-Al-O structure in the $HfAlO_2$ resistive switching film [13].

Various mechanisms have been proposed to explain the resistive switching behaviors in oxide-based RRAM devices, among which the formation/rupture of nanoscale conductive filaments (CFs) that consisted of oxygen vacancies (Vo) in the resistive switching layer has been widely recognized [15]. The origin of the switching performance variation may be due to the random formation of the CFs. Two possible reasons may be responsible for the improvement of resistive switching uniformity in the $HfAlO_2$ RRAM devices with the ozone treatment. First, ozone treatment can increase the film crystallinity, which could provide easy migration of oxygen vacancies along the grain boundaries [16], so oxygen vacancy conductive filaments can be formed in a more orderly way. Second, ozone treatment may change the compositional characteristic of the $HfAlO_2$ resistive switching layer and partially form the new Hf-Al-O structure, which is supported by the XPS results. Therefore, the improvement of resistive switching uniformity in $HfAlO_2$ based RRAM devices with the ozone treatment is related to the changes in compositional and structural properties of the $HfAlO_2$ resistive switching film after the ozone treatment.

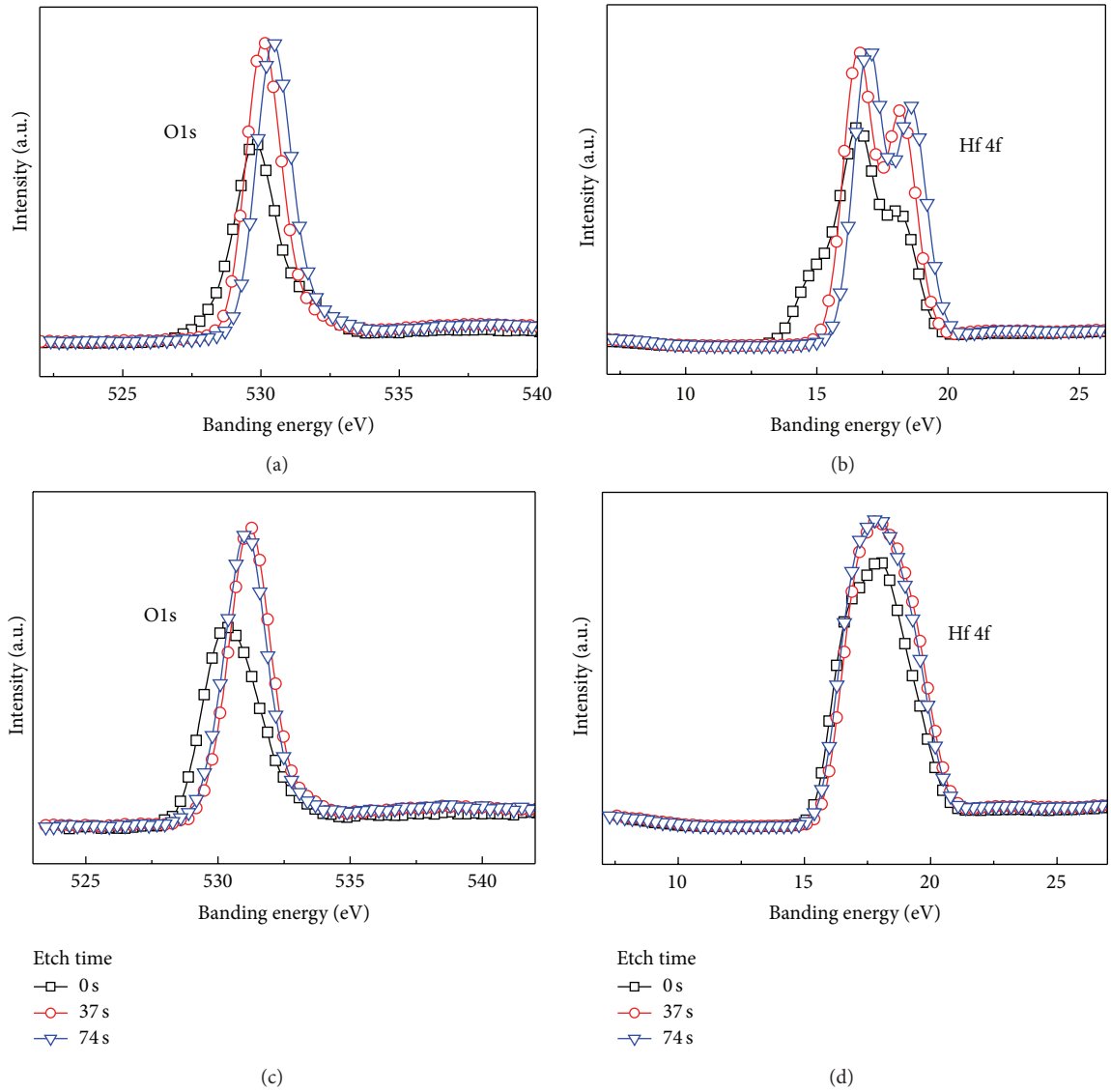


Figure 6: XPS O1s and Hf4f spectra of argon sputtered resistive switching films on different treatment conditions: (a) and (b) without the ozone treatment and (c) and (d) with the ozone treatment.

4. Conclusions

$HfAlO_2$ based RRAM devices were fabricated using atomic layer deposition. The effects of ozone treatment on the resistive switching uniformity of $HfAlO_2$ based RRAM devices were investigated. Ozone treatment significantly improved the resistive switching uniformity of $HfAlO_2$ based RRAM devices. The SEM and XPS measurement results indicate that the uniformity improvement of $HfAlO_2$ based RRAM devices with the ozone treatment is related to the changes in compositional and structural properties of the $HfAlO_2$ resistive switching film with the ozone treatment.

Conflict of Interests

The authors declare no competing financial interest.

Acknowledgments

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References

[1] Y. Z. Guo and J. Robertson, "Materials selection for oxide-based resistive random access memories," *Applied Physics Letters*, vol. 105, no. 2, Article ID 223516, 2014.

[2] M. Zhang, S. Long, G. Wang et al., "Set statistics in conductive bridge random access memory device with Cu/HfO_2/Pt structure," *Applied Physics Letters*, vol. 105, Article ID 193501, 2014.

[3] H.-S. P. Wong, H.-Y. Lee, S. M. Yu et al., "Metal-oxide RRAM," *Proceedings of the IEEE*, vol. 100, no. 6, pp. 1951–1970, 2012.

[4] H. Akinaga and H. Shima, "Resistive random access memory (ReRAM) based on metal oxides," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2237–2251, 2010.

[5] S. Yu, H.-Y. Chen, B. Gao, J. Kang, and H.-S. P. Wong, "HfOx-based vertical resistive switching random access memory suitable for bit-cost-effective three-dimensional cross-point architecture," *ACS Nano*, vol. 7, no. 3, pp. 2320–2325, 2013.

[6] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Materials*, vol. 6, no. 11, pp. 833–840, 2007.

[7] P.-T. Liu, Y.-S. Fan, and C.-C. Chen, "Improvement of resistive switching uniformity for Al-Zn-Sn-O-based memory device with inserting HfO_2 layer," *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1233–1235, 2014.

[8] Y. S. Chen, B. Chen, B. Gao, L. F. Liu, X. Y. Liu, and J. F. Kang, "Well controlled multiple resistive switching states in the Al local doped HfO_2 resistive random access memory device," *Journal of Applied Physics*, vol. 113, no. 16, Article ID 164507, 2013.

[9] H. W. Zhang, L. F. Liu, B. Gao et al., "Gd-doping effect on performance of HfO_2 based resistive switching memory devices using implantation approach," *Applied Physics Letters*, vol. 98, no. 4, Article ID 042105, 2011.

[10] H. Jiang and Q. Xia, "Improvement of resistive switching uniformity for TiO_2-based memristive devices by introducing a thin HfO_2 layer," *Journal of Vacuum Science & Technology B: Microelectronics & Nanometer Structures*, vol. 31, no. 6, Article ID 6FA04, 2013.

[11] C.-Y. Lin, C.-Y. Wu, C.-Y. C.-Y. Wu et al., "Effect of top electrode material on resistive switching properties of ZrO_2 film memory devices," *IEEE Electron Device Letters*, vol. 28, no. 5, pp. 366–368, 2007.

[12] H. T. Liu, H. B. Lv, B. H. Yang et al., "Uniformity improvement in 1T1R RRAM with gate voltage ramp programming," *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1224–1226, 2014.

[13] Z. R. Wang, W. G. Zhu, A. Y. Du et al., "Highly uniform, self-compliance, and forming-free ALD HfO_2-based RRAM with Ge doping," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 1203–1208, 2012.

[14] J. B. Sun, Z. W. Yang, Y. Geng et al., "Equivalent oxide thickness scaling of Al_2O3/Ge metal-oxide-semiconductor capacitors with ozone post oxidation," *Chinese Physics B*, vol. 22, no. 6, Article ID 067701, 2013.

[15] B. Gao, B. Sun, H. W. Zhang et al., "Unified physical model of bipolar oxide-based resistive switching memory," *IEEE Electron Device Letters*, vol. 30, no. 12, pp. 1326–1328, 2009.

[16] M. Y. Chan, T. Zhang, V. Ho, and P. S. Lee, "Resistive switching effects of HfO_2 high-k dielectric," *Microelectronic Engineering*, vol. 85, no. 12, pp. 2420–2424, 2008.