Journal of Nanotechnology

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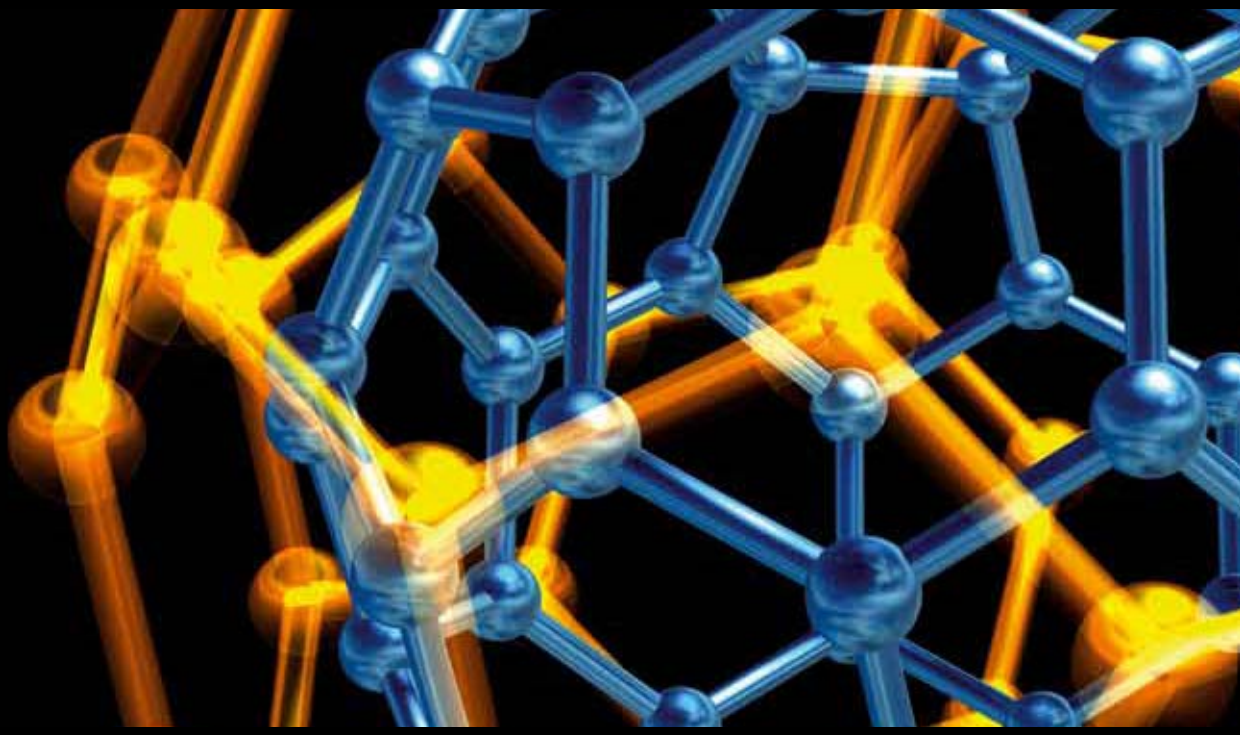
Guest Editors: QiHua Xiong, Craig A. Grimes, Margit Zacharias, Anna Fontcuberta i Morral, Kenji Hiruma, and GuoZhen Shen



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Editorial Board

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Editorial

Semiconductor Nanowires and Nanotubes: From Fundamentals to Diverse Applications

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Research in the field of semiconductor nanowires (SNWs) and nanotubes has been progressing into a mature subject with several highly interdisciplinary subareas such as nanoelectronics, nanophotonics, nanocomposites, biosensing, optoelectronics, and solar cells. SNWs represent a unique system with novel properties associated to their one-dimensional (1D) structures. The fundamental physics concerning the formation of discrete 1D subbands, coulomb blockade effects, ballistic transport, and many-body phenomena in 1D nanowires and nanotubes provide a strong platform to explore the various scientific aspects in these nanostructures. A rich variety of preparation methods have already been developed for generating well-controlled 1D nanostructures and from a broad range of materials. The present special issue focuses on the recent development in the mechanistic understanding of the synthesis, the studies on electrical/optical properties of nanowires and their applications in nanoelectronics, nanophotonics, and solar-energy harvesting.

In this special issue, we have several invited review articles and contributed papers that are addressing current status of the fundamental issues related to synthesis and the diverse applications of semiconducting nanowires and nanotubes. One of the papers reviews the progress of the top-down approach of developing silicon-based vertically aligned nanowires to explore novel device architectures and integration schemes for nanoelectronics and clean energy applications. Another paper reviews the recent developments and experimental evidences of probing the confined optical and acoustic phonon in nonpolar semiconducting (Si and Ge) nanowires using Raman spectroscopy. The paper by K. Hiruma et al. spotlights the III–V semiconductor nanowires and demonstrates selective-area metal organic vapor phase epitaxy grown GaAs/In(Al)GaAs and InP/InAs/InP nanowires with heterojunctions along their axial and radial directions. The paper written by K. Tateno et al. also reviews the vapor-liquid-solid (VLS-) grown core-multishell Ga(In)P/GaAs/GaP nanowires on Si substrates and introduces an interesting phenomenon of formation of flat-top nanowires achieved by using small-sized Au particles in one growth procedure.

The remaining papers illustrate the research on metal oxides semiconducting materials which are well known for wide band gap and transparent conducting properties. The paper by N. Bao et al. reviews the transparent films of self-assembled TiO_2 nanotube arrays, bulk heterojunction solar cells, ordered heterojunction solar cells, and liquid-junction dye-sensitized solar cells. The paper by J. Pan et al. provides a helpful review of the research activities focused on synthesis of 1D SnO_2 nanostructures and their devices applications in gas sensing, lithium-ion batteries, and nanophotonics. The paper by D. Gedamu et al. demonstrates the studies

of different routes of fabrication of ZnO semiconducting nanowires between microstructural contacts formed directly on a silicon chip. The paper by C.-T. Liu et al. focuses on the synthesis of ZnO-nanoparticles to fabricate a mask-free thin-film transistor by ink-jet printing. The emerging process for fabricating printable transistors with ZnO nanoparticles as the active channel and Poly(4-vinylphenol) matrix as the gate dielectric, respectively, suggests that the printable materials and the printing technology enable the use of all printed low-cost flexible displays for transparent electronic applications.

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Research Article

Procedures and Properties for a Direct Nano-Micro Integration of Metal and Semiconductor Nanowires on Si Chips

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1-dimensional metal and semiconductor nanostructures exhibit interesting physical properties, but their integration into modern electronic devices is often a very challenging task. Finding the appropriate supports for nanostructures and nanoscale contacts are highly desired aspects in this regard. In present work we demonstrate the fabrication of 1D nano- and mesostructures between microstructured contacts formed directly on a silicon chip either by a thin film fracture (TFF) approach or by a modified vapor-liquid-solid (MVLS) approach. In principle, both approaches offer the possibilities to integrate these nano-meso structures in wafer-level fabrications. Electrical properties of these nano-micro structures integrated on Si chips and their preliminary applications in the direction of sensors and field effect transistors are also presented.

1. Introduction

Nanowires, that is, 1D metal and semiconductor structures, have gained immense research interest due to their potential role in the miniaturization of modern electronic devices, for example, sensors with improved responses, and so forth. Due to high surface-to-volume (S/V) ratio, nanowires exhibit extraordinary electrical features, and thus they have become the important components of micro- and nanoelectronic devices [1]. In the past few years, progress in the synthesis and characterization of nanowires is thus driven by the need to understand the novel physical properties of 1D nanoscale materials and their potential applications in constructing nanoscale electronic and optoelectronic devices [2]. As a result, the interest in 1D nano-microstructures has increased exponentially, and many synthesis techniques have already been disclosed to the scientific community in the last few years. However, understanding of the basic working principles and easy fabrications of nanowires are still under progress. One of the most challenging tasks is to integrate these 1D wires into device as one requires nanoscale connecting contacts. Possible options include an independent synthesis of nanowires as first step and then integrating them into the devices. However, it is more effective to perform direct fabrication of nanowires between the contacts on microstructured Si-chips. Various methods such as templates [3–5], solution growths [6], lithographic methods (electron beam and conventional) [7, 8], vapor-liquid-solid (VLS) and its modified versions [9–11], and several others have been employed to synthesize 1D structures. Many of these methods stated earlier are either too slow or too expensive when one looks from mass fabrication or market point of view. An optimal integration route should add minimal additional fabrication steps to the processes and has to be compatible either with the already structured circuits or allowing a further microstructuring of the circuit elements after the installation of nanostructures. In this paper, two direct integration recipes for metal and semiconductor nanostructures will be presented and discussed as well as their properties will be compared. One approach is based on a thin film fracture approach [12–14]; the other one is based on a modified vapor liquid solid process allowing bridging between the contacts through interpenetrating junctions.

2. Experimental: Fabrication of 1D Nano-Microstructures

The methods used here produce single- or polycrystalline nanostructures. In present work, two synthesis methods have been carried out which enable us for direct integration of nanowire structures into the micropatterned chips.

2.1. VLS and Modified VLS Approaches. The vapor-liquid-solid (VLS) or the vapor-solid (VS) processes are typically utilized to grow vertically aligned nanostructures such as nanorods, nanowires, nanoSails and nanocombs, and so forth. VLS growth process [15] can be performed in a simple tube furnace equipped with vacuum system and gas flow control. The needed recipes are the precursor material, catalytic nanoparticles, and the substrate on which structures will be grown. Experimental variants are temperature, gas flow rate, and relative distances between source and substrates. The precursor material, that is, ZnO powder, is mixed with graphite powder in appropriate ratio to adjust the Zn vapor pressure. Addition of graphite powder helps to reduce the decomposition temperature of ZnO via chemical reaction [16, 17]. The ceramic crucible filled with ZnO-graphite mixture is placed in the centre of the tube, and the substrates coated with catalytic particles are mounted both sides linearly at equal distances from the crucible along the tube axis in the tube furnace. The VLS growth process can be understood in the following 3 steps. (i) Heating the furnace above a critical temperature (>900°C), the ZnO: graphite mixture is transformed into Zn and CO vapor [18] and Zn vapor atoms are transported by the carrier gas (oxygen and Ar mixture) to the substrates carrying catalytic particles. (ii) Since the temperature of the substrates is higher than the eutectic melting point of the precursor material (Zn) and catalytic particles (Au) [19], Au-ZnO liquid alloy droplet is formed with the necessary oxygen utilized from the carrier gas. (iii) After supersaturation, the additional precursor material (ZnO) is continuously deposited at the bottom of alloy-droplet, and the droplet is lifted up due to capillary force. During cooling, the phase separation occurs resulting in formation of 1D rods with catalytic particles on the top [20–22]. In typical VLS process, temperature, amount of precursor material, size of catalytic particles, and the gas flow rate are the main controlling parameters for growth of 1D structures like nanorods, nanowires, nanoSails and so forth. The fabricated 1D nanostructures show various different growth directions resulting in different shapes of nanostructures ranging from nanorods to nanoSails, and so forth. Figures 1(a) to 1(d) show the nano-microstructures grown by conventional VLS approach in a tube furnace using gold nanoparticles (NPs) as the catalysts. In conventional VLS, catalytic Au NPs offer the main driving force for growth of ZnO structures, and they always remain on the top (circular marked regions) as can be clearly seen in Figures 1(a) and 1(d). It has already been emphasized that the size of Au NPs is an important parameter responsible for the geometry of ZnO nanostructures. When the diameter of gold NPs is relatively small, growth of ZnO nanorods occurs (Figure 1(a)) with NPs on the top; however, if the particle diameter is large enough formation of nanoSail type structures takes place as shown in Figures 1(b) to 1(d) with increasing order of magnifications. For instance, fabrication details of nanorods and nanoSails are described in our previous works [11, 23] whereas the corresponding electron microscopy images are shown in Figure 1.

Figures 1(e) to 1(g) demonstrate the SEM morphologies of different structures grown by modified VLS approach [24] without using the catalytic gold nanoparticles. Nanomast-type ZnO structures were reproducibly grown by MVLS approach and are shown in Figure 1(e). Different types of vertical standing ZnO nanowires (e.g., shown in Figure 1(f)) were also grown on different substrates by using MVLS technique. The working temperature in MVLS technique varies from 800°C to 1000°C, and more details about this are reported somewhere else [24]. In order to demonstrate the versatility of MVLS approach, experiments for growing nanostructures from other metal oxides were also performed, and successful results were obtained. For example, Figure 1(g) shows the SEM image of SnO_2 nanowires grown by MVLS approach.

Apart from the success of the conventional VLS process, several issues are still left undisclosed which motivated us to modify the VLS approach. We simplified VLS approach in terms of using simple muffle-type box furnace in air rather than tube furnace equipped with vacuum control. In modified vapor-liquid-solid (MVLS) approach [24], neither any catalytic particles are needed nor any substrate limitation is there; however, the relative output as well as degree of freedom for synthesizing different nano-meso-microstructures is higher. Several 1D nano-microstructures and their mesoscopic network can be synthesized in a reproducible manner by MVLS approach. Family of different structures have been found in a single growth process itself which could be an advantage for the device performance. Just for demonstration, we have shown some structures here; however, a detailed paper on the growth will be published elsewhere. In this work, our main focus is on a simple way to integrate such a type of nanostructure into Si-chips.

Various fabrication schemes exist to integrate 1D nanowires in Si-structures, for example, to utilize the large surface to volume ratio for a sensor, see [25–27]. All those fabrication schemes grow micro- or nanowires from one contact side to another side by utilizing several lithography steps. Furthermore, all approaches contain a certain statistics about how many bridges form between the contacts; see, for example, [27]. To simplify all those approaches to form a connection between two sides, we carry out growth from both contact sides in parallel and utilize those wires which interpenetrate in between the contacts. The connection formed by interpenetration is usually of high quality as only matching epitaxial directions allow a connection. Like the other approaches, our approach also relies on statistics; however, the following example shows that this does not mean a lack of control. The interconnection probability depends on the distance between the contacts, the length of the contacts, the density of the grown nanowire structures, and the thickness and length of the nanowires.

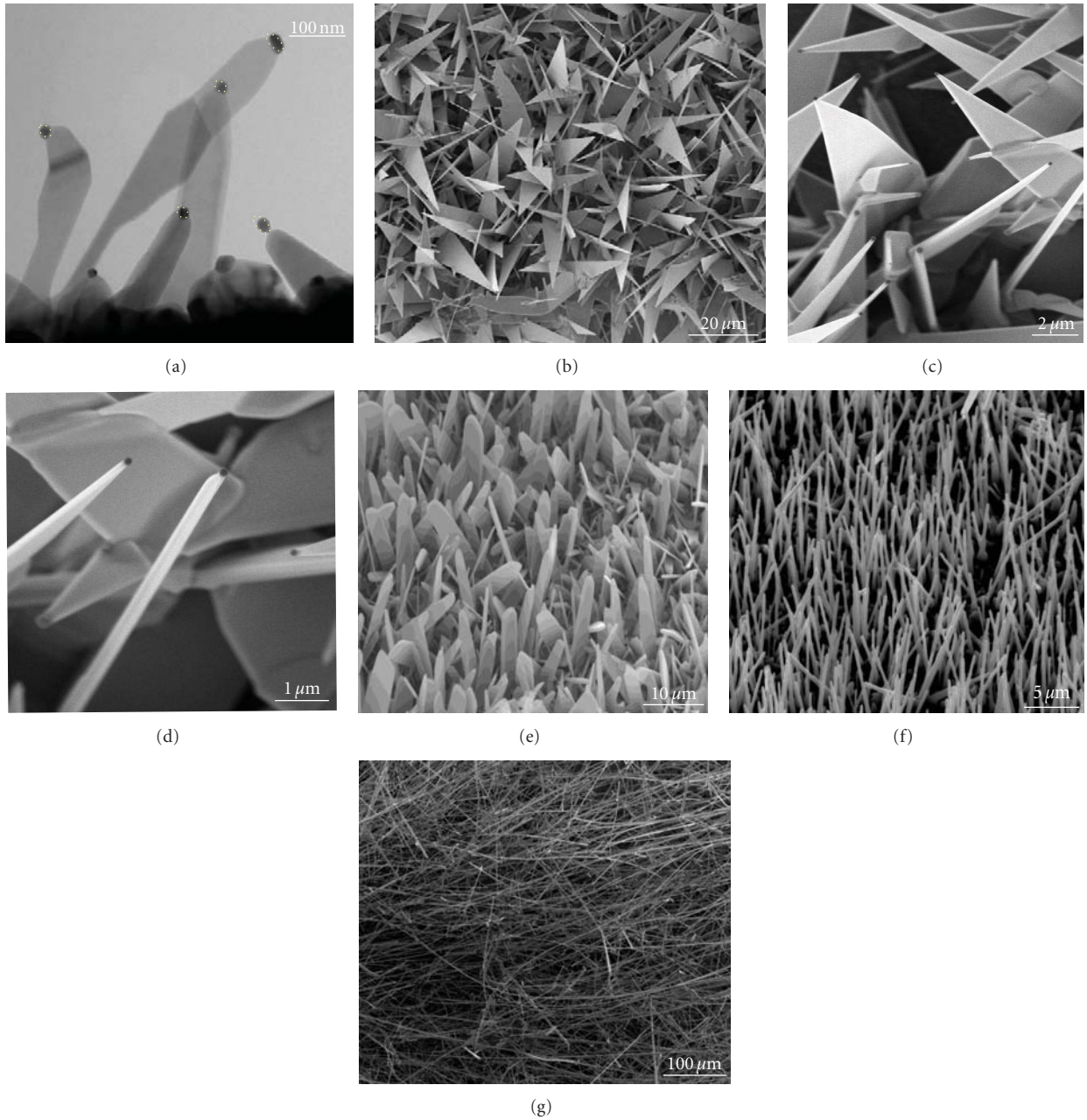

Figure 1: (a)–(d) show nanostructures grown by conventional VLS approach, (a) transmission electron microscope (TEM) image of ZnO nanorods with Au NPs on their heads (inside dotted circles); (b), (c), and (d) scanning electron microscopy (SEM) images ZnO nanoSails at different magnifications. The presence of Au NP on the top of nanoSail can be clearly seen in 1D (inside dotted circles). (e) and (f) show the structures grown by modified VLS approach [24] without any catalytic NPs: (e) ZnO nanomast structures, (f) ZnO nanorods, and (g) tin oxide nanowires.

An example on the smallest useful numbers of connections is with an average of 6-7 connections along the 200 μm wide contacts with an 8 μm gap. Estimating the statistics roughly from SEM analysis brings 80% of chips within a resistance variation of 25%. Doubling the contact length would bring 90% into 20% resistance variance. Longer contacts or higher wire densities further improve the statistic; however, a tradeoff has to be made between reliability and sensitivity, as the more the connections act in parallel the less sensitive the nanowire connection gets. Please see below an example of a UV sensor that shows the feasibility of the approach.

The advantage of MVLS approach over conventional VLS approach, however, is that the nanowires can be grown under ambient atmospheric conditions that one does not need special vacuum or gas environment specifications. Nanowires, for instance, have been directly grown on gold contact lines which were patterned on the 100 nm thick SiO_2-coated Si-chip. In contrast to the polycrystalline nature of the sputter deposited nanowires, the MVLS grown nanowires

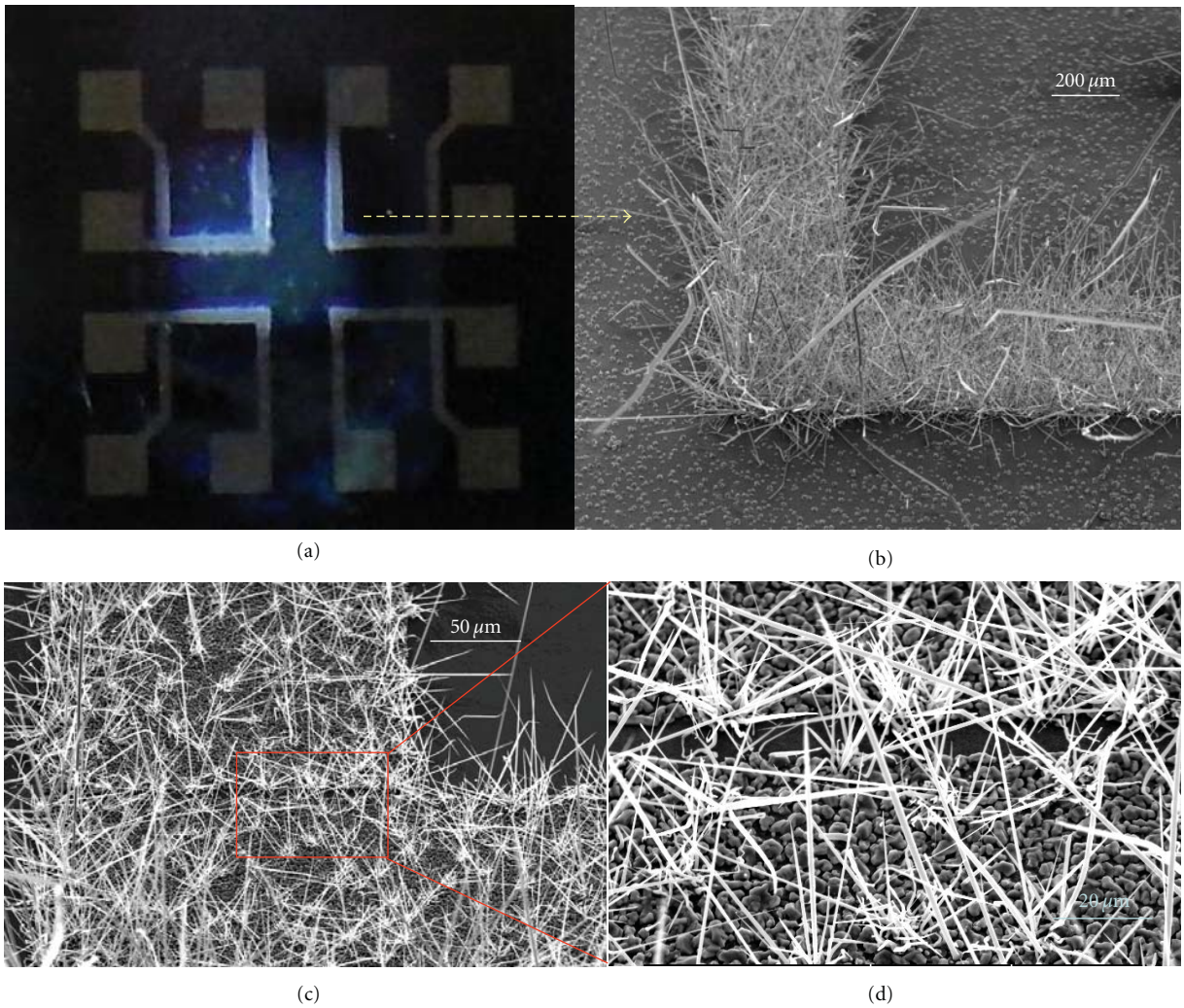

Figure 2: As-grown (a) optical image of 1D ZnO structures deposited area (white) where we have selective deposition around the 10 μm gap. SEM image (b) with high density ZnO nano- and microstructures, (c) relatively lower density networks on the contacts as well as within the 10 μm gap, and (d) magnified view of 10 μm gap part from (c) showing nanowires bridging between Au contact pads.

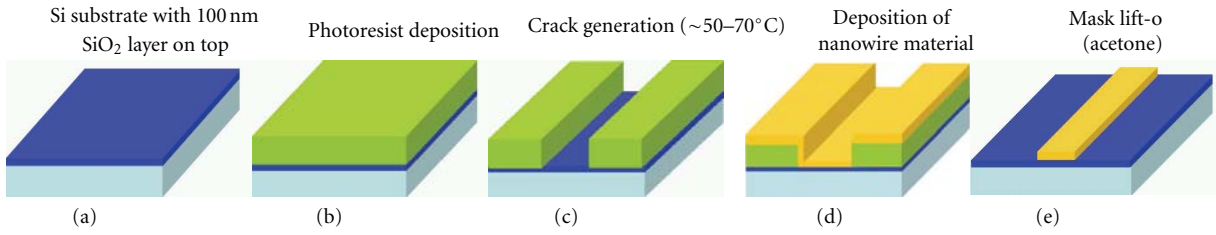

Figure 3: Schematic processes (a) to (e) involved in fabricating the nanowires by thin film fracture approach [12].

are exclusively single crystalline in nature with a variety of shapes which makes it similar to the conventional VLS. Many of oxide-forming materials such as Zn, Sn, Bi, and Fe have already been tested with MVLS approach, and the outcomes are very promising. Just for demonstration, growth of ZnO nanorods, at and between the 10 μm bridge between the gold contacts on the Si chip, is shown in Figure 2.

2.2. Fracture Approach. The main steps involved in thin film fracture (TFF) approach are described below in Figure 3. The photoresist is deposited (thickness varying from 550 nm to 1.5 μm) on the Si wafer which acts as a mask. The Si wafer with photoresist mask undergoes fracture (crack) formation process in which wafer is initially heated on the hot plate (~323 K to 348 K), and then it is subjected to quenching

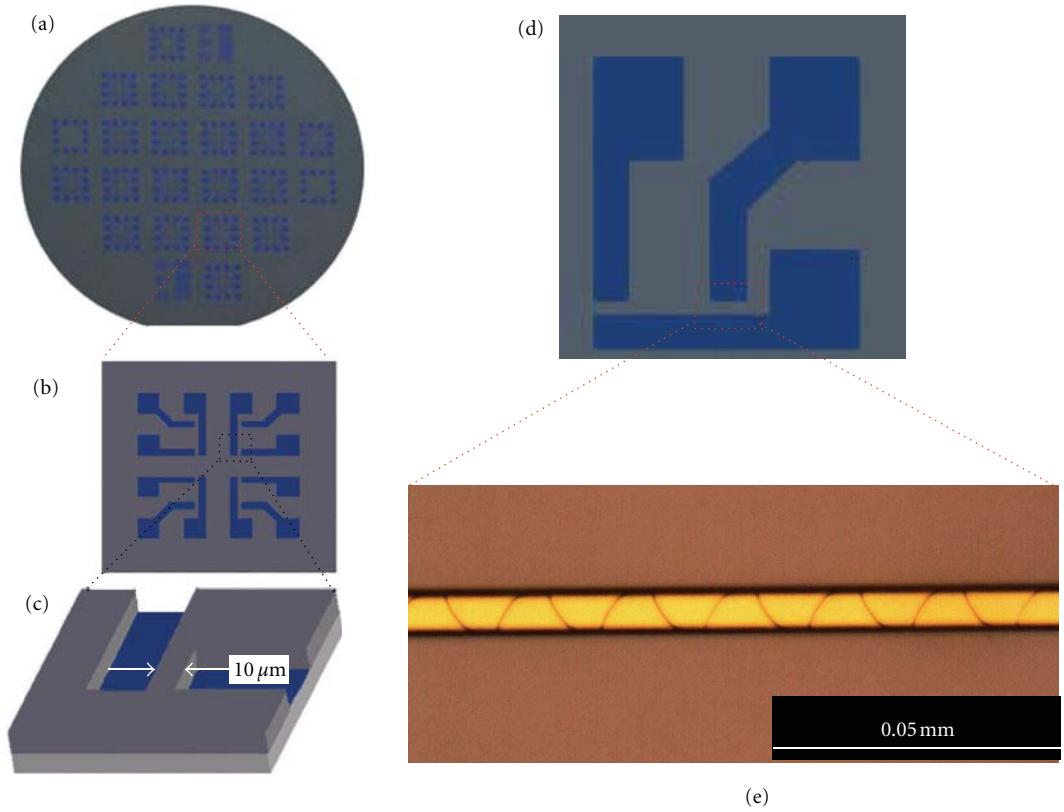

Figure 4: (a) Optical image of a microstructured photoresist film consisting of several microchips on a silicon wafer and a magnified view of a microchip. After UV lithography, each individual chip (b) consists of an open area for the later installed contact lines on the SiO_2 and a 10 μm wide rectangle of photoresist (c), where the nanowires will be installed. (d) Part of a chip cut from a chip design. (e) An optical micrograph of the 10 μm wide and 200 μm long photoresist after it is thermally fractured in liquid nitrogen—a periodic pattern of cracks occur. The cracks in (e) are observable optically as they are bended upwards because of the debonding of the resist from the substrate and causing it a delamination.

for about 5 seconds at cryogenic temperature (~77 K) using liquid nitrogen. As the result of difference in the coefficient of thermal expansion between the resist and the substrate, the drastic thermal shock creates fractures everywhere on the resist, but most importantly it creates well-patterned fractures on a 10 μm by 200 μm wide resist.

Following fracture formation is deposition. The material of interest as a nanowire is then deposited over the entire area of the wafer with fractured resist. A mask lift-off is then performed ultrasonically in acetone bath to lift the resist off the substrate. The undesired material covering to top of photoresist is also lifted off together with acetone leaving behind the nanowires of material within the cracks. The photoresists are mainly two types (i) positive and (ii) negative, and depending upon the requirement, a particular photoresist can be used. Till now we have successfully produced the desired cracks in controlled manner using positive photoresist; however, experiments about the utility of negative photoresist are under progress and will be published elsewhere. As already discussed above, the photoresist can be turned into a shadow mask after thin film cracks are produced in the microstructured photoresist. Depending on the dimensions of the photoresist on the substrate, different shapes of self-organized zig-zag cracks can be generated. In present case the cracks are formed in a rectangular strip of 10 μm width, 200 μm length, and ~700 nm height in the photoresist when the sample is quenched at cryogenic temperature (~77 K) after annealing the wafer to 55°C for 5 minutes. Figure 4 demonstrates a typical example of fractures formed in the 10 μm resist width on an Si wafer with TFF approach.

Commercially available Si wafer (~4 inch in diameter) was patterned by UV lithography and is shown as Figure 4(a). A magnified view of each pattern (1×1 cm^2) from Si wafer is depicted in Figures 4(b), 4(c), and 4(d) show the side view and the top view respectively from a magnified portion from Figure 3(b) where self-organized fractures are formed. Figure 4(e) is the optical micrograph image of cracks formed from fractured resist in a simple experiment.

The exact position of individual cracks can be precisely controlled, if they are confined by the lithographically produced microstructures. Depending on the thickness of the photoresist, cracks can propagate in straight line or follow curved paths or even some times lambda- (λ-) shaped cracks can be formed in the in lithographically confined position. The process has been performed at a wafer

Table 1: Summary of the TFF approach: Success statistics for a 10 μm sized gap width of resist. From approx.100 chips, 80 were fabricated with a 100% success rate at the optimized photoresist thickness between 850–1200 nm.

Thickness of photoresist	Crack formation (TFF approach)	Crack formation after oxygen plasma etching
≤550 nm	<50%	no
600 nm	>75%	no
650−850 nm	100%, straight and some times λ shaped	no
850–1200 nm	100%, bow shaped cracks	no
≥1200 nm	100%, bow shaped and strongly bended cracks, but delamination of the photoresist takes place	no

level, and the reproducibility has been proved for at least thousands of wafers. The formation of cracks with respect to the thickness of photoresist and influence of oxygen plasma treatment is summarized in Table 1. The treatment with oxygen plasma (ion) is a standard method to reduce the resist thickness. In this case it has a negative effect on the TFF approach, as it results in more branching in the polymer chains of the photoresist. This could enhance the crosslinking and entangling of the polymer chains which makes the bonds to be stiff for fracturing. Thus any oxygen plasma treatment will result in a more stiff photoresist which was the main reason to avoid the plasma etching of the resist as the final aim was to obtain fractures. It has been clearly observed that, when the thickness of photoresist is less than ∼550 nm, crack formation probability is less than 50%. With increase in thickness from 550 nm to 600 nm, the crack formation probability increases up to ∼75%. With photoresist thickness in the range of 650 nm to 850 nm, crack formation probability reaches maximum value. Individual cracks appear to be straight but the overall orientation of cracks being zig-zag. Some times λ-shaped cracks are also formed. It appears that critical value of photoresist thickness lies on average 750 nm as at this value, the crack formation probability is 100%, and with further increase in thickness beyond 750 nm crack probability is maximum and different shapes of cracks are formed. However, formation of crack disappears after plasma treatment (etching) for all thicknesses. If the width of the resist is other than 10 μm size, cracks of various shape and orientation could be the result.

As it has already been mentioned above that following the formation of cracks (fractures) is vacuum deposition of the nanowire material, both the electrode and the nanowire materials are deposited in single deposition process which makes this method easy and cost effective and also ensures a reliable contact between the nanowires and the electrodes. However, if it is necessary, with an additional deposition step, it is also possible to have different materials for contacts and nanowire structures. In this process step, the sample is tilted towards the deposition source. Due to the high aspect ratio of 8–10 of the fracture lines, no material penetrates to the bottom of the cracks, but the microstructure openings for the contact lines are filled with material. Subsequently a second nanowire-forming material can be deposited from top. The cracks which are employed here thus form an ideal shadow mask. Typically they have a width in the order of ∼100 nm and a depth all the way through the photoresist, resulting in aspect ratios of 5–10, depending on the used resist thickness. A resist film that is too thin does not allow a crack formation due to an insufficient amount of stress in the film during cooling, also a too thick film does not allow as it results in too much stress and a partial delamination of resist flakes. However, by changing the deposition angle, the width of the fabricated nanowires can be controlled independent of the crack width. Note that the height of the nanowire is below the nominal deposition thickness and below the height of the surrounding microstructures on the substrate as the steep walls of the resist masking already a part of the deposition source. After shadow mask liftoff in acetone bath, the electrode and the nanowire adhere to the substrate.

The nanowires produced by fracture approach using vacuum deposition are found to be polycrystalline with grainy features as shown in Figure 5. The inset in the figure shows grains of different size. This makes such kind of nanowires ideal for sensoric applications since the grain boundaries play crucial role in sensing. For instance, Favier et al. [28] have shown that palladium nanowires are excellent hydrogen sensors. The sensing quality originates from grainy structure of the nanowires which changes their electrical conductivity as a result of change in the nanogaps between the grains. The Pd nanowires were fabricated by the fracture approach which can also be used for hydrogen detection [29].

The fabrication of semiconductor nanowires demonstrated here follow either of two routes: (1) direct RF sputtering of semiconductor material or (2) sputtering of metal first followed by electrochemical anodization. One of the semiconductor candidates which was RF sputtered from a sputter target is ZnO. As deposited, both the ZnO film and/or NW sputtered at 40 Watt, 10^{-6} mbar chamber pressure, showed electrically insulating behaviour. However, after annealing the prepared nanowire samples above 400°C for about 1 hour in normal ambient, they showed electrical conductance which is a clear indication of microstructural change. The correlation between annealing conditions and the physical structure of the films (crystalline structure and microstructure) was investigated by X-ray diffraction (XRD) and atomic force microscopy (AFM). The XRD results on the annealed film showed that *c*-axis preferred orientation which is preferred growth direction of ZnO because of its hexagonal wurtzite crystal structure.

Sputtering of low layer thickness or small amount of semiconductors like ZnO is believed to come up with columnar Volmer Weber-type of growth or separate islands. The AFM image given in Figure 6(a) shows that the as-deposited ZnO film is quite rough which one possibly compares to the schematic in Figure 6(c) with a columnar microstructural growth with possible spacing among columns. Postdeposition annealing has resulted in remarkable changes in the microstructure as shown in Figure 6(b), and the film has been found to be dense and smooth beside a few larger tips and electrically conductive for which the

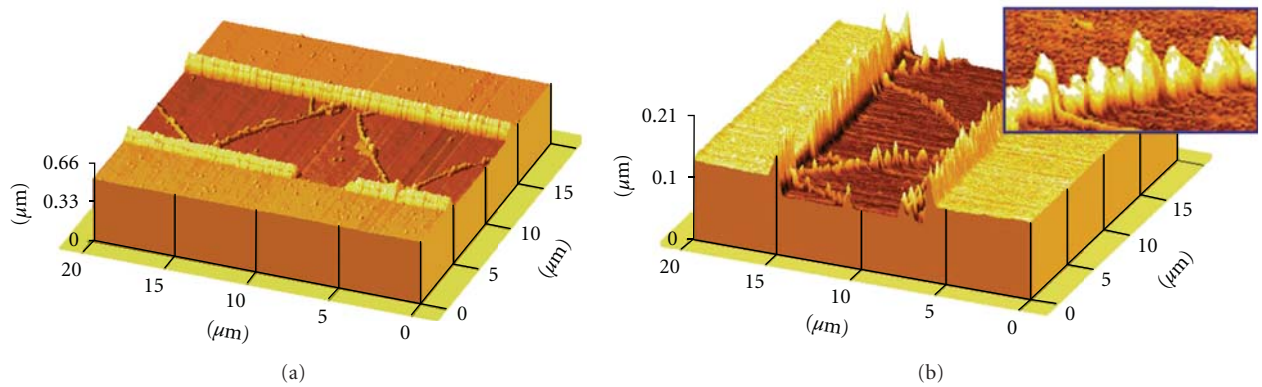

FIGURE 5: AFM Image of zig-zag-oriented (a) Ti nanowire and (b) Pd nanowire. The inset in (b) illustrates grainy features of the nanowires. Note that the z-scale is drastically overemphasized.

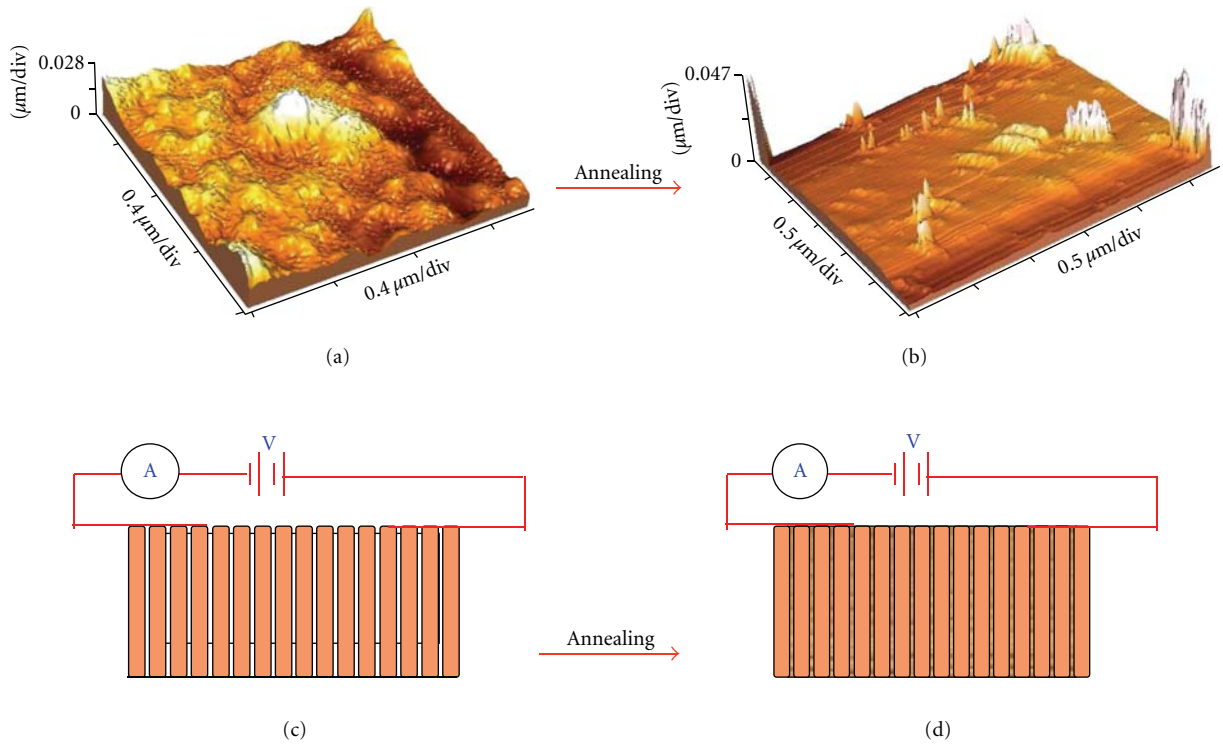

FIGURE 6: (a) AFM images of as deposited 50 nm ZnO thin film, (b) annealed at 400°C for 1 hour. Schematic views of ZnO thin film before (c) and after annealing (d).

microstructure cross-sectional view might be compared with Figure 6(d). Similar results were also reported by Chu et al. [30], although our samples were annealed under ambient atmosphere condition. The observed electrical conductivity is thus believed to come from islands interconnections which occur after post deposition annealing (the measured electrical conductivity curves before and after annealing of nanowires are shown in the discussion part in Figure 8(a)).

The other route for the fabrication of oxide semiconductor nanowire structures is to start from a metal nanowire followed by electrochemical anodization. Thin film fracture approach has also been used here for fabricating the nanowire. After fabrication of a networked crack structure, 70 nm thick Ti was deposited where the nanowires are located on a 100 nm SiO_2 and are anodized with 10 V for 10 minutes. The I-V characteristics before and after anodization are demonstrated in Figure 7.

From the linear I-V response, it can be observed that the resistance is increased from 0.076 MΩ to 217 MΩ after anodization, which is close to the resistance regime where electron tunneling can possibly be involved. The anodized nanowires exhibit several types of electrical conductivities,

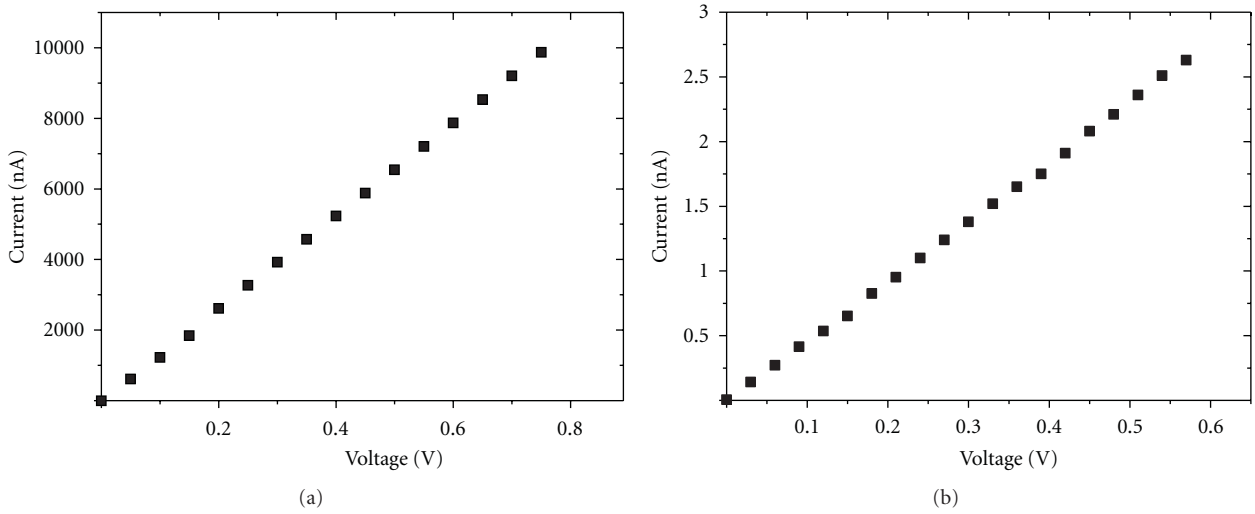

Figure 7: *I-V* characteristics (a) before anodization and (b) after anodization. The resistance increases from 0.076 MΩ to 217 MΩ.

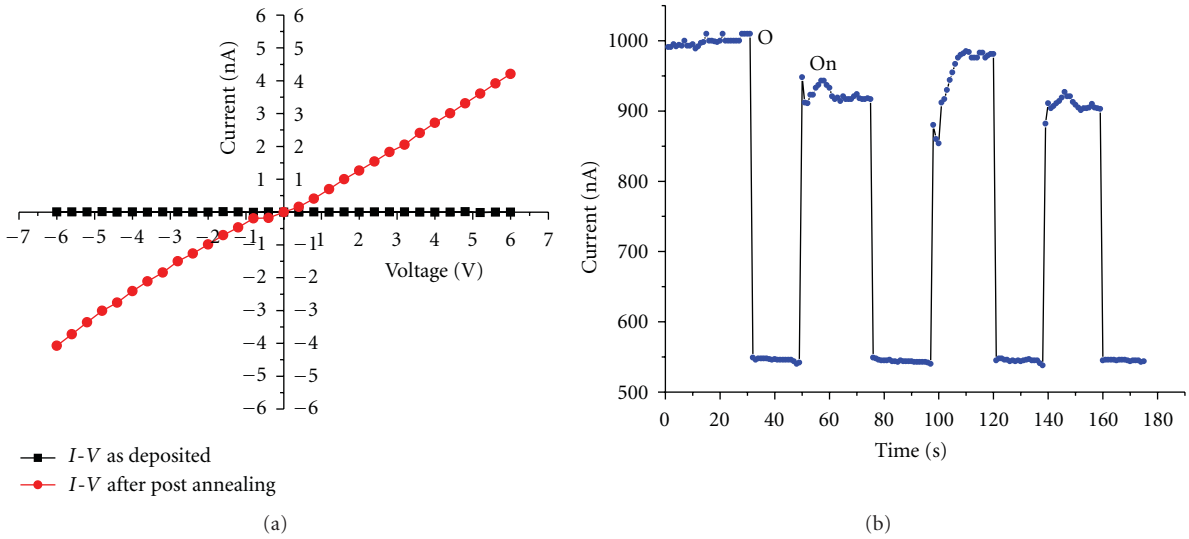

Figure 8: (a) Electrical conductivity of as-deposited and annealed (at 400°C-1 hr in air) 50 nm thick ZnO NW. (b) Current-time switching cycles curve at constant voltage of 2 V under UV illumination.

and the explanation for possible mechanisms or reasons for these variations are discussed in details in our previous paper [31].

3. Results and Discussion

Mainly we have demonstrated the fabrication and growth of metal and semiconductor nanowires by conventional and modified VLS approaches as well as by a thin film fracture approach here. The main intention was to integrate these nanowires on the chip with gold contacts for direct applications in electronic devices or sensor measurements. In the following section, we demonstrate the electronic characteristics of ZnO nanowires, anodized Ti nanowire field-effect transistors (NWFET), and sensor applications.

3.1. UV Photoresponse of the ZnO Nanowires. The UV photodetection of the ZnO nanostructures fabricated under the two approaches [12, 24] was measured under ambient condition (shown in Figure 8). The ZnO nanowires showed reversibly and rapidly switching of conductivity states. As the measurement was performed under open air condition, oxygen is adsorbed on the ZnO surface. Upon illumination with 365 nm UV lamp, the conductivity has increased as it is evidenced by the current versus time characteristics at a constant voltage supply.

Photons of energy greater than the bandgap will generate electron-hole pairs. According to Soci et al. the photogenerated holes migrate to the surface and are trapped, leaving behind unpaired electrons in the NW that contribute to the photocurrent [32]. The normal *I-V* responses and current

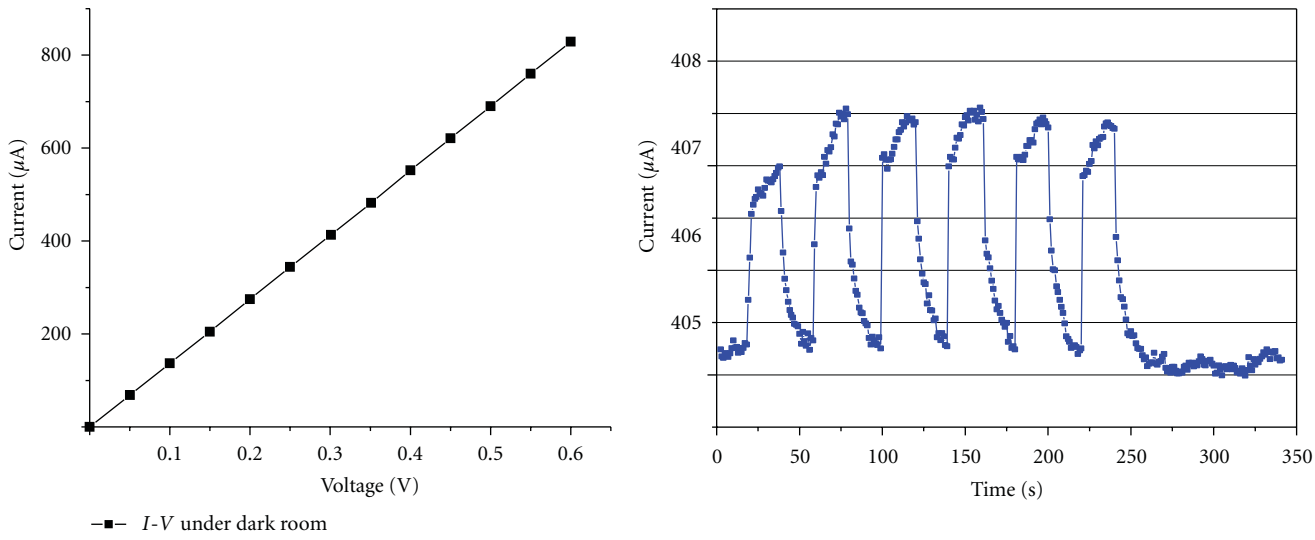

Figure 9: I-V characteristics of ZnO nanowires on chip fabricated by MVLS approach in dark (a) and the corresponding current-time switching response (b) under UV light illumination at constant voltage of 0.3 V.

switching in the ZnO nanowires synthesized by fracture and MVLS method are demonstrated in Figures 8 and 9, respectively. The holes then neutralize the chemisorbed oxygen resulting in increasing the conductivity as shown in Figures 8(b) and 9(b). When the UV light is turned on and off, the increase or decrease in photocurrent takes a time to reach to the saturation. This phenomenon is less pronounced in the case of nanowires produced under fracture approach as shown in Figure 8(b).

The photoresponse of the ZnO nanowires grown in fracture approach under 2 V applied voltage and up on illumination in Figure 8(b) shows the photoresponse is much faster than that of measured for ZnO micro- nano wires grown by modified VLS counterpart as shown in Figure 9(b). The reason would likely be the reduced influence of the surface states seen in that material in the case of modified VLS (MVLS) approach. Because we have got a combination of high-density nanowire networks connected in the MVLS approach in which the surface to volume would be smaller as compared to the fracture approach. Similar results have been reported by Pearton et al. [33].

3.2. Gas Response of the Anodized Titanium Nanowire FET. Before applying a gate bias voltage, the insulating behavior of the back gate was checked by connecting one electrode to gate (P^{++} Si) and the other electrode to drain and ramp voltage from 0 to 3 volts. The applied gate voltage was limited to 3 volts in order to avoid the breaking of the dielectric property of the oxide layer in the nanowire chip. Again in order to be sure that there is no leakage current through oxide, current measurements at several places on the oxide layer were performed, and almost zero leakage current was observed every time. However, there were positions where we observed a resistance in the order of 300 MΩ which might be due to the inhomogeneities in oxide layer thickness (thermally grown oxide layer supplied by Active Business Company GmbH, Munich). Those positions on the chip are excluded from further measurements. A bottom gate voltage was applied for the anodized Ti nanowire, and corresponding curves are shown in Figure 10(a). As the plot (Figure 10(a)) depicts, there is a high increase in source-drain (I_{sd}) current when a bottom gate-source voltage is applied (V_{gs}). In order to show the almost symmetric nature of current behavior in both forward and reverse directions, we have shown a magnified plot in Figure 10(b) corresponding to zero gate-source bias voltage. To demonstrate the increase in current due to applied gate bias, the logarithmic plots corresponding to Figure 10(a) are shown in Figure 10(c) which reveal that drain current is increased by more than two orders of magnitude. The increase in drain current indicates that the nanowires are n-type [34] as the conductance has increased by depleting electrons from the oxide. The transfer characteristics of the anodized Ti nanowire corresponding to different source-drain voltages are shown in Figure 10(d).

The observed field effect behavior might be used to shift the nanowire-operated devices, for example, as sensor, into a sensitive region of its conductivity curve. The TiO_2 nanowire FET, however, showed a drastic and fast response in the drain current when it is exposed to different pressures of oxygen (Figure 11). The reduction in drain current under the exposure of oxygen is believed to be the result of adsorption of O_2 at oxygen vacancy sites forming O_2^- and O^- through depleting electron from titania.

The FETs exhibit properties which are already suitable for applications as sensors. Thus the gas detection experiments were performed with nanowires synthesized with the help of the fracture approach. For comparison, Pd nanowires showed a drastic change in the conductance when exposed to H_2, but the anodized Ti nanowires showed no change in the conductance when the nanowires are exposed to

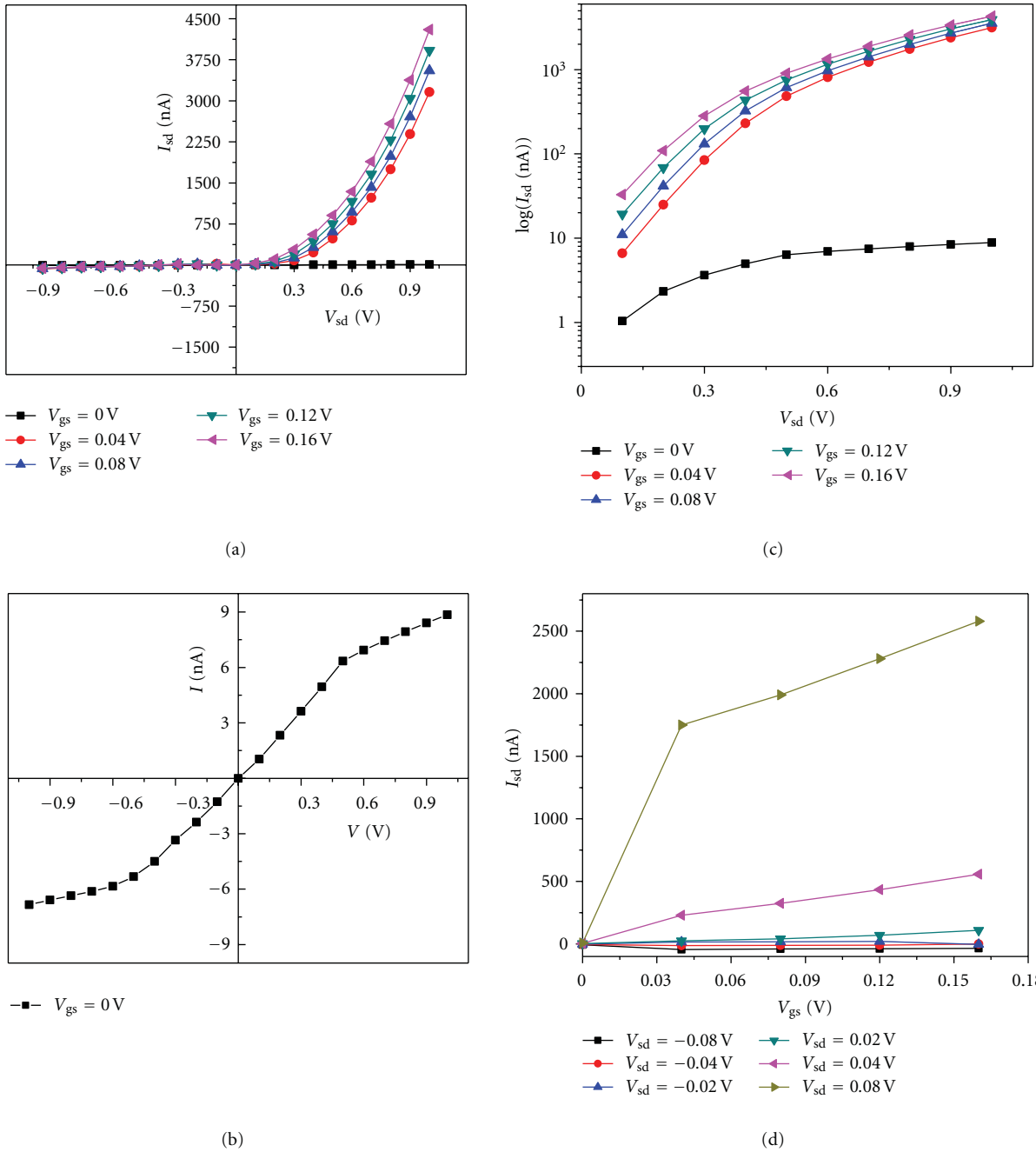

Figure 10: (a) I_{sd}-V_{sd} characteristic of anodized Ti nanowires as a NWFET, (b) the magnified I_{sd}-V_{sd} plot for zero gate voltage in forward and reverse bias, (c) logarithmic plot corresponding to (a), (d) transfer characteristics of nanowire-FET at different source drain voltages (V_{sd}).

H_2. The FETs produced possess properties already suitable for applications as sensors. In this context the gas-sensing capabilities of Pd and anodized Ti nanowires synthesized under fracture approach were also tested which are shown in Figure 12. Pd nanowires showed a drastic change in the conductance when exposed to H_2, but the TiO_2 nanowires showed no change in the conductance when the nanowires are exposed to H_2 as shown in Figures 12(a) and 12(b), respectively.

4. Conclusions

We have demonstrated two different routes for the micro-nano integration of metal oxide semiconducting nanostructures into Si microchips. Both routes allow the integration of nanowires and are in principle ready for upscaling; however, they both are best with individual advantages and disadvantages. The modified VLS type of growth on already existing current lines requires relatively high temperatures

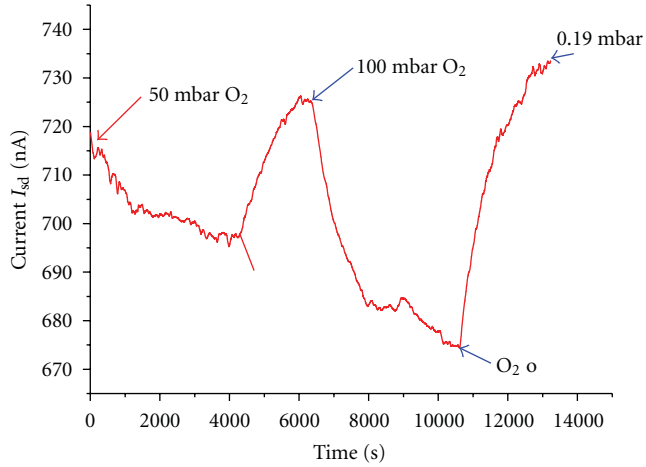

Figure 11: Sensing response of anodized Ti NWFET at different partial pressures of oxygen. A pronounced answer is visible.

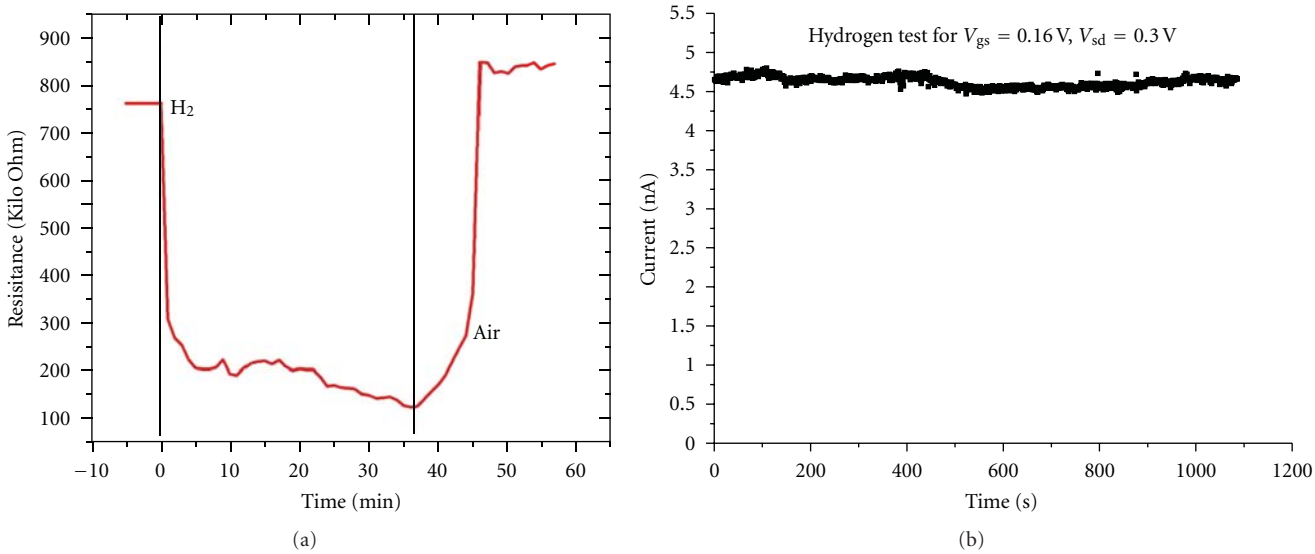

Figure 12: Comparison of sensor properties at H_2 containing atmospheric environments. (a) Palladium nanowire as hydrogen sensor, comparison [29], shows a pronounced answer in terms of increased conductivity. (b) The anodized Ti nanowire FET shows no response to hydrogen.

and therefore need an active cooling of the wafer during fabrication if circuit elements are already structured. On the other hand the approach allows an integration of a 3D network type of structure which might be interesting for sensors that are in touch with a medium like fluid or gas sensors, a housing could allow direct accesses of the media to the network but shield the rest of the electronics. First tests with ZnO nanowires and UV-light show a delayed response of the single crystalline nanowires compared with the polycrystalline nanowires fabricated with the fracture approach, probably due to the larger surface-to-volume ratio of the sputter deposited ZnO wires. The fracture approach allows a simpler integration; it requires only one additional step for the photoresist preparation. However, a simple straight forward sputter deposition can be insufficient to achieve a desired nanowire formation—; or example, experiments with the deposition of ZnO teach that a postannealing step must be carried out in order to obtain a nanowire of interconnected grains. Alternative heating can be avoided by depositing a metal first and carrying out an anodization to turn the metal into an oxide nanowire. The example of anodized Ti nanowires fabricated in this way allows the formation of a bottom gate field-effect transistor. Furthermore, the anodized titanium can serve as oxygen-sensitive element; it has already a selectivity towards hydrogen. In summary, several integration routes for nanowires are possible that can be carried out with standard processes and without E-beam lithography, focused

ion beam methods, or alignment processes for already prepared nanowires that are unlikely to allow a wafer level processing. For a final demonstration of the feasibility of the here suggested methods, a wafer-level processing should be carried out. The first tests of sensitivity are promising to allow the nanowires to serve in sensors; however, for a nanowire sensor a control electronics should be integrated, for example, for sensor drift correction and selectivity, as well as long-term stability tests have to be carried out.

Acknowledgments

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Review Article

Self-Organized One-Dimensional TiO_2 Nanotube/Nanowire Array Films for Use in Excitonic Solar Cells: A Review

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We review the use of self-assembled, vertically oriented one-dimensional (1D) titania nanowire and nanotube geometries in several third-generation excitonic solar cell designs including those based upon bulk heterojunction, ordered heterojunction, Förster resonance energy transfer (FRET), and liquid-junction dye-sensitized solar cells (DSSCs).

1. Introduction

Third-generation photovoltaics encompass a variety of designs including liquid-based dye-sensitized (Grätzel) solar cells, solid-state bulk heterojunction solar cells [1–6], ordered heterojunction solar cells [7, 8], Förster resonance energy transfer- (FRET-) based solar cells [9–14], and organic solar cells [15, 16]. Liquid-based dye-sensitized solar cells (DSSCs) utilizing for a photoanode a dye-coated layer of TiO_2 nanoparticles have reached efficiencies of over 11% [17], but there are concerns with respect to manufacturing photovoltaic panels with a liquid redox electrolyte. Solid-state organic solar cells are easy to handle and manufacture, and have demonstrated efficiencies ranging from 2 to 8.13% [18–20]. Other 3rd generation photovoltaic designs include plasmonic resonance devices [21], quantum dot and, hopefully, multiple exciton devices [22, 23].

Various nanostructures have been used as a means of energy conversion enhancement in 3rd generation solar cells. These structures can be classified into four types: (a) Nanocomposite (3-dimensional), (b) quantum well (2-dimensional), (c) nanowire and nanotubes (1-dimensional, 1D), and (d) nanoparticles (0-dimensional). Our interest in this paper is the photovoltaic application of self-assembled TiO_2-based 1D nanostructures. Self-organized TiO_2 nanowires/nanotubes arrays [24, 25] vertically oriented on a transparent conducting oxide (TCO) substrate offer numerous benefits such as large surface area for dye sensitization resulting in enhanced light harvesting, easy transfer of electrons injected from photon excited dye, vectorial (directed) charge transport to the electrical contact, and a readily assessable space for intercalation of the redox electrolyte or p-type semiconductor. However, while self-assembled vertically oriented 1D titania nanoarchitectured films offer great potential for enhancing 3rd generation photovoltaic efficiencies to date, such films have not yet been achieved. There is, to date, something always lacking in such fields, be it poor crystallinity of the electron transporting backbone which results in poor charge transport, damage to the transparent conductive oxide coating which increases the series resistance and/or reduces film transmission, or low surface area which limits the amount of light that can be absorbed.

Promising self-assembled 1D titania architectures are films comprised of vertically oriented nanotubes or nanowires. TiO_2 nanotube arrays, on fluorine doped tin oxide-(FTO-) coated glass, of desired pore size and length can be achieved by anodic oxidation [26, 27], while vertically aligned TiO_2 nanowire films can be achieved via a hydrothermal process [24, 25, 28, 29]. The length and pore size of the nanotube arrays can be easily controlled by choosing a suitable anodization electrolyte, that is, choice of organic solvent with appropriate concentration of fluoride

ions and conductivity modifying additives—if so desired, as well as the anodization voltage range. The spacing between the nanotubes is found to vary with the type of organic solvent used. Speaking generally, ethylene glycol, for example, results in close-packed nanotube arrays [30], diethylene glycol enables broad control over the tube-to-tube spacing [31], dimethyl sulfoxide yields a two-layer structure where nanotubes are densely packed towards the substrate and well-separated nanotubes in the upper region [32], and the use of formamide results in well-separated nanotubes along the entire tube length [33, 34]. While fabrication of nanotube arrays on FTO-coated glass is not simplistic [35], TiO_2 nanotube arrays up to 53 μm in length have been achieved on FTO-coated glass.

As-anodized nanotubes are amorphous, crystallized by annealing in oxygen at elevated temperatures [36]. TiO_2 nanotubes arrays grown on FTO glass need to be annealed at relatively lower temperatures, no more than $\approx$470°C, to minimize damage to the FTO layer [35]. Annealing above this temperature promotes, we believe, diffusion of the residual Ti into the FTO layer and fluorine into the TiO_2 layer, with a corresponding loss in electrical conductivity. The walls of crystallized nanotubes are anatase, while any residual Ti layer underneath the nanotubes will convert to rutile [36].

Another approach to achieving self-assembled vertically oriented 1D TiO_2 nanostructured films, in this case nanowires, is by hydrothermal synthesis [25]. The self-assembled hydrothermally grown nanowires are of a highly crystalline rutile structure with preferred [001] orientation [25]. In comparison to rutile, use of anatase in DSSCs results in a higher photovoltage due to the higher conduction band level of anatase. Further, for equal degrees of crystallization, the charge transport properties of anatase are generally superior to those of rutile. Nanowire length is increased by the use of extended hydrothermal reaction times, but extended reaction times may also result in a thicker oxide layer at the nanowire base. Shorter nanowires have relatively wider wire-to-wire spacing; however, for a fixed wire length it is difficult to change the wire-to-wire spacing.

To date self-assembled 1D nanostructured titania films have yet to revolutionize third-generation photovoltaics; however, there remains hope that they yet may do so if synthesis techniques can be developed whereby single crystal films of such vertically oriented 1D structures, of extended length for enhanced light absorption, can be obtained without damage to the underlying transparent conductive layer to minimize series resistance. To that end, we consider herein our recent work on the synthesis of 1D nanostructured titania films and their photovoltaic application.

2. Fabrication of 1D Nanostructures

2.1. Transparent Films of TiO_2 Nanotube Arrays. As reported by Varghese and coworkers, there were three major challenges in the fabrication of transparent nanotube array films of extended length possessing high optical transparency and superior electrical properties as needed for application in achieving efficient dye-sensitized solar cells [35]. These were (i) formation of uniform titanium films tens of microns thick on FTO glass with sufficient adhesion to the FTO layer to withstand stresses associated with the anodization process and the different thermal and surface treatments inherent to DSSC fabrication; (ii) anodization of these thick titanium films until achieving uniform optical transparency; (iii) fabrication of TiO_2 nanotubes of great length using fluorine-containing nonaqueous organic anodization electrolytes without debris formation or clumping of the nanotubes [27].

Titanium films were deposited on FTO glass substrates, having sheet resistances of 15 Ω/square and 8 Ω/square, using radio frequency (RF) or direct current (DC) magnetron sputtering of titanium targets [35]. Film deposition was carried out at 5 mTorr in argon, with power densities of 6.34–7.92 W/cm^2 for RF and 4.3–5.66 W/cm^2 for DC sputtering. An RF source was connected to the substrate holder and negative DC self-bias voltages of 130 V and 160 V applied at the substrate for bombarding the growing films with positive argon ions for films of thickness below and above 2 μm, respectively. For films of thickness >3 μm, a second layer of thickness 0.5–0.8 μm was deposited across the top edge of the first layer, through use of a mask, to avoid complete etching of the film at the air-electrolyte interface during anodization. During deposition of the primary metal layer, the substrate was initially heated to about 45–60°C at which time the DC self-bias voltage was increased to about 210 V. No external heating was applied for depositing Ti films of thickness less than about 3 μm. Deposition rates up to 5.4 nm/minute were used. High optical reflectance (>55%) of the metal film was found to be a prerequisite for obtaining distinct-ordered nanotubes, indicating that the starting metal films should be dense and have a surface roughness limited to the nanometer regime.

TiO_2 nanotube arrays were formed by anodizing the Ti/FTO films, at constant voltage, in a two-electrode electrochemical cell with the titanium film as the anode and a platinum foil cathode. Dimethyl sulfoxide (DMSO) or ethylene glycol (EG) electrolytes containing with 2–4 vol% HF and 0–4 vol% water were used. Anodization was performed until the oxide nanotube growth fully consumed the titanium, across the entire thickness, and the film became transparent. The formation of debris, and increase in nanotube length beyond the metal film thickness in fluoride-based organic electrolytes is related to the low conductivity of the electrolyte. The conductivity of an electrolyte composed of hydrofluoric acid (HF) and DMSO, originally low, was enhanced by applying an electric field between two immersed electrodes (60 V between titanium and platinum electrodes). For obtaining debris-free short nanotubes, Ti anodization was done in an electrolyte of high electrical conductivity ($\sim$1000 μS/cm), whereas for longer nanotubes the electrolyte conductivity was low ($\sim$100 μS/cm). Voltages from 8 to 30 V (for the pore size 27 nm to 100 nm) were used for anodizing titanium films of thickness around 1 μm, whereas from 15 to 30 V were used for higher thickness Ti films for obtaining desired pore size and length. Anodization duration was 21–27 hours (at 30 V) for films comprising 20 μm long nanotubes. Transparent nanotube films from 0.3 μm to 33 μm in length were obtained from metal films of thickness up to

20 μm [35]. A field emission scanning electron microscope (FESEM) image of a TiO_2 film consisting of 20 μm long nanotubes is shown in Figure 1, reprinted with permission from [35]. The as-prepared films were annealed in an oxygen environment for crystallization, as well as for oxidizing any residual metal. The films were annealed in oxygen at temperatures ranging from 400°C to 530°C depending upon nanotube length; 1 μm thick films were annealed at 400°C for 6 h, and 20 μm films were kept at 400°C for 4 h and then at 530°C for 2 h. The high transmittance and low total reflectance of a 0.8 μm long nanotube film serves as an antireflection coating enhancing the transmittance by more than 5%, and decreasing the reflectance by about 6%. Even for a 17 μm thick nanotube film (on TEC 8), there is still significant transmittance in the red region. Prior to DSSC use, the films were immersed in 0.02 to 0.05 M $TiCl_4$ aqueous solution for 6–12 h, then rinsed with ethanol and distilled water, dried in air, and annealed at 450°C for 30 min in oxygen.

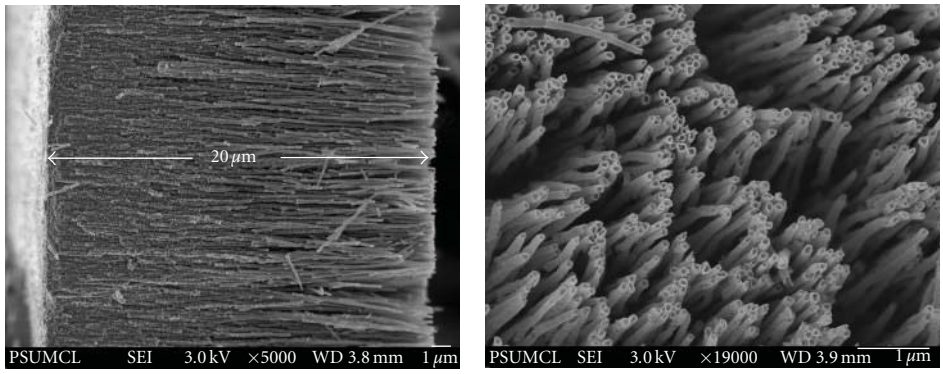
2.2. Transparent TiO_2 Nanowire Array Films. Feng et al. first reported the synthesis route for the fabrication of highly aligned, vertically oriented, densely packed, and highly crystalline nanowire arrays on FTO-coated glass [24]. The synthetic process was performed at relatively low temperatures, below 180°C, without affecting the FTO layer conductivity. Before growing the TiO_2 nanowire arrays, a compact TiO_2 layer 20 nm thick was grown by treating the FTO glass with 0.2 M $TiCl_4$ aqueous solution for 12 h and subsequently heating in air at 500°C for 30 min. These $TiCl_4$-treated FTO glasses were then placed within a sealed Teflon reactor (volume size ~23 mL) containing 10 mL of toluene, 1 mL of tetrabutyl titanate, 1 mL of 1.0 M titanium tetrachloride (in toluene), and 1 mL of hydrochloric acid (37 wt%) [24]. Nanowire array synthesis was achieved using toluene as the nonpolar solvent and toluene-soluble tetrabutyl titanate and titanium tetrachloride as a precursor. With an increase in temperature, Ti^{4+} precursors hydrolyze with water at the water/TiO_2 or FTO interface, resulting in the formation of a crystal nucleus on the substrate. After formation of the first nanocrystalline layer, a new interface forms between hydrophilic TiO_2 and toluene with continuous hydrolysis and subsequent growth-crystallization. A reaction temperature of 180°C was used with reaction times lasting from 30 min to 48 h. Nanowire growth was found to slow with time; for example, a 2 h reaction resulted in 2.1 μm long nanowires, a 4 h reaction leads to 3.2 μm long nanowires, 8 h to 3.8 μm, and 22 h to 4 μm; no increase in nanowire length was achieved for reaction times beyond 22 h. After the reaction period, the nanowire samples were removed, washed with ethanol, and then dried in air. The top and cross-sectional FESEM views of as-synthesized TiO_2 nanowire films, shown in Figures 2(a) and 2(b), reprinted with permission from [24], display a densely packed array of nanowires grown almost perpendicularly on FTO-glass. The nanowires were classified as tetragonal rutile with an enhanced (002) peak [24].

The interwire distance is a key parameter influencing the performance of hybrid photovoltaic cells. If the wires are too densely packed with small interwire separation, the bulky polymeric chains cannot percolate the full sample depth. At the same time, the nanowire separation should not be too great otherwise excitons generated in the interwire regions will recombine before being split at an available polymer-TiO_2 heterojunction. To form well-separated relatively short TiO_2 nanowire arrays, TiO_2 seed layer-coated FTO glass substrates were loaded into a sealed Teflon reactor (volume size ~23 mL) containing 10 mL toluene, 1 mL 1.0 M titanium tetrachloride (in toluene), 0.3 mL tetrabutyl titanate, and 1 mL hydrochloride acid (37 wt%), kept at 180°C for 8 h. Figures 2(c) and 2(d) show FE-SEM top and cross-sectional views of a typical as-synthesized nanowire array sample exhibiting vertically oriented nanowires of length ~600 nm, diameter ~15–35 nm, and interwire spacing ~30–50 nm. As per X-ray diffraction pattern analysis, these nanowires crystallized as tetragonal rutile with a preferred [001] crystal plane orientation.

3. Use of 1D Nanomaterials in Bulk Heterojunction, Ordered Heterojunction, and FRET-Type Solid and Liquid-Junction DSSCs

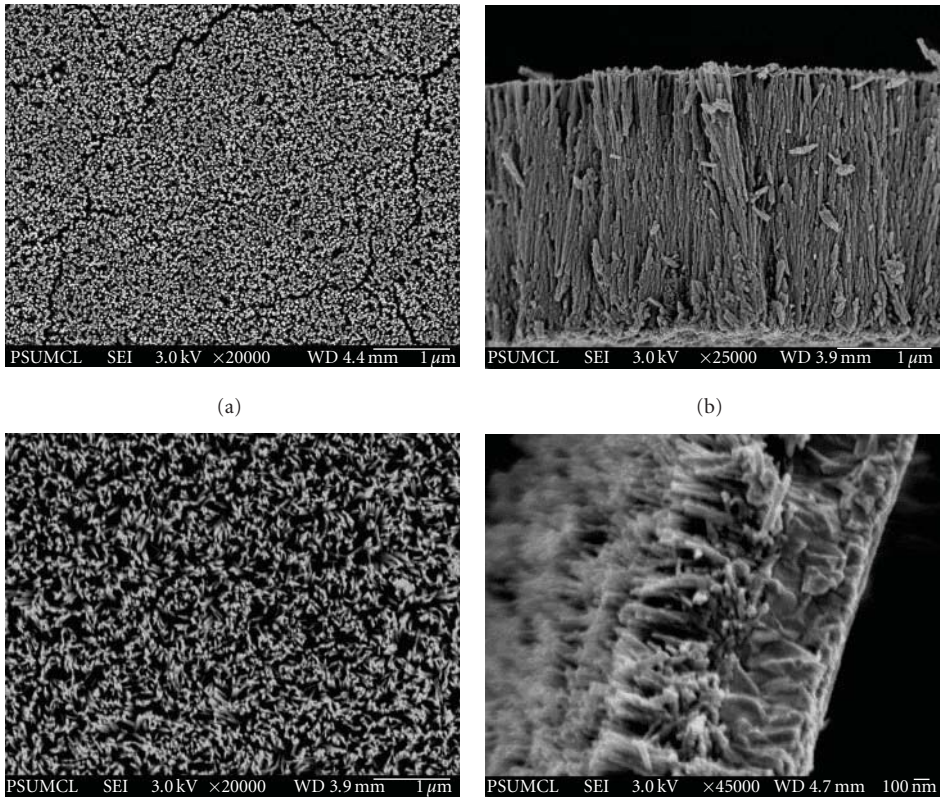
3.1. Bulk Heterojunction Solar Cell. Ideally the donor and acceptor phases within a bulk heterojunction are interspaced with an average length scale of around 10–20 nm, equal to or less than the exciton diffusion length, to ensure high mobility charge carrier transport with reduced recombination [39]. Such a precise nanostructure within polymer mixtures is difficult to achieve. However, self-organization of organic semiconducting polymers can be induced by use of diblock copolymers resulting in self-organized phases [40–42], liquid crystalline self-organizing columns of donor acceptor phases [43], and inorganic oxide nanotube or nanotemplate filled with organic semiconductors [38, 44–47]. Herein we emphasize the use of vertically oriented TiO_2 nanotube/nanowires for use with polymers as appropriate towards solid-state solar application.

Our initial design approach attempted to combine ordered 1D architectures for collecting electrons from PCBM molecules generated upon exciton dissociation at the P3HT/PCBM interface, and bulk heterojunctions present in a polymer/organic molecule blend [38]. A schematic of our device configuration is shown in Figure 3(a), with the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) energies of the component materials (P3HT/PCBM blend, PEDOT:PSS) with respect to the TiO_2 conduction and valence bands, and electrode (FTO and gold) work function, displayed in Figure 3(b). The length and pore size of TiO_2 nanotube arrays used were 270 nm and 50 nm, respectively. The polymer used was a blend of an electron donor P3HT and an electron acceptor $PC_{70}BM$; a 10 mg/mL solution of P3HT in chlorobenzene and 8 mg/mL solution of PCBM in chlorobenzene were mixed in a 1 : 1 ratio using the procedure outlined by Kim et al. [48] and infiltrated into the nanotubes. Subsequently, a PEDOT:PSS layer was deposited by spin coating an aqueous suspension of the polymer at 5000 rpm. The samples were then placed



(a) (b)

Figure 1: (a) FESEM image of a 20 μm long TiO_2 nanotube array (pore size 95 nm and wall thickness ~10 nm) on FTO-coated glass and (b) top view of the nanotubes. Reprinted with permission from [35].



(a) (b)

(c) (d)

Figure 2: (a) Top and (b) cross-sectional FESEM images of vertically oriented self-organized rutile TiO_2 nanowire array grown on FTO coated glass at 180°C for 24 h. Reprinted with permission from [24]. (c) Top-view and (d) cross-sectional FESEM image of short rutile TiO_2 nanowire arrays.

on a hot plate at 170°C for 15 min to remove any residual water and to promote intercalation of the polymer into the TiO_2 nanotube arrays. All spin coating and baking steps were carried out in a nitrogen glove box. A 50 nm film of gold was evaporated onto the devices though a shadow mask to form the top contact.

Charge separation occurs at the TiO_2/P3HT and PCBM/P3HT interfaces. The barrier layer of compact TiO_2 prevents holes in the polymer from reaching the transparent conductive oxide. A key advantage of the TiO_2 nanotube array electron-accepting network is that it prevents the electron-donating material (P3HT) and electron-accepting materials (TiO_2 and PCBM) from both being in contact with anode and cathode of the solar cell at the same time, as is the case with the conventional bulk heterojunction device geometry. The J-V characteristics of the fabricated TiO_2

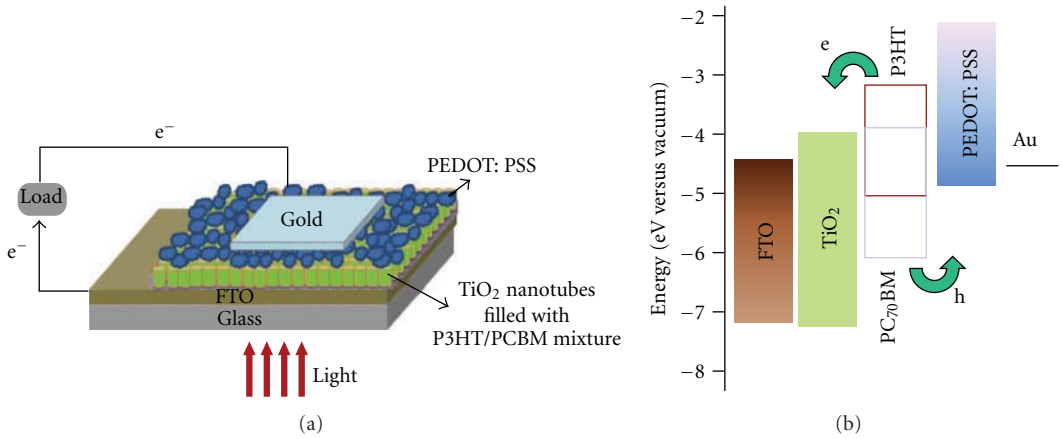


FIGURE 3: (a) Schematic device configuration of polymer TiO_2 nanotube-array-based solid-state solar cell, (b) HOMO and LUMO energies of the component materials of polymer TiO_2 nanotube-array-based solar cell. Reprinted with permission from [37].

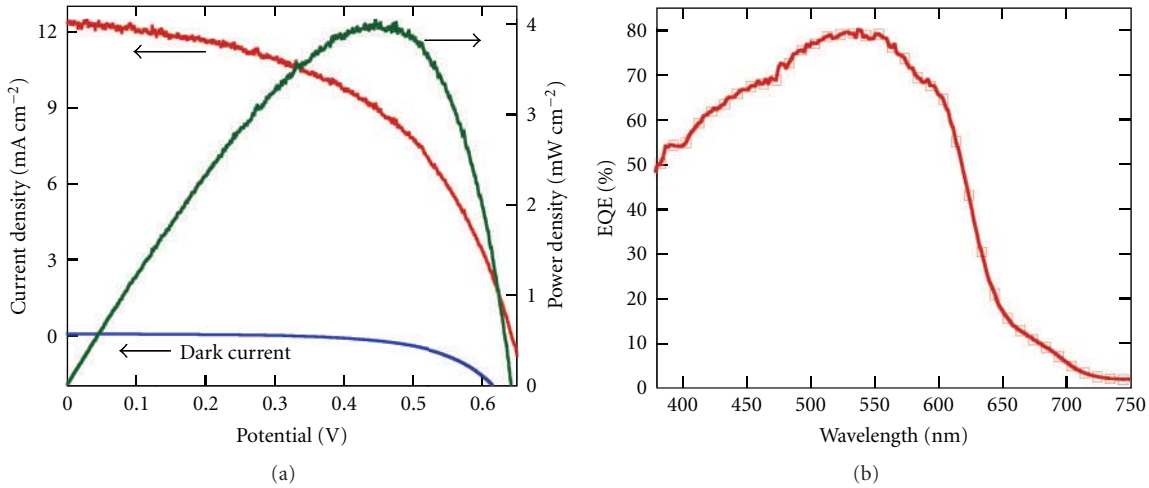


FIGURE 4: (a) *J-V* characteristics of TiO_2 nanotube array-polymer bulk heterojunction solar cells showing the dark current, photocurrent, and power density under 1 sun AM 1.5 illumination. (b) EQE of the nanotube array-polymer bulk heterojunction solar cells. Reprinted with permission from [38].

nanotube array-polymer solar cells under AM 1.5 global illumination are shown in Figure 4(a). The short circuit density is 12.43 mA/cm^2, the open circuit potential was 641 mV, and the fill factor was 0.511, resulting in an overall conversion efficiency of 4.07%. We surmise that the coiling of the polymer chains inside the nanotube pores, as manifested by the blue shift in the absorption peak relative to the neat unannealed film, may be responsible for relatively poor hole transport thus negatively impacting the fill factor. Figure 4(b) shows the external quantum efficiency (EQE) plot of the nanotube array-polymer double heterojunction solar cells, with a maximum value of 80% seen at 538 nm. When adjusted for photonic losses, which include an approximate 15% absorption loss due to the FTO coating and glass substrate, the reflection losses at the FTO-TiO_2 interface, and the FTO-glass interface, the conversion of incident photons at the absorption peak wavelength into collected electrons is nearly quantitative. The position of the EQE maximum at 538 nm is different from conventional bulk heterojunction cells where it occurs close to 500 nm [49], a difference we believe due to the device geometry and stacking order of the absorbing layers.

An alternative device configuration investigated was FTO/TiO_2 nanotubes/P3HT-PCBM/PEDOT:PSS/gold, with illumination through the FTO-glass substrate. The conduction band position of TiO_2 is just below the LUMO energy level of PCBM, resulting in efficient extraction of electrons from the PCBM. The nanotube architecture enhances the interfacial contact area between TiO_2 and P3HT and/or PCBM of the active blend layer, which implies a higher electron collecting surface area. The length of the nanotubes used was 600–700 nm with a pore size of 35 to 40 nm. P3HT and $PC_{70}BM$ blends prepared in chlorobenzene are less polar in nature and do not readily wet the TiO_2 surface which is hydrophilic in nature. For making a blend solution, we replaced chlorobenzene (CB) by o-dichlorobenzene

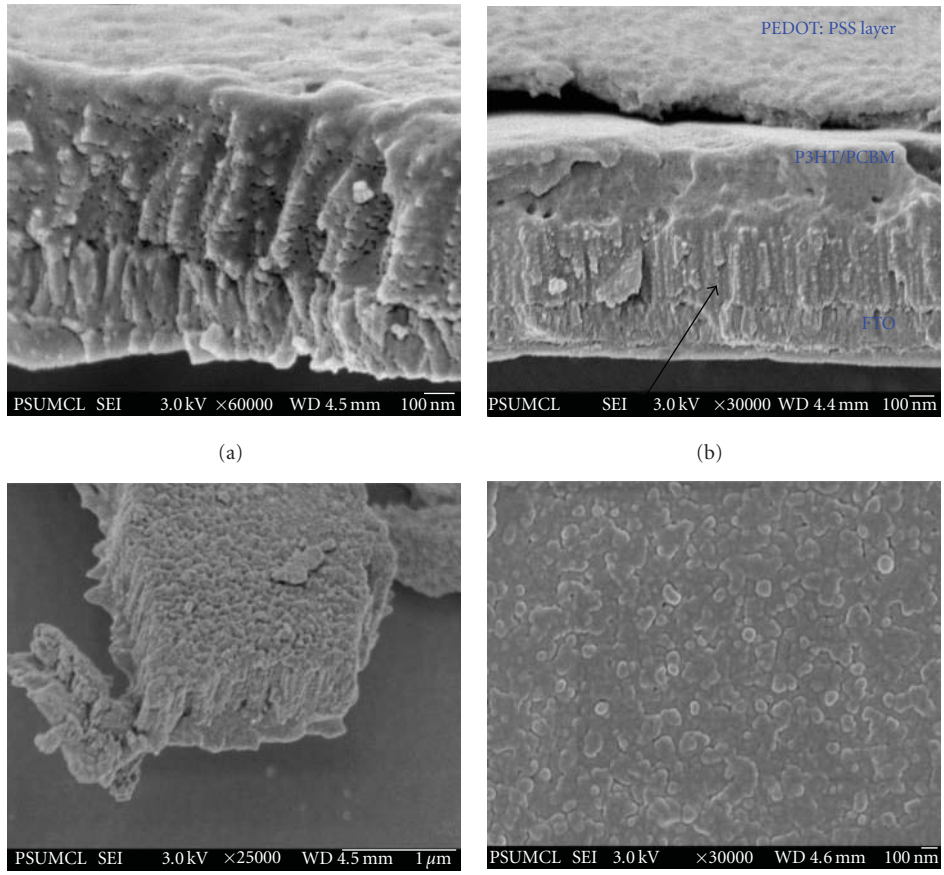


Figure 5: FESEM cross-sectional view of (a) P3HT/PCBM blend-filled nanotubes; (b) full device, with arrow denoting layer of P3HT/PCBM blend-filled nanotubes, with PEDOT:PSS layer on top. (c) FESEM cross-sectional view, of mechanically fractured sample, showing polymer blend decorated nanotubes with top unblocked. (d) Top view of PEDOT:PSS-coated full device. Reprinted with permission from [37].

(o-DCB), which is relatively more polar. The solubility of $PC_{70}BM$ in O-DCB is quite high, about 70 mg/mL, whereas chlorobenzene can dissolve only approximately 40 mg/mL of $PC_{70}BM$. To infiltrate the polymer inside the nanotubes, we wet the nanotube surface with O-DCB and then spin the nanotube sample such that the nanotubes are filled with solvent, while the excess solvent is driven away from the nanotube surface. Here the nanotube dimensions, concentration of the blended solution, and the spin speed are critical variables and require rigorous process optimization. When the P3HT/$PC_{70}BM$ samples are removed from the spin coater, they should be wet. Subsequent baking of the wet samples on hot plate at 150°C further assists the diffusion of the polymer blend into the nanotubes.

Crystallized nanotube array samples were wet with o-DCB, and the excess-solvent spun from the surface. Then a drop of P3HT + $PC_{70}BM$ (conc.) was placed on the wet surface. P3HT/$PC_{70}BM$ was mixed in ratio of 1 : 0.8 and dissolved in DCB : CB organic-solvent mixture (from 2 : 1 to 4 : 1 and then from 1 : 2 to 1 : 4). The sample was then spun, slowly ramping to a final spin speed of 300 rpm. Subsequent baking of the wet sample was performed in closed petri dish covered with aluminum foil at 150°C for 30 mins, after which it was allowed to cool at room temperature on a metal plate for 0.5 h. Afterward, a PEDOT:PSS layer was spin-coated from aqueous solution at 4000 rpm for 120 s, and then baked at 120°C for 8–10 mins in a covered petri dish. The sample was allowed to cool at room temperature for 15 min before taking the sample from the glove box for DC sputter coating of Au circular pads through a mask. Figure 5(a) shows the TiO_2 nanotube walls decorated with polymer and the opening of the tube covered with polymer. Figure 5(b) shows the cross-sectional view of the full device covered with a PEDOT:PSS layer. Figures 5(c) and 5(d) illustrate another device showing the polymer-decorated nanotubes with top unblocked for PEDOT:PSS layer infiltration. Current-voltage characteristics and the overall conversion efficiency of the photovoltaic devices made using P3HT/PCBM-coated TiO_2 nanotubes are shown in Figure 6(a), with corresponding efficiencies shown in Figure 6(b). There are five curves in the I-V plot, each curve represents the treating/wetting of nanotubes with different type of organic solvents just before putting a concentrated P3HT/PCBM solution. Curve 1 represents the device performance of nanotubes treated with t-butyl pyridine (TBP). TBP is a polar solvent, which can easily wet the hydrophilic surface of nanotubes but

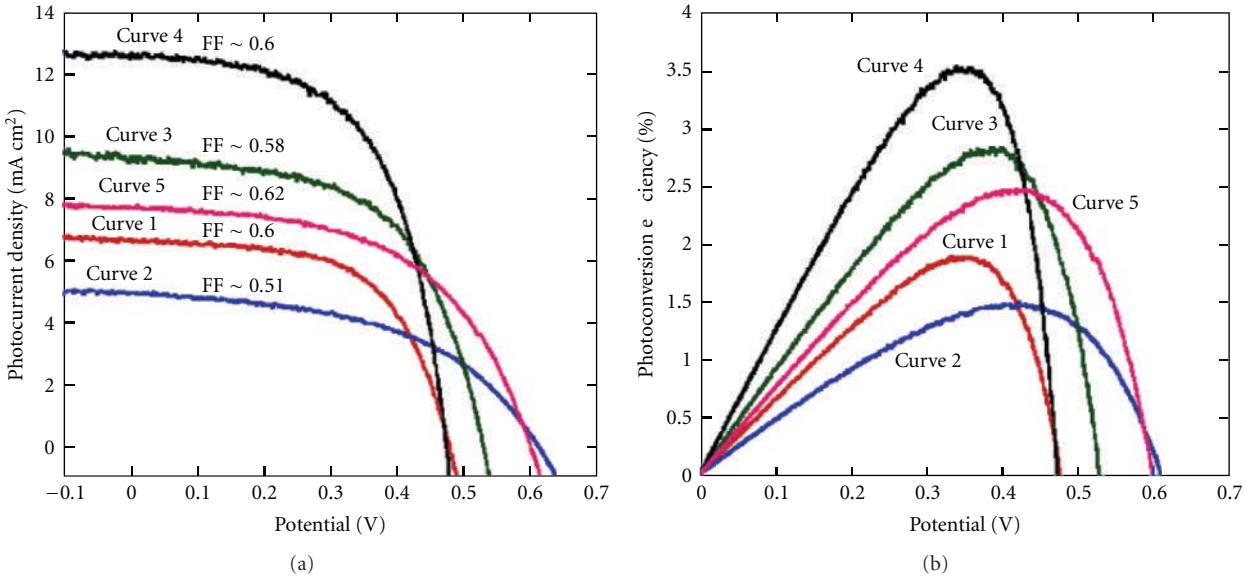


Figure 6: (a) Current-voltage characteristics and (b) the overall conversion efficiency of solid-state photovoltaic devices made using P3HT/PCBM-coated TiO_2 nanotubes. Five curves, 1 to 5, represent five different TiO_2 surface treatments before polymer blend spin coating. Treatment of nanotubes for (1) Curve 1—TBP, (2) Curve 2—CB, (3) Curve 3—o-DCB, (4) Curve 4—soaked in o-DCB, and (5) Curve 5—soaked in o-DCB and baked at 165°C. Curves 1 to 4 were baked at 150°C. Reprinted with permission from [37].

does not allow the polymer film to penetrate within the nanotube pores; minimal polymer coverage of the nanotubes leads to small current. Replacing TBP with chlorobenzene (CB), we achieved the device performance displayed by curve 2. Though the photocurrent is low, the photovoltage is close to the expected value obtained in a conventional bulk heterojunction device. Treating the TiO_2 surface with o-DCB, which has polarity higher than that of CB but lower than TBP, we achieve higher saturated photocurrent density, as shown by curve 3, with a photovoltage higher than that achieved in the TBP-treated sample but lower than that of the CB-treated surfaces. Thoroughly wetting the nanotubes with o-DCB improved the polymer intercalation, with the performance of such a photovoltaic device illustrated by curve 4. All devices shown by curves 1 to 4 were baked at 150°C for 30 min after spin coating on the polymer solution. Using a higher baking temperature of 165°C on our best device, curve 4, resulted in a 4 mA/cm^2 drop in photocurrent but an increase in photovoltage to 0.61 V, see curve 5. Curve 4 showed the best photoconversion efficiency of ≈3.5%, with the low voltage apparently due to high dark currents. Choice of solvent, and its ability to prevent water molecules from residing at the inorganic-organic interface, plays a critical role in determining the overall efficiency of the photovoltaic devices. Two kinds of photovoltaic devices were fabricated by infiltrating organic semiconductors into rutile nanowire arrays, see Figure 2(d), with the first being a blend of P3HT and PCBM and the second purely P3HT. The polymer blend solution prepared in chlorobenzene contained 10 mg/mL of P3HT and 8 mg/mL of PCBM, the optimized concentrations as suggested by Kim et al. [48]. For both kinds of devices, the device fabrication process was identical: the TiO_2 nanowire array sample was wetted with the polymer solution for 30 s, and then spin coated at 600 rpm. The sample was then baked at 150°C for 10 min in a covered petri dish and finally cooled to room temperature. Subsequently, a layer of hole injecting PEDOT:PSS was deposited by spin coating an aqueous suspension of the polymer at 4000 rpm. The samples were then placed on a hot plate at 120°C for 10 min. All spin coating and baking steps were carried out in an inert ambient glove box. Finally a 50 nm film of gold was evaporated onto the devices through a shadow mask to form the back contact (rectangular size—2.2×3.4 mm^2). The average length of the TiO_2 nanowire array and the total thickness of the active layer were 600 and about 700 nm, respectively. Outside the gold top contact area, the PEDOT:PSS layer was carefully scrapped away to avoid any photocurrent contribution from that region. The solar cell testing was performed in air.

A photocurrent density-potential (J-V) characteristic of a typical TiO_2 nanowire array-P3HT and PCBM polymer blend solar cell under AM 1.5 global illumination from a calibrated Class A solar simulator is shown in Figure 7(a). The short circuit current density (J_{sc}) is 8.3 mA/cm^2, the open circuit potential (V_{oc}) 0.44 V, and the fill factor 0.41, resulting in an overall conversion efficiency of 1.5%. In Figure 7(b), the incident photon to current conversion efficiency (IPCE) of the device is plotted as a function of wavelength. The maximum IPCE value for the TiO_2 nanowire device reaches about 56% at 550 nm. Upon integrating the current irradiance, determined using the IPCE curve over the wavelength range from 350 to 750 nm, the value of the overlap integral is close to the J_{sc} obtained from the J-V plot. The electrical characteristics of a typical photovoltaic cell using pure P3HT, not shown, without addition of PCBM were also investigated; for this type of cell, the nanowire array was first coated with a monolayer

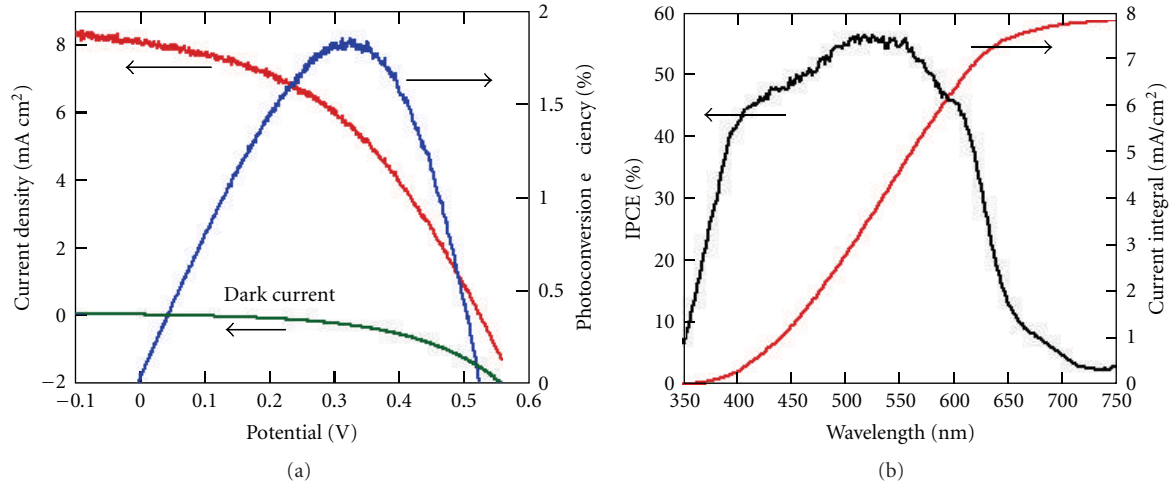


FIGURE 7: J-V characteristics and photoconversion efficiency of TiO_2 nanowire array-polymer blend (P3HT:PCBM) heterojunction solar cell. (b) The IPCE and overlap integral of photocurrent irradiance of the described TiO_2 nanowire array-polymer heterojunction solar cells. Reprinted with permission from [37].

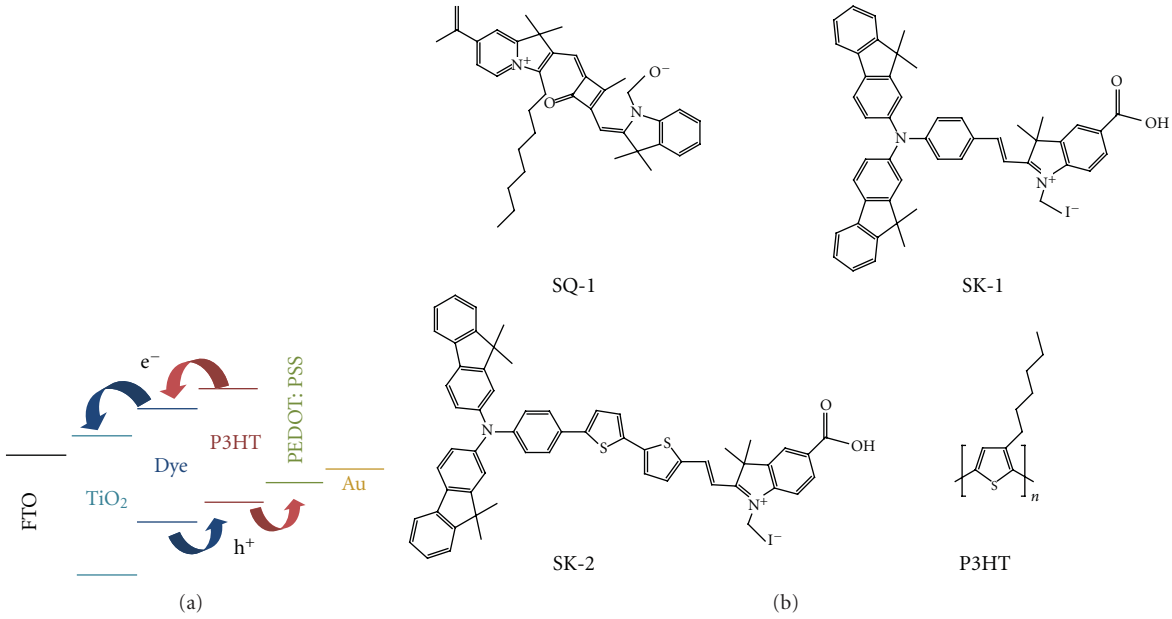


FIGURE 8: (a) Depiction of energy level positions and charge transfer processes of the constituent layers of the described hybrid solar cell. (b) Molecular structure of organic dyes (SK-1, SK-2, SQ-1) and P3HT polymer. Reprinted with permission from [7, 51].

of N-719 dye by immersion in a 0.5 mM ethanol solution of dye overnight to suppress recombination. J_{sc} is 1.5 mA/cm^2, V_{oc} 0.56 V, and the fill factor 0.55, resulting in an overall conversion efficiency of 0.46%. For charge transfer to occur efficiently between the regioregular P3HT and the TiO_2, a TiO_2-P3HT interface needs to be within 10–20 nm of every produced exciton [50]. However, an average nanowire separation of 30 nm existed in our samples; consequently, a significant fraction of the excitons generated in the P3HT are lost to recombination resulting in a lower photocurrent. When a blend of P3HT and PCBM is used, two interfaces, namely, the TiO_2-P3HT and the PCBM-P3HT interface, are available for exciton splitting. Therefore, charge separation is improved and the photocurrent densities are higher in devices employing the blend.

3.2. Ordered Heterojunction Solar Cell. We consider a heterojunction solar cell where unsymmetrical squaraine (SQ-1) organic dye decorated vertically oriented nanotubes are infiltrated with P3HT [7]. The HOMO-LUMO levels favor electron injection from P3HT into the dye and then to the TiO_2, see Figure 8(a). We also investigated two other hemicyanine organic dyes, SK-1 and SK-2 [51], as shown in Figure 8(b), having different optical and electrochemical properties to modify the TiO_2 interface and compared their solar cell performance with respect to SQ-1 dye as a

Table 1: Absorption, emission, and electrochemical properties of SQ-1, SK-1, SK-2 dyes, and P3HT polymer [7, 51].

Dye/Polymer	λ_{abs}[a], nm (ε, $M^{-1}cm^{-1}$)	λ_{em}[a], nm	E_{ox}[b]/[V versus Fc/Fc^+]	$E_{0\text{-}0}$[c], [eV]	E_{HOMO}[d], [eV]	E_{LUMO}[d], [eV]
SK-1	342, 582	642	0.41	2.00	5.21	3.21
SK-2	359, 619	721	0.63	1.85	5.43	3.58
SQ-1 dye	637 (159, 700)	652	0.38	1.93	5.18	3.25
P3HT	443	568	—	1.9	5.1	3.2

[a]Absorption and emission spectra were measured in ethanol solution.
[b]A silver wire was used as a pseudoreference electrode and was calibrated with a ferrocene/ferrocenium (Fc/Fc^+) redox couple. The electrochemical experiments were measured in CH_3CN with 0.1 M $(n\text{-}C_4H_9)_4NPF_6$ with a scan rate of 100 mVs^{-1}.
[c]$E_{0\text{-}0}$ was determined from intersection of absorption and emission spectra in ethanol.
[d]The energy levels of the HOMO and LUMO were determined using the following equations: E_{HOMO} (eV) = $E_{ox} - E_{FC/FC^+} + 4.8$ eV and E_{LUMO} (eV) = $E_{HOMO} - E_{0\text{-}0}$.

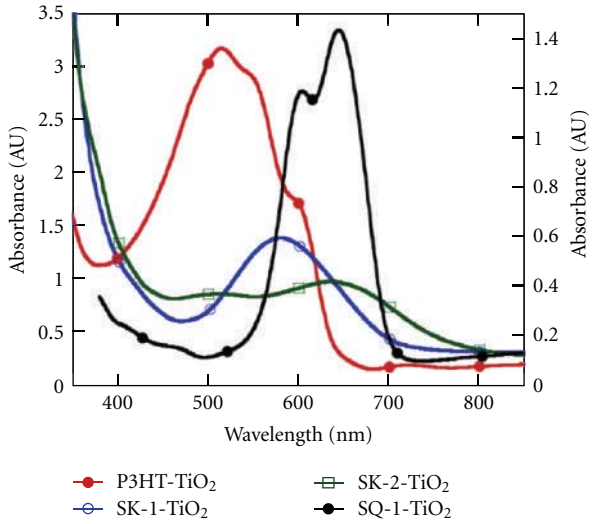


Figure 9: Optical absorbance of SK-1-, SK-2-, and SQ-1-sensitized TiO_2 nanotube arrays, and P3HT intercalated nanotube arrays without dye sensitization. The nanotube arrays had an average pore size of 35 nm and tube length of 600–700 nm. Reprinted with permission from [7, 51].

sensitizer. As seen in Figure 8(b), the molecular structures of the SK dyes have different π-conjugation lengths between the bis-dimethylfluoreneaniline moiety acting as electron donor and carboxylic acid moiety acting as electron acceptor. These two parts are connected by a 1-ethyl-3,3-dimethyl-3 *H*-indolium moiety.

Figure 9 displays the UV-Vis-NIR absorption spectra of four samples, TiO_2 nanotube arrays sensitized with SK-1, SK-2, or SQ-1 dyes, and P3HT-infiltrated TiO_2 nanotube array films [7, 51]. P3HT coverage of the TiO_2 nanotube arrays shows no shift in the absorption peak position compared to that of neat P3HT films [52], indicating a high degree of π-π stacking of the polymer chains within the nanotubes. Compared to the organic dyes, P3HT is highly absorbing in the visible range. The absorption spectrum of the dyes on the nanotube array films is broadened due to interaction between dye and TiO_2 [53]. Dye sensitization of nanotube arrays with SK-2 dye results in a red shift in the absorption peak, while no such change was observed for the SK-1 dye. The absorption spectra of SQ-1 on the TiO_2 nanotubes arrays films show a small red shift of 9 nm suggesting J-type aggregation, which can further extend the photon absorption into the NIR region. The LUMO levels of the two dyes adsorbed on the TiO_2 nanotube array films, estimated from the oxidation potentials and the excitation transition energy ($E_{0\text{-}0}$) determined from the intersection of absorption and emission spectra, are listed in Table 1. The excitation transition energy ($E_{0\text{-}0}$) of SK-1 and SK-2 are calculated to be 2.00 and 1.85 eV, respectively. The reduced excitation transition energy of SK-2 is due to extension of the π-π conjugation length associated with the two additional thiophene units. The LUMO level of the dyes (SK-1: 3.21 eV and SK-2: 3.58 eV) is much higher than the TiO_2 conduction band, suggesting that electron transfer from the excited dye to the TiO_2 conduction band is readily feasible. The LUMO level of the SQ-1 dye is more negative than the P3HT LUMO level and less negative than the TiO_2 conduction band, while the HOMO level of the SQ-1 dye is close to or slightly below the HOMO level of P3HT. Hence, upon absorption of a red/NIR photon, the organic dye injects an electron into the TiO_2 conduction band and is regenerated by donation of a hole to the P3HT.

First, we consider the use of SQ-1 dye as a sensitizer which absorbs in the red and NIR portion of solar spectrum in combination with hole conducting P3HT that absorbs higher energy photons. The low band gap organic dye does not block transmission of the high-energy photons of near UV-visible range, see Figure 9 [7]. In our device, excited states generated in the dye find themselves in close proximity to two interfaces for dissociation: the TiO_2-dye interface and the dye-P3HT interface. For excitons generated in the P3HT, the P3HT-dye interface is the closest available for splitting, and the largest distance the excitons need to diffuse to reach this interface corresponds to the radius of the nanotube pore. After exciton splitting, electrons are injected into the TiO_2, while hole-polarons travel through the P3HT layer to the PEDOT:PSS hole collection contact. The open circuit voltage V_{oc} is determined by the TiO_2 quasi-Fermi level and the P3HT HOMO level. The TiO_2 nanotube array pore size, from 20 to 35 nm, was selected such that P3HT chains can infiltrate into the pores but also allow photogenerated excitons in the P3HT to readily diffuse to

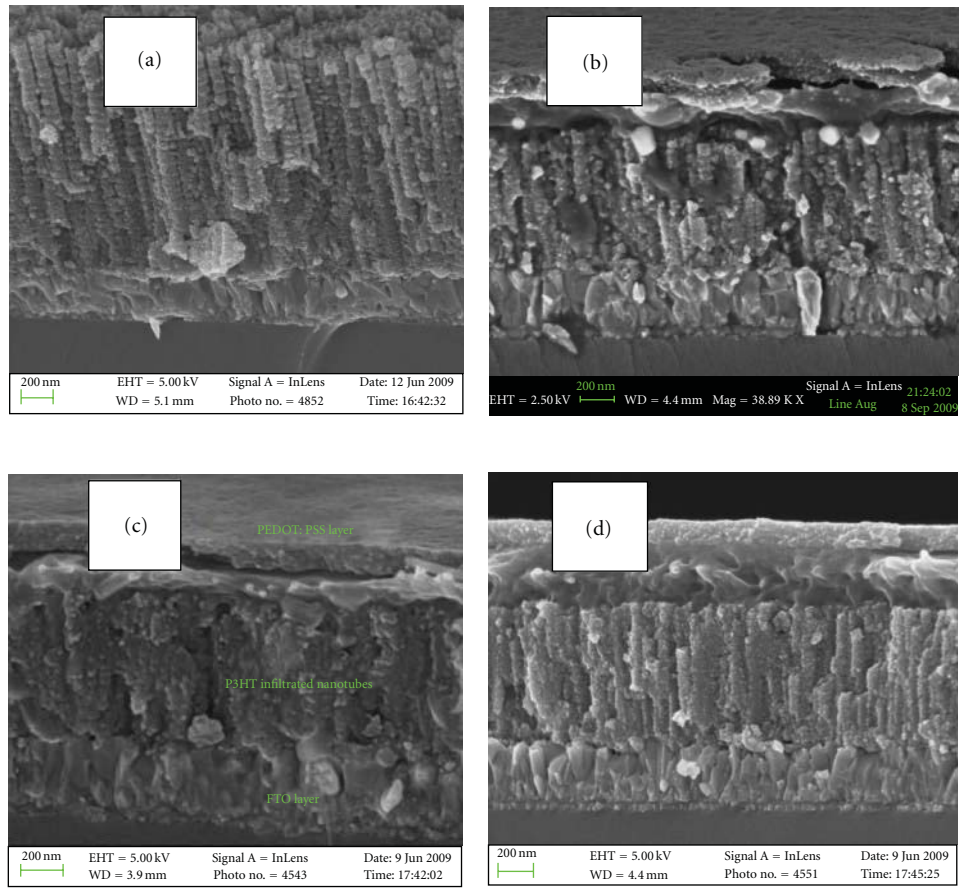


FIGURE 10: (a) Typical cross-sectional view of 60 nm pore size, 1–1.2 μm length TiO_2 nanotube array film after $TiCl_4$ treatment. Cross-sectional FESEM image of TiO_2 nanotube (≈35 nm pore size, ≈600–700 nm nanotube length)/SQ-1 dye/P3HT/PEDOT:PSS photovoltaic devices showing: (b) nanotubes partially infiltrated with polymer, fabricated under the condition of excess wetness; (c) fully infiltrated nanotubes fabricated under optimized wetness condition; and (d) partial infiltration of the P3HT polymer within the nanotubes, fabricated under dry condition. Reprinted with permission from [7].

the exciton splitting interface. This configuration has the following key advantages [7]. (i) The ordered heterojunction architecture provides percolation paths for both types of charge carriers. (ii) The vertically oriented nanotube array architecture decouples exciton diffusion from light absorption. (iii) There are two complementary photon absorbers that provide broad-spectrum absorption, namely, the dye molecules anchored to the nanotube walls and the organic semiconductor (P3HT) within the nanotubes.

Devices built upon nanotube arrays having three different average pore sizes, namely, 20 nm (length ~500 nm), 35 nm (length ~600 to 700 nm), and 60 nm (length ~1 to 1.2 μm) were investigated [35]. All samples were crystallized and treated with aqueous $TiCl_4$ solution under identical conditions. A cross-sectional FESEM view of a $TiCl_4$-treated nanotube array film (length ~1 to 1.2 μm) is shown in Figure 10(a). The nanotubes have the general shape of a common laboratory test tube, with the top of the tube open and the bottom closed [37, 54]. To assist polymer infiltration within the tubes, the nanotube array film was wetted with p-xylene, a nonpolar organic solvent. After removing the excess solvent, nanotube arrays were covered with a P3HT polymer solution (30 mg/mL concentration) prepared in a 3 : 1 mixture of ortho-dichlorobenzene (o-DCB) and chlorobenzene (CB). The sample was then spun, with the p-xylene acting to wick the P3HT inside the nanotube arrays and the polymer solution forming a thin layer atop the nanotube array film. The sample was then immediately transferred onto a hot plate, with the remaining organic solvent quickly evaporating and the polymer inside the nanotubes making a dry interface with the dye molecule layer. Previously, Coakley and coworkers had demonstrated the infiltration of P3HT into the pores of alumina/titania using a polymer melt-infiltration technique [55]. After cooling the sample to room temperature, a thin layer of PEDOT:PSS was spun onto the sample. It was then baked at 120°C to remove water present in the PEDOT:PSS layer, avoiding degradation of the P3HT, and then finally at 150°C to promote adhesion between the PEDOT:PSS and P3HT layers.

The duration of the spin-coating to control the wetting of P3HT solution upon the dye-sensitized TiO_2 nanotube arrays depends on the following factors: type of glove box,

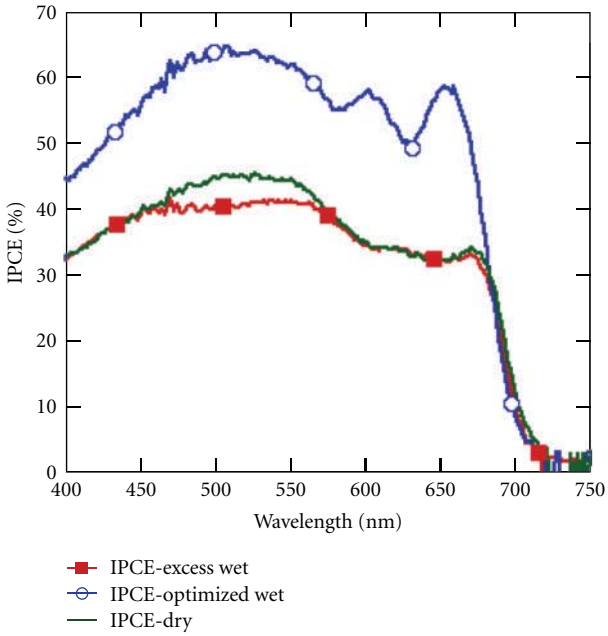


Figure 11: IPCE of an FTO/TiO_2 nanotube array/SQ-1 dye/P3HT/PEDOT:PSS/Au solar cell, where the P3HT layer was prepared with different degrees of surface wetness prior to a 150°C postbake. Excess wetness, where the film was still wet entering the postbake; dry, indicating where the film had dried on the spinner prior to postbake; optimized, where upon just visually drying the device was immediately removed from the spinner and exposed to the postbake. The dye sensitization and PEDOT:PSS layer are identical in all the three samples. Nanotube array films of 35 nm average pore diameter and 600–700 nm length were used. Reprinted with permission from [7].

air circulation, and what the inert gas pressure is inside the glovebox when the device is fabricated. Hence instead of specifying the exact spinning duration, we instead describe the sample condition. After performing the suggested initial treatment with p-xylene on dye-sensitized TiO_2 nanotube arrays, the sample surface was completely covered with P3HT solution (30 mg/mL, prepared using a 3 : 1 ratio of o-DCB and CB) and then spun at 250 rpm. Spinning the sample for 200–300 s, a wet layer of excess P3HT on top of nanotube arrays was observed. This sample was immediately transferred to a hot plate and baked at 150°C for 20 minutes which resulted in partial infiltration of the polymer inside the nanotubes due to evaporation of the o-DCB solvent. A cross-sectional image of this sample with a PEDOT:PSS layer deposited on top is shown in Figure 10(b). On further extending the spinning time to 350–400 s, the P3HT film was partially wet (optimized wet). Immediately baking the sample on a hot plate resulted in complete filling of the tubes, see Figure 10(c). Extended spinning durations, that is, 450 to 500 s, resulted in a dry P3HT layer from which only partial decoration of the nanotube walls was achieved, see Figure 10(d). The glancing angle X-ray diffraction (GAXRD) pattern of the completed device showed the presence of highly crystalline P3HT, where the peak at $2\theta = 5°$ corresponds to a P3HT interchain spacing associated with interdigitated alkyl chains [56, 57].

Details of the device structure, and hence performance, are dependent on the device fabrication procedure. Consider as an illustration the IPCE of three of the described P3HT/dye-sensitized TiO_2 nanotube array devices, see Figure 11, with the P3HT solution (30 mg/mL, prepared using a 3 : 1 ratio of o-DCB and CB) applied in varying degrees of sample surface wetting. Samples coated with an excess amount of P3HT solution, where spinning is stopped before the P3HT solution dries, had minimal polymer within the tubes presumably due to evaporation of the o-DCB solvent. Cells fabricated with a minimal amount of P3HT solution, that is, spinning was stopped after the P3HT solution had completely dried, had only partial decoration of the P3HT on the nanotube walls. Optimal device performance was achieved with an intermediate surface wetting, with the sample removed from the spinner just before the polymer dried, then immediately transferred to the 150°C hot plate. This timing of surface wetting/drying resulted in full penetration of the polymer into the nanotubes, with the polymer making uniform contact with the organic dye layer. Such samples exhibit an IPCE of 50–65% between 420 and 680 nm. The resulting samples appear reddish with a light violet tinge. Due to significant overlap between the emission spectrum of P3HT and the absorption spectrum of the SQ-1 dye, exciton transfer from P3HT to the dye by Förster-type resonance energy transfer (FRET) is possible [9, 58–62]. Upon calculating the spectral overlap integral from the normalized photoluminescence (of P3HT on a very thin TiO_2 film) [59] and absorption (of SQ-1 dye ethanolic solution) spectra, considering an emission quantum efficiency of 1% for P3HT [60], and assuming random orientation of the donor and acceptor molecules and the effective refractive index of P3HT-TiO_2 film of 1.6, we calculate a Förster radius [58] of 2.58 nm which could result in an effective exciton diffusion length in the range of 14 to 18 nm [61, 62]. Based on the exciton harvesting calculation given by Scully and coworkers [62], it was found that about 65–75% of the excitons generated in P3HT infiltrated inside 35 nm pore size TiO_2 nanotube arrays can be harvested. The coexistence of resonance energy transfer may account for the high charge transfer efficiencies in this system as inferred from external quantum yield measurements.

The fill factor and open-circuit voltage of the SQ-1 dye-based solar cells was further improved by wetting the SQ-1 sensitized nanotube array films (pore size ~35 nm, tube length 600–700 nm) with 0.05 to 0.1 M tert-butyl pyridine in p-xylene solution (instead of pure p-xylene), spin coating the P3HT and PEDOT:PSS layers, depositing the gold electrode, and then baking the device at 120°C for 1 min in air. The performance of a typical device is shown in Figure 12, with $J_{sc} = 10.75\,\text{mA/cm}^2$, $V_{oc} = 0.55\,\text{V}$, $\text{FF} = 0.55$, and $\eta = 3.2\%$. Tert-butylpyridine is known to increase the open circuit voltage by upwards shifting the TiO_2 band edge [63, 64], and by physically sealing molecular scale voids at the interface. The efficiency of our champion device was found to be 3.8% ($J_{sc} = 11\,\text{mA/cm}^2$, $V_{oc} = 0.6\,\text{V}$, $\text{FF} = 0.58$). If we account for the transmittance loss of 10% across the visible range due

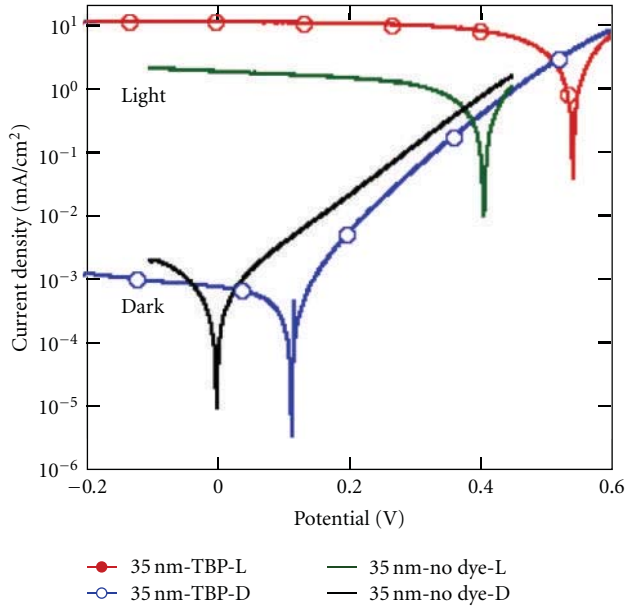


FIGURE 12: J-V curves showing the improved performance of a FTO/35 nm pore, 600–700 nm length TiO_2nanotube array/SQ-1 dye/P3HT/PEDOT:PSS/Au hybrid solar cell where the dye-sensitized nanotube array surface, prior to application of the P3HT layer, is wetted with 0.05 to 0.1 M tert-butyl pyridine in p-xylene. Also shown is the performance of an otherwise identical cell lacking the SQ-1 dye layer. L denotes cell performance under light illumination D denotes cell performance in the dark. Reprinted with permission from [7].

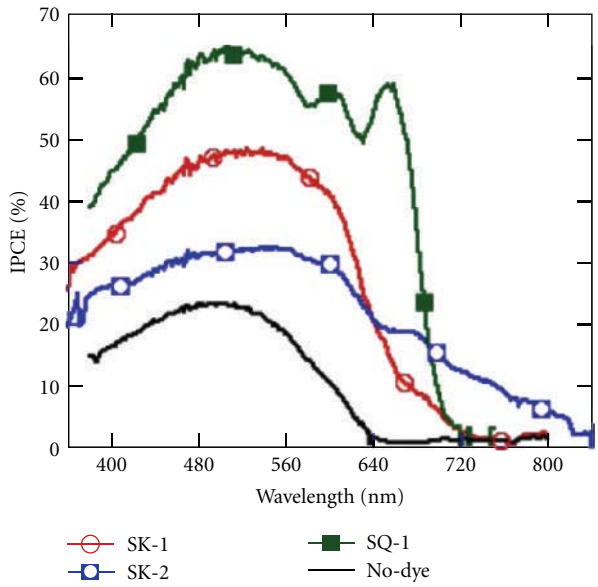


FIGURE 13: IPCE spectra of four hybrid solar cell device structures, namely, FTO/TiO_2 nanotube array/SK-1, SK-2, SQ-1, or no dye layer/P3HT/PEDOT:PSS/Au. The dye sensitization and PEDOT:PSS layer are identical in the four samples. Reprinted with permission from [51].

to the UV filter in the light source (necessary since UV light rapidly degrades the SQ-1 dye), an efficiency of ≈4.2% can be expected. The performance of a TiO_2 nanotube array/P3HT solar cell without an organic dye layer is also shown in Figure 12; $J_{sc} = 1.8$ mA/cm^2, $V_{oc} = 0.41$ V, FF = 0.46, and $\eta = 0.34\%$.

With use of the organic dye layer, the photoconversion efficiency of a typical device increases from 0.34% to 3.2%, with the open circuit voltage increasing from 0.41 V to 0.55 V. Acid-base interactions arising from carboxylic group anchoring of the organic dye affect the TiO_2 band edge by protonating it. As reported by Goh and coworkers [65], the magnitude of this shift is about 0.2 eV for Ru (II) dyes. It was also noted that extensive $TiCl_4$ treatment of the nanotubes was found to increase the open-circuit voltage to 0.67 V, but resulted in considerably lower photocurrents. The J-V and IPCE measurements of our devices were performed in air and the photovoltaic results were consistent for a number of runs made on several days.

Figure 13 shows the IPCE of four hybrid solar cell device structures, namely, FTO/TiO_2 nanotube array/SK-1, SK-2, SQ-1, or no dye layer/P3HT/PEDOT:PSS/Au [51]. The hybrid cell without an organic dye layer shows a maximum IPCE of 22% between 350 and 650 nm; it appears that these relatively small IPCE values are due to the poor interface between the organic polymer and inorganic oxide. The increase in the photocurrent action spectrum for wavelengths beyond 650 nm is due to charge injection from the dyes. In the SK-1 solar cell, IPCE values improve to 50% in the visible range with photocurrent generation up to 750 nm. The photoaction spectrum closely matches the optical absorption spectrum of the SK-1 dye and P3HT polymer, confirming that the observed photocurrent arises from electron injection by the SK-1 dye and P3HT polymer. The IPCE values of the SK-1 device are comparatively small in the red and NIR region due to the relatively lower absorption coefficient of SK-1 dye in this range. With the SK-2 dye, we observe relatively lower values of IPCE in the visible range, a maximum value of about 30%; however, significant IPCE values extend up to 800 nm. In the SQ-1 solar cells, an IPCE of 50–65% is achieved between 420 and 680 nm, indicating that these high IPCE values are at least partially due to the smaller absorption overlap with that of the P3HT polymer. That is, two complementary photon absorbers can provide broad-spectrum absorption.

Regarding the J-V characteristics of FTO/TiO_2 nanotubes/SK-1 or SK-2/P3HT/PEDOT:PSS/Au hybrid solar cells [51], we found that the photovoltaic performance of a typical SK-1 cell are $J_{sc} = 6.7$ mA/cm^2, $V_{oc} = 0.56$ V, FF = 0.43, and $\eta = 1.61\%$. The photovoltaic properties of a typical SK-2 cell are $J_{sc} = 5$ mA/cm^2, $V_{oc} = 0.6$ V, FF = 0.52, and $\eta = 1.57\%$. Our champion SK-dye-based devices demonstrate photoconversion efficiencies of ≈1.9%. It is clear that the dye layer upon the TiO_2 nanotube array substrate acts both as a photo-sensitizer and electronic mediator, significantly improving both the photocurrent and the photovoltage of the solar cell.

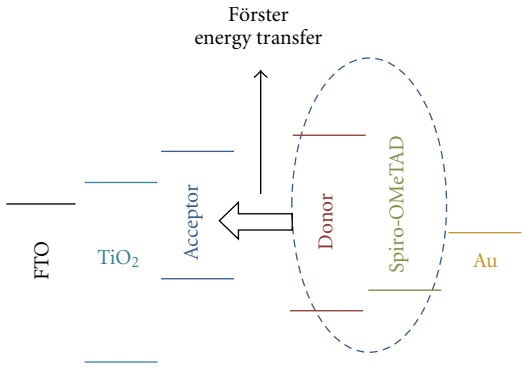


Figure 14: Depiction of energy level positions of FRET-type solid-state dye-sensitized solar cell (SS-DSSC) constituents. Reprinted with permission from [12].

3.3. Förster Resonance Energy Transfer (FRET)

3.3.1. FRET in Solid-State DSSCs Using TiO_2 Nanotubes. It is generally agreed that new materials as well as advanced device concepts are necessary for further improvements in efficiencies [66, 67]. The use of FRET has been contemplated as an alternative mechanism for charge separation and a way to improve exciton harvesting by placing the exciton close to the heterojunction interface [68]. In inorganic quantum-dot-based solar cells, the use of FRET to transfer the exciton generated in the quantum dot to a high mobility path, such as a nanowire or a quantum well, has been proposed as a way to bypass the traditional limitations of charge separation and transport [69].

In conventional DSSCs, a photoactive dye decorates the mesoporous TiO_2 film and the available empty space (porosities of ≈50% to 65% are common) [70] is filled with iodide-based redox electrolyte for dye regeneration. This reddish-brown nonphotoactive electrolyte also absorbs some portion of the visible light spectrum. To achieve a FRET-based photovoltaic architecture, we can effectively use this porous region by filling the pores of red/NIR light absorbing organic dye coated TiO_2 nanotubes with a mixture of spiro-OMeTAD and donor material—a high quantum yield, visible light absorbing fluorescent material. To improve device performance, the florescence spectrum of the donor molecules should match the optical absorption band of the absorber dye on the TiO_2. Further, the pore size dimensions should be small enough so that the nonradiative energy transfer events happen in close proximity. In the present work, the empty space (i.e., pores) of Red/Near IR absorbing SQ-1 organic dye [7, 71] coated transparent TiO_2 nanotube array films [35, 38, 72, 73], 500 to 600 nm in length with 20–28 nm pores on fluorine-doped tin oxide-coated glass, were filled with Spiro-OMeTAD [74] blended with a visible light absorbing 4-(dicyanomethylene)-2-methyl-6-(p-dimethylaminostyryl)-4H-pyran, DCM-pyran [75], donor molecules. The calculated Förster radius is 6.1 nm. The donor molecules contributed a FRET-based maximum IPCE of 25% with an increase in overall photoconversion efficiency by 76% [12].

Solid-state dye-sensitized solar cells (SS-DSSCs) have demonstrated open circuit photovoltages higher than their liquid-junction counterparts [15] and offer the prospect of an easily fabricated photovoltaic technology with relatively low material costs. In particular, SS-DSSC photovoltages of high value have been reported with the combined use of an organic sensitizer dye and hole transporting Spiro-OMeTAD [76–79]. This is attributed to the lower HOMO level of Spiro-OMeTAD in comparison to the redox potential of the I^-/I_2 electrolyte used in TiO_2-based liquid-junction DSSCs [15]. To increase SS-DSSC photoconversion efficiencies, numerous studies have investigated the use of high absorption coefficient dyes to increase light harvesting [79–82]. Higher device photoconversion efficiencies cannot be achieved simply by increasing device thickness; for example, Spiro-OMeTAD remains an effective hole transporting material for nanoporous dye-sensitized TiO_2 layers up to approximately 2.0 μm thick-for greater thicknesses issues of surface wetting and infiltration limits its successful application [83]. While organic dyes are known to strongly absorb light, enabling the use of thin layer devices, they do so only over a narrow spectral absorption bandwidth. Dye cocktails can potentially broaden the range of absorption; however, the coverage of one dye is generally at the expense of the other leading to relatively lower saturation photocurrents in their respective spectral absorption ranges [84–86].

There have been a few initial reports on the use of FRET [58] to enhance the efficiency of hybrid photovoltaic devices through increased light utilization [9–11, 13, 62, 87, 88]. In the FRET-based solid-state organic dye-sensitized solar cell possessing an extended photocurrent spectrum, the donor molecules embedded within the solid-state hole transporting material, Spiro-OMeTAD, absorb the high energy photons subsequently transferring the energy to the acceptor dye. Spiro-OMeTAD is a small organic molecule of high hole mobility, 10^{-4} cm^2/V·s, that is, noncrystalline in nature with a high glass transition temperature [89], properties that facilitate regeneration of the photo-excited acceptor dye. Spiro-OMeTAD is host for the donor molecules, and the Spiro-OMeTAD-donor dye mixture is intercalated within the acceptor dye-sensitized nanotube array films. The vertically oriented TiO_2 nanotube array morphology enables direct transport of the electrons injected from the photo-excited organic dye to the underlying FTO layer [27, 28]. The nanometer-scale nanotube pores, intercalated with the hole transporting materials, provide a facile path for hole transport. The energy level positions of the selected donor, DCM-pyran [75], and acceptor, SQ-1 dye [7], with respect to Spiro-OMeTAD [15, 90, 91] (Typical physical data of Spiro-OMeTAD, provided by EMD Chemicals (Merck KGaA, Darmstadt, Germany): HOMO energy ~ −4.9 eV, LUMO energy ~ −1.9 eV, Band gap ~3.0 eV, Glass transition temperature T_g ~120°C, Melting point T_m ~246°C, Purity >99.9% (Test procedure—HPLC). Note: the energy levels are determined using cyclic voltammetry and UV-VIS; these values are usually 0.2-0.3 eV less deep than with other optical methods (e.g., UPS).) and TiO_2 are shown in Figure 14. The selected donor, DCM-pyran, is a red arylidene laser dye with emission in the 570–620 nm range that is soluble in chlorobenzene (CB).

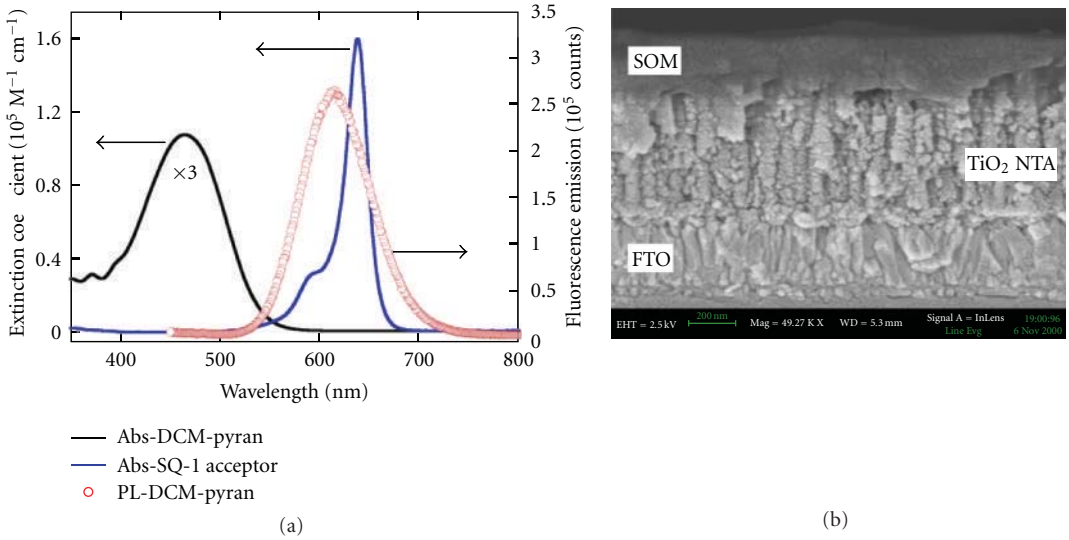


Figure 15: (a) Extinction coefficient of DCM-pyran donor and SQ-1 acceptor molecules dissolved in ethanol/acetonitrile-solvent mixture and the emission spectra of the same DCM-pyran solution. The DCM-pyran extinction coefficient is multiplied by 3 for display purposes. (b) Cross-sectional FE-SEM image showing DCM-Spiro-OMeTAD (denoted SOM) infiltration within SQ-1 dye-sensitized TiO_2 nanotube array (NTA, nanotube pore size ~20 to 28 nm, length ≈500 to 600 nm). FTO denotes the fluorine-doped tin oxide layer upon the glass substrate. Reprinted with permission from [12].

Figure 15(a) shows that a 7.2 μm DCM-pyran solution (DCM-pyran added in equal portions to a 1 : 1 ethanol:acetonitrile mixture) absorbs in the 350–550 nm wavelength range with a molar extinction coefficient of 37,900 $M^{-1}cm^{-1}$ at 460 nm; a fluorescence emission maximum is observed at 580 nm for a 430 nm excitation wavelength. The UV-VIS absorption spectrum of a 3.5 μm SQ-1 acceptor dye solution, in ethanol/acetonitrile, Figure 15(a), shows a molar extinction coefficient of 159,800 $M^{-1}cm^{-1}$ at a λ_{max} of 637 nm corresponding to strong π-π^* charge transfer transitions. As required for FRET, the fluorescence emission spectrum of DCM-pyran overlaps with the SQ-1 absorption spectrum. In calculating the spectral overlap integral from the normalized DCM-pyran photoluminescence and SQ-1 absorption spectra (in ethanol/acetonitrile), given a luminescence quantum yield (photons emitted to the number of photons absorbed by the sample) of 60% for DCM-pyran [92], assuming random orientation of the donor and acceptor molecules and an effective refractive index of Spiro-OMeTAD infiltrated TiO_2 nanotube arrays of 1.5, values ranging from 1.4 to 1.5 have been reported for liquid and Spiro-OMeTAD-based DSSC electrolytes [9–11], we calculate a Förster radius of 6.1 nm.

The SQ-1 dye absorption peak (in ethanol) broadens with sensitization of the TiO_2 nanotube array surface, with λ_{max} red shifted by 9 nm, and an FWHM of 100 nm versus 27 nm in the ethanol/acetonitrile mixture. The fluorescence spectrum of DCM-pyran mixed within Spiro-OMeTAD, with $Li(CF_3SO_2)_2N$ added to the Spiro-OMeTAD to enhance its hole mobility [93–95] then spin-coated onto TiO_2 nanotube films is also broadened, with the emission peak slightly blue shifted. This qualitative information indicates the potential for further enhancement of the spectral overlap integral value and hence a larger Förster radius. Figure 15(b) is an FE-SEM cross-sectional view of a DCM-Spiro-OMeTAD infiltrated SQ-1 dye-sensitized TiO_2 nanotube array film. The presence of FRET in our system was verified by observing the quenching of the fluorescence spectra of DCM-pyran donor molecules, dissolved in ethanol/acetonitrile, with a successive increase of SQ-1 dye concentration.

Starting with device Conc. SOM (30 μL SOM), which contains no DCM, see Table 2 and Figure 16(a), the IPCE is about 10% in the Red/NIR range; diluting the base solution with 15 μL CB, device Dilute SOM (+15 μL CB) shows a doubling of the Red/NIR IPCE to 20%. DCM-containing devices, DCM 10 to DCM 50 and DCM 30–48 mM, exhibit an IPCE of about 30–34% over the peak absorption wavelength corresponding to the SQ-1 dye, with the increase in donor concentration in turn diluting the Spiro-OMeTAD solution. As the 24 mM DCM-pyran solution volume increases from 10 μL to 50 μL, the visible region IPCE increases from 5 to 20%, further increasing to 25% for 30 μL of 48 mM DCM-pyran. The significant broad spectrum IPCE for such a thin-layer device indicates the great utility of FRET in enhancing solar cell efficiency. In comparison, recently phenanthroline ruthenium (II) was used as a phosphorescent energy relay dye in combination with unsymmetrical squaraine-sensitized nanoporous TiO_2 films 2.0 μm thick; the FRET-based contribution to the photocurrent generation in the visible range generated a maximum IPCE of about 8% [11]. With our 500–600 nm long nanotube-based films, we achieve continuous photocurrent generation over a broad spectral range, with the FRET-DCM donor contributed IPCE reaching 25% in the visible range and the acceptor contributed IPCE reaching 30–34% in the Red/NIR.

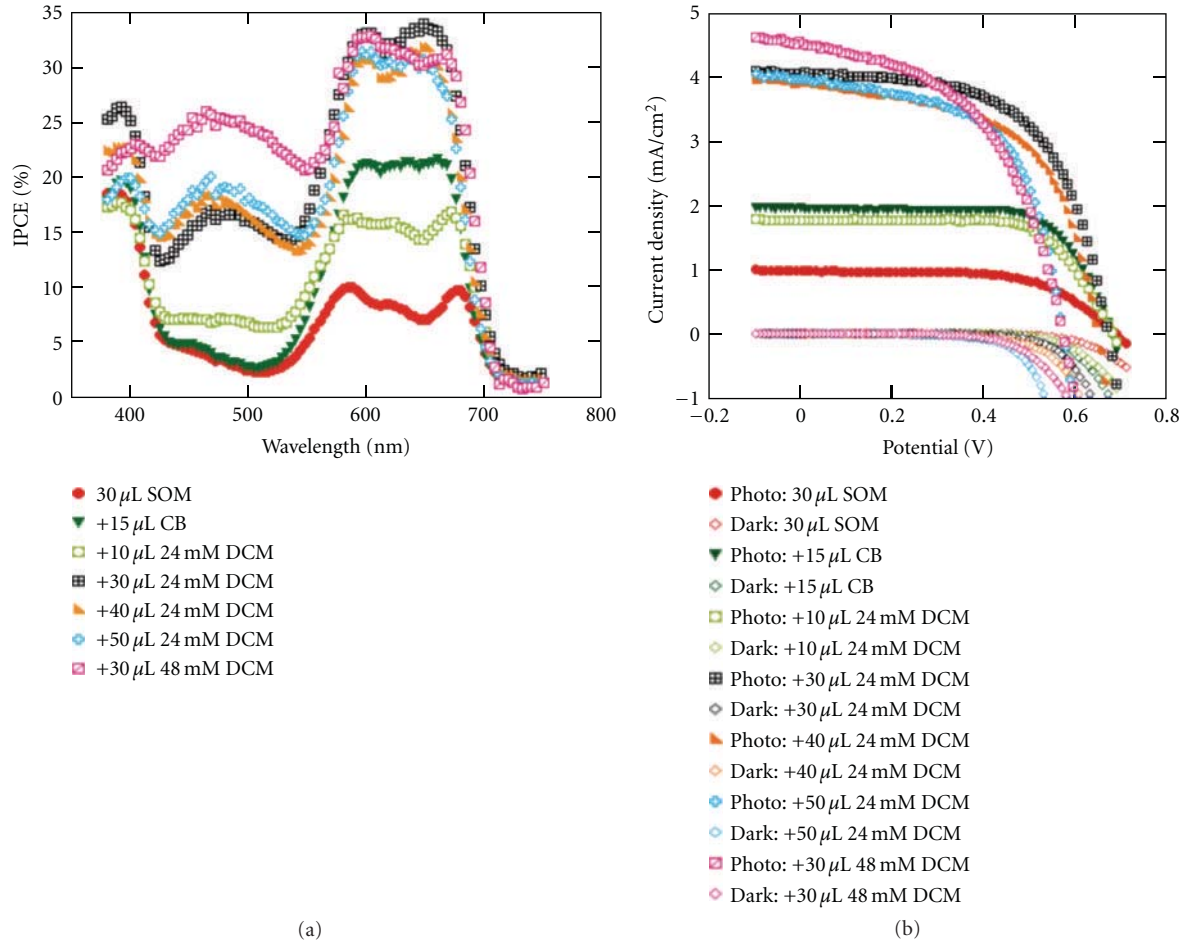


Figure 16: (a) IPCE of FRET-based SS-DSSC devices showing the effect of DCM amount and concentration added to 30 μL Spiro-OMeTAD-blend solution. All solutions were prepared in chlorobenzene. (b) Photocurrent density-Voltage, of FRET-based photovoltaic devices showing the effect of DCM amount and concentration added to 30 μL Spiro-OMeTAD-blend solution. All solutions were prepared in chlorobenzene (CB); the effect of diluting the Spiro-OMeTAD-blend with 15 μL CB is also illustrated. The DCM concentration is 24 mM except where noted. Optimal device performance was achieved with 30 μL of 24 mM DCM-pyran in 30 μL of 0.17 M Spiro-OMeTAD/0.12 M 4-tert butylpyridine/19.5 mM $Li[CF_3SO_2]_2N$, with the resulting (typical) device having a fill factor of 0.67, photovoltage of 0.68 V, J_{sc} of 4.05 mW/cm^2, and power conversion efficiency of 1.64%. Reprinted with permission from [12].

It was suspected that donor molecules near the center of the nanotube are too far from the SQ-1 dye layer, ≈10 to 14 nm, for FRET to occur hence energy is dissipated though fluorescence. However, use of smaller pore nanotubes poses the increased challenge of their uniform filling with the Spiro-OMeTAD solution. This can indirectly be judged by the effect of poor intercalation from the observation of below expected photocurrent generation in device Conc. SOM (30 μL SOM). For device Dilute SOM (+15 μL CB), the improved photocurrent is presumably due to efficient separation of the electron hole pairs photogenerated at the SQ-1 dye layer through the TiO_2 nanotubes and Spiro-OMeTAD, a behavior directly related to improved infiltration of Spiro-OMeTAD inside the nanotube arrays. In contrast, for the same device fabrication procedures, use of an excessively dilute base solution results in an extremely thin overlayer on top of nanotubes, reducing the shunt resistance between the dye-coated TiO_2 and gold electrode. Therefore, the performance of the FRET-based devices should be seen with respect to that of device Dilute SOM.

Figure 16(b) shows the photocurrent density-voltage characteristics of the SS-DSSC devices under 90 mW/cm^2 AM 1.5 G. Device photocurrent density exhibits a rapid increase in addition of up to 30 μL of 24 mM DCM-pyran solution, beyond which the photocurrent is reduced. Device photovoltage remains nearly constant to 40 μL of DCM-pryan solution, thereafter rapidly dropping. A maximum device efficiency η of 1.64% is achieved with a donor concentration of 30 μL of 24 mM DCM-pyran solution, device DCM 30, in 30 μL of 0.17 M Spiro-OMeTAD solution. The increase in device performance is attributed to the increased from 400 to 550 nm IPCE, see Figure 16(a). There is an optimum device composition for maximizing visible region photocurrent over which the photovoltage is not negatively affected. With increasing donor concentration in the base solution, see Table 2, the lithium salt and tert-butylpyridine

Table 2: Device names and their key fabrication details [12].

Device name	Volume of SOM—0.17 M/ Li salt—19.5 mM/ TBP—0.12 M in CB (μL)	Volume of DCM-pyran in CB Concentration—24 mM (μL)	Volume of DCM-pyran in CB Concentration—48 mM (μL)	Volume of CB (μL)	Wetting time before spin coating Sec.
Conc. SOM	30	—	—		60
Dilute SOM	30	—	—	15	90
DCM 10	30	10	—		75
DCM 30	30	30	—		90
DCM 40	30	40	—		120
DCM 50	30	50	—		120
DCM 30–48 mM	30	—	30		90

Note: SOM stands for Spiro-OMeTAD. Li salt for Bis(trifluoromethylsulfonyl)amine lithium salt, 99.95% trace metals basis. TBP for 4-*tert*-Butylpyridine. CB for Chlorobenzene. DCM-pyran for 4-(Dicyanomethylene)-2-methyl-6-(4-dimethylaminostyryl)-4*H*-pyran. Solutions were spin coated on SQ-1 acceptor dye-sensitized TiO_2 nanotubes at 2000 rpm. The 0.02 M $TiCl_4$-treated TiO_2 nanotubes are from 500 to 600 nm in length, and 20 to 28 nm pore size.

concentrations in the Spiro-OMeTAD decrease. It is known that the addition of lithium salt to Spiro-OMeTAD retards the recombination between electrons in the TiO_2 with holes in the Spiro-OMeTAD and increases the Spiro-OMeTAD conductivity [96, 97]. Hence a reduction of the lithium salt concentration in the Spiro-OMeTAD enhances the chances of electron-hole recombination, which in turn lowers the device photovoltage. Personal experience shows that Spiro-OMeTAD cells require a rather precise quantity and quality of lithium salt dopant for efficient performance. Without sufficient tert-butylpyridine to fill vacant sites on the TiO_2 surface, we may expect greater back-injection of electrons into the spiro-OMeTAD manifesting itself as a lower shunt resistance causing a drop in V_{oc}. This behavior is further supported by the performance of device DCM 30–48 mM, where the DCM concentration is doubled in the 30 μL CB solution; although the photocurrent of the resulting device is high, the photovoltage is low with the resulting $\eta = 1.32\%$.

To explore the possibility that diluting the spiro-OMeTAD additives caused our observed drop in V_{oc}, a cell was fabricated using a greater concentration of additives. For comparison, device Dilute SOM had an open circuit voltage of 0.69 V while device DCM 50 had an open circuit potential of 0.58 V. DCM 50 began with a solution of 0.17 M Spiro-OMeTAD in 30 μL chlorobenzene with 0.12 M tert-butylpyridine and 19.5 mM $Li[CF_3SO_2]_2N$ to which 50 μL of 24 mM DCM solution was added. The new test cell began with a solution of 0.17 M Spiro-OMeTAD in 30 μL chlorobenzene with 0.168 M tert-butylpyridine and 27.3 mM $Li[CF_3SO_2]_2N$, to which 50 μL of 24 mM DCM solution was added. By increasing the amount of additives to combat dilution by addition of DCM, the open circuit potential was raised from 0.58 V in DCM 50 to 0.67 V in the new test cell, favorably comparing to the V_{oc} value of 0.69 V in device Dilute SOM.

To help confirm the presence of FRET in our photovoltaic devices, we characterized the performance of device DCM 30, see Table 2, without a SQ-1 dye layer. The IPCE of the resulting device, Figure 17(a), due to electronic transfer of charge from the DCM molecules to the TiO_2 nanotube array surface, is approximately 3.15% in 400–600 nm wavelength range with essentially no photocurrent generation in the Red/NIR. This behavior indicates that the Red/NIR increase in IPCE with use of the DCM-diluted SOM solution is not due to the donor molecules themselves, but to improved infiltration of the DCM-SOM solution into the TiO_2 nanotubes, which increases the SQ-1 to spiro-OMeTAD contact area that in turn enables enhanced extraction of photocurrent from the SQ-1 molecules. The photovoltaic behavior of device DCM 30 fabricated without a SQ-1 dye layer on the TiO_2 surface is shown in Figure 17(b). The absence of the acceptor layer reduces the saturated photocurrent from 4.0 to 0.25 mA/cm^2 with the overall conversion efficiency dropping to $\eta = 0.13\%$. It is experimentally difficult to completely eliminate the possibility of some electronic transition from the DCM to SQ-1 molecules. However, this behavior is suggested by the low photocurrent generation from the TiO_2-DCM device, and the relatively close LUMO positions of the DCM and SQ-1 materials.

To determine the fraction of excited DCM donor molecules that transfer their energy to the SQ-1 acceptor dye-sensitized TiO_2 nanotube arrays, we calculate the excitation transfer energy (ETE) by the following relation [10, 11]:

$$\text{ETE} = \frac{\Delta\text{IPCE}}{\text{IQE} \cdot \eta_{\text{abs, donor}}}. \quad (1)$$

ΔIPCE represents the donor contributed IPCE, IQE is the device internal quantum efficiency, and $\eta_{\text{abs,donor}}$ the fraction of light absorbed by donor. For device DCM 30, the ΔIPCE (at 480 nm) is about 13.57%, $\eta_{\text{abs,donor}}$ (assuming 100% light absorption at 480 nm) is $\approx$62.5%, and IQE $\sim$ 41.6%, for an ETE of 52.2%. For device DCM 30–48 mM, ΔIPCE (at 480 nm) is about 22%, $\eta_{\text{abs,donor}}$ (at 480 nm) is $\approx$80.5%, and IQE $\approx$40.5% for an ETE of about 67.5%.

In FRET-type dye-sensitized solar cells, where Red/IR absorbing acceptor dyes are used to sensitize the TiO_2 and visible light absorbing donor molecules are mixed into the hole transporting spiro-OMeTAD or I^-/I_2, an excitation transfer efficiency (ETE) of up to 90% is needed

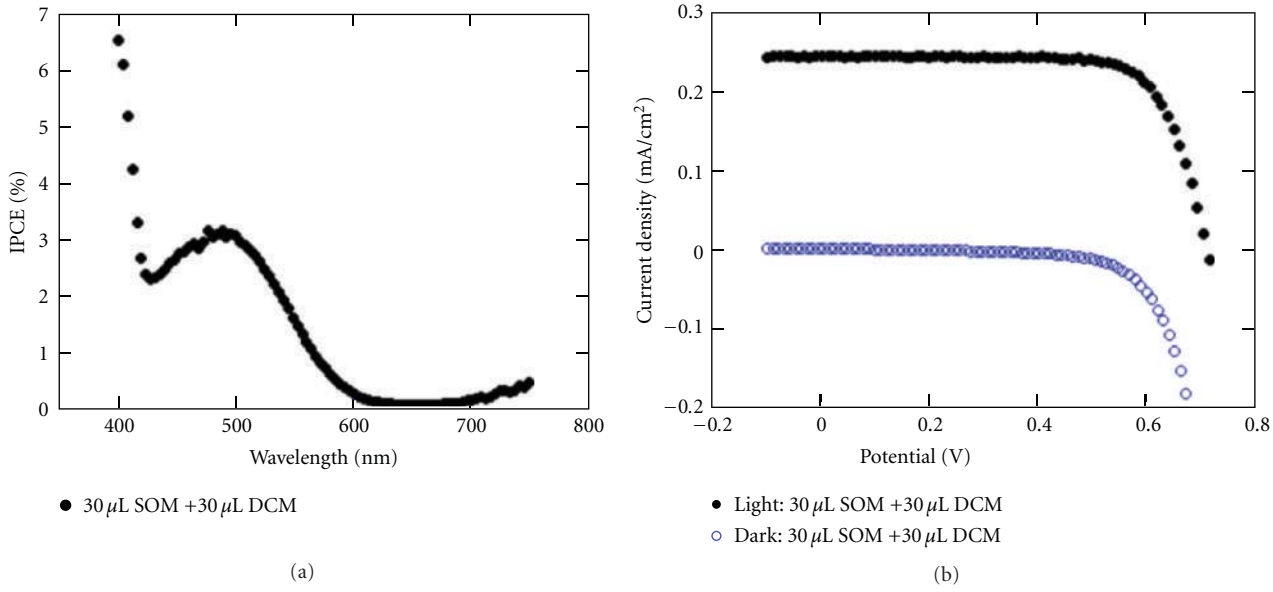


FIGURE 17: (a) The IPCE and (b) Photovoltaic behavior of a DCM 30-nanotube array device without a SQ-1 dye layer. J_{sc} is 0.25 mA/cm^2, V_{oc} = 0.71 V, FF = 0.74, and η = 0.13%. Reprinted with permission from [12].

to achieve record power conversion efficiencies. Recently, Hoke and coworkers analytically determined the ETE from donor to acceptor dyes within cylindrical and spherical pore geometries, correlating the ETE to the critical energy transfer distance (R_c) and the pore diameter [98]. They determined R_c by the following relation:

$$R_c = \left[\frac{C_A R_0^6}{1 + \tau_0 \sum_j k_{qj} \left[Q_j \right]} \right]^{1/4}. \quad (2)$$

R_o is the Förster radius, C_A is surface coverage concentration, τ_0 is the donor lifetime in the absence of a quencher, Q_j is the concentration of quenching species j, and k_{qj} is the bimolecular quenching coefficient for the donor-quencher combination.

For stationary donor and acceptor dyes within a cylindrical pore, achieving a 90% ETE requires an R_c equal to or greater than 0.3 of the pore diameter [98]. For an average 24 nm TiO_2 nanotube pore size, this implies that R_c should be greater than 7.2 nm. Assuming an SQ-1 dye surface concentration of 0.6 dye/nm^2, values from 0.2 to 1 dye/nm^2 have been reported [99], the calculated Förster radius of 6.1 nm, a DCM fluorescence lifetime of 1.6 ns [100], and approximating the $k_{qj}[Q_j]$ value as 10^9 M^{-1}s^{-1} [101], R_c is calculated to be 5.11 nm. Referring to Figure 2(c) of [98], such properties should result in an ETE value of approximately 70%, a value in excellent agreement with our 67.5% calculated ETE value.

3.3.2. FRET in Liquid-Junction DSSCs Using TiO_2 Nanowires. Shankar et al. demonstrated that an enhancement in photovoltaic device performance is possible using long-range resonance energy transfer from a dissolved luminescent dopant confined in the interstices of a nanowire array electrode to an acceptor species confined to the surface of the nanowires [9]. Shankar reported the use of FRET to boost the quantum yield for red photons at 675 to 680 nm by a factor of 4 for N-719 and a factor of 1.5 for black dye [9]. Figure 18 shows the optical properties of the dyes used. Phthalocyanines (traditionally acceptors) as energy donors and nonfluorescing ruthenium polypyridine complexes as acceptors were used. The bis(bipyridine) and terpyridine ruthenium complexes already have broad absorption in the visible region of the spectrum and excellent charge transfer characteristics, thus establishing a high baseline of light harvesting. The choice of phthalocyanines was driven by three considerations: light absorption, solubility, and aggregation. Zinc 2,9,16,23-tetra-*tert*-butyl-29*H*,31*H*-phthalocyanine (ZnPc-TTB) was chosen because the four tertiary butyl groups attached to the ZnPc core disrupt the formation of π-π stacking structures thereby reducing aggregation. Figure 18 presents the absorption and emission spectra of ZnPc-TTB, along with the absorption spectra of ruthenium polypyridine complex dyes. There is a significant overlap between the emission spectrum of ZnPc-TTB and the absorption spectrum of N-719, while for the donor and acceptor pair of ZnPc-TTB and black dye, the emission spectrum of the donor is completely contained within the absorption spectrum of the acceptor. The emission of ZnPc-TTB was found to quench by dilute solutions of N-719 and black dye, a necessary condition for FRET [9].

A key requirement for FRET is that the physical separation of the donor and acceptor species be close to the Förster radius for the donor-acceptor system. For this, 6 to 8 μm long extremely close-packed rutile TiO_2 nanowire array substrates, with an interwire spacing of 5 to 10 nm, were used. The acceptor dye molecule is anchored to the surface of the nanowires. Due to the confinement of

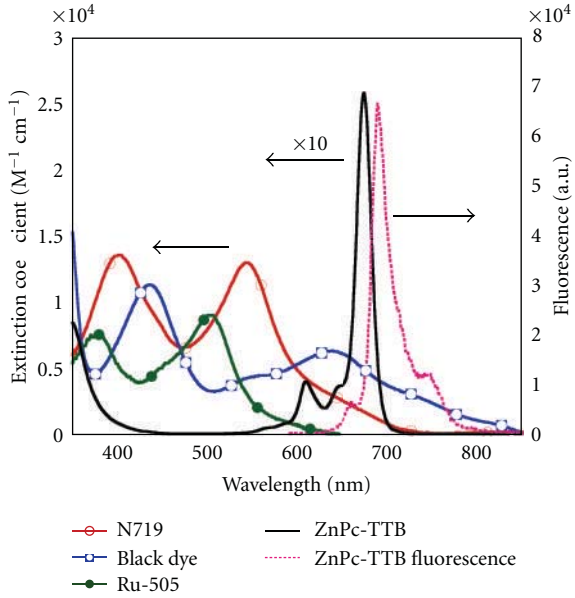


Figure 18: Absorption spectra of donor and acceptor dyes and emission spectrum of phthalocyanine donor. For display purposes, 0.1 times the extinction coefficient of ZnPc-TTB is shown. Reprinted with permission from [9].

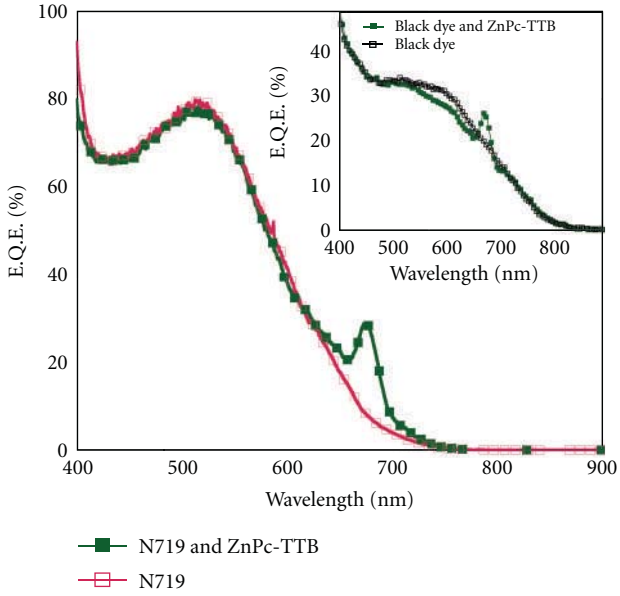


Figure 19: Action spectrum of nanowire solar cell comprising N-719-coated rutile as acceptors, with and without ZnPC-TTB molecules in electrolyte as the donors. Inset shows action spectrum for black-dye-coated rutile acceptors with and without ZnPc-TTB donors. Ten percent of data points are shown. Reprinted with permission from [9].

the liquid electrolyte in the nanowire array interstices, a large number of donor dye molecules dissolved in solution are effectively within a Förster radius of the acceptor molecules, thus facilitating energy transfer between donor and acceptor molecules. However, energy transfer in this device architecture of solution-based donors and surface-confined acceptors can be better represented by a system consisting of energy transfer from a donor chromophore to a two-dimensional sheet of acceptors at a distance d. For this geometry, Kuhn showed that the rate of energy transfer follows the inverse fourth power of the interchromophoric distance [103].

In this device configuration, ZnPc-TTB molecules were introduced directly into the tri-iodide redox electrolyte at a (high) concentration of 1–5 mg/mL. As seen in Figure 19, a dramatic increase in the quantum yield for red photons in the spectral region of 670–690 nm was immediately observed, over and above the quantum yields exhibited by N-719 and black-dye-sensitized nanowire solar cells. N-719 dye forms a nonagglomerated monolayer [104]. Since black dye agglomerates, coadsorption of deoxycholic acid was employed to form the black dye coating and reduce agglomeration [105]. The dilution of black dye in the monolayer reduced the concentration of acceptors available for energy transfer and resulted in lower critical distance and lower energy transfer efficiencies for black dye relative to N-719 despite the higher spectral overlap of black dye absorption with the emission spectrum of ZnPc. Resonance energy transfer of excitons generated in ZnPc-TTB molecules from red photons to surface bound N-719 dye results in a fourfold enhancement of quantum yield at 675 to 680 nm. Since the extinction coefficient of ZnPc-TTB molecules in the spectral region of 670−690 nm is far greater than that of N-719, we believe the entire quantum yield of 28% at the donor absorption maximum is attributable to FRET and is close to the measured fluorescence quantum yield of ZnPc-TTB in solution [106]. At the high concentrations used, zinc phthalocyanine forms multimolecular aggregates with a reduced quantum yield due to concentration quenching. A self-sieving effect of the nanowires admitting only monomeric and dimeric forms into the interwire spaces may account for the nearly quantitative efficiency of energy transfer from ZnPC-TTB in solution to surface-anchored N-719 and black dye molecules, a hypothesis supported by the saturation of the external quantum yields for red photons at values close to the fluorescence quantum yield of the donor.

3.4. Liquid-Junction DSSCs. The building blocks of these solar cells are a photoanode consisting of high surface area TiO_2 anatase nanoparticle film (thickness ~10 μm) on transparent conducting oxide (TCO) glass, upon which the illumination is incident, supporting a monolayer of a light absorbing chromophore, an iodide electrolyte, and a platinum-coated TCO glass counter electrode. High efficiency DSSCs are commonly achieved with the help of a 4 μm thick layer of TiO_2 particles, approximately 400–800 nm in diameter, atop the transparent photoanode to scatter red and near-infrared wavelengths so as to enhance absorption by the dye molecules [107, 108].

The excitons generated in the dye (normally a ruthenium polypyridyl complex) as a result of light absorption are instantaneously split, with electrons injected into the nanoparticle film and holes released to oxidize iodide

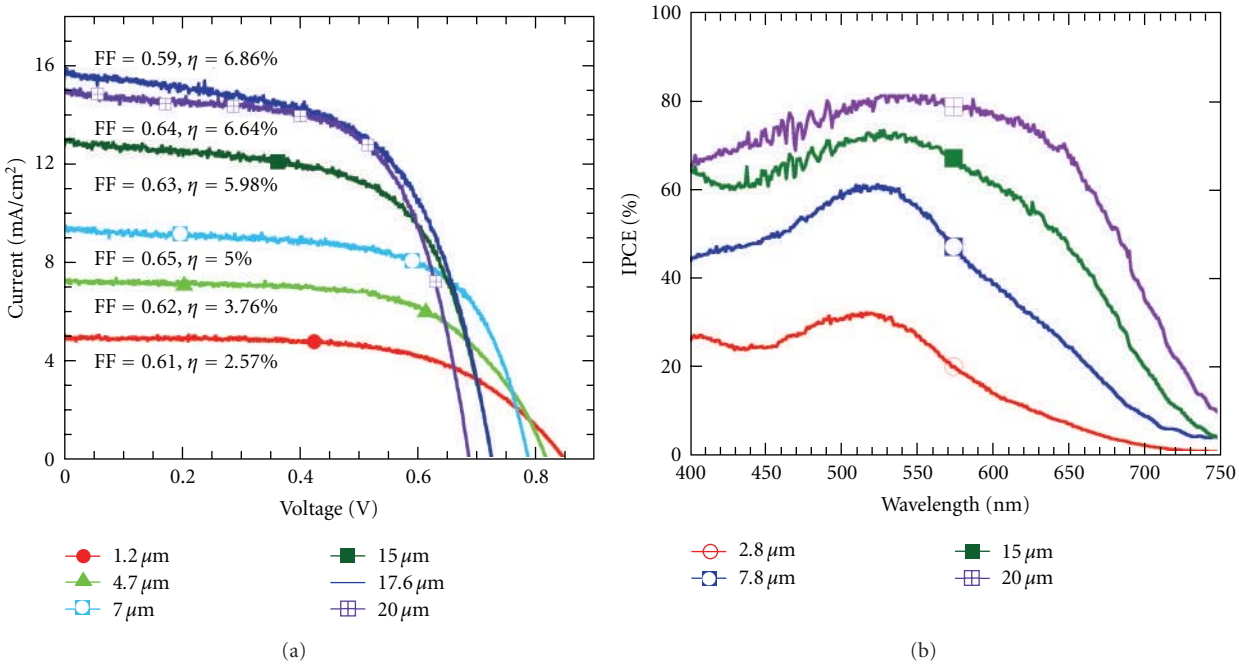


FIGURE 20: (a) Current-voltage characteristics of DSSCs fabricated using transparent nanotube array films of various lengths. The pore size of the 1.2 μm film was 58 nm, while it was 95 nm for the rest of the films. The 20 μm long nanotubes were fabricated from a 12 μm thick Ti film. (b) The IPCE spectra of DSSCs fabricated using transparent nanotube array films of various lengths. Reprinted with permission from [35].

species in the electrolyte. The electrons diffuse through the nanoparticle network and are collected at the TCO. The electrons, while percolating through the randomly oriented nanoparticle network, undergo many trapping and detrapping events at defect states before combining with oxidized electrolyte species or reaching the TCO layer. The electron diffusion length of these films, as determined using intensity-modulated photovoltage and photocurrent spectroscopies (IMVS and IMPS, resp.), is in the range of 10–30 μm [109]. Hence an increase in the nanoparticle film thicknesses significantly above 10 μm, in order to absorb low energy photons (red and near-infrared wavelengths) that are weakly absorbed by commonly used ruthenium bi or terpyridyl complexes, does not generally result in an increase of the photoconversion efficiency. The potential for future increases in DSSC efficiency relies largely on the invention of new dyes, ideally those offering large extinction coefficients and broad spectrum absorption, and on the development of highly ordered material architectures offering longer electron diffusion lengths and shorter electron transport time constants than those in conventional randomly oriented nanoparticle films. With this as motivation, other wide bandgap oxide semiconductors and different architectures have been investigated as alternatives to the nanoparticle films [24, 110, 111].

3.4.1. Short and Long TiO_2 Nanotubes. A promising nanoarchitecture for solar energy conversion within a DSSC is an array of highly ordered, vertically aligned TiO_2 nanotubes grown by anodic oxidation of titanium [54, 112] offering electron transport properties superior to films comprised of randomly oriented TiO_2 nanoparticles. Zhu et al. have shown that (back side illuminated) dye-sensitized solar cells, fabricated using TiO_2 nanotube arrays grown on titanium foil, have a charge collection efficiency 25% higher, and a light harvesting efficiency 20% higher, than corresponding nanoparticle-based DSSCs [28]. The higher light harvesting efficiency has been attributed to the enhanced light scattering properties of the TiO_2 nanotube arrays. In a more recent work, Jennings and coworkers estimated the electron diffusion length in TiO_2 nanotube arrays on titanium foil by considering the electron diffusion coefficient and life time as a function of electron quasi-Fermi level and obtained a value of 100 μm, which is at least 3× better than that in the case of nanoparticle film-based DSSCs [29]. Thus TiO_2 nanotube-array-based DSSCs offer the prospect of photoelectrodes having much greater thicknesses without a corresponding decrease in performance due to unwanted charge recombination. Thicker photoelectrodes would enable the harvesting of low energy photons using either a single dye, or different dyes covering different regions of the nanotube length, with a dye sensitive to shorter wavelengths at the illuminated end of the film, and a dye sensitive to longer wavelengths at the other.

The current-voltage characteristics of dye-sensitized solar cells fabricated using TiO_2 nanotubes of length up to 20 μm are shown in Figure 20(a). The DSSC employing 17.6 μm long nanotubes, fabricated from 20 μm thick Ti films yielded a power conversion efficiency of 6.9% (V_{oc} = 0.73 V, J_{sc} = 15.8 mA/cm^2 and FF = 0.59). In comparison, in high efficiency nanoparticle DSSCs (power efficiency 10-11%)

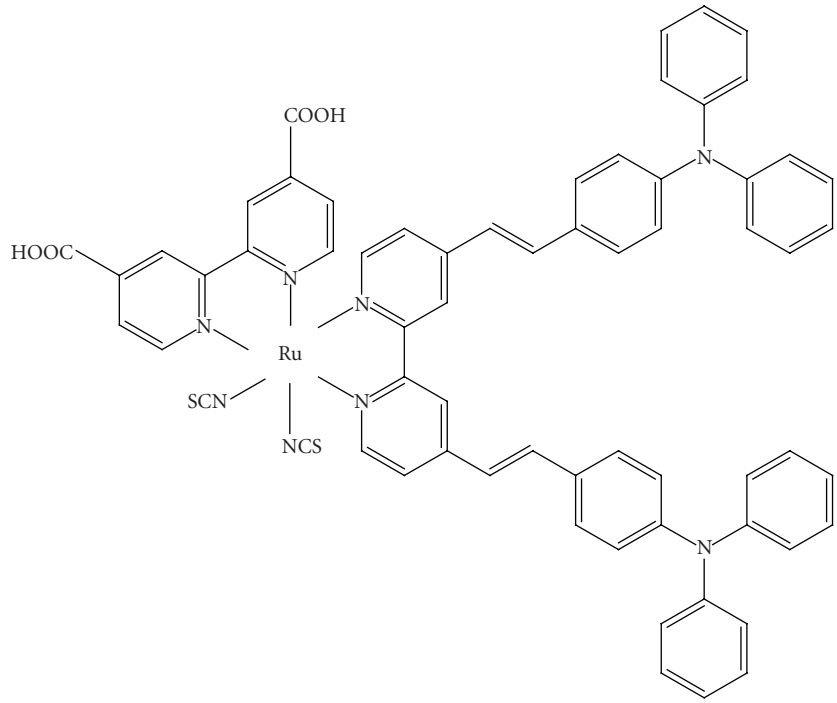


Figure 21: Molecular structure of Ru-TPA-NCS. Reprinted with permission from [102].

fabricated under highly optimized conditions (e.g., using highly purified dyes, nanoparticle scattering layer, etc.), the J_{sc} is about 17-18 mA/cm^2, the fill factor is close to 0.75, and V_{oc} is 0.7–0.85 V [107, 108]. Considering that we used commercially available N719 dye without further purification and that the roughness factor was slightly lower, about 900 for 20 μm long nanotubes versus over 1000 for nanoparticle films of thickness 10–12 μm, the J_{sc} value obtained is remarkable. The major factor that limits the power efficiency of nanotube-array DSSCs is their low fill factor, about 25% lower than their nanoparticle counterparts. This is largely due to an increase in the width of the TiO_2 nanotube array-FTO interfacial layer, which occurs during annealing of the nanotube array samples as required for crystallization and to oxidize trace metal particles within the nanotube film. Higher efficiencies should be possible with elimination of this problem and using nanotubes of greater roughness factor-that is, smaller pore diameter and/or greater lengths.

Figure 20(b) shows the IPCE spectra obtained from nanotube array DSSCs. The IPCE is as high as from 70 to 80% in a wide wavelength range (450 to 650 nm) and has a significant magnitude up to 700 nm. The projection of the shoulder in the wavelength region above 600 nm with increasing nanotube length shows efficient conversion of low energy photons without the need of a scattering layer as used in high efficiency nanoparticle DSSCs [107, 108]. The IPCE spectrum of the DSSC employing 20 μm long nanotubes closely follows the transmittance spectrum of the TEC 8 glass substrate. The loss due to light absorption at 500 nm by the electrolyte trapped in the pores is ~1% (estimated from electrolyte absorbance), which is lower at higher wavelengths. Thus the internal quantum efficiency of the device approaches 95–100% in this wavelength region; that is, about 95–100% of the absorbed photons having energy in this region are converted into electrons in the external circuit even though the thickness of the nanotube film is twice that of nanoparticle films used in high-efficiency DSSCs. This clearly shows that DSSCs can effectively employ nanotubes of still greater lengths; however, making such long tubes is a great challenge.

3.4.2. TiO_2 Nanotubes and Donor Antenna Dyes. The donor-antenna dye *cis*-di(thiocyanato)(2,2′-bipyridyl-4,4′-dicarboxylic acid)-(2,2′-bipyridyl-4,4′-bis(vinyltriphenyl amine) ruthenium(II) (named as Ru-TPANCS) contains the electron-rich donor triphenylamine linked to the bpy by a conjugated vinyl spacer. The molecular structures of the Ru-TPA-NCS donor-antenna dye and the commercially available N-719 dye (Solaronix) are shown in Figure 21, respectively. The extended π electron delocalization in the bpy ligand enables the donor-antenna dye molecules to have high molar extinction coefficients, more than twice that of the commonly used N-719 dye [113]. Furthermore, unlike in N-719, the HOMO of Ru-TPA-NCS are spread over the triphenyl amine moieties [114, 115]. The increased separation of the HOMO levels from the TiO_2 surface has been shown to retard the recombination process at the TiO_2-dye interface and at the TiO_2-hole conductor interface in solid-state solar cells [116]. The procedures for the synthesis of the donor-antenna dye are detailed elsewhere [116].

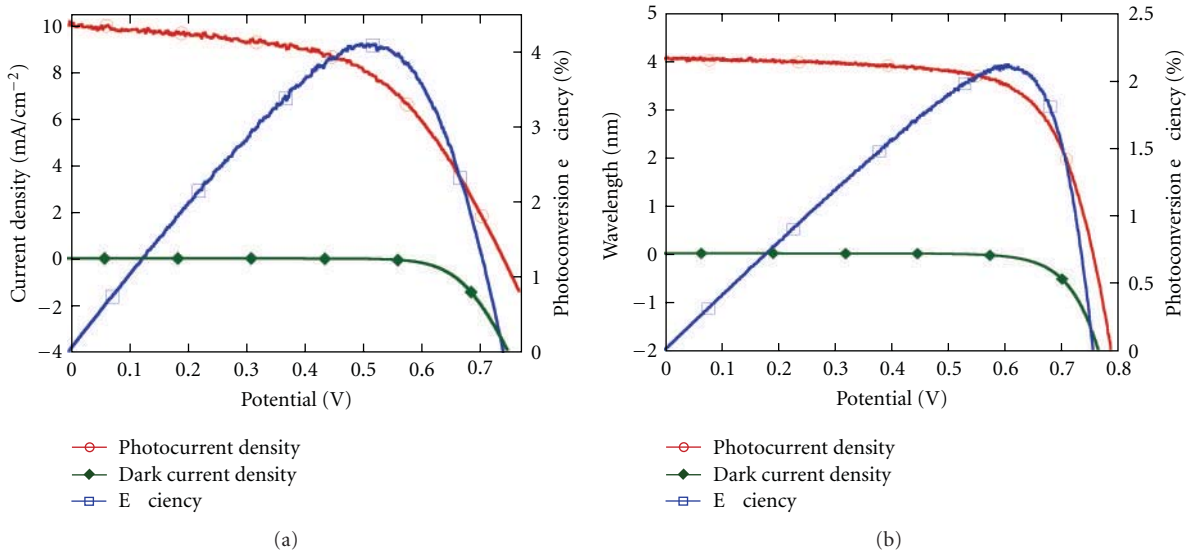


FIGURE 22: (a) Current-voltage characteristics of frontside illuminated solar cells with Ru-TPANCS-sensitized 1 μm long $TiCl_4$-treated TiO_2 nanotube array under 1 sun AM 1.5 illumination. (b) AM 1.5 current-voltage characteristics of a $TiCl_4$-treated 1 μm long transparent nanotube array with N-719. Reprinted with permission from [102].

The donor-antenna dye Ru-TPA-NCS exhibits 4-5 times higher molar extinction coefficient than N-719 at 400 nm [113]. Because of the much higher molar extinction coefficient of the Ru-TPA-NCS dye, a much lower film thickness should suffice to harvest a similar amount of incident photons. Shankar et al. employed vertically oriented TiO_2 nanotube arrays in conjunction with the Ru-TPA-NCS donor-antenna dye to fabricate liquid-junction dye-sensitized solar cells [102]. It was noted that the TiO_2 NT array electrode sensitized with Ru-TPA-NCS dye has higher optical absorption than the N-719-coated sample across the entire solar spectrum with an absorbance more than twice that of the N-719 dye at 470 nm, which corresponds to the wavelength of maximum irradiance in the solar spectrum. Front side illumination was employed using 1 μm long transparent nanotube arrays, with an average pore diameter of 100 nm, on FTO-coated glass [72]. The $TiCl_4$-treated transparent nanotube arrays were sensitized with Ru-TPA-NCS dye and used to fabricate solar cells, whose I-V characteristics are shown in Figure 22(a). With transparent nanotube arrays, the commercially available redox electrolyte MPN-100 (Solaronix) containing 100 mM of tri-iodide in methoxypropionitrile was used. Figure 22(a) shows that a 1 μm long TiO_2 nanotube array yields a short circuit photocurrent density of 10.1 mA/cm^2, an open circuit potential of 743 mV, and a fill factor of 0.55 resulting in an overall conversion efficiency of 4.1%. Figure 23(b) presents the performance of a similar solar cell constructed by sensitizing a $TiCl_4$-treated 1 μm long transparent nanotube array with N-719. While the use of N-719 results in slightly larger values of the open circuit potential, the short circuit photocurrent density J_{sc} is nearly half that obtained with Ru-TPA-NCS sensitization because of the smaller amount of light harvested.

3.4.3. TiO_2 Nanowire Arrays. Rutile TiO_2 nanowire array samples were sensitized with a monolayer of dye by immersion overnight in a 0.5 mM N719 solution. A liquid-junction solar cell was prepared by infiltrating the dye-coated TiO_2 electrode with commercially available redox electrolyte MPN-100 (Solaronix) containing 100 mM of tri-iodide in methoxypropionitrile. A conductive glass slide sputter-coated with 100 nm of Pt was used as the counter-electrode. Electrode spacing between the nanowire and counter-electrodes was assured by the use of a 25 μm thick SX1170 spacer. Photocurrent density and photovoltage of the prepared DSSCs were measured with active sample areas of 0.4-0.5 cm^2 under AM-1.5 G simulated sunlight.

Figure 23(a) shows the J-V characteristics of a typical 2-3 μm nanowire length sample grown directly on the FTO-coated substrate. An overall photoconversion efficiency of 4.35% was achieved (V_{oc} = 0.758 V, J_{sc} = 10.2 mA/cm^2, and FF = 0.56). Table 3 includes statistical data related to the performance of solar cells comprising nanowire arrays of different lengths. By using the same batch of N-719 dye, the same redox electrolyte, and similar active areas, we sought to isolate the effect of nanowire length on device performance. Normally, the surface area and hence the dye adsorbed increases as a function of length because of which an increase in solar cell performance with nanowire length is expected. However, here it was observed that wires 2-3 μm long exhibited the best performance with an average efficiency of 4.83%, with decreasing performance seen for longer nanowires. This can be understood within the context of nanowire array formation. Longer nanowire arrays result when the duration of the hydrothermal growth is extended; the longer times cause an increase in the lateral dimension as well as the axial dimension of the nanowires. An increase in nanowire width decreases the packing density per unit area of

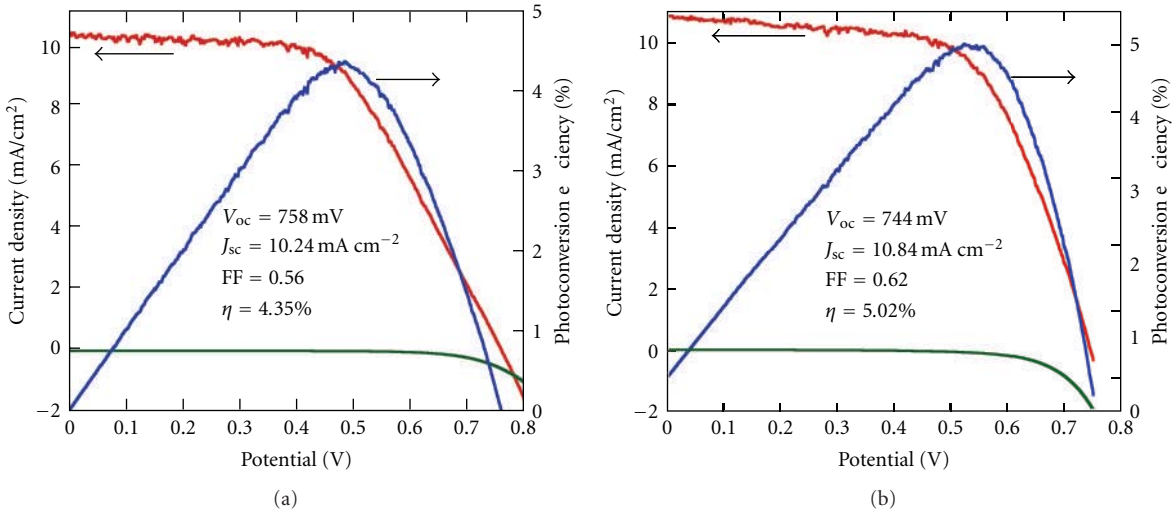


Figure 23: Photocurrent density, dark current density, and power density of 2.0 μm long rutile TiO_2 nanowire-array-based dye-sensitized solar cells under AM 1.5 illumination (100 mW/cm^2): (a) unmodified nanowire array grown directly on TCO substrate and (b) a $TiCl_4$ treatment is used to coat the TCO substrate prior to nanowire array growth and a $NbCl_5$ treatment used on the nanowires prior to device assembly. Reprinted with permission from [24].

Table 3: Statistics of TiO_2 nanowire arrays dye-sensitized solar cells showing the mean (μ), and standard deviation (σ) of the solar cell parameters: Short Circuit Photocurrent Density (J_{sc}), Open Circuit Voltage (V_{oc}), Fill Factor, and Efficiency (η) [102].

Length of nanowires (μm)	Typical nanowires width (nm)	No. of devices	μ_{Jsc}	σ_{Jsc}	μ_{Voc}	σ_{Voc}	μ_{ff}	σ_{ff}	μ_{η}	σ_{η}
2-3	10–15	6	10.3	2.52	751	36	0.57	0.05	4.34	1.09
3-4	20–25	6	8.47	1.06	742	21	0.6	0.05	3.75	0.39
4-5	30–35	10	7.29	2.29	769	19	0.62	0.04	3.39	0.85

the nanowire arrays, which results in lower effective internal surface area available for dye adsorption despite the higher length. It was also noted that the extended reaction times, corresponding to nanowire arrays longer than 4 μm, weaken the nanowire-FTO interface, with the resulting samples demonstrating poorer photoelectrochemical properties.

The device photoconversion efficiency could be improved in the following manner. To improve the fill factor, after the TiO_2 nanowire growth, an overlayer of niobium oxide was subsequently coated onto the nanowires, which was found to improve the efficiency by reducing recombination [117, 118]. To form the Nb_2O_5 coating, the prepared nanowire samples were dipped in a 5 mM $NbCl_5$ dry ethanol solution, then heated in air at 500°C for 0.5 h [118]. Figure 23(b) shows the J-V characteristics of a typical 2-3 μm long Nb_2O_5-treated nanowire array device under AM 1.5 illumination. An overall photoconversion efficiency, after much work, of 5.02% was achieved (V_{oc} = 0.744 V, J_{sc} = 10.84 mA/cm^2, and FF = 0.62).

We note that in spite of their superior charge transport characteristics, 20 μm long ZnO nanowire arrays exhibit relatively low efficiencies when used in dye-sensitized solar cells due to poor dye adsorption [110]. We attribute our much higher light-to-electricity conversion efficiency achieved using rutile TiO_2 nanowire arrays to the ability of the dye to anchor on the (110) crystal plane, which is both stable and has a strong interaction with carboxylate groups of the N719 dye molecule [119]. In contrast, the acidic carboxylate groups of the dye dissolve the outer layer of the ZnO surface forming a Zn^{2+}-dye complex layer [120, 121], which in turn weakens the interaction of the dye with the electrode surface. Solar cells comprising 2 μm long rutile nanowires exhibit higher efficiencies than rutile nanoparticulate films thicker than 5 μm [122]. Efficient vectorial charge transport, enabled by the single crystal nanowires, leads us to believe that significantly higher efficiencies can reasonably be expected through solution of the interface problem and nanowire-bunching presently seen in rutile TiO_2 nanowire arrays longer 4 μm, which would enable greater light absorption without a corresponding penalty in charge transfer capabilities. Of course, the ability to synthesize self-assembled, single-crystal, vertically oriented anatase nanowires directly onto a transparent conductive oxide-coated substrate, without damage to the substrate, would be a tremendous step-forward in the dye-sensitized solar cell field.

4. Conclusions

We have reviewed the fabrication of self-assembled vertically oriented 1D TiO_2 nanostructures such as nanotube/nanowire arrays and their application in various excitonic solar cells such as bulk heterojunction, ordered heterojunction, FRET-type solid-state and liquid-based DSSCs. Self-organized and vertically oriented TiO_2 nanotube arrays

were grown on FTO glass by anodic oxidation of thin/thick Ti films in fluoride ions containing DMSO or EG-based organic solvents. A small amount of water is added in the solution to obtain debris-free nanotube arrays. Small pore size nanotubes, necessary for high surface area films, are possible in shorter length tubes; the pore size increases if we need longer length tubes which require greater anodization voltages. It was shown that transparent TiO_2 nanotube arrays films on transparent conducting oxide glass could be fabricated with lengths between 0.3 and 33.0 μm. Short nanotube array films showed strong antireflection properties, while films of longer nanotube arrays suffered from imperfect light transmission properties due to residual metal atoms. In liquid-junction DSSCs comprised of 17.6 μm long TiO_2 nanotubes coated with N719 dye, a photoconversion efficiency of 6.9% was obtained, with an IPCE of 70 to 80% between 450 and 650 nm.

In bulk heterojunction solar cells, short length tubes (270 nm long and 50 nm pore size prepared by anodization in aqueous HF bath) were filled with a P3HT + PCBM mixture to achieve a photoconversion efficiency of about 4.1%. Given the hydrophilic nature of TiO_2, the hydrophobic nature of P3HT, and the relatively small pore size (~35 nm) of 700–800 nm long, nanotubes infiltration of this blend into the nanotube array pores was difficult. Various organic solvents were used to change the surface wetting properties before polymer filling. Further, these solvents were required to mix well with the polymer blend and then evaporate during the spin-coating process. With such solvents, we achieved greater percolation of the P3HT/PCBM blend inside the nanotube arrays; however, this process appears to change the configuration of the polymer chain leading to a reduction in the device photovoltage.

In fabrication of ordered heterojunction solar cells, an organic dye was anchored to the TiO_2 as an intermediate layer to promote electronic transitions, and to broaden the spectral absorption band with the SQ-1 dye absorbing Red/NIR light and P3HT absorbing in the visible. The HOMO-LUMO levels of the dye and polymer, and the conduction band level of TiO_2 are such that the electrons flow towards the TiO_2 while holes are transported to the opposite electrode. Without the use of fullerene derivatives, we achieved a photoconversion efficiency of approximately 4%.

In FRET-type solar cells, we filled the empty space, normally used for filling with redox electrolyte in liquid-junction DSSCs, in dye-sensitized TiO_2 nanotube arrays with a blend of spiro-OMETAD and DCM (visible light absorbing molecules). To achieve FRET, it is necessary for the DCM photoluminescence to significantly match with the spectral absorption of the anchoring SQ-1 dye. The DCM donor molecules contributed a FRET-based maximum IPCE of 25%. An excitation transfer efficiency of about 67.5% was achieved and a 76% increase in the photoconversion efficiency in our optimal devices. In liquid-based DSSCs, using Förster-type resonance energy transfer from zinc phthalocyanine donor molecules to ruthenium polypyridine complex acceptors results in a fourfold increase in quantum yields for red photons in dye-sensitized nanowire array solar cells. The spatial confinement of the electrolyte imposed by the wire-to-wire spacing of the close-packed nanowire array architecture ensures that the distances between a significant fraction of donors and acceptors are within a Förster radius.

Acknowledgment

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Review Article

Probing Phonons in Nonpolar Semiconducting Nanowires with Raman Spectroscopy

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We present recent developments in Raman probe of confined optical and acoustic phonons in nonpolar semiconducting nanowires, with emphasis on Si and Ge. First, a review of the theoretical spatial correlation phenomenological model widely used to explain the downshift and asymmetric broadening to lower energies observed in the Raman profile is given. Second, we discuss the influence of local inhomogeneous laser heating and its interplay with phonon confinement on Si and Ge Raman line shape. Finally, acoustic phonon confinement, its effect on thermal conductivity, and factors that lead to phonon damping are discussed in light of their broad implications on nanodevice fabrication.

1. Introduction

Since the discovery of the Raman scattering process by Raman and Krishnan in 1928 [1] and the invention of the laser in 1960 by Maiman [2–4], Raman spectroscopy has morphed from standard macroprobe of bulk materials to single molecular detection [5–11]. The innovations in Raman spectroscopy have made it one of the most widely used techniques to probe nanostructures, beside transmission electron microscopy (TEM), scanning electron microscopy (SEM), X-ray diffraction (XRD), and atomic force microscopy (AFM) as shown in Figure 1. The data in Figure 1 was collected from the ISI web of science site for the period of January 1996 to July 2010 on nanoscale characterization tools used in probing nanostructures [12]. Even though probing individual nanostructures by Raman spectroscopy at nanoscale is limited by its low spatial resolution (diffraction limit of the objectives), recent developments in nano-Raman spectroscopy, including scanning near-field optical microscopy (NSOM), tip enhanced Raman spectroscopy (TERS), and surface enhanced Raman spectroscopy (SERS), have made single-molecule detection possible [5–11, 13–17], especially using SERS and TERS. While NSOM is based on the principle of optical tunneling of evanescent waves, TERS and SERS are based on excitation of surface plasmons on the surface of nanometals. The process arises when free electrons on the surface of a metal oscillate collectively in resonance with the oscillating electric field of the incident light wave. The interaction between the surface charge and the electromagnetic field helps concentrate the light on the surface of the metal, leading to electric field enhancement. Irrespective of such great innovative techniques in nano-Raman spectroscopy, nearly 84% (see Figure 1) of Raman characterization use conventional Raman spectroscopy to probe nanoscale samples [12]; that is, probing ensembles of nanostructures instead of individual nanostructures.

The dramatic surge in the use of Raman spectroscopy in probing nanostructures is mainly due to the immense information (such as amorphization, defects, sample temperature (local heating), size distribution, strain effects, phonon confinement, type of doping, phase separation, carrier concentration, and mobility) [24–38] that can be readily acquired

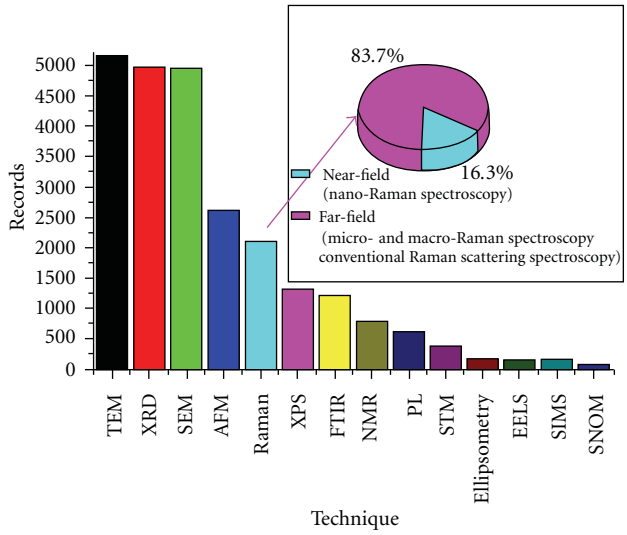


FIGURE 1: Number of records of the listed nanocharacterization tools used in probing nanostructures in the period of January 1996 to July 2010 (Source: ISI Web of Science, http://apps.isiknowledge.com/) [12].

from analysis of the peak-frequency and line width of the Raman profile. Additionally, (i) the nondestructive nature of the Raman probing technique, (ii) limited or no sample preparation, (iii) simultaneous *in situ* measurement, (iv) submicron spatial resolution when coupled with AFM (TERS) or SEM, and (v) very high sensitivity when coupled with surface enhanced/resonance spectroscopy have made Raman spectroscopy an easy-to-use instrument for quick sample screening. Thus, Raman spectroscopy has been used extensively to probe optical phonons, surface phonons, acoustic phonons, and antenna effects in nanowires.

In this paper, we concentrate on recent developments in optical and acoustic phonon confinement in nonpolar semiconducting nanowires, using Si and Ge; as examples, since many of the concepts that we discuss here are applicable to any related systems. Other phenomena in nanowires such as antenna effects and surface phonons are not covered here. In this chapter, we will review optical and acoustic phonon properties using Si and Ge nanowires as prototype and the new phonon dispersion due to radial (circumferential) confinement. Additionally, we will review physical properties such as thermal conductivity that are significantly influenced by phonon confinement.

Our understanding of the bulk properties of crystalline and amorphous Si and Ge continue to be of immense importance to the development of electronic, optoelectronic, photovoltaic, and other devices, as well as the society at large. The past two decades have seen scientific advances in low-dimensional systems by reducing the three-dimensional bulk system (3D) to two-dimensional thin-film systems (2D) to one-dimensional and quasi-one-dimensional (1D) systems of nanowires and nanotubes [39–64] and to zero-dimensional (0D) systems of quantum dots [39–41].

Following the growth of nanowires using pulsed laser vaporization in 1998, different synthesis techniques have been developed using the vapor-liquid-solid mechanism (VLS) [65–79]. These have led to intense research activities due to the unique properties of the nanowires compared to their bulk counterparts, and several applications of nanowires including sensors, transistor and logic gates, electrooptics, thermoelectric, photovoltaic, electrochemical capacitors, and batteries have been proposed. Most of these applications take advantage of quantum confinement effects at small diameters, which for Si and Ge occur at diameters $\leq$20 nm [44–47, 80]. Both theoretical [81–84] and experimental [83, 85–88] evidence of the effects of confinement on the electronic states of nanowires have been reported for Si and other nanowires [89–91]. These reports indicate a transition from indirect band gap to direct band gap in the nanowires where the band gap scales with diameter as $\sim D^{-1.7}$ [83, 84, 88, 92, 93]. Most studies of nanowires have focused on the electronic states; however, the importance of phonon states in nanowires cannot be overemphasized. Most of the electronic properties are intricately influenced by phonon scattering since it is the dominant scattering mechanism at high temperatures. The influence of phonon confinement, geometry, and surface roughness of nanowires on thermal conductivity, specific heat capacity, and electron mobility has been demonstrated theoretically and experimentally [94–101]. Different confinement models including lattice dynamic simulation [102] and spatial correlation (phenomenological) [12, 44–47, 80, 103–111] model have been used to calculate phonon dispersion and Raman line shape profiles of nanowires, respectively. We will discuss the phenomenological model later. However, readers who are interested in the lattice dynamic calculation should see [102].

Majority of the optical phonon confinement reports in the literature for semiconducting nanowires of (a) Si, Ge, (b) III-VI, II-VII compounds, and (c) oxide compounds have analyzed their results using the spatial correlation model developed by Richter and coworkers [106] and further extended by Campbell and Fauchet [107]. Application of this model to experimental data and the influence of laser flux on the Raman line shape will be discussed here.

Small diameter semiconducting nanowires exhibit phonon confinement due to the long length of the phonon wavevector q compared to the radius of the nanowire, which violates the $q = 0$ selection rule, permitting multiple wavevector of various $q < 1$ to contribute to the phonon linshape. Based on the spatial correlation model first proposed by Richter et al. [106] and expanded further by Campbell and Fauchet [107], it has been argued that restriction of the phonon wave function within a particle of size D results in an uncertainty $\Delta q \sim \pi/D$ in the phonon wavevector of the zone-center optical phonon and a corresponding uncertainty $\delta\omega$ in its wavenumber [112]. Consequently light scattering takes place from quasi-zone-center optical phonons with wavevector q up to π/D. This is in fact valid only for weak phonon localization and the effect diminishes as q approaches π/D [110].

Germanium and silicon belong to the cubic O_h^7 space group and crystallize into the ($F4_1/d32/m$) diamond lattice. The conventional lattice of diamond consists of two interpenetrating face-centered cubic (fcc) atomic lattices which

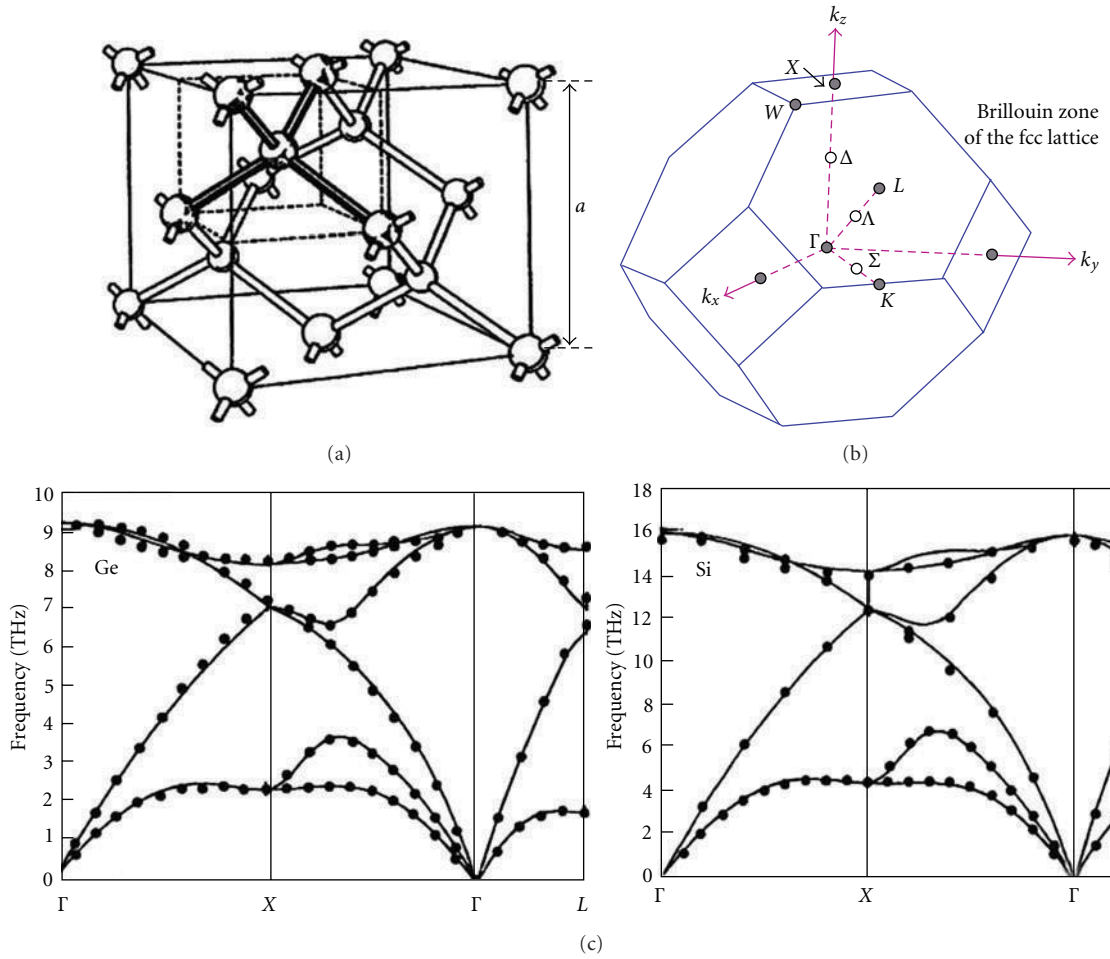


FIGURE 2: (a) Conventional cubic unit cell for the diamond crystal structure ($F4_1/d32/m$). Each atom is tetrahedrally bonded to four nearest neighbors. The lattice parameter of the conventional unit cell containing four atoms, $a = 0.5431$ Å (Si) and $a = 0.5658$ Å (Ge), (b) Brillouin zone for the face-centered space lattice showing the positions of several high-symmetry axes and points [18, 19]. (c) Phonon dispersion curves of Ge [20] (left) and Si [20] (right) along high-symmetry directions. The dots are neutron scattering data [19, 21, 22], and the solid lines are calculations using up to the sixth nearest neighbor interactions in a Born-von Kármán force constant model [20]. The primitive cell contains two atoms; therefore, three optical branches (2TO and 1LO) and three acoustic branches (2TO and 1LO) are observed. These branches are degenerate at the Γ point.

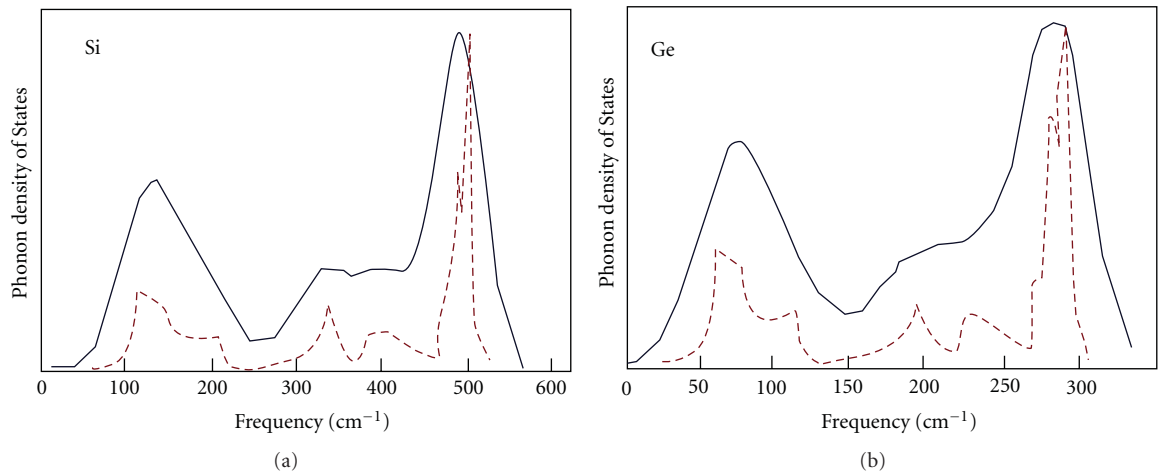


FIGURE 3: Calculated phonon density of state for Si (a) and Ge (b). Solid lines represent a highly disordered material, and the dashed lines represent the crystalline material [23].

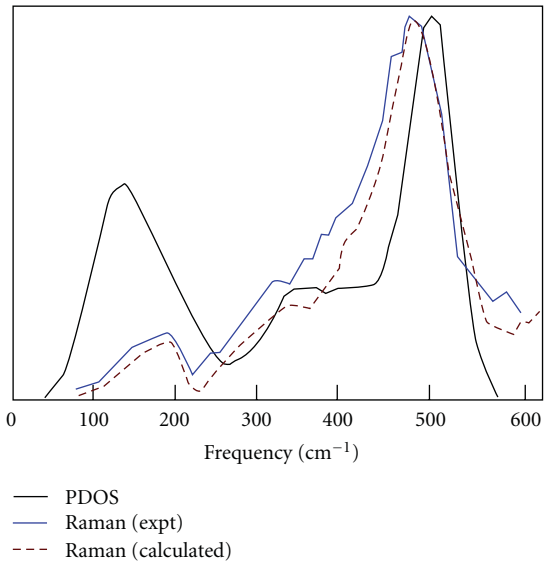


Figure 4: Comparison of experimental Raman profile (thin solid line) and calculated first-order Raman band of highly disordered Si (dashed line). The bold solid line is the calculated phonon density of states (PDOS) for highly disordered Si. The experiment and calculated Raman spectra are in good agreement. The difference in the PDOS and the calculated Raman band shows the importance of matrix element effects [23].

are displaced a quarter of the body diagonal of the conventional cubic cell with respect to each other. Each atom is tetrahedrally bonded to four nearest neighbors. The 3-dimensional unit cell of a tetrahedrally bonded diamond lattice is shown in Figure 2(a), and the corresponding Brillouin zone indicating the positions of several high-symmetry axes ($\mathbf{X}, \mathbf{L}, \mathbf{W}, \mathbf{K}$) and points ($\Gamma, \Lambda, \Delta, \Sigma$) is shown in Figure 2(b) [18, 117]. The phonon dispersion curves along some of these high-symmetry axes for crystalline Si and Ge, obtained from neutron scattering data [19, 21] (dots) and a fit to the data using (up to the sixth nearest neighbor) the Born-von Kármán force constant model (solid line), are shown in Figure 2(c) [19–22] right and left, respectively. At the points in the Brillouin zone where the phonon dispersion curves flatten, $d\omega/dk \sim 0$, and peaks appear in the phonon density of states. However, in highly disordered systems, these features in the phonon density of states are observed to be broadened. Shown in Figure 3 are the calculated phonon density of states for bulk Si (a) and Ge (b). The dashed and solid lines in the figure represent crystalline and highly disordered systems [23], respectively. Note that the disorder introduces both smearing of the sharp peaks in the phonon density of states and disappearance of the fine structures associated with the crystalline state; however, the three main broad features remain. Interestingly, strong disorder does not destroy the main features of the phonon density of states associated with the crystalline system.

If we compare the first order Raman spectra of disordered and crystalline Si, we observe a sharp Lorentzian peak at $\sim 520\,\text{cm}^{-1}$ of full width at half maximum (FWHM) of $\sim 4\,\text{cm}^{-1}$ for the crystalline state. Strongly disordered Si on the other hand exhibits a Raman spectrum that approaches the calculated phonon density of states shown in Figure 3(a). In this case, the peak at $\sim 520\,\text{cm}^{-1}$ now exhibits a FWHM of $\sim 100\,\text{cm}^{-1}$, that is, ~ 25 times broader than the crystalline bulk. In Figure 4, the calculated phonon density of states (thick solid line), Raman spectrum (thin solid line) and calculated Raman spectrum (dashed line) of a highly disordered Si are compared [23]. It is clear that the experimental and the calculated Raman data are in reasonably good agreement. It can also be inferred that the matrix element effects are important if a truly quantitative analysis of the data is desired. Nevertheless, the Raman spectrum of highly disordered system can provide very important phonon density of states information throughout the entire frequency range.

The first Brillouin zone is the smallest volume entirely enclosed by planes that are the perpendicular bisectors of the reciprocal lattice vectors drawn from the origin. The region in k-space that low-k phonons can occupy without being diffracted is called the first Brillouin zone. It contains phonons with k values from 0 to π/a, where a is the lattice parameter. For monoatomic solids with two atoms per primitive cell such as diamond, magnesium, Si, Ge, or diatomic compounds such as GaAs, there are three optic phonon branches in addition to the three acoustic phonon branches. In compounds with a greater number of atoms and complex crystal structures, the number of optical phonons is more than three. If the crystal unit cell contains N atoms, then $3N$ degrees of freedom result in 3 acoustic phonons and $3N - 3$ optical phonons.

Phonons can propagate in the lattice of a crystal as a wave and their dispersion depends on their wavelength [118]. For a given nanowire material, the confinement effects may exhibit different asymmetric broadening and shifts, depending on the symmetries of the phonon and their dispersion curves. There is also dependence on the excitation energy such that phonons of certain symmetry are more responsive to resonance conditions [119]. Transverse phonon confinement in nanowire is due to their one-dimensional geometry. The wavevector is unrestricted in the longitudinal (z) direction, but it is confined and quantized in the tangential (radial) direction as illustrated in Figure 5.

In bulk crystalline materials, Raman spectroscopy and other optical techniques can only probe zone center phonons. Absence of lattice periodicity in nanocrystalline materials relieves this $q = 0$ selection rule. In general, for semiconducting nanowires, phonon confinement is not the only effect linked to diameter. Electronic states of semiconducting-nanowires can be tuned via the wire diameter D, as the band gap should scale approximately as $1/D$ [120].

The organization of this chapter is as follows. We will discuss in Section 2 the spatial correlation phenomenological model for optical phonons and relate it to experimental data from Raman spectroscopy of confined optical phonons in Si and Ge nanowire in Section 3. In Section 4, we will discuss the influence of local inhomogeneous laser heating on the Raman profile of Si and Ge nanowire. Acoustic phonon confinement and its effect on thermal conductivity will be presented in Section 6 and Section 7 will be devoted to summary of the main points presented in this paper and suggestions for future research in phonon confinement.

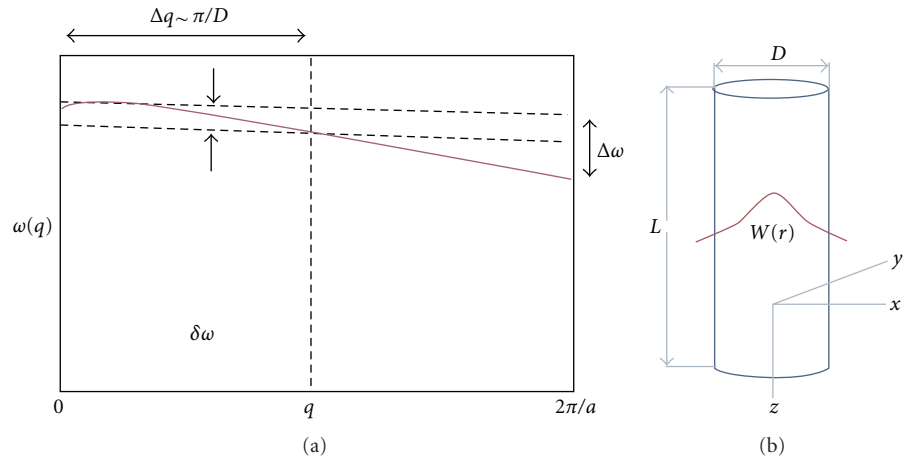


FIGURE 5: (a) Optical phonon dispersion $\omega(q)$ of Si with the first order Raman scattering phonon frequencies extend throughout $\Delta\omega$. Raman active wavevectors of a nanowire with diameter D lie within Δq. (b) Schematic of nanowire of diameter ($D = 2r$) and length L and the confined phonon wave function, $W(r)$.

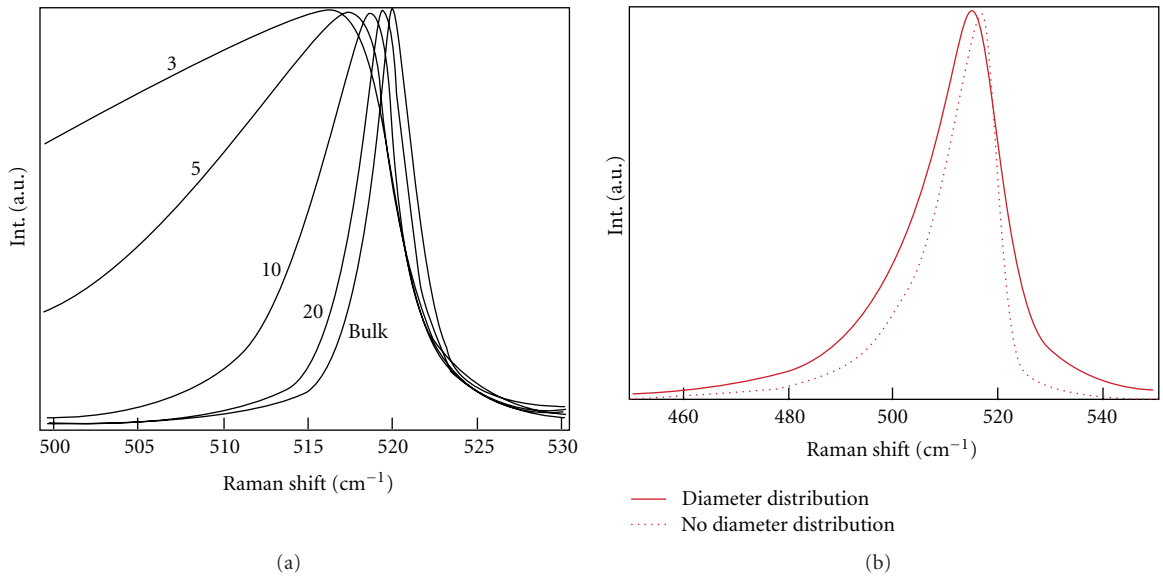


FIGURE 6: (a) A plot showing the finite-size-induced phonon confinement effect (downshift and asymmetric broadening to lower energy) for different diameters of Si nanowires and the Lorentzian line shape of the bulk, for comparison. (b) Comparison of the Raman line shape of 8 nm diameter Si nanowires, taking diameter distribution into account and without diameter distribution. The peak downshift ~1 cm^{-1} and the line width broadened ~30%.

2. Theoretical Models of Phonon Confinement in Nanowires

2.1. Spatial Correlation Model of Raman Scattering for Confined Optical Phonons in Nanowires. Richter and coworkers [106] were the first to propose a phenomenological phonon confinement model (sometimes called Richter model) to explain the experimental observation of a downshift and asymmetric broadening of the first-order Raman profile of crystalline nanostructures. Their approach naturally leads to relaxation of the conservation of the bulk crystal momentum in the scattering process. Assuming a spherical nanocrystalline shape and using the diameter as an adjustable parameter, they fitted the Raman line shape of a film of small Si nanocrystals. Their model was further extended by Campbell and Fauchet [107] who considered other nanocrystalline shapes (i.e., wires and platelets).

For Si and Ge, the longitudinal optic (LO) and the tangential optic (TO) modes are degenerate at the Γ point (zone center). Conservation of the phonon momentum in crystalline Si and Ge produces a Raman active mode of the optical phonons from only the zone center ($q = 0$) at 520 cm^{-1} and 300 cm^{-1} for Si and Ge, respectively. In nanowires, the transverse phonons are confined in the two orthogonal directions perpendicular to the nanowire axis. This allows a greater range of phonon modes to contribute to the Raman

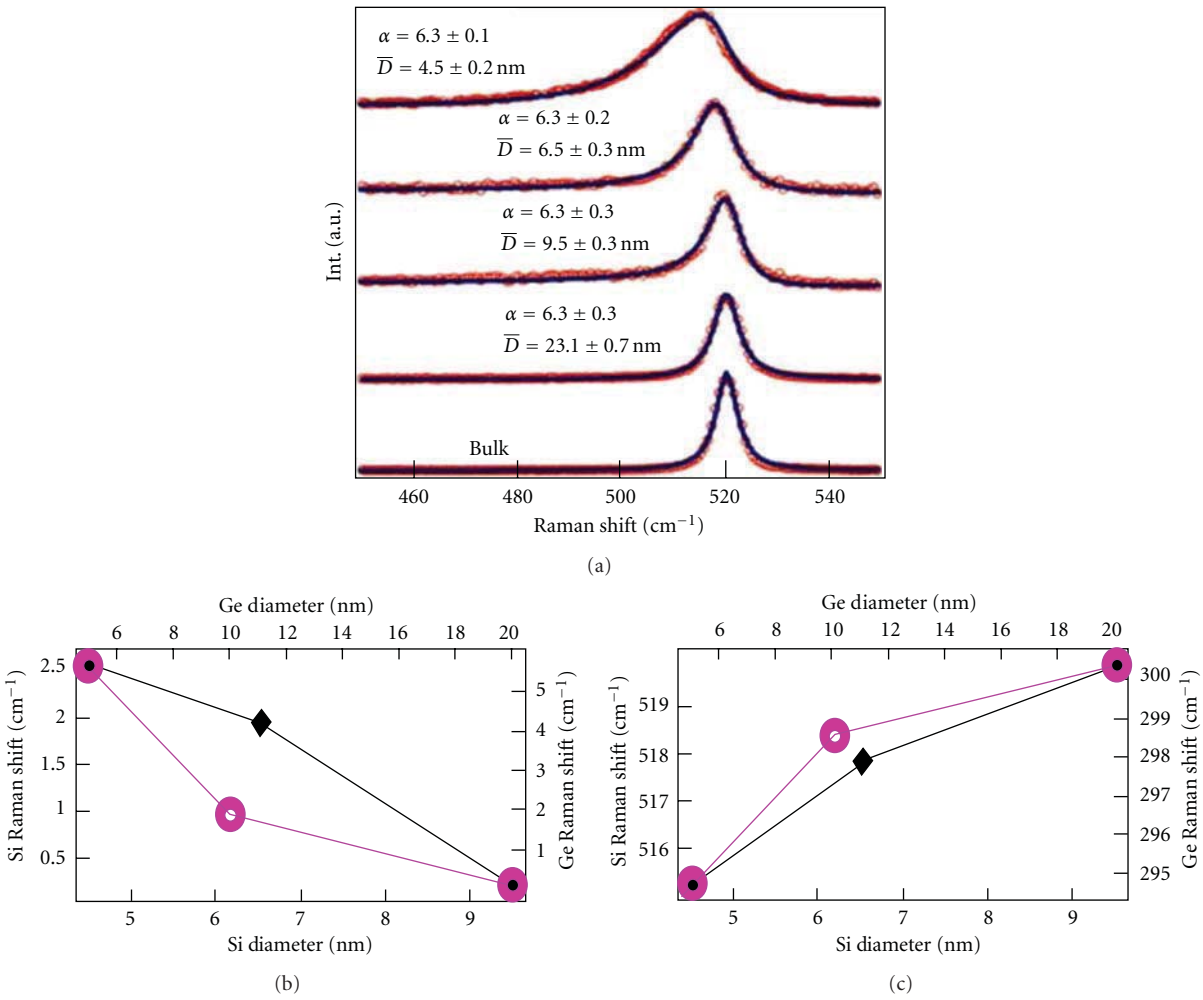


FIGURE 7: (a) Raman spectra showing the first-order Raman band peaks in four ensembles of Si nanowires. The bulk Si (001) spectrum is also shown. Experimental data: red open circles, least-square fit: black solid lines. α is the attenuation factor of the phonon (the width of the Gaussian phonon quantum confinement function) at the real boundary $r = D/2$, $\overline{D}$ is the most probable diameter. (b) Comparison of experimental Raman shift of TO phonon in Si [47] and Ge nanowires [80] for different diameters. Top: absolute shift Si (diamond), Ge (circles); bottom: nanowire Raman shift relative to bulk. Note that the Ge diameter range is twice that of Si.

scattering process. In fact, bulk phonons of wavevector up to $q \sim 1/D$ (D is diameter of the nanowire) contribute to the first-order Raman spectrum.

The Richter model line shape function of the first-order Raman profile of a nanowire expressed in terms of the transverse phonon wavevector ($q_\perp$) can be written as [44–47, 80, 104, 106, 107, 113, 121–123]

$$I_{NW}(\omega) = A_o \int_o^{q_{\max}} \frac{|C(0,q_\perp)|^2}{[\omega - \omega_o(q_\perp)]^2 + (\Gamma/2)^2} 2\pi q_\perp dq_\perp, \quad (1)$$

where A_o is an adjustable parameter, ω is phonon frequency measured relative to the laser line, $\omega_o(q_\perp)$ is the bulk transverse phonon frequency, Γ is the FWHM of the bulk phonon Raman profile, and $|C(0,q_\perp)|^2$ is the spectral weighting function expressed as

$$|C(0,q_\perp)|^2 \sim \exp\left[-\frac{1}{2}\left(\frac{q_\perp D}{\alpha}\right)^2\right], \quad (2)$$

D is the diameter of the nanowire and α is a dimensionless adjustable parameter. Figure 6(a) shows the evolution of the Raman profile with diameter ($20 \geq D \geq 3$) of the 520 cm^{-1} optical phonon of Si nanowire, calculated using (1). Here, $\Gamma = 4.5$ cm^{-1} and $\alpha = 6.3$ were used in the calculations [53]. Since most Raman scattering experiments are performed on ensembles of nanowires, any analysis using the Richter model should take into account the diameter distribution $F(D)$ of the ensemble nanowires. This modifies the Richter model by introducing a second integral due to the diameter distribution as

$$I_{NDW}\left(\omega, \overline{D}\right) = \int_o^\infty F(D) I_{NW}(\omega, D) dD, \quad (3)$$

where $\overline{D}$ is the ensemble most probable diameter and the rest of the parameters are as defined previously. Figure 6(b) shows a comparison of calculated Raman line shape of 8 nm Si nanowire with (solid line) and without (dash line)

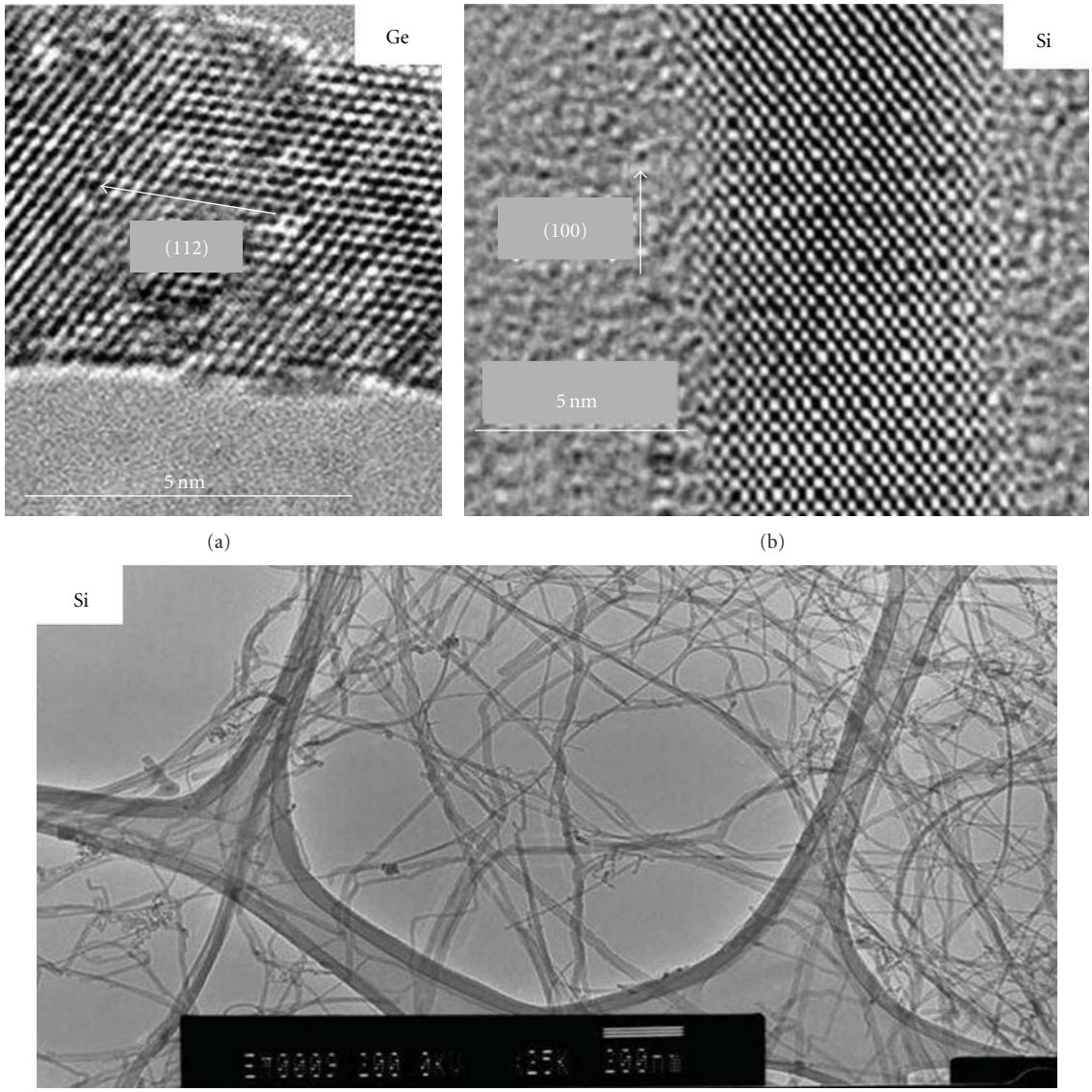


Figure 8: HRTEM images of (a) 6 nm diameter Ge nanowire [80], (b) 7 nm Si nanowire [47], and (c) LRTEM images of Si nanowires.

diameter distribution. There is a clear difference in the Raman profile of with and without the inclusion of the diameter distribution that demonstrates its importance in the interpretation of Raman spectra of confined phonons. It must be emphasized that the model is inconsistent at diameters ≤ 3 nm. This has been discussed in detail in [44–47].

3. Experimental Evidence of Confined Optical Phonons in Nanowires

Optical phonons propagate in the lattice of a single crystal as a wave and exhibit dispersion depending on their wavelength, or equivalently their wavevector in the Brillouin zone [118]. The momentum conservation selection rule determines the region of the Brillouin zone that can be accessed in the Raman scattering process. In a Raman scattering experiment, the magnitude of the scattering vector is $2k_o \sin(\theta/2)$, where k_o is the wavevector of the incident light and θ is the scattering angle. The maximum value of the scattering vector would be $2k_o$ (in the backscattering configuration), $\sim 5 \times 10^4\,\text{cm}^{-1}$ for visible light. Hence, this wavevector is much smaller than the wavevector q of the full phonon dispersion curve, which extends up to the boundary of the Brillouin zone ($\pi/a \sim 10^8\,\text{cm}^{-1}$). Since acoustic phonons mostly have very small wavenumbers, they could only be probed with Brillouin spectrometer consisting of a Fabry-Perot interferometer. Thus, only the optical phonons close to the zone centre ($q \approx 0$) are probed in visible Raman spectroscopy of bulk samples. This $q \approx 0$ selection rule is essentially a consequence of the infinite periodicity of the crystal lattice. However, if the periodicity of the crystal is curtailed, as in the case

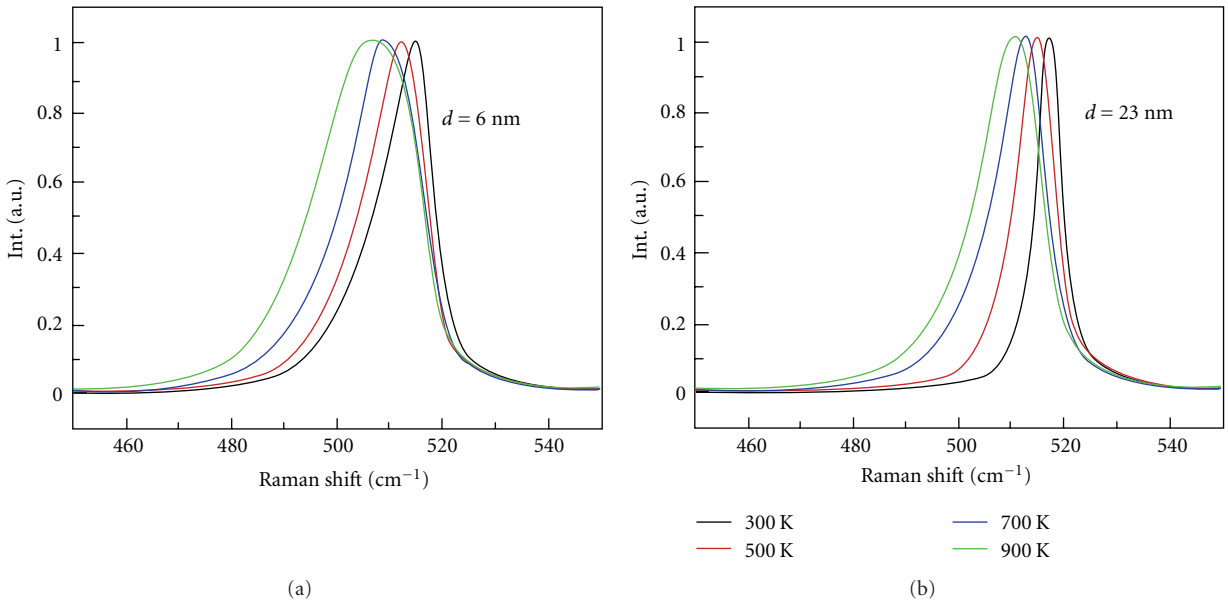


FIGURE 9: Calculated Raman line shape of the 520 cm^{-1} band of Si nanowires subjected to laser inhomogeneous heating. The focal spot size is 1 μm in the micro-Raman focal plane. Results are calculated using (10) at the different peak temperatures indicated for (a) $D = 6.0$ nm and (b) $D = 23$ nm nanowires [44–46].

of nanocrystalline materials, the $q \approx 0$ selection rule is relaxed, leading to asymmetric broadening and downshift in the Raman profile, in the case of Si and Ge.

Additionally, it has also been observed that, the supporting substrate plays an important role in Raman scattering experiment [44, 46, 80, 124]. If the supporting substrate is a poor thermal conductor, the Raman peak shift to lower frequency due to heating [44, 46, 80]. There is substantial evidence showing that both quantum confinement and inhomogeneous heating induce redshift and asymmetric broadening relative to the bulk, in Raman spectra of optical phonons in Si and Ge nanowires [44, 46, 122, 123, 125]. Here, we focus on phonon confinement of the first-order Raman spectrum in semiconducting nanowires of Si and Ge and would discuss the effect of inhomogeneous heating later.

3.1. Semiconducting Nanowires: Si and Ge. Si nanowire has always been the prototype for nanoscale semiconducting studies due to the vast information on its bulk counterpart. The earliest reports of phonon confinement in nanowire [106, 107] focused on Si. The shape and frequency of the Raman peaks due to scattering by the optical phonons are thought to be dependent on the diameter of the nanowire. The onset of phonon confinement is at the point where the phonon mean free path is comparable to the diameter of the nanowire [47]. Figure 7(a) shows the first systematic report on the evolution of Raman spectrum of Si nanowires with diameters for 3 nm $\leq$ D $\leq$ 20 nm. The open circles represent the raw Raman data, and the solid line is a least square fit of the Richter model including diameter distribution (3). It depicts an asymmetric broadening to lower frequency and a downshift as reported by Adu and coworkers [47]. Similar arguments can be made for Ge nanowires which have been reported by Jalilian and coworkers [80].

Figures 7(b) and 7(c) are the plots of measured TO optical phonon peak frequency, versus Si and Ge nanowire diameter [47, 80]. The solid line is a guide to the eye. These plots show a significant difference between Ge and Si TO phonons. In the absolute shift case, the Si slope between 4.5 and 9.5 nm is 0.9086 cm^{-1}/nm and the Ge slope between 5 and 10 nm is 0.7634 cm^{-1}/nm. As the nanowire diameter decreases, the absolute Raman shift of the TO phonon increases but the Raman shift relative to the bulk decreases, in accordance with the theory [47]. The Ge nanowire TO phonon apparently only reaches bulk-like behavior at a diameter between 10 and 20 nm whereas for silicon this occurs between 5 and 10 nm. Both Ge and Si nanowires exhibit TO phonon confinement that induces an absolute Raman shift over a range of 5 cm^{-1} [47, 80]. The ranges of Raman shift relative to bulk, however, are approximately 2.6 and 7 cm^{-1} for Si and Ge, respectively. Although the absolute Raman shift of both Si and Ge shows positive curvature with nanowire diameter, the curvature is negative for Ge in the relative shift. It should be noted that the excitation laser wavelength used in Figures 7(b) and 7(c) is nearly in resonance with the Si sample but far from it for the Ge sample.

4. Effect of Inhomogeneous Laser Heating on Confined Optical Phonons

Typically, the laser irradiation during Raman measurements can cause sample heating and photon excitation of charge carriers [104, 126–130]. Downshifting and broadening of Raman bands in bulk materials, with increasing laser radiation, is typically identified to be due to laser heating. Poor

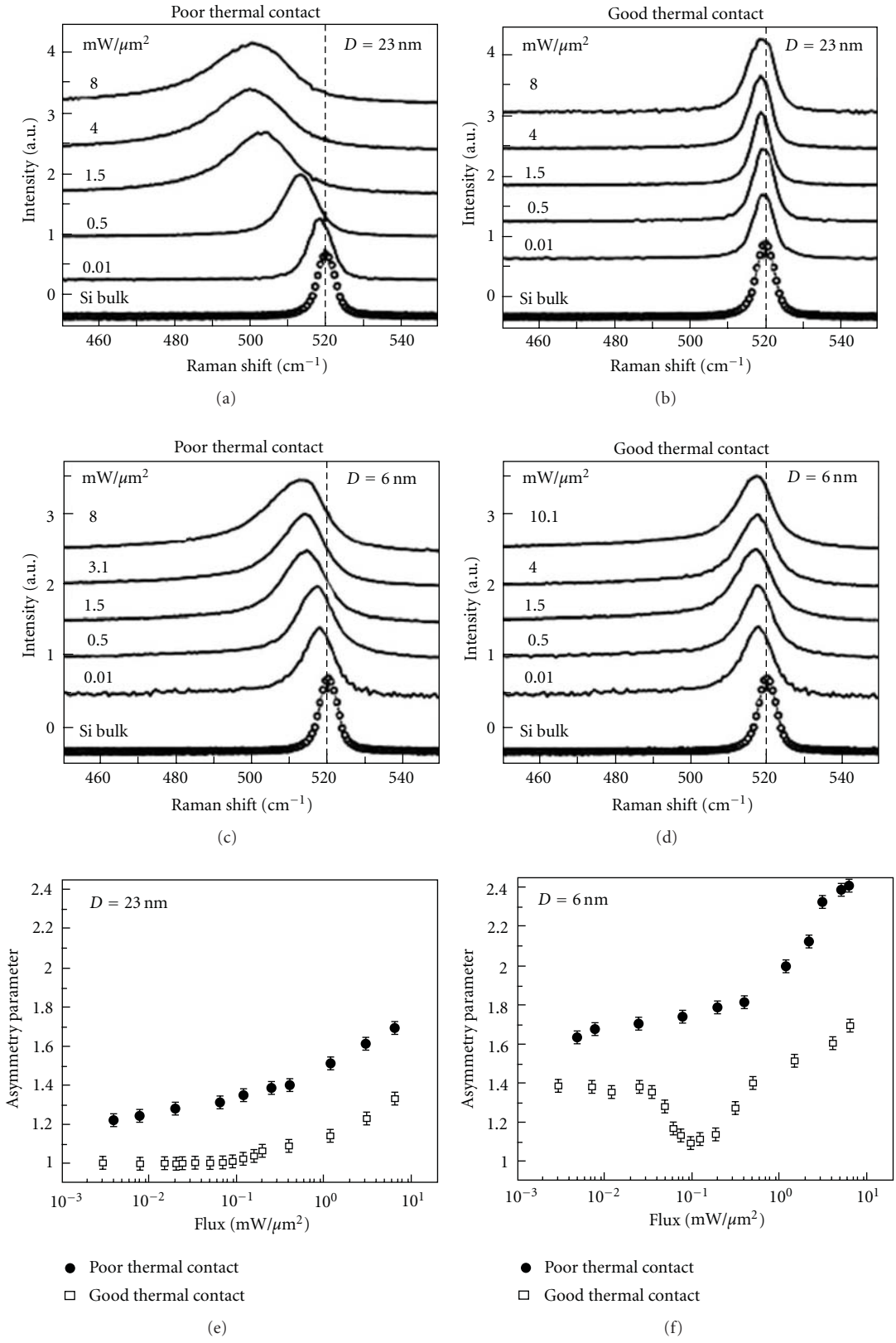
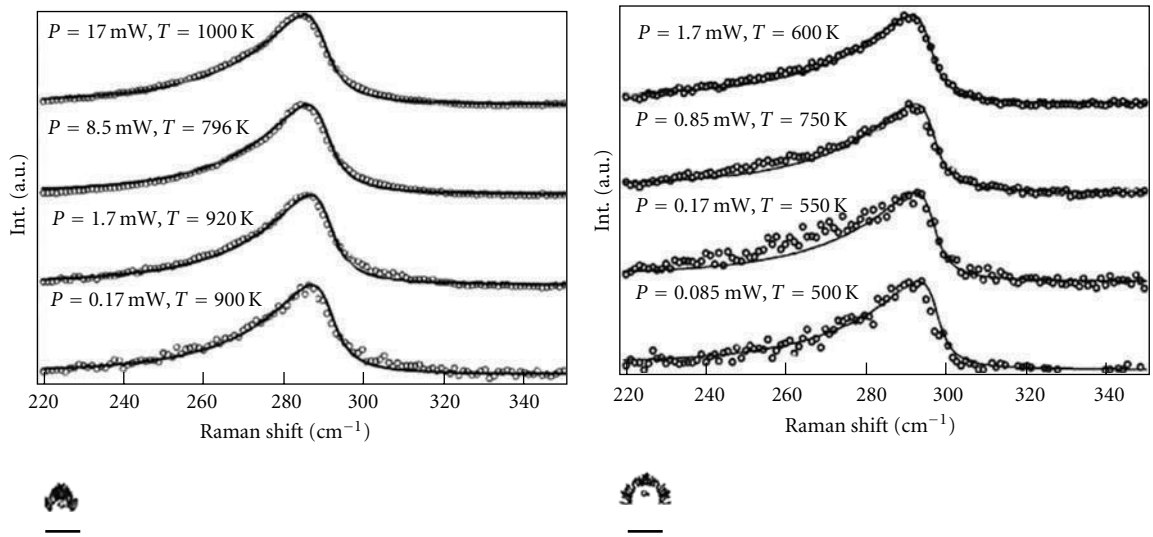


Figure 10: Flux (Φ) dependent Raman spectra of Si nanowires collected under poor thermal anchorage (a, c) and good thermal anchorage (b, d) for 23 nm wires (a, b) and 6.0 nm wire (c, d). The nanowires were located on an Indium substrate. (b) Flux (Φ) dependence of the asymmetry parameter A for Si nanowires under poor thermal contact (solid circles) and good thermal contact (open squares) for (e) 23 nm (f) 6.0 nm Si nanowires [46].



(a) (b)

FIGURE 11: Raman spectra at 632.8 nm for the Ge nanowire ($D = 7$ nm) for varying laser power levels (circles) at two different Ga droplet sizes (a) droplet size ~1 μm and (b) droplet size ~1 mm. The solid lines represent the least square fit (10) [80].

thermal contact of the nanowire to the substrate and intense focusing of the laser beam in a micro Raman spectrometer can lead to significant heating of the sample. In this section, we discuss the temperature dependence of the first-order Raman spectra of Ge and Si nanowire due to variation in laser power and thermal conductance of the nanowire on the substrate. The subtle interplay between quantum phonon confinement and the local heating effect are shown to influence both the frequency shift and the asymmetric broadening of the Raman spectra.

The Stokes-anti-Stokes intensity ratio of first-order Raman spectra is normally used to determine the local temperature of the nanowire sample. The intensity ratio relates to the temperature by

$$\frac{I_s}{I_{as}} = P_o \exp\left(\frac{\hbar\omega_o}{k_B T}\right), \tag{4}$$

where ω_o is the phonon frequency, the prefactor P_o depends on the absorption constant and the Raman cross-section at a given frequency. Typically, the value of P_o is determined by calculating the Stokes-anti-Stokes intensity ratio I_s/I_{as} at room temperature and at the lowest possible laser power to eliminate any laser-induced heating. The phonon confinement function (3) is modified to include temperature dependence [128–130]. The frequency is expressed as

$$\omega(q, T) = \omega(q) + \Delta\omega_1(T) + \Delta\omega_2(T), \tag{5}$$

$\Delta\omega_1(T)$, is the frequency shift due to phonon decay processes. This phonon-phonon coupling term describes the anharmonic coupling between phonons and is approximated by

$$\Delta\omega_1(T) = A_1\left(1 + \frac{2}{x}\right) + A_2\left[1 + \frac{3}{x} + \left(1 + \frac{3}{x^2}\right)\right], \tag{6}$$

where $x = e^{(\hbar\omega_o/2\kappa_B T)} - 1$. The first term describes the coupling of the phonon to decayed low-energy two phonons (three-phonon coupling), and the second term describes the coupling to three decayed phonons (four-phonon coupling). A_1 is adjusted to match the bulk Ge and Si values. $\Delta\omega_2(T)$ is the frequency shift due to the thermal expansion of the lattice. The compressive stress expressed as

$$\Delta\omega_2(T) = \omega_o\{\exp(3\gamma\beta T) - 1\} \tag{7}$$

is neglected since the Si and Ge nanowires used in the studies exhibit limited or no oxide sheath formation as evidenced by Figure 8. γ is the Gruneisen parameter, and β is the thermal expansion coefficient of Ge or Si.

The temperature dependence of the inverse phonon life time (FWHM) in the formalism [128–130] is

$$\Gamma(T) = \Gamma + \Delta\Gamma(T), \tag{8}$$

where Γ is the FWHM of the bulk Ge or Si including the instrumental broadening, and $\Delta\Gamma$ is given as

$$\Delta\Gamma(T) = B_1\left(1 + \frac{2}{x}\right) + B_2\left[1 + \frac{3}{x} + \left(1 + \frac{3}{x^2}\right)\right], \tag{9}$$

where x is as defined previously. The first term is due to the three-phonon coupling, and the second term is the result of the four-phonon coupling effect on the FWHM of the Raman spectrum. Just as before, we neglect the four-phonon coupling term, and B_1 is adjusted to match the bulk Ge or Si values.

The asymmetric broadening of the Raman TO band has been attributed to Fano interference between scattering from the discrete optical phonon and an electronic continuum due to photon-excited charge carriers [126]. At sufficient doping levels, electrons and holes in semiconductors participate in inelastic scattering leading to Fano resonance. An asymmetry of the Fano line shape depends on the electron-phonon coupling strength. Attributable to the observation of asymmetry in the low-frequency tail, the contribution of Fano

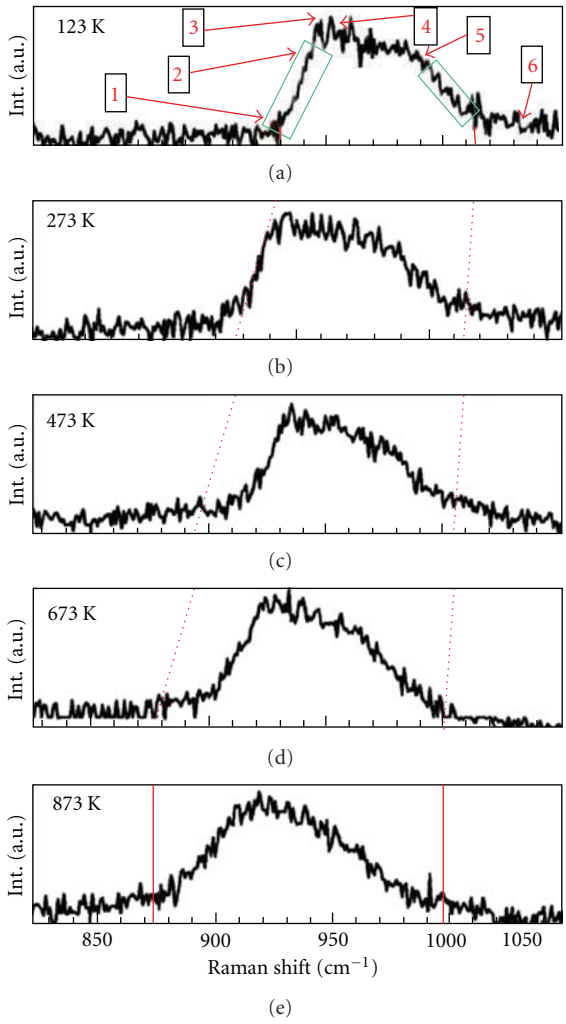


FIGURE 12: Second-order Raman spectra of Si nanowires TO phonons as a function of temperature. The numbers in the top panel (1, 2, 3, 4, 5, and 6) refer to Brillouin zone points **X**, **Q**, $\mathbf{S_1}$, **W**, **L**, and **Γ**, respectively. Temperature-dependent second-order Raman spectra of Si obtained using 632.8 nm laser excitation [113].

resonance for asymmetric broadening of the Raman spectrum can be ruled out, since laser excitations generate equal numbers of holes and electrons in the undoped Ge and Si. The asymmetric line shape in the phonon mode is also known to be affected by strain caused by an oxide layer. There were no indications that the limited oxide layer had any contribution to the asymmetric line shape.

A coupled phenomenological model that accounts for both phonon confinement and temperature effects to best describe the observed asymmetry in the first-order Raman spectra for Ge and Si nanowires is expressed as

$$I(\omega, D, T) = \int_o^1 \int_o^\infty \frac{e^{-(q_\perp^2 D^2/4\alpha^2)} e^{[(D-\overline{D})^2/2\sigma^2]}}{\left[\omega - \omega(q_\perp, T) + \Delta\omega\right]^2 + (\Gamma + \Delta\Gamma/2)^2} 2\pi dq_\perp dD, \quad (10)$$

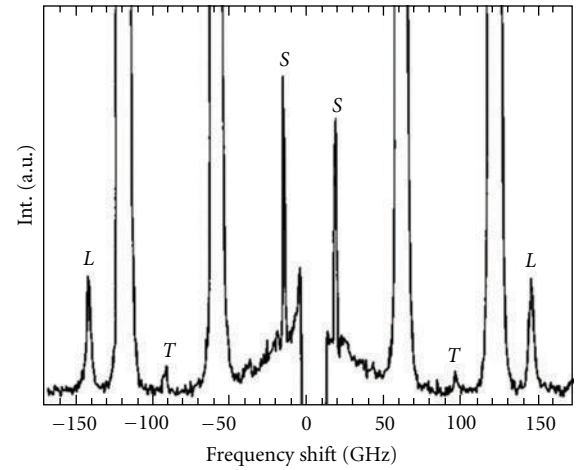


FIGURE 13: The Brillouin spectrum of bulk Si showing a broad quasi-ielastic peak around the central elastically scattered peak. The peaks labeled (S), (T), and (L) correspond to the surface acoustic wave, transverse mode (T), and longitudinal mode (L), respectively [114].

where $e^{[(D-\overline{D})^2/2\sigma^2]}$ is the diameter distribution (log-normal) of the nanowires. Equation (10) shows that the coupled phonon confinement and inhomogeneous local laser heating induce a redshift and asymmetric broadening in the Raman spectra of Si and Ge nanowires. Figure 9 shows the evolution of phonon line shape with temperature of 6 nm and 23 nm Si nanowire calculated using (10).

5. Experimental Evidence of Inhomogeneous Laser Heating in Si and Ge Nanowires

A number of reports on inhomogeneous laser heating effect in the first-order Raman spectrum of nanowires have been published in the literature [44–46, 80, 104, 110, 113, 130–132]. Here, we summarize our results on the coupled phonon confinement and inhomogeneous laser heating in Si and Ge nanowires. Figure 10 shows the Raman spectra of ensemble of Si nanowires with most probable diameter of 6 nm and 23 nm under good (b, d) and poor (a, c) thermal anchoring to the supporting substrate [44, 46]. Both 6 nm and 23 nm diameter nanowires show substantial redshift with increasing flux when they are inefficiently coupled thermally to the supporting substrate. For 23 nm diameter nanowires, there is very little frequency difference between high and low flux when there is good thermal contact between the nanowires and the supporting substrate. In the case of the 6 nm diameter Si nanowires which are poorly anchored to the substrate, we see a redshift in the peak position as a function of increasing flux. The corresponding plot of the asymmetry as a function of laser flux is shown in Figures 10(e) and 10(f). The 23 nm nanowires exhibit monotonic increase in asymmetry with increasing laser flux for both poor and good thermal anchorage to the supporting substrate (Figure 10(e)). On the other hand, for the 6 nm Si nanowires with good thermal anchorage to the substrate, the asymmetry initially remains flat, then decreases, and eventually increases with increasing

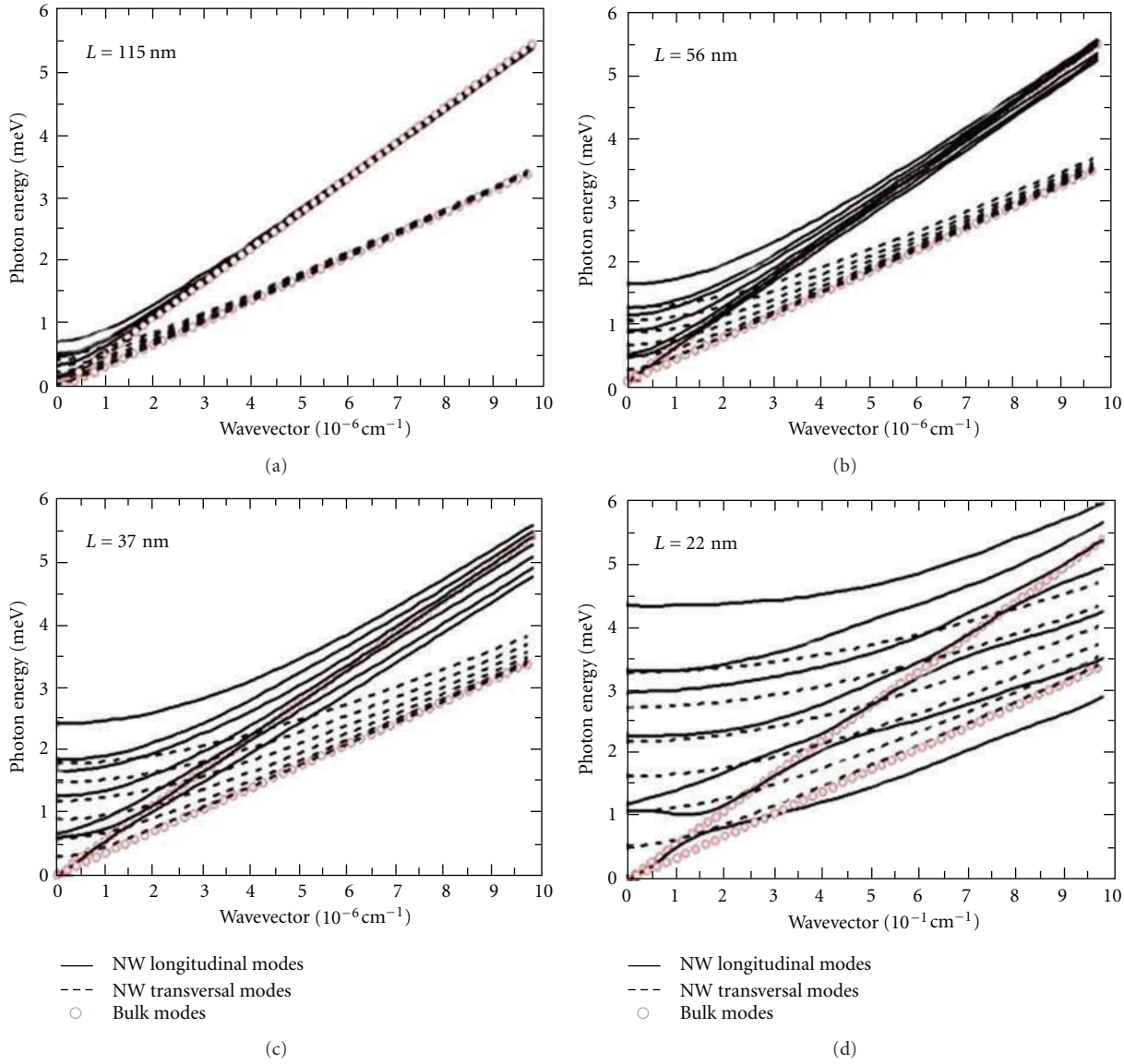


Figure 14: Elastic continuum approximation prediction of the dispersion relations for longitudinal (solid lines) and transversal (dashed lines) modes in Si nanowires of cross-sections 115, 56, 37, and 22 nm [94].

flux. The nonmonotonicity observed in the asymmetry of the 6 nm nanowires is attributed to low coverage and good thermal contact with the Indium substrate which clearly demonstrates the interplay of phonon confinement (dominant at low flux) and inhomogeneous laser heating (dominant high flux) [44, 46]. Similarly, the Raman spectrum of Ge nanowires on quartz and germanium substrates exhibited analogous characteristics as reported by Jalilian et al. [80]. The heating effect is found to be more pronounced for nanowires grown and analyzed on quartz (thermal conductivity $\kappa \sim 6$ w/mK) than for those grown on Ge ($\kappa \sim 60$ W/mK) substrates for a given laser power as shown in Figure 11.

Effects of laser heating have also been observed in second-order Raman spectra of Si nanowires as shown in Figure 12 [113]. The temperature-induced Raman redshift of the 2TA(**X**) and 2TO peaks of Si nanowires were enhanced compared with those of bulk Si. The Raman shift of the 2TO phonon peak of Si nanowires is larger, and thus it is expected that the 2TO(**Γ**) temperature dependence is weaker than the temperature dependence of bulk Si. Additionally, at 300 K, the frequency of 2TO(**Γ**) of Si nanowires (bulk silicon) is 1041 cm^{-1} (1037 cm^{-1}) [113]. An earlier study of the same effects provided analytical inclusion of the anharmonic phonon processes. The asymmetry of Raman peaks was ascribed to quantum confinement since heating alone produces symmetric broadening. The integrated intensity of the phonon modes as a function of measurement temperatures has been reported. One of the earliest studies of size effects in second-order Si mode identified the transition as originating in the Brillouin zone **L** point. The validity of assigning quantum confinement effects to overtone transitions has been questioned without explanation [133].

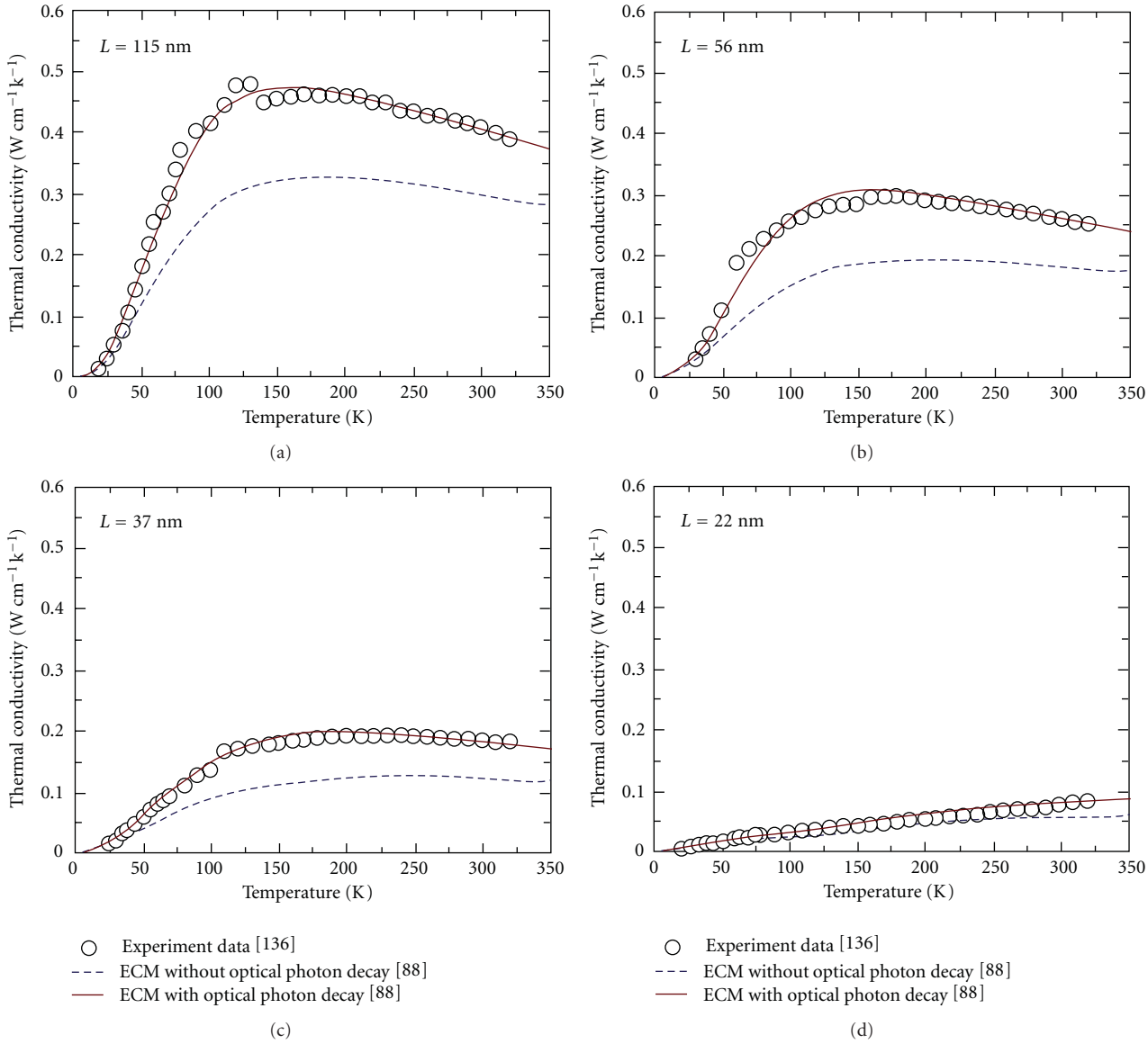


FIGURE 15: Thermal conductivity of individual Si nanowire. Symbols: experimental data [115]. Solid lines: elastic continuous model (ECM) which considers the optical phonons decay into acoustic phonons as acoustic phonon generation rate. Dashed lines: theoretical results obtained from ECM without accounting for the optical phonon decay.

6. Acoustic Phonon Confinement

Since the total wavevector in an inelastic light scattering process is conserved, that is, $\Delta(k + q) = 0$ (where k and q are the wavevectors of the photons and phonons, resp.), the wavevector of resulting phonon in a backscattering configuration is $q = 2nk_i$, where k_i is photon wavevector and n is the refractive index of the solid. In acoustic phonons, this "selection rule" predicts a narrow peak at a frequency shift $\omega = v_s q = 2v_s n k_i$, where v_s is the phonon sound velocity. For Si, these peaks are very close to the laser line, normally observed within the range 0.7–7 cm^{-1} (~20–200 GHz). Brillouin scattering technique is used to detect such low-frequency excitations. Shown in Figure 13 is Brillouin spectrum of bulk Si [114]. The sharp peaks labeled L, T, and S are stokes/antistokes pair of the longitudinal (L), transverse (T) and surface acoustic waves (S), respectively. Note that the unit of the frequency is in GHz.

The acoustic phonon dispersion of nanowires is more complex and significantly altered compared to their bulk counterpart. As shown in Figure 2(c) for bulk Si, there is one LA and two TA modes. In nanowires, however, the number of acoustic phonon modes is influenced by the nanowire diameter. Shown in Figure 14 is the phonon dispersion of the seven lowest acoustic branches in Si nanowire of diameter 115, 56, 37, and 22 nm calculated using the elastic continuum model (ECM) [94], together with the three branches of the bulk. It can be inferred quantitatively that the slope of the acoustic phonon branches decreases with decreasing

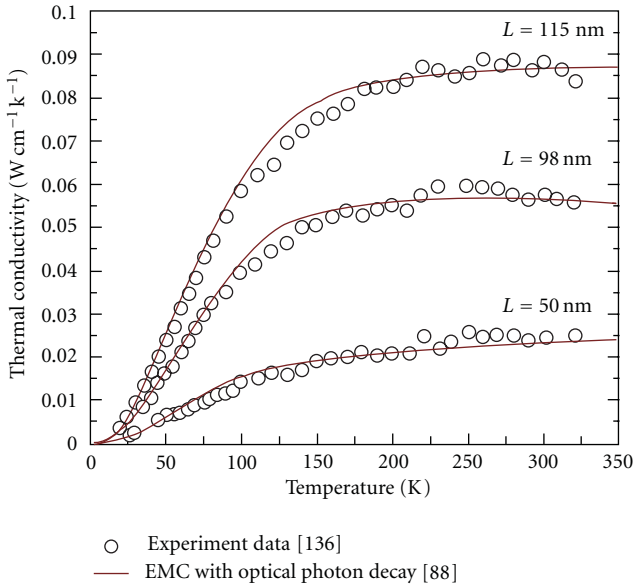


FIGURE 16: Thermal conductivity of rough Si nanowires. Open circles are experimental results from [116], and solid lines are theoretical results obtained from the elastic continuum model including acoustic phonon confinement and surface roughness [94].

diameter of the nanowires, which implies a decrease in the transverse and longitudinal average phonon velocities. To date, there are no reports on Brillouin scattering on Si and Ge nanowires. Recently, Torres and coworkers observed acoustic phonon confinement in Si membranes of 32.5 nm thickness by suspending the membranes over a trench to prevent damping [134].

6.1. Thermal Conductivity. Extensive work on the effects of acoustic phonon confinement in III-V compounds and Si-based nanostructures shows a lower acoustic phonon group velocity, lower thermal conductivity, and increased scattering rate compared to their bulk counterpart [135–137]. The acoustic phonon scattering rate is affected by the nanowire surface roughness and the confinement in the circumferential direction (when the diameter is comparable to the phonon mean free path).

Generally, the thermal conductivity (k) can be expressed in terms of heat capacity (C), the phonon mean free path (l), and the acoustic phonon group velocity (v) as

$$\kappa = \frac{1}{3} vCl. \tag{11}$$

Thus, the reduction of the acoustic phonon average velocity and the scattering effect cause the thermal conductivity of nanowire to decrease with decreasing wire diameter. Figure 15 shows the experimental data-open circles [115] and theoretical fit using the (ECM) solid line [94] of thermal conductivity of 115 nm, 56 nm, 37 nm, and 22 nm Si nanowire with smooth surfaces. The fit takes into account the decay of the optical phonons into acoustic phonons. The calculation without the decay is shown as dashed line. Similar experiment on Si nanowire with surface roughness found an order of magnitude lower thermal conductivity, as shown in Figure 16 [116]. These reports clearly show the potential of using phonon engineering techniques such as surface roughness in addition to core-shell techniques to nanoengineer nanowires for applications where low thermal conductivity and high electron conduction (mobility) are highly desirable, such as thermoelectric nano coolers.

7. Summary and Conclusions

In this paper, we reviewed phonon confinement effects in nanowire using Si and Ge-nanowire as prototypes. The concepts reviewed here are applicable to nanowires of semiconducting materials. We presented both experimental and theoretical models, first proposed by Richter and coworkers that explain the experimentally observed phonon confinement (downshift and asymmetric broadening) effect in Si and Ge nanowires and the interplay of phonon confinement and inhomogeneous laser heating in the Raman spectra of the first-order Raman bands of smaller Si ($D \leq 10$ nm) and Ge ($D \leq 15$) nanowires. Thus, to appreciate the phonon confinement effect in Raman spectroscopy of semiconducting nanowire, it is critical and necessary to use ultra low laser flux and high thermal conductivity substrates with good thermal anchoring.

We also presented the influence of the radial confinement in nanowires on acoustic phonons, particularly in Si nanowires. Theoretical calculations using elastic continuum-model predicted the number of acoustic branches being greater than or equal to four depending on the nanowire diameter. For Si nanowires, both theoretical calculations and experimental measurements clearly revealed suppression of thermal conductivity of nanowires with decreasing nanowire diameter. The suppression is attributed to acoustic phonon confinement and nanowire surface roughness.

To date, there have been limited reports on experimental measurements of acoustic phonons in nanowires, especially Si and Ge. Sensitive experiments are needed to probe these new phonon properties in "confined" nanowires.

Acknowledgments

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Review Article

Fabrication of Axial and Radial Heterostructures for Semiconductor Nanowires by Using Selective-Area Metal-Organic Vapor-Phase Epitaxy

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The fabrication of GaAs- and InP-based III-V semiconductor nanowires with axial/radial heterostructures by using selective-area metal-organic vapor-phase epitaxy is reviewed. Nanowires, with a diameter of 50–300 nm and with a length of up to 10 μm, have been grown along the ⟨111⟩B or ⟨111⟩A crystallographic orientation from lithography-defined SiO_2 mask openings on a group III-V semiconductor substrate surface. An InGaAs quantum well (QW) in GaAs/InGaAs nanowires and a GaAs QW in GaAs/AlGaAs or GaAs/GaAsP nanowires have been fabricated for the axial heterostructures to investigate photoluminescence spectra from QWs with various thicknesses. Transmission electron microscopy combined with energy dispersive X-ray spectroscopy measurements have been used to analyze the crystal structure and the atomic composition profile for the nanowires. GaAs/AlGaAs, InP/InAs/InP, and GaAs/GaAsP core-shell structures have been found to be effective for the radial heterostructures to increase photoluminescence intensity and have enabled laser emissions from a single GaAs/GaAsP nanowire waveguide. The results have indicated that the core-shell structure is indispensable for surface passivation and practical use of nanowire optoelectronics devices.

1. Introduction

Interest in semiconductor nanowires has been growing over the past decade when the fabrication technology for Si-integrated circuits entered an advanced phase where the gate length of a field effect transistor (FET) shrank to a few tens of nanometers with the evolution of the technology. Fabrication of nanostructures to explore nanophotonics has also been a focus of interest for those who have been pursuing a single-photon source that can be used in optical communication systems that are expected to provide high degrees of reliability. Etching of semiconductor crystals has been widely used in conventional production processes to fabricate FETs and optical devices. However, eliminating damage or contamination created by etching on the crystal surface has become more difficult as device sizes have reduced. Compared to etching-based top-down methods of fabrication, the bottom-up method based on crystal growth is a counter approach to fabricating nanostructures without any concern for damage during fabrication.

Wagner and Ellis reported the vapor-liquid-solid (VLS) growth of Si whiskers using Au as a catalyst [1] to form semiconductor nanowires in 1964. Since then, various nanowires comprised of Si [2, 3], Ge [2, 3], GaAs [4], InP [5], In_2O_3 [6], GaN [7], and ZnO [8] grown by VLS have been reported and the crystal structure of the nanowires has been analyzed and applications to light emitting diodes (LEDs) [9], gas sensors [10], piezoelectric generators [11], solar cells [12], resonant tunneling diodes [13], and FETs [14] have been discussed. When we fabricate nanostructures by VLS, we do not always need lithography. So the method has been popular for those who are interested in growth mechanism, nanostructure physics, and novel functional devices. However, incorporating catalysts into the grown crystal might be a concern in using the VLS method. Au, when incorporated into Si, is known to form a mid-gap impurity level and acts as

a carrier trap that might degrade the performance of devices [15]. Therefore, if the performance or reliability of devices is pursued, the VLS growth process should be investigated with consideration whether or not catalysts form a carrier trap level in semiconductors.

Nanowires formed by VLS using a self-catalyst, that is, a Ga or In droplet, which is, thought to be consumed as a source of crystal growth, have been reported for GaAs/AlGaAs core-shell and GaAs/InGaAs axial heterostructures in molecular beam epitaxy [16, 17]. Si and Ge nanowires grown from a thin SiO_2 layer without using a metal catalyst have also been reported [18]. The methods are based on the VLS mechanism but have no concern over contamination originated from catalyst materials that are not consumed for growth.

The formation of nanowires by selective catalyst-free growth using a mask pattern and columnar growth based on anisotropy of the crystal structure with wurtzite have been reported since the late 1990s. These methods are different from the VLS, have not needed any catalysts, and there have been no concerns over contamination by them. Hamano et al. reported GaAs pillar (nanowire) arrays selectively grown along the ⟨111⟩B axial direction by using metal organic vapor phase epitaxy (MOVPE) on a GaAs (111)B substrate with lithography-defined SiO_2 mask openings [19]. They discussed the GaAs growth rate along ⟨111⟩B as a function of the pillar radius and the gas supply pressure of an AsH_3 source. Motohisa et al. investigated the diameter dispersion of GaAs nanowire arrays selectively grown by MOVPE in an effort to fabricate a photonic crystal lattice [20]. Yoshizawa et al. reported GaN nanocolumn growth on an Al_2O_3 (0001) surface during RF radical-source molecular beam epitaxy (RF-MBE) [21, 22]. GaN nanocolumns as thin as 50 nm and as long as 600 nm have been obtained without using a mask pattern. The methods of growth later evolved into fabricating GaN/InGaN nanocolumn arrays grown using a lithography-defined mask pattern for red-green-blue or multicolor LEDs in the visible wavelength range [23]. ZnO nanorods, as thin as 25 nm, grown perpendicular to an $Al_2O_3(00 \cdot 1)$ surface without using a mask pattern during MOVPE have been reported by Park et al. [24]. Using this technology, ZnO nanorods formed vertically on the top layer of a GaN LED have been demonstrated to enhance the efficiency with which light output is extracted from devices [25].

Paetzelt et al. have recently reported selective-area growth of GaAs and InAs nanowires on a GaAs(111)B surface with SiN_x templates by using MOVPE [26]. They argued for the dependence of the rate of nanowire growth on the growth conditions and nanowire radius/pitch. InAs/GaAs heterostructures have also been grown to investigate how the shape and crystal structure of nanowires change. Sladek et al. reported GaAs and AlGaAs nanowires selectively grown on a GaAs(111)B substrate with a hydrogen-silsesquioxane mask pattern by MOVPE using N_2 carrier gas in an effort to fabricate a conductive channel in modulation-doped GaAs/AlGaAs heterostructure nanowires [27]. They observed that the lateral growth of GaAs nanowires had increased due to the reduced surface diffusion of growth species on the mask when Si_2H_6 was added to the source gases, or due to polycrystalline layer growth on the mask when GaAs/AlGaAs core-shell nanowires were grown.

We have concentrated on the selective-area growth of group III-V semiconductor nanowire arrays by using MOVPE over the past several years. GaAs/InGaAs axial (vertical) heterostructures [28], GaAs/AlGaAs radial (lateral) [29] and axial heterostructures [30], an InAs quantum tube sandwiched by InP [31], and GaAs/GaAsP radial/axial heterostructures [32, 33] have been fabricated to characterize crystal structures, atomic composition profiles, and photoluminescence properties with quantum size effects. Laser emissions have quite recently been achieved in GaAs/GaAsP core-shell nanowires under pulsed photoexcitation [32]. We review our studies on fabricating axial and radial heterostructures obtained by selective-area MOVPE (SA-MOVPE) and discuss their growth characteristics and optical properties in this paper.

2. Method for Nanowire Growth and Characterization

There is a schematic of the process for growing nanowires in Figure 1. An SiO_2 layer with a thickness of 20–30 nm, which was used as a mask during SA-MOVPE, was deposited on a GaAs(111)B substrate by plasma sputtering or chemical vapor deposition. An array of mask openings was fabricated for the SiO_2 layer by electron beam (EB) lithography and wet chemical etching of SiO_2 through an EB resist pattern. The diameter of the openings ranged from 20 to 1000 nm, and the pitch was changed between 300 and 3000 nm. The mask opening array was fabricated in a 100×100-μm square area, which was separated with a 100-μm isolation distance by removing SiO_2 from neighboring square array areas that had the same size. The shape of the opening was designed to be hexagonal in EB lithography, but it was rounded into a circular shape after wet chemical etching when the pattern size was less than 100 nm. The source materials used for MOVPE were trimethylgallium (TMG), trimethylaluminium (TMA), trimethylindium (TMI), arsine (AsH_3: 5 or 20% in H_2), and tertiarybutylphosphine (TBP). Silane (SiH_4: 50 ppm in H_2) was used as the n-type dopant, and diethylzinc (DEZ) was used as the p-type dopant for the device structures. The source gases were carried by palladium diffused H_2, and the flow rates were controlled by mass flow controllers. The total pressure inside the growth chamber (horizontal SiO_2 tube) was maintained with a vacuum pumping system at 0.1 atm by adjusting the flow of exhaust gas from the chamber. The gas flows and the total pressure inside the chamber were programmed beforehand and automatically operated by a computer during MOVPE. The substrate for MOVPE was placed on a thin SiO_2 plate in the chamber. A graphite block beneath the SiO_2 plate was heated by RF induction, and the temperature of the graphite block was monitored with a thermocouple, whose output was fed into the RF-induction controller. The growth temperatures adopted for the heterostructure nanowires were controlled between 600 and 850°C. For example, when an axial heterostructure GaAs/GaAsP was grown, the

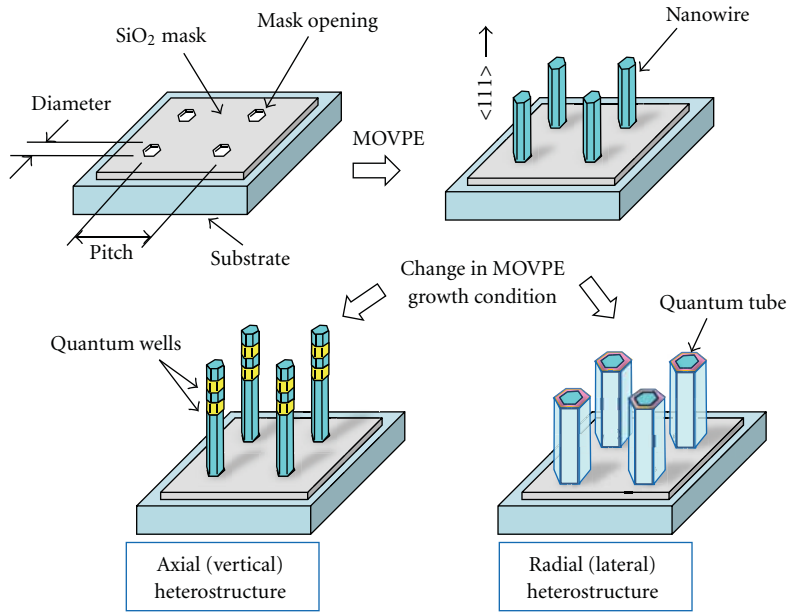


Figure 1: Schematic of process for forming heterostructure nanowires.

temperature was optimized to 750°C, while, for a radial heterostructure GaAs/GaAsP, the temperatures were 750°C for GaAs and 650°C for GaAsP. The pressure ratio of the group III source gases to the group V source gases (V/III ratio) was also changed over time with the control of growth temperature.

The nanowires that were grown were observed by scanning electron microscopy (SEM) to characterize their shape, growth direction, length, and diameter. Some nanowires were further investigated by transmission electron microscopy (TEM) with energy-dispersive X-ray (EDX) spectroscopy to analyze their crystal structure and atomic composition. Photoluminescence (PL) was measured to analyze the optical properties of the nanowires. A He–Ne laser in CW operation (wavelength: 632.8 nm) was used as an excitation source, and the laser light was focused to 2 μm in diameter with ×50 microscope objectives. We can measure PL from one nanowire or bundles of them depending on the pitch, wider or narrower than 2 μm. The PL from nanowire samples was guided into a monochromator (Acton SP-2300i; wavelength resolution of 0.1 or 0.4 nm) and detected with a charge-coupled-device (CCD) camera, which was also used to monitor images of the sample surface.

3. Heterostructure Growth in Axial Direction

3.1. GaAs/InGaAs Vertical Structures with InGaAs Quantum Well [28]. The structure for the nanowires (nanopillars) with a single InGaAs/GaAs quantum well (QW) grown along the ⟨111⟩B direction on the GaAs (111)B substrate surface (called sample I) is schematically shown in Figure 2(a). The growth temperature for the bottom and top GaAs barrier layers was 750°C, their growth times were 20 min for the bottom and 5 min for the top, and the partial pressure for AsH_3 was 2.5×10^{-4} atm and 1.3×10^{-6} atm for TMG. The growth temperature and the growth time for the InGaAs well layer was 600°C and 1 min, and the partial pressures for AsH_3, TMG, and TMI corresponded to 6.3×10^{-5}, 1.3×10^{-6}, and 1.2×10^{-7} atm. Under these conditions, the indium content for the InGaAs epitaxial layers grown on the GaAs (100) substrate and on the GaAs (111)B substrate were measured to be 5.5% for the former and 14.0% for the latter, which can be ascribed to fewer Ga atoms being incorporated on the GaAs (111)B substrate surface terminated with As atoms (As trimers), which are more stable at low growth temperatures, or at high As pressures [34–36]. We speculate that the As trimers impede Ga incorporation onto GaAs (111)B surface and this is why there is difference in the indium content for the InGaAs layers grown on the GaAs (100) and on the GaAs (111)B substrates. After the InGaAs well layer had been grown, a GaAs layer was grown at 600°C for 2 min under the same gas supply conditions as those for the bottom and top GaAs barrier layers, which were grown at 750°C.

The nanopillars with a single InGaAs/GaAs QW fabricated on the GaAs (111)B surface were characterized by SEM (Figure 2(b)). We can see the nanopillars are hexagonal and the top and side surfaces are very smooth, which indicates that six (1–10) facets and a top (111)B facet have been formed. The standard deviation in the diameter of the nanopillars is about 8%, and the standard deviation in their height is about 5%. Compared with planar (layer) growth (thickness of about 45 nm), the nanopillars are one order of magnitude taller (Figure 2(d)). This indicates that the nanopillar growth rate on the patterned substrate is greatly enhanced, which can be attributed to the migration of growth species containing Ga atoms and In atoms from the masked to the exposed region. The nanopillar growth

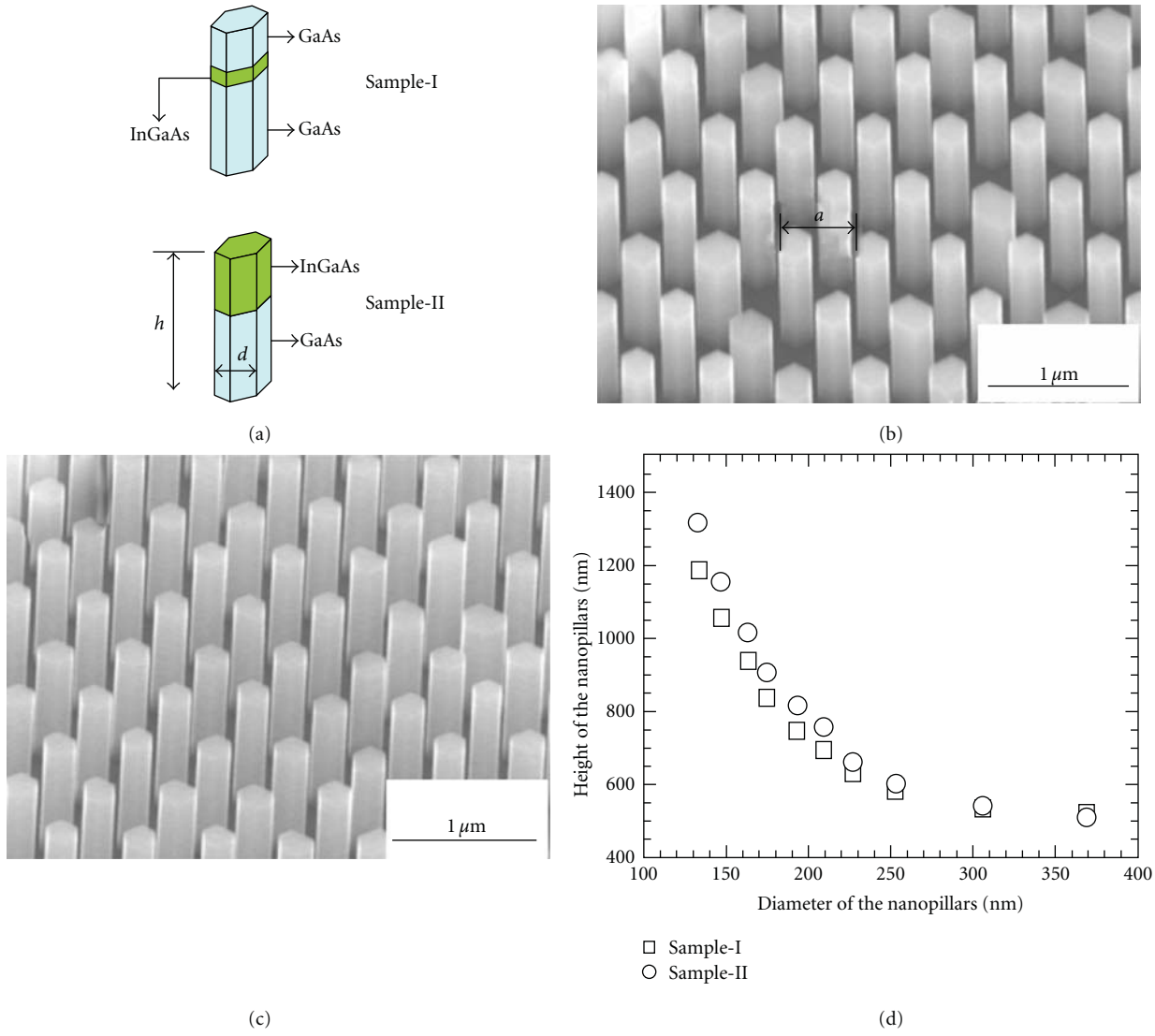


Figure 2: Structures of nanowire samples and SEM images of grown nanowires. (a) Schematics of structures for samples I and II. The nanowire diameter is defined by d. (b) SEM image for sample I. The nanowire pitch is defined by a. (c) SEM image for sample II. (d) Dependence of heights of samples I and II on their diameters [28].

rate is determined in the first approximation. We consider first the ratio of the radius of the collection region for the growth species (on the mask surface) to their diffusion lengths. Next we calculate the filling ratio in the masked pattern. The diffusion lengths for the growth species in the masked region are thought to be on the order of 1 μm and longer than the pitch of the nanopillars investigated here. The filling ratio in the masked pattern is given by $(d/a)^2$, where d and a are the nanopillar diameter and the pitch, respectively, and this was constant (0.09) in our samples for various d and a. Thus, the nanopillar growth rate was expected to be more or less independent of the pitch. However, this was not consistent with our experimental results, in which the nanopillar growth rate was larger for those with a smaller pitch. This peculiar dependence seems to be closely related to the unexpected dependence of the enhanced growth rate on pitch in the SA-MOVPE growth of GaAs nanowires that have previously been reported [37]. The explanation for the observation could be ascribed to the contribution of sidewall facets. Only the growth species on the masked region migrated to the exposed region and contributed to the initial stage of growth. The growth rate at this stage should be almost the same for all the nanopillars with different diameters. After the nanopillars were formed, six (1–10) facets appeared and started to absorb the growth species, which also migrated to the top (111)B facet and thus contributed to the growth of the nanopillars. We think that more growth species were absorbed by the six (11-0) facets as the nanopillar diameter was decreased, that is, the height of the nanopillars was increased with a decrease in the diameter even though the initial filling ratio in the masked pattern was the same.

To investigate whether the InGaAs layer had grown on the top (111)B facet or on the six (11-0) facets, only an

InGaAs layer was grown after the initial GaAs nanopillars (called sample II) (Figure 2(a)) had formed. The growth conditions were the same as those for the bottom two layers in sample I except that the growth time for the InGaAs layer was prolonged from 1 to 5 min. By comparing Figure 2(b) with Figure 2(c), we can see that sample I has almost the same diameter as sample II, while sample II is a little higher than sample I. The same phenomena also existed for the nanopillars with other diameters (Figure 2(d)), which indicates that the InGaAs layer had mainly grown on the top (111)B facet and the growth rate was larger than that for the GaAs layer. For example, the GaAs growth rate along the ⟨111⟩B was about 45 nm/min and the InGaAs was about 80 nm/min for the nanopillar diameter of 130 nm plotted in Figure 2(d).

The micro-PL (μ-PL) spectra for sample I were measured at room temperature (RT) and 77 K. The excitation beam from a He–Ne laser (wavelength: 632.8 nm) was focused to a spot of about 2 μm in diameter with a ×50 microscope objective and onto samples placed in a cryostat. Figure 3 has a schematic of a substrate with nanowires excited by a focused laser beam during PL measurements. The PL collected through the same microscope objective was detected with a liquid nitrogen-cooled CCD. At RT (Figure 4(a)), the peak located at about 870 nm originates from the band edge emission of the GaAs barrier layer, while the other peak located on the longer wavelength side originates from the first electron heavy hole excitonic recombination of the InGaAs/GaAs QW. The peak position shifts to the longer wavelength with an increase in the diameter of the nanopillars (called *red shift*). Red shift in the peak position can also be observed at 77 K (Figure 4(b)). We randomly measured the μ-PL at twenty different points in the same pattern and plotted the peak positions dependent on diameter in Figure 6 to reduce the possible effects of diameter and height fluctuations in the discussion on the origin of red shift. The peak position first shifts to the longer wavelength very quickly with an increase in the diameter of the nanopillars, and the shift then slows. We can speculate that the peak position of the nanopillars will approach the band-edge emissions (1018 nm at RT and 972 nm at 77 K) of the $In_{0.14}Ga_{0.86}$ As epitaxial layer grown on the GaAs (111)B substrate under the same conditions if their diameter becomes large enough. It should be noted that the shift in the peak position from the band-edge emission of the GaAs barrier layer is just 5 nm at RT and 3 nm at 77 K when the diameter of the nanopillars is reduced from 369 to 133 nm, which indicates that the quantum confinement effect in the radial direction is negligible and thus does not account for the large red shift that was observed. Since the height of the nanopillars increases with a decrease in their diameter, we can naturally deduce that the thickness of the InGaAs well layer also increases correspondingly. Therefore, the quantum confinement effect in the axial direction induces the shift in the peak position to the longer wavelength and not to the shorter wavelength with an increase in the height of the nanopillars. We think that this red shift is possibly due to the stoichiometry difference in indium content for nanopillars with different diameters.

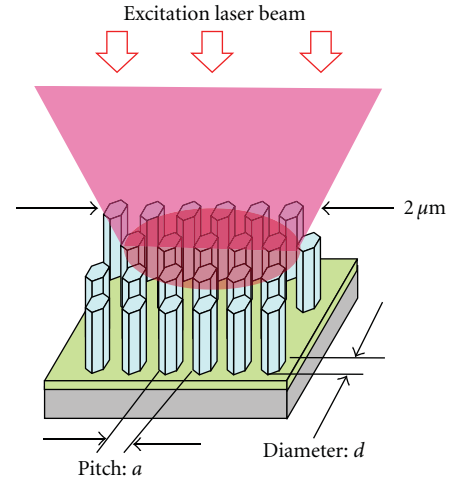


Figure 3: Schematic of substrate with nanowires irradiated by laser beam for PL measurements.

To confirm our speculation, we measured the μ-PL for sample II at five different points in the same pattern (Figures 5(a) and 5(b)) and plotted the peak positions dependent on diameter in Figure 6. The thickness of the InGaAs layer was estimated to be about 100 nm or more for the nanopillars with various diameters and thus could be approximately considered as the bulk material. The indium content was determined by fitting the experimental data with the *Varshni* formula [38], and this was partly confirmed by the energy disperse X-ray (EDX) spectrum (about 9%). We can clearly see that the indium content increases with an increase in the diameter of the nanopillars (Figure 6(c)). The indium content should be the same since the InGaAs layer had mainly grown on the top (111)B facet, if the ratio of the growth species containing Ga atoms to the growth species containing In atoms was the same for planar growth and for the growth on the top of the GaAs nanopillars. Consequently, the different indium content in the nanopillars with different diameters was due to the different diffusion coefficients between the growth species containing In atoms and the growth species containing Ga atoms on six (11-0) facets [39–41]. The growth species containing Ga atoms had larger diffusion coefficients on six (1–10) facets than the growth species containing In atoms under our growth conditions. The difference between the peak positions from the InGaAs layer in samples II and I reflects the quantum confinement effect. Since the thickness of the InGaAs layer increases with a decrease in the diameter of the nanopillars, the quantum confinement effect decreases correspondingly. The fluctuations in the peak position are enhanced at the lower temperature, particularly for sample I, which is probably due to the fluctuations in the indium content within the nanopillars and the localization of electron-hole pairs associated with it. The full width at half maximum (FWHM) (around 20 meV at 77 K) of sample I is larger than that of the general InGaAs/GaAs QW [42]. The main reasons are given here. Since the excitation spot was about 2 μm in diameter, the power density exposed onto the samples was estimated

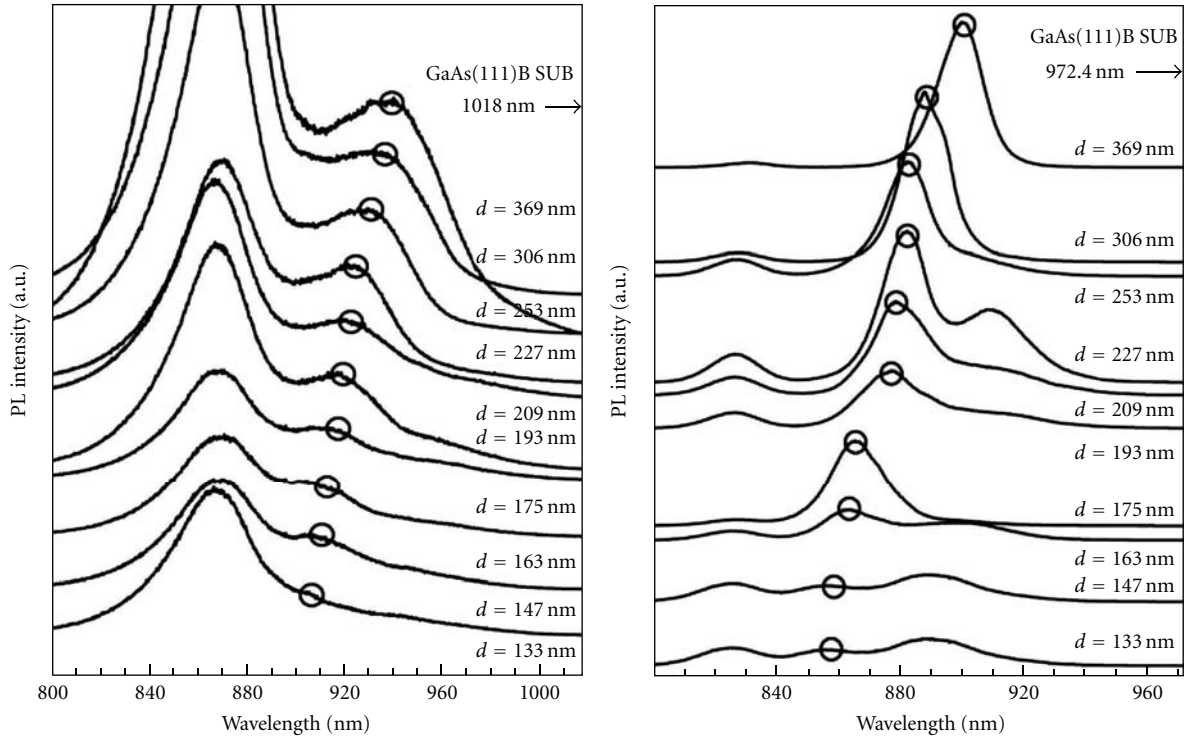


Figure 4: (a) Micro-PL spectra for sample I at room temperature (RT) and (b) at 77 K [28]. Open circles indicate the emission peaks of InGaAs.

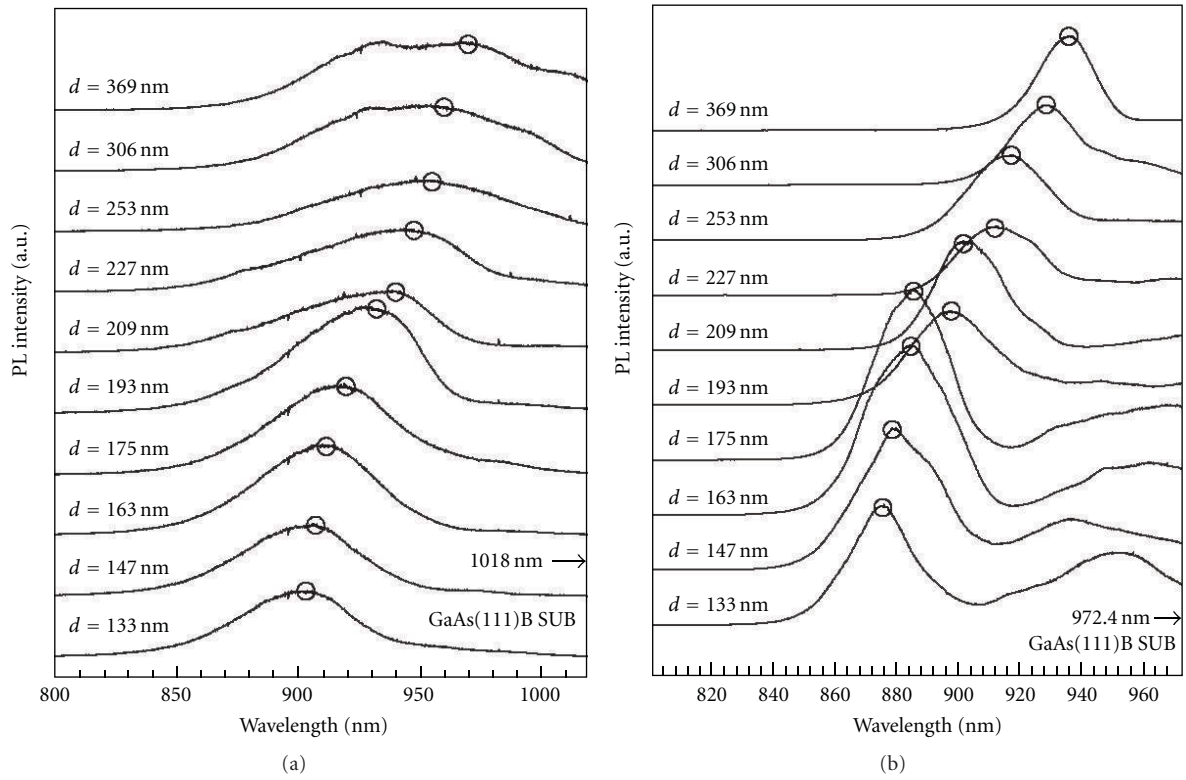


Figure 5: (a) Micro-PL spectra for sample II at RT and (b) at 77 K [28]. Open circles indicate the emission peaks of InGaAs.

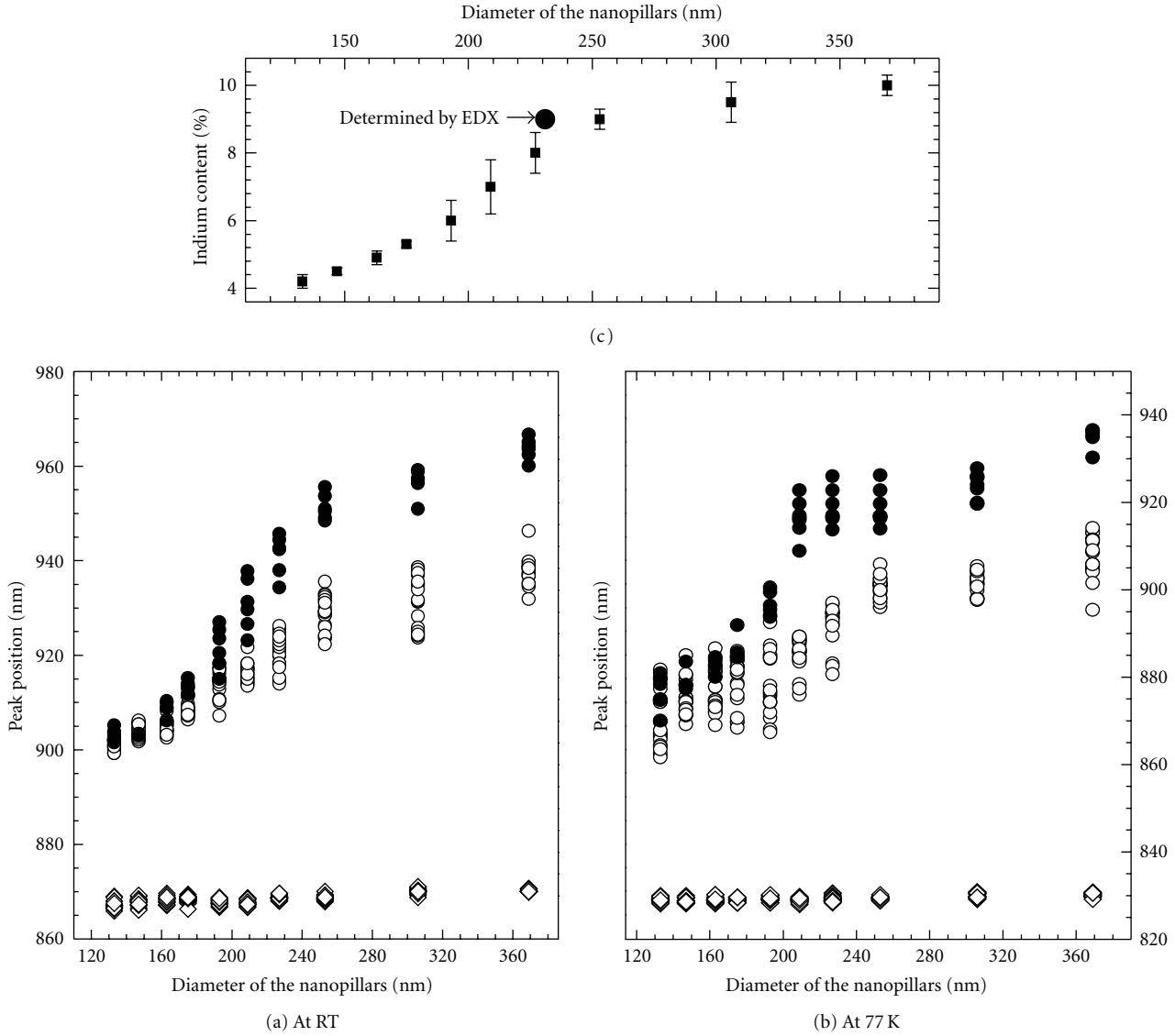


Figure 6: (a) Dependence of PL peak position on diameter of nanopillars at RT and (b) at 77 K. Dependence of indium content on diameter of nanopillars (c). Open diamonds stand for band-edge emission of GaAs barrier layer in sample I, open circles for first electron heavy hole excitonic recombination of InGaAs/GaAs QW in sample I, and filled circles for band-edge emission of InGaAs layer in sample II [28].

to be 1 kW/cm^2 and more than ten nanopillars were excited simultaneously. Under such high power excitation conditions, some optical recombination occurred at $k \neq 0$ and the PL spectrum was broadened [42]. Due to the diameter and height fluctuations of the nanopillars, the thickness of the InGaAs well layer fluctuated slightly for nanopillars with different diameters, which also enhanced the FWHM of sample I. Another possible reason for this large FWHM is the fluctuations in the layer thickness at the interface of the InGaAs/GaAs QW.

A more quantitative analysis of the PL spectra with a piezoelectric effect due to the lattice mismatched (strained) layer structure has been reported [43], where the InGaAs QW thickness along the ⟨111⟩ was estimated at 11.2 nm.

3.2. GaAs/AlGaAs Vertical Structure with GaAs Quantum Well [30]. AlGaAs/GaAs vertical heterostructure NWs are attractive for fabricating a NW light-emitting device at a wavelength of 850 nm. We could ignore the effect of lattice mismatching for the AlGaAs/GaAs heterojunction between GaAs and AlGaAs on the change in the bandgap energy of a GaAs QW compared with that of GaAs/InGaAs or GaAs/InGaP lattice-mismatched junctions. Therefore, we could control the emission wavelength of the GaAs QW by changing the size of the QW in the axial/lateral directions. To date, the number of reports on AlGaAs/GaAs heterostructure NWs with a GaAs QW contained along the axial direction has been limited [44–47], due mainly to difficulty in controlling the size and the shape of AlGaAs. We also need to control

and optimize the growth conditions to fabricate a QW or a quantum dot (QD) buried along the axial direction of NW.

The formation of an NW sample with a GaAs QW buried in AlGaAs began with GaAs core growth, followed by the growth sequence of an AlGaAs shell, a GaAs QW, an AlGaAs shell, and a GaAs cap layer. The growth temperature was 750°C for the GaAs core and QW layer, and the growth times were 5 min for the core and changed from 3 to 8 sec for QWs, respectively. The partial pressure for AsH_3 was 5.0×10^{-4} atm and 2.7×10^{-6} atm for TMG. Optimum growth conditions for the AlGaAs shell were chosen from preliminary experiments by changing the growth temperature between 800 and 850°C and the partial pressures of AsH_3 between 2.6×10^{-4} and 1.6×10^{-3} atm, TMG between 9.2×10^{-7} and 2.8×10^{-6} atm, and TMA between 1.6×10^{-7} and 4.8×10^{-7} atm. The optimum growth temperature and the growth time for the AlGaAs shell layer were 800°C and 2.5 min, where the partial pressures for AsH_3, TMG, and TMA corresponded to 7.8×10^{-4},1.8×10^{-6}, and 3.2×10^{-7} atm. After the GaAs QW layer had been grown, an AlGaAs layer was grown for 20 sec at 750°C under the same source gas pressures as those for the AlGaAs shell-layer growth, where the growth temperature was changed beforehand from 750 to 800°C and the growth time was 2.5 min.

To confirm whether the GaAs QW layer had grown on top of the (111)B facet or on the six (−110) side facets of the AlGaAs shell, a GaAs layer was grown after the GaAs/AlGaAs core-shell NW had formed. Figures 7(a) to 7(c) are SEM images of GaAs NWs, GaAs/AlGaAs core-shell NWs (core-shell NWs) and GaAs/AlGaAs/GaAs heterostructure NWs (heterostructure NWs). Figure 7(d) shows the relationship between the height and diameter of NWs corresponding to the three growth steps in Figures 7(a) to 7(c). Both the height and diameter of the NWs increased during the growth steps from the GaAs NW to the core-shell NW. From the comparison of the core-shell NW with the heterostructure NW, the heterostructure NW was higher by 300 nm on average than the core-shell NW, but the diameter increased by about 10 nm, which indicates that the GaAs layer grew dominantly on the top surface of the GaAs/AlGaAs core-shell NW. We think that once a very thin GaAs layer had been deposited on the side (−110) facets of AlGaAs, the thin GaAs layer masked the active AlAs surface and the surface diffusion length of Ga atoms increased to that of GaAs NW growth, as compared with the AlGaAs NW growth discussed in the previous section. Figures 7(e) to 7(h) demonstrate how the core-shell structure effectively reduced the NW diameter compared with an AlGaAs/GaAs NW structure grown without the GaAs core. As can be seen in the SEM images in Figures 7(g) and 7(h), we reduced the diameter of the GaAs top layer, by about 190 nm, to 150 nm. We could estimate the thickness of a GaAs layer deposited on the side facet of the GaAs/AlGaAs core-shell NW to be less than 0.3 nm from these results when a GaAs QW as thin as 10–20 nm was grown on top of AlGaAs.

Figure 8(a) shows SEM images of heterostructure NWs with a GaAs QW buried in AlGaAs shells and a schematic cross-sectional structure (on the left). The height of the NWs was about 1.2 μm, and their diameters were 180–260 nm. The diameter of the GaAs QW was assumed to be 140 nm for the structure, which was estimated from the change in NW diameters from the growth step of the core-shell NW to the heterostructure NW, as shown in the SEM images and the plot of the NW diameter in Figures 7(b), 7(c) and 7(d). We think that the dispersion of the diameter for the core-shell NW (about ±15 nm (±11%)) should be projected onto that of the GaAs QW. The diameter of the AlGaAs outer shell was designed to be about 180 nm (a target value) around the GaAs QW portion. Figure 8(b) shows the diameter distribution of the heterostructure NWs in Figure 8(a). We found that standard deviation of diameter σ_{diameter} of the NWs was about 29 nm and the uniformity of the diameter calculated using the ratio of $\sigma_{\text{diameter}}/d_{\text{ave}}$ (d_{ave}: average diameter) was 14%. The apparent asymmetry in the histogram of the NW diameter in Figure 8(b) might be specific to the GaAs/AlGaAs heterostructure NWs containing a GaAs QW. When we grew AlGaAs NWs at 800°C, the histogram of the diameter indicated a symmetric distribution with σ_{diameter} of 21 nm. Motohisa et al. [20] reported that the histograms for the diameter of GaAs NWs indicated a symmetric distribution with σ_{diameter} = 7–9 nm but the degree of symmetry was slightly affected by the proximity effect of electron-beam lithography when the pitch of the SiO_2 mask openings was reduced from 0.6 to 0.4 μm. The standard deviation (σ) of NW diameters for the AlGaAs NWs or the GaAs/AlGaAs heterostructure NWs with a GaAs QW was roughly 2–4 times larger than that for the GaAs NWs. We think the increase in diameter dispersion might be attributed to AlGaAs growth.

We measured the μ-PL of the heterostructure NWs at 4.2 K. A He–Ne laser (wavelength: λ = 632.8 nm) was used in this experiment as an excitation source with a maximum excitation power density of about 1 kW/cm^2 and was focused onto about a 2-μm diameter on the sample surface. Figure 9 shows the PL spectra for the three types of heterostructure NWs with a GaAs QW grown for growth times of 3, 5, and 8 sec. A PL spectrum of GaAs NWs has also been plotted as a reference. The pitch of the NWs plotted in Figure 9 was 1 μm. So the number of NWs excited by the laser beam was 3–5. The PL spectra for the three types of heterostructure NWs exhibit strong emission peaks near a photon energy of 1.5 eV, which might have originated from carbon acceptor-related recombination emissions. The PL spectrum of GaAs NWs also displays a main peak near 1.49–1.50 eV, which is about 20 meV below the second main peak at 1.515 eV, corresponding to band-to-band (band edge) recombination emissions. We can see a weak peak at 1.546 eV for the heterostructure NW with a GaAs QW grown at 8 sec. The peak energy shifted to 1.560 eV for the sample with a GaAs QW grown at 3 sec. Noborisaka et al. [29] reported that the PL intensity of GaAs NWs was an order of magnitude weaker than that of GaAs/AlGaAs core-shell NWs. Our results coincided well with their measurements, and we confirmed that the AlGaAs shell worked as a passivation site for the GaAs core NW. The PL intensity of the GaAs

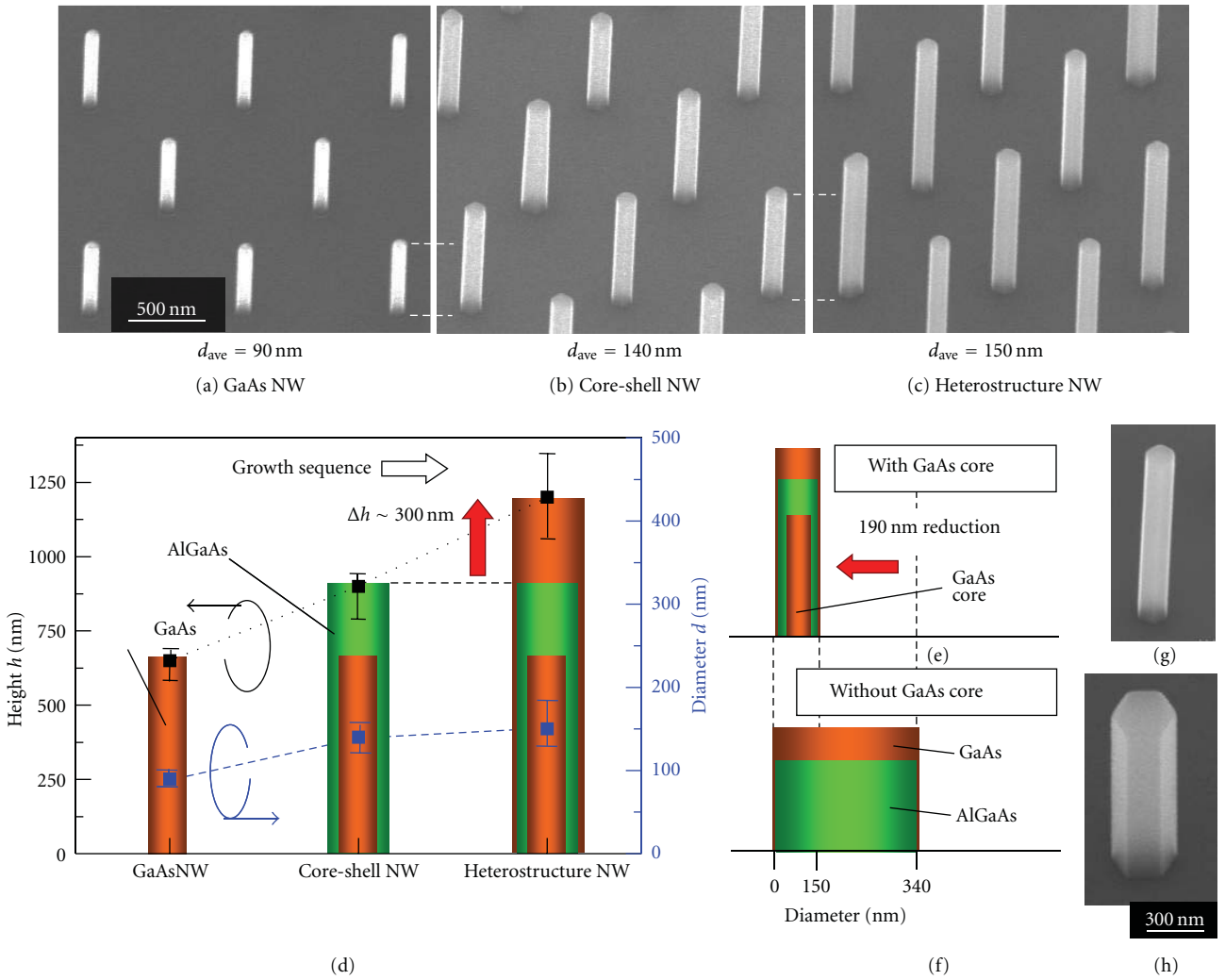


FIGURE 7: SEM images of NWs and changes in NW height and diameter. NW pitch $a = 1.0\,\mu$m and SiO_2 mask opening size $d_0 = 80$ nm. (a), (b), and (c) correspond to SEM images for GaAs NWs, core-shell NWs, and heterostructure NWs. White dotted parallel lines bridged between SEM images (a) and (b), or (b) and (c) clarify how NW height changed between growth steps. (d) Changes in height and diameter of NWs corresponding to growth steps of GaAs NW (GaAs core growth time: 5 min), GaAs/AlGaAs core-shell NW (AlGaAs shell growth time: 2.5 min), and GaAs/AlGaAs/GaAs heterostructure NW (top GaAs growth time: 2 min). (e) and (f) illustrate reduced NW diameter by introducing GaAs core. (g) and (h) are SEM images of NW grown with and without GaAs core, corresponding to schematics in (e) and (f). Growth time for AlGaAs is 20 min and 5 min for GaAs for structures in (f) and (h) [30].

QW was one order of magnitude weaker than that of the acceptor-related emissions shown in Figure 9. We believe this was caused by two factors. The first was that the volume of the GaAs QW was about 1/30 of that of the GaAs core. The second factor was that the Al composition of the AlGaAs NW measured using PL measurements (not shown here) was about 0.11, which was roughly equal to that of the outer shell measured using EDX. The difference in the energy bandgap between the GaAs QW and the AlGaAs shell was thus estimated to be as low as 0.11 eV, which is not sufficient to confine photoexcited carriers in the conduction band of the GaAs QW, compared with a GaAs QW sandwiched by AlAs barriers [48, 49]. The relatively broad spectral feature of the GaAs QWs, when compared with that of the acceptor-related emission peaks at 1.50 eV, might be originated from the dispersion in the GaAs QW thickness. We think this was caused by the dispersion in the NW height (Figure 8(a)).

We measured PL for three different areas on the sample surface for each growth time of the GaAs QW. Figure 10(a) plots the GaAs QW width (thickness along the ⟨111⟩ direction) estimated from the PL peak energy versus that calculated by the GaAs NW growth rate along the ⟨111⟩ direction. The inset in Figure 10(a) shows a dark-field scanning TEM (STEM) image of the top region of a heterostructure NW with a GaAs QW for a growth time of 5 sec. The depth profile for Al composition measured using EDX is plotted on the left side of the STEM image in Figure 10(a). The Al composition profile indicates different peak values above or below the GaAs QW. This could be attributed to different growth temperatures for the AlGaAs shells, but the reason

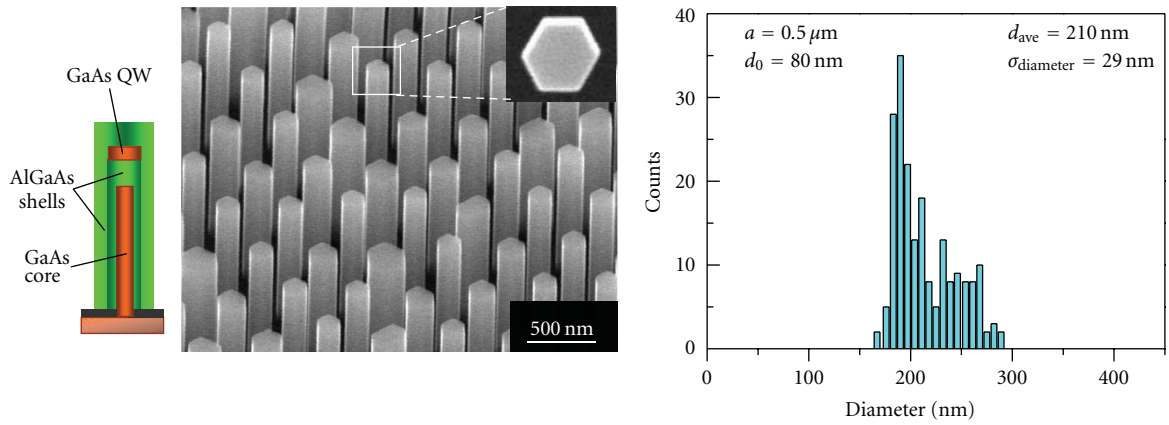


Figure 8: SEM images and schematic of structure of heterostructure NWs and distribution of diameters. (a) SEM images of grown NWs and schematic of cross-sectional structure of NW containing GaAs QW. GaAs cap layer is not shown in schematic. Inset SEM image in upper right is top view of NW. (b) Histogram of diameter distribution for NWs with pitch of $a = 0.5\,\mu$m [30].

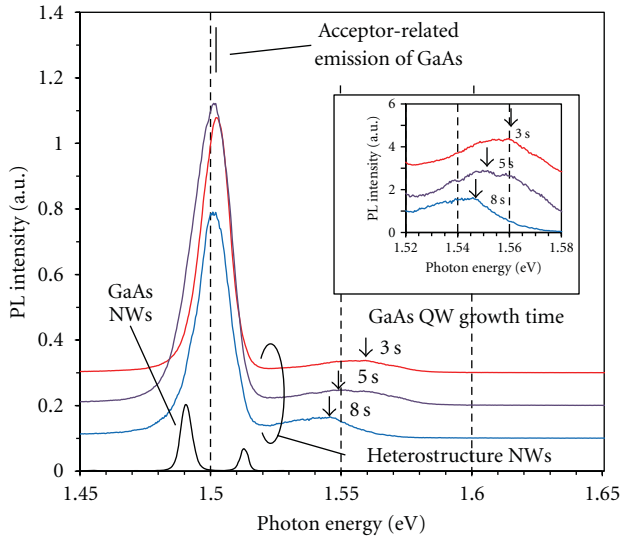


Figure 9: PL spectra for three types of heterostructure NWs with a GaAs QW grown for 3, 5, and 8 sec and GaAs NWs (as a reference) measured at 4.2 K. NW pitch was 1 μm for all the NW samples. Inset is enlarged spectra for the GaAs QWs [30].

is not entirely clear. Figures 10(b) and 10(c) show a bright-field STEM image and a transmission electron diffraction pattern for the heterostructure NW, the analyzed part is corresponding to a segment from the GaAs QW region to the NW's top. There is a high-resolution TEM image of a center part of the NW top in Figure 10(d). There is a dark-field STEM image in Figure 10(e) corresponding to the top half of that in Figure 10(a). We found that the heterostructure NW with a GaAs QW had stacking faults perpendicular to the ⟨111⟩ direction, which are distributed along the ⟨111⟩ with a frequency ranging from a few nanometers to 20 nm as can be seen in Figure 10(b). The crystal structure was found to be zincblende with rotational twins around the ⟨111⟩ axis (Figure 10(c)). The stacking faults originated from the rotational twins, which was confirmed by the change in the alignment of lattice image, and the positions are indicated by the arrows on the high-resolution TEM image taken near the top surface of the NW in Figure 10(d). In Figure 10(e), the positions for the GaAs QW and the AlGaAs barriers are indicated by the broken arrowed lines, which are corresponding to the areas of light-and-dark contrast on the STEM image except for the fine ones caused by stacking faults. We found that some of the stacking faults were distributed in the GaAs QW region from the STEM images in Figures 10(b) and 10(e). We think that the stacking faults developed at some stages of layer growth along the ⟨111⟩B direction. But it is not clear whether they propagated from the GaAs core to the AlGaAs shell.

We used formulas for the optical transition between the energy levels of electrons and holes to obtain the QW width from the PL measurements, which are given below [49, 50]:

$$\hbar\omega = E_g(\text{GaAs}) + E_1 + E_{\text{hh1}}, \tag{1}$$

and quantized energy level E for electrons or holes with effective mass m is given by

$$E = \left(\frac{\hbar^2\pi^2}{2m}\right)\left(\frac{n}{L_{\text{QW}}}\right)^2, \tag{2}$$

where $\hbar = h/2\pi$ (h: Planck's constant), ω is the angular frequency of light, and E_g(GaAs) is the GaAs bandgap. Here, n is a positive integer, E_1 is the lowest energy level of electrons in the conduction band, E_{hh1} is the lowest energy level of heavy holes in the valence band, and L_{QW} is the width of the GaAs QW along the axial direction of the NW. The effective masses for the electrons and heavy holes used for fitting were $m_e^* = 0.067$ and $m_{\text{hh}}^* = 0.45$ [49, 50]. For the strict treatment of the PL peak energy analysis of the GaAs QWs, we need to consider the finite energy barriers of AlGaAs, but here we assumed that the energy barrier height was infinite

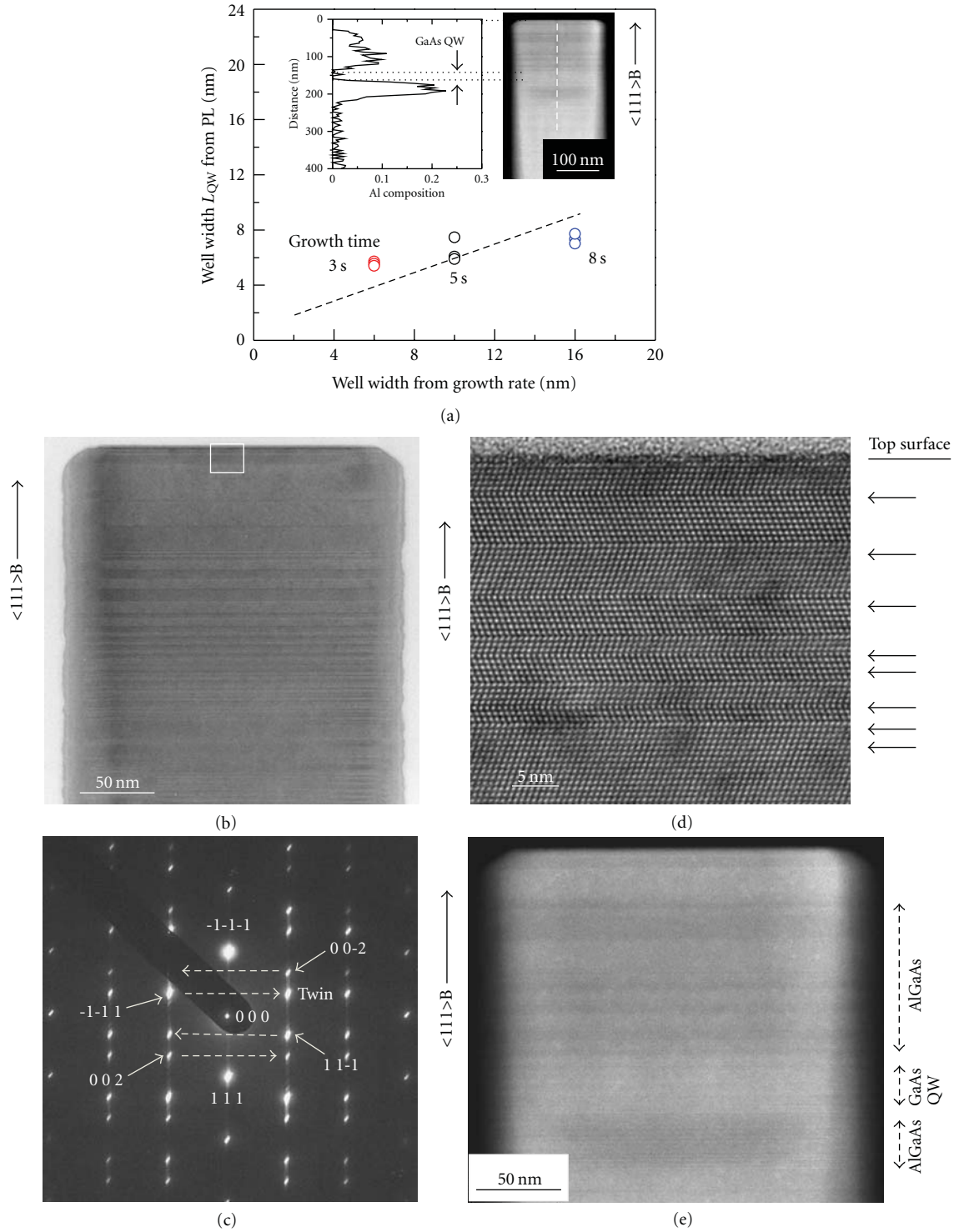


FIGURE 10: GaAs QW width calculated from PL spectra and growth rate and analysis by TEM. (a) Comparison of GaAs QW width obtained from PL peak energy with that estimated from axial growth rate of GaAs NW. NW pitch was 1 μm. Inset in upper right is dark-field STEM image of heterostructure NW taken with electron-beam direction parallel to $\langle -110 \rangle$. Inset at left above has depth profile of Al composition measured from top of NW by using EDX, which indicates GaAs QW portion sandwiched by AlGaAs. White broken line along $\langle 111 \rangle$ direction on STEM image indicates path scanned by electron beam for EDX. (b) Bright-field STEM image of NW. (c) Transmission electron diffraction pattern. (d) High-resolution TEM image of NW top portion indicated by white rectangle on STEM image of (b). Twin boundaries are indicated by arrows. (e) Dark-field STEM image of (b). Layer positions of GaAs QW and AlGaAs barriers estimated along $\langle 111 \rangle$ direction are indicated by broken arrows [30].

and quantum confinement was only in the ⟨111⟩ direction and ignored lateral confinement perpendicular to the ⟨111⟩ direction for simplicity. We find this simple approximation can give some difference in the QW thickness (Figure 10(a)). The depth profile of the Al composition shown in the inset in Figure 10(a) indicates that a GaAs QW with a thickness of 5–20 nm was formed about 150 nm from the top surface of the heterostructure NW. The position of the GaAs/AlGaAs heterojunction interface looks diffuse (showing ambiguity of ±10 nm) from the dark-field STEM image in Figure 10(e), but we could estimate the thickness of the GaAs QW along the ⟨111⟩ was roughly 30 nm, which is wider than that obtained by EDX. We could not find the GaAs/AlGaAs core-shell interface along the lateral direction of the GaAs QW in the dark-field STEM image, because we could hardly see any light-and-dark contrast laterally. Tambe et al. [51] discussed the heterojunction interface structure of a GaAs/$Al_xGa_{1-x}As$ core-shell NW from the images obtained with dark-field STEM. They used an Al composition of $x = 0.9$ for the sample, and they obtained high contrast at the interface. We think the difference in the GaAs QW thickness measured by EDX and that from the STEM image was caused by low Al content in the AlGaAs barriers compared with the one that Tambe et al. reported. The GaAs QW thickness measured using EDX is in fair agreement to a certain extent with that estimated with the PL spectra or the GaAs NW growth rate for the QW growth time of 5 sec. The results obtained by PL measurement combined with TEM/EDX analysis indicate successful fabrication of the GaAs QW using SA-MOVPE.

Figure 11 shows the PL spectra for heterostructure NWs with a GaAs QW grown with different NW pitches from 0.5 to 3.0 μm. The growth time for the GaAs QW was 5 sec. We found a broad weak peak for the GaAs QW at the 50–70 meV higher energy side of a strong emission peak near 1.5 eV, corresponding to acceptor-related recombination emissions. The broad weak peak position shifted to a higher energy region from 1.548 to 1.567 eV as the NW pitch increased from 0.5 to 3.0 μm. We found the PL intensity weakened as the NW pitch changed from 0.5 to 3 μm. This was caused by the decrease in the number of NWs excited by the laser beam as the pitch increased. The graph in the inset at the upper right of Figure 11 indicates that the GaAs QW width estimated from the PL peak energy decreased as the NW pitch increased. This means the GaAs growth rate along the ⟨111⟩B direction decreased on top of AlGaAs as the NW pitch increased, which is further evidence of the dependence of the growth rate of GaAs NWs on the NW pitch discussed by Noborisaka et al. [34]. The broad distribution of GaAs QW thickness along the ⟨111⟩ direction might be a cause of the broad PL peaks for the GaAs QW compared with the relatively sharp acceptor-related emission peaks of the GaAs core. We found that there was a distribution of NW heights, as can be seen from the SEM image in Figure 8(a). The change in NW heights implies a distribution of GaAs QW thicknesses buried inside, which means spectral broadening of PL.

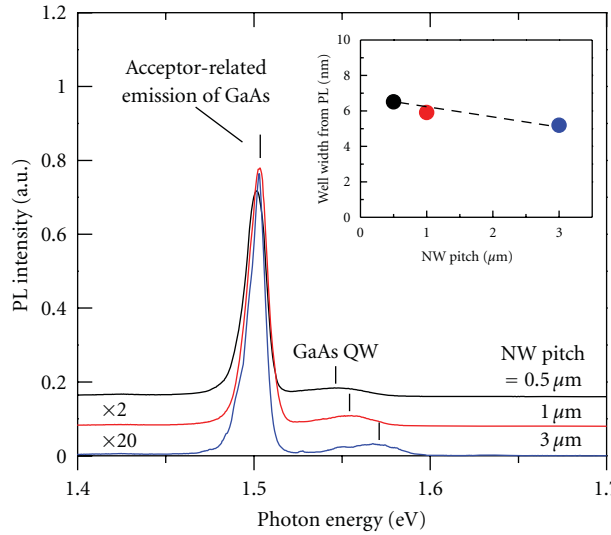


Figure 11: Dependence of PL spectra on NW pitch for heterostructure NWs containing GaAs QW. Graph in insert indicates GaAs QW width as function of NW pitch [30].

3.3. GaAs/GaAsP Vertical Structure with GaAs Quantum Well [33]. Another material we used as a barrier layer when fabricating a vertical heterostructure with a GaAs QW was GaAsP, which should be less affected by oxidation compared with materials containing Al like AlGaAs. Several reports have been published on GaAsP NW growth [52–55], but, to the best of our knowledge, only one [32] has been published on such growth using a catalyst-free method. Here we start with GaAsP NW growth then discuss GaAs/GaAsP heterostructure fabrication.

The source materials were TMG, tertiarybutylphosphine ($(C_4H_9)PH_2$: TBP), and AsH_3 (20% in hydrogen). The growth temperatures of GaAsP NWs ranged between 750 and 775°C, and the growth time was 20 min. The partial pressures of TMG were from 2.7×10^{-6} to 4.1×10^{-6} atm, those of TBP were from 4.2×10^{-5} to 2.5×10^{-4} atm, and those of AsH_3 were from 4.2×10^{-5} to 2.5×10^{-4} atm. The (TBP + AsH_3)/(TMG) ratios (V/III ratios) were from 20 to 185. The optimum growth conditions for the GaAsP NWs were chosen from preliminary experiments on GaAsP NW growth. The optimum growth temperature and growth time for the GaAsP NWs were 750°C and 5 min, where the partial pressures for TMG, TBP, and AsH_3 were 4.1×10^{-6}, 8.3×10^{-5}, and 8.3×10^{-5} atm, respectively. The V/III ratio was 20.

Figure 12 shows SEM images of GaAsP NWs grown at a V/III ratio of 20. We can see that the NWs have hexagonal and triangular structures and crystal facets, which indicate the formation of (−110) equivalent side facets and a top (111)B facet. The NW diameter was rather dispersed compared with that of GaAs NWs, as can be seen in Figure 12. This might be attributable to As- and *P*-contained NW growth, but the reason is not yet clear.

Figure 13 shows the PL spectrum of GaAsP NWs grown at the V/III ratio of 20. The PL spectrum of the GaAs substrate has also been plotted with the blue line as a

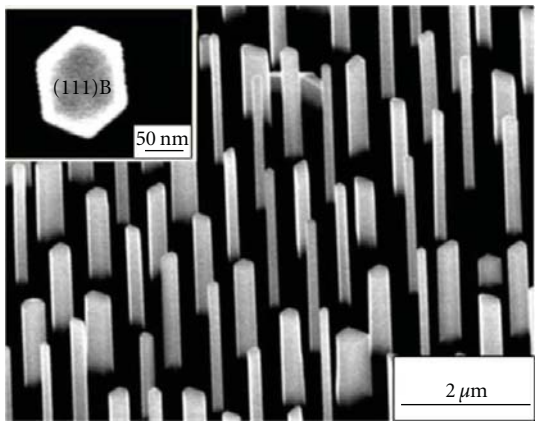


Figure 12: SEM images of GaAsP NWs grown at 750°C with V/III ratio of 20. Upper left inset is SEM image of top view of NW [33].

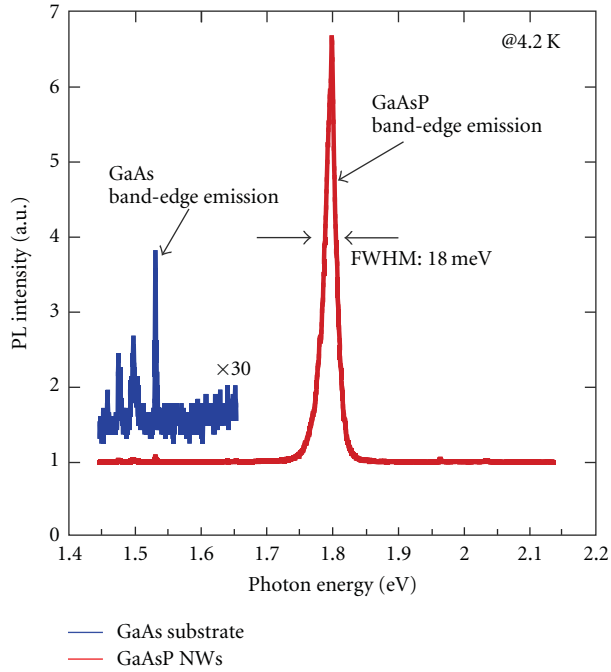


Figure 13: PL spectra for GaAsP NWs and GaAs substrate at 4.2 K [33].

reference. The number of NWs excited by the laser beam was about 3–5 for the sample with a pitch of 1 μm. The PL spectrum of GaAsP NWs had a strong emission peak at a photon energy of 1.80 eV, which is clearly different from the main peak of the GaAs substrate. The full width at half maximum (FWHM) of the PL spectrum of the NWs was 18 meV. The PL peak energy and the FWHM did not change when we changed the position of laser excitation on the sample surface. This indicates that GaAsP NWs with an equal atomic composition were formed within the NW grown area. The FWHM values for the GaAsP NWs were as narrow as those for the InGaAs NWs [35]. We estimated the solid P atomic content at 25% from the PL peak energy, that is, $GaAs_{0.75}P_{0.25}$ (single crystal $GaAs_{1-x}P_x$ layers had a direct bandgap between the valence band and the conduction band when solid P atomic content x was less than 0.44 [56]).

Here, we will explain the fabrication process for a GaAs QW buried in a heterostructure NW and the PL analysis to which it was subjected. To form a GaAs QW on top of a GaAsP NW and confine carriers in the QW three-dimensionally, uniform hexagonal pillar structures with a reduced diameter should be formed. However, growing a GaAs QW directly onto the GaAsP NWs was a major challenge, because laterally growing GaAsP still created problems in forming a NW with a reduced diameter of less than 100 nm and good uniformity in shape for the NW array. To solve this, we selected a method of growing a GaAs NW (height: about 500 nm, diameter: about 60 nm) before we grew the first GaAsP NW shell and then grew a GaAs QW on top of the first GaAsP NW shell, which was similar to the procedure for growing the GaAs/AlGaAs vertical heterostructure with a GaAs QW [30]. We used a single growth temperature of 750°C and a V/III ratio of 20 to form the heterostructure based on the optimum growth conditions for GaAsP NWs.

Figures 14(a) and 14(b) show SEM images of heterostructure NWs with a GaAs QW buried in GaAsP and a schematic cross-sectional structure (on the right of Figure 14(b)). The pattern pitch and the mask-opening diameter we designed were 3 μm and 60 nm. The NW height and diameter were approximately 630 nm and 80 nm. The GaAs QW diameter was assumed to be 70 nm for the structure, which was estimated from the changes in diameter from GaAs (growth time: t_g = 5 min)/GaAsP (t_g = 5 min) single-heterostructure NWs to GaAs (t_g = 5 min)/GaAsP (t_g = 5 min)/GaAs (t_g = 5 min) double-heterostructure NWs. By comparing the heterostructure NW (Figure 14) with the GaAsP NW (Figure 12), we can see that the uniformity in diameter was considerably improved by introducing GaAs NW growth before heterostructure growth.

We measured the μ-PL of the heterostructure NW with a GaAs QW buried in GaAs/GaAsP NWs. Figures 15(a) and 15(b) show the PL spectra of the heterostructure NWs with a GaAs QW grown with different growth times (t_{QW} = 1.5, 3.0, and 4.5 sec) and different NW pitches (0.5, 1.0, and 3.0 μm). A PL spectrum of a GaAs/GaAsP heterostructure NW (single heterostructure NW without QW) has been plotted in Figure 15(a) as a reference. The NW pitch is 3 μm, and one NW was excited by the laser beam for the spectra in Figure 15(a). The PL spectra for the four types of NWs in Figure 15(a) and for the three types of NWs in Figure 15(b) have strong emission peaks near a photon energy of 1.5 eV, which might have originated from the carbon acceptor-related recombination emissions in GaAs [57]. A short but clear peak for GaAs band-edge (band-to-band recombination) emissions can be confirmed at 1.515 eV, which is on the slightly higher energy side of the acceptor-related emission peak of GaAs. The peaks for GaAs band-edge emissions at 1.515 eV were not observed for the GaAs/AlGaAs heterostructure NWs discussed in the previous section. We think this is a clear difference between

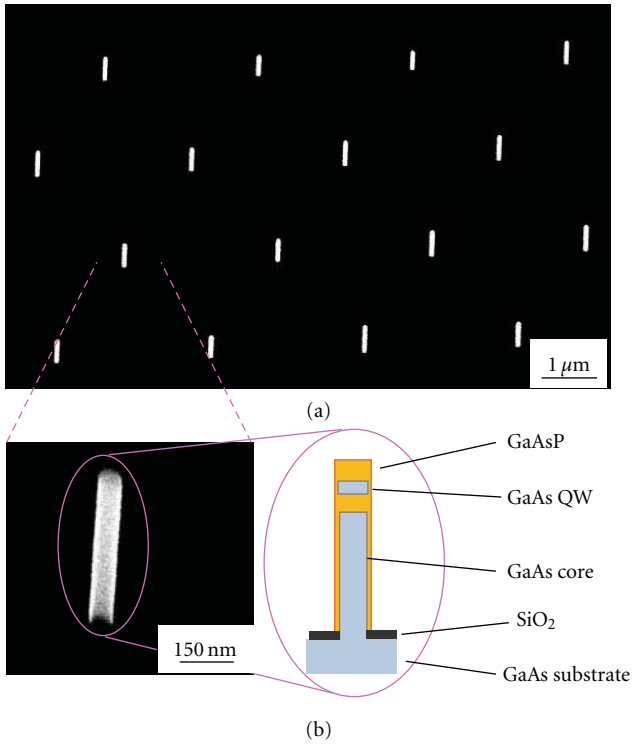


FIGURE 14: SEM images of heterostructure NWs with GaAs QW buried in GaAsP and schematic cross-sectional structure of NW containing GaAs QW. SEM image at lower left is enlarged view of NW [33].

the GaAs/GaAsP NWs and that GaAs/AlGaAs, whose quality might be affected by Al oxidation. The PL spectrum for the single heterostructure NW also indicates the main peak at 1.8 eV, which is almost the same as that of the GaAsP NWs with the pitch of 1 μm (Figure 13). This indicates that the atomic content of the GaAsP shell was independent of the pitch. We can see clear emission peaks between 1.60 and 1.62 eV for the heterostructure NWs with a GaAs QW, which is on the higher energy side of acceptor-related emissions and on the lower energy side of the GaAsP NW peak at 1.8 eV. The emission peak energy for the GaAs QW was increased as the time to grow the QW was decreased (Figure 15(a)) or the NW pitch was increased (Figure 15(b)). The GaAs QW thicknesses along the ⟨111⟩ direction estimated by using the PL peak energy in Figures 15(a) and 15(b) and the approximation in the previous section (1) and (2) were 5.7–6.0 nm, which were roughly equal to those grown sandwiched between AlGaAs. The number of NWs excited by the laser beam was about 10–12 for the sample with the pitch of 0.5 μm and about 3–5 for the sample with the pitch of 1 μm. We estimated that the greater the number of NWs, the larger the dispersion of QW thicknesses. This is why the FWHM of the PL peak for the QW increased from 10 to 20 meV as the pitch was decreased from 3.0 to 0.5 μm, as can be estimated from the PL spectral shapes in Figure 15(b). The relative PL intensity of the QW compared with that of the acceptor-related emission peak at 1.5 eV for the GaAs/GaAsP structures (Figures 15(a) and 15(b)) is one order of magnitude greater than that for the GaAs/AlGaAs structures (Figures 9 and 11). Moreover, the FWHMs of the PL peaks for the QWs buried in GaAsP were smaller, by 30–50%, than those buried in AlGaAs (Figures 9 and 11). This indicates that we can obtain GaAs QWs of better quality in GaAs/GaAsP NWs than in GaAs/AlGaAs NWs.

We carried out measurements with TEM/EDX to investigate the atomic content around a GaAs QW buried within GaAsP barrier layers. Figures 16(a) to 16(c) show dark-field STEM (DF-STEM) images and profiles of the atomic content of Ga, As, and P measured along and across the ⟨111⟩ direction. The DF-STEM image of the NW top portion is shown in Figure 16(b), in which a GaAs core and a GaAs QW are identified as bright portions compared with a relatively dark GaAsP portion. It should be observed that stacking faults (rotational twins around the ⟨111⟩ axis) contained in the NW appear as segments with light-and-dark contrast in the STEM image. The atomic content profiles for Ga, As, and P detected by EDX scanned across the QW region (along the ⟨111⟩ direction) and the NW trunk with the GaAs core are plotted on the right side of the STEM image in Figure 16(b). The profiles indicate that the QW, which is 10-nm thick, is located 70 nm below the NW's top, is separated 37 nm from the GaAs core, and is buried in $GaAs_{0.80}P_{0.20}$. The GaAs QW thickness measured from the EDX profile is roughly equal to that calculated from the GaAs growth rate along the ⟨111⟩ direction and that obtained from the PL peak energy. We found that the GaAs core NW was not capped by a GaAsP layer within the resolution limit of EDX from the atomic content profile around the bottom half of the trunk shown in Figure 16(c).

4. Heterostructure Growth in Radial Direction

Radial (core-shell) heterostructure nanowires enable the passivation of interface states and thereby improve the overall performance of the semiconductor devices that result from these. Core-multishell nanowires formed by sequential modulation of the composition along the radial direction offer the distinct ability of enabling multifunctions to be incorporated into individual nanowires.

4.1. GaAs/AlGaAs Core-Shell Structure [29]. The formation of core-shell heterostructures by using lateral growth of AlGaAs shows an increase in the photoluminescence intensity in nanowires. We grew GaAs and AlGaAs in succession for core-shell heterostructures. The partial pressure of TMG for GaAs was 2.7×10^{-6} atm and that for AsH_3 was 5.0×10^{-4} atm. The partial pressures in the growth of the AlGaAs shell of the total group III precursors and AsH_3 were the same as for GaAs growth. The growth temperature was 750°C for GaAs and 850°C for AlGaAs. Perfect selective epitaxy of both GaAs and AlGaAs was achieved under these conditions. The growth time was 20 min for GaAs and from 10 to 40 min for AlGaAs. Figure 17(a) is an SEM image of GaAs nanowires before AlGaAs was grown. A periodic array with a pitch of 1 μm of free-standing GaAs nanowires with a height of 3 μm was formed in the mask openings. The cross-section of the

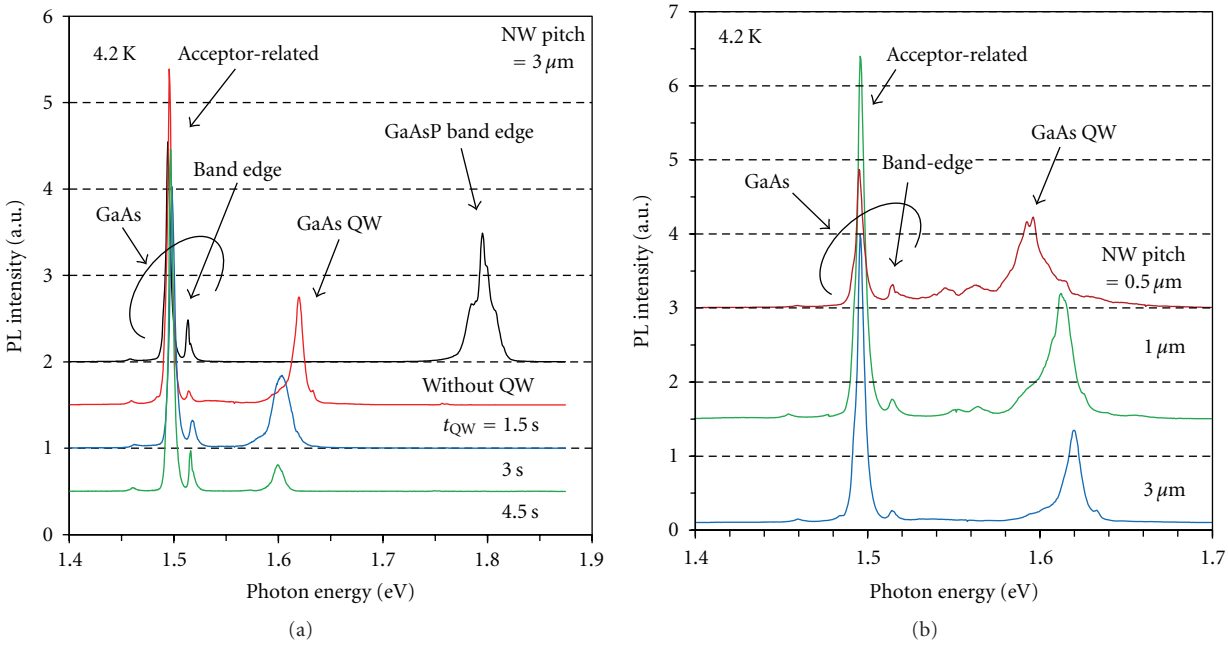


FIGURE 15: 4.2-K PL spectra for heterostructure NWs with GaAs QW buried in GaAsP. (a) PL spectra for NWs with GaAs QW for growth times (t_{QW}) of 1.5, 3.0, and 4.5 sec. NW pitch is 3 μm. PL spectrum for GaAsP/GaAs heterostructure NW without QW has been plotted as reference. (b) PL spectra for NWs with GaAs QW for NW pitches of 0.5, 1.0, and 3.0 μm. t_{QW} is 1.5 sec.

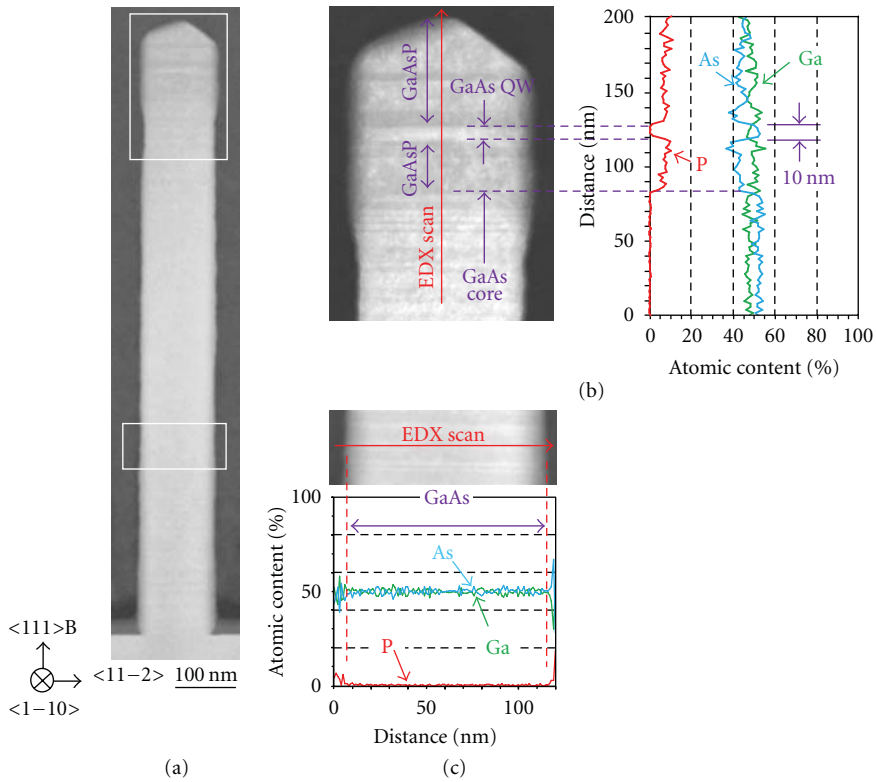


FIGURE 16: TEM/EDX analysis of heterostructure NW with GaAs QW. (a) Dark-field STEM (DF-STEM) image of NW. (b) DF-STEM image at top of NW of (a) and atomic content profiles for Ga, As, and P measured by EDX. (c) DF-STEM image at center-bottom part of NW and atomic content profiles obtained by EDX.

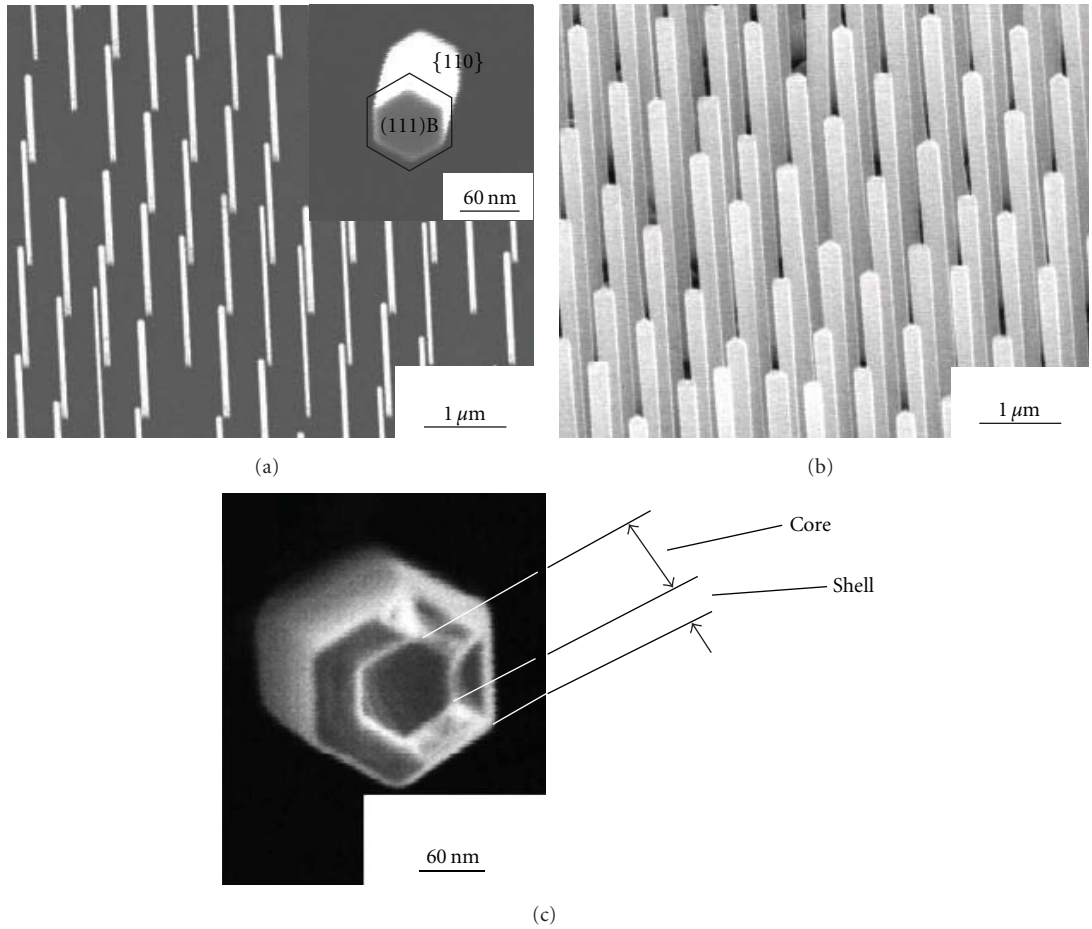


Figure 17: SEM images of grown nanowires. (a) SEM images of GaAs nanowires. Inset has image of nanowire from top. (b) SEM image of nanowires after growth of AlGaAs. (c) Top-view SEM image of GaAs/AlGaAs core-shell nanowire after preferential etching [29].

nanowires is hexagonal with well-defined sidewalls, as can be seen from the inset. Their diameters d are from 50 to 100 nm. Nonuniformity in their size originated mainly from the irregular mask-opening sizes. Figure 17(b) shows an SEM image of AlGaAs growth on GaAs nanowires. The growth time of AlGaAs was 10 min. Although they maintained their hexagonal shapes, we found that the nanowires became taller (5 μm) and thicker (200–300 nm).

Figure 17(c) has a top-view SEM image of a GaAs/AlGaAs core-shell nanowire after a two-step etching process; specifically, anisotropic dry etching followed by preferential wet etching on core-shell nanowires. We used reactive ion-beam etching for dry etching with CH_4, H_2, Ar, and N_2 for 30 min and used a mixture of NH_4OH and H_2O_2 for wet etching. We can clearly distinguish the GaAs core part with a diameter of 100 nm from the AlGaAs shell with an outer diameter of 200 nm from Figure 17(c). Here, the AlGaAs shell remained as a nanotube after the etching process. Figures 17(a) to 17(c) also indicate that AlGaAs was grown laterally on the sidewalls of GaAs nanowires as well as on their tops.

Lateral growth was confirmed by the dependence of nanowire diameter on the AlGaAs growth time shown in Figure 18. We concluded from these results that free-standing GaAs/AlGaAs core-shell nanowires had been formed by using SA-MOVPE. In Figures 17(a)–17(c), the thickness of the AlGaAs shells is 75–100 nm, and the top of the nanowires is capped with 2-μm-long AlGaAs. If we subtract the length of the capped AlGaAs on the top, the aspect ratio of the core-shell part of the nanowires is about 10. As has previously been reported [37], the sidewalls of GaAs hexagonal nanowires are (110) facet surfaces, vertical to the (111) plane. The appearance of these facet sidewalls is because their growth rate is slower than that of (111)B. In addition, we found that diameter d of the nanowires is equal to mask-opening diameter d_0 [37]. This means that the growth on (110) sidewalls is negligible for GaAs grown under the present conditions. Growth, on the other hand, takes place on the sidewall surfaces laterally as well as on the top surfaces for AlGaAs. Ando et al. have reported enhanced lateral growth of AlGaAs on the (110) sidewalls of selectively grown GaAs wire structures on (111)B under slightly different conditions [58]. The enhanced lateral growth on the sidewall (110) facet in AlGaAs could be explained by a stronger bonding and a shorter migration length of Al atoms on (110) surfaces.

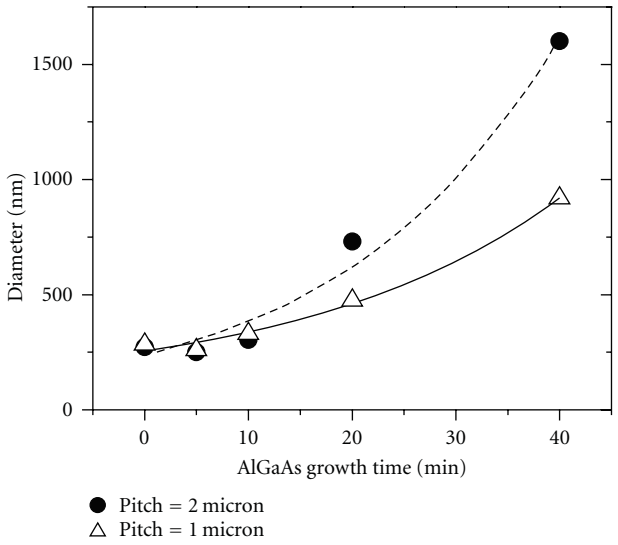


Figure 18: Dependence of nanowire thickness on AlGaAs growth time. Initial GaAs nanowire diameter was 270 nm. Nanowire diameter increased with AlGaAs growth time [29].

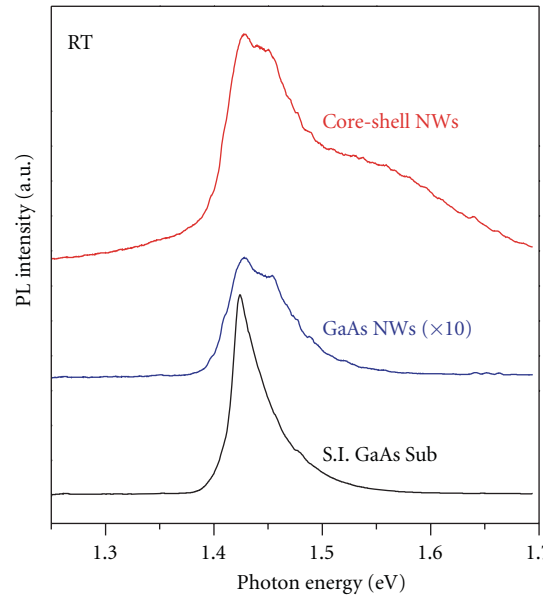


Figure 19: PL spectra of core-shell nanowires (NWs), bare GaAs nanowires, and reference semi-insulating GaAs substrate. Intensity of core-shell nanowires is about 20 times larger than that of bare GaAs nanowires [29].

To obtain the results given in Figure 18, we conducted an experiment on growing GaAs nanowires using larger mask openings and pitches to minimize the effect of irregular mask opening sizes than those used to grow the nanowires shown in Figures 17(a) and 17(b). The diameter of GaAs nanowires we obtained in this experiment was 270 nm, and their typical size fluctuations were on the order of several percent [20]. We found that the amount of AlGaAs lateral growth was nonlinear and depended on pitch a of the mask openings. Furthermore, as mentioned earlier, the amount of lateral growth for a 10-min growth time was estimated to be 75–100 nm for the nanowires when d = 50–80 nm, whereas it was negligible in the results presented in Figure 18. These findings mean that the lateral growth rate of AlGaAs is critically dependent on the size and arrangement of nanowires. Further studies are needed to clarify the details of the growth process.

Next, we conducted μ-PL measurements of GaAs and GaAs/AlGaAs nanowire arrays at 290 K. An He–Ne laser was used for excitation in this experiment, and the excitation intensity was 60 μW (power density of about 1 kW/cm^2). Figure 19 shows the μ-PL spectra of GaAs and core-shell nanowires. The average diameters of the nanowires are 80 nm for GaAs and 300 nm for the core-shell, and the pitch of the array is 0.4 μm. A PL spectrum of a semi-insulating (S.I.) GaAs substrate has also been plotted for reference. We can see some differences between the two types of nanowires and the reference. First, the PL intensity of the core-shell nanowires was much stronger than that of bare GaAs nanowires by a factor of about 20, and almost equal to that of the S.I. GaAs substrate. The weak emission from GaAs nanowires can be explained by the nonradiative recombination of photoexcited carriers at the air-exposed GaAs sidewall surface where there is a high density of surface states. The recovery of PL intensity in core-shell structures can also be explained by the surrounding AlGaAs barrier that prevents the coupling of photoexcited carriers in GaAs with the surface states [59, 60]. These results are consistent with our previous reports on GaAs/AlGaAs nanowires [20] and provide clues to obtaining high-quality and optically active nanowires. Second, when we compared the PL spectra of GaAs nanowires with that of GaAs/AlGaAs core-shell nanowires and with the S.I. GaAs substrate, we attributed the emissions at 1.45 eV in both nanowires to the band-edge emission of GaAs and we found that the emissions indicated a blue shift of 30 meV from the emission of the S.I. GaAs substrate. In circular nanowires surrounded with infinitely high potential barriers, the ground-state quantized energy associated with lateral confinement is given by $(2\hbar^2\lambda_{01}^2)/(md^2)$, where m is the effective mass and λ_{01} is the first zero of the zeroth-order Bessel function. For a GaAs core of 80 nm, the expected blue shift is only 2.5 meV, which is much smaller than the observed 30 meV. The possible origin of the shift may be strain [61] or other mechanisms. A more careful study is required to clarify the origin of the blue shift of PL peaks in nanowires. Third, a broad feature on the high-energy side of GaAs was observed in core-shell nanowires when we compared the PL spectrum of the two types of nanowires. We think this is an emission from the AlGaAs shell and its spectral broadening indicates a broad distribution in Al composition. Estimating the aluminum content from the high-energy shoulder of the spectrum reveals that it is distributed approximately from 4% to 16%, while the PL and X-ray diffraction measurements of AlGaAs grown on planar (111)B indicate the Al content to be 12%. The origin of the tendency for slightly less Al to be incorporated into nanowires is probably due to the difference in the migration

length between Ga and Al during SA-MOVPE. Furthermore, as we previously reported [37], since the growth rate of GaAs depends on the nanowire diameter, there is a probability that the growth and Al incorporation rates in AlGaAs will change as the diameter increases due to lateral growth. This could give rise to nonuniform aluminum content in nanowires. In addition, the compositions of aluminum in AlGaAs between the sidewalls and that on top surfaces are possibly different.

4.2. InP/InAs/InP Core-Multishell Structure and InAs Quantum Tube [31]. We investigated the fabrication of an innovative core-multishell nanowire that was designed to embed a single strained radial quantum well (QW) in a higher band gap nanowire. The InP/InAs material system with a lattice mismatch of 3.2% was chosen for the present work. InP/InAs-strained QWs have tremendous potential for long wavelength optoelectronic applications because of their flexibility in enabling the electronic band structure to be tailored by using the combined effects of quantum confinement and strain. There is a schematic of the proposed core-multishell nanowire in Figure 20(a). The layer structure consists of an inner InP core and InAs and InP inner and outer shells, in which the InP core and the outer InP shell serve as the barrier layers while the InAs shell is the strained QW layer. Since the active layer, which is the InAs-strained QW, is in the form of a hollow cylindrical tube, this nanostructure can be deemed to be a quantum nanotube and is likely to exhibit exceptional properties as it is a two-dimensionally (2D) confined system with a three-dimensional (3D) cylindrical symmetry within a one-dimensional (1D) nanowire structure. It is extremely challenging to fabricate a lattice mismatched nanowire with a core-multishell heterostructure because of several complex requirements. Despite the lattice mismatch, InAs 2D layer-by-layer growth should essentially occur on the InP nanowire core and also be preferentially along the lateral direction. Further, the fact that the inner core and the outermost shell are composed of the same material, InP, intrinsically necessitates InP to be grown axially for the inner core and laterally for the outer shell. The core-multishell nanowires reported earlier based on Si/Ge [62] and GaN/InGaN [63, 64] have been synthesized by a different approach, where the nanowire core was grown with the catalyst-assisted vapor-liquid-solid (VLS) method and the shells were formed on the nanowire surface by vapor phase deposition. Unlike such a synthesis, our work involves growing both the core and the shells with a pure epitaxial method without the assistance of any catalysts. Critical factors are to accurately control the fabrication process, have precise knowledge about the growth mechanism, and control the direction of growth.

The source materials were TMI, TBP, and 5% AsH_3 in hydrogen. The core as well as the shells were grown sequentially as a single-continuous process. The growth conditions for an InP core and InAs shell have been described in detail elsewhere [65, 66]. Subsequent to the growth of InAs, the conditions were changed yet again to grow the InP outer shell. While the growth of the inner InP core occurred along the top (111) direction, the outer InP layer should preferentially grow along the (110) direction. It is essential to control the direction of axial/radial growth of InP to achieve this complicated task. Phosphorus (P) coverage governed by the growth temperature and TBP partial pressure was found to strongly influence the direction of InP growth [65]. While relatively lower P coverage induced axial growth, higher P coverage influenced lateral growth. Thus, as P coverage was altered, competing growth of the top (111)A surface and the (110) sidewall plane occurred and it was possible to exactly define the direction of growth by precisely choosing the conditions. A growth temperature of 600°C and a high TBP partial pressure of 5.5×10^{-3} atm were the optimum conditions that favored the lateral growth of InP over InAs sidewall facets. The single-step growth process under these conditions ultimately resulted in the successful fabrication of nanowire arrays with an InP/InAs/InP core-multishell heterostructure.

Our SEM studies clearly indicated that the grown structures were well defined (Figure 20(b)). The length of a typical core-multishell nanowire was about 2.5 μm, and its diameter was about 140 nm. The grown nanowires were subjected to anisotropic dry etching followed by stain etching to analyze their cross-sectional features. The diameter of the inner InP core and the thickness of the outer InP shell covering it were 70 and 30 nm, respectively. The InAs QW layer exhibited a well-defined hexagonal cross section, and the well width was found to be 5 nm (inset of Figure 20(b)). The most remarkable feature of this nanostructure is that the dimensions as well as the layer structure thickness could be accurately defined by growth conditions. Thus, precise control over the fabrication process gave us the freedom to engineer the physical properties determined by the shape, size, and QW width of the nanostructure. Further, selective-area growth enabled the fabrication of these nanowires to be guided in a highly periodic manner. The successful fabrication of this core-multishell nanowire is extremely significant as all three layers are single crystalline and these were epitaxially grown without the presence of any catalysts. Core-multishell nanowires with different InAs QW widths were grown by varying the InAs growth time to enable further characterization.

Four K μ-PL measurements were carried out on the core-multishell nanowires with an InAs well width of 1.5 nm using the 532-nm continuous-wave output of a diode pumped Nd: YVO_4 laser for excitation. The excitation beam was focused onto a 2 μm-diameter spot with a ×20 microscope objective on the sample, which had been placed in a cold finger cryostat. The PL collected through the same microscope objective was dispersed into a spectrometer with a liquid-nitrogen-cooled InGaAs photomultiplier tube. The PL spectra of core-multishell nanowires with different pattern periods are shown in Figures 21(a) and 21(b). Spectrum (a) shows PL from a nanowire array with a 3-μm period, whereas (b) is from an array with a 0.4-μm period. Since the 3-μm period is greater than the spot size, spectrum (a) can be concluded to be from a single core-multishell nanowire [67]. Spectrum (a) consisted of two distinct emission peaks. The PL peak observed at an energy of 0.861 eV is due to an InAs QW formed on the (110) sidewalls of InP nanowires, while the peak at 1.401 eV corresponds to the InP barrier, as will be

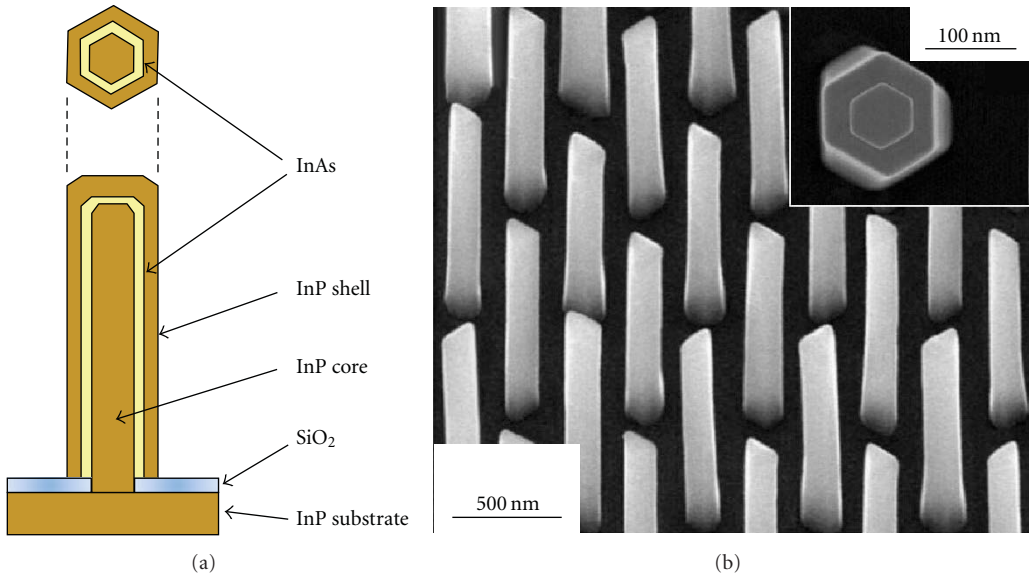


Figure 20: Cross-sectional structures and SEM images of nanowires. (a) Schematic of cross-sections of InP/InAs/InP core-multishell nanowire. (b) SEM image of periodically aligned InP/InAs/InP core-multishell nanowire array. Inset is top view of high-resolution SEM image of core-multishell nanowire observed after anisotropic dry etching and stain etching [31].

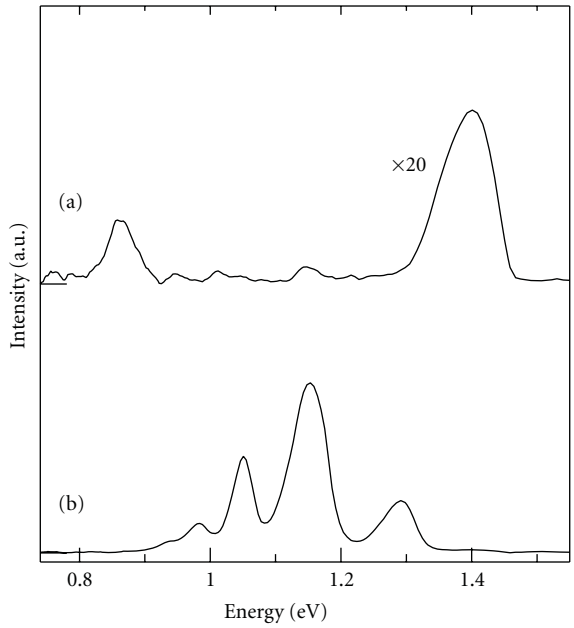


Figure 21: 4-K PL spectra of nanowire arrays with (a) 3- and (b) 0.4-μm periods [31].

discussed later in detail. Further, the InAs layer on top of the InP core is rather thick and does not have any influence on the observed PL spectra. Spectrum (b), taken from multiple core-multishell nanowires (30 nanowires, considering the size of the spot), on the other hand, exhibits multiple peaks at around 0.86–1.45 eV, which are also due to the emissions from InAs radial QWs.

To confirm these peak assignments, the ground-state transition energy in strained InAs QWs on InP (110) was calculated using a simple square well potential. The parameters for calculation were determined as follows. Initially, offsets for conduction and heavy hole bands were calculated based on model solid theory [68] taking into account strain in InAs on InP (110). While the unstrained isotropic effective mass was used for electrons, the heavy hole effective mass (m_{hh}) was determined based on

$$m_{\mathrm{hh}} = \frac{m_0}{\left(\gamma_1 - \left(\gamma_2^2 + 3\gamma_3^2\right)^{1/2}\right)}, \tag{3}$$

where m_0 is the free electron mass and γ_1, γ_2, and γ_3 are the Luttinger parameters. The heavy hole effective mass was obtained using a 4×4 Luttinger-Kohn Hamiltonian with the quantization axis along the (110) direction [69]. The values of the deformation potential and Luttinger parameters were taken from Chuang [70] and Sugawara et al. [71]. The present calculation considerably simplifies the treatment of nonparabolicity in the conduction band and complex valence band structure of strained (110)-oriented QWs. A more accurate account on the electronic structure in a strained core-multishell nanowire will be reported elsewhere, but the accuracy of the present theoretical treatment is expected to be within the ambiguity of the parameters, the difference in the crystallographic structure [66] of InP and InAs, and effective mass approximation. The results of the calculation have been plotted as a function of the InAs well width (Figure 22). According to these results, the PL peak at 0.861 eV observed for a single core-multishell nanowire corresponds to a well width of 2.08 nm, which reasonably agrees with the measured thickness of the InAs layer. Further, this peak is relatively broader with a full width at half maximum (FWHM) of 48 meV, which can be mainly

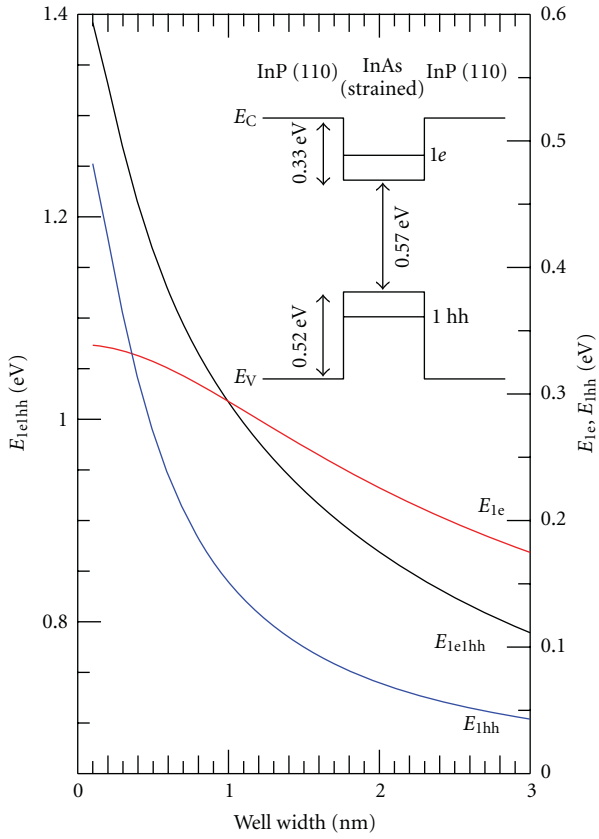


FIGURE 22: Plot of ground-state transition energy as function of well width for InP/InAs/InP strained QW on InP (110) [31].

attributed to the fluctuations in well width, although it may be in part due to inhomogeneous strain in the InAs layer. Also note that the PL peak of InP has slightly red shifted compared to the bare InP nanowires [65]. Our preliminary calculations suggest that this shift is not due to the tensile strain in InP nanowires but it bears further investigation. In spectrum (b) the peaks at 0.984, 1.05, 1.154, and 1.292 eV correspond to InAs QW widths of 1.16, 0.856, 0.532, and 0.262 nm. A minimum width for InAs in InP is accomplished by substituting one layer of *P* with As, and this corresponds to a half monolayer thickness for (110). Thus, the thinnest InAs QW in the elastic continuum model is expected to be 0.219 nm, and the well width should be its integer multiples. Considering the accuracy of the present model, these results reiterate the formation of InAs QWs on the side walls of InP nanowires and the multiple peaks indicate that there might be monolayer QW thickness variations in individual nanowires in an array. The peak broadening, in this case also, can be partly attributed to inhomogeneous strain in the InAs layer in the nanowire array. Further, the InAs layer thickness is less in nanowires with a 0.4-μm period than that in nanowires with a 3-μm period. This difference in the InAs layer thickness may be attributed to the gas-phase diffusion of In, where the lateral growth rate of InAs on the sidewalls is much higher for smaller densities of nanowires, that is for nanowire arrays with larger periods. However, as this kind of diffusion model cannot fully account for the vertical growth rate of nanowires, it thus requires more detailed investigations.

The band offset of the lowest energy levels for the conduction band and the valence band of the InP/InAs/InP core-multishell nanowire depicted in the inset of Figure 22 indicates a heterostructure with Type-I alignment, that is, the bottom (top) of the InAs conduction (valence) band is at a lower (higher) energy level of the conduction (valence) band bottom (top) of InP. Recent investigations, using time-resolved and spectrally resolved PL and PL excitation measurements, of the InP/InAs/InP core-multishell nanowires revealed the possibility of a Type-II heterostructure, that is, band alignment with the conduction (valence) band of InAs lying 0.16 (0.32) eV above the conduction (valence) band of InP [72].

4.3. GaAs/GaAsP Core-Shell Structure and Laser Emission [32]. Semiconductor subwavelength nanowires have been demonstrated in recent years to have laser emissions [73–79]. Representative semiconductor materials for fabricating nanowire lasers involve ZnO, GaN, and CdS. Such nanowire lasers are currently among the smallest known lasing devices, with lengths between 1 and several tens of micrometers and diameters that can be significantly smaller than the emission wavelength in a vacuum. Because of the large dielectric contrast between the nanowire and the ambient in this size range, strong lateral optical confinement is created. The end facets of a single-crystalline nanowire form a natural mirror surface that creates an axial resonator. That is, one-dimensional semiconductor nanowires act not only as a gain medium but also as a waveguide and a Fabry-Perot resonator, which provide coherent feedback. The light-emitting capability of the nanowires, combined with their other unique features that arise due to their one dimensionality, makes them particularly interesting to consider as candidates for components in future nanoscale photonic systems. However, most advances in nanowire lasers have successfully been achieved through wide-bandgap semiconductor materials, which provide ultraviolet-to-blue laser emissions. To date, limited investigations into nanowire lasers in the near-infrared (NIR) spectral range have been reported [80], while there are vast areas of applications in NIR lasers particularly for optical fiber communications. For instance, lasers operating at 850 nm can be used in in-house and in-enterprise local area networks with extremely high transmission bit rates. In this case, GaAs-based materials are primarily important while the main difficulty in attaining nanowire lasers in these material systems is that the high density of surface states will lead to strong decay of emission intensity in GaAs nanowires.

We here describe GaAs/GaAsP coaxial core-shell nanowires fabricated by SA-MOVPE and report our observations that a single wire has optically pumped NIR lasing emissions. GaAs and GaAsP were grown in succession for core-shell heterostructures. The partial pressures for GaAs were 1.0×10^{-6} atm for TMG and 2.5×10^{-4} atm for AsH_3. The growth temperature and growth time were set to 750°C and 60 min. The partial pressures for growing the GaAsP shell

corresponded to 1.0×10^{-6}, 2×10^{-4}, and 2.5×10^{-4} atm for TMG, TBP, and AsH_3. The growth temperature and growth time were 650°C and 5 min. Perfect selective epitaxy of both GaAs and GaAsP was achieved under these conditions.

As-grown nanowires were mechanically cut down and dispersed onto 2-μm thick SiO_2-covered Si substrates to optically characterize single nanowires. PL measurements were carried out using a regeneratively amplified Ti:sapphire pulsed laser (140-fs pulse duration and 78-MHz repetition rate) with a wavelength of 753 nm. The excitation beam was focused with a ×50 microscope objective (NA = 0.42) onto a spot of about 2 μm in diameter on a sample in a cryostat. The emissions through the same microscope objective were collected into a liquid-nitrogen-cooled CCD for spectral analysis or a CCD camera for imaging.

First, the overall morphology of as-grown nanowires was examined by SEM. A schematic cross-section of a GaAs/GaAsP nanowire and typical SEM images of GaAs nanowires and GaAs/GaAsP core-shell nanowires are shown in Figures 23(a) to 23(c). A uniform array of vertical standing nanowires was prepared with a smooth top surface and sidewall. Close-up SEM images of nanowires indicate they have a clear hexagonal shape. As the wires grew perpendicularly on GaAs (111)B substrates, the growth direction thus coincided with the (111)B direction. Since this SA-MOVPE method fully utilized the nature of epitaxial growth and used no gold as a seed for the nanowires, they were synthesized with superior crystalline quality at atomic precision. The nanowire diameters, d, in this study were controlled, so they ranged between 200 and 500 nm and their lengths ranged between 2 and 6 μm. The nanowire sizes depended on the prepared mask openings on the substrate and growth conditions [37, 81]. The relatively larger nanowire diameters in this experiment were necessary to enhance reflectivity at both ends of the nanowire surface and bring sufficient optical confinement for lasing, especially at NIR wavelengths. SEM images (b) and (c) in Figure 23 show that the length of the core-shell wire is almost equal to that of GaAs, but the diameter of the core-shell wire is approximately 100 nm greater than that of the GaAs wire, suggesting a 50-nm thick GaAsP shell around the GaAs core wire.

TEM and EDX spectroscopy (EDX) were then applied to examine the structure of nanowires and their atomic composition. A bright-field TEM image and EDX line scans obtained from the axial plane of a single nanowire exposed by focused ion beam (FIB) etching are shown in Figures 24(a) to 24(c). Even though the heterointerface of GaAs and GaAsP cannot clearly be distinguished in the bright-field and high-resolution TEM images, the EDX line scan clearly shows the formation of core-shell structures. The green, blue, and red lines in Figures 24(b) and 24(c) correspond to the EDX counts of elemental Ga, As, and P. The length of this nanowire was 2.8 μm, and its diameter was 390 nm. In Figure 24(b), the results are presented for an EDX line scan along the axis of the nanowire (along the solid white arrow in Figure 24(a)). Here the right end of the nanowire corresponds to its top end during growth. Another line scan performed across the diameter of the nanowire is shown in Figure 24(c). The scan position is labeled with a blue solid arrow in Figure 24(a). The axial EDX scan indicates that the nanowire core is entirely composed of GaAs along the center axis, and the P content on its top surface is negligible. However, the radial line scan clearly designates the presence of a P element around the GaAs core. These results prove that the nanowire structure should be a GaAs core surrounded by a GaAsP shell. The P concentration in the GaAsP shell is around 10% in atomic content, that is $GaAs_{0.8}P_{0.2}$, and the thickness of the outer GaAsP shell is estimated to be 50 nm, which is consistent with that SEM observations (Figures 23(b) and 23(c)) before and after the growth of GaAsP.

Fabry-Perot microcavity modes were observed in single GaAs nanowires [82] in our previous study. The PL spectra results suggested that a Fabry-Perot microcavity was formed along the length of the nanowire, and the (111) facets of both ends acted as reflecting mirrors. However, due to the nonradiative recombination of photoexcited carriers on the air-exposed GaAs sidewall surface where there is high density of surface states, the emission intensity of bare GaAs wires is too weak to obtain lasing. Core-shell nanowires are expected to be used instead of bare GaAs wires to further optimize this cavity quality. The function of the shell layer is to passivate the surface states of the GaAs core nanowires, resulting in high-quality and optically active nanowires. The PL spectra of the GaAs/GaAsP core-shell nanowires in this study displayed apparently strong emission intensity, which was stronger than that of bare GaAs nanowires by a factor of over two orders of magnitude. A shell, 50 nm in thickness, should have been sufficient in this study to passivate surface states since it has been reported that a shell of around 10 nm in thickness suppressed the reduction of PL efficiency [59, 60].

An isolated single GaAs/GaAsP core-shell nanowire was then excited with a pulsed laser, and PL emissions were subsequently collected at 4.2 K, as can be seen in Figures 25(a), 25(b), and 25(c). This wire is 330 nm in diameter and 5.5 μm in length. The PL spectra at low excitation power densities display a broad emission band at about 820 nm. However, above a certain threshold (8.4 kW/cm^2 in this nanowire), a sharp and narrow peak centered at about 816 nm appears and the peak intensity increases rapidly with excitation energy. This emission peak is exactly consistent with the GaAs band gap energy (1.52 eV at 4.2 K), indicating the onset of stimulated emissions from the GaAs core of the nanowire. From Figure 26(a), stimulated emission or lasing can be evidenced by the appearance of simultaneous line narrowing and a superlinear increase in intensity at pump densities above the threshold. However, as the pump power density is further increased above 15.0 kW/cm^2, the emission intensity saturates, indicating that gain is pinned. We speculated on what contributed to the quick saturation of laser emissions with the present experimental configuration. That is, we used a tight focus for the incident laser on the nanowire, where the diameter of the laser beam was around 2 μm, which is much less than the wire's length. These led to a smaller pumping area in the nanowire; thus, gain was only obtained in the vicinity of the excitation region. As a result, gain quickly saturated. Excitation-induced local heating may also be a reason for the quick saturation in gain. Moreover, the line

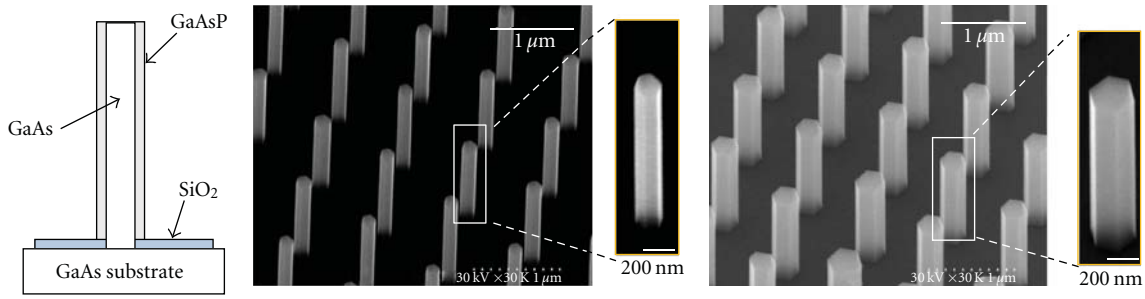


FIGURE 23: Schematic of structure and SEM images of nanowires. (a) Schematic of cross-sectional structure of core-shell nanowire. (b) and (c) SEM images of as grown GaAs and GaAs/GaAsP nanowires for comparison [32].

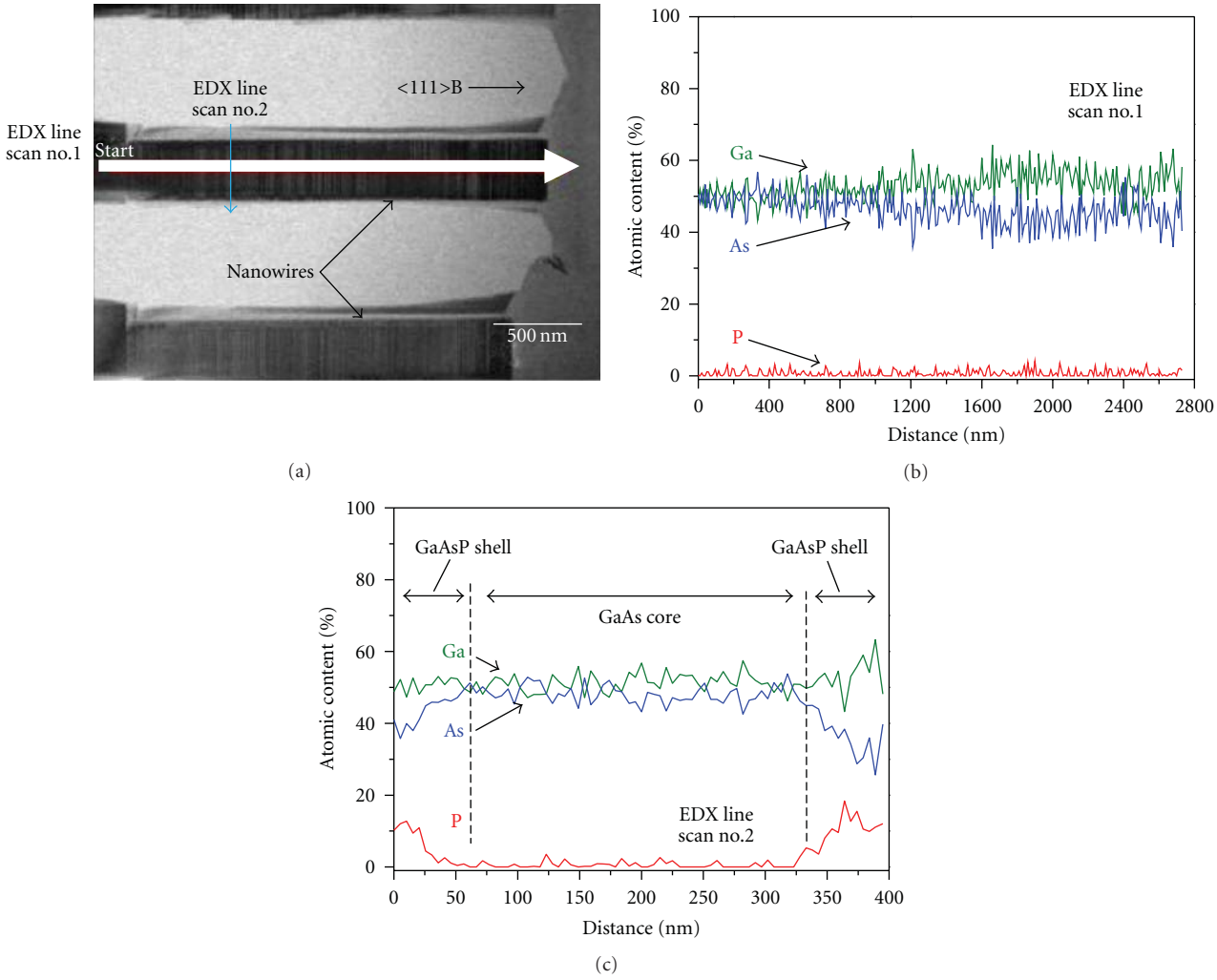


FIGURE 24: TEM/EDX analysis of GaAs/GaAsP nanowire. (a) Bright-field TEM image and axial/radial EDX line scans on nanowire. Axial plane of wire was exposed with FIB etching. (b) Variations in Ga (green), As (blue), and *P* (red) content for axial line scan no. 1 in (a). (c) Variations in Ga, As, and P content for radial scan no. 2 in (a). Radial EDX scan indicates that GaAs core is surrounded by approximately 50-nm thick GaAsP shell [32].

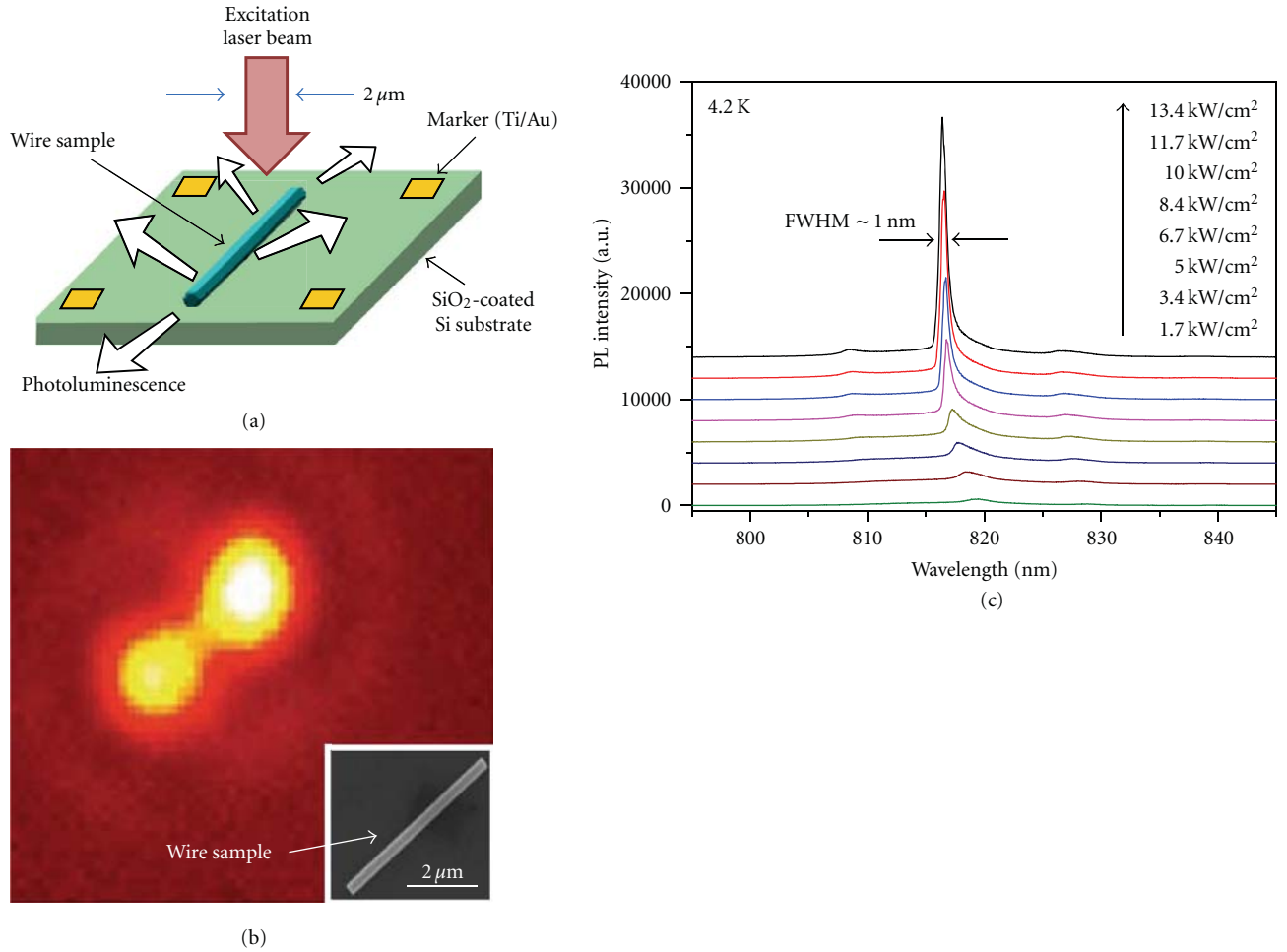


Figure 25: Images of optically pumped single GaAs/GaAsP core-shell nanowire lasers and PL spectra. (a) Schematic of nanowire sample excited by laser beam. (b) CCD camera image of luminescence from nanowire. Inset at bottom right is SEM image of 5.5-μm-long nanowire. (c) PL spectra from single GaAs/GaAsP core-shell nanowire with length of 5.5 μm, as function of increasing excitation power density at 4.2 K [32].

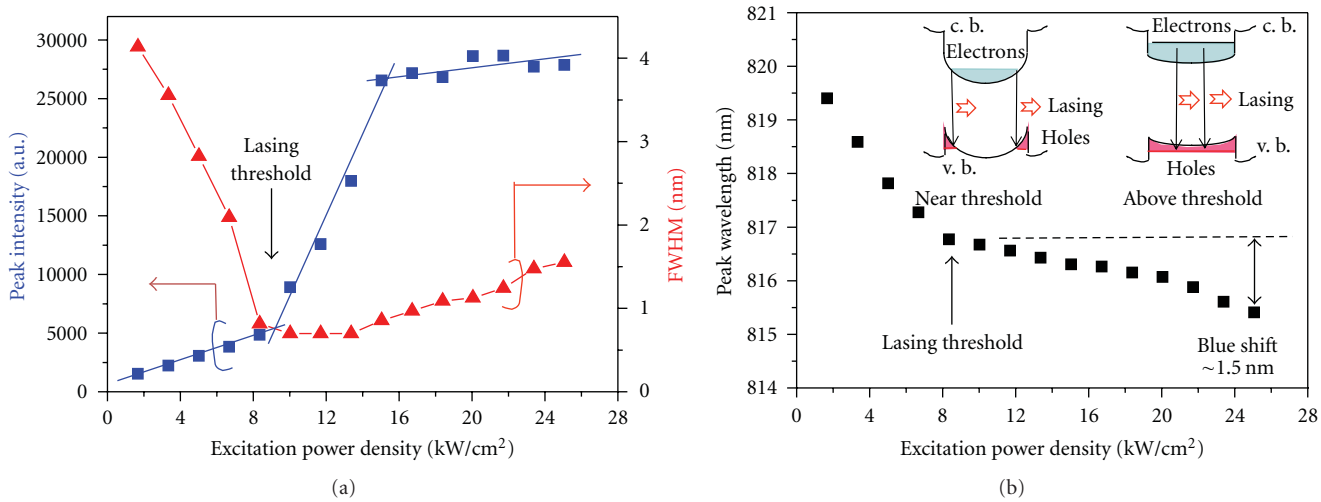


Figure 26: PL peak intensity/wavelength as function of excitation power density. (a) Plots of emission peak intensity (marks with filled squares) at center wavelength of 816 nm and full width at half maximum (FWHM) (marks with filled triangles) of PL spectra. (b) Plots of lasing peak wavelength versus excitation power density. Inset indicates how band bending of conduction band (c. b.) bottom and valence band (v. b.) top change as densities of accumulated photoexcited electrons and holes increase [32].

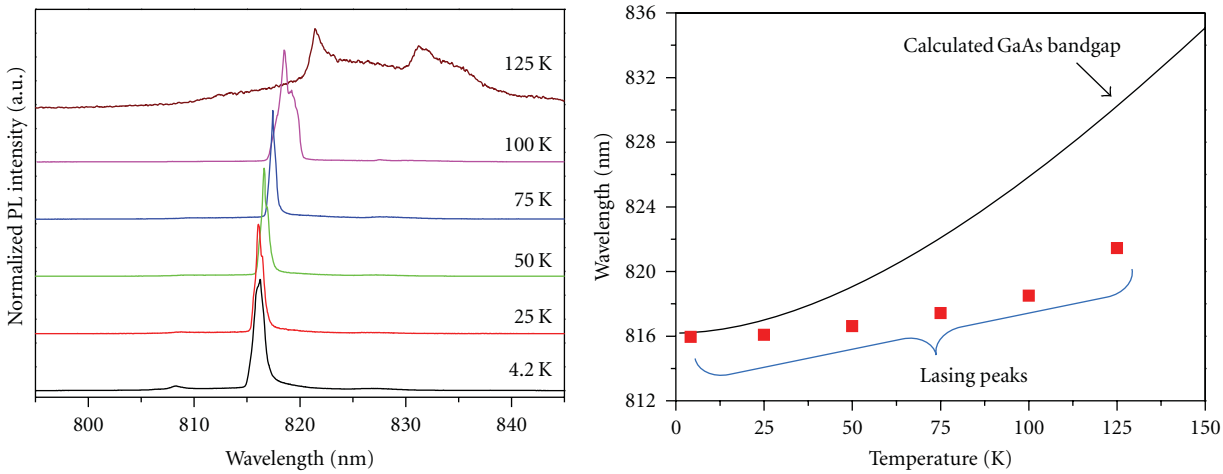


FIGURE 27: Normalized temperature-dependent spectral features recorded from single GaAs/GaAsP nanowire for lasing. (a) PL spectra for lasing recorded at 4.2, 25, 50, 75, 100, and 125 K. (b) Plots of temperature-dependent lasing wavelengths (marks with filled squares). Dependence of temperature on GaAs bandgap is also given in curve for comparison [32].

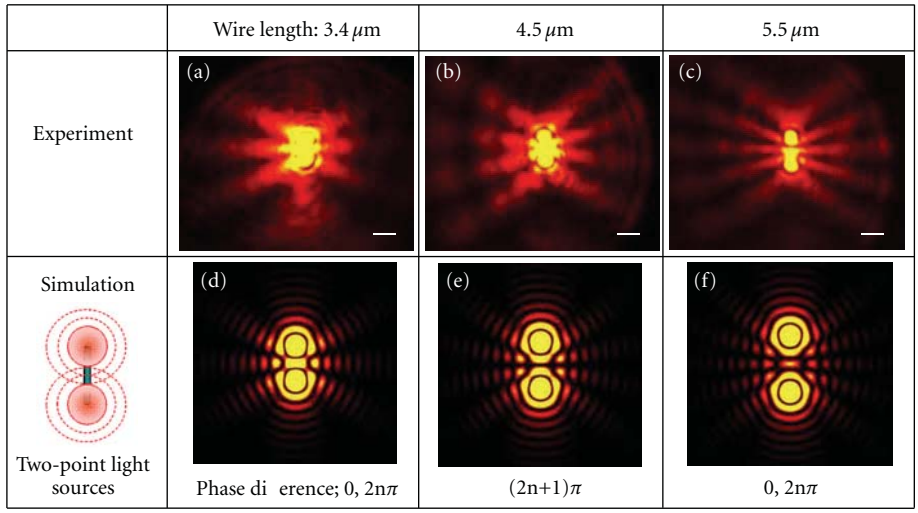
width for conventional semiconductor lasers varies inversely with pump power, due to an increasing degree of population inversion. However, microlasers pumped with short intense pulses can exhibit additional nonequilibrium effects that act to broaden the lasing peak [83]. Such an effect can also be seen in Figure 26(a). The laser peak is broadened from 0.7 to 1.5 nm over the power range of 13.4 to 25.1 kW/cm^2. It is likely that there is increased spontaneous emission noise at higher pump intensities due to amplified spontaneous emissions that cause phase fluctuations that couple to the real and imaginary parts of the material susceptibility. These optical density fluctuations would couple to the cavity modes and act to broaden the lines, especially in regions with the highest dispersion and absorption.

As usual, nanowire lasing red shifts with increasing excitation power, due to the heating effect or the bandgap renormalization induced by the electron-hole plasma state [84]. In contrast, blue shift in the lasing peak of this wire can be observed due to an increase in the pump power as shown in Figure 26(b). The reason for this blue shift is unclear, but one possibility may be due to band bending [85, 86]. According to the model, photoexcited charge carriers are generated and reach a dynamic equilibrium, where electrons get confined near the nanowire surface but holes accumulate near the nanowire center. Thus, an electron near the surface recombines with a hole near the center, leading to low transition energy, while at the high excitation intensity, the band bending effect weakens due to the formation of more charge carriers, bringing about high emission energy and transition probability. The nanowires used in the model are nondoped GaAs [85] and p-type InP [86]. However, the GaAs nanowires in our experiment were assumed to be n-type (carrier concentration of around 4×10^{17} cm^{-3}, obtained by electron Hall measurements of planar GaAs epitaxial layers grown on S.I. GaAs (001) substrates at the same temperature as the nanowires). Thus, the band bending and the accumulation of photoexcited charge carriers for the present GaAs/GaAsP nanowires could be reversed compared to van Weert et al.'s model [86], as depicted in the inset of Figure 26(b), and the PL blue shift can be explained in the same fashion.

Furthermore, the normalized temperature-dependent PL spectra of the same nanowire were recorded from 4.2 to 150 K, as shown in Figure 27(a). The excitation power density was set to 21.0 kW/cm^2 for all the spectra. The spectral features associated with lasing were expected to exhibit pronounced red shift with temperature. However, from Figure 27(b), compared to the temperature-dependent red shift in the GaAs bandgap energy, the red shift in the lasing wavelength is weak ($\Delta\lambda$ is 2.5 nm from 4.2 to 100 K). These results agree with the previous observation of the temperature-dependent cavity mode in single GaAs nanowires ($\Delta\lambda$ was 2–2.6 nm from 4.2 to 100 K) [82]. Considering the expression of $m = 2nL/\lambda$, where m is the longitudinal mode order, the peak position is strictly determined by refractive index n, for a certain nanowire with a length of L. With temperatures ranging from 4.2 to 100 K, the temperature-dependent variations in the refractive index are weaker, leading to less change in the lasing peak with temperature.

The lasing characteristics of the GaAs core indicate that these heterostructure nanowires are very efficient gain media, which can be attributed to their ideal photon-confinement structures. Since the regular dimensions of the wires make them excellent waveguides, emission light can be accumulated and amplified through them being reflected from both ends of the wires to finally produce stimulated emissions or lasing under sufficiently high excitation. As a comparison, it must be emphasized that no lasing has been observed thus far for pure GaAs nanowires. The lasing in the present

Table 1: Far-field optical images of lasing emissions from single GaAs/GaAsP core-shell nanowires. (a)–(c) Observed lasing emissions from different nanowires with lengths of 3.4, 4.5, and 5.5 μm. Incident laser spot is focused perpendicularly at center of nanowires. Scale bars: 5 μm. (d)–(f) Simulated interference patterns for corresponding nanowires in panels (a)–(c), assuming spherical nondirectional emissions from wire end facets [32].



core-shell structures is mainly attributed to the reduction in nonradiative surface recombination as previously discussed. The influence of photon confinement due to index contrast between the core and shell is not important in the present structure because of the small refractive-index contrast (the refractive index at a λ of 816 nm is 3.66 and 3.56 for GaAs and GaAsP, resp.) and thin shell thickness (about 50 nm).

The top half of Table 1 shows lasing emission images from several core-shell nanowires of different lengths. The images were recorded with a laser filter when the excitation laser was focused at the center of the nanowires. All wires exhibit very bright luminescence spots that can be observed at both ends. This is a typical feature of an optical waveguide, and it suggests that the wires are able to absorb excitation light and propagate PL emissions toward the ends. Almost all the core-shell nanowires exhibited this kind of waveguide behavior. Since wave-guided light is generated from PL within the nanowires, these wires can be classified as active waveguides instead of passive ones where light must be coupled-in from external sources. Interestingly, intensity modulations around the wires can be observed, suggesting that diffraction and interference occur, which originate from spherical emissions from both wire end facets with a difference in fixed phase. These interference patterns are expected to depend on the wire length. The longer nanowires obviously exhibit more complex interference patterns, compared to the shorter ones. We simulated diffraction and interference patterns to enable more quantitative understanding following van Vugt et al.'s approach [87] (assuming spherical nondirectional emissions in nanowire end facets), which are presented in the bottom half of Table 1. Here, the NA of the microscope objective and the difference in the phase at two edges have been taken into account. We can see that the interference patterns around the nanowires are nicely reproduced for all three nanowires.

The next issue with GaAs/GaAsP core-shell nanowires is to develop an electrode fabrication process to enable current injection to the nanowires, where light from them should be extracted without being blocked or absorbed by electrode metal. Heat dissipation from nanowires during current injection is another issue that needs to be solved to enable stable operation of devices at room temperature (RT). The active layer in commercially available semiconductor lasers is buried in a semiconductor material with a greater energy bandgap than the active layer. Therefore, buried heterostructures should be considered to dissipate heat from nanowire LEDs to allow their practical use.

5. Outlook for the Future

The mitigation of mechanical strain and curbs to the development of crystal dislocations at the junction interface of lattice mismatching systems are advantages of using nanowires. Reducing the number of defects should effectively enable semiconductor nanowires to be fabricated on a Si platform, which is promising for integrating them with ICs or using them in large-scale production to achieve low cost. Important factors to consider in practical use in lighting and display systems for optical information processing where LEDs are used as optical sources are control over their emission wavelength and optical power and the reliability of devices. Lattice-mismatched heterostructure epitaxial layers, for example GaInAs/GaAs, GaInP/GaAs, and GaInN/GaN grown on a III-V semiconductor substrate or on a sapphire substrate, have been used to control the emission wavelength of LEDs. Material costs for the substrates would be reduced if Si was employed instead of expensive substrates [88–92]. However, as previously mentioned, the heterostructures grown on Si are subject to mechanical strain and crystal

dislocations at the substrate interface due to lattice mismatching. The dislocations developed in the active region of devices are detrimental to reliability. Using nanowires would offer a solution to this problem.

We found that InAs and GaAs nanowires were grown perpendicular to a Si(111) substrate surface with reduced misfit dislocations at the interface of Si and the nanowire [93, 94], which demonstrated tremendous potential for developing III-V nanowire devices on Si [95, 96]. A serious issue for III-V nanowires on Si is how the series resistance attributed to the energy band offset between Si and III-V can be minimized when electric current flows across the junction interface. Using an Esaki tunnel diode structure is a solution to the problem [92]. Compatibility with the planar structure of conventional CMOS-FETs is another issue when III-V nanowires are used as channel replacements in FETs. Further ideas for structures are expected.

6. Summary

III-V semiconductor nanowires with heterojunctions along their axial and radial directions grown by selective-area metal organic vapor phase epitaxy were reviewed. The photoluminescence of InGaAs/GaAs, GaAs/AlGaAs, or GaAs/GaAsP was investigated in axial heterojunction nanowires to estimate the thickness of an InGaAs or GaAs single quantum well buried in them. Radial heterostructure (core-shell type heterostructure) nanowires, that is, GaAs/AlGaAs, InP/InAs/InP, or GaAs/GaAsP, were fabricated to evaluate what effect surface passivation had on the core nanowire, which indicated enhanced intensity in photoluminescence. Further, photoexcited laser emissions from a single GaAs/GaAsP core-shell nanowire were evaluated. Transmission electron microscopy combined with energy dispersive X-ray spectroscopy was used to analyze the crystal structure and atomic composition of the nanowires, which indicated that the axial or the radial heterostructure was successfully fabricated. The results revealed the basic optical properties of the nanowires and showed their promise in applications to optoelectronics devices.

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Research Article

Synthesis of ZnO Nanoparticles to Fabricate a Mask-Free Thin-Film Transistor by Inkjet Printing

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We report a low-cost, mask-free, reduced material wastage, deposited technology using transparent, directly printable, air-stable semiconductor slurries and dielectric solutions. We have demonstrate an emerging process for fabricating printable transistors with ZnO nanoparticles as the active channel and poly(4-vinylphenol) (PVP) matrix as the gate dielectric, respectively, and the inkjet-printed ZnO TFTs have shown to exhibit the carrier mobility of 0.69 cm^2/Vs and the threshold voltage of 25.5 V. We suggest that the printable materials and the printing technology enable the use of all-printed low-cost flexible displays and other transparent electronic applications.

1. Introduction

Solution-processable organic semiconductors such as pentacene, poly(3-hexylthiophene) (P3HT), and α,ω-dihexyl-quaterthiophene (DH4T) have been also investigated, but they exhibits low mobility (<0.1 cm^2/Vs) and poor stability against humidity [1–3] in common processes. For these reasons, solution-processed inorganic materials that are stable in air and suitable for solution processes have attracted recent research interest.

Metal oxides are well-known high carrier mobility, and transparent conducting materials as SnO_2, In_2O_3, ZnO [4], and other mixed oxide of Ga, In or Sn, and Zn as amorphous semiconductors, such as IGO, ZTO, IZO, and IGZO [5–9]. They usually reveal n-type property by virtue of oxygen vacancies or incorporation and also can achieve high mobility of 1–100 cm^2/Vs in amorphous state [5, 10], much higher than a-Si ($\leqq$1 cm^2/Vs). These materials can be deposited by vacuum or soluble thin-film techniques.

Until now, ZnO is still considered an ideal candidate for realizing new transparent and flexible electronics for flat panel display, such as transparent thin-film transistors (TTFTs). Compared with organic TFTs, these oxide TTFTs clearly have more potential for OLED since the mobility is higher and the soluble fabrication is less equivalent to a-Si and simple than LTPS process, which results in higher drive currents, low cost, resolution raising, and uniform large-area fabrication [5]. Zinc oxide films have been studied and fabricated as the active channel of TTFTs using vacuum or soluble processing, such as sputtering, pulsed laser deposition (PLD), chemical vapor deposition (CVD), atomic layer deposition (ALD), spin coating, spray, chemical bath deposition (CBD), and several printing techniques [11–17]. An important advantage of ZnO is one oxide that can be crystallized at relatively low temperature, which indicates that the solution processes are introduced into the high-quality film production in place of lithographically defined deposition on plastic substrates for flexible displays. However, TFT devices based on polycrystalline ZnO as active layer by various processes have been reported with mobilities of about 0.2–3 cm^2/Vs [18–21].

Recently, Inkjet printing (IJP) technology has been used as a low-cost research appliance in laboratory environment, depositing various experimental soluble materials of printing electronics as semiconductors, dielectrics, or conducting constructions of devices, such as the of OTFT, LED, solar cell, metalize, memory, and sensors [22]. IJP is part of non-contact, wide material applications and mask-free deposited technology. The advantage of directly printed property by IJP can achieve multilayer films with various functional inks in one device, simply process and rapidly revise print patterns via controlling digital design for patternable. Other

attractive advantages of inkjet-printed electronic include low cost, reducing material waste, and fabrications of large area for roll to roll.

The aim of this work is to prepare and disperse ZnO NPs solutions in high boiling point solvent by dispersants for the inkjet-printed active layer of TFTs. The printed inks were prepared using Poly(4-vinylphenol) (PVP) and zinc acetate dehydrate, which were used for the gate dielectric and semiconductor films of TFTs as precursors, respectively. The thin films of TFTs were deposited on ITO/glass substrates by inkjet printing at low temperature.

2. Experimental

2.1. Preparations of the Semiconductor and the Dielectric Materials. In this work, two types of device were fabricated and shown in Figure 1. The polymer dielectric layers were formed in a metal-insulator-metal (MIM) structure and top-contact TFT device. The cross-linked PVP (Mw~25,000, from Aldrich) and cross-linking reagent poly(melamine-co-formaldehyde) methylated (PMCF, Mw = 511, from Aldrich) dissolved uniformly in propylene glycol monomethyl ether acetate (PGMEA) were selected as the polymer matrix for the soluble dielectric.

According to a previous literature by Baoquan [23], ZnO nanoparticles (NPs) were synthesized by mixing a methanol solution (mol ratio, KOH : $Zn(Ac)_2$ = 1.6 : 1.0), comprising 29.58 mL of 0.31 M potassium hydroxide, 53.98 mL of 0.11 M Zinc acetate, and 320 uL of water, then heating and magnetic stirring at 60°C for 5 h to acquire an opaque suspension.

The transparent part of the staying solution was taken away after 30 min and 30 mL of methanol is readded into the solution then stirring for 5 min twice. The suspension after washings to 16.9 mL in the second washing then stands for 12 h. To well control the solid concentration of ZnO in the suspension from 3.92 to 3.0 wt%, we used 2.8 mL of the suspension to calculate the requirement of the solvent (methanol) and readded about 2.78 g.

Finally, the suspension was mixed with 16.2 mL of PGMEA (V : V, 50 : 50), then 14 mg of the polyester dispersant (4.0% wt. for ZnO-NPs) and 0.26 mL of *n*-butylamine (0.8% vol.) were dissolved in the mixture to obtain a clear solution, which was used to disperse the ZnO nanoparticles. We utilize another higher boiling point solvent as the second matrix in order both to prevent the jetting nozzle from clogging and to inhibit convective flow in evaporation process. The NPs solid content of ZnO inks is 3 and 7 wt%. To investigate the relation between characterizations of ZnO-NPs film and the composite of suspensions, we prepare ZnO-NPs suspensions and ZnO-NPs/Zn^{2+} mixture, which were possessed at the concentration of 3 wt%.

2.2. Fabrication of Devices. Bottom-gate, top-contact TFTs were fabricated on a glass substrates and shown in Figure 1. 100 nm thick indium tin oxide (ITO) layer was thermally deposited as a gate electrode on the glass substrate. After cleaning the glass with acetone in an ultrasonic bath, the polymer solution as gate dielectrics on ITO glass substrates

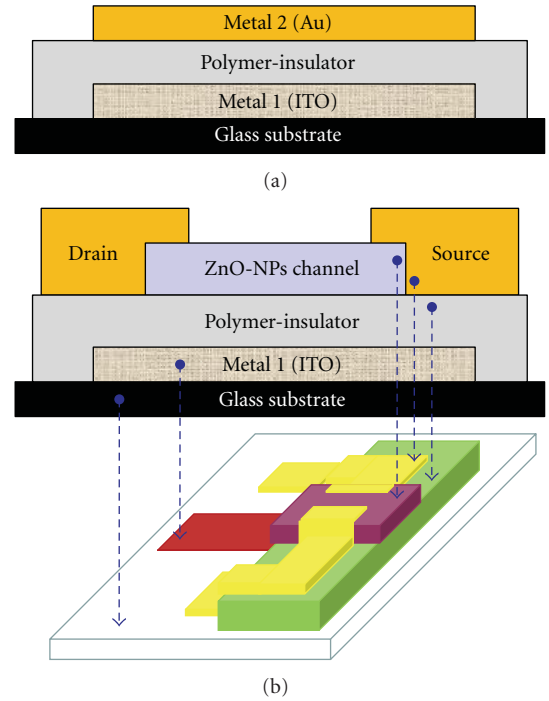


Figure 1: (a) Sandwich structure (MIM) of PVP gate dielectric insulator. (b) Configuration of "bottom-gate" and "top-contact" structure of a ZnO-NPs TFT with the polymer gate dielectric.

was prepared by inkjet printing with a thickness of 1-2 um, from the filtered (0.45 um PTFE filter) compound slurry and then baked at 190°C for 30 min. To obtain the leakage current density and dielectric constant, gold was thermally evaporated through the shadow mask and used as cover electrodes of the MIM structure.

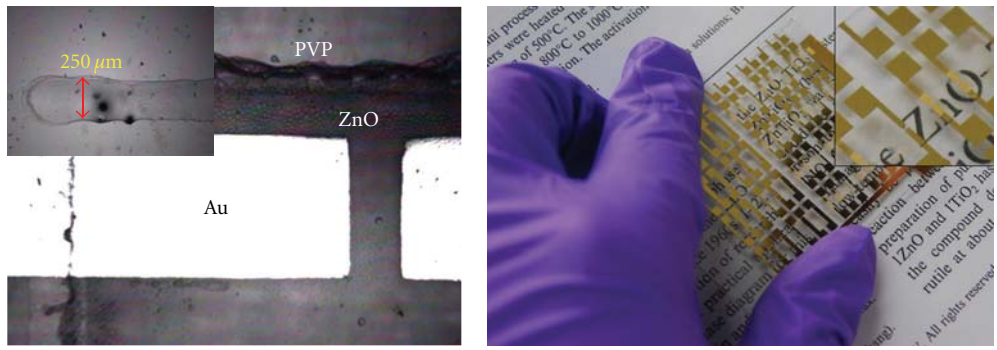
To comparison, as the electrodes for Hall measurement, Mo was deposited onto the spin-cast films of ZnO-NPs and ZnO-NPs/Zn^{2+} (S.C. = 3 wt%) on PVP layer and postannealed at 200°C for 1 h in air ambient or reducing atmosphere (RA).

To fabricate top-contact TFT structure, ZnO-NPs (3 and 7 wt %) filtered through a 0.45 um PTFE filter (Advantec MFS), is inkjet printed as an inorganic semiconductor layer on ITO/glass substrates with 1.2 um thick PVP, and its thickness was about 2 um. The resulting films are dried at 180°C for 2 hr to evaporate the solvent and annealed at 200°C for 1 h in reducing atmosphere for achieving thermal decomposition of organic residues, metal salts, and the carboxylate anion. Finally, the gold source/drain electrodes are thermally evaporated through the shadow mask on top of the ZnO-NPs layer on PVP/glass, which has the ratio of channel width (W) and length (L) are 2.

The printer constituted a drop-on-demand (DOD) piezoelectric inkjet nozzle (with a drop volume of 1–10 pL) produced by Dimatix (DMP-2800) is used in this work. The print head with 16 nozzles at 254 μm spacing in single row is mounted onto a computer-controlled three-axis gantry system exhibiting a movement accuracy of ±25 um. Stably droplet ejecting is accomplished by applying an 11.5 us long

(a) (b)

Figure 2: Transparency and sedimentation observation result of suspensions comprising the ZnO nanoparticles without dispersants and ZnO nanoparticles with dispersants after (a) 0 hr and (b) 2 weeks.



(a) (b)

Figure 3: Photos of inkjet-printed patterns obtained from ZnO NPs ink (3 wt%) as a function: (a) microscope images; (b) the devices on a glass substrate on one paper.

17 V pulse at a frequency of 1 kHz. The drop spacing was regulated at about 5 um during printing, and layer counts were 3 (and 20 V, 1 kHz, and 10 um of drop spacing).

2.3. Measurements. For spin coating and inkjet printing, a vacuum sintering furnace, filled air, or reducing atmosphere was used to anneal the ZnO NPs film. The thicknesses of the films were measured by an Alpha-Step Profilometer. A Hall measurement was performed to characterize the carrier concentration and Hall mobility of spin-coated ZnO-NPs films on PVP/glass substrates by annealing in various atmospheres. To obtain the optical absorption properties of inkjet-printed ZnO-NPs films, the spectra were measured using a double beam UV-VIS-NIR spectrophotometer (Jasco V-670). Phase transformation and crystallization were measured using high resolution X-ray diffraction (X PETPRO MRD, Phillips). The current-voltage (I-V) characteristics of MIM were measured by an HP 4156A semiconductor parameter analyzer. The capacitance measurements were conducted with an HP 4284A Precision LCR meter. All the measurements were carried out at room temperature in the dark. The surface microstructures of ZnO film on the dielectrics were characterized using a scanning electron microscope (SEM, XL-40FEG, Philips).

3. Results and Discussion

A sedimentation test was supplied by the ZnO-NPs suspensions with the added amines of 0 and 5.2-vol%, whose result after 0 hr and 2 weeks is presented in Figures 2(a) and 2(b), respectively. While the butylamine dissolve in the solution, the rapid changes to transparent and remains with added-butylamine of 3 wt%. It was observed that the suspension without butylamine have been precipitated obviously and the ink sample containing the amines remains stable.

3.1. Morphological Properties. Figures 3 and 4 show the optical microscope and scanning electron micrograph of the ZnO thin film on a PVP/ITO/glass substrate, respectively. It was observed that hexagonal particles were closely packed on the substrate. The hexagonal particles seem to grow from the surface of the substrate. The pole formation may occurr due to the rapid evaporation rate of the solvent by the low boiling temperature or the viscosity excessively low to aggregate the ZnO NPs film with possibly high fluidity. In organic slurry, in order to disperse uniformly nanoparticles, the smaller molecular and shorter chain dispersants such as amines, phosphate esters, fatty acids, or carboxyl acids are used [23, 24]. In certain literature, increasing solid

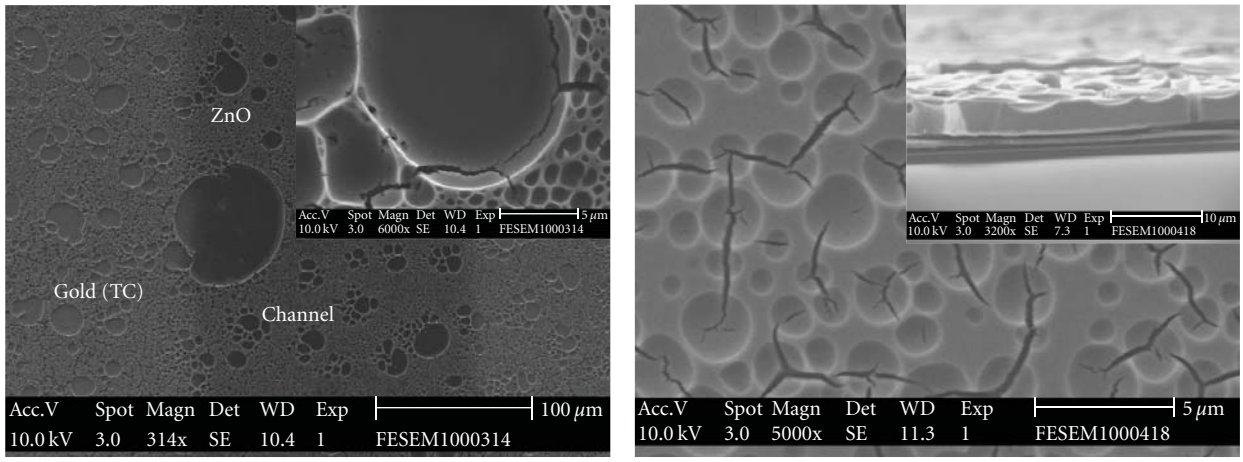


FIGURE 4: Scanning electron microscopy image of the inkjet-printed ZnO-NPs film using various concentrations onto the IJP-dielectric layer of a top-cntact transistor (plain view): (a) 3 wt%; (b) 7 wt%.

phase in the coating solution could decrease the shrinkage and pole for growth of smooth films [25]. Nevertheless, we obtained the different result and Figure 5 *illustrated* dispersants with lower boiling point such as butylamine in Marangoni flow mechanism [26]. Butylamine [23] as a ligand with a shorter chain and a low boiling point (78°C) can instead of the comprise acetate ($CH3COO^-$) ligand groups chelating with zinc atoms on the surface of ZnO nanocrystals to help achieve high-concentration dispersions of the suspension, hence the residual groups can be removed readily. In particular, butylamine in the higher solid phase content of the ZnO-NPs suspension evaporated faster than other solvent to the nanoparticles aggregated due to the high surface energy during drying, which may results in crack, split and unsmooth by non-uniform deposition and stress after annealing.

3.2. Structural Properties. The properties of the ZnO thin films fabricated by inkjet-printing under the appropriate conditions are examined. Figures 6(a)–6(d) show the X-ray diffraction spectrum of the ZnO nanoparticle powder, spin-cast film, and inkjet-printed film. In Figure 6(a) of X-ray diffraction spectrum, the peaks at 2θ = 31.72, 34.36, 36.18, 47.44, and 56.5°, corresponding to the lattice planes (100), (002), (101), (102), and (110), respectively, of the hexagonal phase of ZnO [27], were present. The XRD pattern indicates that the longer heating condensation time could enhance the orientation of (101) phase, which anticipate enhancing the crystallinity of the ZnO-NPs layer for the performance of these devices. The peak at 2θ = 36.04°, which corresponds to the diffraction from the (101) plane, and the stronger crystalline quality were attributed to Zn^{2+} in the mixture as shown in Figures 6(b) and 6(c). The patterns also exhibited that the spin-cast ZnO/Zn^{2+} film formed on PVP dielectric by annealing in RA at low temperature of 200°C had polycrystalline property in *evident*, which probably scatters or trap the carriers of transport.

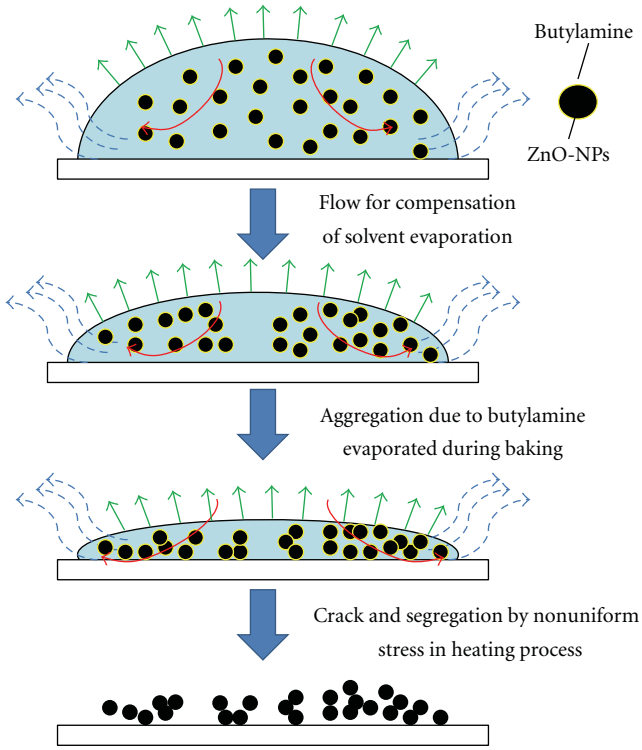


FIGURE 5: The modified formation process of droplet drying onto the surface of the substrate with inkjet printing [26].

The crystallite size of ZnO nanoparticles with increase in synthesis time was calculated using Scherrer's formula from Cullity (1970):

$$D = \frac{0.9\lambda}{B\cos\theta}, \quad (1)$$

where λ, θ, and B are the X-ray wavelength (1.54056 Å), Bragg's angle, and the full width at half maximum (FWHM)

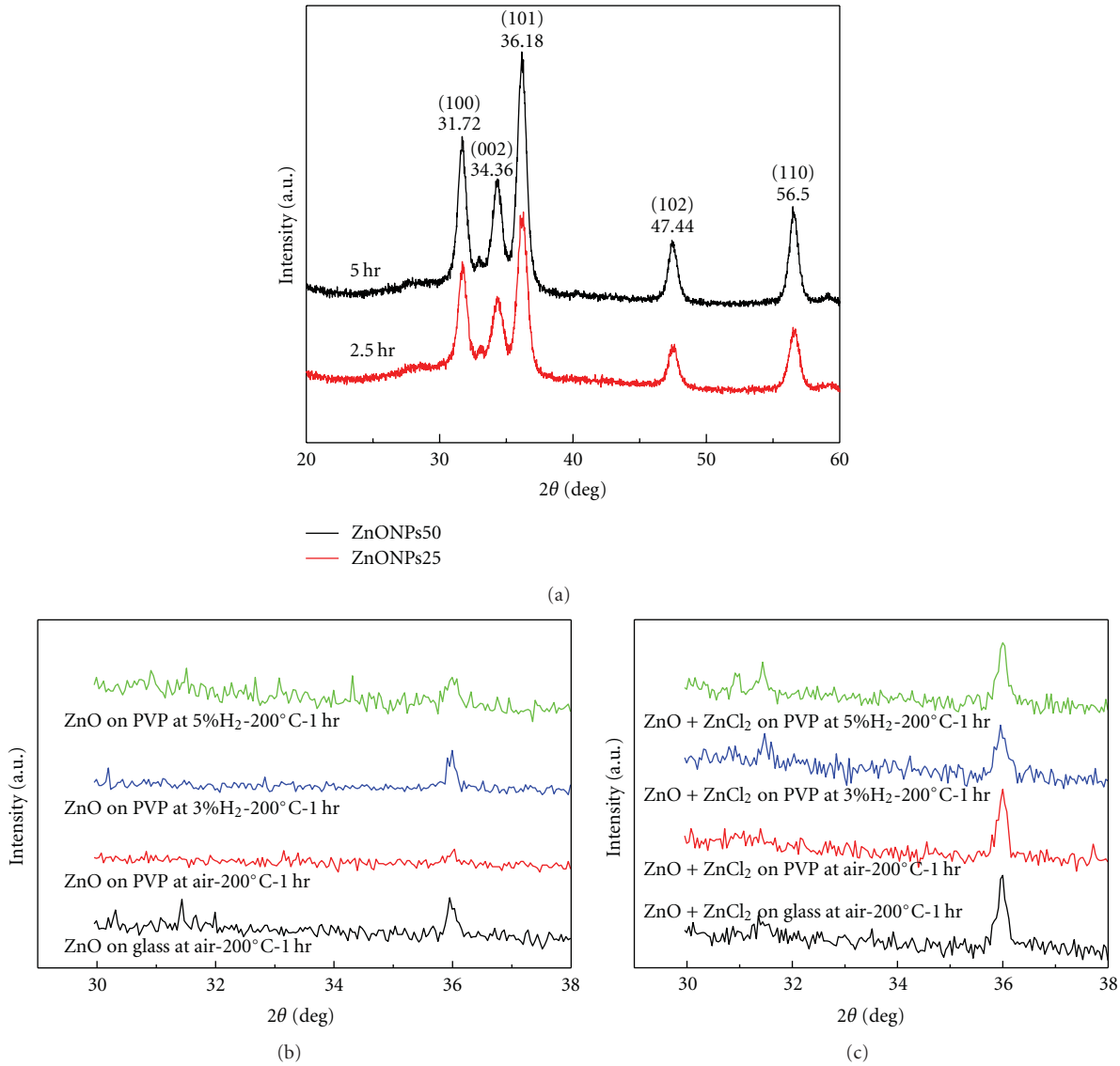


Figure 6: XRD patterns of ZnO with different composite of inks after annealing in various atmospheres: (a) nanoparticles of different synthesis times; (b) and (c) spin-cast films with inks of ZnO-NPs and ZnO-NPs/Zn^{2+}, respectively.

of the peak. It was found that the average sizes of ZnO particles in 2.5 and 5.0 hr are 9.7 and 13.06 nm, respectively. The sizes of crystallites corresponding to major diffracting plan are summarized in Table 1. We remark that the crystallites are smaller on the surface of the PVP film, except ZnO-NPs annealed in RA (3 vol%), which demonstrates the lager grain size with decreasing the amount of grain boundary.

3.3. Optical Properties. Figure 7 shows the optical transmittance spectrum of the entire IJP-ZnO film (excluding other layers of device or substrate), which exhibits the energy gap of ~3.35 eV. The transmittance pattern in visible part of the spectrum (400–700 nm) is around 60–70%, while the printed film with the lower concentration of the suspension.

3.4. Electrical Properties. The current density-voltage characteristic of inkjet-printed PVP dielectric is shown in Figure 8. The insets in Figure 8 show an optical image and profiler measurement result of the inkjet-printed PVP layer. We obtained that the IJP film possesses a leakage current less than 10^{-8} A/cm^2 under bias of 100 V applied. Nevertheless, taking into account the insulator thickness excluding the gate contact, the dielectric strength of the IJP-film was calculated about 0.83 MV/cm. The stronger strength with thick layer can resist the device work, but induced carriers in the active channel of a transistor in "on" mode decreas due to the weak polarity. We also calculated the dielectric constant of 4.17 at 1 kHz by the C-V characteristic analyzed.

The ZnO-NPs deposited on glass and PVP/glass by annealing at low temperature of 200°C and exhibited Hall effect mobilities of the latter samples in RA exceeding

Table 1: Crystallite sizes calculated from XRD.

Composite	Substrate, atmosphere condition	2θ (°)	FWHM (rad)	D (nm)
ZnO-NPs (S.C. = 3 wt%)	Glass	36	3.5 E-3	41.8
	PVP/glass, air ambient	36.08	3.5 E-3	41.8
	PVP/glass, N_2 + H_2-(3 vol%)	36.04	2.6 E-3	55.7
	PVP/glass, N_2 + H_2-(5 vol%)	36.04	4.5 E-3	32.1
ZnO-NPs+Zn^{2+} (S.C. = 3 wt%)	Glass	36.01	3.8 E-3	49.1
	PVP/glass, air ambient	36.08	3.1 E-3	39.7
	PVP/glass, N_2 + H_2-(3 vol%)	36.04	1.5 E-2	36.3
	PVP/glass, N_2 + H_2-(5 vol%)	36.04	6.2 E-3	23.2

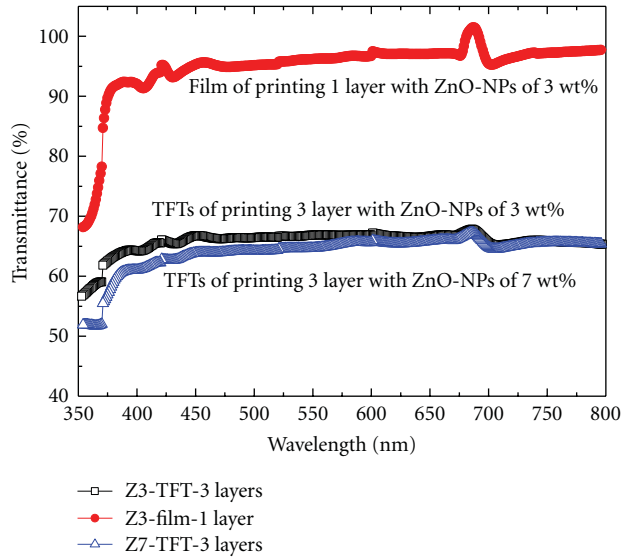


Figure 7: Plots of the measured optical transmission spectrum of the 1 layer ZnO-NPs of 3 wt% as a film; the device with 3 layer printed ZnO-NPs of 3 wt% and 7 wt%.

8 cm^2/Vs are shown in Figures 9(a) and 9(b), which have electric potential indeed with an order of magnitude larger than those of amorphous silicon for flexible electronics. A postannealing step at 200°C in an H_2 + N_2 (3 vol%) atmosphere was performed to improve the electrical performance of the other transistors for the measurement.

Finally, we implemented successfully the printer using a well-dispersed ZnO-NPs suspension to fabricate the active layer and gate dielectric of a top-contact TFT (TC-TFT) at low temperature. Figure 10 shows the transfer and output characteristic of ZnO-NPs-based TFTs fabricated using inkjet-printed active channel and gate dielectric. The I_D-V_D curve of the ZnO-based TFT device was measured for the output drain current as the drain voltage (V_D)

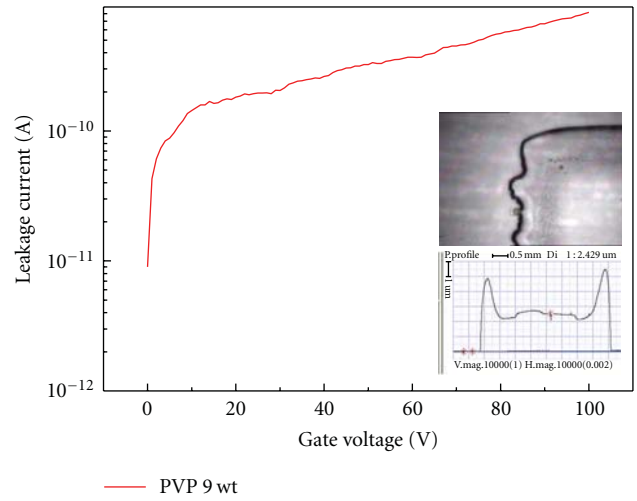


Figure 8: Leakage current density-voltage characteristic of the inkjet-printed gate dielectric layer. Optical microscopy image and thickness measurement of the inkjet-printed dielectric layer on ITO/glass (plain view).

was swept from 0–60 V at gate voltage of 0–50 V in 10 V increments. The I_D-V_D ZnO-based TC-TFT shows a typical electrical behavior, pinch-off, and current saturation. It also was observed that the device turns off with zero gate bias indicating that the ZnO-NPs TFT operate in accumulation mode. The field effect mobility (μ) is calculated from the saturation regime of the transfer characteristics with the the following relationship for the continuous thin film [28]:

$$\mu = \frac{L \cdot g_m}{W \cdot C_{ox} \cdot V_{DS}}, \quad (2)$$

where L, W, and C_{ox} indicate the channel length, channel width, and dielectric capacitance, respectively. The off-current, current on/off ratio, saturation field mobility, and threshold voltage calculated are 1.2×10^{-8} A, ~4×10^{1} 0.69 cm^2/Vs, and 25.5 V, respectively. The ZnO-NPs-based TC-TFT has identical saturation field mobility and off-current. However, the mobility is still lower than those published ZnO-TFTs. The on-current did not rise effectively may be attributing to the ZnO-NPs film quality, poor polarity by thick PVP, or interface characteristics of heterolayers. Raising the sheet resistance and excess defect formation due to the rapider evaporation of butylamine in the suspension from the film surface result in adjacent NPs as-aggregated each during the drying process, which made the on-current decline. In Figure 4, we observed films printed with low-concentration suspension reducing the defect such as crack and split. Nevertheless, the inkjet-printed ZnO-NPs-based TFT device is suitable for flat plate display, which would be applied further.

4. Conclusions

In conclusion, we have made good use of sol-gel method to prepare ZnO NPs ink, introduce soluble polymer, and

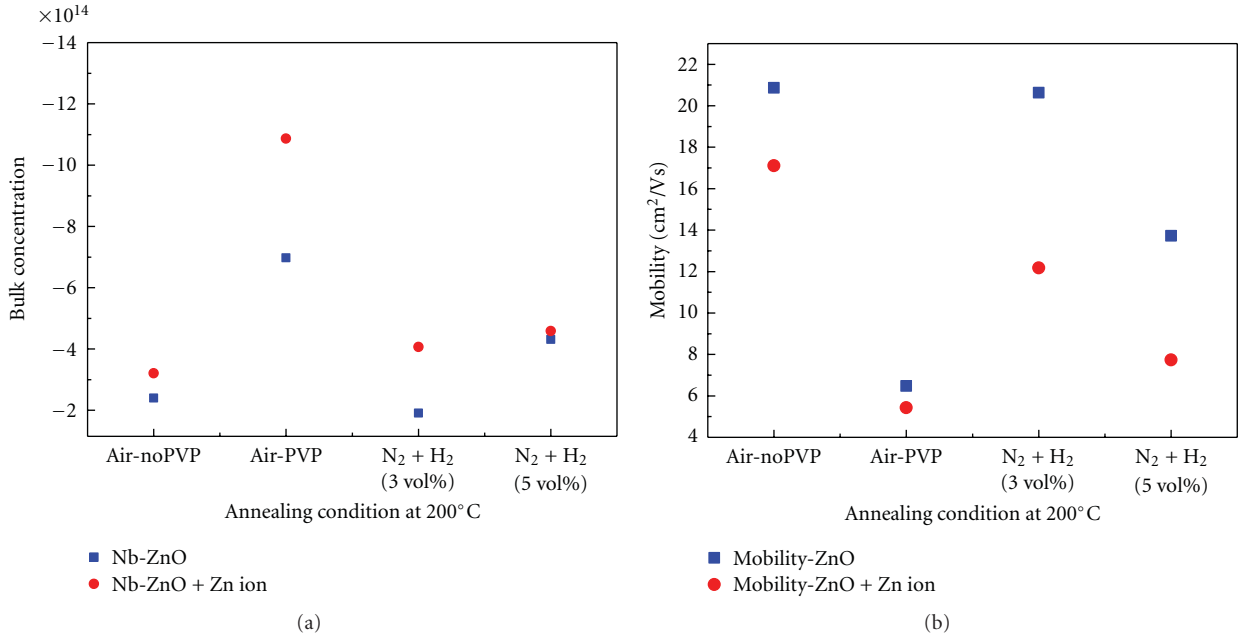


FIGURE 9: (a) Bulk concentrations and (b) Hall mobilities of the spin-cast ZnO-NPs and ZnO-NPs/Zn^{2+} films on gate dielectric.

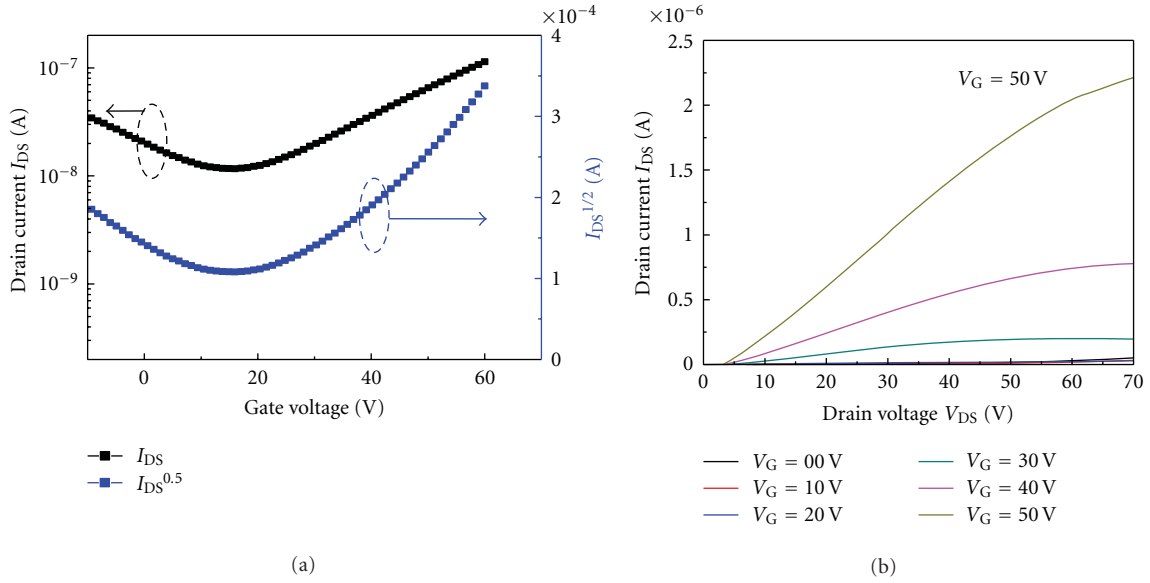


FIGURE 10: Transfer and output characteristic of ZnO-based TFTs fabricated using inkjet-printed active channel and gate dielectric layers.

fabricated directly printable gate dielectric films and active channel layers for TFTs using inkjet printing. For printing with mask-free process of semiconductor, preparing the NP inks by dispersant and butylamine, the nano-ZnO particles in the suspension were well dispersed to transparent and more stable effectively for more than 2 weeks then micronozzle jets successfully. Furthermore, in this work, we successfully utilize inkjet printing process to fabricate the active and insulator layers of TFT devices. It is expected that it is possible to implement the low-cost nanoparticles materials and high-performance devices using a simple solution-based fabrication processes.

Acknowledgments

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Review Article

One-Dimensional SnO_2 Nanostructures: Synthesis and Applications

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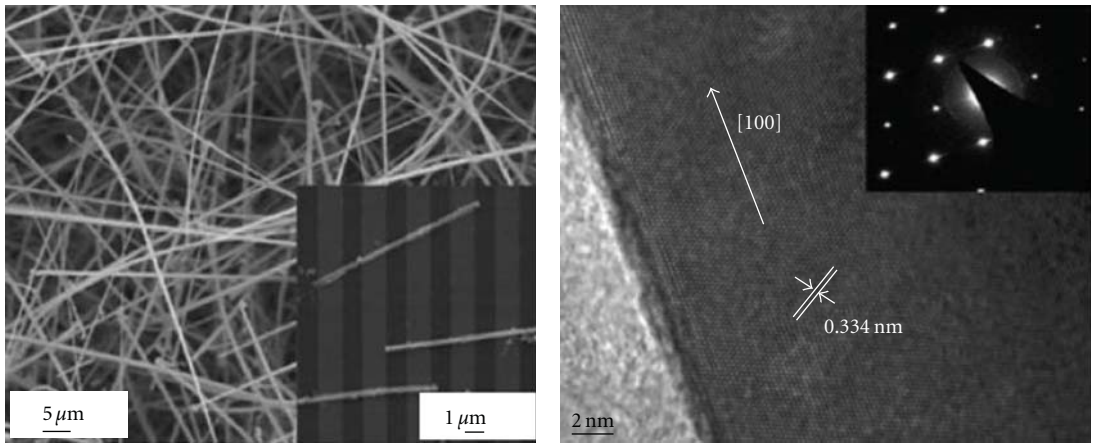
Nanoscale semiconducting materials such as quantum dots (0-dimensional) and one-dimensional (1D) structures, like nanowires, nanobelts, and nanotubes, have gained tremendous attention within the past decade. Among the variety of 1D nanostructures, tin oxide (SnO_2) semiconducting nanostructures are particularly interesting because of their promising applications in optoelectronic and electronic devices due to both good conductivity and transparence in the visible region. This article provides a comprehensive review of the recent research activities that focus on the rational synthesis and unique applications of 1D SnO_2 nanostructures and their optical and electrical properties. We begin with the rational design and synthesis of 1D SnO_2 nanostructures, such as nanotubes, nanowires, nanobelts, and some heterogeneous nanostructures, and then highlight a range of applications (e.g., gas sensor, lithium-ion batteries, and nanophotonics) associated with them. Finally, the review is concluded with some perspectives with respect to future research on 1D SnO_2 nanostructures.

1. Introduction

One-dimensional (1D) nanoscale materials, such as nanotubes, nanowires, and nanobelts, have attracted significant attention due to their unique size- and dimensionality-dependent electrical, optical, chemical, and mechanical properties and promising applications as interconnection and functional components in designing nano-sized electronic and optical devices [1, 2]. 1D semiconductor nanostructures represent an important and broad class of nanoscale wire-like structure, which can be rationally and predictably synthesized in single crystalline form with controlled chemical composition, diameter, length, and doping level with high precision. The availability of nanostructures has enabled a wide-range of proto-type devices and integration strategies [3, 4].

It is well known that materials behave differently at the nanoscale than their bulk counterparts. Low-dimensional nanoscale materials, with their large surface areas and possible quantum confinement effects, exhibit superior mechanical, thermal, chemical, electrical, and optical properties distinct from their bulk counterparts. The manipulation of well-controlled precise dimensions, crystallinity, and composition of 1D nanostructures gives rise to unique properties, thus enabling a variety of applications that would not be possible with materials with bulk dimensionality. Doubtlessly, a thorough understanding of the fundamental properties of the 1D nanostructures system is indisputably the prerequisite of research and development towards practical applications [5].

As a n-type direct wide-band semiconductor (E_g = 3.6 eV at 300 K), SnO_2 is transparent in the visible light region and useful as optoelectronic devices [6], catalyst supports [7], transparent conducting electrodes [8], antireflective coatings [9], and a proto-type material for metal oxide sensors [10]. One-dimensional tin oxide nanostructures have been synthesized by a variety of techniques, including vapor transport [11], carbothermal reduction [12], laser ablation of pure tin in an oxidizing Ar/O_2 atmosphere [13], oxidation of electrodeposited tin wires [14], oxidation of tin vapors at elevated temperatures [15], solvothermal synthesis [16], and electrospinning [17], and so forth, Our group reported a molecule-based chemical vapor deposition (MB-CVD) to synthesize 1D SnO_2 nanowires [18, 19], nanowire arrays [20, 21], and heterostructures [22] by the decomposition



(a) (b)

Figure 1: SEM image and of high-resolution TEM image with the corresponding SAED pattern of SnO_2 nanowires.

of a single-molecular precursor $[Sn(O^tBu)_4]$ containing preformed Sn-O bonds on gold nanoparticles, on a Si, Al_2O_3, and TiO_2 substrates via the well-known vapor-liquid-solid (VLS) growth mechanism. Meanwhile it is precisely controlled over chemical composition, morphology, and deposition rate.

This article will provide a helpful review of the state-of-the-art research activities focused on synthesis and devices of 1D SnO_2 nanostructures. The first section introduces typical 1D nanostructures obtained on SnO_2, including nanowires, nanotubes, nanobelts, and some special nanostructures. Next, some important electronic and optoelectronic devices built on 1D SnO_2 nanostructures are presented, which include gas sensor, lithium-ion batteries, and nanophotonics. This review will then conclude with some perspectives and outlook on the future developments in the 1D SnO_2 nanostructures and related research areas.

2. Typical 1D SnO_2 Nanostructures

2.1. Nanowires. SnO_2 nanowires have been synthesized by several physical and chemical methods, for example, vapor-solid (VS) synthesis by SnO evaporation under pulsed flow conditions led to the formation segmented wires [23]. In addition, thermal evaporation of SnO or SnO_2 was also used to the formation of nanowires in high quantity [24]. Further, SnO_2 nanowires have been obtained by self-catalyzed growth mechanism via carbothermal synthesis [25], the laser ablation of pure tin in oxidising Ar/O_2 atmosphere [13], and oxidation of electrodeposited tin wires within structure directing AAO membranes [26] or through oxidation of tin vapours at elevated temperatures [15]. The catalyst-assisted molecule-based CVD growth is a generic approach towards controlled synthesis of metal oxide nanostructures and had been demonstrated for SnO_2, as shown in Figure 1. It is revealed that the average radial dimension of the SnO_2 wires is approximately 0.9–1.1 μm. The indexing of the SAED pattern shows that the SnO_2 nanowires grow along the [100] direction with an interplanar spacing of 0.334 nm, which corresponds to the {110} plane of SnO_2 in the rutile phase [18]. Large surfaces covered with tin oxide nanorods could be achieved by an aqueous approach controlling ionic strength and pH of precursor solutions [27].

2.2. Nanotubes. Considerable attention has also been paid to semiconducting nanotubes due to high surface-to-volume ratios compared with their solid wire counterparts since the first report of carbon nanotubes by Iijima in 1991 [28]. Nanotubes are often obtained for materials with layered or pseudolayered structures [29]. For the preparation of SnO_2 tubular structures, the template-assisted approach has been proven to be an effective route, which generally involves the use of removable templates, such as preobtained nanorods [30], cellular fibers [31], porous membranes [32], and carbon nanotubes (CNTs) [33]. However, the morphologies of the tubular structures are rather limited due to the difficulty in fabricating templates with diverse morphologies. Recently, 1D silica mesostructures are used as sacrificial templates to synthesize SnO_2 nanotubes with preserved morphologies via a simple hydrothermal route (Figure 2(a)), resulting in the formation of well-defined SnO_2 nanotubes with different lengths and unique helical SnO_2 nanotubes with a wealth of conformations (Figures 2(b) and 2(c)) [34]. In addition, SnO_2 nanotubes with controlled diameter and length were synthesized using an electrochemical method at room temperature. The length and wall thickness of the nanotubes increased monotonically with the deposition time, and the diameter of the nanotubes was altered by varying the pore size of the scaffolds [35].

2.3. Nanobelts. Nanobelts (or nanoribbons), an independent family in the realm of 1D nanomaterials, are regarded as an ideal system to fully understand dimensionally confined transport phenomena and may act as valuable units to construct nanodevices owing to their well-defined geometry [36]. SnO_2 nanobelts have been successfully synthesized by thermal evaporation of different source materials. Structurally perfect and uniform single crystalline SnO_2

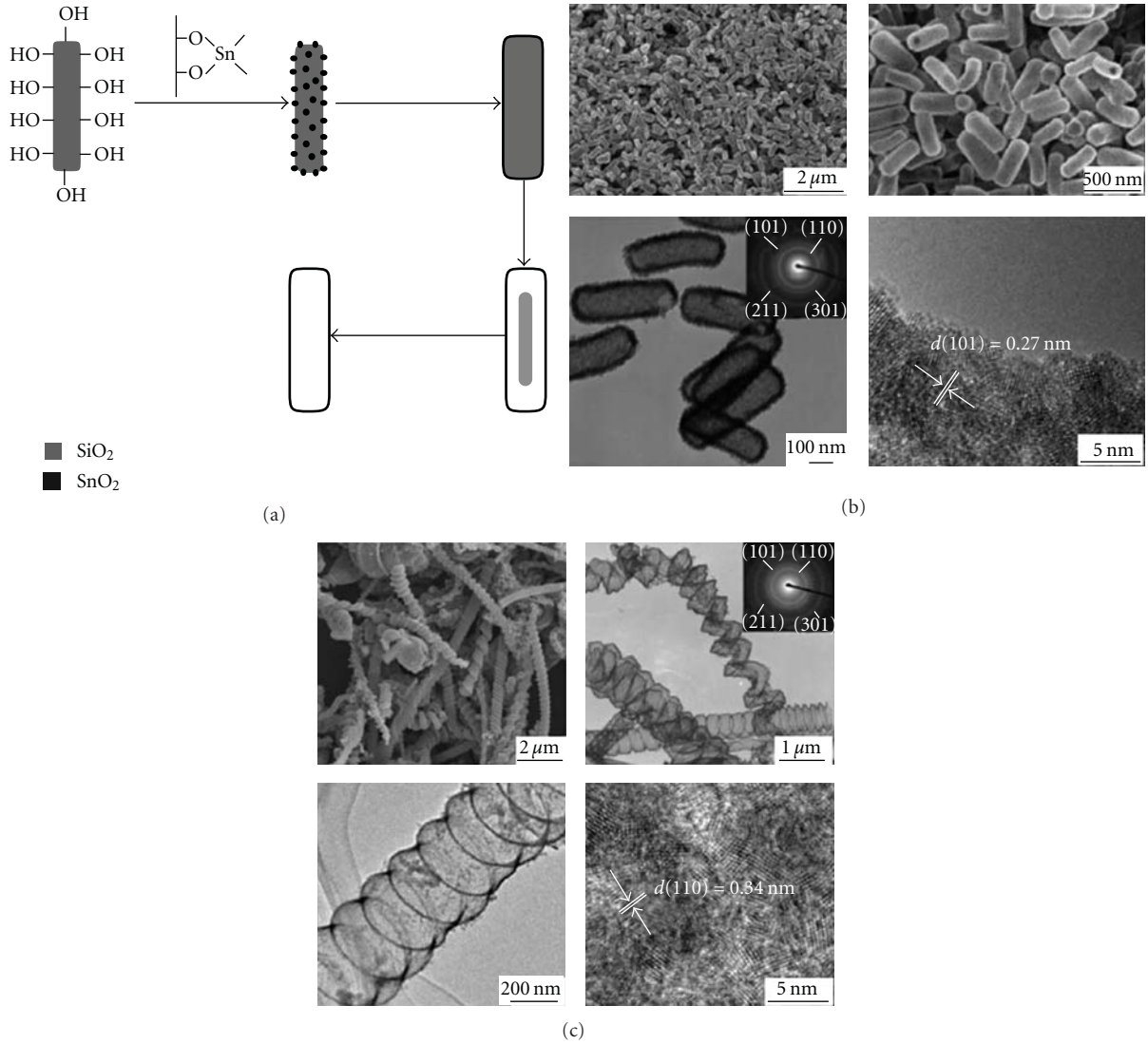


Figure 2: (a) Schematic illustration of a tentative mechanism for the template-directed formation of SnO_2 nanotubes. SEM and TEM images of (b) short and (c) helical SnO_2 nanotubes.

nanoribbons, with widths of 30–200 nm, width-to-thickness ration of 5–10, and length of several hundred micrometers to a few millimeters, were synthesized by simple thermal evaporation of SnO_2 or SnO powder at high temperatures. It is worth to notice that wire-like nanostructures can be observed in the first stage of growth process due to the presence of strain. The profile of the fringes implies that the geometrical shape of wire-like nanostructures is likely to be a ribbon [37]. SnO_2 nanobelts also were synthesized by mixture of Sn foil and SnO powders with the same growth mechanism [24]. A simple rapid oxidation of elemental tin was proposed for large-scale production of SnO_2 nanoribbons. The width of the nanostructure was sensitive to the reaction temperature. When the growth temperature was increased to 1350°C, the diameter range of these nanostructures increased markedly to 50–350 nm (Figure 3(b)) compared to the wire-like nanostructures grown at 1080°C (Figure 3(a)). The lengths of the nanoribbons were up to several hundreds of micrometers, and the typical width and thickness were in the range of 30–150 nm and 10–30 nm (Figure 3(c)), respectively. The as-synthesized SnO_2 nanoribbons appeared to be single crystalline and exhibited [110] and [203] growth directions (Figures 3(d)–3(e)) [38]. Recently, {101} surfaces of zigzag SnO_2 nanobelts have been synthesized by a VS process, which are reduced surfaces terminated by Sn atoms and the Sn terminated surface is a nonpolar surface. As both reduced SnO and stoichiometric SnO_2 (101) surfaces are neutral terminations, the polar surface model is no more suitable for the (101) type surface of rutile SnO_2 nanobelts [39].

2.4. Other SnO_2 1D Nanostructures. Synthesis and assembly of SnO_2 1D nanostructures with special morphologies, shapes, and compositions have attracted great interests very recently because they process unique properties and functionalities that are not accessible in the single-component materials, due to the combination of material classes such

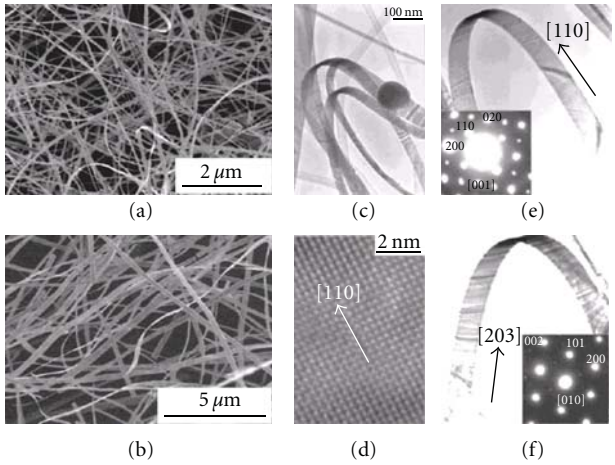


Figure 3: SEM images of SnO_2 (a) wire-like nanostructures and (b) nanoribbons, and TEM images (c)–(f) of SnO_2 nanoribbons.

as metals, metal oxides, semiconductors, and polymers. They may also be used to fabricate special electronic and optoelectronic devices which cannot be fulfilled using simple 1D nanostructures [40, 41]. Branched 1D SnO_2-V_2O_5 heterostructures were fabricated by growing vanadium oxide nanostructures on as-grown SnO_2 backbones (Figure 4(a)). HR-TEM images of the SnO_2-V_2O_5 interface revealed a strong alignment of the two different crystal lattices, resulting in a heteroepitaxial growth of vanadium oxide on tin oxide. The single-crystalline nature and growth direction of the V_2O_5 were indexed to be ⟨111⟩ (Figure 4(b)) [20]. Hierarchical nanostructures with SnO_2 backbones and ZnO branches are successfully prepared in a large scale by combining the vapor transport and deposition process (for SnO_2 nanowires) and a hydrothermal growth (for ZnO). The ZnO nanorods grow epitaxially on the SnO_2 nanowire side faces mainly with a four-fold symmetry. The number density and morphology of secondary ZnO nanostructure can be tuned by adjusting the baking condition, such as the salt concentration, reaction time, and additives [42]. In addition, SnO_2 nanobelt/CdS nanoparticle core/shell heterostructures are successfully prepared via a simple and efficient sonochemical approach. The CdS nanoparticles are nearly spherical in shape and have typical sizes in the range of 10–20 nm. The measured spacing of the crystallographic planes is 0.315 nm, which corresponds to the {101} lattice plane of the hexagonal structured CdS crystal [43].

3. Applications of 1D SnO_2 Nanostructures

As an important group of wide-band gap semiconductors with tunable conductivity and high transparency, 1D SnO_2 nanostructures have been used to fabricate nanoscale gas sensor, electronic and optoelectronic devices.

3.1. Gas Sensor. Gas sensing using nanomaterials is an attractive, versatile application for important molecule species, environmental and security-checking purposes [44, 45].

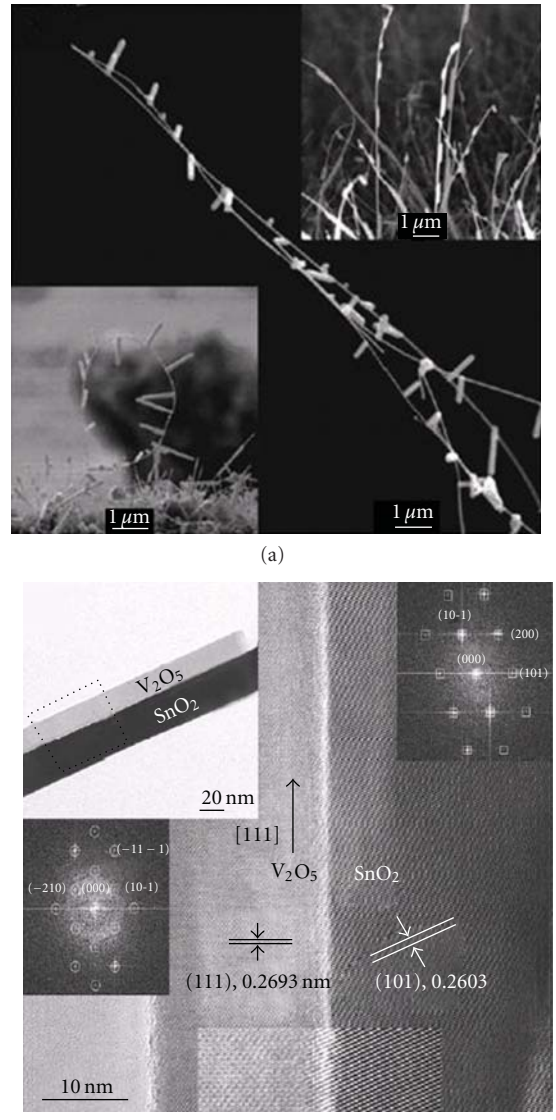


Figure 4: SEM and TEM images of SnO_2-V_2O_5 heterostructures.

The advantages of using 1D nanostructures for chemical sensing are diverse. With a large surface-to-volume ratio and a Debye length comparable to the nanowire radius, the electronic property of the nanowire is strongly influenced by surface processes, yielding superior sensitivity than their thin film counterpart. The sensing mechanism of metal oxides is mainly governed by the fact that the oxygen vacancies on the oxide surfaces are electrically and chemically active, therefore, the conductivity (or resistivity) of oxide nanomaterials is strongly affected by the adsorbed molecules. SnO_2 is n-type semiconductor with oxygen deficiency. The lattice oxygen is evaporated in the form of gas, which makes the doubly ionized oxygen vacancy and electrons. If tin dioxide is heated at 300–400°C, the oxygen in the atmosphere is adsorbed at the surface of SnO_2 with the negative charge. Because electron is provided from the surface of crystal, the surface of tin oxide becomes an electron depletion layer.

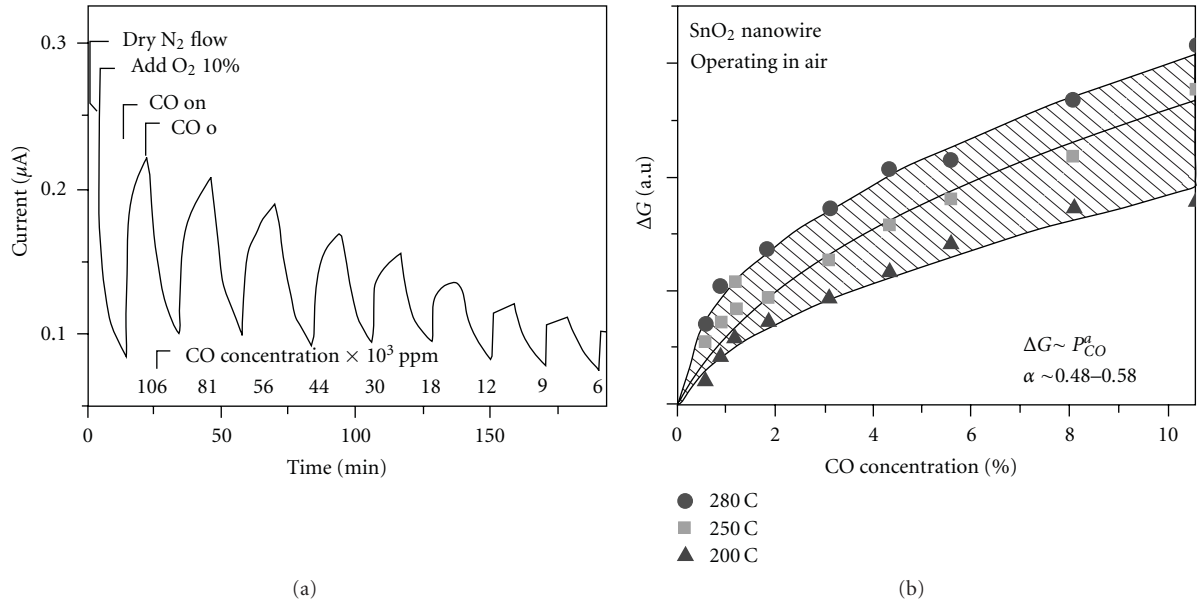


FIGURE 5: (a) Response of the SnO_2 nanowires towards CO pulses. (b) Change in conductance of individual SnO_2 nanowires as a function of CO concentration at three temperatures.

This means the formation of potential barrier near the grain boundary. If CO is present in the atmosphere, the CO oxidizes into CO_2 with the reaction of adsorbed oxygen and remaining electron returns to the SnO_2 crystal. This increases the electrical conductivity to a great extent. So, we can detect CO by measuring the remarkable resistance decrease upon CO reaction. Generally speaking, the reduction in resistance occurs mainly at the surface and can be explained by the reduction of potential barrier [46].

The first SnO_2 nanobelt chemical sensor was made on an alumina substrate by dispersing SnO_2 nanobelts atop prefabricated platinum interdigitated electrodes on a substrate. The sensor was employed to detect CO and NO_2 for environmental polluting species and ethanol for breath analysis. A single-SnO_2-nanobelt sensor integrated with microheaters to sense dimethyl methylphosphonate (DMMP) was fabricated. The conductance of the SnO_2 nanobelt sensor was reduced by 5% when the sensor was exposed to 78 ppb of DMMP [47]. It was also reported that light photoactivates molecule absorption and desorption as an alternative way to the use of temperature. An explosive environment is the typical application where the use of heated sensors is not favorable. The strong photoconducting response of individual single-crystalline SnO_2 nanoribbons makes it possible to achieve equally favorable adsorption-desorption behavior at room temperature by illuminating the devices with a ultraviolet (UV) light of energy near the SnO_2 bandgap. The active desorption process is thus photoinduced molecular desorption [48]. Kolmakov et al. realized an array of parallel nanowires of SnO_2 by using self organized highly ordered porous alumina templates. Conductance measurements were performed on isolated individual nanowires with vapor-deposited Ti/Au microcontacts. They analyzed the behavior of nanowire in N_2 and N_2 + 10% O_2. CO reacts with preadsorbed oxygen species on SnO_2 to form carbon monoxide thus donating few electrons back into the bulk resulting in an increased conductivity, which depends monotonically on the gas phase partial pressure of CO (Figure 5) [14]. Single SnO_2 metal oxide nanowires are used at the nanoscale level as individual monocrystal for the electrical transduction of the gas interaction with these sensing materials. Electrical contact characteristics and resistance variations under different gas ambient are analyzed from two- and four-probe measurements of individual nanowires. CO and humidity behaviors are reported for single SnO_2 nanowires with CO detection threshold smaller than 5 ppm and measurement instability lower than 4% (Figure 6) [49]. A technical approach to fabricate practical devices by coupling a single-crystal SnO_2 nanowire sensing element with a microhotplate gas sensor platform was also presented [50].

In order to tune the sensitivity and selectivity of SnO_2 nanowires-based sensors, many techniques have been explored. The addition of a small amount of noble metals such as Au, Pd, Pt, and Ag and Ni speeds up surface reactions and improves selectivity towards target gas species [51]. Kolmakov examined the influence of the surface sensitization with catalyst particles of Ni/NiO and Pd [52]. Wan reported the use of Sb doping to tailor the resistivity of SnO_2 nanowires deposited by thermal evaporation process starting from a mixture of Sn and Sb powders in the ratio 10 : 1 [53]. Meanwhile, Pan et al. modified SnO_2 nanowires by Ar/O_2 plasma treatment through preferential etching of the lattice oxygen atoms, which produced nonstoichiometric surface compositions that imparted a many-fold higher sensitivity toward gas absorption on such surfaces (Figure 7) [54].

3.2. Anode Materials for Lithium-Ion Batteries. Rechargeable lithium-ion batteries (LIBs) have been recognized as

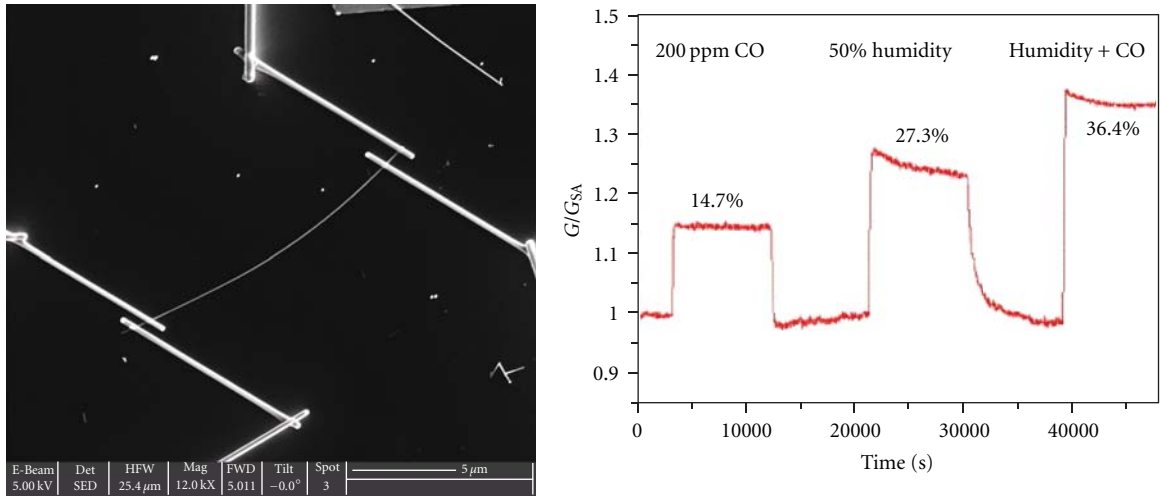


Figure 6: (a) A single SnO_2 nanowires contacted in a 4-probes configuration. (b) Comparison between the simultaneous detection of 200 ppm of CO and 50% of RH.

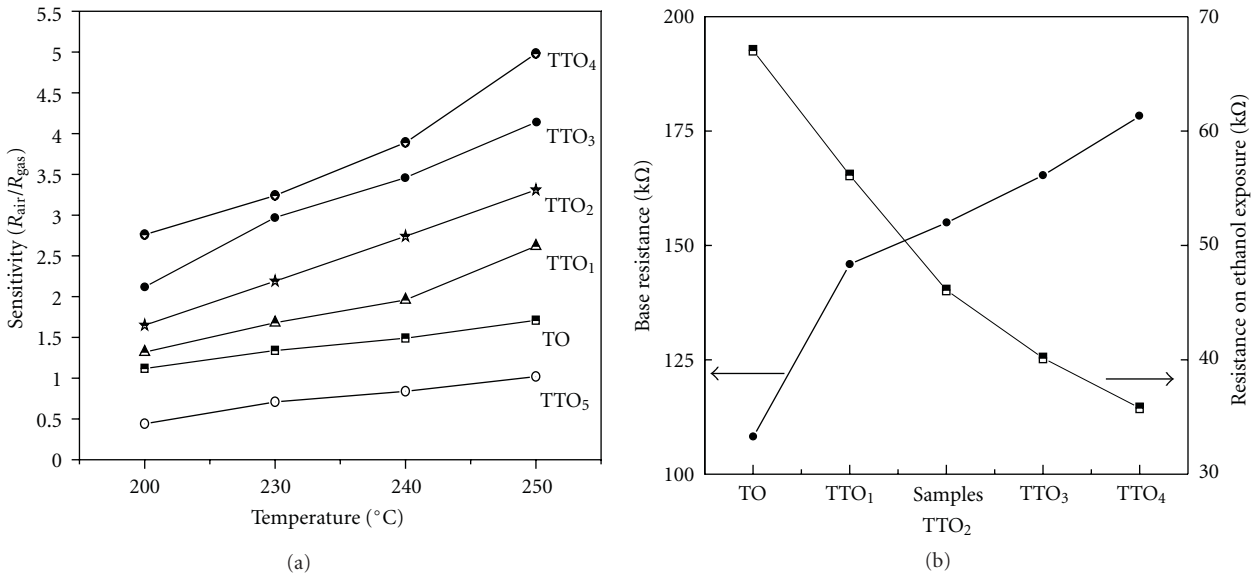


Figure 7: (a) Temperature-dependent sensing response curves and (b) base and sensing resistances dependency to the power of plasma treatment.

an attractive power source for popular mobile devices. At present, LIBs are efficient, light-weight, and rechargeable power sources for consumer electronics such as laptop computers, digital cameras, and mobile phones. Moreover, they have been extensively studied for use as power supplies of electric vehicles (EVs) and hybrid electric vehicles (HEVs), which require high energy and power densities [55].

As a promising anode material for LIBs, tin-based material has attracted growing attention owing to the extraordinary electrochemical behavior, such that the initial irreversible capacity induced by Li_2O formation, and the abrupt capacity fading caused by volume variation could be effectively reduced when in nanoscale form, the high theoretical capacity (992 $mAhg^{-1}$) and the higher operating voltage comparing to traditional carbonaceous anode active materials [56, 57]. The self-catalytically grown SnO_2 nanowires could provide more reaction sites on the surface and enhance the charge transfer in the electrochemical reactions. Moreover, Sn particles at the tips of nanowires also contributed to the Li^+ storage and prevented the capacity loss that is induced by the existing metal catalysts. SnO_2 nanowires showed an initial Coulombic efficiency of approximately 46.91% and improved cyclic performance and a higher reversible specific capacity of over 300 $mAhg^{-1}$ up to the 50th cycle as shown in Figure 8 [58]. In addition, SnO_2 nanowire

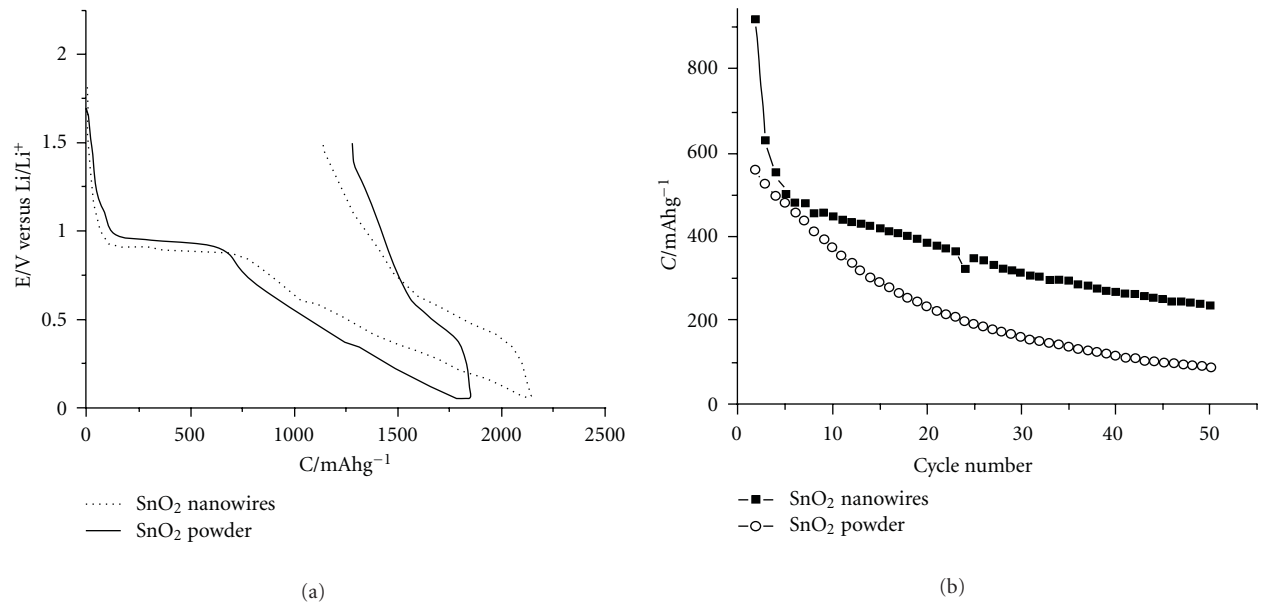


Figure 8: (a) The voltage profile for the first cycle between 0.05 V and 1.5 V compared with pure SnO_2 powder. (b) The cyclic performance from the second cycle to the 50th cycle of SnO_2 nanowires and pure SnO_2 powder.

electrode without any buffer layer was used as rechargeable LIBs and exhibited superior electrochemical performance stable cycling behaviors and delivered a high specific discharge capacity of 510 $mAhg^{-1}$, even at the 50th cycle [59].

SnO_2 nanorod arrays represent an excellent geometry because they can offer direct channels for efficient electron transport. SnO_2 nanorod array electrodes can be produced in a one-pot template-free alkaline hydrothermal process. The array electrode showed good performance as a LIB anode in properties such as capacity retention (580 $mAhg^{-1}$ after 100 cycles at 0.1 C) and rate capability (stable 350 $mAhg^{-1}$ at 5 C) [60].

SnO_2-based heterostructure is a very promising strategy to achieve high-power-density and high-energy-density LIBs. A high electrochemical activity of V_2O_5 loaded on SnO_2 nanowire-based electrode showed a very-high rate capability. The thin V_2O_5 layer is beneficial for fast Li^+ intercalation/deintercalation, while the SnO_2 core nanowire provides a fast path for electron transportation and also increases the electrochemical utilization of V_2O_5. SnO_2/V_2O_5 core/shell nanowires could deliver a high power density of 60 $kWkg^{-1}$ while the energy density remains as high as 282 $Whkg^{-1}$. A better rate capability was achieved at high temperature (Figure 9) [61]. Carbon-coated SnO_2 nanorod array also revealed excellent cycling stability (stable 320 $mAhg^{-1}$ at 3000 mAg^{-1}) and rate capability (585 $mAhg^{-1}$ after 50 cycles at 500 mAg^{-1}) [62].

3.3. Nanophotonics. Nanowires represent attractive building blocks for active nanophotonic devices, including light-emitting diodes (LEDs), lasers, and detectors [63, 64]. Significantly, the ability to assemble and electrically drive nanoscale sources and detector blocks could allow for fully integrated nanophotonic systems for use in applications ranging from biodetection through information processing. Nanowires of binary oxides have been employed throughout this work because of the variety of beneficial properties, including extreme mechanical flexibility and chemical stability.

SnO_2, has recently been shown to act as an excellent subwavelength waveguide because of its defect-related PL bands at 2.5 eV (green) and 2.1 eV (orange) (Figure 10) [65]. Nonresonant waveguiding (i.e., subbandgap light) in these structures can be achieved by simply focusing laser diodes on the end facet of the nanowire. SnO_2 wires have dimensions between 100 nm and 400 nm, an optimal size range to efficiently guide visible and UV wavelengths because of the high index of refraction of SnO_2 ($n > 2$). Optical linkages between active nanowires (GaN and ZnO) and passive nanowires (SnO_2) can be formed via tangential evanescent coupling (Figure 11). It has been shown that a staggered side-by-side configuration, in which the active and passive elements interact over a few microns, outperforms bridged, or direct end-to-end coupling. Weaker coupling is achieved by staggering structures with a thin air gap (several hundred nanometers) between them, allowing communication via tunneling of evanescent waves [66]. With further integration, it should be possible to create more functional geometries, such as branched optical hubs and Mach-Zehnder interferometers (optical modulators) that use the electro-optic effect for phase shifting. The integration of high-frequency electrically driven lasers with passive nanowire waveguides is the next step toward effectively transducing and routing packets of optical information within an optical computer

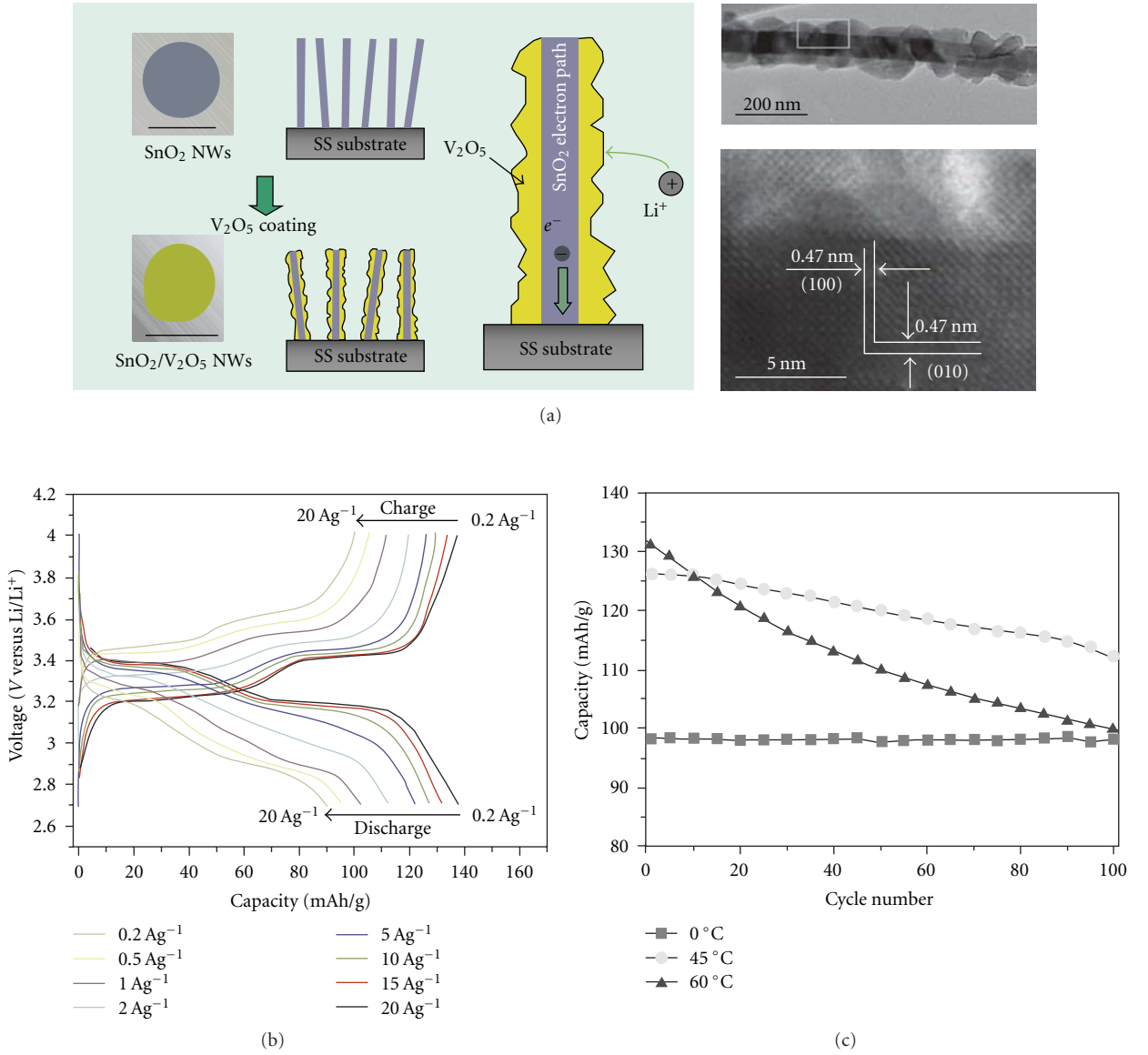


Figure 9: (a) Schematic diagram showing the strategy for coating V_2O_5 on SnO_2 nanowires, and typical TEM images of a single SnO_2/V_2O_5 core/shell nanowires, (b) the galvanostatic charge/discharge curves at different current densities, and (c) the cycling performance at different temperatures of the SnO_2/V_2O_5 core/shell nanowires electrode tested.

or communication device [67]. However, the goal of room temperature, electrically driven nanolasers, remains an active area of current research.

4. Summary and Perspective

In summary, we provide a comprehensive review of the state-of-the-art research activities focused on rational synthesis (e.g., nanowires, nanobelts, nanotubes, and heterostructures) and potential applications (e.g., gas sensor, lithium-ion batteries, and nanophotonics) of 1D SnO_2 nanostructures. The fascinating achievements, till now, towards the device applications of 1D SnO_2 nanostructures should inspire more and more research efforts to address the remaining challenges in this interesting field in the future.

Controlled manipulation of matter at the nanoscale will lead to fascinating and novel behavior and also impact device properties. The ability to rationally control key 1D SnO_2 nanostructures parameters during growth, fabricate intra-NW heterostructures with well defined [68], and atomically abrupt crystalline interfaces should further increase the versatility of 1D SnO_2 nanostructure-based electronic and photonic devices and also reduce the load for subsequent assembly processes.

Such a synthetic control will be extremely useful for creating precisely defined systems to investigate the effects of quantum confinement on electronic and optical properties

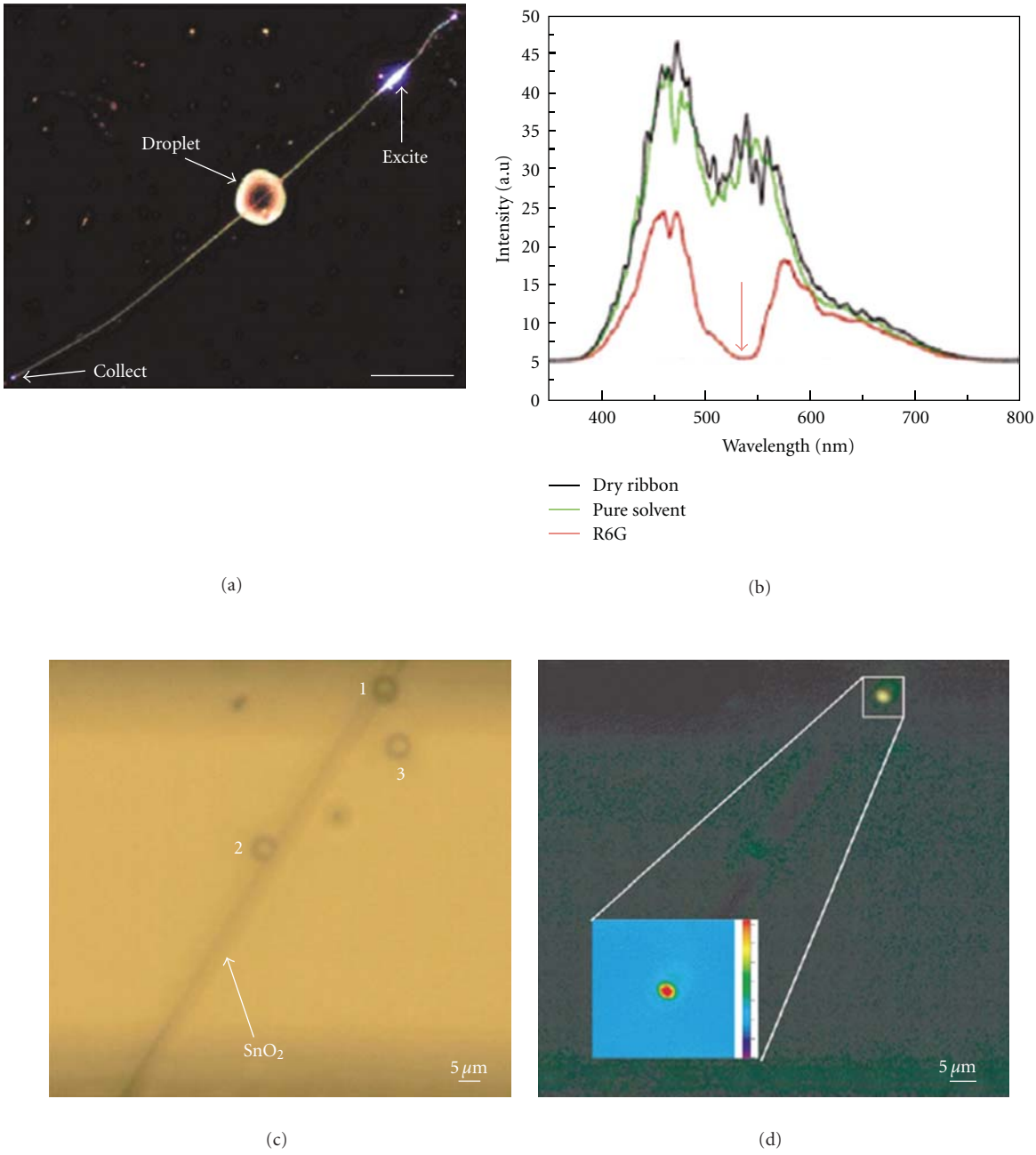


FIGURE 10: Demonstration of absorption and fluorescence schemes using individual SnO_2 nanoribbon waveguides. (a) Dark-field photoluminescence image of the absorption scheme showing an analyte centered in the middle of the ribbon and the labeled excitation and collection locations. (b) Spectra recorded after the SnO_2 defect emission traversed through the ribbon in air (black), pure glycol (green), and 1 mM dye-loaded glycol (red). (c) Bright-field image of 2 μm yellow-green fluorescent polystyrene beads placed with an optical trap precisely on or near a SnO_2 nanoribbon. (d) Fluorescence image of beads after waveguiding of photoluminescence from the SnO_2 ribbon. Inset: false color expansion of bead 1 during UV excitation of the ribbon.

of nanostructures resulting from the modification of the electronic density of states and also aid in developing novel nanophotonic devices.

Looking into the future, with extensive research in nanostructures synthesis to accurately control dimension and composition, a critical understanding of the modified properties of materials at the nanoscale, and the hierarchical assembly of nanostructures with exquisite spatial control, progress will be made, and new and interesting nanosystems will create the technologies of the future.

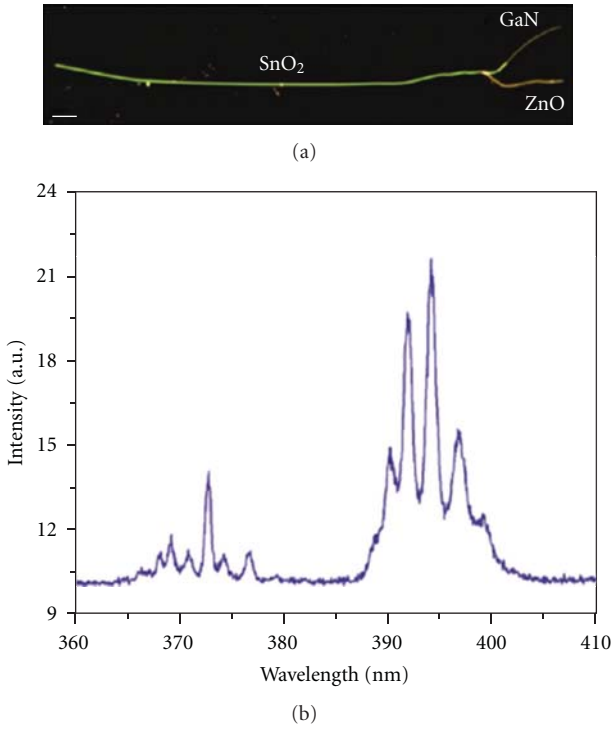


Figure 11: (a) Dark-field image illustrating the coupling of two nanowire lasers (GaN and ZnO) to a common SnO_2 nanoribbon waveguide. Scale bar = 25 μm. (b) Spectra recorded at the left terminus of the SnO_2 nanoribbon after simultaneous nanowire laser injection.

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Review Article

Vertical Silicon Nanowire Platform for Low Power Electronics and Clean Energy Applications

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This paper reviews the progress of the vertical top-down nanowire technology platform developed to explore novel device architectures and integration schemes for green electronics and clean energy applications. Under electronics domain, besides having ultimate scaling potential, the vertical wire offers (1) CMOS circuits with much smaller foot print as compared to planar transistor at the same technology node, (2) a natural platform for tunneling FETs, and (3) a route to fabricate stacked nonvolatile memory cells. Under clean energy harvesting area, vertical wires could provide (1) cost reduction in photovoltaic energy conversion through enhanced light trapping and (2) a fully CMOS compatible thermoelectric engine converting waste-heat into electricity. In addition to progress review, we discuss the challenges and future prospects with vertical nanowires platform.

1. Introduction

Since late 1990s, the nanowire has become a buzz word in nanoscience and nanotechnology domain with many promises, demonstrations and surprises in the technologically important and application-rich areas. For example, nanowire devices, especially in Gate-All-Around (GAA) architecture, have emerged as the front-runner for pushing Complementary Metal-Oxide-Semiconductor (CMOS) scaling beyond the roadmap. These devices offer unique advantages over their planar counterparts and other contenders, which make them feasible as an option for 15 nm and beyond technology nodes with sub-10 nm channel length devices already demonstrated through simulations [1] and experiments [2]. Indeed, the cylindrical geometry gives inverse logarithmic dependence of the gate capacitance on the channel diameter, and thus the gate length in these devices can be scaled with wire diameter without reducing the gate dielectric thickness aggressively. With the same principle, it also makes the GAA nanowire architecture an excellent candidate for Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) type nonvolatile memory applications where the gate dielectric has to be necessarily thicker. Chemical and biological sensing has been another important area where large surface to volume ratio enhances detection limit and make nanowire sensors as potential candidates [3, 4]. The giant piezo-resistive coefficient and reduced low frequency noise make the nanowires suitable for transducer world [5]. Nanowires have also shown excellent potential in the area of photonics [6], solar energy harvesting [7, 8], and energy storage [9]. Fundamentally, the improved properties of nanowire devices are a result of a combination of shape, density, and strong confinement of photon, phonon and electrons and their relative changes in reference to planar bulk structure.

The fabrication technology of nanowire can be broadly categorized into two groups: (i) the bottom-up and (ii) the top-down. The bottom-up approaches involving synthesis of nanowires have been extensively reviewed in the literature [10–12] and are not discussed in further detail here.

The top-down approach starts with pattern definition, mainly using conventional lithography, followed by pattern transfer and then trimming to reduce the diameter of the wire to nanoscale. Although isotropic wet etch can be used to trim the wire diameter, self-limiting oxidation process

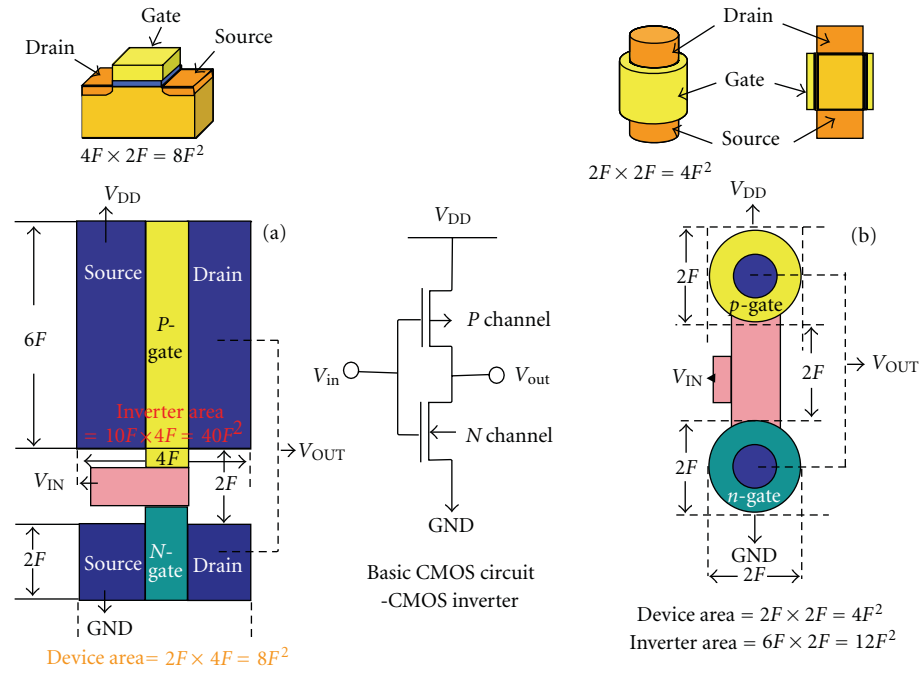


Figure 1: Schematic illustration of the footprint of (a) lateral and (b) vertical GAA nanowire MOSFET and corresponding CMOS inverters.

is generally used for better process control and has been extensively exploited at our institute [13].

In this paper, we review the progress of our top-down vertical nanowire technology platform from low power electronics and clean energy applications view point. A review of lateral nanowire platform focusing logic, nonvolatile memory, and biosensing applications has been published recently [13] and therefore will not be included here. The vertical platform resolves most of the fabrication-related challenges of lateral nanowires, for example, gate definition under the wire, gate etching on the wire, lithography, free gate length control and provides CMOS circuits with much smaller foot print as compared to any lateral (including planar, Fin, nanowire) MOS transistor at the same technology node. Being vertical, it decouples source/drain (S/D) implant processes and therefore acts as a natural platform for tunneling FETs—allowing independent tuning of S/D junctions and implant type for achieving low subthreshold slope (SS) and suppressing ambipolar behavior. Nonvolatile memory devices on vertical wires have the potential to be stacked vertically along the wire length in addition to footprint benefit similar to the CMOS. Under the green electronics title, Section 2 discusses the scaling through vertical approach followed by our progress on three electronic devices, namely, Metal-Oxide-Semiconductor field effect transistor (MOSFET), Tunneling field effect transistor (TFET), and SONOS nonvolatile memory (NVM); all fabricated in GAA format. In Section 3, we discuss clean energy harvesting, where results on solar cell showing performance improvement through enhanced light trapping and absorption, and a fully CMOS compatible thermoelectric engine converting waste heat into electricity, are presented. The challenges and future prospects with vertical nanowires are discussed in Section 4. Finally, Section 5 summarizes the paper.

2. Low Power Electronics

2.1. Scaling Through Vertical Approach. Vertical nanowire devices, having source, drain, and gate terminals on top of each other, occupy much less area than planar as described in Figure 1. In terms of half-pitch "F", generally the minimum lithographic printable feature size, a planar transistor occupies $8F^2$ while a vertical transistor can be designed in $4F^2$ thus reducing the foot print by 50% for a given technology node. When connected together to fabricate circuits, the impact is even more, for example, a CMOS inverter which uses $40F^2$ of area with planar devices can be fabricated in $12F^2$ using vertical nanowires, resulting in an area saving of about 70%. The area saving directly relates to improvement in speed and saving in power consumption through resistance "R" and capacitances "C", both of which scale directly with area. The circuit speed being inversely proportional to "RC"-constant increases by ~6.1 × (e.g., simply Speed $\propto 1/RC \propto (\text{Area})^{-3/2}$). The power consumption, being proportional to CV^2, reduces to 30% of the planar (e.g., Power $\propto CV^2 \propto$ (Area)). A summary of the area, speed, and power advantages with vertical nanowires devices as compared to planar and lateral nanowire is provided in Table 1. Worth mentioning here that these back-of-the envelop calculations do not take into account any parasitic.

Despite the same scaling potential from gate control perspective as for lateral wire, the vertical wire device takes lead over lateral wire in foot print scaling followed by speed and power advantage. Indeed the lateral wire device foot

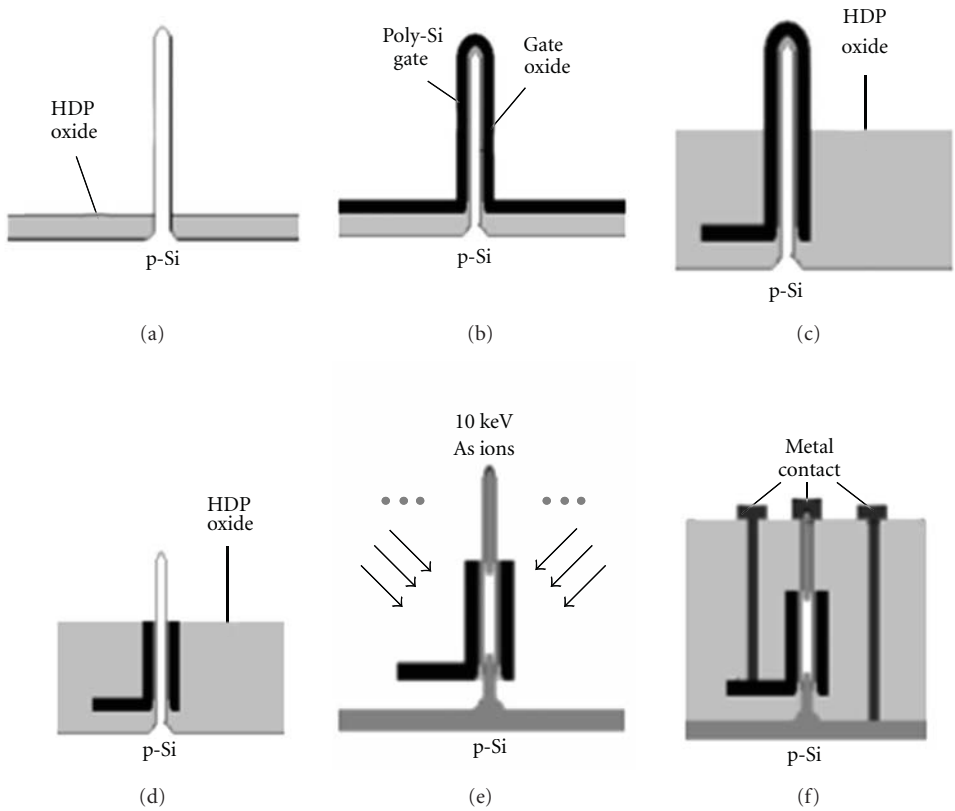


Figure 2: (a) Single silicon nanowire with bottom isolation, (b) after gate stack deposition, (c) after gate extension pad definition and HDP oxide deposition followed by etch back defining gate length, (d) after poly-silicon end cap removal, (e) removal of oxide followed by S/D and gate implant (single implant for all three electrodes), (f) final device after metalization. (Reprinted with permission from [15]. [2008] IEEE.)

print remains $8F^2$, the same as planar device. At circuit level, however, lateral nanowire can do little better than planar device as it can allow current matching with stacking of lateral wires, for example, forming two wires out of a Fin [14] and using both as channel for PMOS but only one for NMOS. In contrast, the current matching in vertical devices is possible with gate-length scaling without penalty on foot print. Further, the vertical approach is a route to resolve design and fabrication issues related to lateral nanowires. For example, defining uniform gate is a challenge as the shadowing effects in plasma etching may not allow clearing the gate material beneath the lateral nongated regions. Vertical GAA nanowire transistors are anticipated to be promising candidates as there is no shadowing effect issue and the gate length can be defined by the film deposition and etch back rather than lithography.

2.2. Integration Feasibility. We used GAA vertical nanowire CMOS transistors as test vehicle to develop vertical platform on 8″ silicon wafers [15]. The fabrication process steps of which are illustrated in Figure 2. Shown in Figure 3 are scanning electron microscopy (SEM) images taken as various fabrication stages. Circular resist dots of different diameters (from 160 nm to 600 nm) were patterned using deep ultraviolet (DUV) lithography followed by 1 μm deep Si etch with SF_6 chemistry under resist mask. The etch depth can be tuned depending upon the device design. Si pillars were then oxidized at 1150°C to be converted into nanowires. High temperature was used to decrease the viscosity of grown oxide, ensuring smooth cylindrical Si core at the center of the pillar. The oxidation rate at the bottom of the pillar was low due to increased stress at high curvature [16, 17]. The

Table 1: Benchmarking of lateral and vertical nanowire devices with planar.

	planar	NW (lateral)	NW (vertical)
Device circuit Areas (A)	$8F^2$, $40F^2$	$8F^2$, $24F^2$ Shrink ~40%	$4F^2$, $12F^2$ Shrink ~70%
Speed $\alpha 1/t$ α $(RC)^{-1}$ α $(A)^{-3/2}$	1	~ 2.2×	~ 6.1×
Power α CV^2 α $(A)^1$	1	~ 0.6×	~ 0.3×

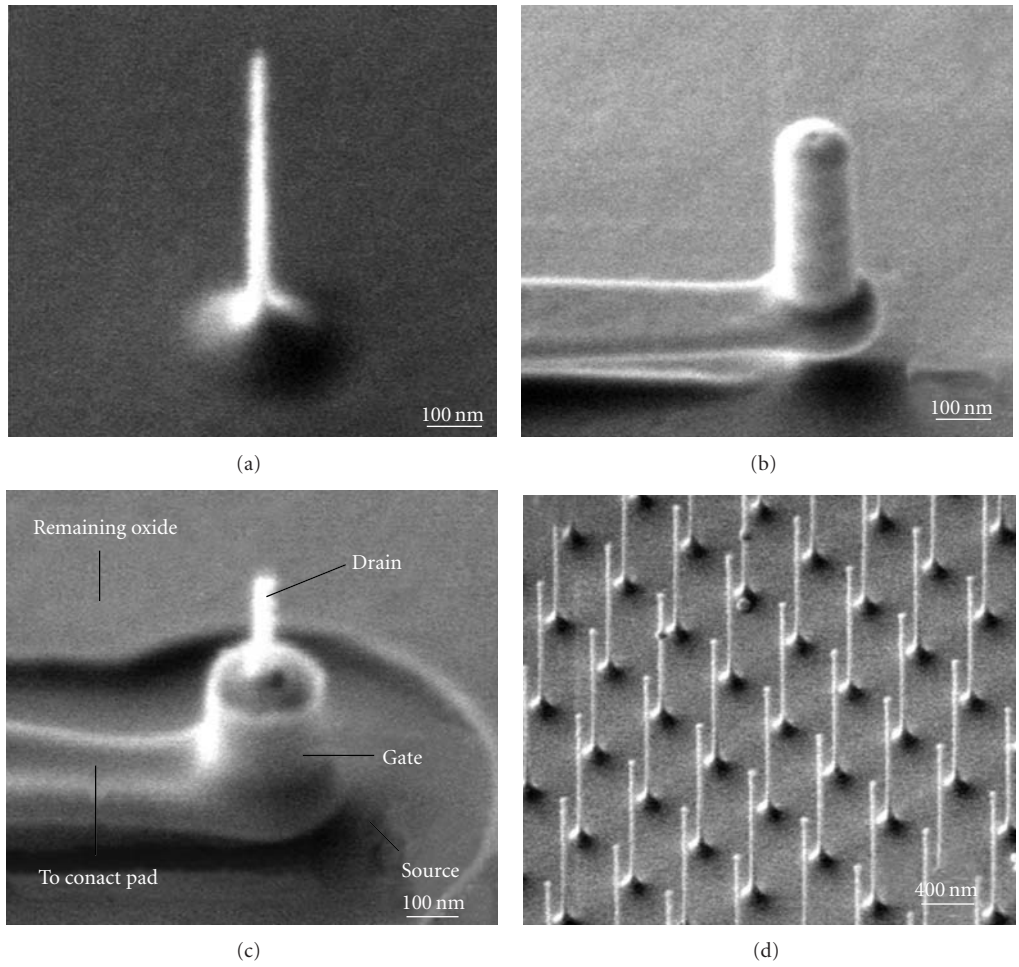


Figure 3: SEM pictures at different stages of device fabrication. (a) Vertical nanowire with diameter ~20 nm; (b) after gate patterning by lithography but before exposing the drain (the tip of the pillar) of the transistor; (c) after the drain (pillar tip) is exposed, ready for taking metal contacts, (d) vertical nanowire arrays with pitch of 500 nm. Nanowires are 1 μm tall with a diameter of ~20 nm. (Reprinted with permission from [15]. [2008] IEEE.)

grown oxide was then stripped in diluted HF (DHF). The SEM images of nanowire thus fabricated are shown in Figures 3(a) and 3(d).

Vertical nanowire formation was followed by a 250 nm thick layer of high density plasma (HDP) oxide deposition and wet etch-back using DHF (1 : 25). The HDP deposition resulted in thicker oxide on the bottom surface and thinner oxide along the nanowire sidewalls due to the nonconformal deposition. After wet etch-back ~150 nm, thick oxide remained to cover the footing of the vertical standing wire. This technique separates the gate electrode from the source extension pad and thus reduces the gate to source fringing capacitance. Gate oxide of ~5 nm was then thermally grown on the exposed wire surface, followed by deposition of 30 nm poly-Si, which serves as the gate electrode (Figure 3(b)). Gate pad was then patterned and etched under resist mask which covers the nanowire and provide a poly extension for gate contact. After gate pad etching, the process of HDP oxide deposition followed by wet etch back was repeated to access the poly on top of nanowire while protecting the gate pad defined earlier. The exposed poly-Si was then isotropically etched by low RF power SF_6 plasma. Alternatively, this cap could be removed in wet Tetramethylammonium Hydroxide (TMAH) solution. The oxide on the wafer was then completely stripped in DHF (Figure 3(c)), and As (1×10^{15} cm^{-2}/10 keV) was implanted four times from four directions, 90 degrees apart, with large tilt angle (45 degree) It was followed by a rapid thermal annealing and standard metallization process.

Figure 4 shows typical characteristics from NMOS of channel diameter ~20 nm and PMOS of channel diameter ~40 nm, both having channel length of 150 nm. The device displayed very good performance with steep turn-on (SS~75 to 100 mV/dec), strong gate electrostatic control (extremely low Drain induced barrier lowering (DIBL) (10 to 50 mV/V)), and high I_{on}/I_{off} ratio (~10^7). However, the threshold voltage V_{th}, with poly-Si gate is much lower than required to integrate these devices into circuits [18–21].

Due to the small channel volume, conventional channel doping proves difficult with nanowires and may result in

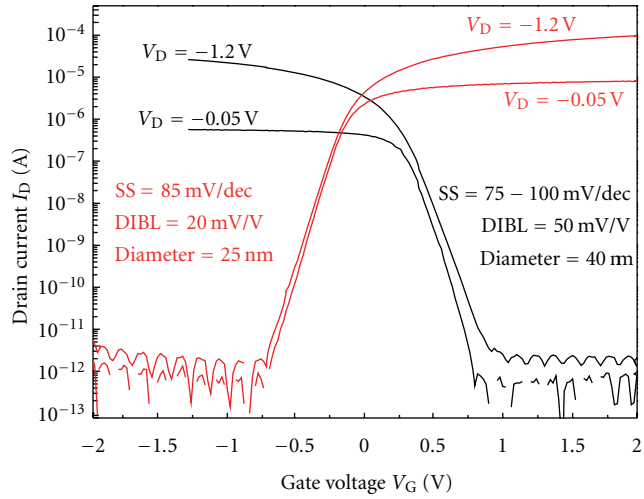
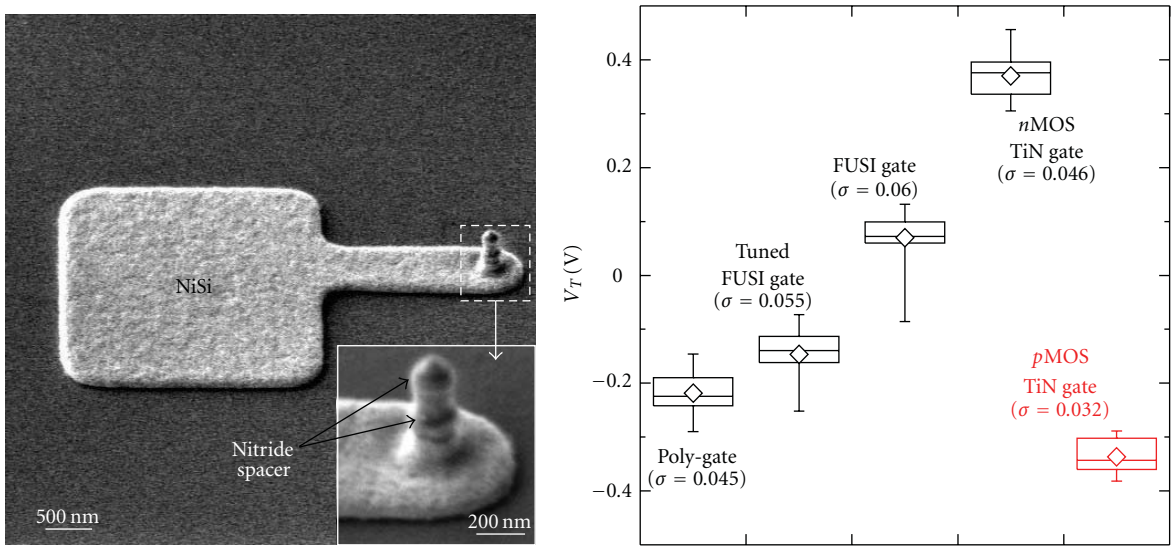


Figure 4: Transfer characteristics of GAA n- and p-FETs showing near ideal subthreshold swing indicating the excellent electrostatic control.



(a) (b)

Figure 5: (a) A scanning electron microscope (SEM) image of an FUSI gate device after silicidation (440°C, 30 s) and removal of unreacted Ni in H_2SO_4:H_2O_2:H_2O solution. (b) Box plots of the V_{th} distribution of measured devices for each split. V_{th} extraction using linear extrapolation was done for over 10 devices in each split.

significant V_{th} fluctuation due to dopant fluctuations in addition to mobility degradation. A better method of V_{th} adjustment is through gate work function tuning. We have implemented NiSi fully silicided (FUSI) and TiN gates, both with undoped nanowire channel. TiN is found to provide better symmetry for N and P devices, however, on the other hand, FUSI gate showed tenability with implant in gate poly-Si. Figure 5 presents SEM image of FUSI gate device and V_{th} values of both the TiN and FUSI gate devices.

The V_{th}-adjusted devices show distinct V_{th} shifts (ΔV_{th}) relative to each other as can be seen in Figure 5(b). The TiN PMOS and poly-gate NMOS have the lowest V_{th} (~ -0.38 V and -0.22 V), followed by the tuned FUSI gate device (~ -0.15 V) and the FUSI gate device ($\sim$0.07 V), while TiN NMOS has the highest V_{th} ($\sim$0.42 V). The TiN gate shows great potential in adjusting V_{th} for vertical SiNW MOSFETs to allow them to be integrated into low standby power circuits.

2.3. Turning MOSFET into Tunneling FET. Scaling of MOSFET to improve device performance and increase device density faces enormous challenges beyond the 22 nm node due to excessive increase in passive power. This arises due to the nonscalability of the SS that limits further reduction in MOSFET threshold voltage, V_{th}, and hence supply voltage, V_{dd}. To overcome this problem and to design more

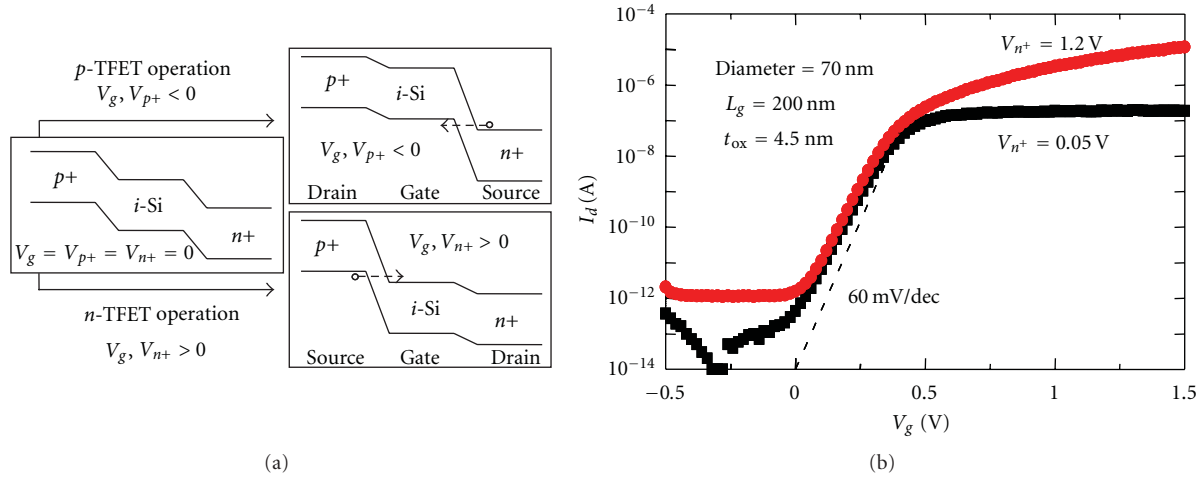


FIGURE 6: (a) Band diagram of TFET showing tunneling junction, (b) I_d-V_g and characteristics of a vertical SiNW TFET with diameter 70 nm, gate length 200 nm and gate oxide thickness 4.5 nm. (Reprinted with permission from [28]. [2009] IEEE.)

energy-efficient devices, alternative transistor designs with low SS are needed. One of such devices is the TFET [22–28]. Unlike the MOSFET, which utilizes thermionic injection of carriers, TFET uses tunneling as the carrier injection mechanism. Therefore, it is possible for TFET to achieve low OFF state current as well as SS below the theoretical limit of 60 mV/decade for MOSFETs at room temperature. TFETs are essentially gated p+ −i −n+ diodes working under reverse bias and can operate as n- or p-TFETs. By controlling the i region with a gate, a tunneling barrier can be created either at the p+ −i (n-TFET, $V_G > 0$) or n+ −i (p-TFET, $V_G < 0$) junctions where carriers are able to tunnel through as shown in Figure 6(a) using band structure [27]. The reverse-biased p–i–n diode gives the TFET the low OFF-state diffusion current.

Leveraging on our vertical nanowire platform, tunneling FETs are fabricated similar to MOSFET using the same mask sets but with opposite type of source/drain doping. We used nitride hard mask to protect the wire top while implanting the bottom electrode. Shown in Figure 6(b) is the n-TFET I_d-V_g curves obtained from a device with diameter ~ 70 nm, gate oxide thickness 4.5 nm, and gate length 200 nm. Excellent I_{on}/I_{off} ratio at $V_{n+} = 1.2$ V is observed (~10^7), with an I_{off} (at $V_g = 0$ V) of ~7 pA/μm and I_{on} (at $V_g = 1.2$ V) of ~53 μA/μm (normalised with the wire circumference). The resulting record high I_{on} and low DIBL (~17 mV/V) for this Si TFET is a result of the excellent gate control of the GAA nanowire structure. However, the obtained SS of 70 mV/dec is beyond the limit of kT/q (≈60 mV/dec), likely due to the tunneling junction ($p + -i$) not being perfectly abrupt.

To achieve SS < KT/q limit, we improve the abruptness of tunneling junction through a novel silicidation induced dopant segregation process [29] depicted in Figure 7. To demonstrate this experimentally, we used nanowires with height of 400 nm and diameter ranging from 30 to 200 nm. Afterwards, the bottom part of the nanowire was vertically implanted with BF_2 for pTFETs and with As for nTFETs to form the drain regions of the TFETs. Isolation and gate stack was formed similar to presented for MOSFET. Then Source was implanted with As for pTFETs and BF_2 for nTFETs and thereafter followed by silicidation, which segregated the dopants to form abrupt source/channel junction. Finally, contact metallization was done.

The transmission electron microscopy (TEM) image showing vertical section of the fabricated p-TFET device is presented in Figure 8.

Figure 9 shows the I_d-V_g characteristics for both pTFET and nTFET, respectively. SS of 30 mV/decade averaged over a decade of drain current is obtained for both pTFET and nTFET devices. Improvement is due to the sharp doping profile at the source side as a result of dopant segregated silicidation, which causes dopants to pile up at the silicide edge [30, 31]. Suppression of ambipolar conduction is also achieved because of natural asymmetry of the vertical nanowire platform, which facilitates independent tuning of source and drain.

SS distribution with drain current is presented in Figure 10(a). SS below 60 mV/decade is achieved for 3 decades of drain current for pTFET and for more than 2 decades in the case of nTFET. The difference in SS behavior of pTFET and nTFET may arise because of the difference in the dopant segregation between As and BF_2 and wafer to wafer process variations. The impact on nanowire diameter on SS is presented in Figure 10(b); SS degrades with the increase of channel diameter. When channel gets wider, the gate electrostatic control on the channel region gets weaker or behaves more like a planar device. Moreover, for larger wires, the encroachment of NiSi into the wire is reduced, therefore, dopant gradient at the source-channel interface is less steep, and hence the SS degrades.

By using higher permittivity (high-κ) gate dielectric and low-bandgap materials at tunneling interface, ON current can be further enhanced [32, 33]. We also noted the difference in ON current between our pTFET and nTFET devices, that is because of the difference in the gate-drain underlap

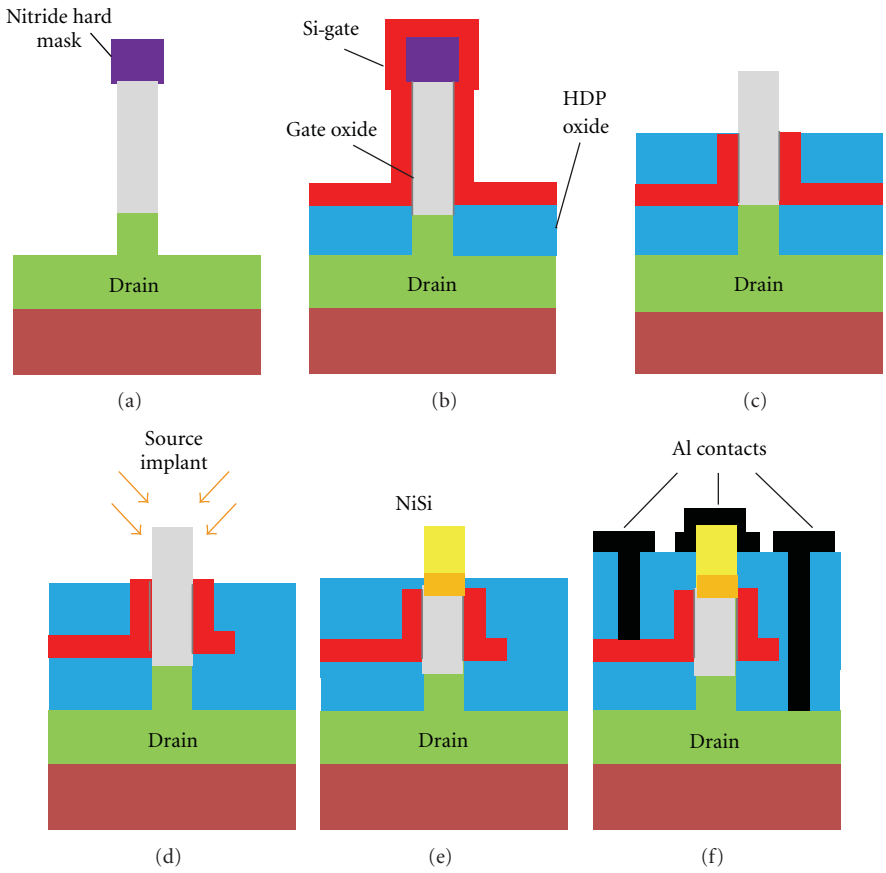


Figure 7: Vertical Silicon nanowire TFET process flow schematic. (a) Vertical pillar etch and As implantation to form the drain region, (b) isolation oxide deposition and gate stack formation, (c) the top amorphous-Si etched to expose source side of TFET, (d) source implanted with BF_2, (e) dopant segregated Ni silicidation, (f) contact opening and Al metallization. (Reprinted with permission from [29] [2011] IEEE.)

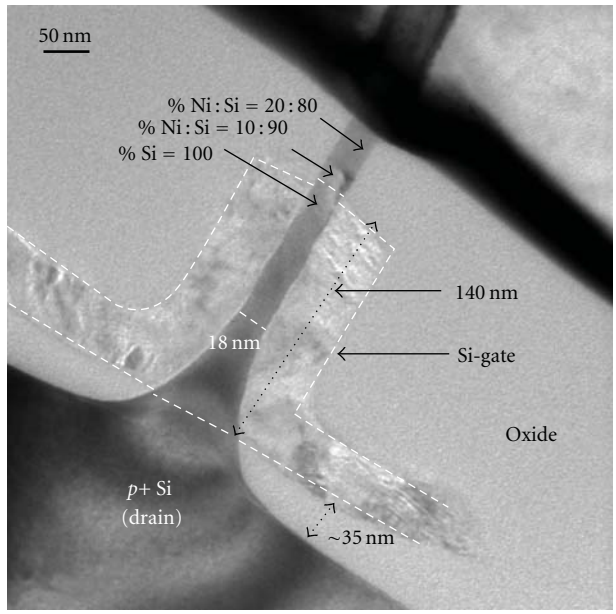


Figure 8: Cross-sectional TEM of pTFET showing a very narrow uniform wire surrounded with gate and silicide at top.

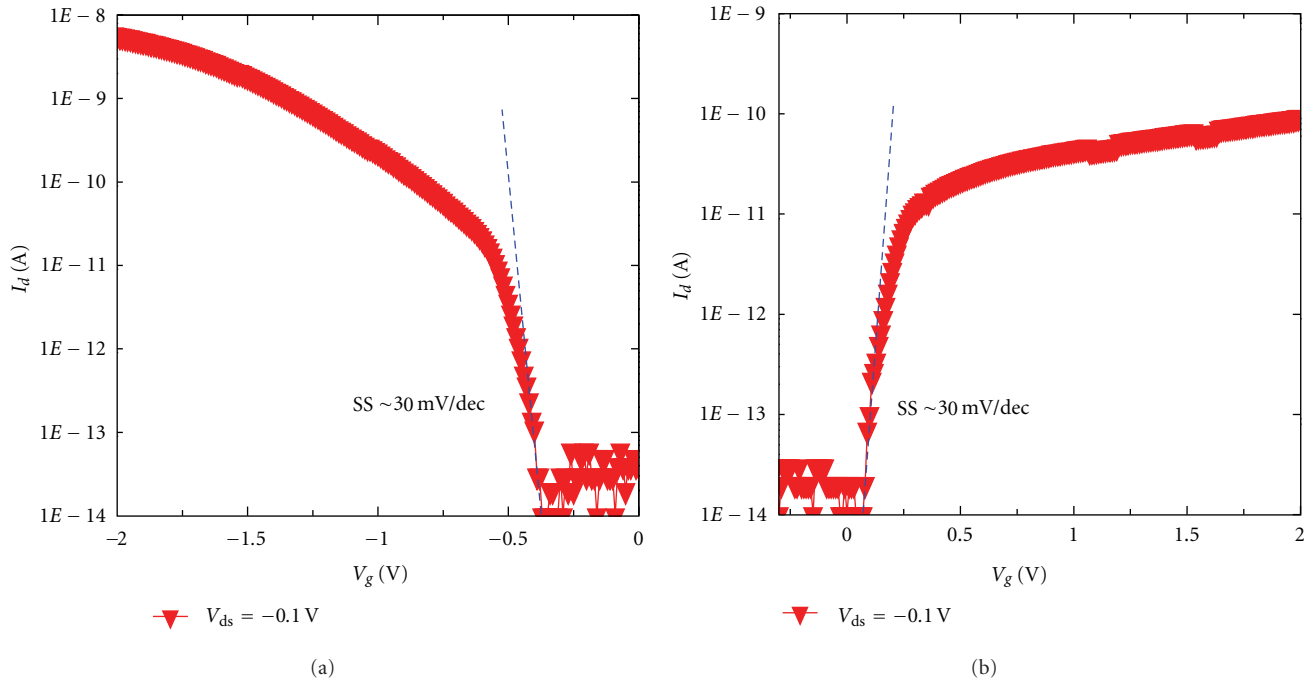


FIGURE 9: (a) Measured I_d-V_g characteristics of (a) p-TFET and (b) n-TFET with SS = 30 mV/decade averaged over a decade.

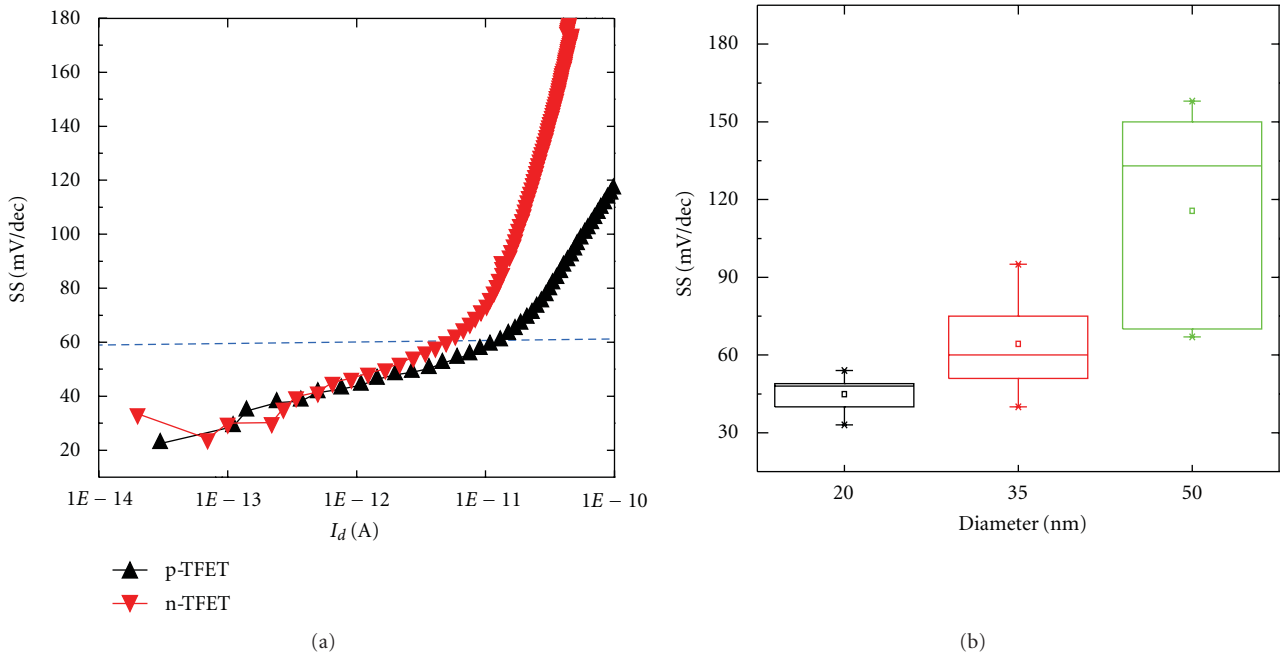


FIGURE 10: (a) SS versus I_d for TFETs. p-TFET exhibits sub-60 mV/decade swing for 3 decades of I_d, while n-TFET maintained sub-60 mV/decade for more than 2 decades of I_d (V_{ds} = 0.1 V). (b) SS variations on nanowire diameter of p-TFETs. SS increases as NW diameter gets wider.

thickness, pTFET has underlap of ~35 nm while nTFET has large underlap of ~100 nm. Large underlap on drain side seems to be one of the reasons suppressing the ON current of nTFET. Optimum gate-drain underlap is required to further suppress ambipolar conduction as well as to maximize ON current.

2.4. Vertical Nanowire-Based Nonvolatile Memory. Market of the nonvolatile memory has been booming persistently due to increasing demand of the portable electronic devices. It is currently dominated by flash memory having poly-silicon floating gate as the charge storage material. The floating gate memory, however, is facing rigorous challenges

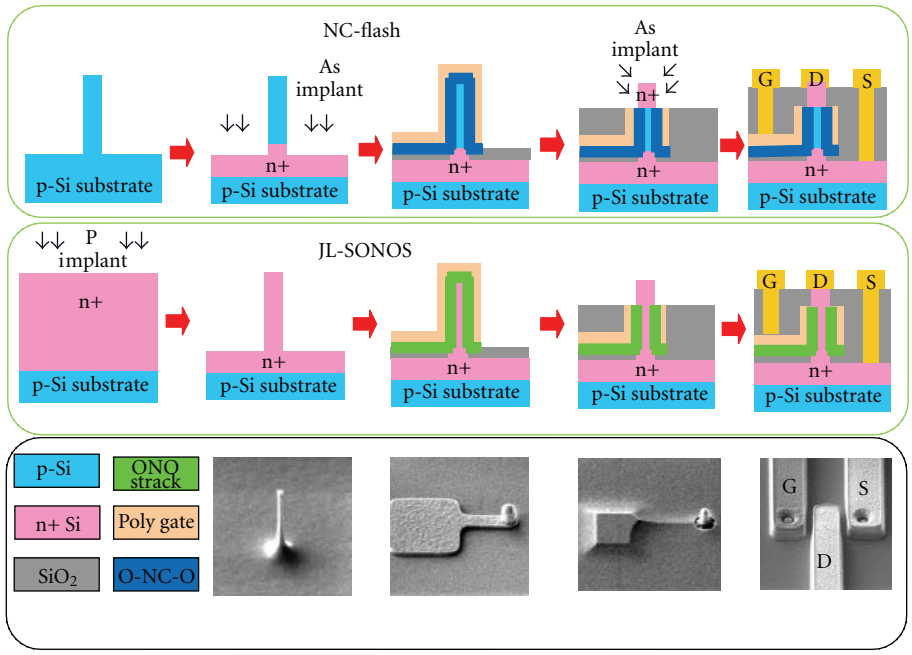


Figure 11: (a) Process integration flow of vertical SiNW junction-based NC-Flash: (a-1) vertical SiNW formation; (a-2) As is implanted to form the source; (a-3) gate stack deposition (O-N-O or O-NC-O for SONOS and NC-flash, resp.) and gate pad definition; (a-4) tip poly and O-NC-O removal, followed by drain implant; (a-5) metallization; (b) process integration flow of vertical JL-SONOS: (b-1) bulk implant and annealing; (b-2) vertical SiNW formation; (b-3) gate stack deposition and gate pad definition; (b-4) tip poly and ONO removal; (b-5) metallization; (c) tilted top view SEM image of SONOS/JL-SONOS fabrication during key process steps (left to right): vertical SiNW formation; gate pad definition; tip poly and ONO removal; metallization. (Reprinted with permission from [45]. [2011] IEEE.)

in the course of scaling beyond the 22 nm technology node because of significantly reduced coupling ratio and increased gate interference [34]. To overcome the scaling issues, the discrete charge trapped devices are being investigated widely. These devices use charge trapping materials such as silicon nitride, high-κ dielectric, and metal/silicon nanocrystals in place of conductive poly-Si floating gate and have simple fabrication process, lower programming voltage, and robust tolerances to defects in the thin tunnel oxide [35–40]. However, in discrete charge trap devices the gate dielectric thickness, for example, oxide-nitride-oxide (ONO) in case of silicon nitride as trap layer, is hard to scale due to the data retention concerns, and therefore it is difficult to avoid concomitant problems of severe short channel effects with scaling.

From transistor structure view point, the cylindrical architecture relaxes the requirement for ultrathin gate oxide and therefore is promising for SONOS-type nonvolatile memory, where thicker tunnel/block oxide is favored for longer retention time [41]. Apart from the superior gate control and electric field enhancement at tunnel oxide to channel interface, observed from the lateral- nanowire-based GAA SONOS cell [42], memory cell fabricated on vertical nanowires platform has more implication due to its small foot print and potential for 3D multilevel integration [43].

In our recent work, we fabricated a gate-all-around (GAA) SONOS flash memory on a vertical Si nanowire (SiNW) of diameter of 20 nm as the channel and presented excellent program/erase (P/E), retention, and endurance characteristics [44]. The performance was further improved by replacing the charge trap layer with silicon nanocrystals (NC). The fabricated cells were an important building-block towards three-dimensional (3D) multilevel integration for ultrahigh density application. Though looks simple, vertical stacking of memory cells could be very challenging in forming junctions on nanowires between the cells. To overcome the junction formation issue, we also designed and fabricated a novel junction-less vertical SiNW-based SONOS cell. Being free of doped junctions, the junction-less (JL) memory device makes vertical SiNW a suitable platform for vertical stacking of memory cells to achieve ultra-high density application. The fabrication steps of our memory cells are sketched in Figure 11 and their detail are available in [45]. Just to highlight here, the JL-SONOS process was started with phosphorus implantation in p-type Si wafer followed by furnace annealing to create a uniform doping profile with different concentrations in the upper portion of the substrates. After that it follows the process flow of conventional junction-based vertical SiNW SONOS to form the wire channel and p-type doped poly-Si gate without S/D implantation, as shown in Figure 11(b). The absence of junctions on wire allows easy stacking of multiple cells on a nanowire.

Shown in Figure 12(a) is a cross-sectional TEM image of a vertical SiNW GAA JL-SONOS with wire diameter equals to 20 nm and gate length of ~120 nm. Figure 12(b) shows the cross-sectional TEM image of the gate stack with ONO thickness 5/7/7 nm. An atomic force microscopy

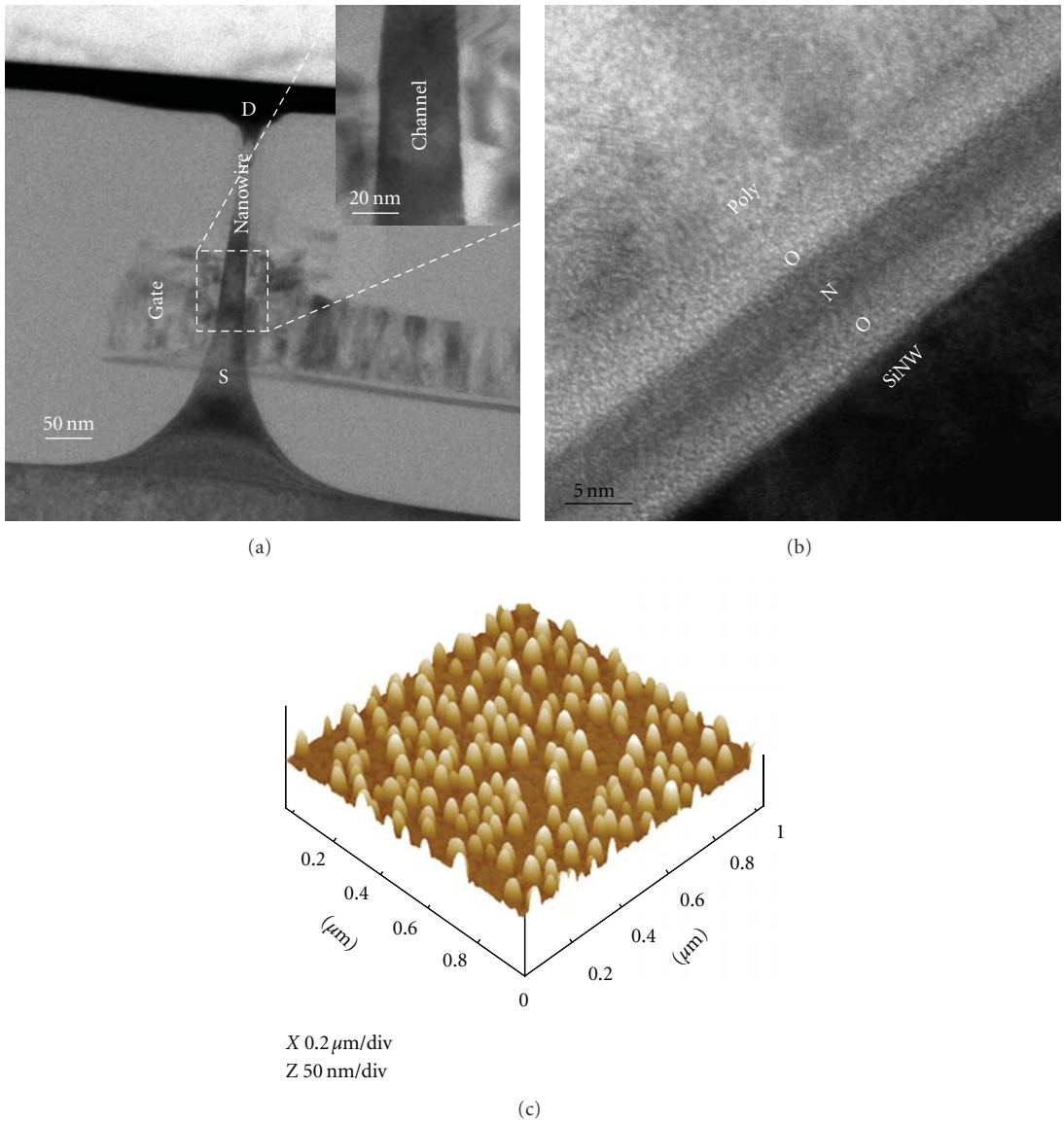
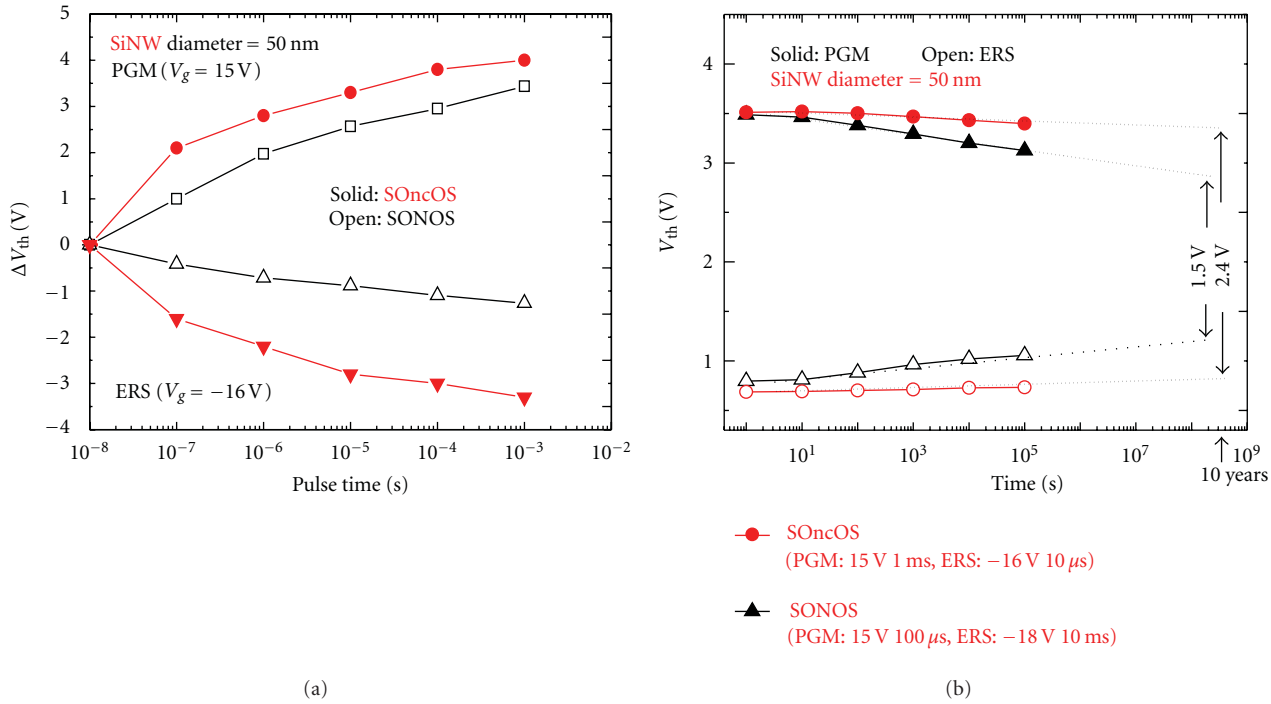


Figure 12: (a) Cross-sectional TEM image of vertical SiNW GAA JL-SONOS: diameter of wire is 20 nm and gate length 120 nm, (b) Cross-sectional TEM image of gate stack showing ONO thickness 5/7/7 nm. (c) AFM image scanned on $1 \times 1\,\mu m^2$ surface area that reveals the formation of Si-NC with a density of $7.5 \times 10^{10}/cm^{-2}$. (Reprinted with permission from [45]. [2011] IEEE.)

(AFM) image over $1\,\mu m \times 1\,\mu m$ area of the nanocrystals deposited on tunnel oxide (in case of NC-flash) is shown in Figure 12(c). It reveals good uniformity and isolation between Si-NCs, although the size is big ($\sim 30 \pm 10$ nm in diameter) and density is low (around $7.5 \times 10^{10}/cm^{-2}$), indicating lot of room for further improvement. The effect of embedding SiNCs as trapping layer is illustrated in Figure 13(a) by comparing the P/E speed of NC-SOncOS with the control SiN-SONOS cell, both on 50 nm thick wire. The NC-SOncOS shows larger ΔV_{th} for the same P/E time period, indicating a better charge storage capability. The results indicate that the trapping centers in devices using silicon nanocrystals as charge trapping medium are superior than that of SiN, which enhances the trapping efficiency of the devices.

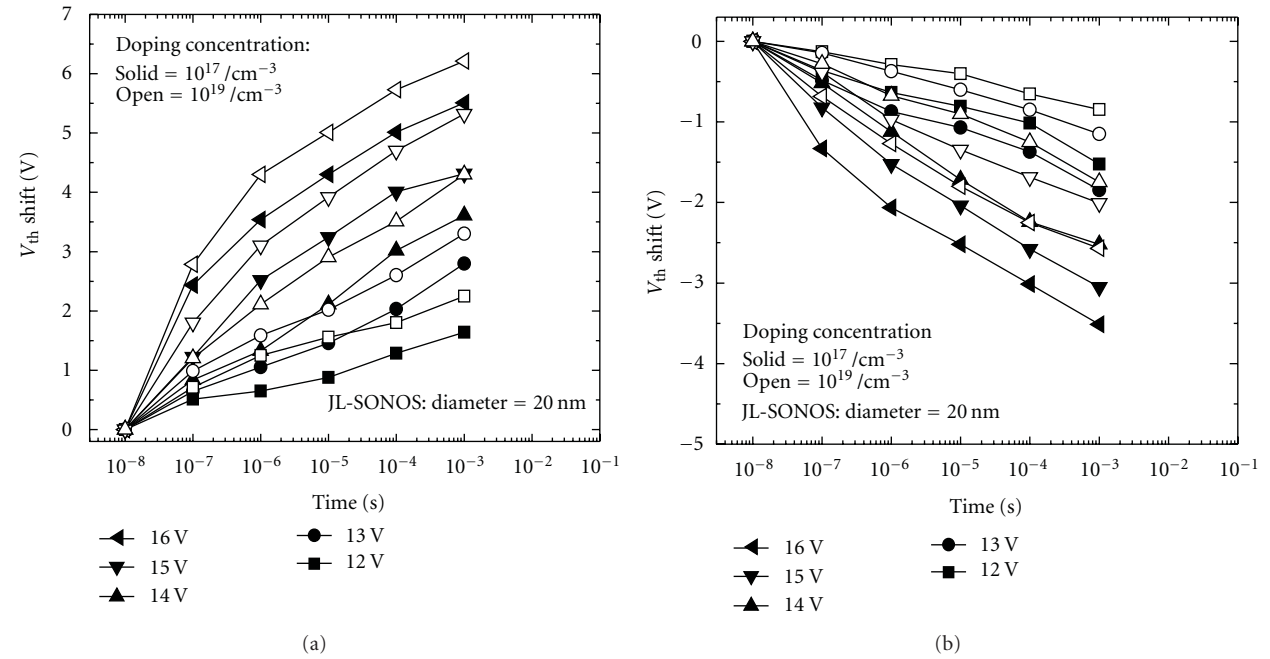
As can be seen in Figure 13(b), a partial window closure ($\sim$30% projected after 10 years) is observed for SiN-SONOS after 10^5 seconds 85°C retention for which the devices were programmed at 15 V for 100 μs and erased at -18 V for 1 ms. Incorporating SiNCs into the trap layer can significantly improve the charge loss by forming isolated energy wells due to conduction band offset [46] between Si and dielectrics. As shown in Figure 13(b), after SiNCs incorporation, the retention characteristics show great improvement and negligible memory loss was observed after 10^5 seconds retention at 85°C. Excellent endurance properties have been obtained for both SiN-SONOS and NC-Flash devices.

The characteristics of junction-less cells are presented next. Figure 14 illustrates the P/E characteristics of JL-SONOS with channel doping of $1 \times 10^{17}\,cm^{-3}$ and



(a) (b)

Figure 13: (a) Comparison of P/E speed between vertical SiNW-based NC-SOncOS and SiN-SONOS, with gate length of 150 nm and wire diameter of 50 nm. (b) Retention characteristics at 85°C for vertical SiNW-based GAA SONOS and NC-SOncOS. (Reprinted with permission from [45]. [2011] IEEE.)



(a) (b)

Figure 14: (a) Programming and (b) erasing characteristics using FN tunneling of vertical SiNW-based GAA JL-SONOS memory device with channel doping of 1×10^{17} cm^{-3} and 1×10^{19} cm^{-3}. (Reprinted with permission from [45]. [2011] IEEE.)

1×10^{19} cm^{-3}, respectively, for a fixed wire diameter of 20 nm. For both the doping concentrations, the memory window is nearly same, more precisely, 3.2 V for low doped (1×10^{17} cm^{-3}) and 2.7 V for moderately doped (1×10^{19} cm^{-3}), when a P/E time of 1 ms was used at +15 V/−16 V, respectively.

Shown in Figure 15 is the feasibility on the multibit programming for the JL-SONOS measured on cell with

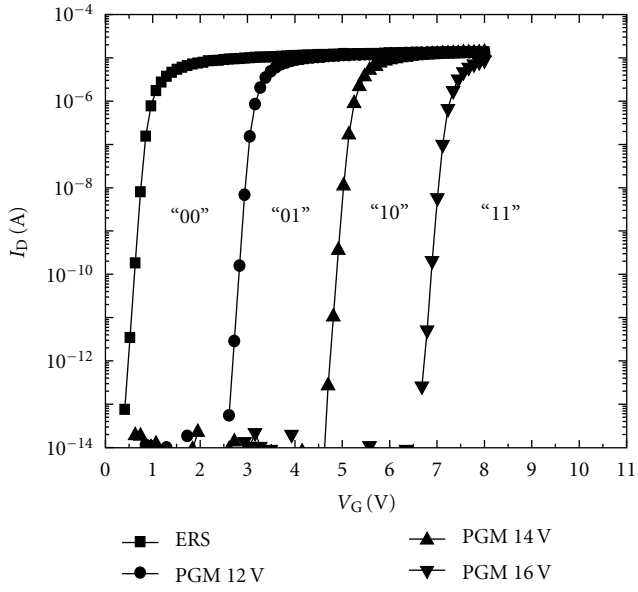


FIGURE 15: Multibit programming characteristics of JL-SONOS memory with a gate biases of 12, 14, and 16 V for 1 ms. Wire diameter = 20 nm, channel doping = $1 \times 10^{19}/\text{cm}^{-3}$. (Reprinted with permission from [45]. [2011] IEEE.)

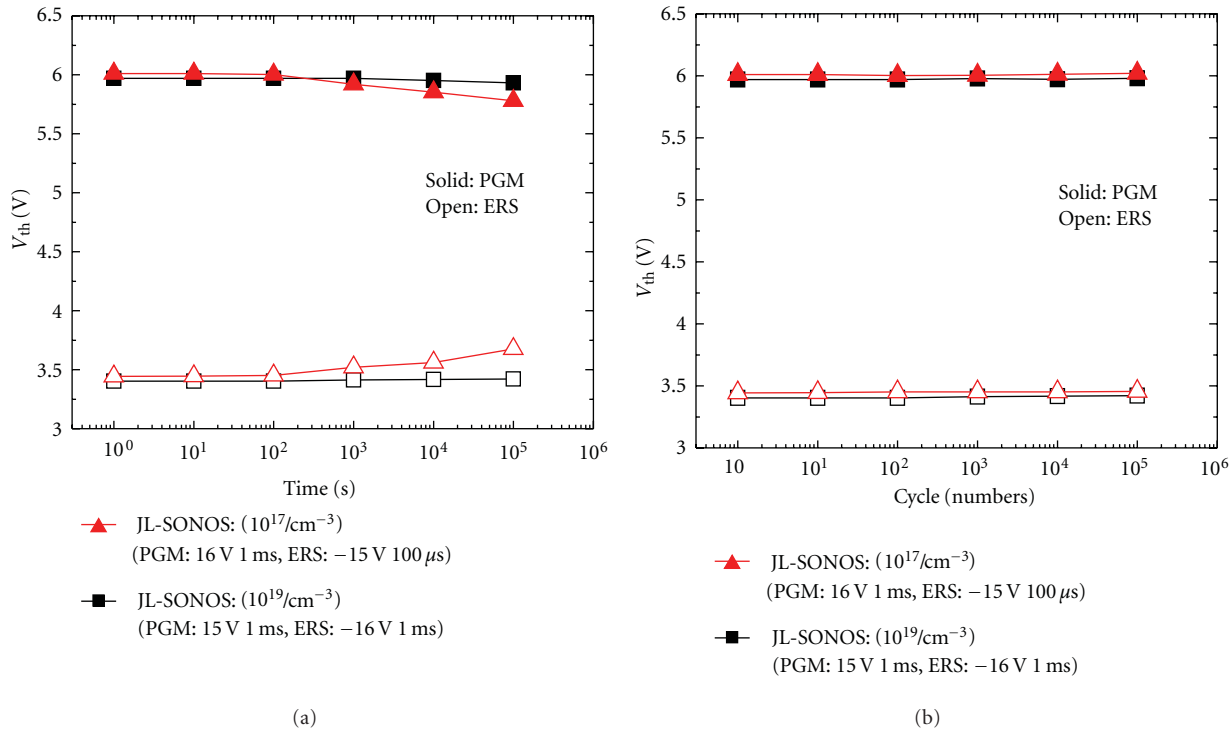


FIGURE 16: (a) Retention characteristic at 85°C for JL-SONOS memory device with channel doping of 1×10^{17} cm^{-3}.and 1×10^{19} cm^{-3}. (b) Endurance characteristic at 85°C for JL-SONOS memory device with channel doping of 1×10^{17} cm^{-3}.and 1×10^{19} cm^{-3}. (Reprinted with permission from [45]. [2011] IEEE.)

doping 1×10^{19} cm^{-3}. As obvious from the figure, the memory cell is able to store 2 bits per cell using four states "00", "01", "10", and "11" with each state defined a different V_{th} of >1 V.

The high temperature retention characteristic at 85°C for JL-SONOS is shown in Figure 16(a). The JL-SONOS with high channel doping (1×10^{19} cm^{-3}) exhibits less V_{th} degradation as compared to lightly doped JL-SONOS (1×10^{17} cm^{-3}), and its memory window can be well maintained up to 10^5 sec. Under retention conditions, direct trap-to-band (TB) tunneling from a nitride traps to the channel conduction band is the main discharge mechanism. With

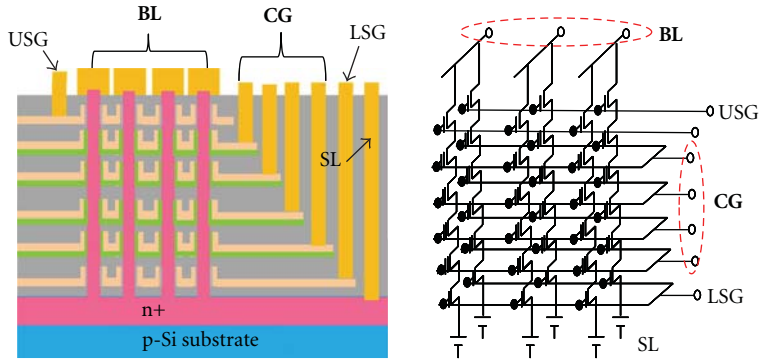


Figure 17: Schematic of 3D multilevel stacked NAND using JL-SONOS as building blocks.

increased channel doping, the energy states close to the channel conduction band are more likely to be occupied by electrons. This reduces the probability of further electron injection from the trap layer, and thus more reliable charge storage can be expected [47]. The endurance characteristic of JL-SONOS is shown Figure 16(b), in which all devices can maintain the P/E window after 10^5 cycles at 85°C.

A possible 3D memory cell circuit design based on vertical SiNW JL-SONOS is illustrated in Figure 17. Without using junction for both selection gate transistors and memory cell, the integration process would be significantly simplified.

3. Clean Energy

3.1. Vertical Nanowire-Based Solar Cell. Si thin film solar cell is considered for the next generation of solar cell as it provides a viable pathway towards low material and production cost [48]. Nonetheless, the thickness of Si thin film is much lower than the optical thickness to absorb 90% or more of the above-band-gap-photons [49], limiting the total power conversion efficiency (PCE). One of the possible approaches to enhance the light absorption is the integration of Si nanostructure on thin film. In addition to many other optical phenomenons, diffraction of light plays a key role with nanostructured surface making poorly absorbed red light to enter at higher angle into the film, thus improving the chances of absorption. Although, the exploitation of Si nanowire or nanopillar (SiNP) in solar cell application [49–53] has been widely studied over the past decade due to its excellent optical [53–56] and electrical properties [49, 52], there was not much systematic analysis that could guide design of high efficiency solar cells. Our group did a very through simulation-based study [7] and followed that by experimental verification [8]. We found the optimized pillar diameter (D) is 0.20 μm, at diameter/periodicity (D/P) ratio of 0.5 (i.e., periodicity 0.4 μm) and height (H) 1 μm [7, 56], the SEM image of which is shown in Figure 18(a).

We comprehensively study the electrical characteristics of the optically optimized structure for both the axial and radial p-n junctions using simulations. Our simulations incorporate optical properties of the device studied by using 3D Finite Element Method (FEM). The light is assumed to be incident normally to the SiNP array, under AM 1.5 G 100 mW cm^{-2} spectrum. The electric field ($\vec{E}$) at each coordinate of the 3D simulation grid is calculated and exported to the Cogenda Genius Simulation Manager [57] for electrical solving the current continuity equation and Poisson's equation self-consistently. The calculations of the current-voltage (J-V) characteristic of the SiNP solar cell follow the description in [58]. Drift-diffusion model is implemented for carrier transport within the device. Shockly-Reed-Hall (SRH) and Auger recombination are also taken into consideration.

We discuss only axial junction (device in Figure 18(b)) here. Shown in Figure 19(a) is the effect of minority carrier diffusion length on short circuit current I_{sc} and open circuit voltage V_{oc}. Inset shows the PCE comparison with planar reference device. It can be observed that a diffusion length as poor as 0.6 μm is tolerable with our design, showing the possibility of exploitation of low-grade Si in photovoltaic application to lower the production cost [59]. Indeed a PCE of 17.4%, assuming surface recombination velocity "S" = 0 cm-s^{-1}, is predicted with small minority carrier diffusion length for electron ($L_n \geq 0.6\,\mu$m). Figure 19(b) shows the photo-generated carrier concentration with a clear concentration effect inside the wire. Designing the junction location inside this highly concentrated area is the key of getting high performance. Further, it is worth mentioning that though bulk recombination is lowered in thin film solar cell, and the Auger and surface recombination may increase due to higher carrier densities near the surface. It would have a negative impact on the short circuit current density (J_{sc}) and open circuit voltage (V_{oc}) [60], especially for nanopillar solar cell due to the increased surface area and absorption near the surface. We found a decrease in PCE from 17.4% to 15.5% with S increased from 0 cm-s^{-1} to 1000 cm-s^{-1}, indicating its detrimental impact [7].

Next we present our experimental results of axial junction nanopillar solar cells, the fabrication details of which are available in [8]. Owing to the significantly enhanced light absorption of the optimized SiNP array texturing,

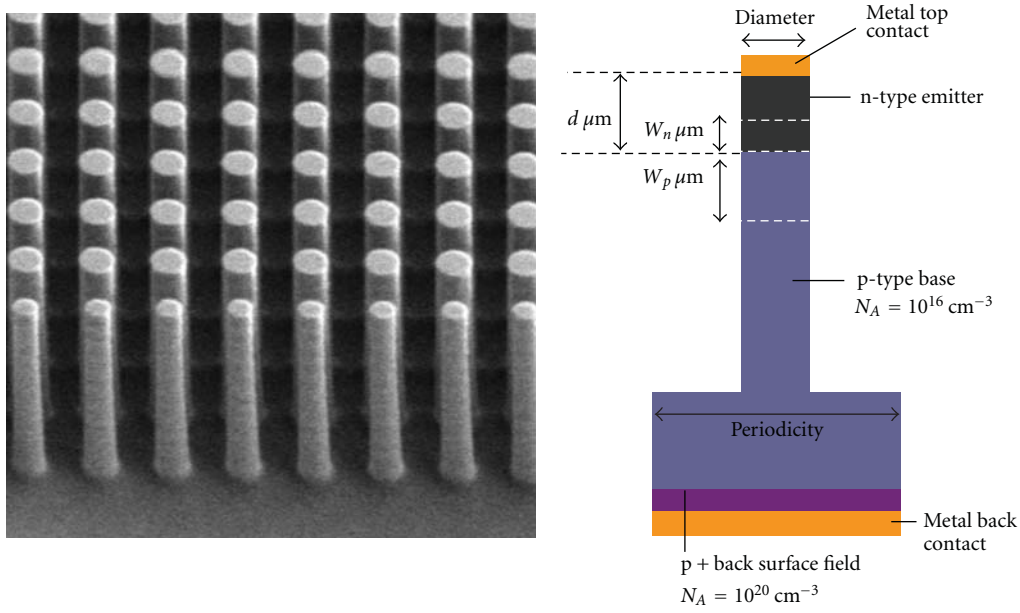


FIGURE 18: (a) SEM image of a Si nanopillar pattern used for simulating PCE analysis. Pillar parameters are diameter = 200 nm, pitch = 400 nm, and height = 1000 nm; (b) crossectional schematic of axial junction. (Reprinted with permission from [8]. [2010] IEEE.)

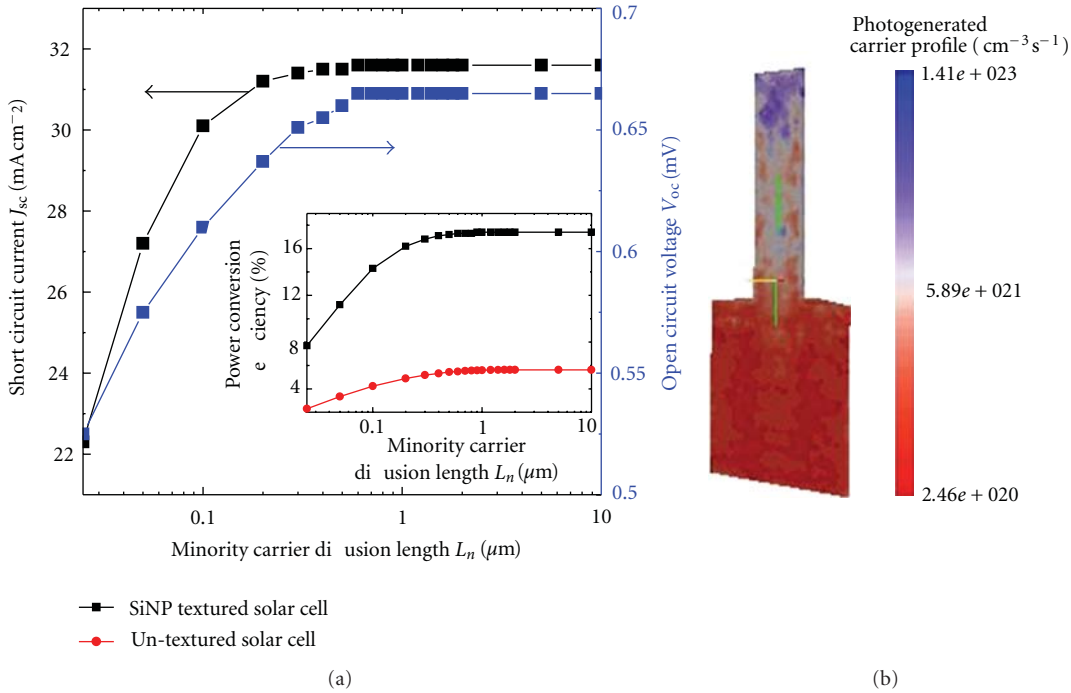


FIGURE 19: (a) Short circuit current and open circuit voltage of the SiNP textured solar cell at various L_n. Inset is the efficiency of the SiNP textured and untextured solar cell; (b) photo-generated carrier profile G in a Si nanopillar textured thin film solar cell at $L_n = 0.6\,\mu$m. (Reprinted with permission from [59]. [2010] IEEE.)

a short circuit current density (J_{sc}) of 34.3 mA/cm^2 is realized on axial p-n junction inside SiNP surface textured solar cell, which is the highest to date among reported Si nanowire (SiNW)/SiNP-based solar cells. This is in distinct comparison to J_{sc} of 18.1 mA/cm^2 demonstrated on the solar cell without SiNP.

Shown in Figures 20(a) and 20(b) are the microscope images of the nanopillar-based and planar solar cells,

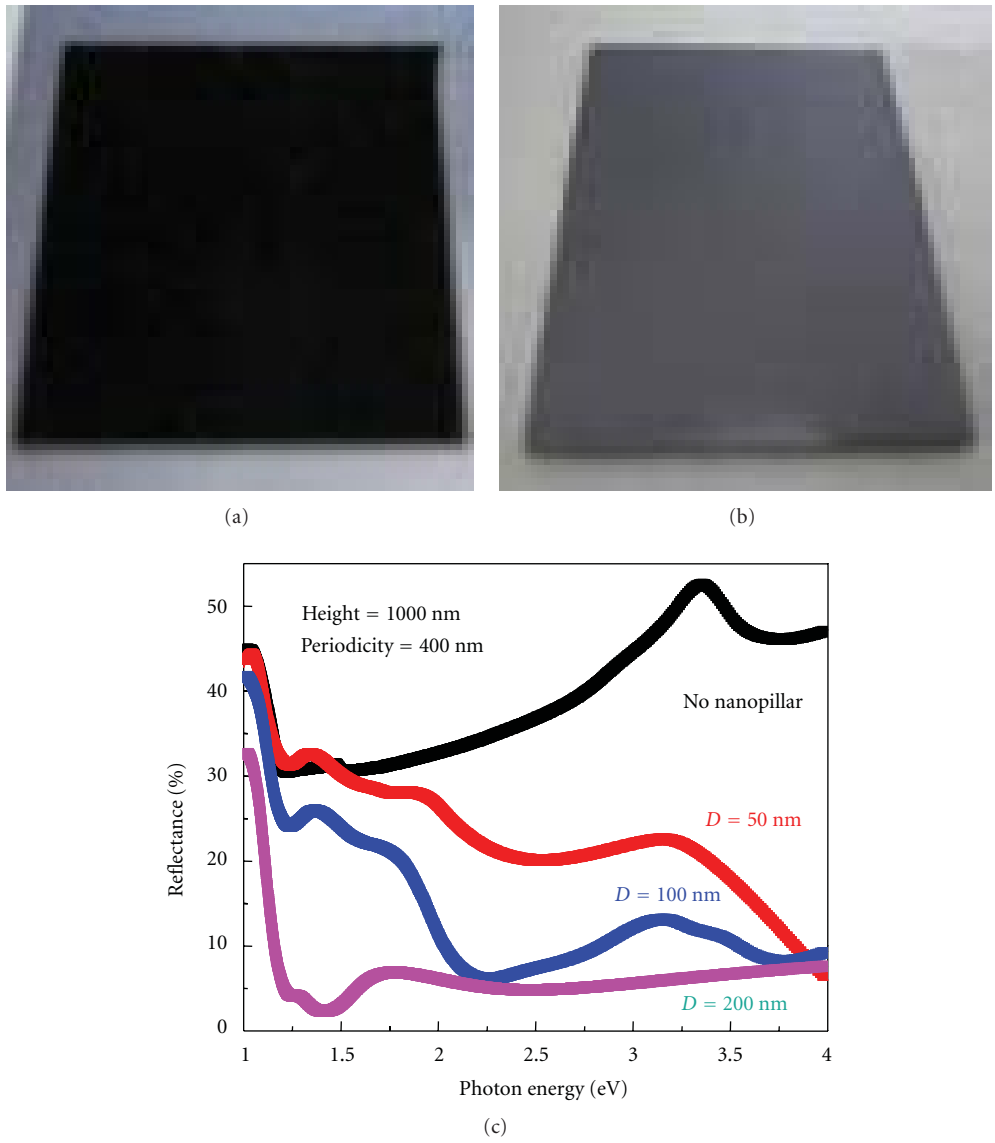


Figure 20: Photographs of (a) SiNP textured and (b) untextured solar cell (without top TCO layer). (c) Reflectance spectra with varying parameters. (Reprinted with permission from [8]. [2010] IEEE.)

respectively. It is clearly observed that the textured solar cell appears darker than the untextured one due to its superb antireflection properties. In align with our previous theoretical prediction, the lowest reflection is achieved when the SiNP diameter is 200 nm as shown in Figure 20(c) (e.g., D/P is 0.5) [7, 56].

The external quantum efficiency (EQE) was measured to investigate efficiency of the light absorption and carrier separation/carrier collection for the device (Figure 21). The doping concentration of the emitter (with junction depth of 250 nm) and back surface is 10^{20} cm^{-3}, and the doping level of base is 10^{16} cm^{-3} in the devices. The illuminated condition is AM 1.5G, that is, 100 mW cm^{-2}. Figure 21 depicts the EQE in the main energy range of solar spectrum as a function of SiNP diameter. The EQE of SiNP array textured devices is much higher than that of untextured one, indicating that the photons are more efficiently absorbed. The device textured by the SiNP array with D of 200 nm (or D/P of 0.5) and H of 1000 nm has the best EQE (>200% of the untextured one), implying the excellent light trapping and carrier extraction capability for the sample with optimized surface texturing. The results are also well matched with the aforementioned reflection measurement and simulation result [7].

The short circuit current "J_{sc}" measured under AM 1.5 G 100 mW cm^{-2} illumination for nanopillar devices with various diameter is shown in Figure 22(a) along with simulated current-voltage graphs in Figure 22(b). The measured J_{sc} increases with increasing D/P ratio, and the trend is in good agreement with the simulation results and EQE data.

The J_{sc} of SiNP surface textured device is boosted to a maximum of ~31.4 mA/cm^2 with pillar D of 200 nm, which is ~1.7 times larger than that of the untextured device

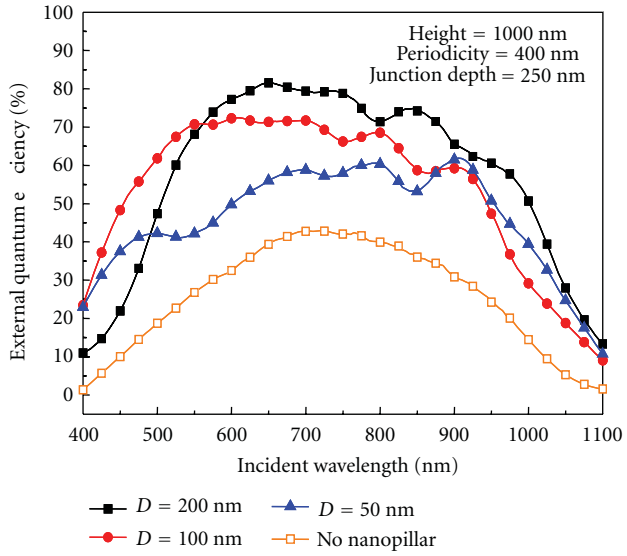


FIGURE 21: External quantum efficiency for various pillar diameter showing best result for 200 nm pillar diameter under AM 1.5 G 100 mWcm^{-2} illumination. (Reprinted with permission from [8]. [2010] IEEE.)

(18.1 mA/cm^2). To the best of our knowledge, the device in our work achieved the highest J_{sc} using the nanopillar p-n junction.

In brief, nanowires are shown to have high potential for improving solar cell performance through improvement in reflection /absorption behaviour. With proper design, poor quality silicon is shown to be acceptable and does not deteriorate performance till diffusion length is as low as 0.6 μm. High short circuit current is demonstrated experimentally with an improvement of 1.7× in comparison to planar cell.

3.2. Vertical Nanowire-Based Thermoelectric Cooling/Thermoelectric Generation. With the aggravation in the high heat flux fields like 3D electronics, implantable bioanalytical devices, and semiconductor lasers, the thermal map of general electronics has become extremely uneven and detrimental to the devices' performance [61]. Besides a growing need to cool down the local hot spots generated, there is an even more attractive opportunity to harvest the surplus heat. However, chip level harvesting has not been feasible due to the low thermoelectric conversion efficiency of current bulk materials and also due to a lack of proper CMOS compatible material.

The basic principles of thermoelectric cooling/thermoelectric generation (TEC/TEG) are based on Peltier or Seebeck effects where all electric current is accompanied by heat current and vice versa. A thermoelectric device can alternate between being a power generator via heat to electrical current conversion or a cooler via electrical current carrying away the heat [62]. The efficiency of the thermoelectric modules is dictated by the dimensionless figure-of-merit ZT, that is, $S^2\sigma T/\kappa$, where S, σ, k, T, are Seebeck coefficient, electrical conductivity, thermal conductivity, and absolute temperature, respectively. Commercial state-of-art thermoelectric materials-alloys of Bi, Te, Sb, and Se have ZT ≥ 1 at room temperature [62]. However, these materials are difficult to handle and process like silicon technology, which is widely used in the semiconductor industry. Although thermoelectric materials have their performance limited in their bulk form, their low-dimensional nanostructures seem to outperform expectations [63]. Silicon, which was never considered for thermoelectric applications in its bulk form, has become a potential contender at the nanoscale. Studies show that the thermal conductivity of a 50 nm wide SiNW is reduced by 2 orders (to a k of 1.6 W/mK) resulting in an improvement in the ZT value to 1 from the bulk material of 0.01. The tremendous reduction of κ is attributed to the effect of phonon boundary scattering at nanoscale [64–69]. This significant discovery opens up a window for chip-level thermoelectric energy harvesting with potential to be integrated into conventional electronic circuitry. With Silicon as the TEG material, the use of Bi_2Te_3-based materials can be avoided.

We recently reported a top-down CMOS compatible integration technology for SiNW-based TEG [70], the schematic flow of which along with SEM images is shown in Figure 23. The P and N SiNW elements are connected at the top by Aluminum and at the bottom through metal-silicide formed by selective silicidation. This SiNW-based TEG is highly scalable and appropriate for chip level cooling and power generation due to the ease of integration with other CMOS ICs.The microscope image of the completed device is shown in Figure 24(a) with stack details during measurement in Figure 24(b). It had a total surface area of 5 mm × 5 mm (60% filled with doped wires) and consisted of 162 thermocouples.

The power generation of the device was characterized by heating one side using a copper heater designed and fabricated on separate wafer and attached to device under test. The heater die also had temperature measurement devices. Shown in Figure 25(a) is the open circuit voltage, V_{oc} across the TEG with different temperatures generated across the device "dT". As expected, an increase in V_{oc} is observed with an increase in dT. A V_{oc} of 1.5 mV was measured under an overall applied dT of 70 K across the whole experimental setup (0.12 K across the SiNW). A linear relationship across all data points is due to S = dV/dT relationship. With the thermal resistance values presented in Figure 24(b) and using S = dV/(NdT) on the largest V_{oc} measured across setup (dT = 70 K), the effective Seebeck coefficient of the TEG was extracted to be 39 μV/K. The extracted value is lower than reported SiNW value at comparable doping level [64]. However, it can be pointed out that each layer in the experimental setup has its own interfacial thermal resistances which will lower significantly the actual dT across the TEG. As it is a first demonstration, there is a room to improve interfacial thermal resistances and thus improve the dT across the nanowire. Indeed, the idea of an ultrathin thermoelectric device is envisioned to be directly integrated onto chips for direct energy harvesting. In this way, the interfacial thermal resistance associated with the experimental setup can be eliminated. Hence, the effective dT across the SiNW can

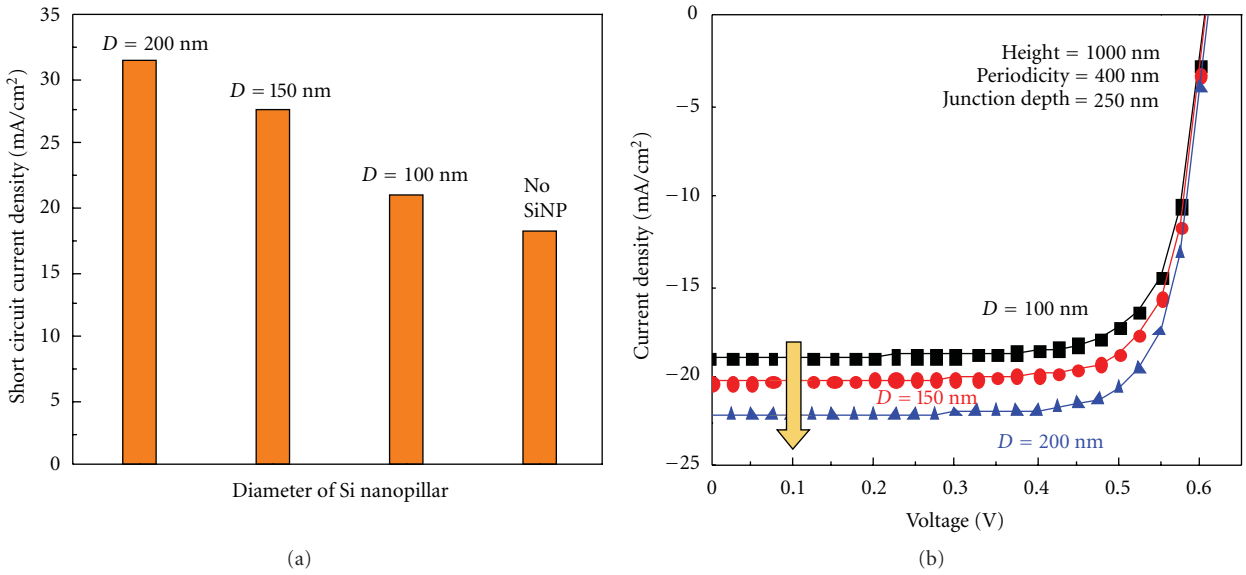


FIGURE 22: (a) Measured J_{sc} as a function of Si nanopillar diameter under AM 1.5 G 100 mWcm^{-2} illumination (b) Simulated J-V characteristic of Si nanopillar thin film solar cell (with underlying Si thin film of ~800 nm). (Reprinted with permission from [8]. [2010] IEEE.)

be increased. In Figure 25(b), the generated voltage/power is plotted as a function of current at a total dT of 70 K across the experimental setup. A maximum power output of 1.5 nW is realized under a voltage and current of 0.75 mV and 2 μA, respectively. In our device, if we could extend the dT across the wire to 1 K, a power density of 1.2 μW/cm^2 can be harvested. However, the ability to maintain a large dT across the SiNW to generate a larger power is another important aspect that needs to be considered and optimized.

In brief, SiNW TEG was fabricated using CMOS compatible top-down processes. Seebeck effect was demonstrated and power generation was measured. With further improvements in top metallization and low thermal conductivity material filling between nanowires, such as polyimide, excellent nanoscale thermoelectric energy harvesters can be realized. Such SiNW TEG can be cost-effective, scalable and possibly easier to be integrated. By potential integration of these TEG beneath (wafer backside) traditional high heat flux circuitry, these nanoscaled generators can provide location specific thermal harvesting and pave way to ultra low powered IC's and self-powered circuits.

4. Challenges and Opportunities

There has been significant progress in fabrication technology and in understanding of the electrostatics and transport in the GAA nanowire devices; huge challenges remain to be met before this new device architecture reaches the level of manufacturing. The first challenge is large device parameter variability in the threshold voltage and I_{on} as reported in [10]. This variability is mainly attributed to possible variation of nanowire shape, size/diameter, roughness and variation in interface quality. Tight control of the starting pillar dimensions with advanced lithography and surface smoothing using H_2 annealing [71] may help in reducing this variation. Indeed, being controlled from all sides the sensitivity of device parameters to nanowire diameter, which is defined by lithography and generally has ±5% variation, is large. Poor lithographic process window for pillar pattern is one the main contribution of critical dimension variation across the wafer. However, one of the solutions for this problem is the change of pattern polarity using hard mask scheme. Use of variability-specific designs, such as eight transistor SRAM [72] or probabilistic circuit design techniques, such as neuromorphic designs [73], could form part of the solution for successful implementation of GAA nanowire devices into manufacturable circuits.

The second challenge pertains to the tuning of the threshold voltage. Due to very limited volume of channel body, the doping of the channel for V_{th} adjustment is not feasible. Due to cylindrical architecture, the impact of gate oxide thickness on V_{th} is also expected to be significantly diminished. The feasible solutions lie only with the tuning of the gate electrode work function and the wire diameters.

The third challenge, specific to vertical nanowire devices, is inherent asymmetry between source and drain resistance, and also in channel diameter if profile is not controlled well. These asymmetries have to be taken care of in circuit designs and therefore provide an opportunity to designers to come up with novel design solutions. Further, the vertical wire is shown as natural platform for TFET; the challenge with circuit design which could be huge as TFET will not work as pass transistor in both directions. Designing hybrid circuits with MOSFETS and TFETS could be one of the solutions to resolve this issue.

The issues which are a challenge in electronics domain have either little or no impact on energy harvesting or could even be favorable. For example, critical dimension

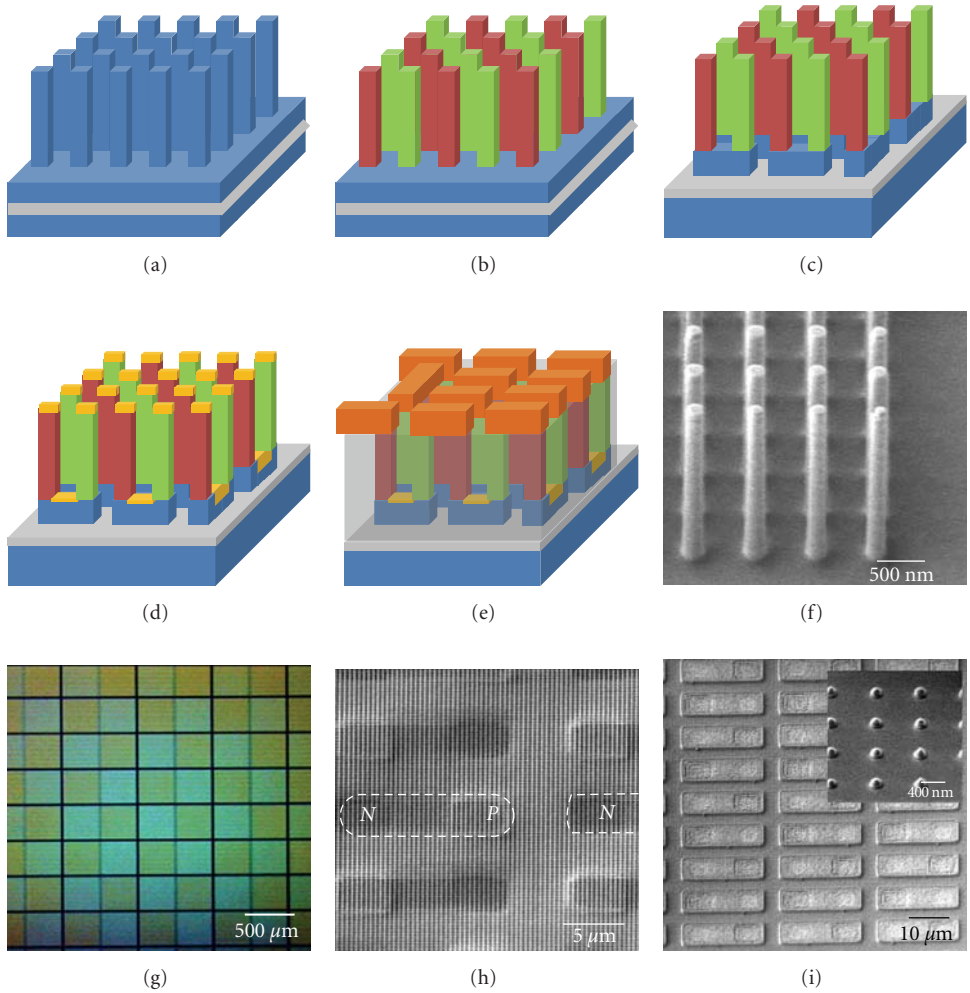
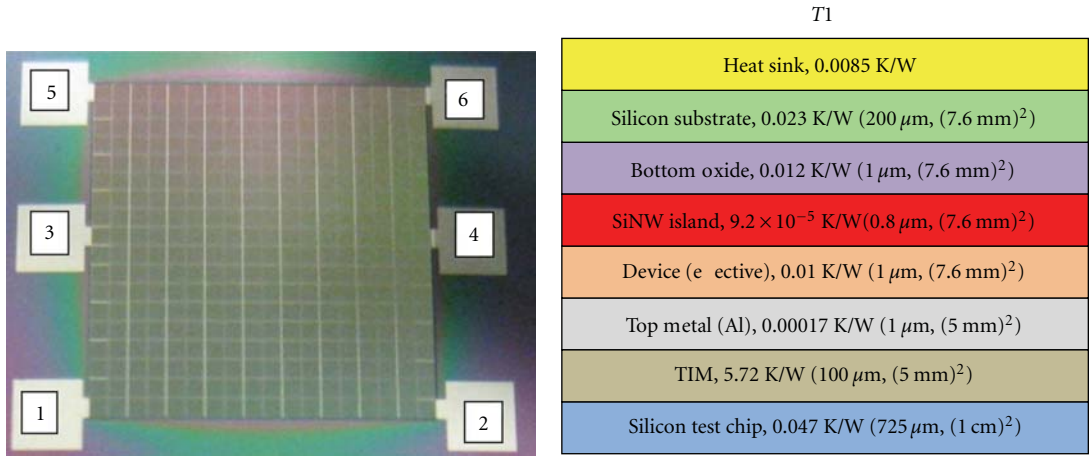


Figure 23: Schematic of fabrication (a) SiNW formation by dry etch, (b) Ion implantation, P/N elements definition, each element consists of hundreds of SiNW, (c) P/N couples formed by dry etch, (d) SiNW top and bottom silicidation while protecting the sidewall, (e) dielectric deposition and etch back to expose only the tip of the SiNW, and Top metallization. (f) SEM images of pillar formation, (g) N & P implants can be seen clearly under microscope with a different shade, (h) SEM image of SiNW after N/P implant, and (i) metallization etch showing individual N/P couples. Inset shows the tips of the SiNW exposing after oxide etch which confirms structure of the TEG. (h) and (i) are images of test structures, the actual design is too large to be shown in SEM image. (Reprinted with permission from [70]. [2011] IEEE.)

variation should not impact on solar efficiency, and thermoelectric power generation is expected to improve with surface roughness as a result of decreased thermal conductivity [64, 65]. Though not reviewed in this paper, the use of nanowires in Li ion batteries as anode is another high potential application where none of the issues described above will have any impact [9]. Nanowires also provide opportunity of cointegrating various types of devices either from functionality or performance perspective or for the both on silicon platform. For example, Si/III-V and Ge wires co-integration can provide high performance electronics with NMOS on Si/III-V and PMOS on Ge wire. Worth mentioning here that such hetero-integration may be limited to bottom up technologies as top down would require wafer level selective epitaxial deposition of these materials on silicon which has been a challenge for long due to lattice missmatch.

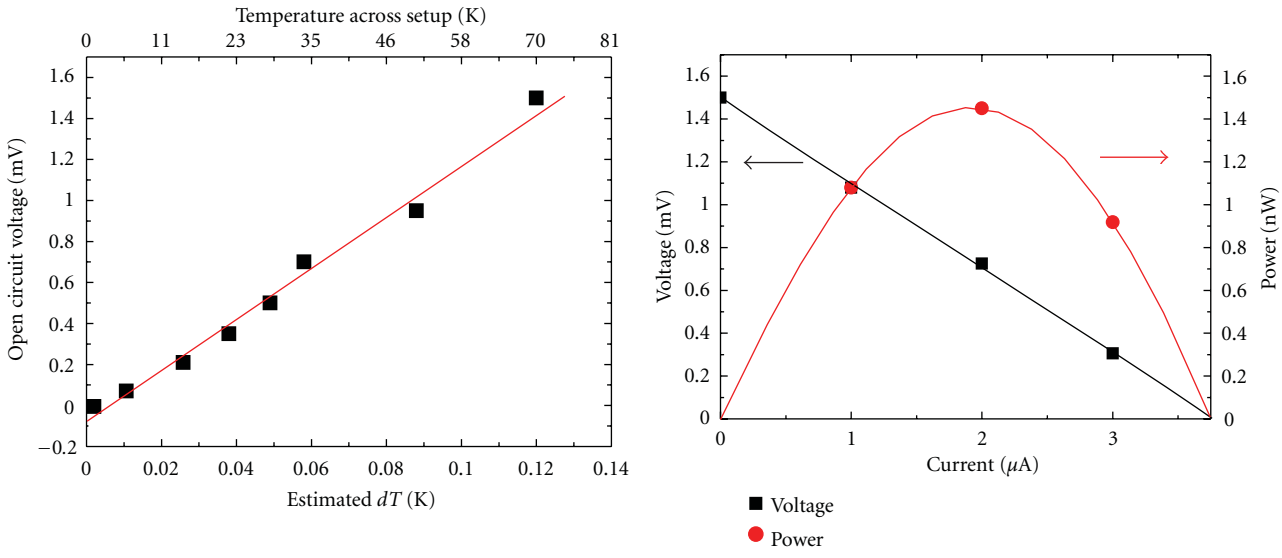
5. Summary

The status of vertical GAA nanowire technology platform developed using top-down approach has been reviewed. Area, speed, and power advantages of vertical platform for green CMOS based electronics are discussed. In addition to excellent MOSFET scaling potential, the vertical wire is projected as a natural platform for TFET devices demonstrating record low subthreshold slope. Progress on nonvolatile memory cells is reviewed and junction-less wire memory is projected as an excellent platform for 3D stacking. Nanowires seem to have possible novel solutions in low cost solar and thermal energy harvesting. The presented top-down techniques can potentially address the needs of "end-of-the-Silicon technology-roadmap" and beyond CMOS era, possibly can lead to an all nanowire autonomous system where data computation, data storage, energy harvesting,



(a) (b)

FIGURE 24: (a) Snapshot of the completed TEG (6 pads at the sides of the TEG to allow connections of different areas). Connecting the terminals 1 and 5 establishes an ohmic path between several serpentine P- and N-elements in a 5 mm × 5 mm area. (b) Different layers used in the experimental setup. Indicated in the different layers is the thermal resistance used in the calculations. The heat sink thermal resistance calculation is based on Al with a dimension of 5 cm × 5 cm × 5 mm. (Reprinted with permission from [70]. [2011] IEEE.)



(a) (b)

FIGURE 25: (a) Plot of the TEG's V_{oc} versus the different dT (actual/estimated) applied across it. A best fit line is drawn through all the data points. (b) Voltage/Power versus Current curve when dT (estimated) is 0.12 K with V_{oc} and I_{sc} of 1.5 mV and 3.79 μA, respectively. The black line is a linear fit and the red line a polynomial fit of the data points. (Reprinted with permission from [70]. [2011] IEEE.)

and energy storage could all be possible by using nanowire devices, all integrated on chip either at same level or different, using TSV if not direct. Thus, nanowire technology indicates feasibility of opening up newer application opportunities for Si technology.

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Research Article

Flat-Top and Stacking-Fault-Free GaAs-Related Nanopillars Grown on Si Substrates

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The VLS (vapor-liquid-solid) method is one of the promising techniques for growing vertical III-V compound semiconductor nanowires on Si for application to optoelectronic circuits. Heterostructures grown in the axial direction by the VLS method and in the radial direction by the general layer-by-layer growth method make it possible to fabricate complicated and functional three-dimensional structures in a bottom-up manner. We can grow some vertical heterostructure nanopillars with flat tops on Si(111) substrates, and we have obtained core-multishell Ga(In)P/GaAs/GaP nanowires with flat tops and their air-gap structures by using selective wet etching. Simulations indicate that a high-Q factor of over 2000 can be achieved for this air-gap structure. From the GaAs growth experiments, we found that zincblende GaAs without any stacking faults can be grown after the GaP nanowire growth. Pillars containing a quantum dot and without stacking faults can be grown by using this method. We can also obtain flat-top pillars without removing the Au catalysts when using small Au particles.

1. Introduction

Free-standing nanowires are promising for future nanoscale devices. The VLS growth method enables us to make quantum structures in nanowires, which will contribute to the development of nanodevices such as transistors [1], nanolasers [2], and nanosensors [3]. The VLS mechanism was first proposed for Si whiskers by Wagner and Ellis in the 1960s [4]. Later, after the encouraging studies on light-emitting diodes using nanowires by Hiruma et al. in the 1990s [5], many studies of semiconductor nanowires aiming at the production of functional devices have been reported. The VLS mechanism is similar to liquid-phase epitaxy but is driven catalytically in the nanoarea by nanosized particles of a metal such as Au. This feature is very useful from the viewpoint of reducing growth time and the consumption of both power and source materials for industrial fabrication. Moreover, VLS growth is suited for application to Si-based optoelectronic integrated circuits (OEICs) because it enables to connect various III-V materials and is performed at low temperature. As already demonstrated by several groups, vertical GaP nanowires can be grown on Si(111) without dislocation at the interface between the nanowire and the substrate [6–8]. One of our future plans is to make nanolasers on Si substrates. The number of quantum dots can be defined in one pillar by the VLS process, which makes it easy to access quantum dots in an optical manner. And we believe that VLS growth is the most promising technique for realizing nanodevices by means of a fully bottom-up process in the future. We have recently reported core-multishell nanowires with flat tops and shown that air-gap structures can be formed just by using selective wet etching [9, 10]. These structures were grown by combining the VLS growth and MOVPE (metalorganic vapor phase epitaxy). Our fabrication methods are in general bottom-up approaches. In this paper, after briefly explaining the fabrication procedure and characterization methods, we first describe core-multishell nanowires with air gaps and show the possibility of photonic crystal (PhC) devices using nanowires. Next, we report stacking-fault-free GaAs nanopillars using GaP nanowires on Si. We show that zincblende GaAs can be formed over GaP nanowires without any stacking faults, which will lead to refined heterostructures and band engineering. A technique for removing Au particles helps us form pillars with flat tops,

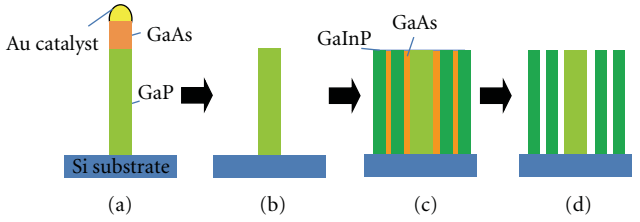

Figure 1: Cross-sectional schematic images of core-multishell nanowires with air gaps explaining the fabrication process. (a) GaAs/GaP nanowires on Si(111); (b) GaP nanowires after Au/GaAs removal; (c) alternated GaAs/GaInP shell growth at high temperature; (d) after removal of GaAs for air gaps.

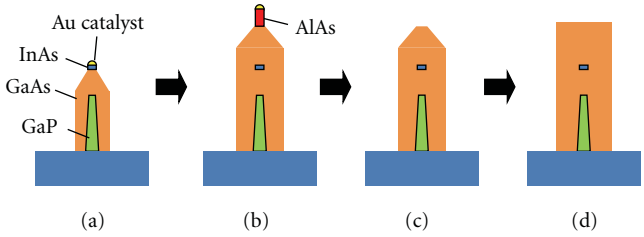

Figure 2: Cross-sectional schematic images of nanopillars explaining the fabrication process. (a) InAs/GaAs/GaP nanowires on Si(111); (b) GaAs and AlAs growth; (c) after removal of AlAs together with Au particles; (d) GaAs growth.

which are very suitable for light propagation. Finally, we introduce an interesting phenomenon: the formation of flat-top nanowires achieved by using small-sized Au particles in only one growth procedure.

2. Experiments

The wire growth was carried out in a low-pressure (76 Torr) horizontal MOVPE reactor [7–10]. Trimethylgallium (TMGa), trimethylaluminum (TMAl), and trimethylindium (TMIn) were the group III sources. Phosphine (PH_3) and arsine (AsH_3) were the group V sources. The catalysts were Au particles obtained from Au colloids (5, 10, 20, and 40 nm in diameter).

First, GaP nanowires were grown on Si(111) substrates in two steps [7]. A small amount of GaP was grown for 5 s at 550°C by introducing TMGa of 4.8×10^{-6} mol/min and PH_3 of 4.5×10^{-4} mol/min. Then, the remaining GaP wire growth was performed at 480°C by introducing the same source gasses. This two-step growth increased the probability of vertical nanowires.

Figure 1 shows the fabrication procedure for core-multishell nanowires with air gaps [10]. For core-multishell GaInP/GaAs/GaP nanowires, the flow rates of TMGa and AsH_3 or PH_3 were 9.5×10^{-6} and 4.5×10^{-4} mol/min for GaAs/GaP(core) nanowires, those of TMGa and AsH_3 were 4.6×10^{-5} and 1.1×10^{-3} mol/min for GaAs shells, and those of TMGa and TMIn were the same, 9.5×10^{-6} mol/min. The flow rate of PH_3 was 1.6×10^{-3} mol/min for the GaInP shells. The alternating GaAs/GaInP shell layers were grown at 580°C after the fabrication of GaP core nanowires from which gold had been removed. After the GaAs/GaP(core) nanowires had been grown, the GaAs with Au particles were removed by wet etching (etchant of one part 96% H_2SO_4, ten parts 30% H_2O_2, and 50 parts H_2O) as shown in Figures 1(a) and 1(b). Then multishells were grown in the MOVPE chamber again (Figure 1(c)). Finally, air-gap structures were formed by removing GaAs layers with the same wet etchant (Figure 1(d)).

Stacking-fault-free nanopillars were also formed by combining the VLS growth mode and MOVPE mode. The flow rate of the group III sources was $5–10 \times 10^{-6}$ mol/min and that of the group V sources was 4×10^{-4} mol/min. Figure 2 shows the procedure for obtaining the target nanostructure. After the Au particles from the Au colloids had been dispersed on the surface, the temperature was raised to 520°C to grow GaP nanowires for one minute. Then GaAs growth was performed at 550°C (HT-GaAs) for 10 min, after which the nanostructures show pillars surrounded by {112} facets with tapered tops. Next, as shown in Figure 2(a), InAs growth was performed at 460°C for 3 s. The Au particles used here were 20 nm in diameter so quantum confinement was not strong enough in the lateral direction. In principle, we can make the InAs smaller in the lateral direction by using smaller Au particles. The thickness of the InAs was not optimized in this study, but we aimed at a thickness of under 10 nm. The InAs nanowire growth on GaAs pillars was confirmed at this temperature by other additional experiments. Finally, HT-GaAs was grown again for 10 min and AlAs nanowires were grown at 460°C for 20 s (Figure 2(b)). The process from (a) to (b) in Figure 2 was one continuous run in the chamber. After that, the sample was dipped in wet-etchant ($H_2SO_4/H_2O_2/H_2O$, the same as described above) to remove AlAs nanowires together with the Au particles (Figure 2(c)). The sample again loaded into the growth chamber, and HT-GaAs was grown for 7 min to make flat-top pillars (Figure 2(d)). The nanopillars shown in the last section were formed by using the same flow rates as described here.

The structures of the nanowires were observed by scanning electron microscopy (SEM, Hitachi, S-5200, operated at 15 kV) and transmission electron microscopy (TEM, JEOL, JEM2100F, at 200 kV). High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) and energy dispersive X-ray spectrometry (EDS) analyses were also performed in the TEM chamber to evaluate the element distribution in the nanowires. For optical characterization, photoluminescence (PL) measurements were performed at 4 K using cw excitation (a Ti:sapphire laser: 710 nm, 100 μW). The collected luminescence was fed to a spectrometer equipped with a silicon charged-coupled device (CCD) and InGaAs diode array.

3. Results and Discussion

3.1. Core-Multishell Nanowires with Air Gaps. For most reported core-shell nanowires, the aim has been to just cap the core for protection against various surface effects in

order to improve the conductivity of electrons or holes or to enhance emission from the optical active part [11, 12]. Our purpose with the core-multishell structure here is to form a high-Q cavity utilizing the large difference of the refractive index between semiconductor and air [10]. Figure 3 shows core-multishell nanowires that we formed using GaP/GaAs in order to investigate heterostructure in the radial direction. The fabrication process was the same as that for GaInP/GaAs as explained in Figure 1. The TEM sample of the core-multishell GaP/GaAs/GaP nanowires was thinned to about 100 nm by using the FIB (focused ion beam) method. The nanowires were vertically aligned on the Si(111) substrates. To form flat-top structures, the removal of Au catalysts was performed. The nanowires appeared as hexagonal cross sections with six {110} sidewalls from the top view. From EDS data in Figure 3(b), the core and outer shells were confirmed to be GaP and the inner shell to be GaAs. Due to the removal of Au particles, the vertical growth in the VLS mode was completely suppressed. The species absorbed on the top face could not be crystallized there. Instead, they migrated to the sidewalls and contributed to the radial growth, since it was difficult for two-dimensional nucleation to occur on the (111)B faces under the currently used growth conditions. The nanowires had a [111]B-oriented zincblende structure. For general VLS-grown nanowires, stacking faults are observed when nanowires are grown along the [111]B orientation [13]. As seen in the TEM images, the stacking faults in the core apparently continue to the shell layers. These stacking faults indicate the formation of a polytypic structure, which makes it difficult to estimate the band structure and to evaluate the properties of carrier transport, emission, and so on. To improve the crystallinity, it is necessary to grow stacking-fault-free core nanowires as explained in the next section. The core nanowires had a hexagonal cross-section with {112} sidewalls, which were faceted by alternating {111}A and {111}B microfacets as has been explained by Johansson et al. [14]. After the growth of the shell layers, the {112} sidewalls changed into {110}. Different growth modes under certain growth conditions, namely, the VLS and MOVPE or layer-by-layer growth modes, may be responsible for the transition of the sidewalls. When the GaP nanowires were grown in the VLS mode at low temperatures, {112} sidewalls appeared. When the GaP shell layer was grown in the layer-by-layer growth mode at high temperatures, {110} sidewalls appeared.

On Si(111) substrates, we observed core-shell heterostructures whose interfaces continued to the tops and bottoms as shown in Figures 3(c) and 3(d). This is very important because it enables us to form air-gap structures by selective wet etching alone. If the layers were capped at the flat top, we would have to perform dry etching to remove the top layer. And we should also protect the side walls so that they are not etched off by the etchant. Some top-down process is therefore necessary here. Further, if the layers were deposited on the Si and had continued to the shell layers, the shells would come off easily after the wet etching. Actually, we have seen several samples with covered tops and continuous layers on the Si surface to shell layers, so the structure seen in Figure 3 is rather rare. One possible way to obtain high yields for ideal structure is to fabricate Au-array patterns on the substrate, select proper precursor materials, and control the surface state and distance between each nanowires, that is, control the diffusion properties of reaction species on the surface.

GaP is not suitable for investigating optical characteristics because it is an indirect band-gap material. And the difference in the lattice constant between GaAs and GaP leads to defects or dislocations. We therefore tried to use ternary GaInP for shell growth. Actually, GaP shells were largely strained on GaAs so that cracks were easily formed after the removal of GaAs. By using GaInP, we can adjust the composition of the layer so that it is lattice matched to GaAs. Figure 4(a) shows a SEM image of a core-multishell GaInP/air-gap nanowire. On the surface, aggregated materials occupied a large area, and some structures were covered with a thin overgrown layer on the tops, which prevented the wet etchant from permeating the structures. We managed to observe a well-shaped pillar. The wet etching time was not optimized in this experiment, and it was not apparent if the GaAs shells were completely removed. Because it was difficult to find such well-shaped pillars as seen in Figure 4(a), we could not perform further experiments. Considering the border between the GaP shell and the substrate seen in Figure 3(d), it seems that GaP did not form chemical bonds to the Si substrate. Possibly, most GaP and also GaInP reaction species diffused largely on the substrate surface without epitaxial growth. These core-shell structures with air gaps are promising for PhCs. Due to the large difference in refractive index between semiconductor and air, we can make some efficient cavities. Expecting a high-Q factor and a small mode volume, we performed several simulations using the three-dimensional FDTD (finite differential time domain) method. As shown in Figure 4(b), a structure with three-alternated shells showed a high-Q factor of 2770 and small effective mode volume of $0.8\,(\lambda/n)^3$ (λ is wavelength and n is refractive index) as a whispering gallery mode. The Q factor was comparable to that of vertical-cavity surface-emitting lasers (VCSELs), which is about 2100, but the mode volume was very small compared with that of VCSELs (about $5\,(\lambda/n)^3$) [15]. We are planning further optimization for this kind of structures.

Here, we performed the Au particle removal by wet etching. Exposing nanowires to air permits surface oxidization and impurity contamination. A continuous process from core nanowire growth to shell growth in a growth chamber is a promising way to prevent this. Some in situ selective etching or selective removal of a certain material, like the technique we performed to make bending nodes by annealing [16], will be necessary for refinement of the crystal.

In this section, one possible way to make optical cavities using nanowires was described. At this stage, there are still many challenges in realizing ideal structures for devices. One of them is how to make structures without stacking faults, which is very important for band-gap engineering as stated above. The next section presents one solution for obtaining stacking-fault-free structures.

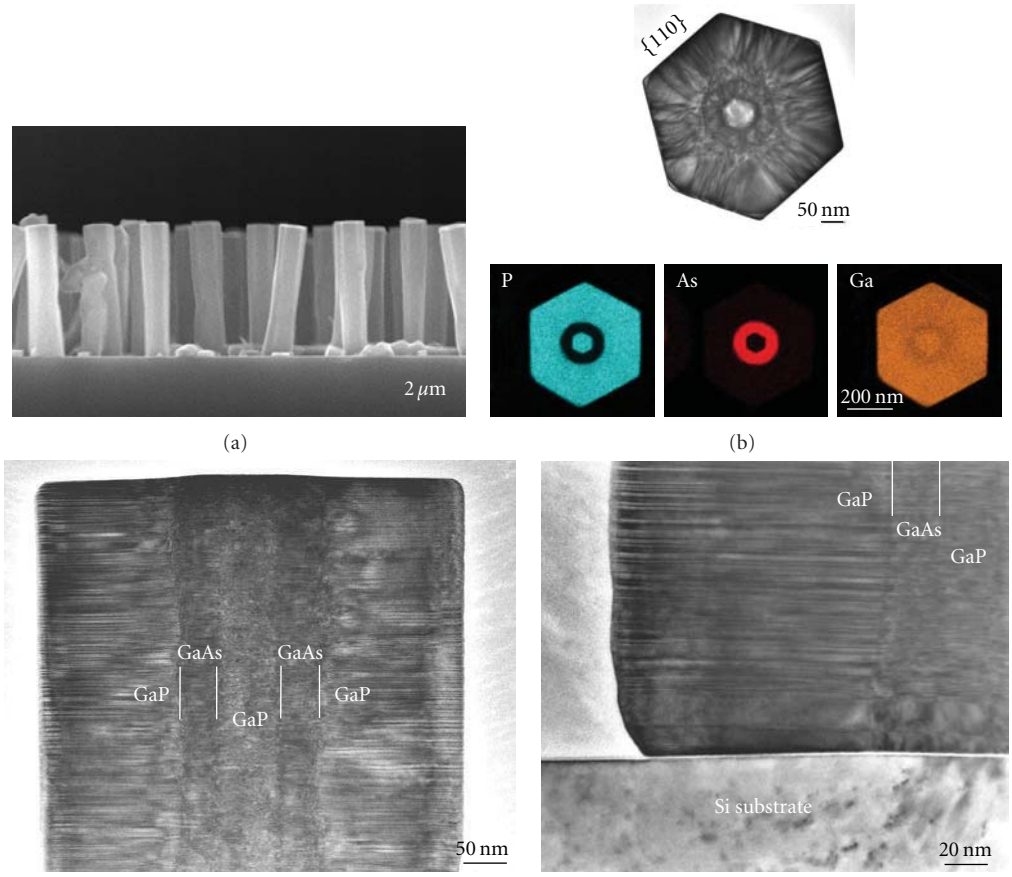

Figure 3: (a) SEM and (b)–(d) TEM images of the core-multishell GaP/GaAs/GaP nanowires. EDS mapping images are also included in (b). (a) Side view. (b)–(d) Sliced and thinned samples: (b) perpendicular to the axis; (c), and (d) along the axis.

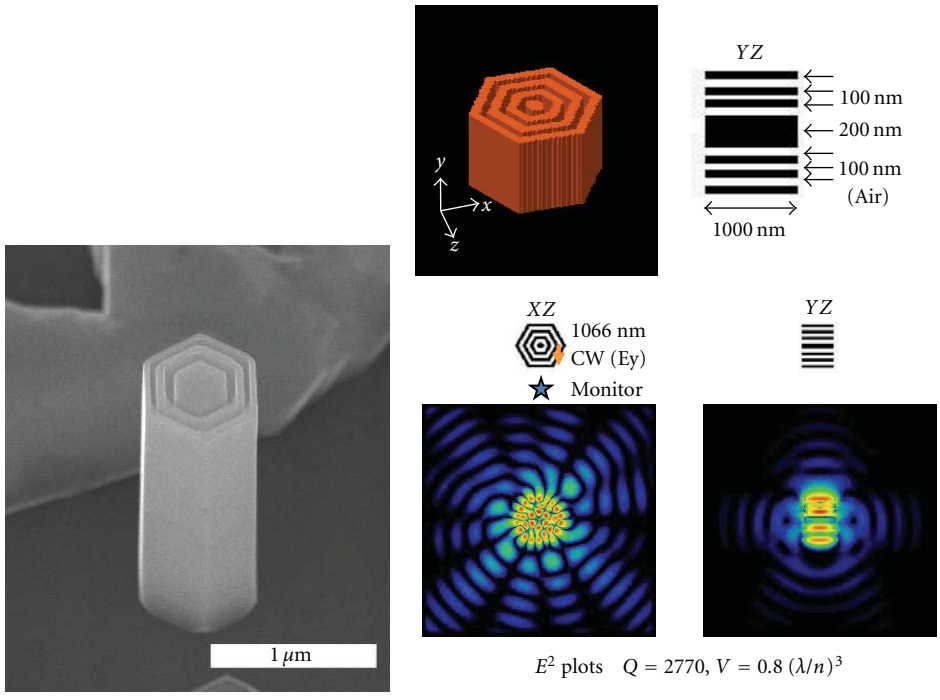

Figure 4: (a) SEM image of core-multishell $(GaInP/air\text{-}gap)_2/GaInP/GaP$ nanowires on Si(111). (b) One simulation result by 3D-FDTD for the illustrated structure.

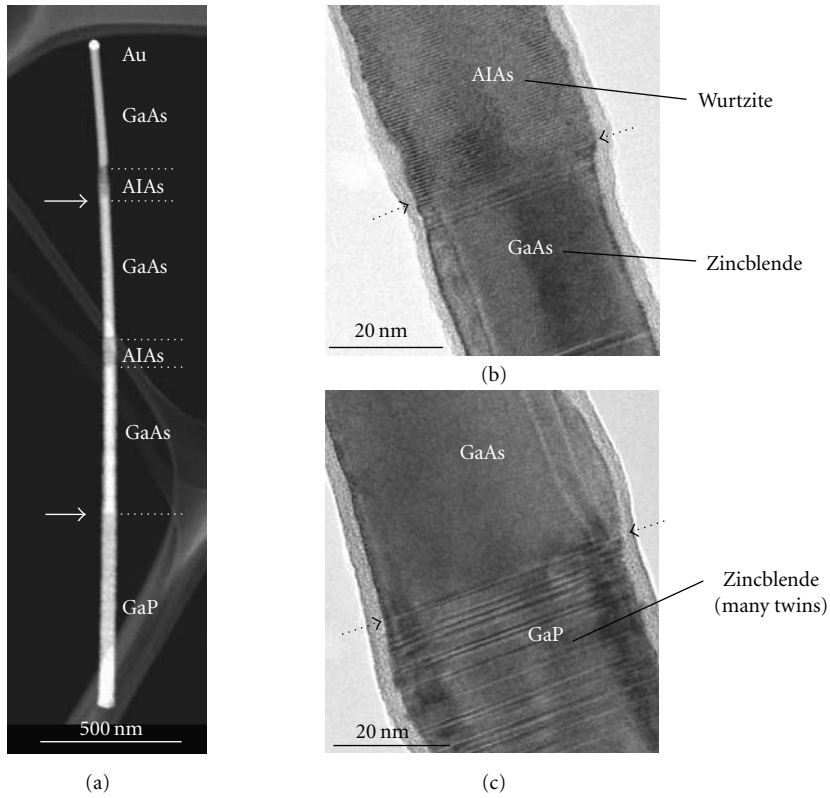

Figure 5: An AlAs/GaAs/GaP heterostructure nanowire. (a) A HAADF-STEM image; (b) and (c) HRTEM images of the areas near AlAs/GaAs and GaAs/GaP interfaces, respectively [17].

3.2. Stacking-Fault-Free GaAs-Related Nanopillars. Recently, we reported the structural characteristics of AlAs/GaAs/GaP nanowires on Si and found some interesting structures in them [17]. Figure 5 shows the TEM images on such nanowire. The GaP had a zincblende structure with many stacking faults. However, zincblende GaAs that was almost completely free of stacking faults was grown on this GaP. And AlAs with a wurtzite structure was grown on this GaAs. Among the three materials, we focused on the GaAs on GaP nanowires and studied it further.

Figure 6(a) shows a TEM image of the nanopillars on a Si substrate, whose fabrication process was explained in Figure 2. We could obtain flat-top nanopillars vertically grown on Si substrates. The TEM image and the selected area electron diffraction (SAED) patterns were observed through the $[1\bar{1}0]$ projection. In contrast to the bottom SAED pattern that shows some satellite-like spots in between the main diffraction spots due to a polytypic structure containing rotational twins, the upper region is apparently a single-crystal zincblende structure. From the evaluation of the height, the boundary between the regions with and without stacking faults was the top of the GaP nanowires. Although we could obtain this unexpected and fortunate result, the mechanism for stacking-faults-free growth is not clear at present. After the growth on Si and a GaP nanowire, the Au particle contained much Si and GaP [8]. One hypothesis is that the Si and GaP in the Au alloy particle reduced the effective volume for the supersaturation. This would prevent changes in the layer-stacking sequence (ABC-ABC stacking for zincblende structure), leading to stable and continuous nucleation [14, 18].

As shown in the growth procedure in Figure 2, we inserted an InAs quantum dot. From the evaluation of the height, the quantum dot was located in the stacking-fault-free region. To determine the quantum dot position more precisely, we performed EDS analysis as shown in Figure 6(b). However, no clear sign of an InAs quantum dot was detected. The InAs seemed to be so thin that the luminescence from the K line for In was under the detection limit. We also performed low-temperature PL measurement. Figure 6(c) shows the PL spectrum at 4 K obtained from a single pillar. Only one peak with shoulders was seen in the range from 750 to 1600 nm. The peak at 821 nm (1.51 eV) is attributed to zincblende GaAs [19, 20]. A shoulder at 832 nm (1.49 eV) is also seen, which is attributed to carbon-related emission [20]. Possible InAs-related emission around 1.46 eV as a shoulder is seen. The intensity is very week, although the InAs is located in the twin-free region. Possible reasons are high concentrations of impurities and nonradiative centers. In addition, InAs dots were about 20 nm in diameter, which might cause stress around the dot region due to large lattice mismatch, and this stress would influence the emission. We have to reduce the impurities, especially carbon, by optimizing the growth conditions and should use low-strain quantum-dot material-like GaInAs.

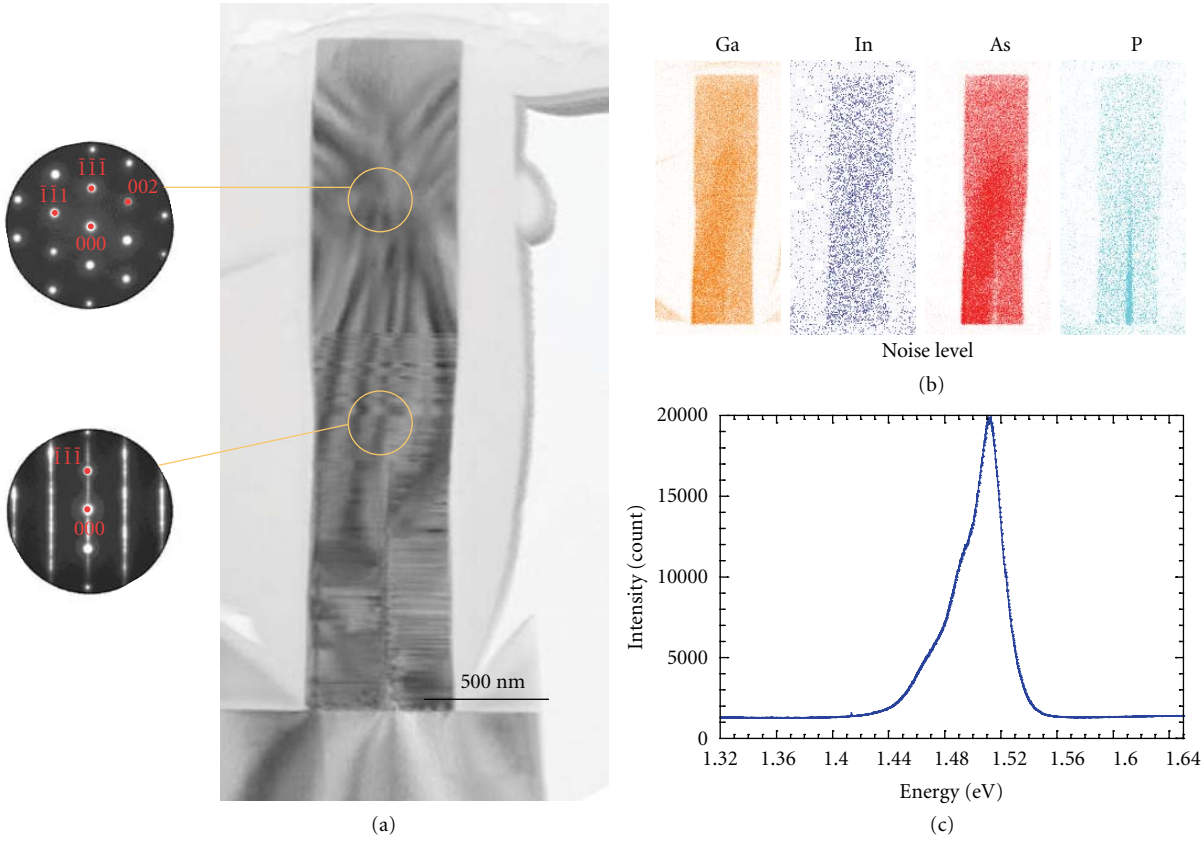

FIGURE 6: GaAs nanopillar containing an InAs dot. (a) HR-TEM image of the nanopillar and SAED patterns; (b) element mapping by EDS obtained from K lines; (c) PL spectrum of one nanopillar at 4 K.

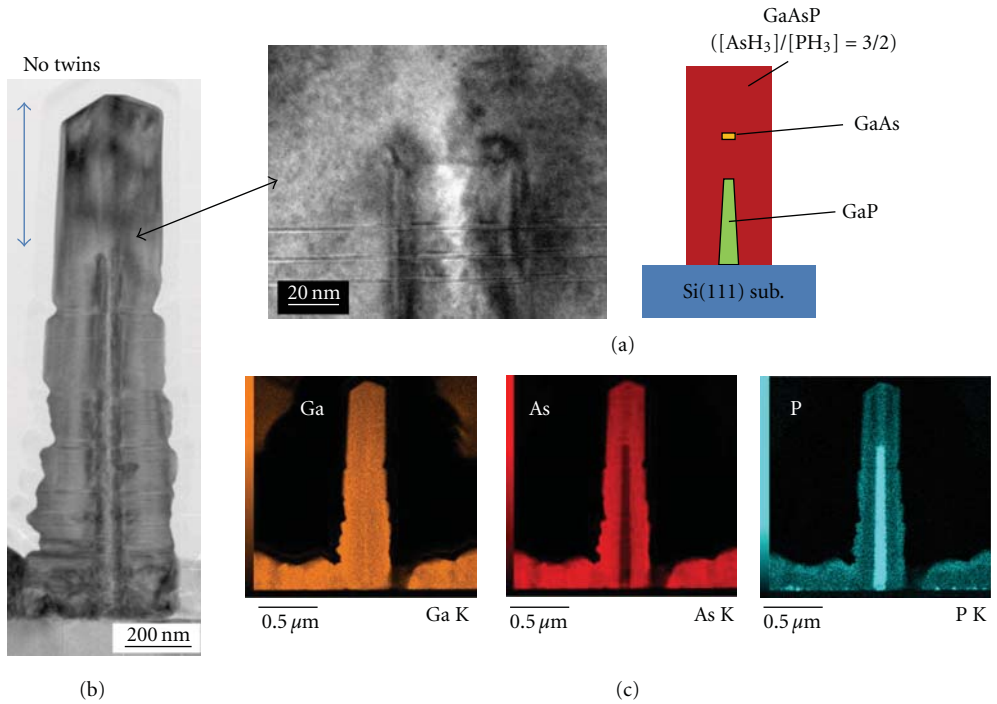

FIGURE 7: GaAsP nanopillar containing a GaAs dot. (a) Schematic illustration; (b) TEM images; (c) EDS mapping images. Here, an Au colloid with 60-nm diameter was used. The sample was thinned by the focused ion beam method. A stacking-fault-free region is confirmed above the GaP nanowire. However, we could not observe the dot in the pillar.

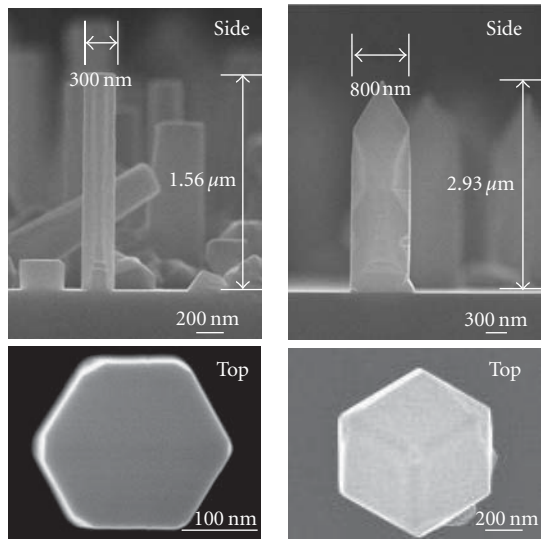

Figure 8: SEM images of GaAs/GaP nanopillers on Si. Diameters of Au colloids are (a) 5 and (b) 60 nm.

In order to observe a quantum dot in a pillar, we tried another experiment in which we changed the material combination and growth conditions. Figure 7 shows a GaAsP nanopillar with a GaAs dot. The fabrication process was the same as explained above (Figure 2), and the structure is schematically illustrated in Figure 7(a). For the growth of GaAsP, the flow ratio of AsH_3 to PH_3 was kept at 3/2 for both the core and shell regions. We sliced the sample for TEM measurement to about 100-nm thick with an FIB method so that we could see the crystal structure clearly. Figure 7(b) is the TEM image of this sample. Since we used 60-nmϕ Au colloids, the shell was not thick enough to make a flat top. The interface between the GaP and GaAsP is clearly seen. EDS mapping images in Figure 7(c) more clearly show the interface than those in Figure 6(b). A stacking-fault-free region is confirmed above the GaP nanowire. But unfortunately, we could not observe the dot in the pillar. This may be due to the high As content in the GaAsP region, whose intensity was not so different from that of the GaAs quantum dot. In our experiments, we failed to see a quantum dot in the pillar. Considering the growth process, we believe that the quantum dot could be formed in this zincblende sacking-fault-free region and will seek to identify it by another method in the near future.

3.3. Flat-Top Nanowires by One Growth Procedure. To make flat-top pillars, we have to remove Au particles, which still act as catalyst and selectively enhance the axial growth also at high growth temperature. There are several methods for removing Au particles as described in Section 3.1. Selective wet etching is a reliable method, but the nanowires have to be exposed to air which causes impurity contamination. We can remove Au particles just after the nanowire growth by selectively removing one part of the heterostructure nanowires by annealing or gas etching. In this case, possible material combinations are limited for achieving high selectivity. Here, we introduce another method for making flat-top pillars. We found that, when we use small-sized colloids 5 nm in diameter, GaAs pillars showed flat tops. First, GaP nanowires were grown at 520°C, and then GaAs was grown at 600°C. Figure 8 shows SEM images for this sample and a sample with GaAs pillars formed by using Au colloids with 60 nm in diameter. The pillars with 60-nm Au have a tapered structure at the top region due to VLS growth mode. On the other hand, the pillars with 5-nm Au have flat tops and are surrounded by six {110} side facets. We also confirmed that the GaAs above GaP nanowires is a stacking-fault-free zincblende structure from TEM images (not shown here). At high growth temperature, the concentration of Ga in Au particles becomes high. So it is assumed that highly Ga-containing Au particles could not keep their hemispherical shape and were buried in the surrounding layer, forming stable facets of {110} and (111)B at the top. It resembles GaAs nanowires buried with AlGaAs layers which were grown at high temperature [21]. But in this case, it seems that there was no Au particle on the top surface. If this is the mechanism, the pillars may contain Au inside. We hope to confirm this experimentally and investigate its influence on device performance. Whether Au is in the core region or not, high-quality layers can be grown in the radial direction just after the core growth. The pillars are not exposed to air on the way, and the layers are epitaxially grown on the single-crystal GaAs core. By combining our techniques described above, we expect to be able to obtain a refined laser structure in the bottom-up manner; we can already make a quantum dot without stacking faults as described in Section 3.2 and cavity structures explained in Section 3.1. We hope to demonstrate this in the near future.

4. Conclusions

We grew vertical nanopillars with flat tops on Si substrates and were able to make cavity structures with air gaps and

stacking-fault-free GaAs regions containing a quantum dot in the upper part of the pillars. We obtained core-multishell Ga(In)P/GaAs (or air-gap)/GaP nanowires with flat tops, which we will be able to apply to photonic crystal devices. In the fabrication and characterization of GaAs nanopillars using GaP-based nanowires on Si(111), we found that zincblende GaAs without any stacking faults can be grown after the GaP nanowire growth. And we obtained flat-top pillars using small Au particles. We expect to obtain a refined laser structure in the bottom-up manner by combining these growth techniques.

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