International Transactions on Electrical Energy Systems

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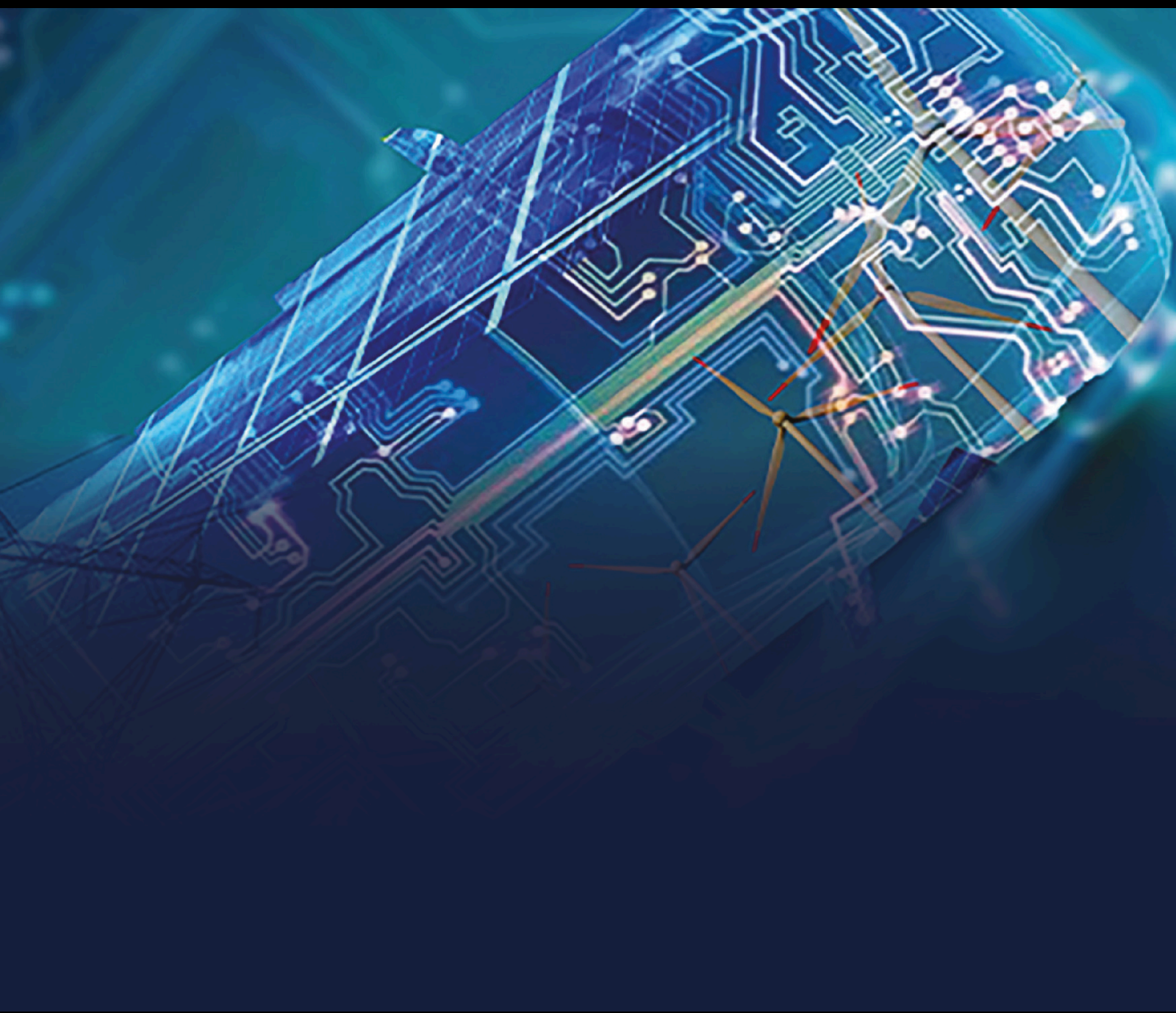

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Research Article

Experimental Implementation of Cascaded H-Bridge Multilevel Inverter with an Improved Reliability for Solar PV Applications

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This study presents the boost converter-based cascaded H-bridge (CHB) multilevel inverter with improved reliability for solar PV (photovoltaic) applications. The solar PV is associated with the boost converter to enhance DC link voltage by using the maximum power point tracking-perturb and observe (MPPT-P & O) technique. The proposed configuration is aimed toward the performance analysis of the boost converter-based CHB MLI by reducing the number of components, low total harmonic distortion (THD), reduced power, less cost function, low total standing voltage (TSV), improved reliability, and switching losses for solar PV application. In this study, a CHB multilevel inverter is used to obtain stepped pure sinusoidal AC from the solar PV array. The proposed boost converter extracts maximum power and enhances higher DC link voltage which provides high efficiency. The boost converter is integrated with a 27-level CHB multilevel inverter to generate near-sinusoidal output voltage with lower THD. The inverter is tested with linear and nonlinear loads for robustness, and during dynamic loads, inverter is stable and well suited to grid-connected applications. A detailed comparison is presented on the component count and reliability aspects with existing MLIs and 27-level MLIs. The simulation outcomes of the implemented arrangement are presented with the help of MATLAB/Simulink, an experimental prototype is developed using a dSPACE RTI1104 controller and also tested in the research laboratory for checking the possibility of the implemented arrangement.

1. Introduction

There must be situated worldwide creativities in favor of the elevation of independent renewable energy schemes. This creativity has run for the growth of renewable power-producing systems that remain accomplished in giving self-sufficient power production with the help of additional standalone renewable energy sources (RES) [1, 2]. The further most usually used hybrid RES is the wind in addition to solar power [3, 4]. These two RES remain irregular; consequently, the utilization of ESS (energy storage system) is typical within stand-governing submissions [5, 6]. The hybrid renewable energy schemes are having some controlling methods which offer a resourceful transfer of power. An approach to the energy translation arrangement as well as converters has various demerits at several stages in the system; this is to be implemented with a lot of technical concentration and investigation in this part [7–9]. Henceforth, there is rapid growth in the study of different RES such as solar, tidal, and wind to extract power. Amongst PV, the energy extracted plays an energetic role, and it is direct current (DC) in nature. After getting DC from panels, it is important to convert as AC to meetup with locals as well as industrial power requirements. For this, the inverters play a very important role [1, 9]. The 2-level MLI are operated underneath, a higher switching frequency, resulting in higher dv/dt of voltage production, higher EMI (electromagnetic interferences) [10, 11] as well as increased heat issues in the switches. The MLI can overawe disadvantages related to the 2-level MLI from multiple points of view. With a created number of MLI levels, an almost unadulterated sinusoidal wave structure is accomplished. As the number of MLI levels rises, the THD in the air conditioner yield is diminished. It can minimize the harmonic contents along

with maximizing the power in the AC voltage output side [12, 13]. The tweak game plan serves the purpose of properly turning ON and OFF the force switches. Diode clamped, flying capacitor, and CHB (cascaded H-bridge) MLI are 3 regular MLI topologies [14, 15]. MLIs are usually used in various variable speed drives and renewable energy applications as well as static reactive power compensators [16, 17]. Diode clamped alongside flying capacitor MLI experience issues at higher yield levels such as voltage offsetting alongside unique voltage sharing. Consequently, among the traditional MLI CHB arranging is broadly perceived because of their secluded structure as small as shortcoming open-minded capacity [18–41]. The exchanging heartbeats can be created by utilizing various regulation procedures for MLIs. The boost converter is the standout reasonable converter as it can build the dc voltage as needed, and it is associated with a dc-dc converter among load and sun-based boards to fulfill the necessities [39]. The voltage output from the solar PV feed to the boost converter boosts the output and the output can be changed by changing the parameter of the boost converter.

In this investigation work, a configuration of boost converter-based 27-level cascaded MLI has been presented as an analysis in detail. A brief description of the boost converter is explained in Section 2. Implemented 27-level cascaded MLI is discussed along with simulation results in Section 3. The proposed system losses, efficiency, TSV, cost function, and reliability are presented in Section 4. The comparison of the proposed system with existing topologies is presented in Section 5. The experimental results are described in Section 6. Finally, the conclusion is discussed in Section 7.

2. Proposed Configuration

Figure 1 shows the projected arrangement, and it involves a solar photovoltaic- (PV)-based boost converter with integrated CHB MLI. The maximum possible voltage at the boost converter to survive high variable input currents from radiation through the photovoltaic array is to be maintained. According to the input voltage variations, the boost converter consisting of switches must be given the gate pulses. For constant voltage, the boost control is provided by the MPPT algorithm.

2.1. Modeling of a Boost Converter. The boost converter circuit contains capacitor (C), inductor (L), diode (D), and a load resistor (R_L) alongside the control switch (S). These components are related to the voltage input source (V_{in}) to support the voltage. By the obligation cycle control switch, the output voltage of the lift converter is controlled. The output voltage can be differed by shifting the ON season of the switch, and for the obligation cycle (D), the normal yield voltage can be determined by utilizing the following beneath equation:

$$\frac{V_0}{V_{\text{in}}} = \frac{1}{(1-D)}, \tag{1}$$

where V_{o} = output voltage and V_{in} = input voltage of the converter, respectively, and D = duty cycle.

2.2. Choice of Inductor. The boost converter inductor value is calculated by using following equation:

$$L = \frac{V_{\text{in}}}{F_s * \Delta I_L}, \tag{2}$$

where F_s is the switching frequency (10 kHz) and ΔI_L is the current ripple.

CRF (Current ripple factor) is defined as the ratio between input current ripple and output current. For a respectable estimate of an inductor, the CRF value should be assured within 30%. The inductor current rating is always higher than that of the output maximum current $(\Delta I_L / I_0) = 0.3$.

2.3. Choice of Capacitor. The value of the capacitor can be obtained from

$$C = \frac{I_{\text{out}}}{(F_s * \Delta V_0)D}, \tag{3}$$

where ΔV_0 = voltage output ripple which is typically measured as 5% of voltage output which produces $\Delta V_0 / V_0 = 5\%$.

The boost converter modeling can be calculated by using the above equations and the obtained values are presented in Table 1.

2.4. Solar Photovoltaic Powered Boost Converter. The current and voltage received from the solar photovoltaic array depend on temperature, the number of series-connected strings, and the number of parallel-connected string sand irradiance. So, it is essential to select the type of solar panel intelligently. Here, 1STH-215-P panel, 1Soltech with 2 parallel strings along with 2 series-connected modules per string is designated. The specifications of the selected solar panel are given for 1 series-connected module 1 and parallel string at 25°C temperature and irradiance of 1000 W/m^2 and are described in Table 2. Figure 2 represents the control and operation of a 3-level boost converter 19, which contains two dc-link capacitors C_1 and C_2, boost inductor L, and S_1 and S_2 switches, and Table 1 specifications of the boost converter are tabulated. The 3-level boost converter has 4 modes of operation depending on the switching states. Mode 2 & 3 occurs when either S_1 or S_2 is turned ON. Mode 1 & 4 occurs when S_1 and S_2 are turned OFF or ON, respectively. It is seen that dependent on the estimation of obligation proportion D there are 2 working areas. The converter permits working in Modes 2, 3, and 4 for the obligation cycle ($0 < D < 0.85$), whereas the converter permits working in Modes 1, 2, and 3 for ($0.85 > D < 1$). The connection between the complete dc-interface voltage and PV input source voltage is given by the following expression:

$$V_{dc} = \frac{V_{PV}}{(1-D)}. \tag{4}$$

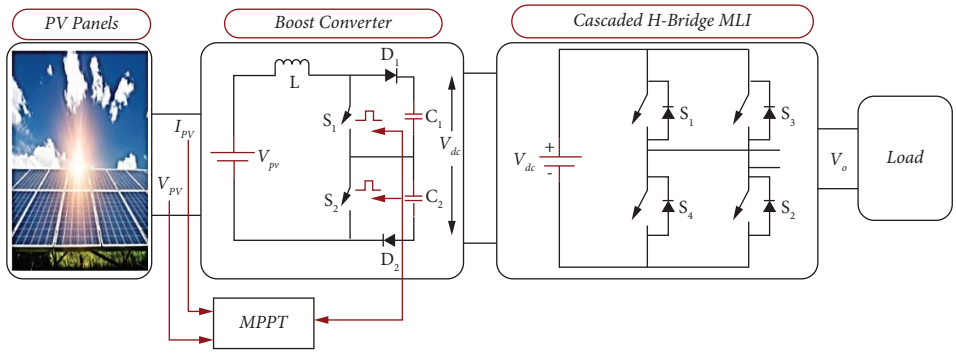

Figure 1: The proposed arrangement.

Table 1: Specifications of a boost converter.

Parameters	Value
Inductance L	15.38 mH
Input DC voltage	~60 V
Capacitance C_1 & C_2	282 μF
Duty cycle	0.85
Resistance (R_2)	10 Ohms

Table 2: Specifications of 215 W PV module.

Parameters	Value
Maximum power	213.15 W
Short circuit current (I_{sc})	7.84 A
Open-circuit voltage (V_{oc})	36.3 V
Current at maximum power point (I_{mpp})	7.35 A
The voltage at maximum power point (V_{mpp})	29 V
Diode ideality factor	0.98117
Diode saturation current (I_o)	$2.9259 * 10^{-10}$A

2.5. MPPT Method. In favor of tracing the maximum power point, it is required to use an algorithm in the P vs. V graph of the solar photovoltaic module. So, many methods are available to track the maximum power point such as incremental conductance, perturbing, and observing the fractional open-circuit voltage, and genetic algorithm. The MPPT algorithm implemented is represented in Figure 3, and the solar PV panel specifications are mentioned in Table 2.

In this paper, perturb and observe algorithm has been used. By varying the perturbation value, the maximum power point willpower speed can be controlled. Figure 3 shows the P&O algorithm flowchart. The algorithm for perturb and observe technique is as follows:

(a) From the solar PV module, read the voltage V_{pv} and current I_{pv} values.

(b) From the measured I_{pv} and V_{pv}, the Power P_{pv} is calculated.

(c) At M^{th} instant, the value of power and voltage is saved.

(d) Repeat step next values at $(M+1)^{th}$ instant are measured.

(e) From M^{th} instant, voltage and power at $(M+1)^{th}$ instant are detracted with the values.

(f) It is inferred that in the correct hand side bend in the force voltage bend of the sun-based PV module where the incline of intensity voltage is negative ($dP/dV < 0$), and the voltage is practically consistent whereas in the left-hand side, the slant is positive ($dP/dV > 0$). In this way, the lower obligation cycle is the correct side of the bend and the higher obligation cycle is the left side bend.

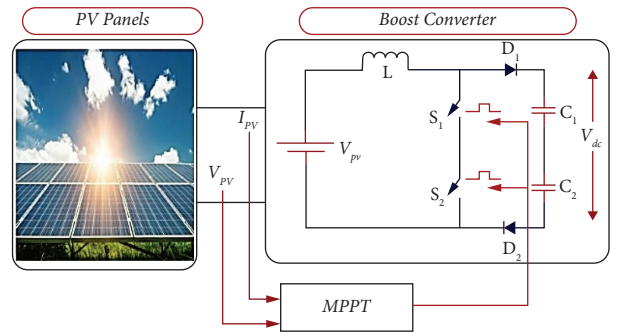

Figure 2: Solar powered 3-level boost converter.

(g) Contingent upon the sign of dV, for example, ($V(M+1) - V(M)$) and dP, for example, ($P(M+1) - P(M)$) regardless of whether to build the obligation cycle or to decrease the obligation cycle chooses after deduction of the calculation. Figure 3 shows the flowchart of perturb and observe algorithm. 1Soltech 1STH-215-P solar PV panel generates 60 V dc voltage with 5 A current, and by using a 3-level DC-DC boost converter, it will boost up the voltage 60 to 403 V dc with 4 A, and the simulation and experimental outcomes are shown in Figures 4 and 5, respectively. The simulation results of PV variation for several irradiances are presented in Figure 6, whereas the experimental results of PV irradiance are presented in Figure 7.

The efficiency of the converter during the irradiation condition is calculated as follows.

Equation (5) represents the output power relation of the PV system during irradiation conditions.

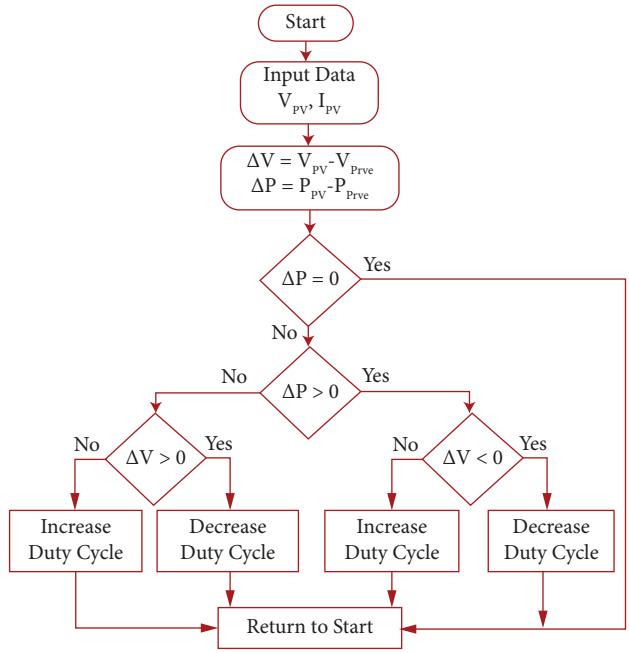

Figure 3: Flowchart of P&O (perturb and observe) algorithm.

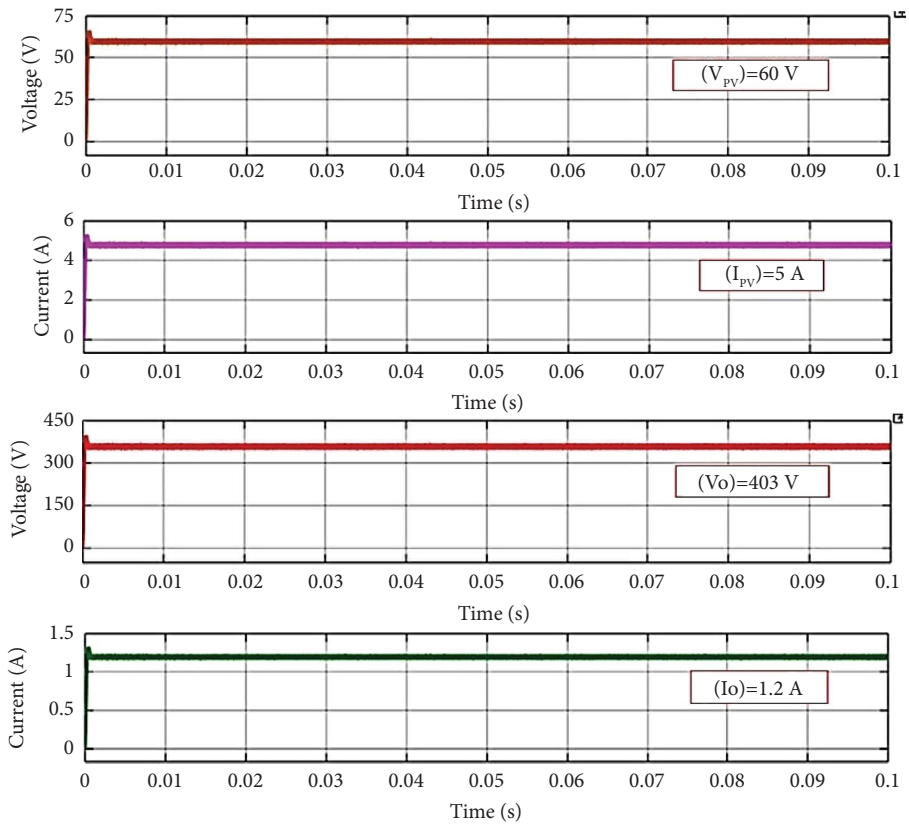

Figure 4: Proposed system simulation waveforms.

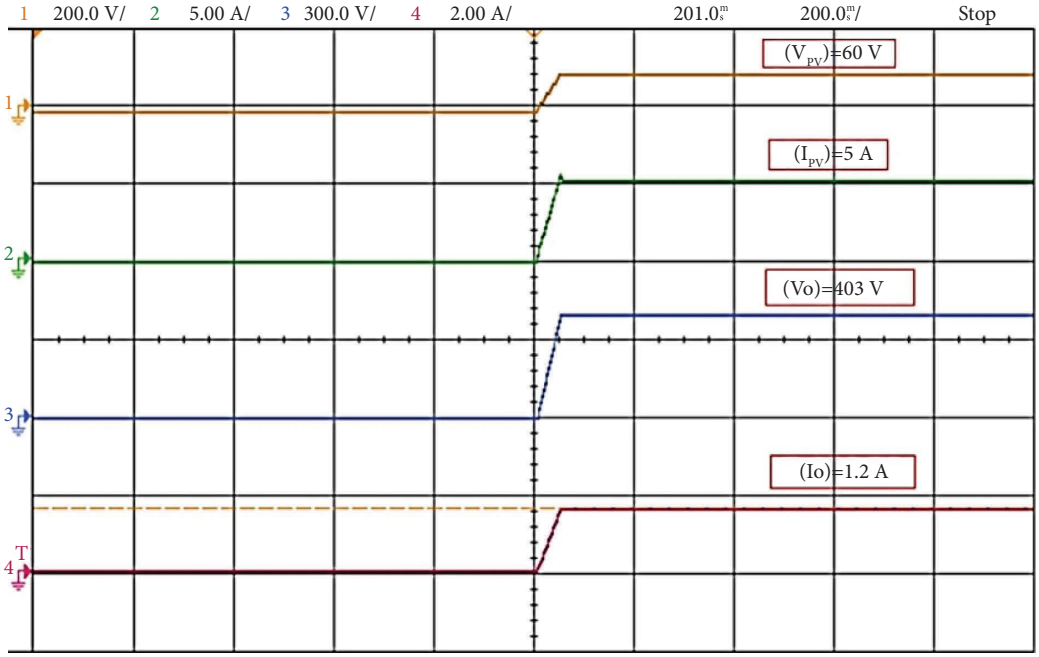

Figure 5: Proposed system experimental waveforms.

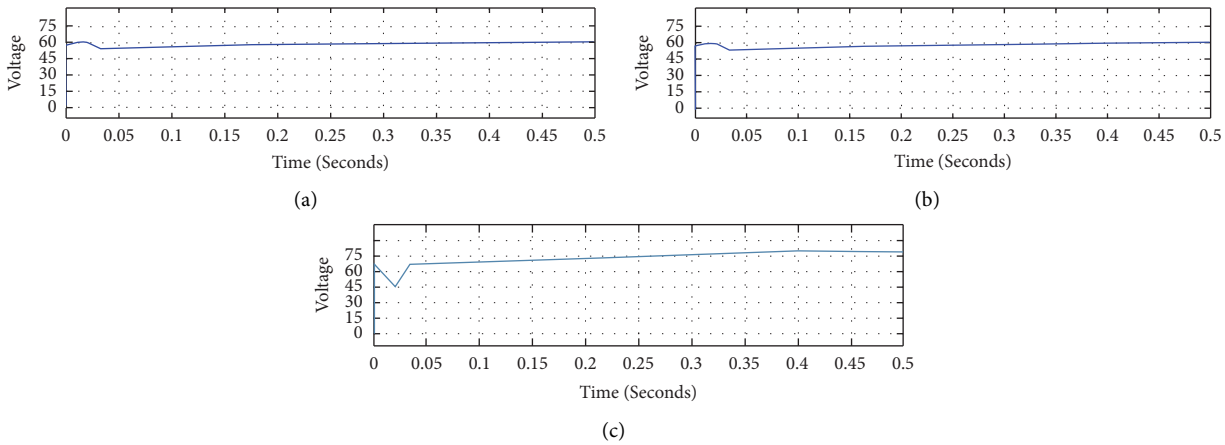

Figure 6: Simulation results of PV irradiance variation. (a) 490 W/m^2. (b) 660 W/m^2. (c) 1000 W/m^2.

$$P_{AC} = I_{rr} A_m \eta_m \eta_i p_{\text{loss}}, \tag{5}$$

where I_{rr} is the irradiance of the PV module (K_{wh}/m^2), A_m is the module (m^2), η_m is the module efficiency = (Output of module/1000 $*$ A_m) $*$ 100, η_i is the efficiency of the inverter = $(P_{\text{out}}/P_{\text{out}} + P_{\text{loss}})$, and P_{loss} is the converter loss = $P_c + P_s$.

Hence, during the irradiation of 1000 W/m^2 to 700 W/m^2, the efficiency is calculated from (5) and found to be 95.68%.

3. Implementation of CBH 27-Level MLI

The inverter is integrated with a boost converter with solar *PV* and electric vehicle applications to produce a pure sinusoidal waveform. The boost converter-based cascaded MLI is shown in Figure 8. The presentation of the cascaded MLI is discussed. The single-phase single bridge inverters are associated in a cascaded fashion giving cascaded MLI. In this analysis situs usually from various DC voltage buses, the desired voltage is appreciated. Considering the DC sources, the fell MLIs are considered into 2 kinds, deviated and symmetric inverters. In a symmetric sort, the voltage of the DC joins is held at a similar level.

The inconvenience of symmetric geography is that the expansion in voltage yield levels builds the number of switches. To overcome the above drawback, the DC buses supplied with unequal voltages are named asymmetric topology. The implemented 27-level MLI uses the asymmetric topology as presented in Figure 8. It contains 3 modules with 3 DC buses and each cell contains 4 switches. It is a mix of 3 single-stage *H*-connect inverters associated with the fell

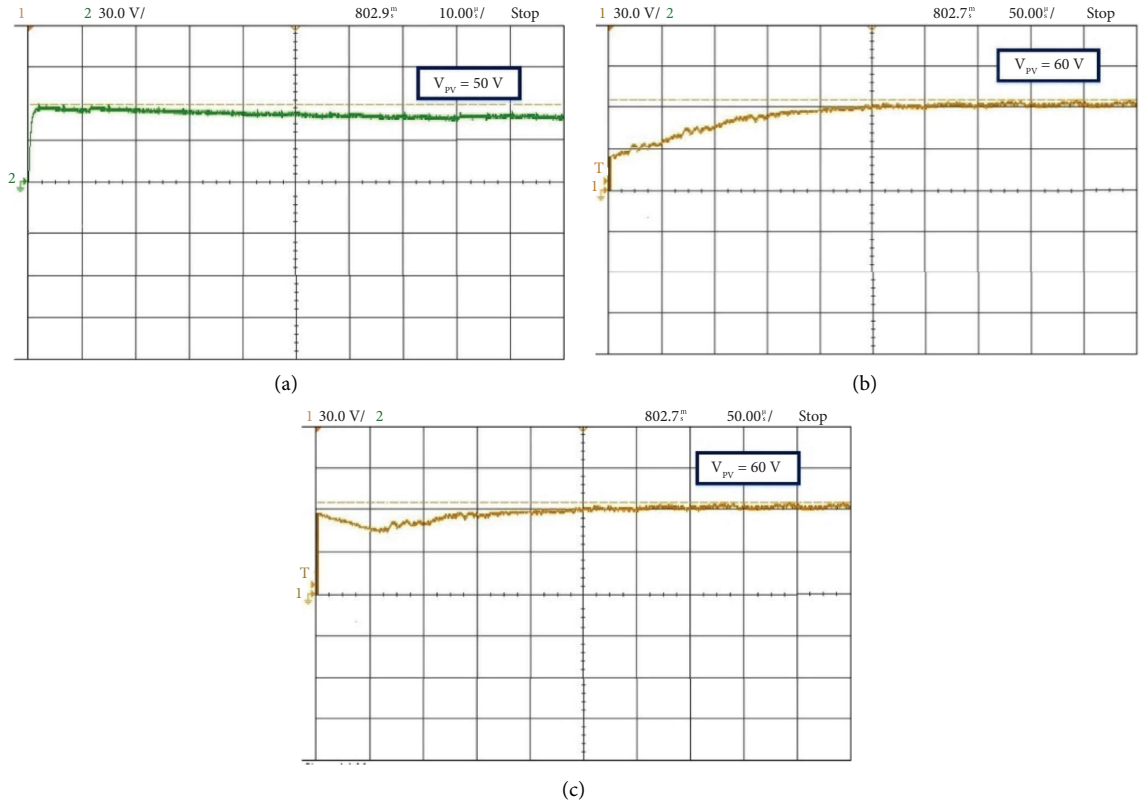

Figure 7: Experimental results of PV irradiance variation. (a) 490 W/m^2. (b) 660 W/m^2. (c) 1000 W/m^2.

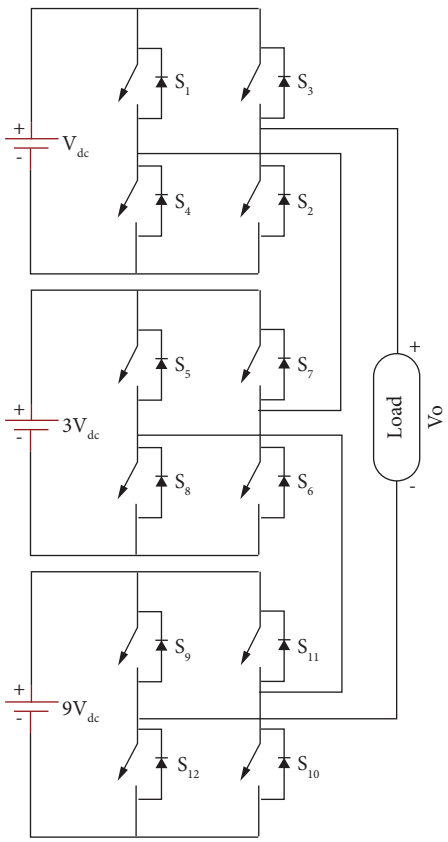

Figure 8: Cascaded H-bridge of 27-level MLI.

mode. The exchange plan for each single inverter cell is comparable to $S_1 = \overline{S_3}$ and $S_2 = \overline{S_4}$ from short-circuiting to avoid the circuit.

The power switches are MOSFETs or IGBTs as shown in Figure 8. The dc voltage is in the proportion of 1 : 3 : 9. A higher no of levels brings about expanded execution with more modest sounds. The benefits of fell staggered inverters are less number of DC sources, exchanging misfortunes, yield exchanging frequencies, decrease in cost, consonant levels, and expanded yield productivity. These wellsprings of DC are connected to a solitary stage H connect inverter, which creates the 3-levels of yield voltages such as follows+V_{dc}, 0, and $-V_{dc}$. The exchanging misfortunes in the framework depend on exchanging recurrence, which thusly is lesser due to the diminished voltage. This examination merges a mix of a few changes to propel the presentation of the inverter. In this technique, the various DC joins are associated with an association of 1 V, 3 V, 9 V... $3S-1$ V. A yield equivalent to $3S$ voltage levels are created by the inverter. A 27-level MLI is to create 27 distinctive voltage levels in the yield. The 27 levels in the yield waveform are ±13, ±12, ±11, ±10, ±9, ±8, ±7, ±6, ±5, ±4, ±3, ±2, ±1, and 0. By using the above equations, the implemented inverter number of switches and number of levels as well as peak PV output voltage can be attained.

3.1. Modes of Operation of 27-Level Cascaded H-Bridge MLI. For +1 V_{dc}, the PV output voltage level is +31 v which is generated by turning on switches S_1, S_2, S_6, S_8, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(a). For +2 V_{dc}, the PV output voltage level is +62 V which is generated by turning on switches S_3, S_4, S_5, S_6, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(b). For +3 V_{dc}, the PV output voltage level is +93 V which is generated by turning on switches S_2, S_4, S_5, S_6, S_{10}, and S_{12}, and that can be obtained at the load terminals as shown in Figure 9(c). For −1 V_{dc}, the PV output voltage level is −31 V which is generated by turning on switches S_3, S_4, S_6, S_8, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(d). For −2 V_{dc}, the output voltage level is −62 V which is generated by turning on switches S_1, S_2, S_7, S_8, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(e). For −3 V_{dc}, the output voltage level is −93 V generated with turning on switches S_2, S_4, S_7, S_8, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(f). Likewise, the remaining levels are followed by using switching (Table 3).

3.2. The Circuit Parameters are Determined for the Proposed 27-Level Topology. The cascaded 27-level inverter parameters such as the number of power switches, sources, voltage levels, and voltage can be estimated as follows.

The number of switches is required as follows:

$$N \text{ swicthes} = 2^m + 4, \tag{6}$$

where m = number of basic unit by considering here m value is 3, then

$$\begin{aligned} \text{swicthes} &= 2^3 + 4 \\ &= 12. \end{aligned} \tag{7}$$

The number of sources is required as follows:

$$N \text{ sources} = m. \tag{8}$$

By considering the m value is 3, then N sources = 3
The number of levels is obtained as follows:

$$N \text{ levels} = 3^m. \tag{9}$$

By considering the m value is 1, then N levels = 3^3 = 27
The output voltage of the 27-level is determined as follows:

$$V0 = \left[2^m + 5\right] * V\text{dc}. \tag{10}$$

By considering the m value is 3 and V_{dc} value is 31, then $V0 = [2^3 + 5] * 31 = 403$V.

The input supplies specified to the circuit are $V_{dc} = 403$ V to accomplish the decided pinnacle voltage of 403 V with the loads ($R = 100\,\Omega$ & 98 mH). The simulation output waveform of the cascaded H-bridge of 27-level MLI is shown in Figure 10. The switching table is shown in Table 3 for the conduction state of switches in 27-level MLI. By using the staircase modulation method, the implemented MLI, gate pulses are created for switches. It is calculated from MATLAB at 10 kHz of switching frequency. The transporter signal is related to a reference sign of 50 Hz. Figure 11 shows the yield voltage just as the current for 27-levels MLI. For the arrangement association, the voltage proportion is 1 : 3 : 9. The information that supplies the predefined voltages to the circuit is $V_{dc} = 31$ V, $V_{1dc} = 93$ V, and $V_{3dc} = 279$ V to accomplish the decided pinnacle voltage of 403 V with the ($R = 100\,\Omega$ & 98 mH) loads. The yield voltage of recreation yields current alongside THD as introduced in Figures 11 and 12.

4. Calculation of Reliability, TSV, Cost Function, Losses, and Efficiency

4.1. Losses and Efficiency. The misfortunes can be estimated by two methods; two significant misfortunes related to switches are exchanging misfortunes and misfortunes of conductions. The conductivity let-down of IGBTs can be overcome [20, 21].

$$Q_{\text{Cl,IGBT}(t)} = \left[V_{\text{IGBT}} + R_{\text{IGBT}} i^{\beta}\right] i(t), \tag{11}$$

where V_{IGBT} is the drop in forwarding voltage of the IGBT, and the drop in forwarding voltage of the diodes is V_d. R_{IGBT} is the equivalent resistance of the IGBTs, and the equivalent resistance of the diodes is R_d, and β is a constant with IGBT specification favors. The normal estimation of the MLIs conductive force misfortune (Q_{cl}) can be given as follows [20, 21] as N_d diodes and N_{IGBT} transistors are present in the current path at a time t [20, 21].

$$Q_{\text{Cl}} = \frac{1}{2\pi} \int_0^{2\pi} \left[N_{\text{IGBT}}(t) Q_{\text{cl,IGBT}}(t)\, \mathrm{d}t\right]. \tag{12}$$

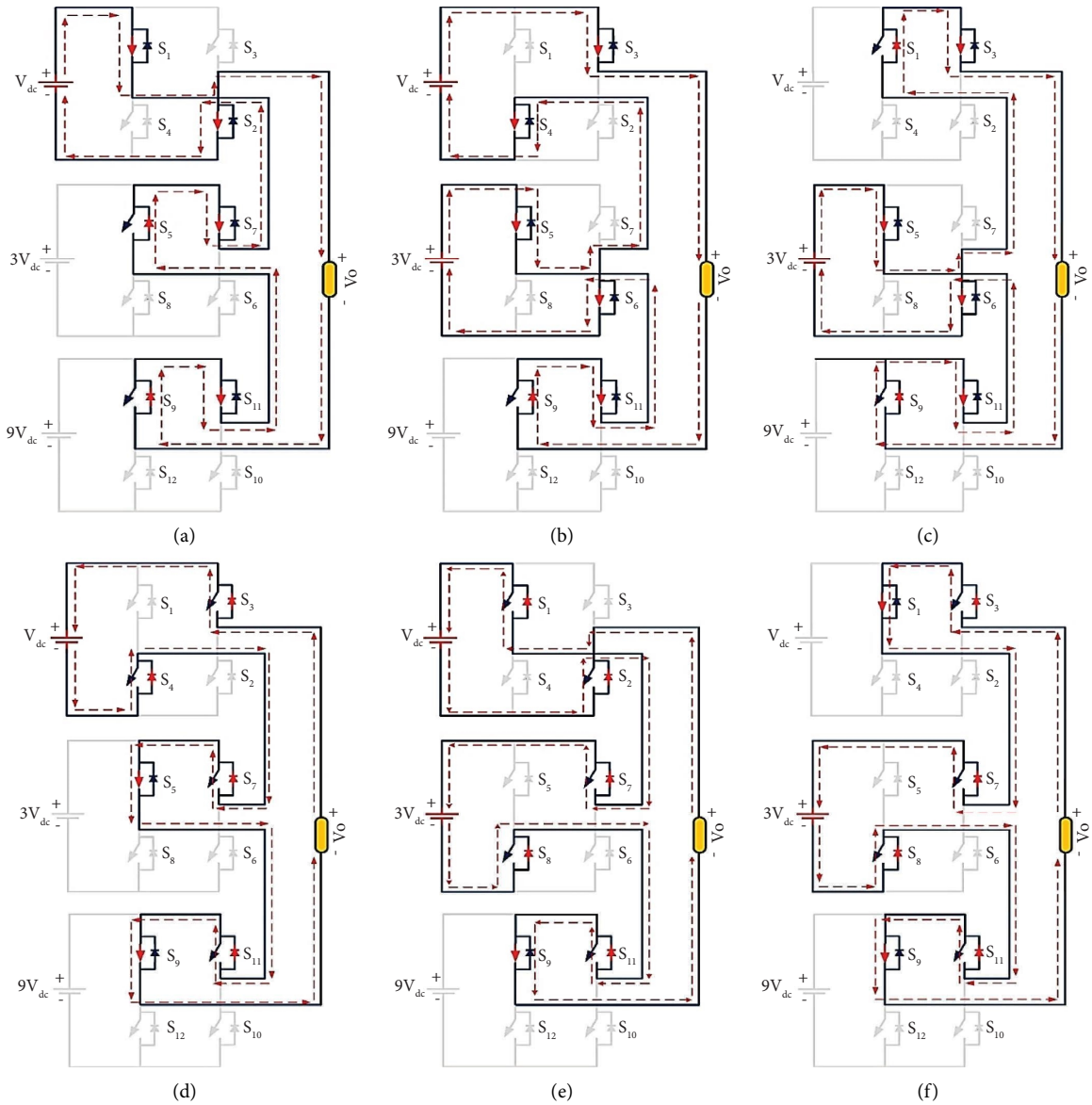

Figure 9: (a–f). Modes of operation of cascaded H-bridge of 27-level MLI.

Table 3: Switching states (ON) of 27-level MLI.

Modes	ON states of switches
0	$S_1, S_3, S_5, S_7, S_9, S_{11}$
1	$S_1, S_2, S_5, S_7, S_9, S_{11}$
2	$S_3, S_4, S_5, S_6, S_9, S_{11}$
3	$S_1, S_3, S_5, S_6, S_9, S_{11}$
4	$S_1, S_2, S_5, S_6, S_9, S_{11}$
5	$S_3, S_4, S_7, S_8, S_9, S_{10}$
6	$S_1, S_3, S_7, S_8, S_9, S_{10}$
7	$S_1, S_2, S_7, S_8, S_9, S_{10}$
8	$S_3, S_4, S_5, S_7, S_9, S_{10}$
9	$S_1, S_3, S_5, S_7, S_9, S_{10}$
10	$S_1, S_2, S_5, S_7, S_9, S_{10}$
11	$S_3, S_4, S_5, S_6, S_9, S_{10}$
12	$S_1, S_3, S_5, S_6, S_9, S_{10}$
13	$S_1, S_2, S_5, S_6, S_9, S_{10}$
−1	$S_3, S_4, S_5, S_7, S_9, S_{11}$
−2	$S_1, S_2, S_7, S_8, S_9, S_{11}$
−3	$S_1, S_3, S_7, S_8, S_9, S_{11}$
−4	$S_3, S_4, S_7, S_8, S_9, S_{11}$
−5	$S_1, S_2, S_5, S_6, S_{11}, S_{12}$
−6	$S_1, S_3, S_5, S_6, S_{11}, S_{12}$
−7	$S_3, S_4, S_5, S_6, S_{11}, S_{12}$
−8	$S_1, S_2, S_5, S_7, S_{11}, S_{12}$
−9	$S_1, S_3, S_5, S_7, S_{11}, S_{12}$
−10	$S_3, S_4, S_5, S_7, S_{11}, S_{12}$
−11	$S_1, S_2, S_7, S_8, S_{11}, S_{12}$
−12	$S_1, S_3, S_7, S_8, S_{11}, S_{12}$
−13	$S_3, S_4, S_7, S_8, S_{11}, S_{12}$

Because of the energy the exchanging misfortunes can be assessed used during turn-off and turn-on cycles in the switches, it is esteemed dependent on straight contrasts of the exchanging voltage and current [20, 21]. The energy value could be as follows:

$$\begin{aligned} \mathrm{Em}_{\mathrm{on},l} &= \int_o^{t_{\mathrm{on}}} v(t) i(t) \\ &= \frac{1}{6} V_{\mathrm{switch},l} I' t_{\mathrm{on}}, \end{aligned} \tag{13}$$

$$\begin{aligned} \mathrm{Em}_{\mathrm{off},l} &= \int_o^{t_{\mathrm{off}}} v(t) i(t) \\ &= \frac{1}{6} V_{\mathrm{switch},l} I' t_{\mathrm{off}}, \end{aligned} \tag{14}$$

where $\mathrm{Em}_{\mathrm{off}}$ and $\mathrm{Em}_{\mathrm{on}}$ are the turn-on and turn-off misfortunes with l. The misfortunes from exchanging are comparable to the amount of the misfortunes from turn-off and turn-on energy, esteemed as follows:

$$Q_{\mathrm{Sl}} = f \sum_{\mathrm{l}=1}^{M_{\mathrm{switch}}} \left[\sum_{s=1}^{M_{\mathrm{on,l}}} \mathrm{Em}_{\mathrm{on,ls}} + \sum_{s=1}^{M_{\mathrm{off},l}} \mathrm{Em}_{\mathrm{off,ls}} \right]. \tag{15}$$

The total loss of power was valued as follows:

$$P_{\mathrm{Totallosses}} = Q_{\mathrm{cl}} + Q_{\mathrm{sl}}. \tag{16}$$

The inverter efficiency (η) is given as follows:

$$\begin{aligned} \eta\% &= \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} \\ &= \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{losses}}}, \end{aligned} \tag{17}$$

where P_{in} and P_{out} correspond to the input and output power.

The power output can be assessed in the following way:

$$P_{\mathrm{out}} = V_{\mathrm{rms}} * I_{\mathrm{rms}}. \tag{18}$$

The experimental power output of 718.7 W for twenty-seven-level inverters is obtained using (14) ($V_{\mathrm{rms}} = 282.84$ V and $I_{\mathrm{rms}} = 2.828$ A). The parameter values for calculation are collected from the IGBT CM7FDU datasheet. From the performance characteristics plot the R_{IGBT} is 0.4 and V_{switch} value (0.6 V) is taken, 200 ns turn-off delay, 100 ns turn-off, 250 ns turn-off, and 12 switches turn-off as 300 ns. The proposed inverter design will cover 53 steps in one complete cycle [20, 21]. The losses from the conduction are calculated using equation (9).

$Q_{\mathrm{cl}} = 58.75$ W and $\mathrm{Em}_{\mathrm{off}}$ and $\mathrm{Em}_{\mathrm{on}}$ are calculated from equations (13) and (14). $\mathrm{Em}_{\mathrm{off}} = 0.254$ W and $\mathrm{Em}_{\mathrm{on}} = 0.127$ W.

The switching losses are designed as follows:

$Q_{\mathrm{sl}} = 0.381$ W, total losses are designed using (16) during switching and lead time.

$$\begin{aligned} P_{\mathrm{Totallosses}} &= 58.75 + 0.381 \\ &= 59.131\mathrm{W}. \end{aligned} \tag{19}$$

The η (efficiency) is designed by utilizing equation (17):

$$\begin{aligned} \eta\% &= \frac{718.7}{718.7 + 59.131} \times 100 \\ &= 92.38\%. \end{aligned} \tag{20}$$

The above calculations guarantee the proposed 27-inverter efficiency at 92.38 percent.

4.2. Total Standing Voltage (TSV). The standing voltage of the inverter is estimated using the following equations:

$$\begin{aligned} \mathrm{TSV} &= \sum_{i=1}^{n} V_{SWi}, \\ \mathrm{TSV} &= 2\left(V_{\mathrm{dc}}\right) + 2\left(3V_{\mathrm{dc}}\right) + 2\left(9V_{\mathrm{dc}}\right), \\ \mathrm{TSV} &= 26V_{\mathrm{dc}}, \\ \frac{\mathrm{TSV}}{L} &= \frac{26V_{\mathrm{dc}}}{27} \\ &= 0.962\frac{V_{\mathrm{dc}}}{L}, \\ \text{Total Blocking Voltage} &= V_{\mathrm{dc}} + 3V_{\mathrm{dc}} + 9V_{\mathrm{dc}} \\ &= 13V_{\mathrm{dc}}. \end{aligned} \tag{21}$$

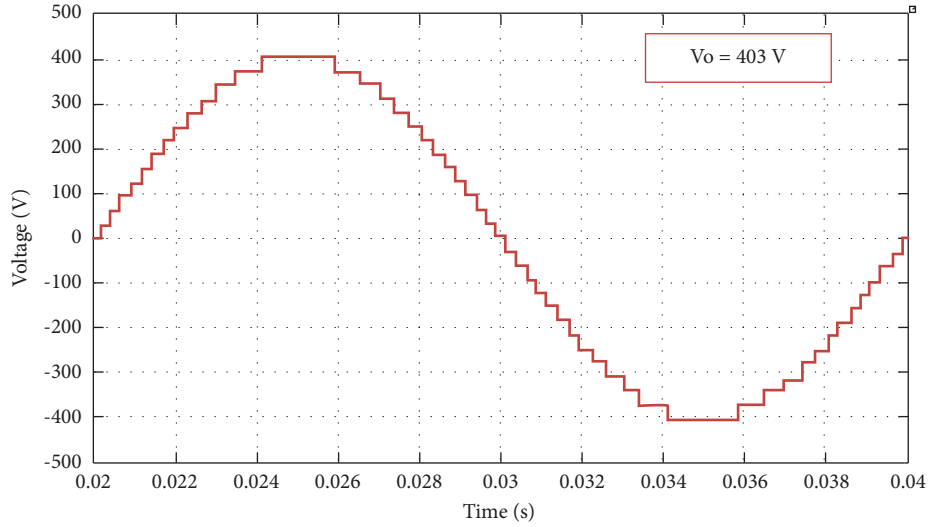

Figure 10: Simulation output waveform of the cascaded H-bridge of 27-level MLI.

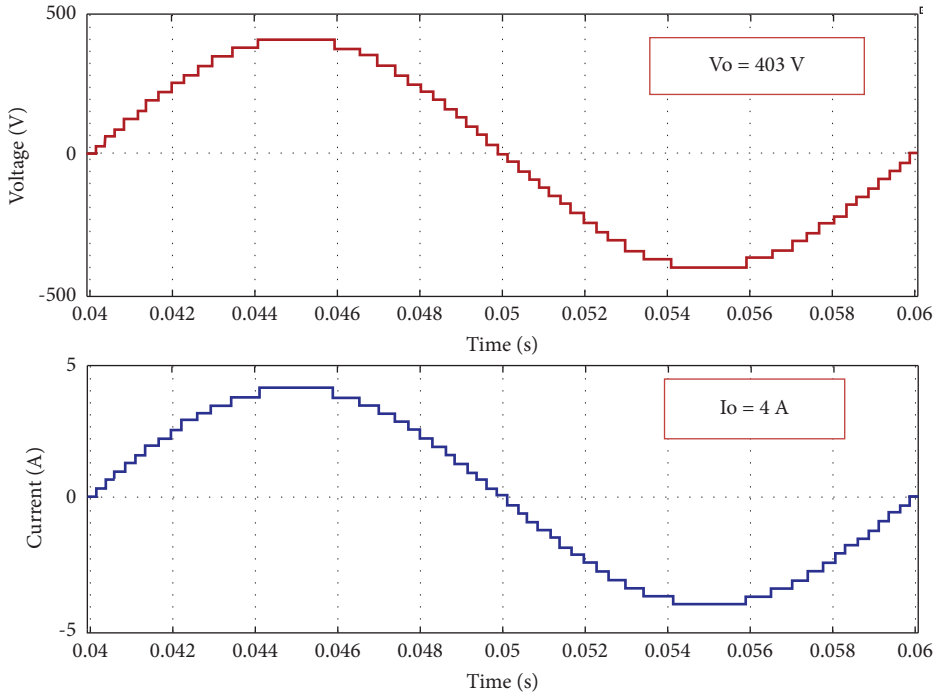

Figure 11: Simulation of 27 output voltage and output current of the inverter.

In open-circuit conditions, the switches will block the voltages of blocking voltages of switches [37];

$$\begin{aligned} &S_1, S_2, S_3 \text{ and } S_4 \text{ is } V_{\text{dc}}, \\ &S_5, S_6, S_7 \text{ and } S_8 \text{ is } 3V_{\text{dc}}, \\ &S_9, S_{10}, S_{11} \text{ and } S_{12} \text{ is } 9V_{\text{dc}}. \end{aligned} \tag{22}$$

Blocking voltages across the switches are as follows:

$$\begin{aligned} S_1 &= S_2 \\ &= S_3 \\ &= S_4 \\ &= \frac{V_{\max}}{V_{\text{block}}} \\ &= \frac{13V_{\text{dc}}}{V_{\text{dc}}} \\ &= 13V, \\ S_5 &= S_6 \\ &= S_7 \\ &= S_8 \\ &= \frac{V_{\max}}{V_{\text{block}}} \\ &= \frac{13V_{\text{dc}}}{3V_{\text{dc}}} \\ &= 4.33V, \\ S_9 &= S_{10} \\ &= S_{11} \\ &= S_{12} \\ &= \frac{V_{\max}}{V_{\text{block}}} \\ &= \frac{13V_{\text{dc}}}{9V_{\text{dc}}} \\ &= 1.44V. \end{aligned} \tag{23}$$

The total voltage blocked across the switches as follows:

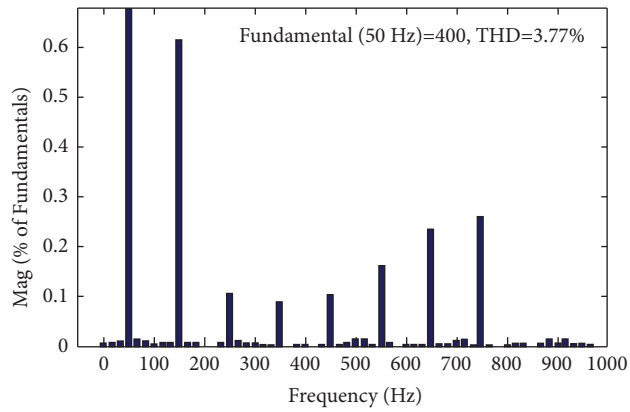

Figure 12: 27-level multilevel inverter simulation THD.

$$\begin{aligned} \text{TSV} &= 4(13) + 4(4.33) + 4(1.44) \\ &= 75.08V, \\ V_{\text{Switch}}^{p.V} &= \frac{\text{Total Voltage}}{\text{Max voltage}} \\ &= \frac{75.08}{13} \\ &= 5.77. \end{aligned} \tag{24}$$

4.3. Cost Function (CF). The cost function of the inverter is estimated using the following equation [37].

$$\text{The Cost Function } CF = N_{\text{SW}} + \alpha V_{\text{Switch}}^{p.V}, \tag{25}$$

where the N_{sw} is the switches count, α is the weighting coefficient, and V_{switch} is the voltage across the switch.

The inverter estimated cost function is tabulated in Table 4.

4.4. Reliability Calculation of the Inverter. The mean time to failure rate (MFFT) is important for the inverters; the reliability analysis is presented for the proposed system. The total MTTF of power electronic circuits can be calculated by estimating the total failure rate (FR) value of the circuit elements that are present [38]. The total FR and λ_T, are calculated by multiplying the number of components, such as switches and diodes by their corresponding FR values.

$$\lambda_T = (\lambda_{PS} * N_{\text{SW}}) + (\lambda_{\text{PD}} * N_D). \tag{26}$$

The total MTTF of the power electronic circuit can be derived from following equation:

Table 4: Cost function.

∝	CF	CF/L
0.5	14.885	0.55
1.5	20.655	0.76
2.5	26.425	0.97
3.5	32.195	1.19

$$\mathrm{MTTF}_T = \frac{1}{\lambda_T}. \tag{27}$$

The MTTFT of the electronic circuits can be calculated based on the number of device counts.

The inverter has 12 switches (N_{SW}) and 12 diodes, respectively, and the total failure rate (FR) and mean time to failure rate (MFFT) are estimated using (26) and (27).

$$\begin{aligned} \mathrm{FRT} &= 0.0000042, \\ \mathrm{MTTFT} &= 238095.2. \end{aligned} \tag{28}$$

5. Comparative Analysis

A boost converter-based CHB staggered inverter is proposed for the utilization of extracted PV energy. The solar photovoltaic is connected to the boost converter, and it enhanced voltage from PV output voltage 60 V to 403 V with the help of the MPPT technique. The boosted output voltage is higher compared to existing converters [22–25] as shown in Table 5 and Figure 13 shows the comparison of the proposed converter with existing converters. The output of the implemented 27-level CBH multilevel inverter has fewer switching losses as well as switch count compared with the existing topologies [26–30] as shown in Table 6 and comparison is shown in Figure 14. As experimental voltage value adapts to disorient situations of injected voltage and power. The inverter which is a linked *PV* module can be a unit with reduced power losses as it consists of fewer driver circuits. This study reports a 27-level inverter using just helped voltage got from a sustainable power source. The inverter proficiency is high and the yield voltage waveform is entirely sinusoidal. The expense is little as the number of intensity switches used is 12. The power switches are reduced apparently due to a reduced number of power driver circuits, also low transmission losses than traditional inverter modules. Expanding the degree of the inverter can get a few points of interest: get a decent voltage wave structure and very low THD 3.77% which is achieved through the experiment as shown in Figure 15. The comparison of implemented inverter THD values with existing topologies. The conventional MLIs are compared with 27MLI is tabulated in Table 7 and Figure 16 shows the comparison of implemented MLI with the conventional MLIs. The reliability analysis conducted for the inverter with existing MLIs is shown in Table 8. The inverter has reliability when compared to existing MLIs in all aspects as shown in Figure 17. The references [26, 27, 29] have less THD compared with the proposed MLI but the MBV of the other topologies are high whereas the MBV of the proposed topology is less, which results in the added advantage of the topology.

Table 5: Comparison of the proposed converter with existing converters.

References	Input voltage (V)	Output voltage (V)
[22]	18	42
[23]	36	60
[24]	12	14.5
[25]	600	700
Proposed method	60	403

6. Experimental Results

The extracted PV two voltages and one programmable DC source are fed to the 27 MLI. The 27-level MLI equipment model setup was used in the model scale and tried tentatively. The social occasion of Simulink block bunches into dSPACE RTI 1104 computerized input/output ports are performed, and the flight of stairs tweaks PWM technique execution in MATLAB/Simulink is performed. To rearrange continuous interfacing applications, by the computerized I/O ports, the 20 yield pins are controlled. From the dSPACE RTI1104, the TLP 250 driver is separated to include, is the beat made. The experimental twenty-seven output waveform is shown in Figure 18(a). The consistent state testing checks with R-load with 400 V alongside the current yield are accomplished with 4 A. Yield current and voltage RMS esteems were to start with 282.84 V and 2.828 A, correspondingly. The staging point between the heap current and the heap voltage is zero, as appeared in the waveform. Consistent state testing with an R-load, competition after here gave the L-load 403 V and 3.4 A, correspondingly, and relating RMS esteems were achieved with 284.96 V and 2.404 A, correspondingly. The output voltage and currents are 403 V and 2.3 A, and the RMS values are 284.96 V and 1.626 A, correspondingly obtained investigational results are given in Figures 18(b)–18(d). The investigational results check at consistent state, load aggravation conditions, executed with R to L load as appeared in Figure 19, executed with L to R load as appeared in Figure 20, correspondingly. In assurance, stacks infrequently happen particularly and they will surely occur in a blend of resistive and inductive burdens. Generally, in a particular spot, when an R (resistive) load is by and by working an unexpected collection of L (inductive)-load corresponding to the R load or the other way around is indistinguishable likely. Figure 21 shows the experimental results of the 27-level multilevel inverter THD trial voltage is 4.02%. The proposed system hardware setup is shown in Figure 22. The experimental output parameters are shown in Tables 9 and 10.

The actualized inverter created a higher number of voltage yield levels with a less number of equipment components and low THD values. Similar aftereffects of the trial have appeared in Tables 9 and 10. The experimental setup component details are mentioned in Table 11.

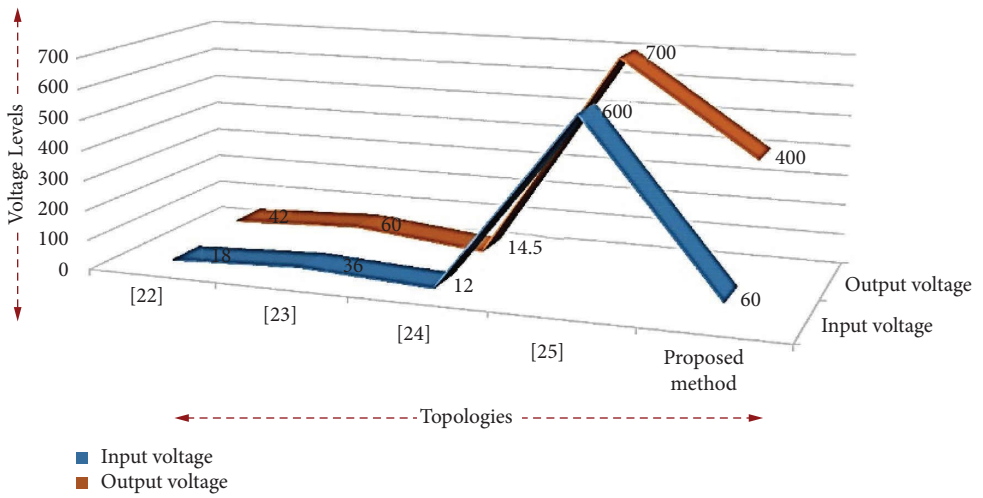

Figure 13: Comparison of the proposed converter with the existing converters.

Table 6: Comparison of implemented MLI with active MLIs.

MLIs	No. of levels	No. of switches	No. of sources	Diodes	(%) THD	(%) Efficiency
[26]	27	12	3	12	1.248	—
[27]	27	13	1	13	2.74	—
[28]	27	12	3	12	13.75	—
[29]	27	13	3	13	2.68	—
[30]	27	36	3	36	5.87	—
[42]	27	14	5	14	2.037	—
27-Level MLI	27	12	3	12	3.77	92.38

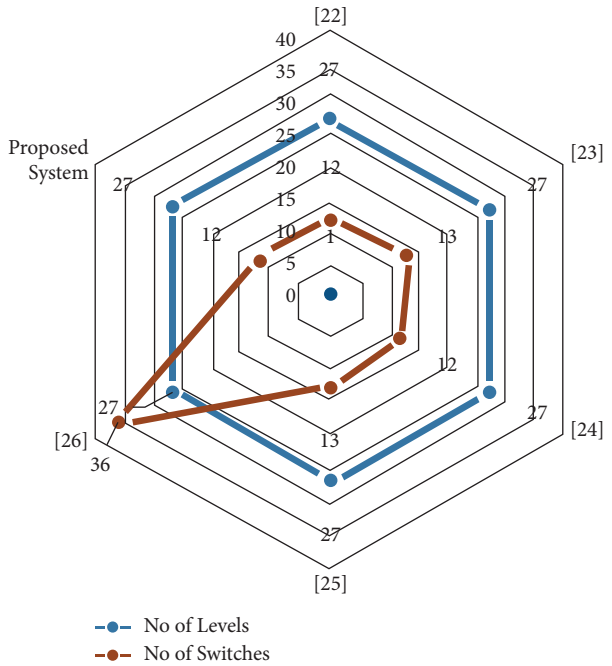

Figure 14: Comparison of implemented inverter levels and switches with the existing topologies.

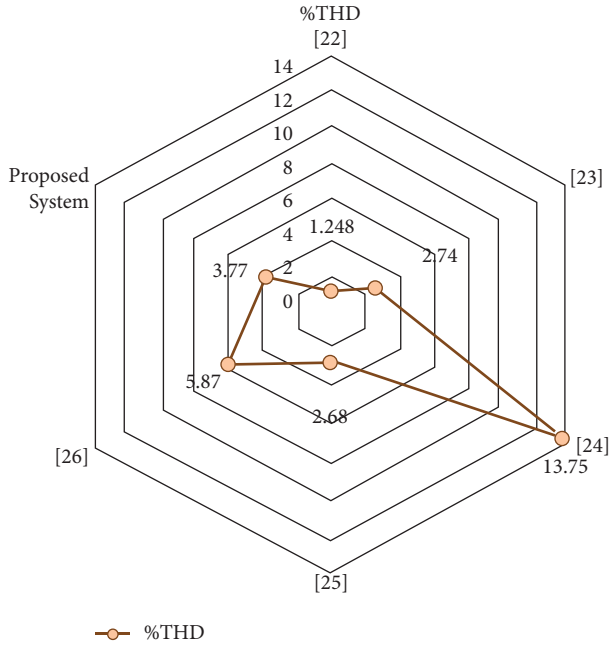

Figure 15: Comparison of implemented inverter THD values with existing topologies.

Table 7: Comparison of implemented MLI with the conventional multilevel inverters.

Required items	CMLI	DCMLI	FCMLI	Proposed MLI
No of levels	27	27	27	27
No of switches	52	52	52	12
Diodes	52	52	52	12
Clamping diode	0	650	0	0
Dc bus capacitor	13	26	26	0
Balancing capacitor	0	0	325	0
Gate-amp	52	52	52	12

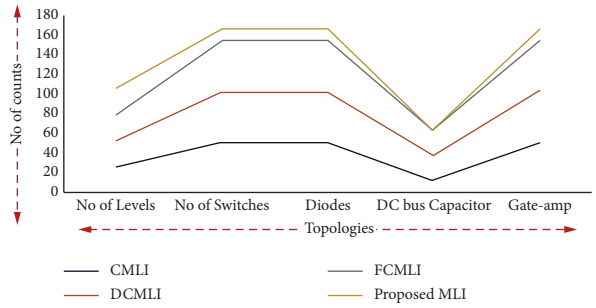

Figure 16: Comparison of implemented MLI with conventional MLIs.

Table 8: Comparison of topologies based on reliability aspects.

Topology	N_{SW}	N_D	FR_T	$MTTF_T$
[26]	12	12	0.0000042	238095.2
[27]	13	13	0.00000455	219780.2
[28]	12	12	0.0000042	238095.2
[29]	13	13	0.00000455	219780.2
[30]	36	36	0.0000126	79365.08
Proposed system	12	12	0.0000042	238095.2

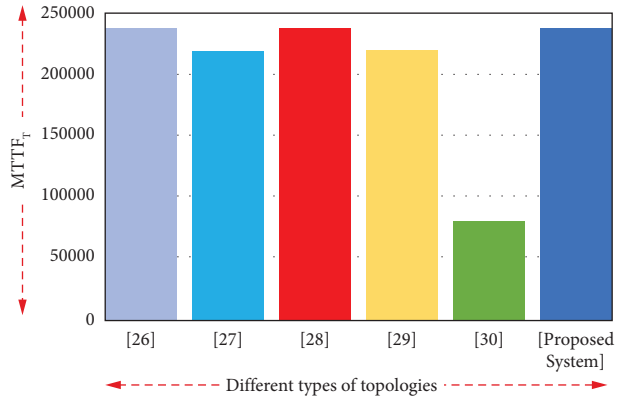

Figure 17: Comparison of topologies based on reliability aspects.

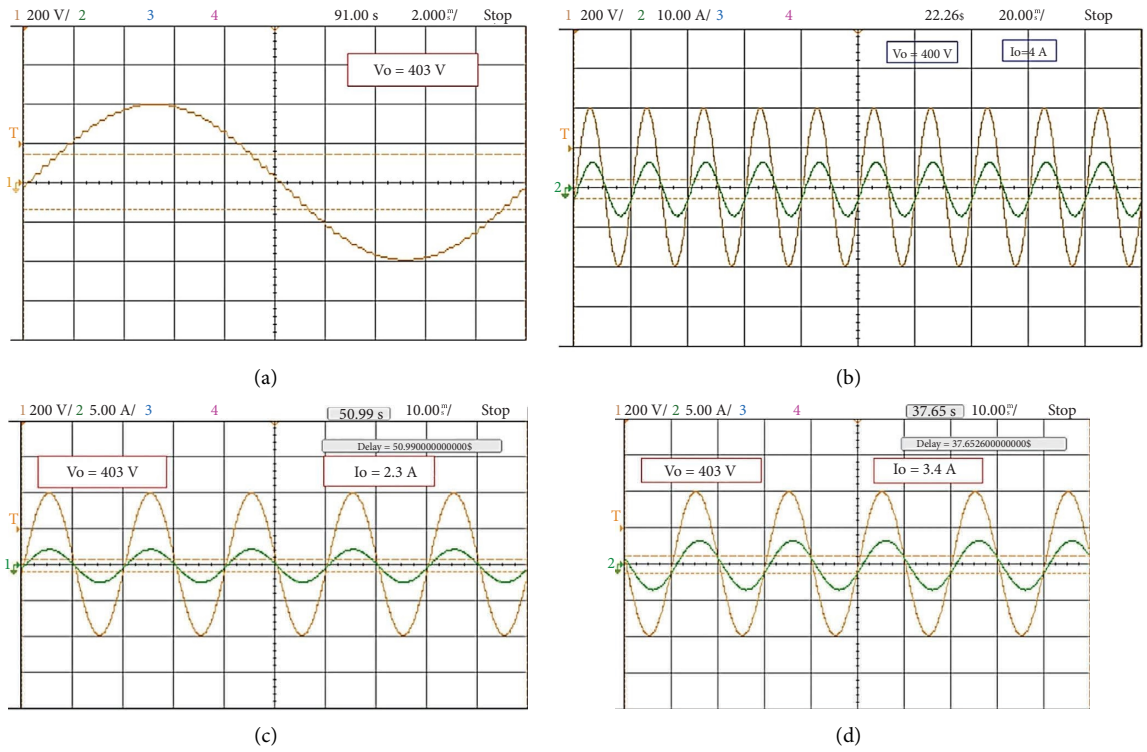

Figure 18: (a) O/P voltage of the actualized inverter. (b) O/P current and voltage of inverter with R load (c) O/P current just as the voltage of the inverter with engine load (d) O/P current and voltage of the inverter with L load.

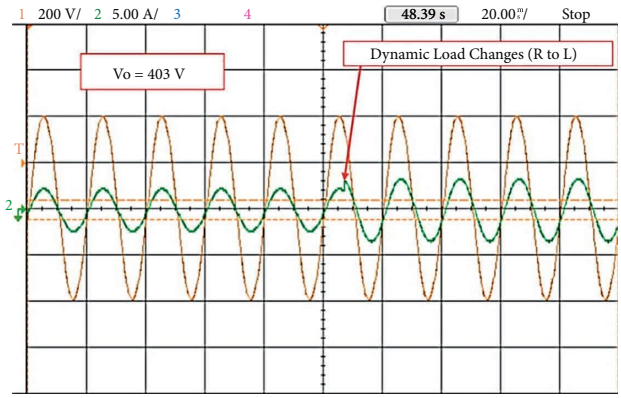

Figure 19: 27-level multilevel inverter dynamic (R to L) loads changes.

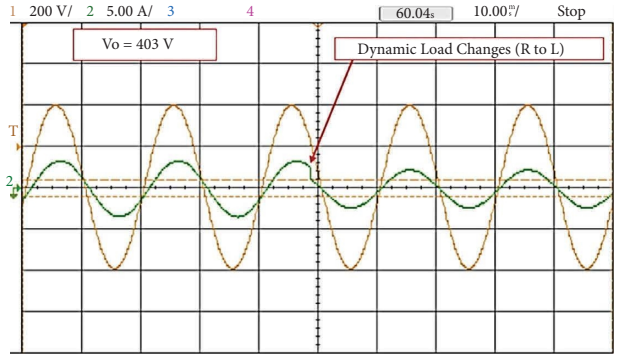

Figure 20: 27-level multilevel inverter dynamic (L to R) loads changes.

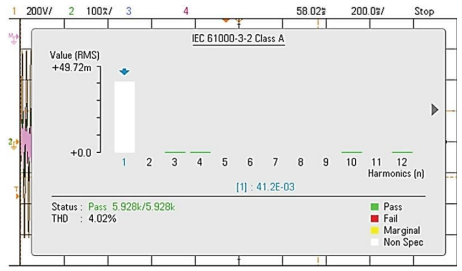

Figure 21: Experimental results of 27-level multilevel inverter THD value.

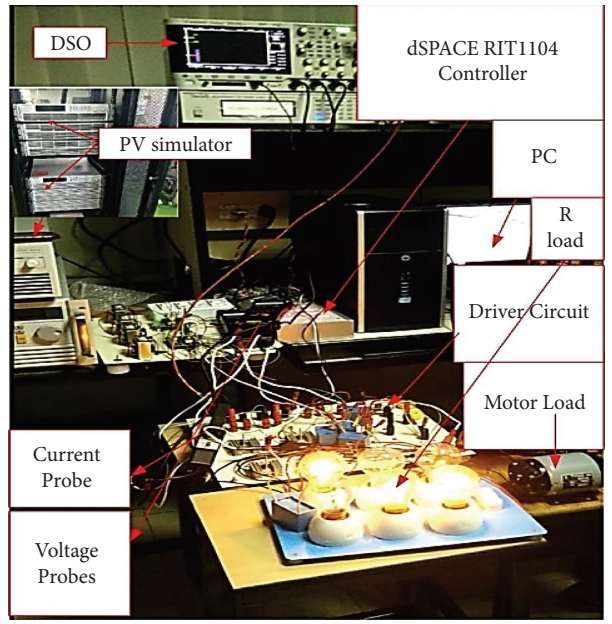

Figure 22: Proposed system hardware setup.

Table 9: Output experimental parameters of 27 MLI.

Inverter type	27 MLI	27 MLI	27 MLI
Load	R (ohms)	L (henry)	Motor (henry)
I_0 (A)	4	3.4	2.3
I_{rms} (A)	2.828	2.404	1.626
V_0 (V)	403	403	403
V_{rms} (V)	284.96	284.96	284.96
P_0 (w)	799.871	679.94	459.89
THD (%)	3.77	3.77	3.77

Table 10: Comparison of experimental and simulation of implemented 27 MLI.

Items	Implemented 27 MLI simulation results	Implemented 27 MLI experimental results
I_0 (A)	4	4
THD	3.77	4.02
V_0 (V)	403	403

Table 11: Experimental specifications.

Sl. no.	Elements	Specifications
1	Inductor	175 mH
2	Programmable-DC sources	500 Volts
3	Driver circuit	TLP250
4	Motor load	0.5 Hp 1-Φ (373 W, 0.75 PF, 230 V)
5	dSPACE controller	RTI1104
6	IGBTs (CM75DU-12H)	75 A, 600 V
7	Resistor	100 Ohms

7. Conclusion

In this study, a boost converter-based CHB staggered inverter for solar PV applications is implemented. Solar PV is associated with the lift converter and improved voltage from PV yield voltage 60 V to 403 V with the help of the MPPT method. The inverter is integrated with a boost converter with solar *PV* applications to generate a pure sinusoidal waveform. A 27-level CHBMLI is implemented with reduced power losses and lower THD. The 27-level topology has been planned and afterward reenacted in MATLAB/Simulink, and it uses 12 switches and three voltage sources to develop 27-level voltage sources THD for 27 levels is 3.77% and efficiency is 92.38%. The inverter has lower TSV, is cost-effective, and has improved reliability. Finally, a detailed comparison with the existing system is given focusing on the advantages of the proposed converter and implementation for the 27-level inverter. The proposed topology is limited to medium-power devices with a restricted number of levels. The proposed system is well suited for electric vehicles and grid-connected applications and FACTs [8].

Data Availability

The data used to support the findings of this study are included in the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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Research Article

Dynamic Performance Improvement of a Single-Phase VSI with Digital Implementation of an On-Line Optimal Trajectory Control Algorithm

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A single-phase voltage source inverter (VSI) still suffers from a long settling time and significant voltage overshoot/undershoot under the abrupt step-change of load current. This article analyzes the comprehensive large-signal dynamic process and limitation of the linear controller during step change in load current. The combination of linear and nonlinear control is presented which is a realistic, simple, and low-cost technique for enhancing the dynamic response of the single-phase VSI. A nonlinear controller based on the simplified capacitor charge balance algorithm is employed to drive the inductor current and capacitor voltage to attain the target value by precisely following the projected optimal trajectory during the transient process in a brief period. A linear PI controller is utilized during the steady-state operations such as input voltage variations, temperature drifts, and component ageing. The complete mathematical derivation as well as a design method is presented to guide the practical hardware implementation for the given main circuit parameters and identified load step change. Even though accurate time instants can be obtained using off-line numerical calculations, reasonable simplifications are provided for real-time practical engineering applications in DSP. Finally, simulation and experimental verifications prove that the single-phase VSI achieves a substantial settling time decrease and reduced voltage oscillations.

1. Introduction

Single-phase alternating current power supplies are commonly used in applications such as active power filters, solar power generating systems, and laboratory testing, including power equipment research and development and electrical manufacturing. When delivering a load that fluctuates too quickly between many steady-state locations, most single-phase VSIs still have a lengthy settling period and severe voltage overshoot/undershoot. Under a 10% to 80% load step change, the usual transient recovery time is larger than 2 ms, which does not match the high-precision test requirement. As a result, significant research efforts have been directed into improving the dynamic performance of high-precision single-phase AC power sources delivering the impact load in recent years [1, 2].

Traditional linear control techniques, such as PI and PR [3–7], are best suited for situations with gradual load changes. However, in applications that need quick and precise current monitoring, the dynamic response of these kinds of current controllers is often poor. A nonlinear control technique is intensively investigated to increase the dynamic performance because it responds too rapidly to transients. Nevertheless, the majority of them may lead to undesirable performance, such as nonzero steady-state error and varying switching frequency. For example, the critical parameters of deadbeat [8] are developed considering the particular information of load conditions. It is challenging to calculate these characteristics when there are large fluctuations in the load. The hysteresis control [9–11] provides virtually instantaneous reference tracking and is impervious to instability problems but at the expense of variable switching frequency and higher control complexity. Dead

time affects current-tracking precision, switching frequency, and duty cycle range for parabolic current-controlled VSIs [12, 13]. The advantages of sliding mode control (SMC) [14–16] include rapid dynamic reaction, rejection of external disturbances, and insensitivity to parameter fluctuations. However, it is difficult to obtain a suitable sliding surface. In addition, boundary control (BC) [17–19] and H-infinity [20] are options for enhancing the dynamic performance. BC and H-infinity are effective but hard to implement.

Combining linear and nonlinear control techniques (PI + non-linear) is used to fully use their benefits, using a nonlinear controller during the transient and a linear controller in the steady state to speed up the transient behaviour and preserve strong steady-state performance. This nonlinear control approach forecasts the best trajectory for single-phase inverters under varying loads. It determines the appropriate switching sequences to force the converter to move from one steady state to another to regain lost charge. This can be performed by fixing the duty cycle high (for a step-up change) and low (for a step-down change) for a specified interval and followed by low (for a step-up change) and high (for a step-down change) for the additional interval. Thus, the controller enhances the dynamic response (reduced settling time and minimal output voltage undershoot/overshoot) undergoing fast load changes.

In the literature [21, 22], a straightforward design strategy for traditional DC-DC converters was given. The capacitor charge balance control (CBC) method is used to calculate the on- and off-state time intervals of power devices [21, 23–31]. It has been shown that the quickest transient response may be attained in a single switching period. And its fundamental concept is to estimate the ideal dynamic trajectory and establish the precise switching sequence of the power device to drive the converter from one steady-state to another in response to rapid load shift. Under conditions of rapid load changes, the single-phase VSI's output voltage and inductor current fluctuate frequently. As a result, enhanced CBC is offered since the traditional CBC strategy cannot be utilized to the single-phase VSI to boost dynamic response. This article first analyzes the comprehensive large signal dynamic model and transient response limitation of the single-phase VSI in Section 2. Section 3 proposes an online trajectory approach for properly monitoring the projected ideal trajectory during the transient phase, therefore causing the inductor current to achieve the desired value. The method for designing system control and the precise mathematical derivation are both provided in Section 4. Section 5 provides examples of both simulation and experimental validation. The last portion is the conclusion.

2. Single-phase VSI Load Step Challenges

The basic circuit of a single-phase full-bridge VSI is seen in Figure 1, and it supplies the pure resistive load R_{L1} with the help of an LC filter. The additional switch S_d simulates abrupt load change by connecting or disconnecting R_{L2}.

As an example of fundamental analysis, a single-phase VSI with the bipolar pulse width modulation (PWM) approach is chosen and modelled for the research. Two pairs of

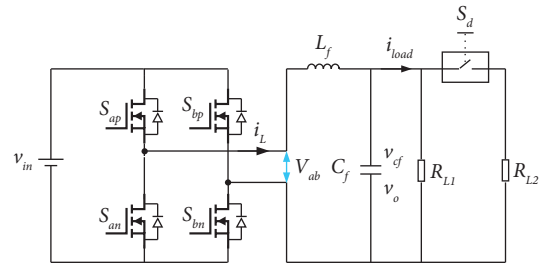


Figure 1: The single-phase full-bridge VSI.

switches (S_{ap} and S_{bn}) and (S_{bp} and S_{an}) work in complementary states. According to the switching state, there are two equivalent circuits, as shown in Figure 2. When $S_{ap} = S_{bn} = \text{ON}$ and $S_{bp} = S_{an} = \text{OFF}$, the energy flows through S_{ap} and S_{bn} to supply R_{L1} via the LC filter as demonstrated in Figure 2(a). When $S_{bp} = S_{an} = \text{ON}$ and $S_{ap} = S_{bn} = \text{OFF}$, the power source energy flows through S_{bp} and S_{an} to provide R_{L1} via the LC filter, as shown in Figure 2(b).

Figure 3 depicts the transient response waveform of the single-phase VSI with a linear controller when the load current is abruptly increased or decreased. As seen by the red waveform, i_{load} quickly changes from its starting value $I_{o1}\sin(\theta)$ to $I_{o2}\sin(\theta)$ when S_d is turned on at θ_0. However, the inductor current i_L cannot fluctuate too rapidly to match the required load current. Cf thus compensates the transitory current. As for the positive load current change shown in Figure 3(a), the error, sampling voltage feedback signal $v_o^{'}$compared with v_{ref}, is amplified to increase i_{ref}. i_L is slowly growing. Until θ_1 when i_L equals i_{load}, i_{load} is still higher than i_L, and v_o continues to decline.

After θ_1, i_L keeps growing and is higher than i_{load} $C_f$when it begins recharging. $v_o$rises and exceeds the reference value. At θ_2, i_L declines and equals to i_{load} again. C_f begins discharging, and $v_o$tends to be close to the reference value. Until θ_3, both i_L and v_{Cf} are close to $I_{o2}\sin(\theta)$ and v_{ref} and the new steady-state single-phase VSI is reached.

Most of the time, this fluctuation process continues for a long time until it recovers from one steady-state to another steady-state after a sudden change in load. A good tradeoff between the voltage/current overshoot/undershoot and dynamic regulation time should be considered for the optimal parameter design of the linear controller. Furthermore, the dynamic regulation time is increased too much due to the sudden load step-change magnitude under the relatively low switching frequency.

3. On-Line Trajectory Control for the Single-Phase VSI

As seen in Section 2, the single-phase VSI with a standard controller still exhibits a long settling period, and substantial voltage overshoots and undershoots in response to rapid changes in load current. To overcome the challenge, an online optimal trajectory control as an improved nonlinear predictive digital control method is proposed to improve the dynamic response as the problem terminator [32]. The fundamental concept is identifying optimal trajectory by

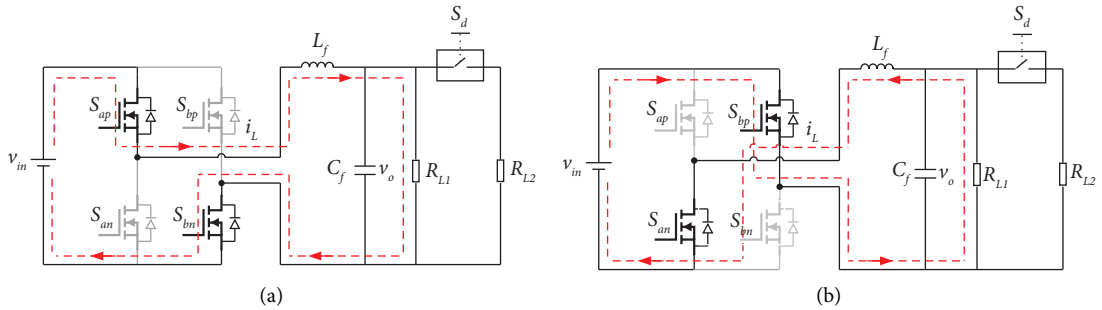


FIGURE 2: The equivalent circuit of the full-bridge single-phase VSI. (a) $S_{ap} = S_{bn} = \text{ON}$ and $S_{bp} = S_{an} = \text{OFF}$. (b) $S_{an} = S_{bp} = \text{ON}$ and $S_{ap} = S_{bn} = \text{OFF}$.

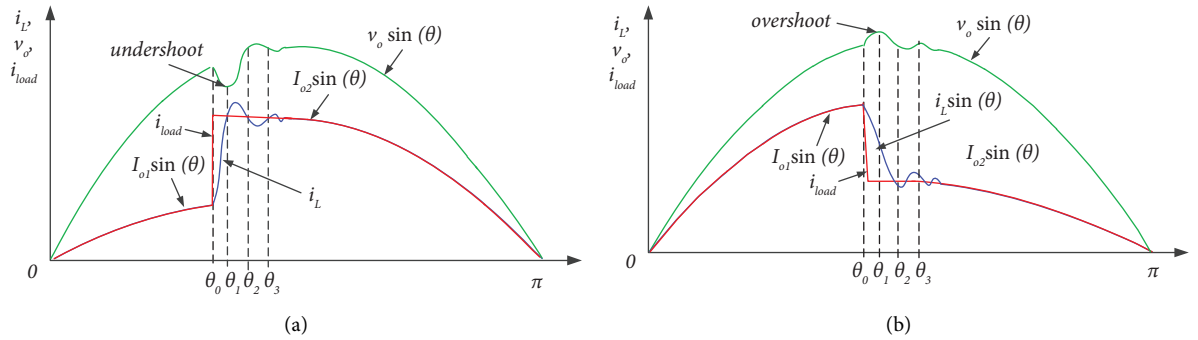


FIGURE 3: Transient response of the single-phase VSI with the linear controller in response to load current. (a) Positive step change. (b) Negative step change.

examining the large signal dynamic process when the load changes abruptly. In response to load variation, the projected ideal waveforms of capacitor voltage and inductor current from the initial steady state to the final steady-state are shown in Figure 4.

The suggested controller incorporates two distinct controls: a linear controller for steady-state operation and a nonlinear controller for transient situations. The capacitor current will provide the necessary current since the inductor current does not vary immediately in response to load current variations. The capacitor charge balance theory states that the charge supplied to the capacitor S_1 (discharge) at the end of the transient cycle must equal the charge withdrawn from the capacitor S_2 (charge), as shown in Figure 4(a). As S_1 has been reduced, the recharging part S_2 has also been reduced. The time required to charge S2 must be reduced in order to decrease the settling time. According to Figure 4(a), the time necessary to recharge the capacitor t_{ch} may be shortened by increasing the height h of the S_2 triangle (defined by θ_0–θ_2); this is achieved by fixing the duty ratio to 100% for θ_0–θ_2 and 0% for θ_2-θ_3.

The recommended controller is intended to do the following:

(i) Determine whether there is an abrupt load shift.

(ii) Fix the duty ratio to 100% (θ_0–θ_2) and 0% (θ_2-θ_3) for a step-up change in a positive half cycle; for a step-down change, fix the duty ratio to 0% (θ_0–θ_2) and 100% (θ_2-θ_3) in a negative half cycle.

(iii) Fix the duty ratio to 0% (θ_0–θ_2) and 100% (θ_2-θ_3) for a step-down change in a positive half cycle; for a step-up change, set the duty ratio to 100% (θ_0–θ_2) and 0% (θ_2-θ_3) in a negative half cycle.

(iv) Switch back to the linear controller once again.

Figure 4 shows the projected ideal waveforms of i_L and v_{Cf} throughout the transient process with positive and negative load current fluctuations. The trainset regulation process is divided into three-time intervals for detailed analysis.

The red waveform depicts the instantaneous transition in i_{load} from $I_{o1}\sin(\theta)$ to $I_{o2}\sin(\theta)$ when Sd is activated at θ_0. i_L cannot vary rapidly to maintain the required load current at θ_0. To speed up the transient, once the positive step change of i_{load} is detected, as shown in Figure 4(a), $S_{ap} = S_{bn} = \text{ON}$ and $S_{an} = S_{bp} = \text{OFF}$ are set instantly to rise i_L. Until θ_1, when $i_L = I_{o2}\sin(\theta_1)$, v_{Cf} declines to deliver the necessary load current. After θ_1, i_L rises higher than $I_{o2}\sin(\theta)$, and v_o begins to rise. The inductor current rising slope during θ_1 and θ_2 may be described using the equivalent circuit depicted in Figure 2(a) as follows:

$$k_1 = \frac{v_{in} - v_o \sin(\theta)}{2L\pi f_{line}}. \tag{1}$$

At θ_2, $S_{an} = S_{bp} = \text{ON}$, $S_{ap} = S_{bn} = \text{OFF}$, and i_L begin to decline as v_{Cf} grows. At θ_3, i_L is close to the load current, and v_o is back to the reference voltage. Both i_L and v_{Cf} enter the quasi-steady state. The inductor current falling slope

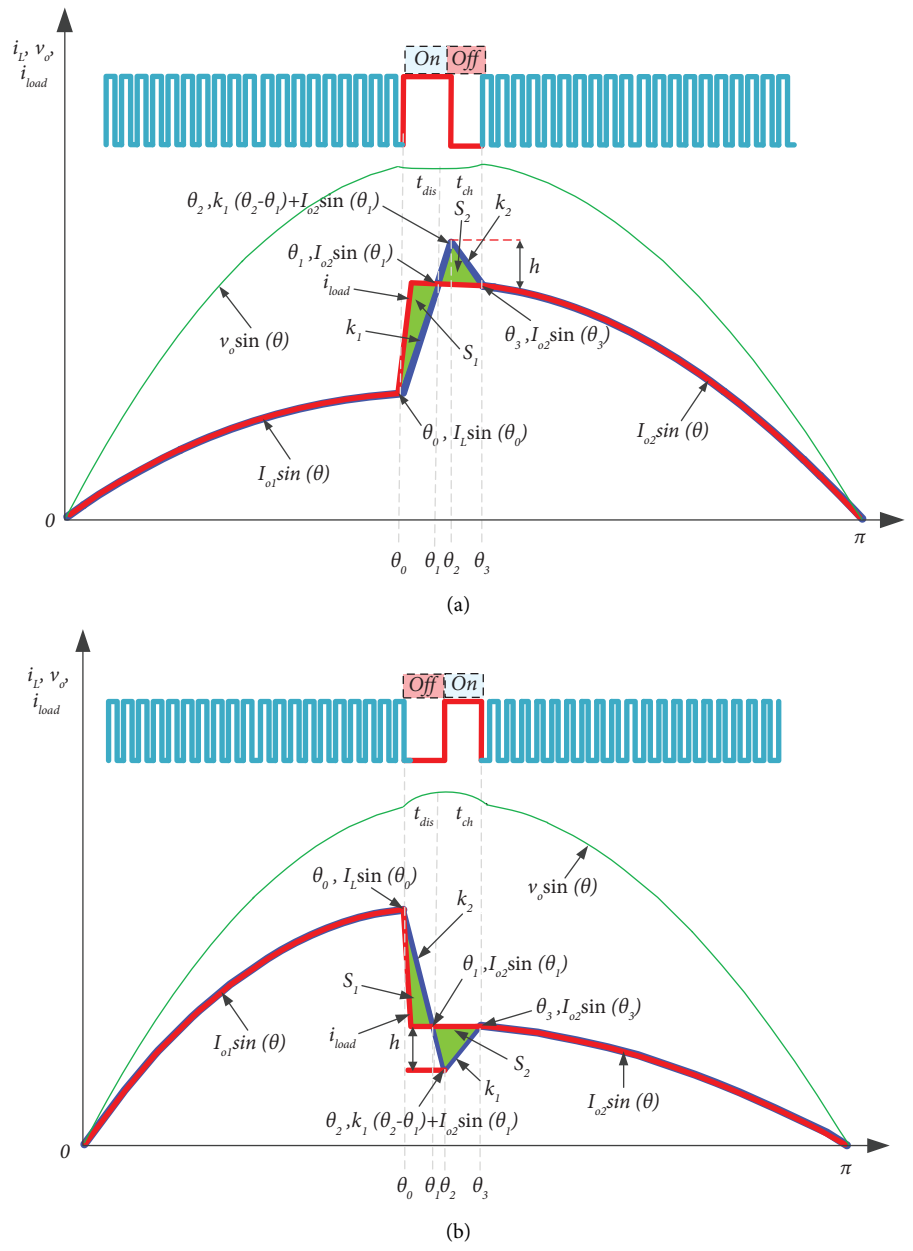


FIGURE 4: The transient response waveform with the optimal trajectory controller in response to load changes. (a) Positive step change. (b) Negative step change.

through (θ_2 and θ_3) is derived in (2) using the equivalent circuit depicted in Figure 2(b).

$$k_2 = \frac{-v_{in} - v_o \sin(\theta)}{2L\pi f_{line}}. \quad (2)$$

In the same way, the analysis described above can also be performed for single-phase VSIs with the optimal trajectory controller in response to a negative step change, as shown in Figure 4(b) which is as follows:

As seen in Figure 4, the proposed controller ensures that iL and vCf arrive at the desired value by precisely following the projected best trajectory while simultaneously reducing the settling time and voltage fluctuations that occur throughout the transient operation. Figure 5 indicates the operation diagram of the proposed predictive control algorithm in conjunction with the linear regulator. A digital control chip makes it easier to combine linear and nonlinear control algorithms to generate the PWM signal. All the transient switching state sequence and ON/OFF state time duration under the different load change conditions are calculated using on-line calculation or prestored off-line results as a look-up table in the on-chip flash. Furthermore, the linear controller parameters can be efficiently designed with relatively high bandwidth to handle the slow load change condition. Once the abrupt change in load current is noticed, the nonlinear controller quickly bypasses the linear regulator and controls the power devices in one switching period.

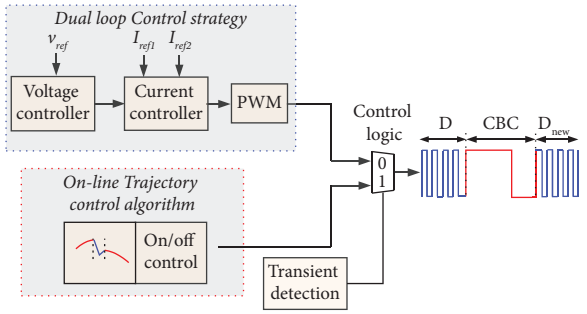


FIGURE 5: The on-line trajectory control algorithm in combination with the linear compensator.

4. Mathematical Derivation and Controller Design

The optimal trajectory control technique is implemented in four steps based on comprehensive theoretical research and mathematical derivation.

Step 1. Detection of load current step change at θ_0.

After detecting an abrupt change in load current, the on-line trajectory control module halts the linear controller. The power devices are instantly switched. $S_{ap} = S_{bn} = \text{ON}$ and $S_{an} = S_{bp} = \text{OFF}$ are fixed for step up, and $S_{an} = S_{bp} = \text{ON}$ and $S_{ap} = S_{bn} = \text{OFF}$ are fixed for step down.

Step 2. Calculate θ_1 and capacitor discharge portion S_1.

As shown in Figure 4(a), i_L goes up from $I_{o1}\sin(\theta_0)$ to $I_{o2}\sin(\theta_1)$, and C_f discharges between θ_0 and θ_1.

As demonstrated in Figure 4(a), i_L is rising from $I_{o1}\sin(\theta_0)$ to $I_{o2}\sin(\theta_1)$, and C_f is discharging during θ_0 and θ_1. Based on the current increasing slope coefficient k_1 expressed in (1), i_L meets

$$(I_{o2}\sin\theta_1 - I_{o1}\sin\theta_0) = k_1(\theta_1 - \theta_0). \tag{3}$$

The red waveform in Figure 4(a) shows that the load current does not significantly alter after the rapid step shift between θ_0 and θ_1, so $I_{o2}\sin\theta_1 \approx I_{o2}\sin\theta_0$. Equation (3) can be simplified, and θ_1 is calculated as follows:

$$\theta_1 = \frac{I_{o2}\sin\theta_0 - I_{o1}\sin\theta_0 + k_1\theta_0}{k_1}. \tag{4}$$

The green-shaded region S_1, representing the charge discharged by C_f, may be estimated using elementary geometric theory.

$$S_1 = \frac{1}{2}(\theta_1 - \theta_0)(I_{o2}\sin\theta_1 - I_{o1}\sin\theta_0) = \frac{1}{2}k_1(\theta_1 - \theta_0)^2. \tag{5}$$

Step 3. Calculate θ_2, θ_3, and capacitor charging portion S_2.

At θ_2, as presented in Figure 4(a), $S_{ap} = S_{bn} = \text{OFF}$ and $S_{an} = S_{bp} = \text{ON}$ are set. i_L begins to decline at the slope of k_2, and C_f starts to increase till θ_3. Throughout the transient θ_0 and θ_3, i_L encounters

$$I_{o1}\sin\theta_0 + k_1(\theta_2 - \theta_0) + k_2(\theta_3 - \theta_2) = I_{o2}\sin\theta_3. \tag{6}$$

Based on the green-shaded portion S_2, the charge absorbed by C_f can be calculated as follows:

$$S_2 = \frac{1}{2}(\theta_3 - \theta_1)(k_1(\theta_2 - \theta_1) + I_{o2}\sin\theta_1 - I_{o2}\sin\theta_3). \tag{7}$$

To ensure that both i_L and v_{cf} approach the region of the new quasi-steady state, the C_f released charge, represented by the green-shaded area S_1 during θ_0 and θ_1, should be equal to the absorbed charge, represented by S_2 during θ_1 and θ_3 and $S_1 = S_2$ as follows:

$$\begin{aligned}&(\theta_1 - \theta_0)(I_{o2}\sin\theta_1 - I_{o1}\sin\theta_0)\\ &\quad = (\theta_3 - \theta_1)(k_1(\theta_2 - \theta_1) + I_{o2}\sin\theta_1 - I_{o2}\sin\theta_3).\end{aligned} \tag{8}$$

Apparently, equations (6) and (8) are nonlinear equations that include two unknown variables, θ_2 and θ_3. It is easy to get the numerical solution of θ_2 and θ_3 using computer-assisted software such as Matlab or Mathcad.

Even though the accurate time instants θ_2 and θ_3 can be obtained using off-line numerical calculation, the on-line calculation is more suitable for practical engineering applications using a digital signal processor (DSP). Theoretical research and simulation demonstrate that the transient regulation time interval (θ_3–θ_0) is too short, so the load current can seem like a constant value. To simplify the calculation and apply the aforementioned optimal trajectory control algorithm in the C2000 DSP, some reasonable assumptions ($I_{o2}\sin\theta_3 \approx I_{o2}\sin\theta_2 \approx I_{o2}\sin\theta_1$) are made to simplify the analysis. Equations (6) and (8) are rewritten as follows:

$$\begin{cases} k_1(\theta_2 - \theta_0) + k_2(\theta_3 - \theta_2) \approx I_{o2}\sin\theta_0 - I_{o1}sin\theta_0, \\ (\theta_1 - \theta_0)^2 = (\theta_3 - \theta_1)(\theta_2 - \theta_1). \end{cases} \tag{9}$$

By solving (9), θ_2 and θ_3 are as follows:

$$\begin{cases} \theta_2 = \dfrac{2Xa + 2ak_1\theta_0 - k_2\left(-b \pm \sqrt{b^2 - 4ac}\right)}{2a(k_1 - k_2)}, \\ \theta_3 = \dfrac{-b \pm \sqrt{b^2 - 4ac}}{2a}, \end{cases} \tag{10}$$

in which $a = -k_2/k_1 - k_2$, $b = 1/k_1 - k_2(X - k_1\theta_1 + k_1\theta_0 + 2k_2\theta_1)$, $c = -X\theta_1 + k_1\theta_0\theta_1/k_1 - k_2 - \theta_0^2 + 2\theta_0\theta_1$, and $X = I_{o2}\sin\theta_0 - I_{o1}\sin\theta_0$.

Step 4. Trajectory control module deactivation (θ_3)

When i_L and v_{cf} enter the vicinity of a new quasi-steady state at θ_3, the trajectory control module is deactivated.

The entire settling period $\theta_{settling}$ for positive/negative step change described as θ_3–θ_0 is derived in (11).

$$\theta_{settling} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} - \theta_0. \tag{11}$$

The suggested on-line optimal trajectory control approach equations were found for a step-up change in load

Table 1: The theoretical value and simplified calculation results for different step changes.

Operation conditions: $V_{\text{in}} = 200\,\text{V}$, $M = 0.78$, $L_f = 1.2\,\text{mH}$, $C_f = 20\,\mu\text{F}$, and $I_{o1} = 5\,\text{A}$					
Radians	20% step-up change	40% step-up change	60% step-up change	80% step-up change	100% step-up change
Positive step change at $\theta_0 = \pi/3$ (*theoretical value*)					
θ_{1t}	1.0522	1.0572	1.0622	1.0670	1.0724
θ_{2t}	1.0568	1.0664	1.0762	1.0856	1.0958
θ_{3t}	1.0577	1.0682	1.0789	1.0892	1.1004
Positive step change $\theta_0 = \pi/3$ (*simplified analytical solution*)					
θ_{1s}	1.0521	1.0570	1.0619	1.0668	1.0717
θ_{2s}	1.0566	1.0659	1.0753	1.0847	1.0941
θ_{3s}	1.0575	1.0677	1.0780	1.0883	1.0985
Positive step change at $\theta_0 = 2\pi/3$ (*theoretical value*)					
θ_{1t}	2.0992	2.1040	2.1088	2.1137	2.1182
θ_{2t}	2.1036	2.1127	2.1217	2.1310	2.1395
θ_{3t}	2.1044	2.1144	2.1243	2.1346	2.1439
Positive step change at $\theta_0 = 2\pi/3$ (*simplified analytical solution*)					
θ_{1s}	2.0993	2.1042	2.1091	2.1140	2.1189
θ_{2s}	2.1038	2.1131	2.1225	2.1319	2.1413
θ_{3s}	2.1047	2.1149	2.1252	2.1355	2.1457

current. The operating principles and equations for adapting the approach to a negative load current step change are almost identical to those described above.

Table 1 lists the theoretical value of θ_1, θ_2, and θ_3 by the numerical calculation and the analytical solution from the simplified equations (4) and (10) under the different load current step-change amplitude at $\pi/3$ and $2\pi/3$. The corresponding simplification error δ, defined as (12), is shown in Figure 6.

$$\delta = \frac{\theta_{3s} - \theta_0}{\theta_{3t} - \theta_0} \cdot 100\%. \tag{12}$$

The regulation time intervals of theoretical and simplified calculation results are approximately equivalent to each other, enabling the real-time on-line application and preserving enough control precision. δ grows as the step-change amplitude and filter inductance L increase. However, the slight simplification difference does not significantly impact the control performance.

The settling time of the on-line trajectory control algorithm during step change of load current is independent of the linear regulator parameters and mainly determined by the increasing and decreasing slopes of i_L, step-change initial angle θ_0, and amplitude. This is different from the dynamic behaviour of the single-phase VSI with the conventional controller because it does not use the output voltage as a feedback mechanism during the transient response from θ_0 to θ_3.

Figure 7 shows the program flow chart of the on-line trajectory control algorithm. After detecting the rapid step change, the transient regulation module is activated. In the end, the control system returns to using the linear regulator. Figure 8 illustrates the total settling time for the single-phase VSI with different inductance L_f, θ_0, and amplitude under the operation conditions $v_{in} = 200\,\text{V}$, $v_o = 154\,\text{V}$, and $I_{o1} = 5\,\text{A}$.

From the previous analysis, the on-line trajectory control algorithm is more suitable for the dramatic load change. It does not work well under relatively small or slow load change conditions in the vicinity of 0 and π, as shown in Figure 9. A linear regulator can work very well in these operating conditions and provide a good dynamic performance.

5. Implementation Techniques for the Detection of Critical Points for Transferring

The proposed implementation techniques that can be used to detect these critical points and provide a seamless transition between controllers are given as follows:

5.1. Detection of Load Step Changes. The proposed load step detection approach uses analog and digital signal processing techniques. A delayed output voltage signal and a comparator are used to detect load step changes in a power supply or load. The delayed signal is generated by a simple RC filter circuit, and the comparator generates a pulse signal if their difference exceeds a certain threshold. The microcontroller processes the comparison results to realize the step detection of load. Figure 10 shows a load change detector circuit with an adjustable delay.

5.2. Smooth Transferring Back to Linear Control. To transition smoothly to the linear controller, this article suggests increasing sampling frequency, maximizing system bandwidth, and running the linear controller at max speed. After the transient, the control system reverts to the PI controller for steady-state regulation. Before reverting to the linear controller, the optimal approach computes new steady-state values denoted as $i_{L\text{new}}$ and D_{rew} for inductor current and duty cycle to avoid oscillations.

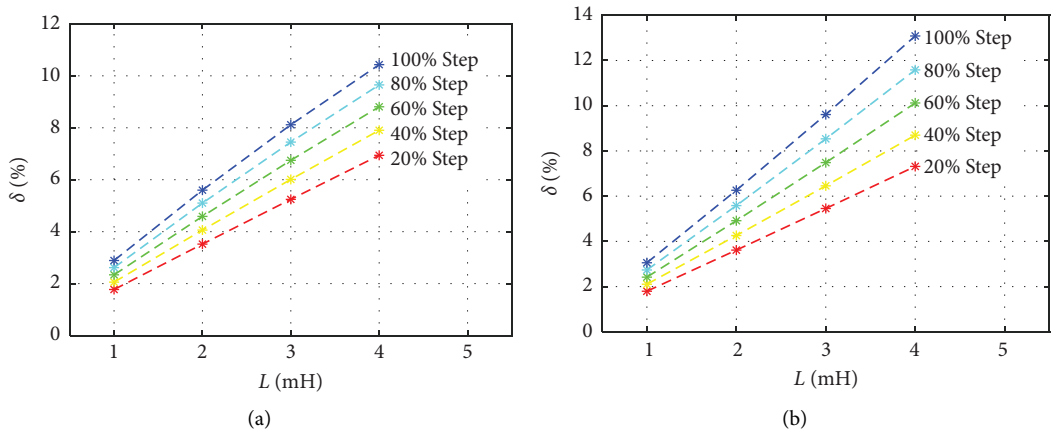


Figure 6: The simplification error δ under different inductance and load current step change at $V_{in} = 200$ V, $v_o = 154$ V, and $I_{o1} = 5$ A: (a) positive step change ($\theta_0 = \pi/3$) and (b) positive step-change ($\theta_0 = 2\pi/3°$).

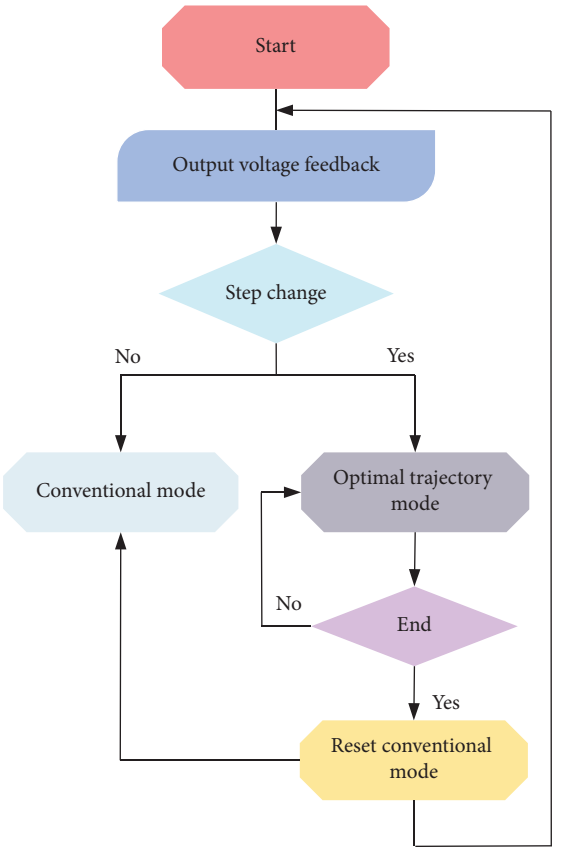


Figure 7: Flow chart of the on-line optimal trajectory control algorithm under the different load step change.

$$i_{L\text{new}} = I_{o2} \sin(\theta_3),$$
$$D_{\text{new}} = \frac{1 + M_i \sin(\theta_3)}{2}. \quad (13)$$

6. Simulation and Experiment Results

Numerical simulations in MATLAB/Simulink were used to evaluate the suggested on-line trajectory control approach and theoretical analysis. For comparison, a well-designed

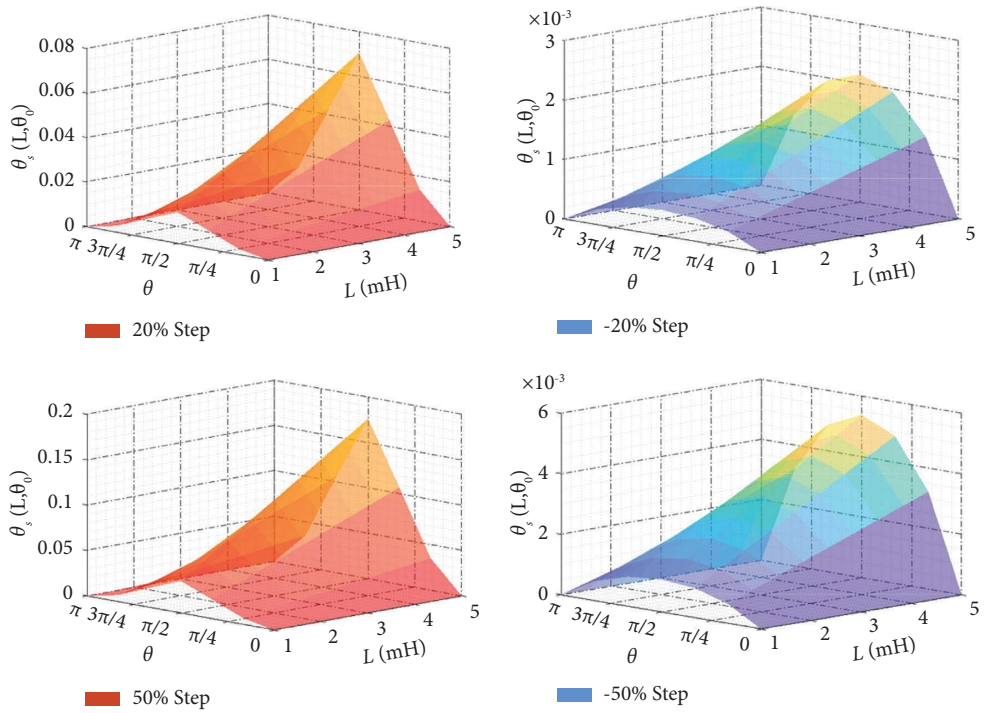


Figure 8: The settling time with the on-line trajectory controller under different inductance and load current step change.

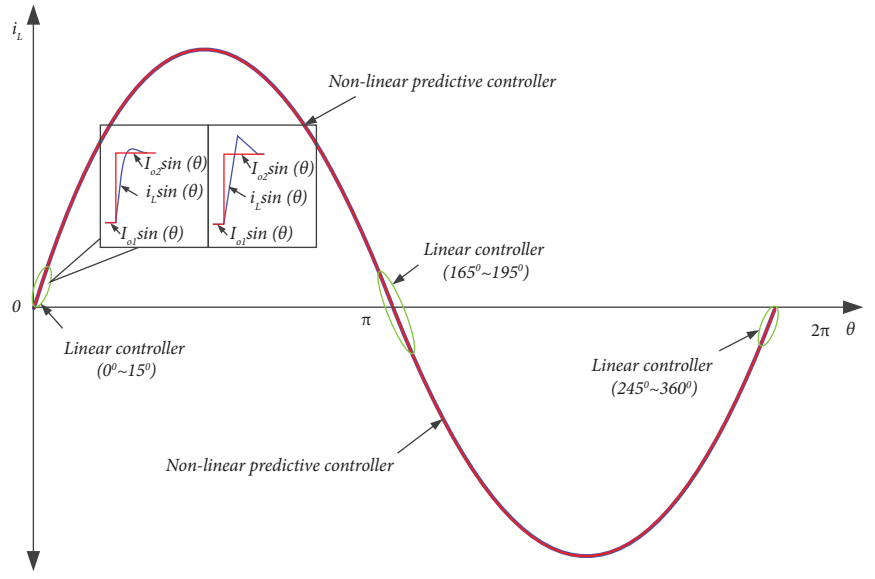


Figure 9: The suitable load step-change condition for the single-phase VSI with the on-line trajectory control algorithm.

single-phase VSI with a linear controller is constructed. The main circuit parameters are $v_{in} = 200$ V, $v_o = 154$ V, $C_1 = C_2 = 5000$ uF, $L_f = 1$ mH, $C_f = 20$ uF, $R_{L1} = 20\,\Omega$, and $R_{L2} = 50\,\Omega$. The switching frequency f_s is 100 kHz, and the output line frequency f_{line} is 50 Hz. The main parameters of the PI controller are $k_{vol}(z) = 0.5 + 0.005\ z/(z-1)$ and $k_{\text{cur}}(z) = 4.2 + 0.025\ z/(z-1)$.

The transient response of DC-AC with a traditional PI controller to load current ranging from 7.8 A to 10.5 A and back to 7.8 A is presented in Figure 11, and Figure 12 depicts the transient response utilizing the on-line trajectory method. The measured waveforms comprise the identified load step-change signals, V_{ab}, i_L, and v_{Cf}.

To control i_L and v_C from the one steady state $i_{L\_\text{int}} = 7.8$ A and $v_{cf\_\text{int}} = 133.36$ V to the final steady state $i_{L\_\text{final}} = 10.5$ A and $v_{cf\_final} = 136.36$ V, the optimal trajectory of a transient is predicted and implemented. According to (4) and (10), the on-state time interval of S_a 116 μs and off-state time interval 10 μs calculated in the theory for positive step change are identical to the

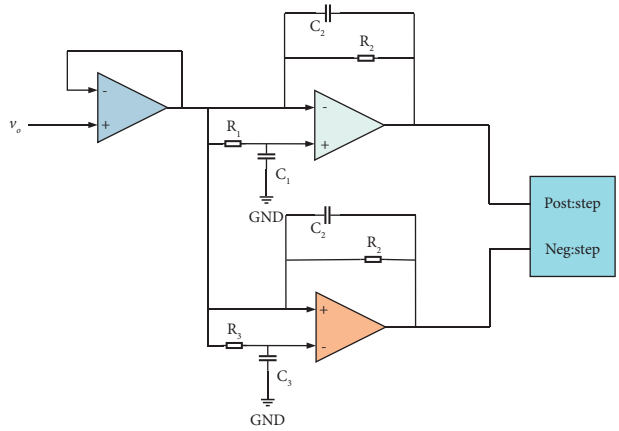


Figure 10: Implementation of the load change detector.

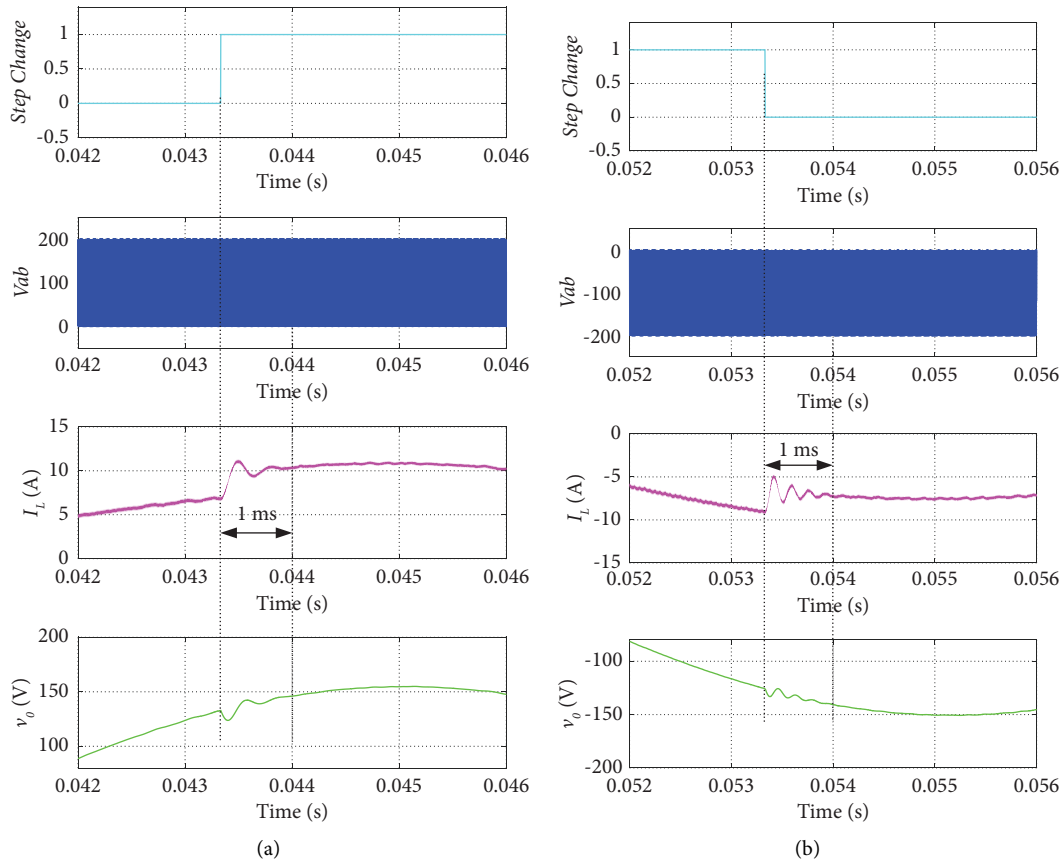


Figure 11: Transient response load current with linear control. (a) Step up from 7.8 A to 10.5 A at $\pi/3$. (b) Step down from 10.5 A to 7.8 A at $4\pi/3$.

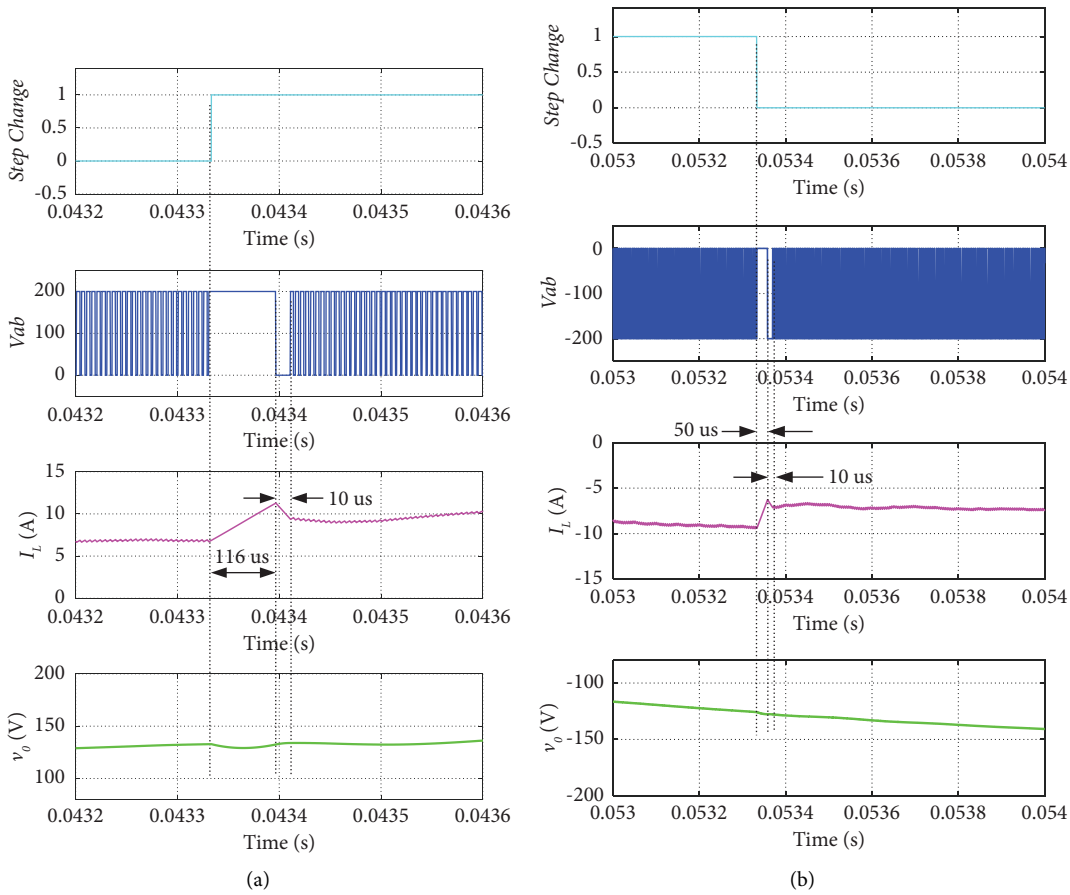


Figure 12: Transient response with on-line trajectory control. (a) Step up from 7.8 A to 10.5 A at $\pi/3$. (b) Step-down from 10.5 A to 7.8 at $4\pi/3$.

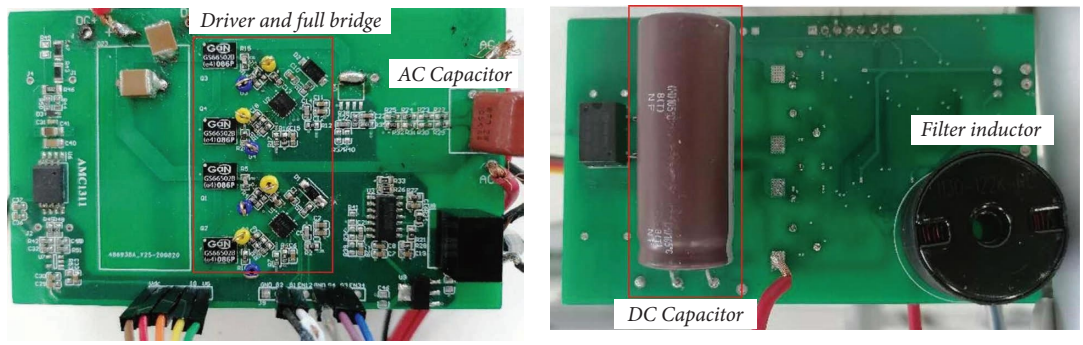


Figure 13: The prototype of the single-phase VSI. (a) Top view. (b) Bottom view.

simulation results displayed in Figure 12(a). The recovery period is decreased from 1 ms to 126 μs, which is a more than 80% decrease compared to a traditional dual-loop linear PI controller. Additionally, voltage undershoot is significantly decreased.

It is demonstrated in Figure 12(b) that with load current ranging from 10.5 A to 7.7 A, the transient settling time is reduced from 1 ms with the conventional dual-loop controller to 60 us using the on-line trajectory control algorithm.

As illustrated in Figure 13, a laboratory prototype of the 800 W single-phase VSI is constructed to validate the theoretical calculations, and the corresponding system diagram is shown in Figure 14. The six-step on-line trajectory control method can be readily created and executed using the EPWM and high-speed ADC capabilities of the TMS320F28377D. Each switching instant's duration is computed on-line and saved on a chip. AC load step change is executed via a bidirectional switch with two MOSFETs linked in reverse. In addition, the

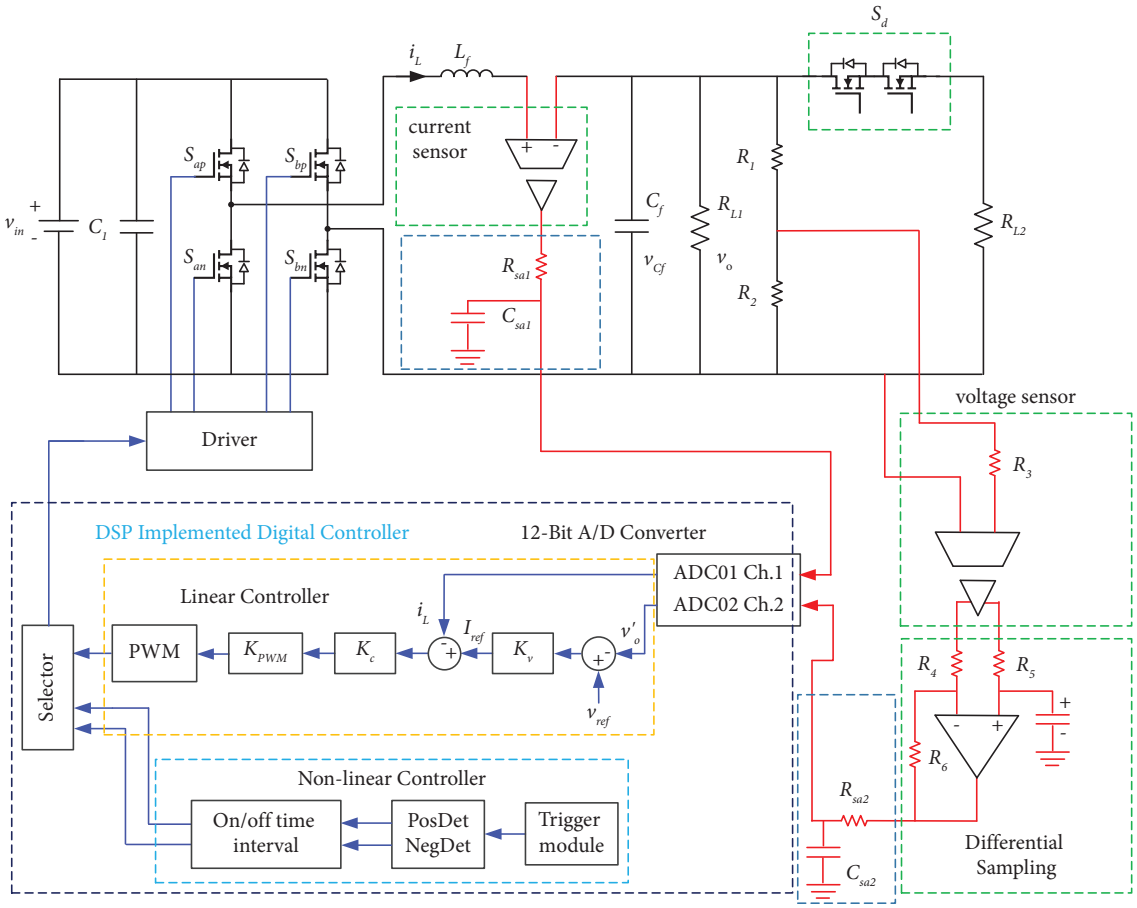


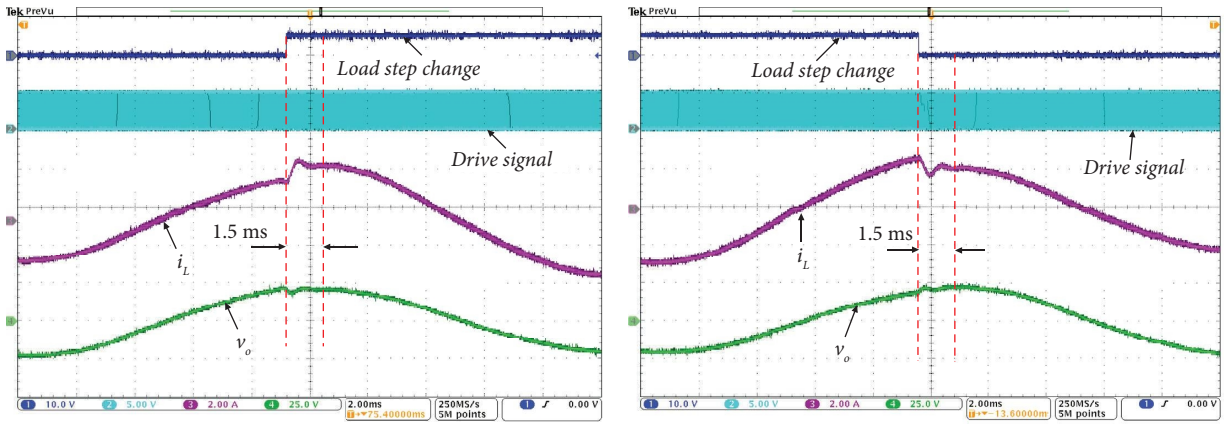
Figure 14: The hardware implementation block diagram of the proposed controller.

Table 2: The specifications for the experimental prototype.

Switching device	S_{ap}, S_{an}, S_{bp}, S_{bn} S_d	GAN (GS65004B) MOSFET (SiHJ6N65E)
Passive components	C_{dc} L_f C_f	5000 uF 0.5 mH 20 μF
R_L load	R_{L1} R_{L2}	30 Ω 50 Ω
Switching frequency	f_s	100 kHz
Current sensor Voltage sensor	K_i K_v	0.1 0.01

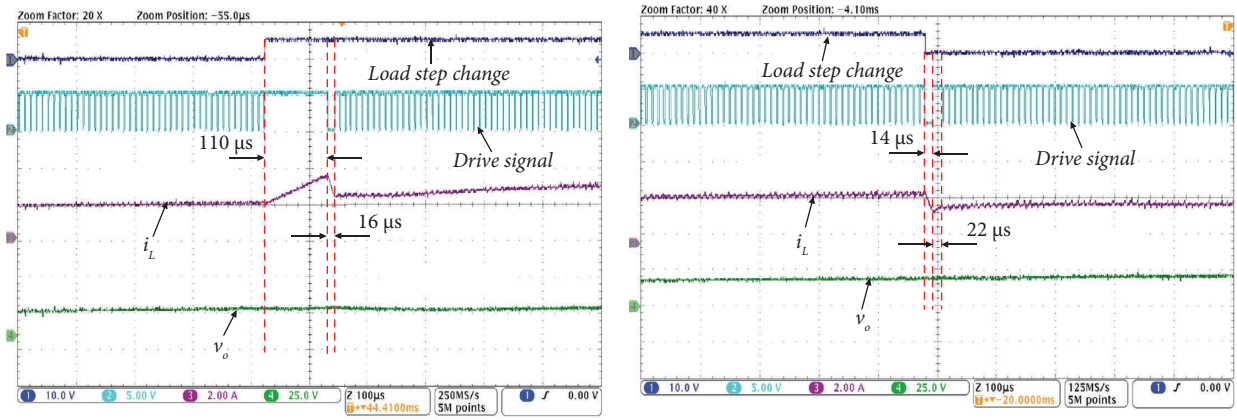
external interrupt is employed to identify the abrupt change in load current i_L, and v_{cf} is measured using two operational amplifiers with excellent bandwidth and isolation. The voltage and current loop's PI controller guarantees that v_o tracks the reference with zero steady-state error. The PWM module then creates four driving signals for power devices. As soon as a step-change is recognized, the linear controller shifts to a nonlinear optimal controller.

The on/off time module generates a control signal according to the calculated time instants. PI parameters are reset at the completion of the transient, and the control system is switched back to the linear regulator. The controller undergoes a smooth transition with negligible switchover effects because v_o, i_L, and Dnew are at their new quasi-steady-state values. A "slow" PI controller does not need to maintain stability during mode switchovers. Consequently, the maximum speed of the linear control may be attained. Table 2 lists the specifications of the experimental prototype, and key parameters of dual-loop PI controllers are $k_{vol}(z) = 0.2 + 0.0034 \cdot z/(z-1)$ and $k_{cur}(z) = 1.2 + 0.017\, z/(z-1)$. Two step-change points, $\pi/3$ and $4\pi/3$, are chosen for the hardware demonstration of the on-line trajectory control algorithm. Figure 15 illustrates the transient



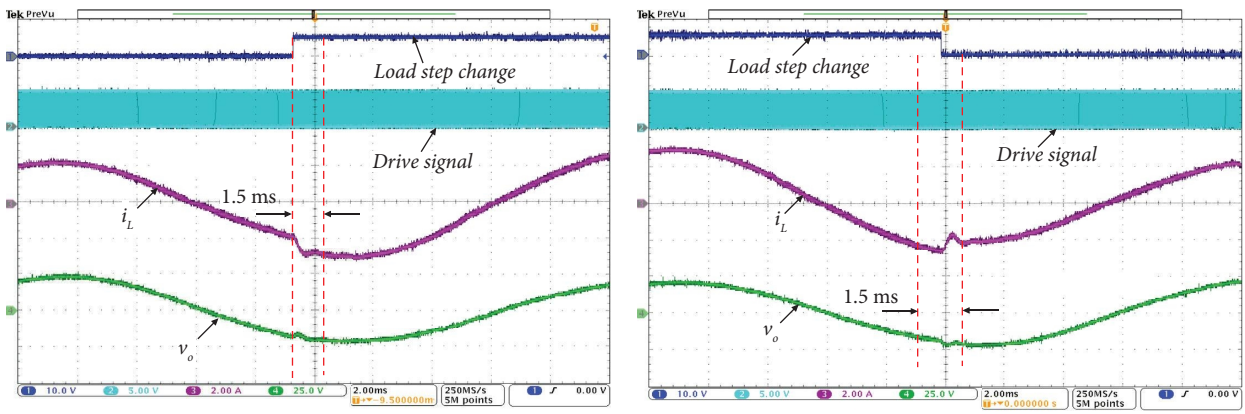
(a) (b)

Figure 15: Transient waveforms with the PI controller at $\pi/3$. (a) Step change of i_{load} from 2.2 A to 3.5 A. (b) Step change of i_{load} from 3.5 A to 2.2 A.



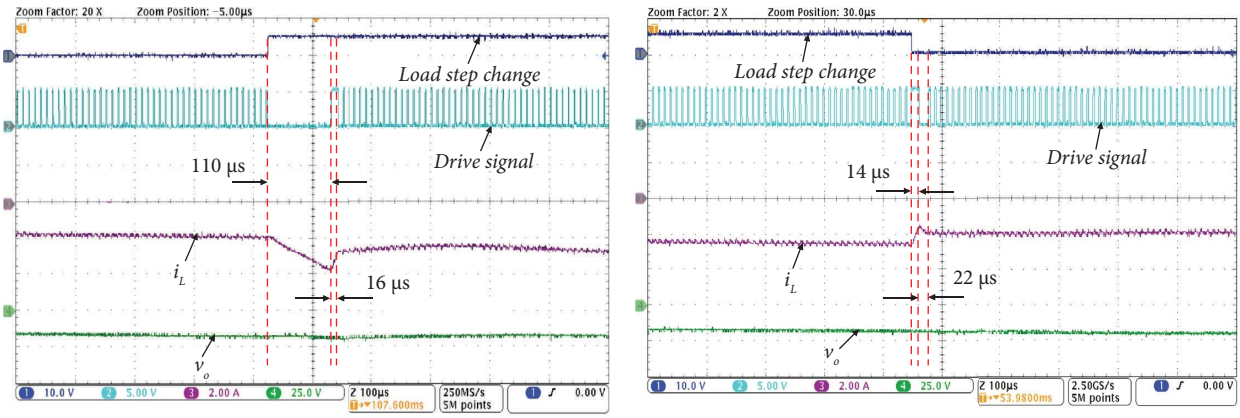
(a) (b)

Figure 16: Transient waveforms of the proposed controller at $\pi/3$. (a) Step change of i_{load} from 2.2 A to 3.5 A. (b) Step change of i_{load} from 3.5 A to 2.2 A.



(a) (b)

Figure 17: Transient waveforms with the PI controller at $4\pi/3$. (a) Step change of i_{load} from 2.2 A to 3.5 A. (b) Step change of i_{load} from 3.5 A to 2.2 A.



(a) (b)

FIGURE 18: Transient waveforms of the proposed controller at $4\pi/3$. (a) Step change of i_{load} from 2.2 A to 3.5 A. (b) Step change of i_{load} from 3.5 A to 2.2 A.

experimental waveforms of a single-phase VSI with the linear controller during a rapid step change at $\pi/3$. And Figure 16 depicts the similar transient response of the suggested nonlinear optimal trajectory control approach during the identical step change in load current. Both v_{Cf} and i_L recover rapidly. The settling time using the on-line trajectory control method is approximately consistent with the theoretical calculation, coming in at 113 microseconds for positive step changes in load current and 36 microseconds for negative step changes in load current.

The voltage/current overshoot and oscillation amplitude throughout the transient process are smaller than the simulation value due to the hardware test platform's relatively large system damping coefficient. Figures 17 and 18 show the measured experimental results of the single-phase VSI with the existing linear controller and the on-line trajectory control algorithm during step change at $4\pi/3$, respectively.

7. Conclusion

This article presents a hardware-efficient, low cost, and simple on-line trajectory controller with the following merits: The controller can work conveniently (bandwidth-free) with a linear-nonlinear combination without sacrificing stability or having any steady-state errors. The controller is far superior to conventional methods, in addition to being less complicated, less expensive, and having fewer limitations than the control methods mentioned above. The voltage deviation may be lowered by 74%, and the settling time can be reduced by 80% in response to the load current step change in a positive direction. On the other hand, if the load current is altered in a negative direction, the converter overshoot will be reduced by 70%, and the settling time will be cut down by 75%. At the same time, a set of nonlinear optimization equations are constructed, which can change the output voltage according to the application scene and realize the real-time on-line control. Simulation and experimental platforms are built to verify the proposed scheme's correctness. The results show that the proposed control scheme can effectively shorten the stabilization time, reduce the voltage spike in the transient state process, and improve the reliability of the equipment.

Nomenclature

K_1: Upward slope
K_2: Downward slope
S_1: Charge portion
S_2: Discharge portion of
i_L: Inductor current
i_{load}: Load current
i_{ref}: Reference current
i_L: Sensed current
v_{ref}: Reference voltage
I_{o1}: Initial load current
I_{o2}: Final load current
v_{in}: Input dc voltage
v_o: Output voltage
v_{cf}: Capacitor voltage
L_f: Filter inductor
C_f: Filter capacitor
S_d: SSR relay switch
R_{L1}: Initial load
R_{L2}: Second load
D_{new}: New duty ratio
f_{line}: Line frequency.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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Research Article

The Design of 2S2L-Based Buck-Boost Converter with a Wide Conversion Range

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This manuscript proposes a novel nonisolated negative output buck-boost converter topology for wide voltage conversion applications. To design this converter, a typical buck-boost converter configuration is used. In conventional buck-boost converter, the active switches designed are replaced by two switches-two inductors (2S2L) cells. The proposed converter operates in the continuous conduction mode (CCM) operation under steady-state conditions. This converter has a lower component count and low voltage stress on the switches and diodes. Moreover, the major advantage of this buck-boost converter topology is that a wide range of step-down and step-up voltage conversions can be achieved. The performance of the proposed system is designed in MATLAB/SIMULINK. A few other comparisons are also presented to demonstrate the competitiveness of the proposed buck-boost converter.

1. Introduction

Negative output DC-DC converters are now available with a significant contribution within the industrial domain, such as regenerative braking systems (RBS), data transfer interfaces, signal generators, power electronics systems with neutral point clamping, and generation of solar power [1–4]. The buck-boost converter and the Cuk converter, two well-known negative output converters, have a similar conversion ratio. These two converters are designed to provide an output voltage that is either higher or lower than the input voltage.

At the duty cycle where D is close to 0 or 1, both converters can generate exceptionally good step-down or step-up DC output voltage, which cannot be observed in reality due to the limitations of active switches and diodes unless a transformer (such as a flyback converter) is used to acquire a wider conversion ratio. Unfortunately, using a transformer might result in switching voltage overshoot and EMI difficulties, lowering efficiency [5–7]. Transformer-less converters have been thoroughly researched over the years to achieve high efficiency. There are two types of transformer-less converters, namely, nonconnected inductor converters and coupled inductor converters. Many coupled inductor-based high step-up converters have been developed; similar to isolated converters, a high voltage gain can be achieved by increasing the coupled inductor's turns ratio, and voltage stresses can be reduced using a variety of voltage-clamp strategies, including active and passive circuits.

To achieve high voltage, the magnetic components of noncoupled inductor-type converters are reduced [7]. In recent decades, many negative output converters have been introduced, such as the voltage conversion ratio ($-D$)

indicated in [8] for the negative output KY buck converter, which has a quick dynamic response and smooth switching operation. Reference [9] presents a KY buck-boost topology with the inverted output and a voltage conversion ratio of ($-2D$) but no inverse features. The inverted load voltage-based KY boost converter was described in [10], and it was built by adding a capacitor with an extra diode to boost the converter which has a voltage gain of ($-1/(1-D)$).

The voltage lift methodology is used in the N/O self-lift Luo converter [1], the enhanced N/O self-lift Cuk converter [2], the N/O super-lift converter [11], and the voltage-lift-type Cuk converters [12]. However, all of the converters presented have an obvious error: a significant current spike running through the energy-transferring capacitor due to an abrupt change in voltage across it. Basic power loss and EMI are created by the current spike induced by this capacitor, which is essentially constrained by the dependent parameters [13].

There are a few atypical switched-capacitor converter topologies that use resonant operation rather than forced charging and discharging and are more efficient than standard switched-capacitor converters [14]. There have been several quadratic PWM converters with negative output switching proposed. They are a modified cascade of buck and buck-boost converters that just need a single switch and three diodes to work. Despite having different configurations, they have the same voltage conversion ratio ($-D^2/(1-\mathrm{D})$).

Conventional buck-boost converters have a reduced conversion ratio and a smaller step-down capacity [15]. In [16, 17], switched networks are used in the Cuk converter to make negative output hybrid Cuk converters as well as in the buck-boost converter to make hybrid buck-boost converters. A switched-capacitor (SC) structure is used in one inverted output hybrid buck-boost configuration, whereas a switched-inductor (SL) structure is used in another inverted output hybrid buck-boost configuration.

The addition of switched networks necessitates the use of extra diodes, capacitors, or inductors in the network design to increase the conversion rate, leading to even more sophisticated circuits, higher power losses, and lower efficiency. The voltage ratio ($-1/(1-\mathrm{D})$) for a single-stage switched-capacitor-inductor inverted output boost converter was published in [18]. However, to decrease the current spike caused by the power transferal capacitor, an auxiliary resonant inductor must be added, adding circuit convolution and reducing efficiency.

Power is supplied to today's integrated circuits (ICs) by a power supply that is less than 5 volts. To reduce the power loss of modern high-power consumption CPUs, future microprocessor supply voltages are expected to drop from 3.5 to 1 V, or even lower. As a result, power sources that can reduce the conventional 12 V (or 48 V) voltages to around 1 V are needed. Internet services require a 48 V DC battery that can be increased to a 380 V intermediate DC level, whereas high-intensity discharge lights (HID) used in vehicle headlamps require a voltage spike from the battery's 12 V to more than 100 V during start-up.

It was necessary to get such a high voltage-to-conversion ratio. Step-down converters would have to run at less than 0.1 duty cycle, while step-up converters would have to run at more than 0.9 duty cycle. The peak duty cycle of this magnitude lowers efficiency and impairs transient responsiveness [19]. A new negative output buck-boost converter topology is proposed in this paper. It modifies the buck-boost converter design somewhat and uses a high conversion ratio to generate a reversed output voltage. The power-transferring capacitor is used to store the power in this new converter, and there is no quick voltage shift on it.

The main contribution of the proposed work is as follows:

(i) For wide voltage conversion applications, a novel nonisolated negative output buck-boost converter topology is proposed.

(ii) In a conventional buck-boost converter, the active switch is replaced by two switches-two inductors (2S2L) cells.

(iii) The operation of this converter configuration's continuous conduction mode (CCM) under steady-state conditions is briefly discussed.

(iv) The proposed converter can produce wide voltage conversion ratio in both ways (step-down and step-up) with continuous input current. These are most promising and necessary features for any DC-DC converters used for renewable and EV applications. So for the applications such as PV and fuel cell inputs, the generated voltage is limited considering the size, hence the proposed converter can be most suitable.

The proposed converter is designed and simulated using MATLAB/Simulink. The structure of the paper is summarized as follows: In Section 2, the working principle and steady-state analysis of the planned converter are described, and in Section 3, simulation findings are presented to verify the preliminary theoretical study. Finally, in Section 4, some findings are offered.

2. Steady-State Analyses

We consider the circuit in Figure 1 for steady-state analysis. It is a new voltage negative output converter with a V_{DC} input voltage. Passive components include inductors L_A and L_B, capacitors C_A and C_B, and a resistive load R_L. Power switches S_A and S_B, as well as diodes D_A and D_B, govern the circuit's operation. The continuous conduction mode is used by this converter circuit (CCM). We assume that all of the circuit's components are in excellent condition.

2.1. Operating Principle. The circuit has two stages of operation. The power switches S_A S_B, which regulate the operation of a circuit, are turned on in the first step, as shown in Figure 2(a). Currents begin to flow via the inductors L_A L_B, which are represented by the characters i_{LA} and i_{LB} in the circuit. As illustrated in the diagram, V_{CA} this is the voltage across the capacitor C_A and V_{CB} is the output voltage. In the second stage, both the active switches S_A S_B are switched off,

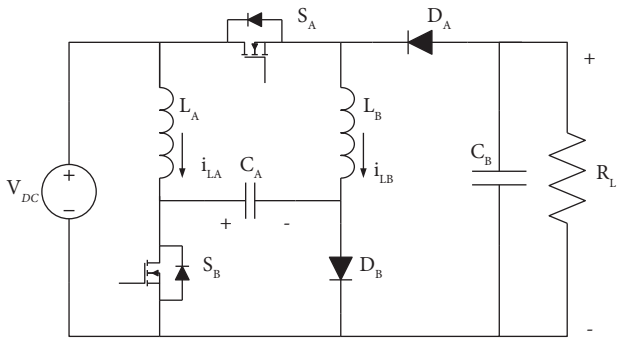

Figure 1: The suggested inverted output buck-boost configuration.

as presented in Figure 2(b). By turning on and off the active switches synchronously, the circuit is operated in two steps.

2.1.1. Mode 1. During stage 1 operation, active switches S_A S_B are switched on, as previously mentioned. The time interval during which these switches are turned on is (NT, NT + DT). Reverse voltage flows across diodes D_A and D_B since the active switches are in the ON state, which make them open switches. V_{DC}, the circuit's input voltage supply, delivers power to the inductor L_A and capacitor C_A. Diodes D_A D_B are subjected to voltage stresses. The voltage produced at the capacitor C_A is viewed by the diode-applied voltage. The input voltage V_{DC}, as well as the energy dissipated by a capacitor C_A, energy, is supplied to any of the other inductors L_B. The voltage stress across the diode D_B is described as the variation between the input voltage V_{DC} and the output voltage V_0.

$$\begin{aligned} L_A\frac{di_{L_A}}{dt} &= V_{DC},\\ L_B\frac{di_{L_B}}{dt} &= V_{DC} + V_{C_A},\\ C_A\left(\frac{dV_{C_A}}{dt}\right) &= -iL_B,\\ C_B\left(\frac{dV_B}{dt}\right) &= -\frac{V_B}{R_L}. \end{aligned} \tag{1}$$

2.1.2. Mode 2. As previously indicated, the power switches S_A S_B are switched off throughout the next time interval (NT + DT, NT + T) in the second stage. In this operation, the diodes D_A D_B come into the picture as closed switches. Power is delivered to the capacitor C_A via the diode D_A from the input voltage V_{DC} and inductor L_A. Because the diodes are conducting in this circumstance, the output capacitor C_B receives energy from the inductor L_B through these diodes. Voltage stresses develop across the power switches S_A S_B. The voltage stress S_A is equal to the voltage along the capacitor C_A. Just like in the first stage, the voltage stress induced across S_B is equal to the difference between the input voltage V_{DC} and the output voltage V_0.

$$\begin{aligned} L_A\left(\frac{di_{L_A}}{dt}\right) &= V_{DC} - V_{C_A},\\ L_B\left(\frac{di_{L_B}}{dt}\right) &= V_B,\\ C_A\left(\frac{dv_{C_A}}{dt}\right) &= i_{L_A},\\ C_B\left(\frac{dv_B}{dt}\right) &= -i_{L_B} - \frac{V_B}{R}. \end{aligned} \tag{2}$$

2.2. Voltage Conversion Ratio M (D). V_{DC}, V_{C_A}, by i_{L_A} by i_{L_B}, I_0, and V_0 are considered to be the DC values. Inductors L_A L_B fulfil the volt-second balance if the designed converter is in steady-state, with net volt-seconds within each period equal to zero. Thus,

$$\begin{aligned} DV_{DC} + (1-D)\left(V_{DC} - \mathrm{V_{C_A}}\right) &= 0,\\ D\left(V_{DC} + V_{C_A}\right) + (1-D)V_B &= 0. \end{aligned} \tag{3}$$

As a result, (3) can be used to calculate V_{CA} and V_0, with the following results:

$$V_{C_A} = \frac{1}{1-D}V_{DC}, \tag{4}$$

$$V_0 = \frac{\mathrm{D}\ (2-\mathrm{D})}{(1-\mathrm{D})^2}V_{DC}. \tag{5}$$

As a result, the proposed converter's voltage conversion ratio may be inferred from (5), and its expression is

$$\begin{aligned} M &= \frac{V_B}{V_{DC}}\\ &= -\frac{D(2-D)}{(1-D)^2}. \end{aligned} \tag{6}$$

The designed converter operates in step-down mode if the duty cycle is less than 0.29 and the voltage conversion ratio M is even less than 1. The rest of the time, it 'is in step-up mode.

2.3. Voltage Stresses of Switch and Diode. The diodes voltage stresses can be calculated using mode 1.

$$\begin{aligned} V_{D_A} &= \frac{V_{DC}}{1-\mathrm{D}},\\ V_{D_B} &= \frac{V_{DC}}{(1-D)^2}. \end{aligned} \tag{7}$$

The power switches' voltage stresses can be calculated using mode 2.

$$\begin{aligned} V_{S_A} &= \frac{V_{DC}}{1-\mathrm{D}},\\ V_{S_B} &= \frac{V_{DC}}{(1-D)^2}. \end{aligned} \tag{8}$$

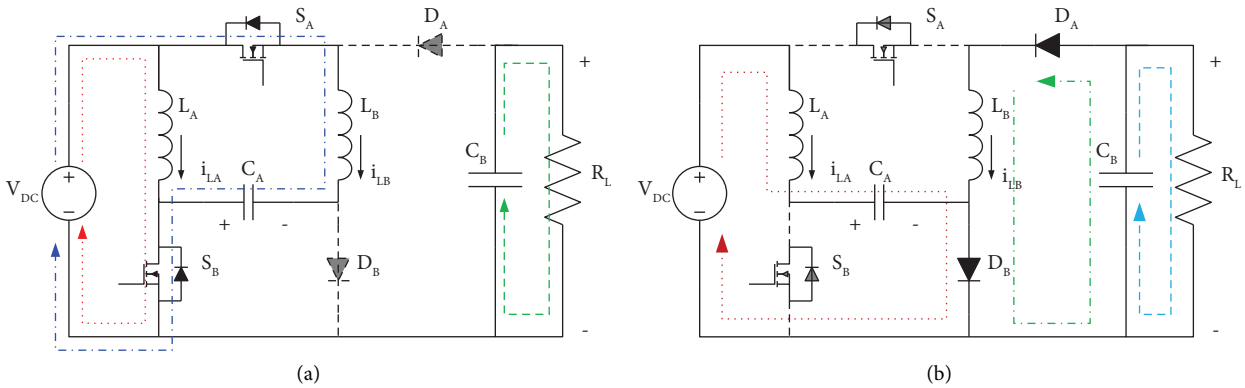

Figure 2: Steady state operating modes of the converter; (a) mode 1 and (b) mode 2.

2.4. Switch and Diode Current Stresses. C_A and C_B capacitors meet the charge balancing principle when the proposed converter reaches a steady state. As a result, the following i_{L_A} i_{L_B} expressions can be derived:

$$i_{L_A} = \left(\frac{\mathrm{D}}{(1-D)^2}\right) I_0,$$
$$i_{L_B} = \left(\frac{1}{1-\mathrm{D}}\right) I_0. \tag{9}$$

The current through the power switch S_A is, according to the operating principle,

$$i_{S_A}(t) = \begin{cases} i_{L_A}(t) + i_{L_B}(t), \\ 0, \end{cases} \tag{10}$$

As a result, the DC value i_{S_A} can be calculated as follows:

$$i_{S_A} = \left(\frac{\mathrm{D}}{(1-D)^2}\right) I_0. \tag{11}$$

Similarly, the current across the power switch S_B has a DC value of

$$i_{S_B} = \left(\frac{\mathrm{D}}{1-\mathrm{D}}\right) I_0. \tag{12}$$

The current that flows through the diode D_A is generated by operating modes, where

$$i_{D_A}(t) = \begin{cases} 0, \\ i_{L_A}(t) + i_{L_B}(t). \end{cases} \tag{13}$$

As a result, it may get the DC value of i_{D_B} by

$$i_{D_B} = \left(\frac{1}{1-\mathrm{D}}\right) I_0. \tag{14}$$

The DC value of the current passing through the diode D_B can be computed using the same approach

$$i_{D_B} = I_0. \tag{15}$$

2.5. Current and Voltage Variation Ratio. The inductor current i_{L_A} rises during the first subinterval and dips during the second subinterval, which has been shown in the traditional time-domain waveforms in Figure 3. As a result, the current ripple and current deviation from the peak value can be calculated as follows:

$$\Delta i_{L_A} = \frac{V_{DC} DT}{L_A}, \tag{16}$$

$$\delta_1 = \frac{\left(\Delta i_{L_A}/2\right)}{i_{L_A}} = \frac{(1-D)^2 \mathrm{T} R_L}{2|\mathrm{M}| L_A}. \tag{17}$$

Moreover, the current ripple from peak to peak and i_{L_B} deviation is determined as follows:

$$\Delta i_{L_B} = \frac{D(2-D) V_{DC} T}{(1-D) L_B}, \tag{18}$$

$$\delta_2 = \frac{\left(\Delta i_{L_B}/2\right)}{i_{L_B}} = \frac{(1-D)^2 \mathrm{T} R_L}{2 L_B}. \tag{19}$$

The following equations can be used to determine the maximum average voltage ripple and also the change in voltages V_{CA} and V_0

$$\Delta V_C = \left(\frac{D^2(2-\mathrm{D})}{(1-D)^3}\right)\left(\frac{V_{DC}\mathrm{T}}{R_L C_A}\right), \tag{20}$$

$$\varepsilon_{C_A} = \frac{\left(\Delta V_{C_A}/2\right)}{V_{C_A}} = \frac{D|M|T}{R_L C_A}, \tag{21}$$

$$\Delta V_B = \left(\frac{D^2(2-\mathrm{D})}{(1-D)^2}\right)\frac{V_{DC}\mathrm{T}}{R_L C_B}, \tag{22}$$

$$\varepsilon_{C_B} = \frac{(\Delta V_0/2)}{V_B} = \frac{DT}{2R_L C_B}. \tag{23}$$

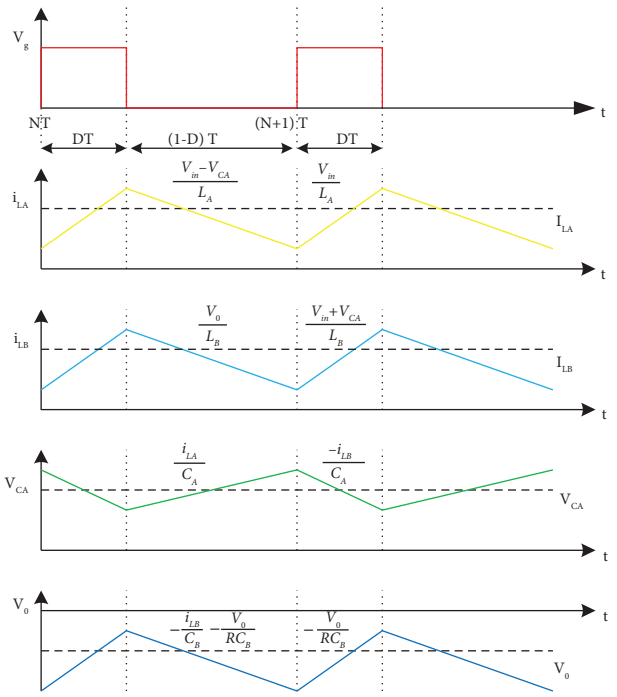

FIGURE 3: The proposed converter's time-domain waveforms under steady-state conditions.

2.6. Inductor and Capacitor Design. The equation is used to compute the ripple current of the inductors L_A, L_B. The inductor voltage V_L, ripple current (Δi_{L_A}) switching frequency (f_s), and duty cycle (D) are used to select the inductor. In mode 1, the incoming inductances L_A L_B contain voltages similar to V_{DC}. As a result, L_A L_B inductance values are determined by employing (24) and (25), respectively.

$$L_A = \frac{V_{DC}DT}{\Delta i_{L_A}}, \tag{24}$$

$$L_B = \frac{D(2-D)V_{DC}T}{(1-D)\Delta i_{L_B}L_B}. \tag{25}$$

For $D = 0.673$, $V_{DC} = 12\,\text{V}$, $f_s = 40\,\text{kHz}$, $\Delta i_{L_A} = 0.5\,\text{A}$, and $\Delta i_{L_B} = 0.8\text{A}$. The value of L_A and L_B is given by $L_A = 403.8\,\mu\text{H}$ and $L_B = 1024.16\,\mu\text{H}$, respectively.

The capacitor charge variance can be used to determine the value of the capacitors C_A and C_B both of which contain voltage ripple. As a result, C_A and C_B can be determined by using relation (26) and (27).

$$C_A = \left(\frac{D^2(2-D)}{(1-D)^3}\right)\left(\frac{V_{DC}T}{R_L\Delta V_{CA}}\right), \tag{26}$$

$$C_B = \left(\frac{D^2(2-D)}{(1-D)^2}\right)\left(\frac{V_{DC}T}{R_L\Delta V_{CB}}\right). \tag{27}$$

For $D = 0.673$, $I_0 = 0.5\,\text{A}$, $f_s = 40\,\text{kHz}$, $\Delta V_{CA} = 2\text{V}$, and $\Delta V_{CB} = 1\,V$. The value of C_A and C_B is given by $C_A = 12.9\,\mu\text{F}$ and $C_B = 8.45\,\mu\text{F}$

2.7. Comparisons with Various Negative Output Topologies. The proposed converter topology is compared to several different switched-inductor converters, including the N/O hybrid buck-boost configuration, N/O self-lift Luo configuration, and basic buck-boost converter. The change of voltage conversion ratios of these converters concerning the duty cycle is depicted graphically in Figure 4. As indicated in Table 1, none of these converters uses inductors, capacitors, diodes, or switches. The abrupt voltage shifts in these converters are also depicted. The converter is meant to have a larger voltage conversion ratio than other N/O converters, such as the topology of the self-lift Luo converter, which can only give higher output voltage. For the step-down voltage conversion ratio, a N/O buck-boost converter is evaluated to the proposed converter. Because it does not have any abrupt voltage changes and has an additional power switch. The proposed converter is chosen over the hybrid buck-boost converter since it has no abrupt voltage changes and has an additional power switch. The presence of abruptly changing voltage in the self-lift Luo converter causes a change in current, causing the capacitor to be shut off. In addition, the number of diodes employed in these N/O converters varies from the specified converter.

From Figure 4(a), we can conclude that the converter which is designed has the maximum value of ideal step-up voltage conversion ratio, i.e., about 45 at duty cycle $D = 0.8$ compared with the other N/O converters, which have a much lesser value of this ratio.

From Figures 4(b) and 4(c), we can conclude that the converter which is designed has the less switch and diode voltage stresses compared with the other N/O converters, which have higher voltage stresses on the switches and diodes.

3. Simulated Results

Initially, a DC-DC converter is simulated in the step-up mode of operation using PSIM simulation to validate the theoretical review. The components used, such as inductors and capacitors, are arranged in detail using (17) and (19), and their properties are listed in Table 2. Because the inductor resists current changes and the capacitor resists voltage changes, the current tolerance value for the inductor is set to 0.5, the voltage across capacitor C is set to 2%, and the voltage across capacitor Co is set to 1%. Time-domain waveforms of step-up and step-down modes are obtained after the simulations. All the simulation waveforms from Figure 5 are in the step-up mode only. The proposed DC-DC converter is considered to be operating in the continuous conduction mode (CCM).

In the MATLAB/Simulink environment, a 2S-2L-based buck-boost converter (see Figure 1) is designed. For the steady-state analysis., the inductors L_A L_B in the proposed converter are assumed to be working in CCM. The values of the inductors and capacitors are calculated using the theoretical analysis described in section II and the equations (16), (18), (20), and (22) stated in Table 2. The inductors $L_A(\Delta i_{L_A})$ and $L_B(\Delta i_{L_B})$ current ripples are 0.5 and 0.8 amps, respectively. Similarly, the capacitors $C_A(\Delta V_{C_A})$ $C_B(\Delta V_{C_B})$ have voltage ripples of 2 V and 1 V, respectively.

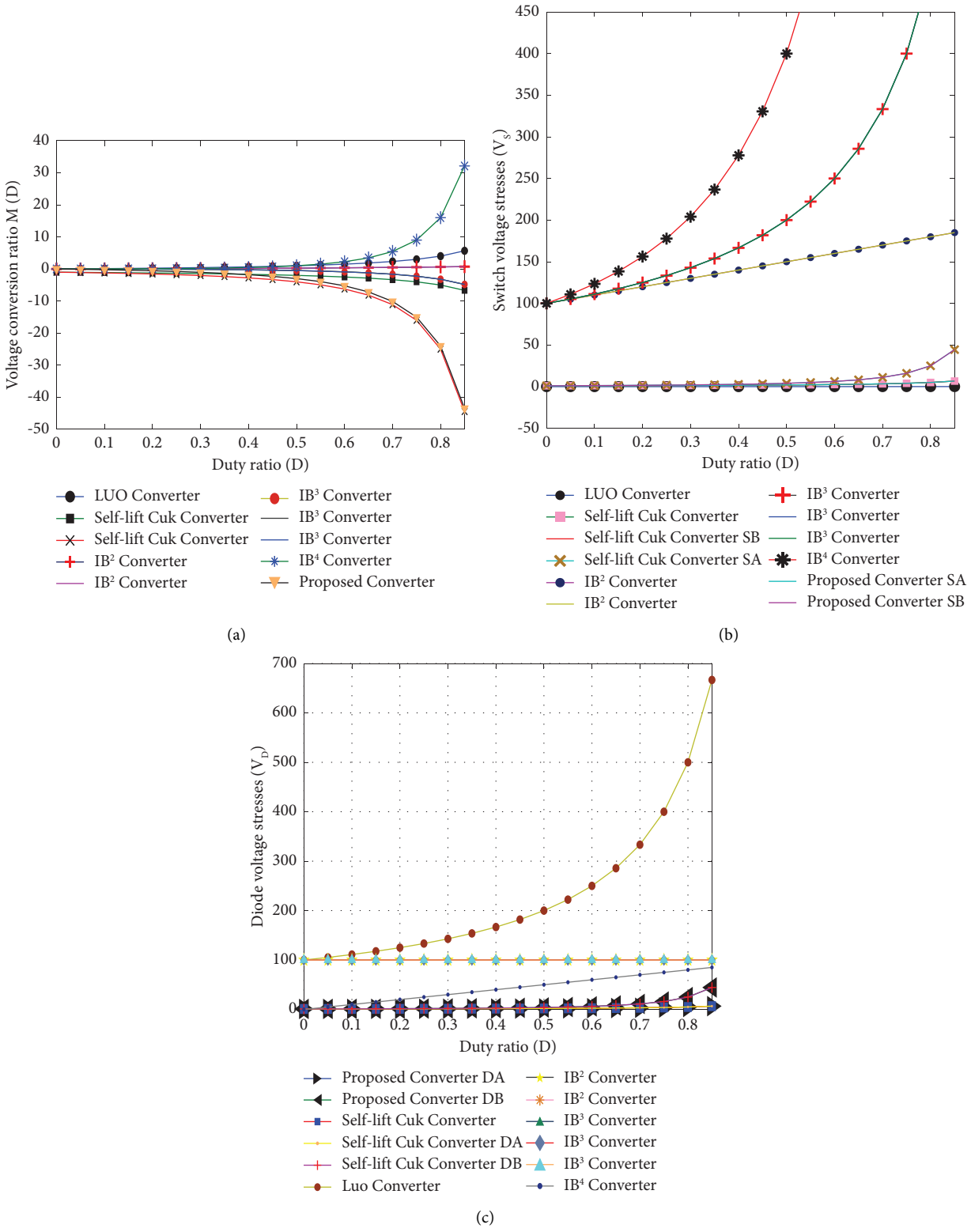

Figure 4: (a) D and $M(D)$: voltage conversion ratio $M(D)$ values for various duty ratio (D). (b) D and $V(D)$: switch voltage stresses for various duty ratios. (c) D and $V(D)$: diode voltage stresses for various duty ratios.

Table 1: Comparisons with Various Negative Output Topologies.

References	Parameters				
	No. of switches	No. of diodes	No. of inductors	No. of capacitors	$M(D)$
[4]	1	1	2	2	$D/1-D$
Converter–1 [12]	1	2	2	3	$-1/1-D$
Converter–2 [12]	2	3	3	3	$-1/(1-D)^2$
Converter–1 [15]	1	3	2	2	D^2
Converter–2 [15]	1	3	2	2	D^2
Converter–3 [15]	1	3	2	2	$-D^2/1-D$
Converter–4 [15]	1	3	2	2	$-D^2/1-D$
[16]	1	3	2	2	$-\mathrm{D}^2/1-D$
[18]	1	3	2	2	$D^2/(1-D)^2$
Proposed converter	2	2	2	2	$-D(2-D)/(1-D)^2$

Table 2: Parameters of main components.

Components	Step-up mode
Input voltage V_{in}	12 V
Output voltage V_{out}	100 V
Switching frequency f	40 kHz
Output load R	200 ohms
Duty cycle D	0.673
Inductor $L_A = V_{\mathrm{in}}\mathrm{DT}/\Delta i_{L_A}$	403.8 μH
Inductor $L_B = D(2-D)V_{\mathrm{in}}T/(1-D)\Delta i_{L_B}$	1024.16 μH
Capacitor $C_A = D^2(2-D)V_{\mathrm{in}}T/(1-D)^3R\,\Delta V_{C_A}$	12.89 μF
Capacitor $C_B = D^2(2-D)V_{\mathrm{in}}T/(1-D)^2R\Delta V_{C_B}$	8.43 μF
Δi_{L_A}	0.5 A
Δi_{L_B}	0.8 A
ΔV_{C_A}	2 V
ΔV_{C_B}	1 V
$\mathrm{M}(D) = -\mathrm{D}(2-D)/(1-D)^2$	8.33

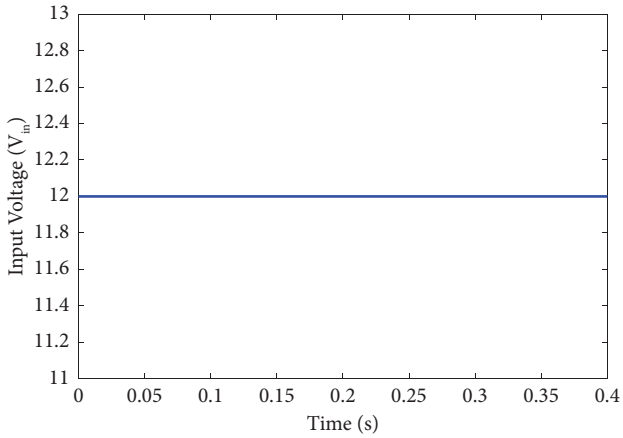

Figure 5: MATLAB simulated input voltage 12 V (V_{in}) waveform of the proposed configuration.

Figure 5 depicts a simulated waveform of input voltage (12 V) obtained from a DC voltage source. The simulated input current waveforms for the few switching cycles are displayed in Figure 6. The simulated waveform of the input current does not hit the zero level, as discussed in the theoretical analysis. As a result, the proposed converter

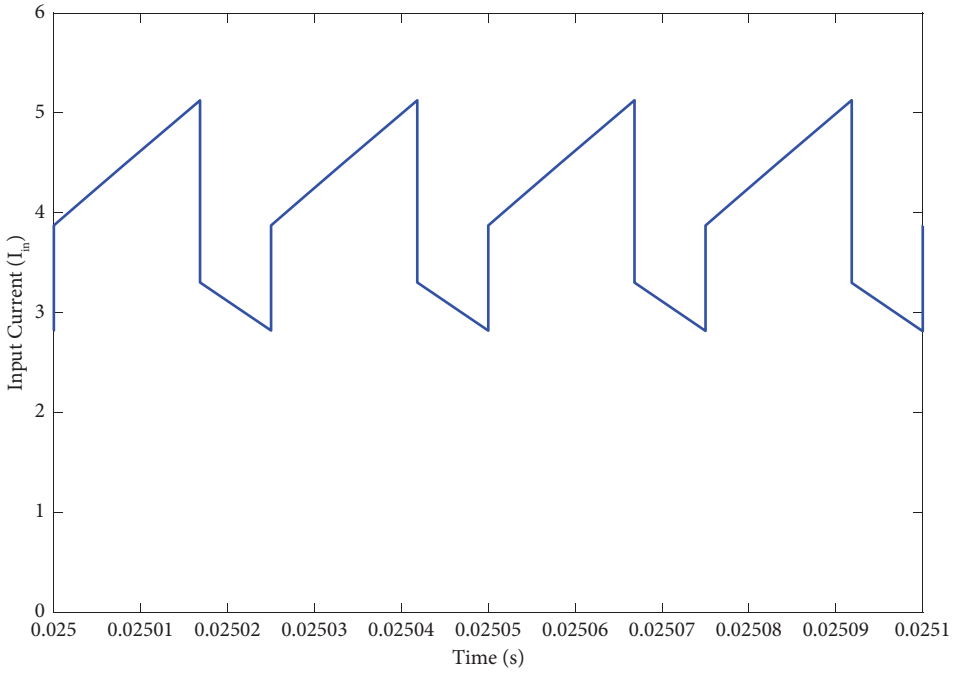

FIGURE 6: Simulation waveform of input current (I_{in}) showing the continuous operation.

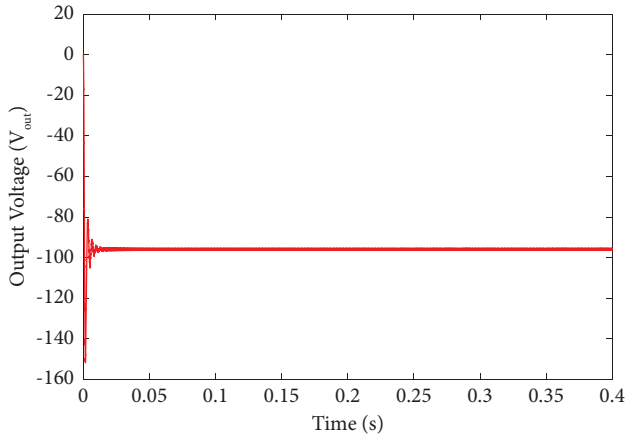

FIGURE 7: The simulation result of output voltage with a ripple of 0.94%.

generates a continuous input current, which is important in renewable energy systems.

Figure 7 depicts the simulated output DC voltage waveform. In the theoretical study, the output voltage is considered to be 100 V, while the simulation result shows an average of 95.95 V. The ripple in the output voltage is approximately 0.94%, which is well within the universal limitations (2%). The magnified version of the DC output current with a small ripple is shown in Figure 8. For a 100 V output voltage, the output load current is 0.5 A, according to theoretical calculations. The average value of the simulated waveform is 0.48 A.

The simulated waveforms of active switching elements are shown in Figures 9–12. Figures 9 and 10 illustrate the voltage and current waveforms of the active switch S_A. The waveforms of the voltages and currents of the active switch S_B are shown in Figures 11 and 12.

The simulated waveforms of passive switching elements are shown in Figures 13–16 (diodes). The voltage and current waveforms of the diode D_A are shown in Figures 13 and 14,

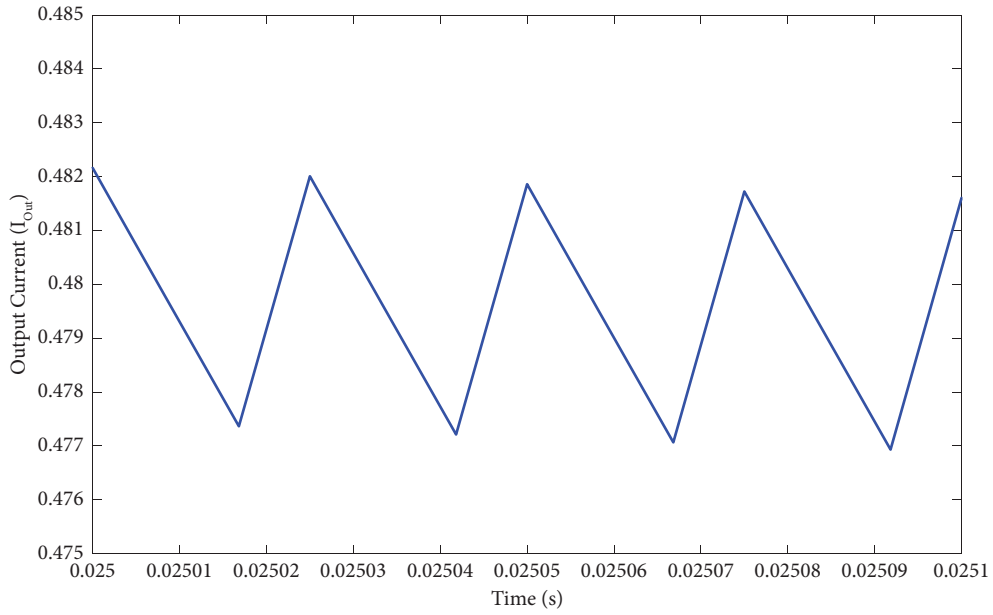

Figure 8: The simulation result of output current with an average value of 0.48 A.

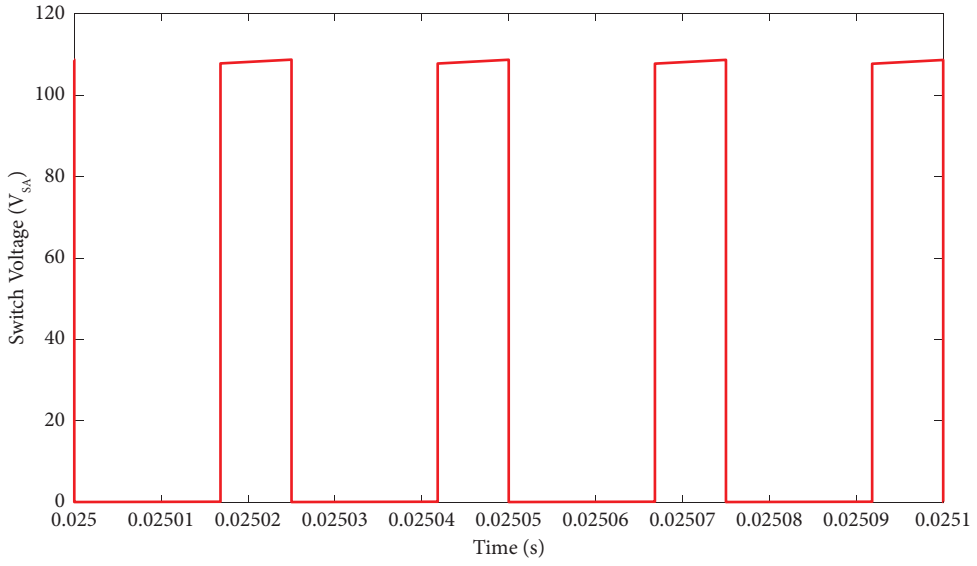

Figure 9: The switch S_A simulated voltage waveform.

whereas the voltage and current waveforms of the diode D_B are shown in Figures 15 and 16.

Both inductors' working modes are set to CCM with a permissible ripple, as indicated in the theoretical analysis. Equations (24) and (25) are used to compute the inductor L_A and L_B values for ripple currents of 0.5 and 0.8 amps. The computed current waveforms of inductors L_A L_B are shown in Figures 17 and 18. The ripple currents (Δi_{L_A}) (Δi_{L_B}) are the same as the theoretical values, as seen in these figures.

Using formulas (26) and (27), the capacitors are designed with a ripple voltage of 2 V and 1 V, respectively. Figures 19 and 20 illustrate the simulated voltage waveforms

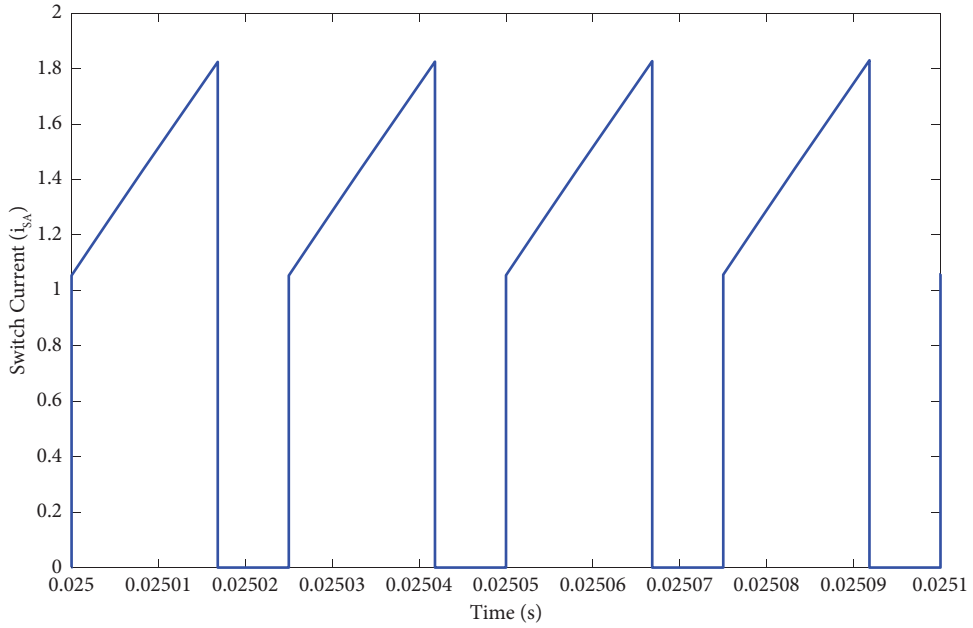

FIGURE 10: The switch S_A simulated current waveform.

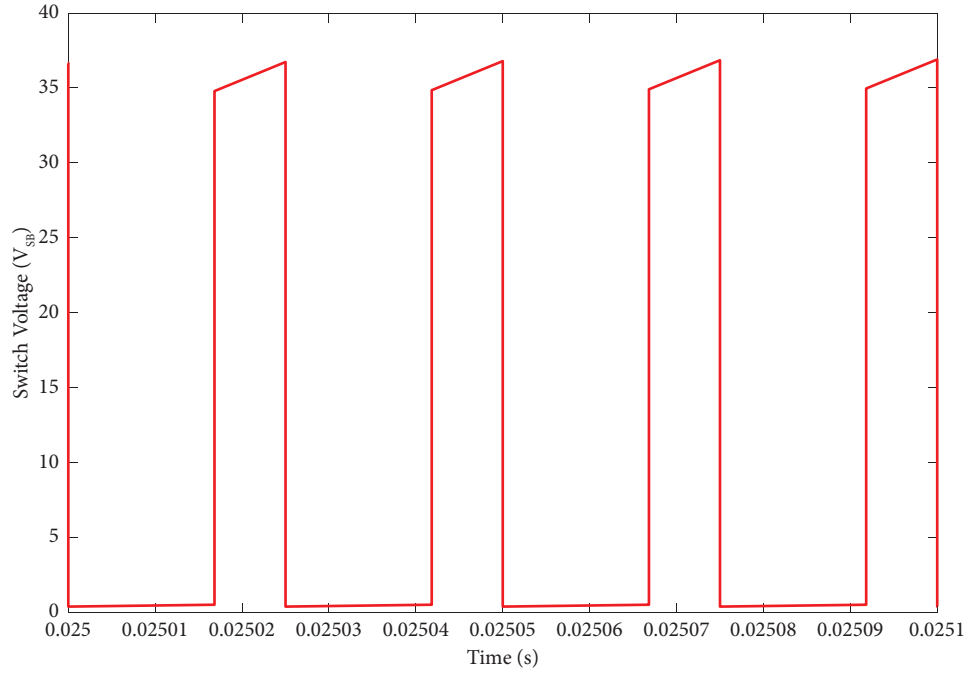

FIGURE 11: The switch S_B simulated voltage waveform.

of capacitors C_A C_B. The ripple voltages (ΔV_{CA}) and (ΔV_{CB}) are the same as the theoretical values, as shown in these figures.

Table 3 shows the performance of the proposed 2S2L-based buck-boost converter for various duty ratios. For duty ratios of 0.2 to 0.7, the proposed converter has an efficiency better than 90%, with high efficiency of 96.67% for duty ratios of 0.55 or 55%. With an efficiency of over 84%, the proposed converter has also demonstrated better performance at very low duty ratios. It is also worth noting that the

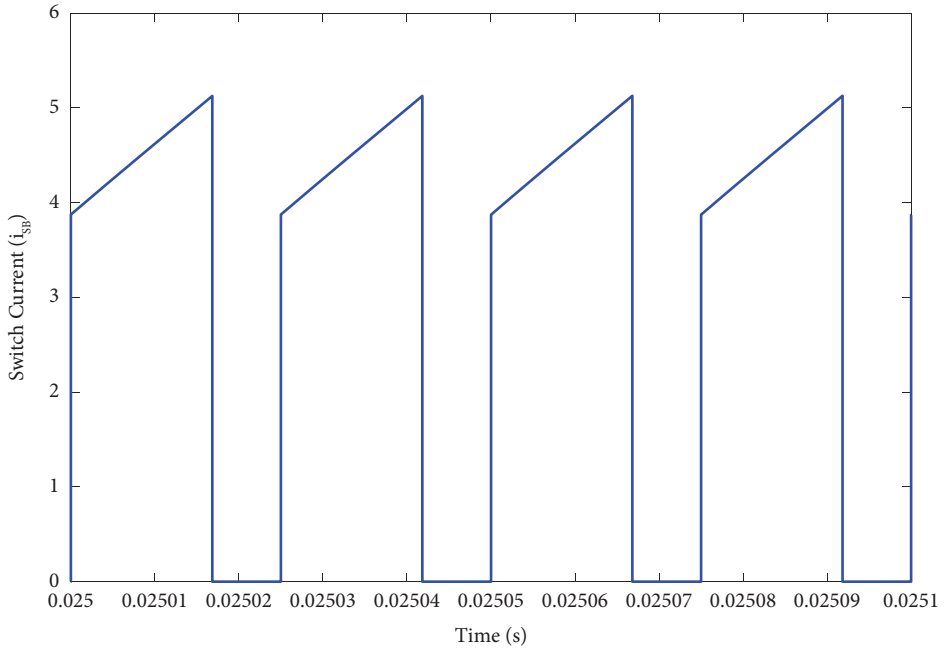

Figure 12: The switch S_B simulated current waveform.

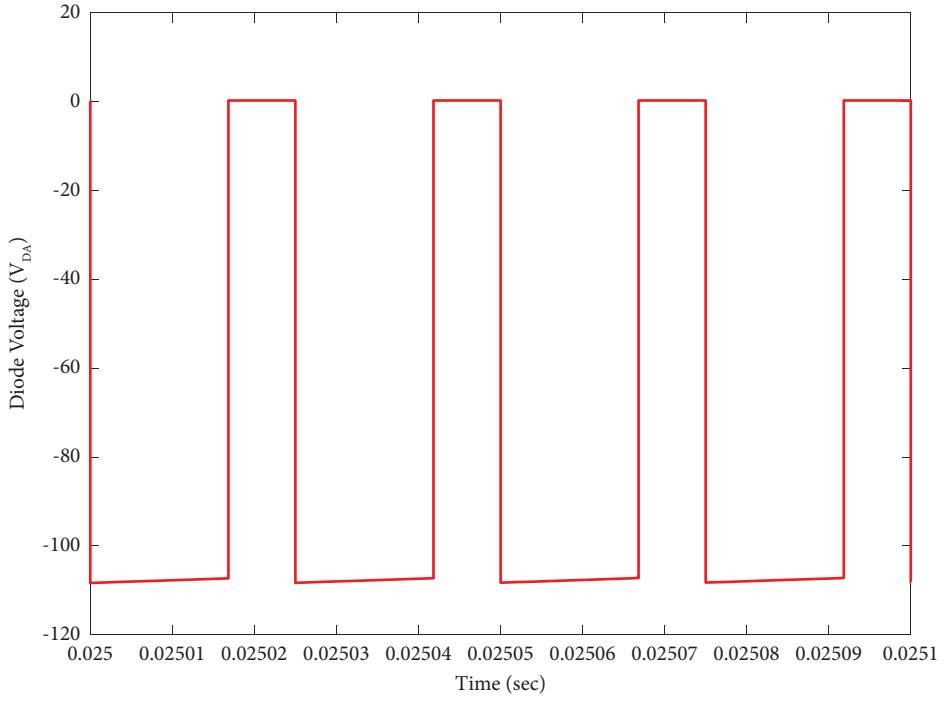

Figure 13: The diode D_A simulated voltage waveform.

proposed converter's ripple percentage is less than 2%, which is highly acceptable (universal acceptable range). The simulated values of the switching voltage stresses are displayed in Table 4 (both active and passive). Table 4 displays that the voltage stresses on the active switch S_A and the diode D_A are closer to the converter's output voltage.

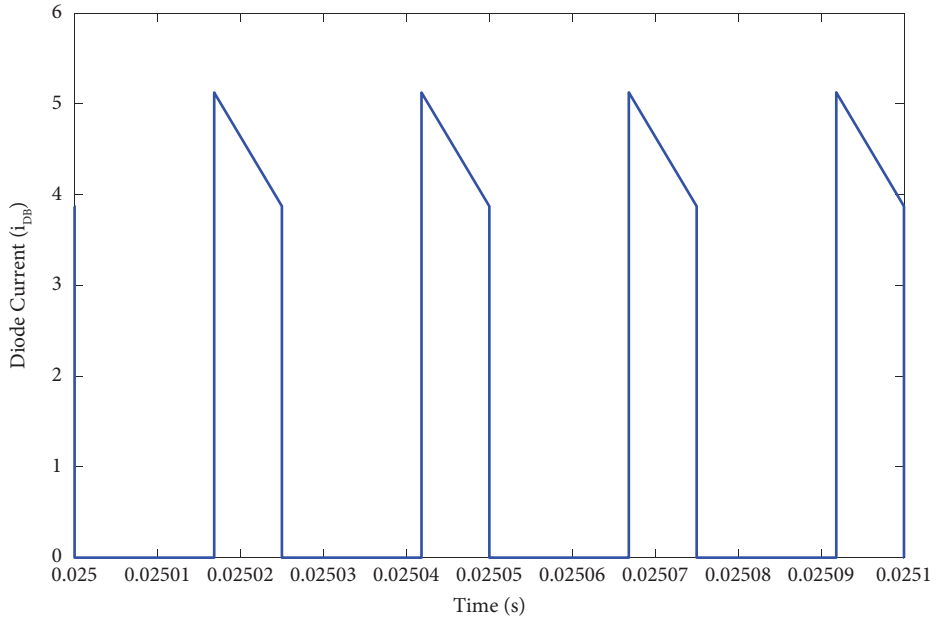

Figure 14: The diode D_A simulated current waveform.

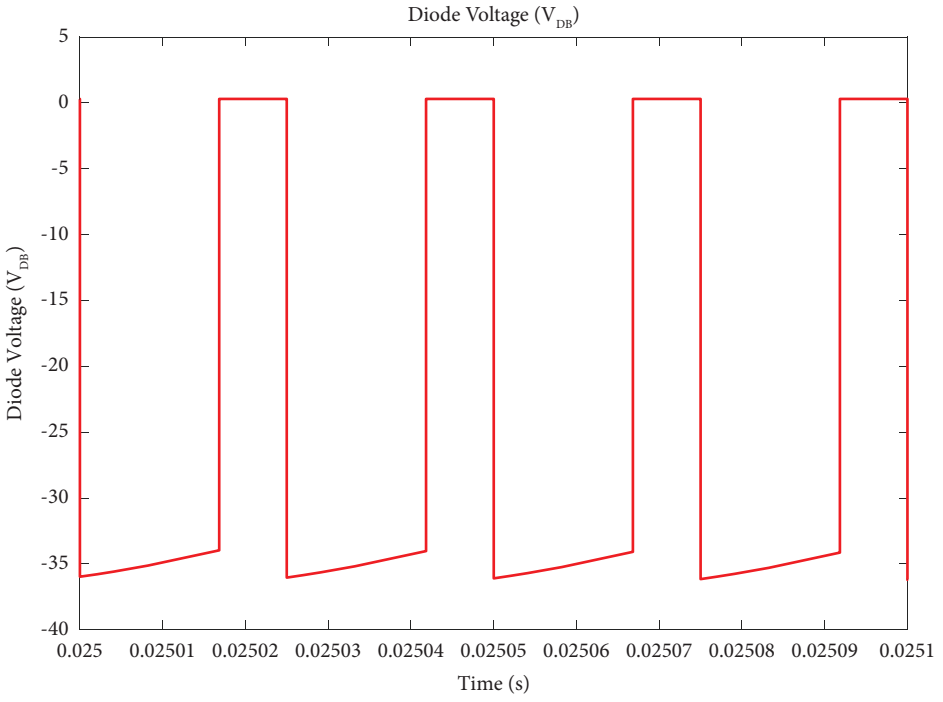

Figure 15: The diode D_B simulated voltage waveform.

When compared to the converter output, the voltage strains on the active switch S_B and the diode D_B are also quite low.

Figure 21 shows the performance curve of simulated output voltage (V_{out}) for different duty ratios (D). Figure 22 demonstrates the designed converter's efficiency curve in terms of duty ratio (D), and Figure 23 represents the plot of output ripple voltage (%) for various duty ratios (D).

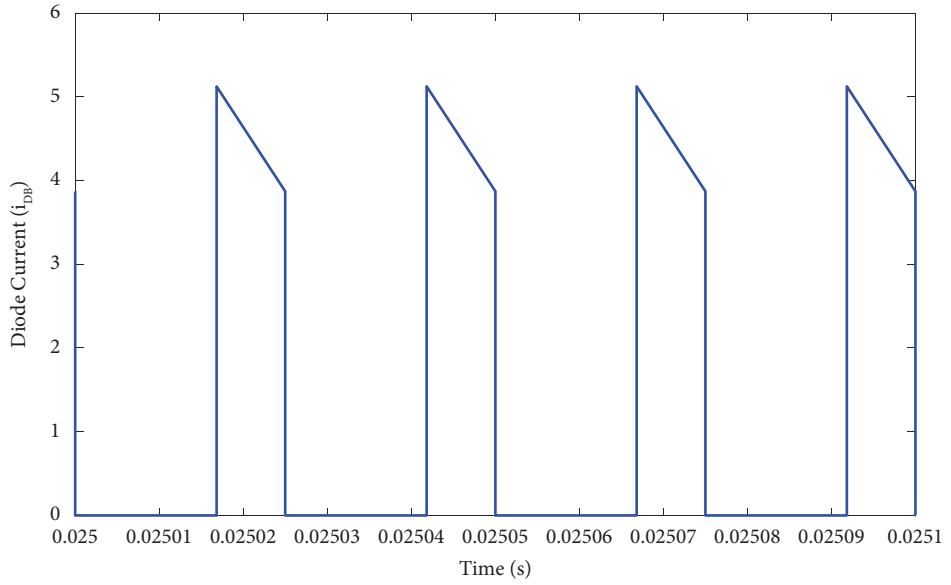

FIGURE 16: The diode D_B simulated current waveform.

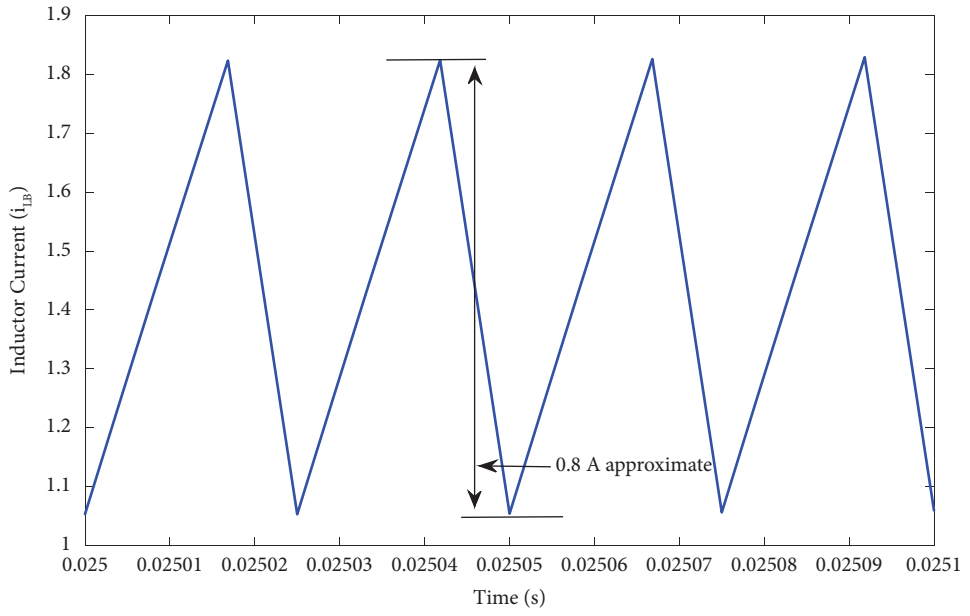

FIGURE 17: The inductor L_A simulated current waveform.

In Table 5, the proposed 2S2L circuit performance is presented for the designed duty ratio under light load conditions (below 50%). The load current as well as the output power of the configuration is varied as the load is changing. For a very light load (10%), the 2S2L converter performance is not up to the mark as it is designed for a full load (100%). However, as the load increases, the performance of the converter improves, which is recorded in Table 5. Figure 24 shows the performance of the 2S2L converter under light load conditions.

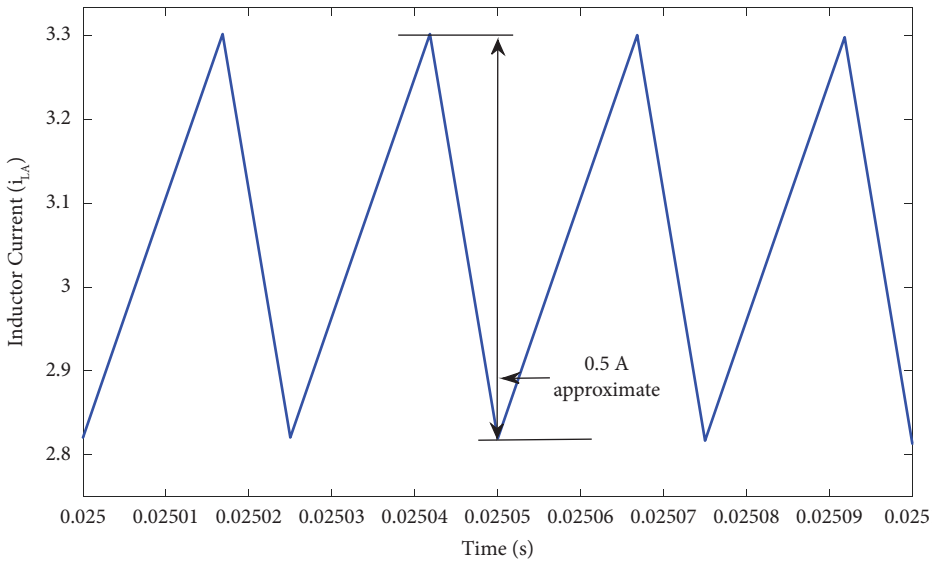

Figure 18: The inductor L_B simulated current waveform.

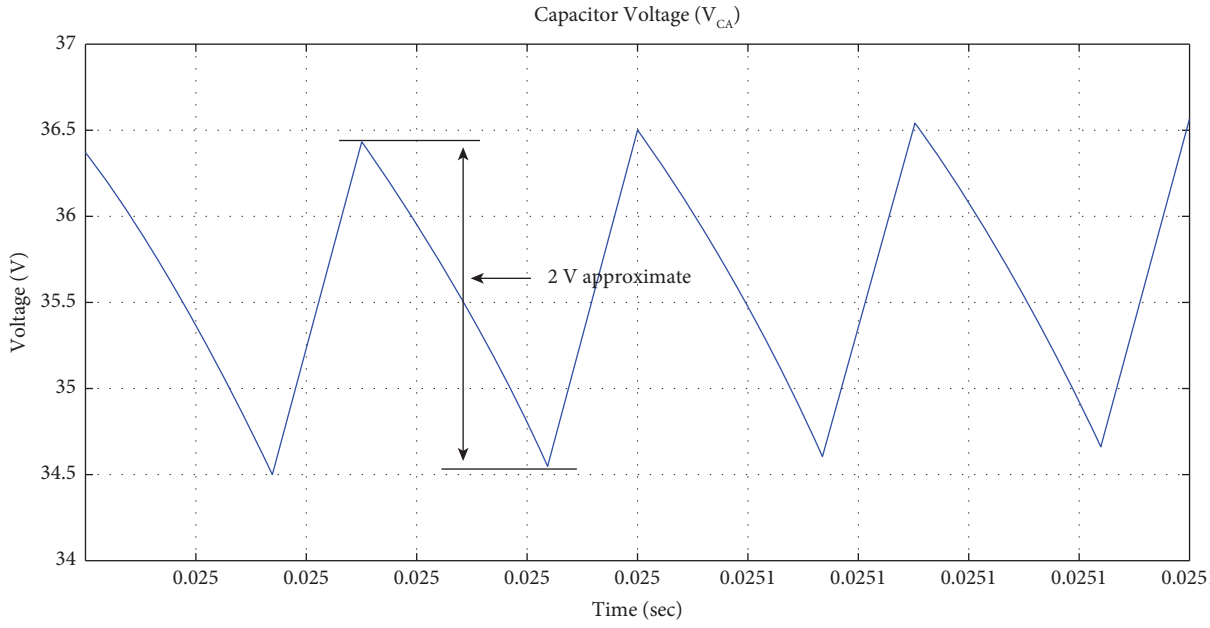

Figure 19: The capacitor C_A simulated voltage waveform.

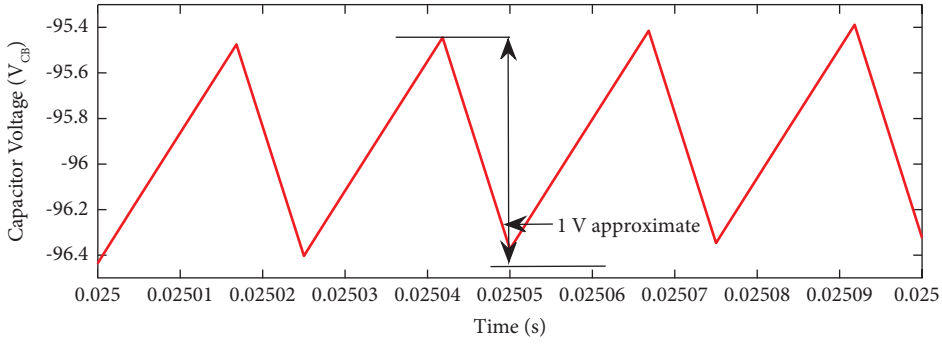

Figure 20: Simulated voltage waveform of capacitor C_B.

Table 3: Performance analysis for various duty ratios.

S.no	Duty ratio (D)	Output voltage (V_0)	% ripple	P_{in} (Watts)	P_0 (Watts)	% efficiency
1	0.1	4.761	0.5250	0.1341	0.1133	84.48
2	0.15	7.401	0.5404	0.3058	0.2738	89.53
3	0.2	10.09	0.4955	0.5544	0.5090	91.81
4	0.25	12.82	0.5460	0.8796	0.8217	93.41
5	0.3	15.56	0.5784	1.2852	1.2105	94.18
6	0.35	18.32	0.5458	1.7688	1.6781	94.87
7	0.4	21.06	0.6172	2.3268	2.2176	95.30
8	0.45	26.72	0.6736	3.7176	3.5697	96.02
9	0.5	34.91	0.5729	6.3168	6.0935	96.46
10	0.55	45.92	0.7621	10.9056	10.5432	96.67
11	0.6	61.14	0.8177	19.344	18.6904	96.62
12	0.65	82.84	0.8450	35.736	34.3123	96.01
13	0.673	95.95	0.9379	48.252	46.0272	95.38
14	0.7	114.7	0.8718	69.84	65.7804	94.18
15	0.75	162.1	0.9870	146.4	131.3820	89.74
16	0.8	227.3	1.0998	328.44	258.3264	78.65

Table 4: Active and passive switching voltage stresses.

S.no	Duty ratio (D)	Output voltage (V_0)	V_{S_A} Simulated	V_{S_B} Simulated	V_{D_A} Simulated	V_{D_B} Simulated
1	0.1	4.761	17.07	15.66	−16.75	−15.35
2	0.15	7.401	19.71	17.06	−19.39	−16.74
3	0.2	10.09	22.41	18.23	−22.08	−17.91
4	0.25	12.82	23.14	19.16	−24.81	−18.85
5	0.3	15.56	27.89	19.84	−27.57	−19.53
6	0.35	18.32	30.66	20.25	−30.33	−19.94
7	0.4	21.06	33.43	20.38	−33.10	−20.08
8	0.45	26.72	39.10	21.86	−38.78	−21.55
9	0.5	34.91	47.34	24.08	−47.02	−23.75
10	0.55	45.92	58.41	26.78	−58.08	−26.41
11	0.6	61.14	73.7	30.14	−73.36	−29.07
12	0.65	82.84	95.5	34.4	−95	−33.8
13	0.673	95.95	108.7	36.72	−108.32	−36.02
14	0.7	114.7	127.6	40	−127.15	−39
15	0.75	162.1	175	46.45	−175	−44.91
16	0.8	227.3	240.9	53	−240	−50

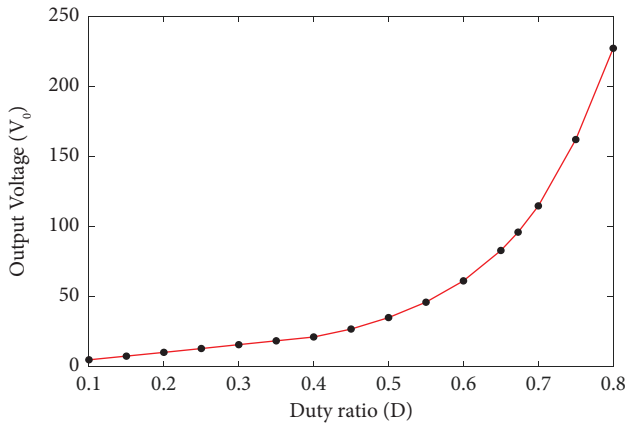

Figure 21: Performance curve of simulated output voltage (V_{out}) versus duty ratio (D).

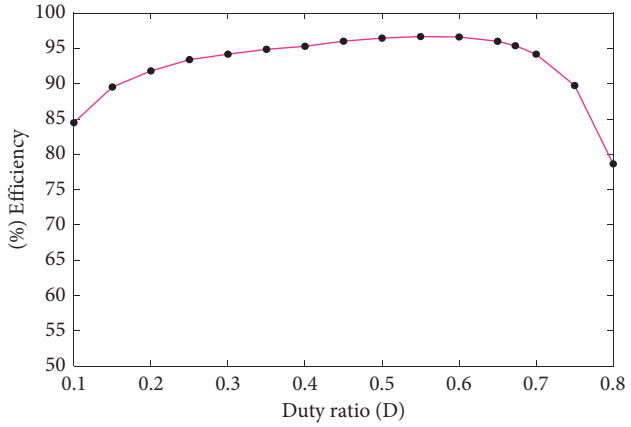

Figure 22: The designed converter's efficiency curve in terms of duty ratio (D).

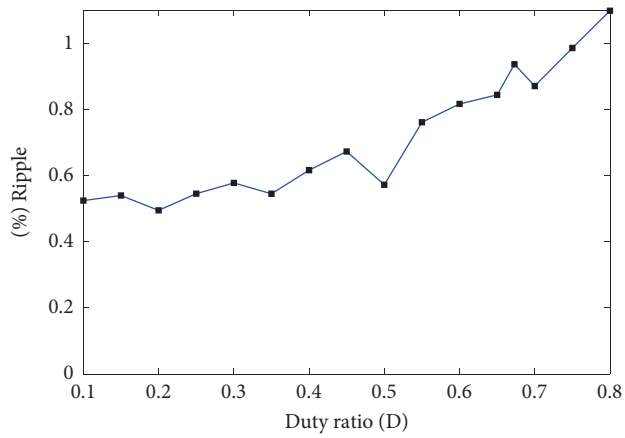

Figure 23: Plot of output ripple voltage (%) for various duty ratios (D).

Table 5: Performance of the converter under light load conditions.

S. no.	Load (%)	Output voltage (V)	Output current (A)	Output power (W)	Efficiency (%)
1	10	82.5	4.12	340	68
2	30	105.3	1.75	185	86
3	50	117.8	1.18	139	90
4	100	95.95	0.48	46	95.4

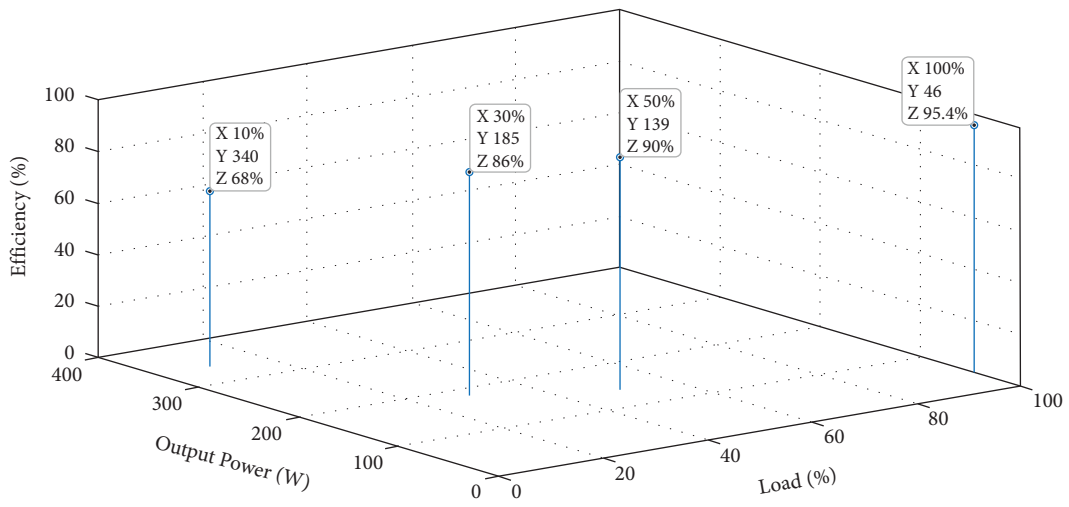

Figure 24: Performance of the proposed converter under light load conditions.

4. Conclusions

This proposed converter includes deep step-down and step-up voltages, as well as a percentage ripple of less than 2%, which is acceptable because it lowers the capacitor filter's output value. It can be observed that the proposed converter has an efficiency greater than 90% for duty ratios ranging from 0.2 to 0.7, with the highest efficiency of 96.67% at 55% or a 0.55 duty ratio. At duty ratios less than 0.2 or 20%, several other conventional converters have an efficiency less than 70%. The proposed converter, on the other hand, has an efficiency of 84% at such low duty ratios. The diode and switching stresses in the proposed converter are both low, which decreases losses. The proposed converter has several advantages, including being simple to modify by adding only four components to a traditional buck-boost converter, having a constant input current, a high voltage conversion ratio, and a simple control system. To achieve the step-up or step-down voltage, no transformers or coupled inductors are used. Furthermore, the proposed converter is low-cost and lightweight, and it can handle a wide range of duty ratios. Furthermore, the suggested converter has a lower rate of voltage stress on the switches as compared to the output voltage. According to the results, the designed converter has

a higher output voltage than the other topologies. The proposed converter is used in energy renewable systems, regenerative braking systems, and other industrial applications.

Data Availability

No data were used to support the findings of this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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Research Article

Design of New Nonisolated High Gain Converter for Higher Power Density

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A high gain nonisolated DC-DC converter using a single power semiconductor switch is proposed in this article. The operation of the proposed converter is explained under continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary conduction mode (BCM). The mathematical expressions for steady-state voltage gain, voltage stress, and current stress of diodes and switch are provided. Also, the design of inductors and capacitors in the CCM mode is explained with appropriate mathematical equations. The proposed topology is tested with a 200 W prototype at 50 kHz and a 60% duty cycle. The dynamic behavior of the proposed converter is examined by changing the duty cycle value and also load values. The proposed converter is verified with experimental results to prove the effectiveness of its operation. The proposed converter provides higher steady-state voltage gain as compared with recently developed topologies. The efficiency and power density of the proposed converter is 90% and 1.16 kW/L, respectively.

1. Introduction

The increase in carbon emission and depletion of natural resources due to nonrenewable power generation affects the environment largely. This downside makes a gaining reputation in incorporating the renewable energy sources (RES). The development of RES like photovoltaic (PV) and wind are evolving around the globe in recent years. As per the International Energy Agency report [1], RES will be the largest source of electricity generation globally in 2025. The increase in PV installation capacity motivates the researchers to focus more on the DC-DC power conversion topologies for effective utilization of RES power [2]. The development of DC-DC power conversion topologies mainly depends on few significant parameters such as high efficiency, high conversion ratio, transformerless configuration, control techniques, low size, and less cost.

The DC-DC converter can be classified broadly into two types such as isolated and nonisolated topologies [3]. The isolated topologies utilize a high-frequency transformer that acts as galvanic isolation between the source and the output as well as it increases the voltage gain of the converter by adjusting its turns ratio [4]. But it has certain drawbacks such as the higher volume and cost and saturation of the transformer. Considering RES application, the DC-DC converter plays vital role to provide good efficiency, high voltage gain, and low cost. Therefore, the development of new nonisolated topology for RES application is considered to be the right choice. But the nonisolated DC-DC converter topology should provide high voltage gain at low duty cycle which is the key challenge for designing a new topology. Though several changes have been incorporated on the traditional nonisolated converters to improve the voltage gain [5], but still there is the necessity to develop a new converter with high voltage gain at a low duty cycle with reduced stress.

A voltage lift technique based on the high step-up DC-DC converter has developed in [6] for providing high voltage gain, but it utilizes two switches that may lead to increase in power loss of the converter. In [7], the buck-boost converter based on the ZETA converter has been designed with the single power semiconductor switch for automobile electronics. It has focused on both step-up and step-down conversion. The hybrid

converter has been developed [8] by combining the cuk and boost converter that provides low output ripple and high voltage gain. It supports the hybridizing two input power sources such as photovoltaic cells, fuel cells, and battery. But the power loss is high due to multiple switches thereby reducing the efficiency [8]. The quadratic boost converter topology has been developed [9] such that it provides high voltage gain as compared with a conventional boost converter. But the topology has utilized two switches for achieving high voltage gain thereby increasing the overall loss of the converter and reducing the efficiency [9]. Many transformerless hybrid converter topologies have been developed with the help of voltage multiplier cells, switched capacitor, and switched inductor combinations for providing high voltage gain [10]. An improved hybrid topology has been developed [11] by combining the switched inductor and switched capacitor cells. The topology provides reasonable voltage gain at less duty cycle, but it utilizes three switches [11]. Voltage multiplier cells (VMC) are one of the best methods to increase the converter's voltage gain. The development of high step-up converters with different multiplier cells continuously evolves yearly to improve their power density, efficiency, and fast dynamic response for different advantages and applications. Therefore, in this article, a new voltage multiplier cell is proposed with two inductors, two diodes, and four capacitors to provide the maximum voltage gain and reduced voltage stress across the main switch.

The advantages of the proposed converter are given below:

(i) The proposed converter utilizes single switch with less voltage stress (0.59 times of output voltage) which produces higher voltage gain ($G = 10.75$) at 60% duty cycle

(ii) The power density and efficiency of the proposed converter are 1.16 kW/L and 90%, respectively

(iii) The dynamic behavior of proposed converter is examined under varying duty cycles and load conditions

Furthermore, the operation of the proposed converter is examined through the laboratory-based experimental prototype with 200 W.

2. Operation of the Proposed High Gain DC-DC Converter

The proposed high gain DC-DC converter topology is developed by combining the modified quadratic boost converter (MQDBC) with the unique voltage multiplier cell (VMC). The proposed high gain DC-DC converter topology is shown in Figure 1, which consists of single switch (S_1), five inductors (L_1, L_2, L_3, L_4 and L_5), seven capacitors ($C_1, C_2, C_3, C_4, C_5, C_6$, and C_o), six diodes (D_1, D_2, D_3, D_4, D_5 and D_6), and load R_0. It has two modes of operation such as mode-I and mode-II in CCM. The topology consists of multiple components, but it operates at less duty cycle to provide higher voltage gain with reduced voltage and current stress which is the significant aspect of the proposed topology.

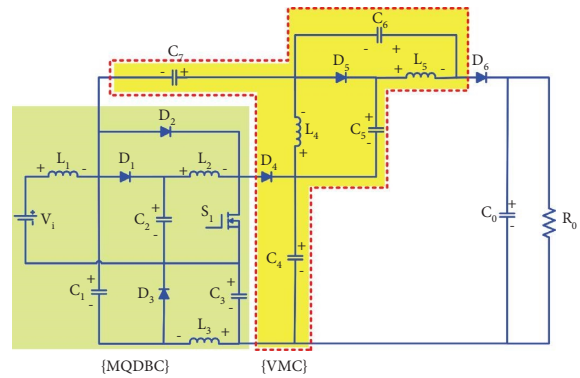

Figure 1: Proposed high gain DC-DC converter.

2.1. Continuous Conduction Mode

2.1.1. Mode-I. The operation of mode-I is explained when the switch is closed. The current path is shown in Figure 2, where the energy from the DC input charges the inductor L_1, and the capacitor C_2 charges the inductor L_2. The capacitor C_4 charges the inductor L_4 and C_5 charges inductor L_5. The combined charge of the capacitors C_4 and C_5 supports for charging the capacitors C_3, C_6, and C_7. The capacitor C_1 supports to charge the capacitor C_3 and inductor L_3. The capacitor C_0 discharges the stored charge to the load:

$$\left\{\begin{array}{c} V_{L1} = V_i; V_{L2} = V_{C2}; V_{L3} = V_{C1} - V_{C3} \\ V_{L4} = V_{C4} - V_{C3} - V_{C7}; \\ V_{L5} = V_{C4} + V_{C5} - V_{C6} - V_{C3} - V_{C7} \end{array}\right\}. \quad (1)$$

2.1.2. Mode II. The operation of mode-II is explained with two stages of operation when the switch is opened. The current path of the first stage of operation is shown in Figure 3. Here, the energy stored in inductor L_1 and the energy from DC source charges the capacitor C_1 through D_3. The stored energy in the inductor L_2 & L_3 and the capacitors C_2 & C_3 discharge through D_3 and D_4 to the capacitor C_4. It should be noted that the capacitor C_2 makes the D_1 to be in reverse biased condition due to $V_{C2} > V_{C1}$. The inductor L_4 charges the capacitor C_5 through D_5. The stored energy in the capacitor C_7, C_6, and inductor L_5 discharges through D_6 to charge the capacitor C_0 and supply the energy to the load.

In the second stage of operation, $V_{C2} < V_{C1}$ makes the diode D_1 in forward-biased condition. Therefore, the energy from the DC source charges the capacitor C_2 through D_1. The changes in current flow of the capacitor C_3, C_4, and inductor L_3 occurs, which is predicted as shown in Figure 4:

$$\left\{\begin{array}{c} V_{L1} = V_i - V_{C2} = V_i - V_{C1} \\ V_{L2} = V_{C2} + V_{C3} - V_{C4} \\ V_{L3} = -V_{C3}; V_{L4} = -V_{C5} \\ V_{L5} = -V_{C6} \\ V_0 = V_i - V_{L1} + V_{C7} + V_{C6} + V_{C3} \end{array}\right\}. \quad (2)$$

The analytical waveform of the proposed converter under CCM is illustrated in Figure 5. Applying the volt-sec

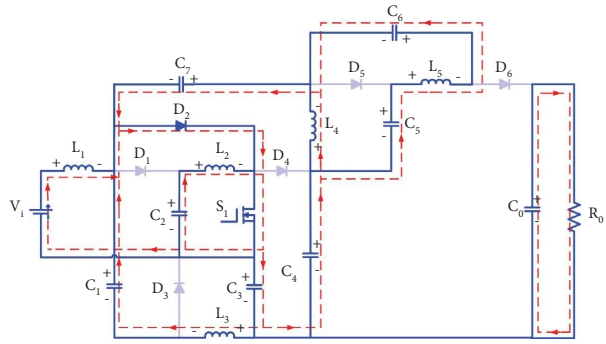

Figure 2: Equivalent circuit of proposed in mode-I.

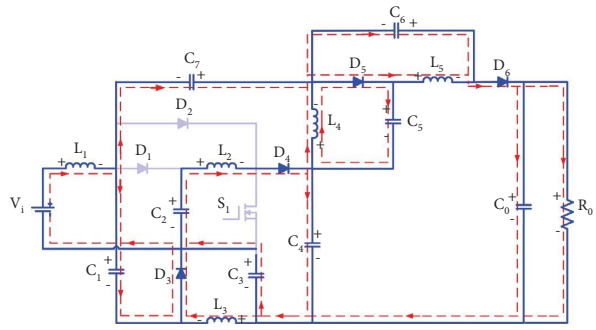

Figure 3: Equivalent circuit of proposed converter in mode II (first stage).

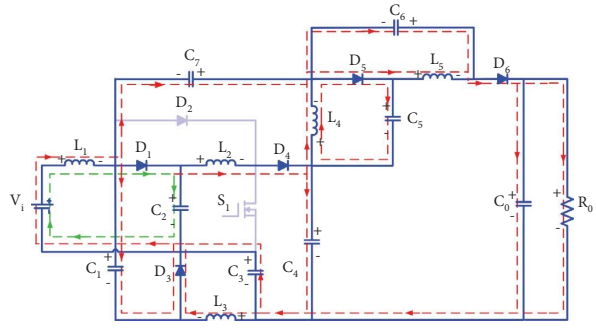

Figure 4: Equivalent circuit of the proposed converter in mode II (second stage).

balance principle on the inductors (L_1toL_5), the following expressions can be obtained:

$$\left\{\begin{array}{l} V_{C1} = V_{C2} = \dfrac{V_i}{1-D}; V_{C3} = V_{C5} = V_{C6} = \dfrac{DV_i}{1-D} \\ V_{C4} = \left[\dfrac{1+D-D^2}{(1-D)^2}\right]V_i; V_{C7} = \left[\dfrac{\left(2\ D-D^2\right)}{(1-D)^2}\right]V_i \end{array}\right\}, \quad (3)$$

$$V_i - V_{L1} + V_{C7} + V_{C6} + V_{C3} = V_0. \quad (4)$$

The proposed converter steady-state voltage gain (M) is derived by solving the equations (3) in (4) as

$$\left\{M = \frac{V_0}{V_i} = \frac{1+3\ D-3D^2}{(1-D)^2}\right\}. \quad (5)$$

2.2. Discontinuous Conduction Mode. The operation of the proposed converter in DCM is divided into three instants. At the first instant ($t_0 < t < t_1$), the switch S_1 is closed. It is similar to the mode-I operation in CCM. At the second instant ($t_1 < t < t_2$), the switch S_1 is opened and the inductor starts to decay. It is also similar to mode-II operation in CCM. At the third instant ($t_2 < t < t_3$), the switch S_1 is still opened and the inductor currents decays to zero. The equivalent circuit of DCM mode for this instant is shown in

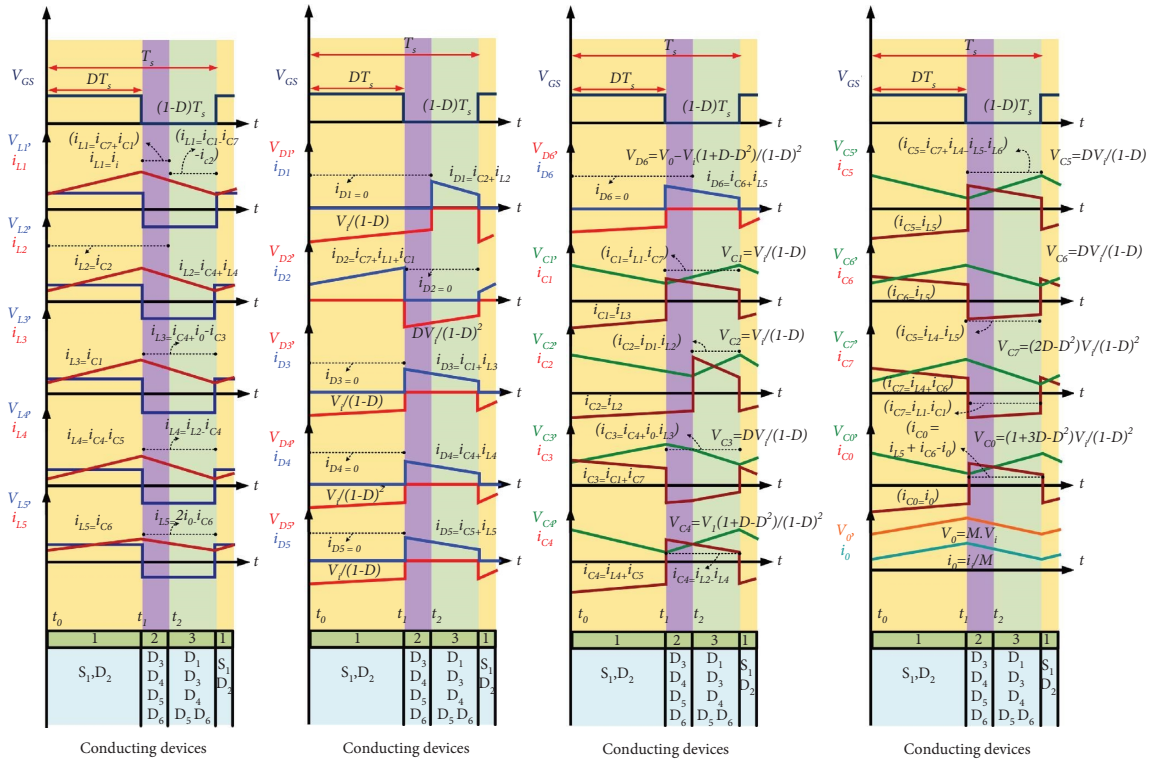

Figure 5: Analytical waveform of the proposed converter under CCM operation for one switching cycle.

Figure 6. It is noted that all the diodes are in reverse biased condition, and the stored energy in capacitor C_6 is discharged to the load R_0.

Applying the volt-sec balance principle across the inductors L_1, L_2, L_3, L_4, and L_5 under DCM operation, the voltage gain and duty cycle can be obtained as follows:

$$G_{\mathrm{DCM}} = \frac{V_0}{V_i} = 1 + \frac{5\ D}{D_{m2}} + \frac{D^2}{D_{m2}^2}, \tag{6}$$

$$D_{m2} = \frac{D}{1.5}. \tag{7}$$

From the analytical waveform of the DCM operation, as shown in Figure 7(a), the average current of diode D_6 is derived, and it is expressed as given below:

$$i_{D6\_\mathrm{avg}} = \frac{1}{2} D_{m2} \frac{V_i D}{L_{eq} f_s}. \tag{8}$$

The duty cycle of "D_{m2}" is calculated as follows:

$$D_{m2} = \frac{K_L G_{\mathrm{DCM}}}{D}. \tag{9}$$

The voltage transfer gain (G_{DCM}) can be obtained by equating (7) and (9)as

$$G_{\mathrm{DCM}} = \frac{D^2}{1.5 K_L}, \tag{10}$$

where K_L is the normalized inductor time constant, which is given as

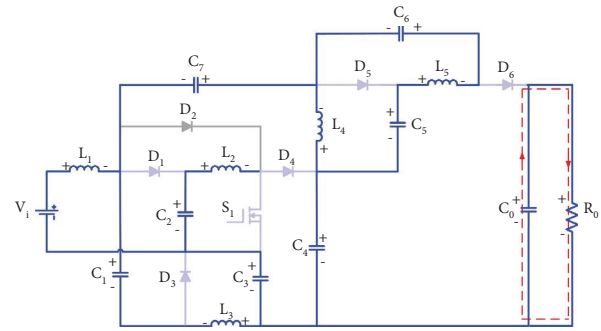

Figure 6: Equivalent circuit of the proposed converter in DCM.

$$K_L = \frac{L_{eq} f_s}{R}. \tag{11}$$

Figure 7(b) shows the plot between voltage gain versus duty cycle under CCM and DCM operation.

2.3. Boundary Conduction Mode. When the proposed converter is operated at the boundary of CCM and DCM, then the voltage gain of CCM and DCM is equal. Therefore, the normalized boundary inductor time constant "K_B" is found by equating (5) and (10) as

$$K_b = \frac{D^2 (1 - D)^2}{\left(1 + 3\ D - 3D^2\right)}. \tag{12}$$

From Figure 7(c), it is evident that if the "K_b" is larger than "K_L," then the converter operates in DCM else in CCM.

2.4. Design Considerations. The accurate design of proposed converter components is necessary to obtain the desired outcome. The voltage ripple and current ripple equations can be determined by applying amp-sec balance and volt-sec balance on the proposed converter capacitors and inductors, respectively:

$$\left\{\begin{array}{c} i_{L5}=2i_0(1-D);\, i_{C5}=2i_0;\, i_{C6}=\dfrac{i_0[2(D-1)]}{(1-D)} \\ i_{L4}=2i_0\left[(1-D)+(1-D)^2\right]-i_0\left[\dfrac{(2\,D-1)^2}{(1-D)}\right] \\ i_{L2}=\dfrac{i_{L4}+(2\,D-1)i_{C5}}{(1-D)};\, i_{C4}=2i_0D-i_{L4}+i_{L2} \\ i_{L3}=i_0(D-1)+i_{C4}(2\,D-1);\, i_{C2}=\dfrac{i_{L2}D}{(1-D)} \\ i_{C7}=\dfrac{(2i_0-i_{L5})(1-D)}{D}+i_{L4};\, i_{L1}=\dfrac{i_{L3}D}{1-D}+i_{C7}+i_{C2} \end{array}\right\}. \tag{13}$$

Here, f_s is the switching frequency of the switch S_1:

$$\left\{\begin{array}{c} \Delta i_{L1}=\dfrac{V_iD}{L_1f_s};\, \Delta i_{L2}=\dfrac{V_iD}{(1-D)L_2f_s};\, \Delta i_{L3}=\dfrac{V_iD}{L_3f_s} \\ \Delta i_{L4}=\dfrac{V_iD}{L_4f_s};\, \Delta i_{L5}=\dfrac{V_iD^2}{(1-D)L_5f_s} \end{array}\right\}. \tag{14}$$

The capacitor ripple voltage are as follows:

$$\left\{\begin{array}{c} \Delta V_{C1}=\dfrac{i_{C1}(1-D)}{C_1f_s} \\ \Delta V_{C2}=\dfrac{(i_{L1}-i_{C1}-i_{L5}+i_{C6}-i_{L2})(1-D)}{C_2f_s} \\ \Delta V_{C3}=\dfrac{(i_{C1}+i_{L4}+i_{C6})D}{C_3f_s};\, \Delta V_{C4}=\dfrac{i_{L2}(1-D)}{C_4f_s} \\ \Delta V_{C5}=\dfrac{i_{L4}(1-D)}{C_5f_s};\, \Delta V_{C6}=\dfrac{i_{C6}D}{C_6f_s} \\ \Delta V_{C7}=\dfrac{(i_{L4}+i_{C6})D}{C_7f_s};\, \Delta V_{C0}=\dfrac{(i_{L5}+i_{C6})(1-D)}{C_0f_s} \end{array}\right\}. \tag{15}$$

2.5. Voltage and Current Stress Analysis. From the mode-I, the voltage stress of the diodes $D_{1,3,4,5,6}$ and current stress of the switch S_1 and diode D_2 can be determined as

$$\left\{\begin{array}{c} V_{D1}=V_{D3}=V_{D5}=\dfrac{V_i}{1-D} \\ V_{D4}=\dfrac{V_i}{(1-D)^2};\, V_{D6}=V_0-V_i\left[\dfrac{1+D-D^2}{(1-D)^2}\right] \end{array}\right\}, \tag{16}$$

$$\{i_{D2}=(i_{L1}+i_{C7})D;\, i_{S1}=(i_{L1}+i_{C7}+i_{L2})D\}.$$

From the mode-II, the voltage stress of diode D_2, switch S_1, and current stress of the diodes $D_{1,3,4,5,6}$ can be calculated as

$$\left\{V_{D2}=\frac{DV_i}{(1-D)^2};\, V_{S1}=\frac{V_i}{(1-D)^2}\right\},$$

$$\left\{\begin{array}{c} i_{D1}=(i_{C2}+i_{L2})(1-D);\, i_{D3}=(i_{C1}+i_{L3})(1-D) \\ i_{D4}=i_{L2}(1-D);\, i_{D5}=(i_{C5}+i_{L5})(1-D) \\ i_{D6}=(i_{C6}+i_{L5})(1-D) \end{array}\right\}. \tag{17}$$

3. Comparison with Recently Developed Quadratic Topologies

This section presents the comparison of proposed high gain DC converter with recently developed nonisolated topologies. Figure 8(a) illustrates the comparison of voltage gain with various duty cycles. It is worth mentioning that the proposed converter provides higher voltage gain when compared to the topologies developed in [12–23]. Figure 8(b) clearly depicts the total semiconductor switch utilization and operating duty cycle of the proposed converter with other recently developed topologies. From Figure 8(b), it is clearly understood that the proposed converter utilizes a single semiconductor switch as compared with the topologies developed in [12–18, 22, 23]. Increase of semiconductor switch may increase the size of the converter and decrease the power density of the converter. The converters developed in [13–16, 18, 22, 23] were operated at higher duty cycle to obtain reasonable voltage gain which shall increase the conduction loss of the converter. The ratio of voltage gain (M) to Total Component Count (TCC) is measured to find the component utilization factor of the converter. The proposed converter is operated at a duty cycle of 60% which provides a voltage gain of 10.75. Figure 8(c) shows the comparison of M/TCC ratio of the proposed converter with recently developed topologies at duty cycle of 60%. It is noted that the proposed converter developed converter in [17, 22] has a same ratio (0.55), but those topologies utilizes more than a single semiconductor switch. Also, the component utilization factor is performed for a higher duty cycle of 0.8 for all converters, as shown in Figure 8(d). It is noted that the proposed converter has a higher M/TCC ratio as compared with other developed converters in [13, 15–23].

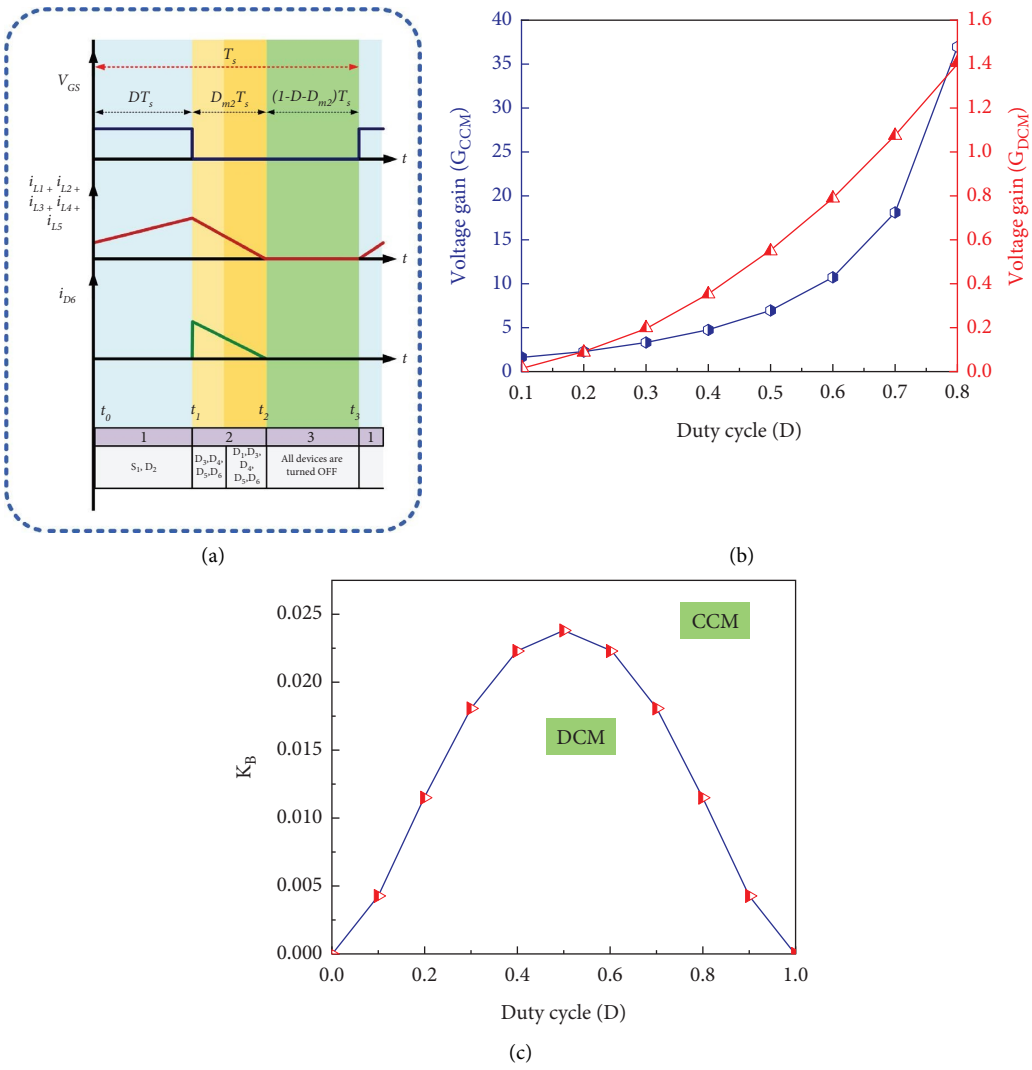

FIGURE 7: (a) Analytical waveform under DCM operation. (b) Voltage gain of CCM and DCM versus duty cycle. (c) (K_b) vs duty cycle.

4. Experimental Results

In order to validate the functionality of the proposed converter in CCM operation, a laboratory-based 200 W prototype is developed. The proposed converter is operated at 50 kHz for an input voltage of 20 V with 60% duty ratio. The parameter of the proposed converter are listed in Table 1.

The maximum height of the prototype is 1.65 inch, and the total area is 6.35 inch^2. Therefore, the power density of the proposed converter is 1.16 kW/L. Figure 9(a) shows the input and output voltage waveform of the proposed converter where the output waveform is maximized in Figure 9(a) to show the magnitude of ripple voltage. It is 1.7% of the output voltage which is similar to the designed value. The obtained experimental result of output voltage is found to be 204 V which is 5% lower than the theoretical value. Figure 9(b) shows the input and output current waveform. The maximum value of input (I_{in}) and output current (I_0) obtained from the experimental result are 11 A and 0.88 A, respectively. The experimental results confirm that the output current is found to be continuous at 60% duty cycle. Therefore, the proposed topology is more suitable for renewable energy applications. Figure 9(c) represents the voltage and current stress of the switch. The maximum voltage across the switch during OFF-state is 121 V. During the ON-state, the maximum current flowing through the switch is 16.9 A. Figures 9(d)–9(f) show the voltage across the diodes. It is observed that the average voltage of diode D_4 blocks the maximum voltage as compared with other diodes.

The reverse peak voltage of the diodes is $V_{R\,D1,3,5\_peak}$ = 44 V, $V_{R\,D2\_peak}$ = 79 V, $V_{R\,D4\_peak}$ = 121 V, and $V_{R\,D6\_peak}$ = 46 V. The maximum voltage across the capacitor is shown in Figures 9(g)–9(j). The maximum value of the individual capacitor voltage is V_{C1} = 48 V, V_{C2} = 49 V, V_{C3} = 29.1 V, V_{C4} = 151.4 V, V_{C5} = 27 V, V_{C6} = 26.9 V, V_{C7} = 102.2 V, and V_{C0} = 204 V. These values are closely matched with the designed values. The dynamic behavior of the proposed converter is examined by changing the duty ratio and load values. Figure 9(k) shows the output voltage and output current for change in load. The values of the

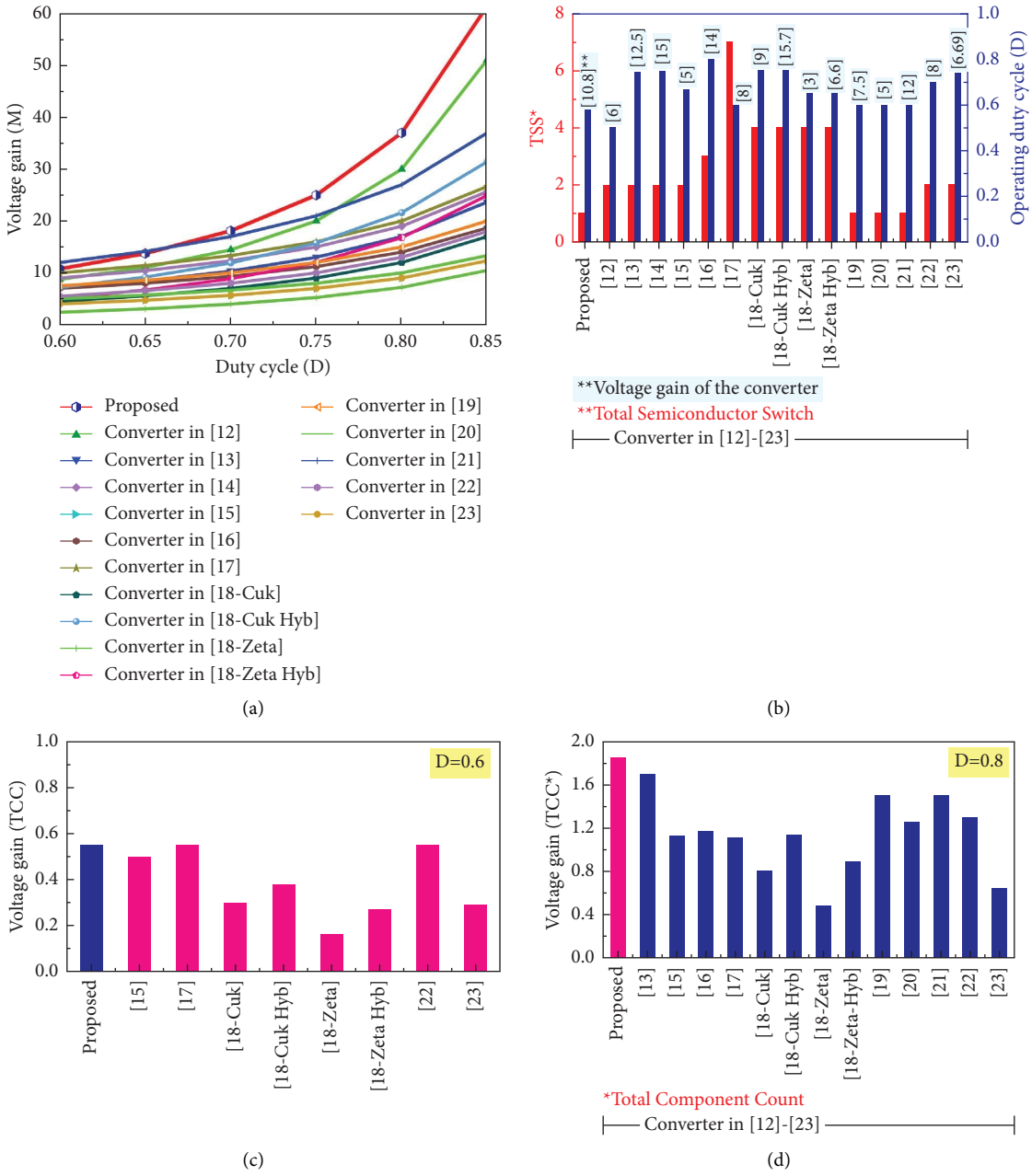

FIGURE 8: Comparison of the proposed converter with recently developed converters found in [12–23]. (a) Voltage gain vs duty cycle. (b) TSS vs duty cycle. (c) Voltage gain/TCC for $D = 0.6$. (d) Voltage gain/TCC for $D = 0.8$.

resistive load is adjusted (i.e., R = 308Ω, R = 230Ω, and R = 230Ω) at 60% duty cycle. It is observed that the output voltage is maintained constant, and the output current varies with the load. Figure 9(l) shows the variation in output voltage for the various duty cycles. The proposed converter is tested by varying the duty cycle (i.e., $D = 0.4$, 0.5, and 0.6) for a constant load of R = 185Ω.

The power loss and efficiency of the proposed converter are analyzed to show the effectiveness of the proposed converter. The expression for the total power loss is

$$\left\{P_{\text{Loss}} = P_{\text{ind}} + P_{\text{cap}} + P_{\text{switch}} + P_{\text{diode}}\right\}, \tag{18}$$

where P_{ind} and P_{cap} are the total power loss of the inductors and capacitors, respectively. P_{switch} and P_{diode} are the total

Table 1: Specifications of the proposed converter.

Component	Values	Dimension
Inductors	$L_1 = 1.2$ mH, $L_2 = 3$ mH, $L_3 = L_4 = 1$ mH, $L_5 = 1.4$ mH	1.5 inch $(L) \times 1.15$ inch $(B) \times 1.08$ inch (H)
Capacitors	$C_1 = C_2 = 12\,\mu$F(ESY156M063AC3), $C_4 = C_7 = 10\,\mu$F (ESK106M160AH1), $C_3 = C_5 = 33\,\mu$F (ESY336M050AG1), $C_6 = 6.8\,\mu$F (ESY685M050AC2) and $C_0 = 5.6\,\mu$F (ESK685M250AG3)	0.43 inch $(L) \times 0.19$ inch (D), 0.47 inch $(L) \times 0.39$ inch (D), 0.28 inch $(L) \times 0.31$ inch (D), 0.28 inch $(L) \times 0.19$ inch (D), 0.43 inch $(L) \times 0.31$ inch (D)
Diodes	$D_1 = D_3 = D_5 = D_6 =$ MUR1610CTG, $D_2 =$ MUR1615CTG $D_4 =$ STTH2002)	0.42 inch $(L) \times 0.19$ inch $(B) \times 1.18$ inch (H) 0.41 inch $(L) \times 0.18$ inch $(B) \times 1.17$ inch (H)
MOSFET	IXFH120N30X3	0.62 inch $(L) \times 0.19$ inch $(B) \times 1.65$ inch (H)

L-length, B-breadth, H-height, D-diameter.

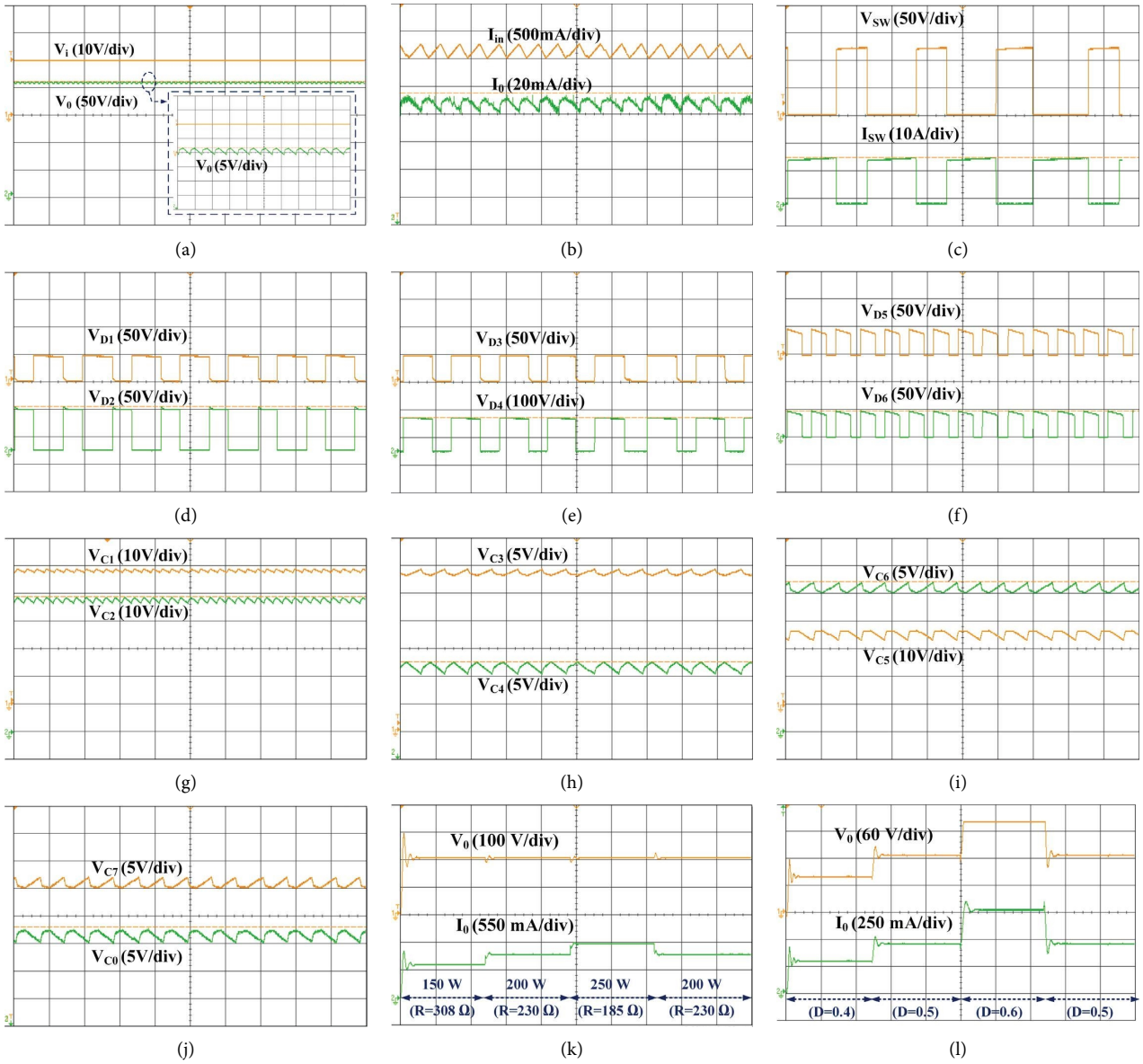

Figure 9: (a) Input and output voltage, (b) input and output current, (c) voltage and current stress on switch, voltage across diodes, (d)D_1 and D_2, (e)D_3 and D_4, (f)D_5 and D_6, (g) voltage across capacitors C_1 and C_2, (h)C_3 and C_4, (i)C_5 and C_6, (j)C_7 and C_0, (k) output voltage and output current for the varying load, and (l) output voltage for the varying duty cycle.

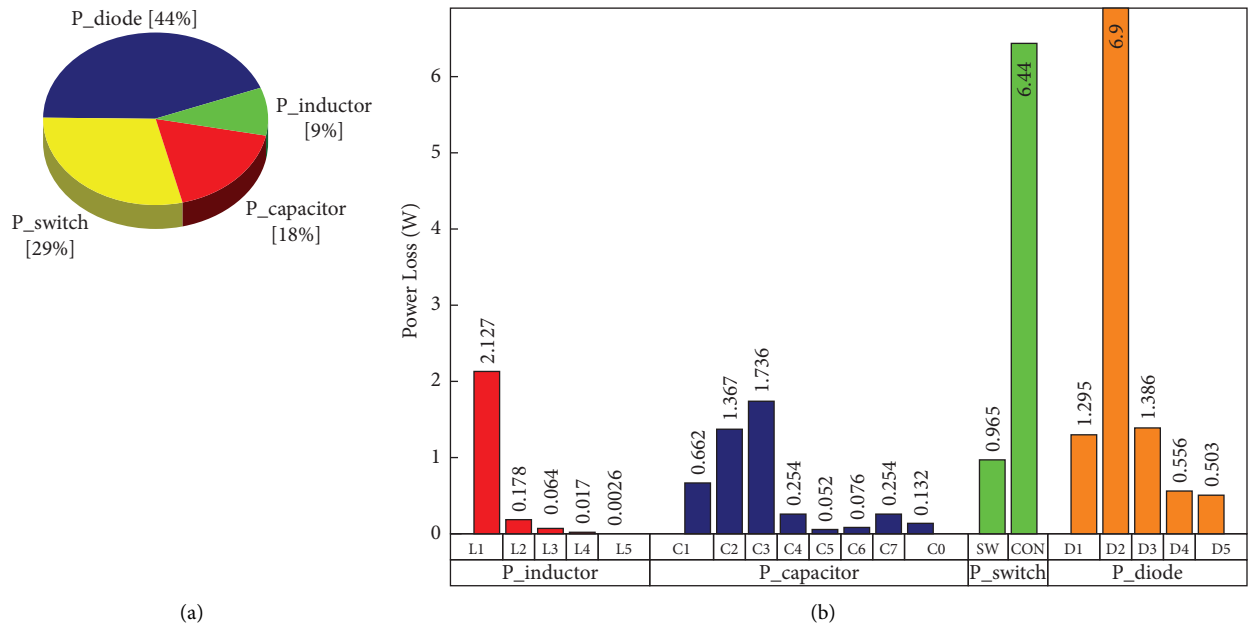

Figure 10: (a) Cumulative losses. (b) Loss breakdown analysis.

power loss of switch and diodes, respectively. The conduction loss and switching loss are considered for calculating the P_{switch}.

The power loss expression for individual components are given below:

$$\left\{\begin{array}{l} P_{\text{ind}} = \sum_{n=1}^{5} r_{Ln}.i_{Ln}^2;\ P_{\text{cap}} = \sum_{n=1}^{7} r_{Cn}.i_{Cn}^2 \\ P_{\text{diode}} = \left(\sum_{n=1,\ n\neq 2}^{6} r_{F\,Dn}.(1-D)i_{Dn}^2 + V_{F\,Dn}.(1-D)i_{Dn} \right) \\ \quad + \left(r_{F\,D2}.Di_{D2}^2 + V_{F\,D2}.Di_{D2} \right) \\ P_{\text{cond.loss}} = r_{DS}D\left(i_{S1}\right)^2 \\ P_{\text{switching.loss}} = f.C_s.\left(\dfrac{V_i}{(1-D)^2}\right)^2 \end{array}\right\}, \quad (19)$$

where r_{DS} is the ON-state resistance of the MOSFET; r_L and r_C are the equivalent series resistance of inductor and capacitor, respectively; and r_{FD} and V_{FD} are the forward resistance and threshold voltages of the diode, respectively. Figures 10(a) and 10(b) show the cumulative loss of the proposed converter components and breakdown loss of the individual components in the proposed converter, respectively. The loss analysis for individual components will help to evaluate the efficiency of the converter. This proposed converter delivers an efficiency of 90% for an input voltage of 20 V with a 60% duty cycle for a switching frequency of 50 kHz. From the loss breakdown analysis, it is confirmed that the loss of diode D_2 and conduction loss of the switch is higher than the other components.

5. Conclusion

A high gain DC-DC converter has been proposed and examined under CCM, DCM, and BCM in this article. The steady-state voltage gain has been derived along with the voltage stress and current stress of the components. The mathematical expression for designing the inductors and capacitors has been provided. The proposed topology has been tested with 200 W in the laboratory-based prototype, and the results have been obtained effectively. The proposed topology has tested with dynamic condition by changing the duty cycle and load value to check the feasibility of the topology. The efficiency and power density of the proposed converter is 90% and 1.16 kW/L, respectively. The proposed converter utilizes a single switch for achieving higher voltage gain so that it could be useful for RES applications.

Data Availability

Not applicable for this research work.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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Research Article

Automatic Distributed Control Method for Indoor Low-Voltage Electricity Based on Modal Symmetry Algorithm

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The traditional control method has a low margin of indoor voltage stability, which can easily lead to voltage collapse, and the control effect is not ideal. An automatic distributed control method for indoor low-voltage electricity system based on modal symmetry algorithm is proposed. In order to improve the voltage stability margin, the decoupling between the indoor low-voltage electricity characteristics and regions was analyzed. Based on the analysis results, the decoupling between regions and the robustness to faults of the distributed zone scheme were considered comprehensively, and the modularity and the optimal zoning scheme were screened. Based on the principle of modal symmetry, the original data of the distributed control matrix of low-voltage electricity was obtained. Mean standardization method was used to standardize the matrix, so as to realize the distributed control of indoor low-voltage electricity. The experimental results show that the proposed method improves the margin of voltage stability, overcomes the drawbacks of traditional methods, and reduces the probability of voltage accidents. It shows that this method has higher flexibility, higher reliability, and higher application value as well as improving the automatic control level of voltage.

1. Introduction

With the progress and development of science and technology, distributed control system technology has been widely used in electric automation engineering of power plants. Its own characteristics have been generally recognized. Rational application of distributed control system can improve the automation level of power plants and achieve higher flexibility and reliability of electric automation of power plants [1–3]. The integration of distributed control system into indoor environment is helpful to improve the level of voltage automation. Distributed control system is called DCS. In the process of control, a collection station is composed of several microprocessor cores [4–6]. It can organically combine computer technology, communication technology, display technology, and control technology, connects different functions and local computers, and has the advantages of good monitoring performance, high reliability, good expansibility, and easy maintenance [7–9]. With the interconnection of cross-regional power grids and constraints from economy and technology, in order to make the full use of existing system resources, power grids are often forced to operate near the critical point, and the voltage stability margin is very low, which increases the probability of power accidents such as voltage collapse [10–12]. In order to ensure voltage quality and reactive power balance, and realize the optimal coordination between voltage stability and reactive power optimization, the automatic distributed control of indoor low-voltage electricity system has become an important measure [13, 14]. At present, the relevant researchers have studied the low-voltage electricity control method and achieved some research results.

In the field of distributed control of power system, there have been relevant studies based on swarm algorithm, neural network, hybrid system theory, and other methods. Some scholars proposed a nonlinear distributed controller based on the swarm algorithm. The controller receives part of the real-time state information of the power grid through the phasor measurement unit and realizes local information

interaction with the weight matrix. The controllable external energy storage equipment with fast action characteristics is used to control the output (or absorption) active power in the generator bus, so as to realize the transient recovery of the system quickly and efficiently. In reference [15], a distributed adaptive controller based on radial basis function neural network (RBFNN) was proposed. The method based on RBFNN was used to compensate the unknown nonlinear items and external disturbances in the system, and the corresponding adaptive parameter estimation method was designed to approximate the ideal weight matrix of the unknown nonlinear items. For the control of low-voltage power, the relevant research mainly focused on the application of automatic power control system in low-voltage distribution system. The automatic power control system mainly includes digital power measurement and control device, multi-function power instrument, control equipment, bus concentrator, monitoring system and communication module. Automatic power control system can be divided into hierarchical structure and distributed structure. According to the composition of some multi-functional power instruments, serial ports were used to connect them and automatically connect them to the power control system. Bus is used to connect and unify the components. In addition, researchers have designed intelligent low-voltage power capacitors to improve the voltage quality in low-voltage AC power systems. However, the design of power automatic control system and low-voltage power capacitor is not fully constrained. In references [16, 17], a regional generator reactive power reserve method based on voltage control zoning was proposed. This method synthetically measured the reactive power reserve value of static voltage stability and quasi-steady voltage control and the availability of reactive power reserve, and analyzed the characteristics and selection methods of control variables. A quadratic programming model for optimizing regional reactive power reserve and regional voltage level was established. However, this method had a low-voltage stability margin, thereby reducing the voltage level. In reference [18], "all PV nodes in the power grid should be relaxed to PQ nodes" was proposed, and the voltage over limit nodes could be calculated by the power flow equation in the form of injected current. The linear sensitivity between the voltage over limit node and the voltages of other nodes in the power grid could be continuously adjusted until the voltage over limit of the entire network node was no longer exceeded. The number of center points of the whole network was determined as the number of partitions to be divided, and the linear sensitivity between the node voltage and the reactive current injected into the node was taken as the scale of the reactive voltage. The reactive power control space was established. However, due to the complexity of the process, the voltage stability margin decreased. In reference [19], an electromagnetic loop network division and scheme evaluation method based on the improved GN splitting algorithm was proposed. According to the importance of the shrinking nodes, the feature node integrator was selected, and then, the edge median was obtained using the GN splitting algorithm to evaluate the weakness of the straight line, so as to obtain the segmentation scheme. An information entropy evaluation model based on two-level indicators was constructed to evaluate the ring network division scheme. Although this method was effective, it did not control the indoor voltage and lack pertinence [20, 21].

In order to solve the problems of the traditional methods mentioned above, improve the voltage stability margin and fully constrain the control conditions, an automatic distributed control method for indoor low-voltage electricity system based on modal symmetry algorithm was proposed. Experiments show that this method effectively solved the problem of low-voltage stability margin that easily to lead to voltage collapse accident and improved the control effect [22, 23].

2. Automatic Distributed Control Method for Indoor Low-Voltage Electricity

2.1. Characteristics of Low-Voltage Electricity. Low-voltage electrical apparatus is an electrical apparatus that plays the role of protection, control, regulation, conversion, and on-off in the circuit with rated voltage of AC 1000 V or DC 1500 V. The power range is generally 100 W to 1000 W. The rated voltage of low-voltage appliances shall be compatible with the nominal voltage of the circuit, and the rated impulse withstand voltage shall be compatible with the overvoltage category required by the installation site. The rated frequency of low-voltage apparatus shall conform to the nominal frequency of the circuit and the rated current shall not be less than the load calculation current of the circuit. Indoor low-voltage distribution devices are mainly composed of switching appliances and control appliances. They are mainly used for power conversion, shunting, and regulation of electrical equipment. Once an accident occurs, the accident electrical appliances can be cut off in time without affecting the normal work of non-accident electrical appliances. Therefore, the automatic distributed control of indoor low-voltage electrical appliances is conducive to reducing the probability of accidents and ensuring personal safety. Distributed control of indoor low-voltage electricity system is the decoupling of regional voltage control and the improvement of voltage stability margin. According to the current research, the distributed areas should follow the following principles.

(1) Representation of the central node: the voltage characteristics of the central node in the region can reflect the voltage characteristics of all the nodes in the region.

(2) Controllability in the area: there is enough reactive power reserve in the area to control the voltage in the area.

(3) Inter-regional decoupling: the regional voltage is controlled by the reactive power source in the region and is less affected by other regions.

(4) Robustness to faults: before and after faults, the changes of electrical connections between nodes should be small; otherwise, the zoning scheme may

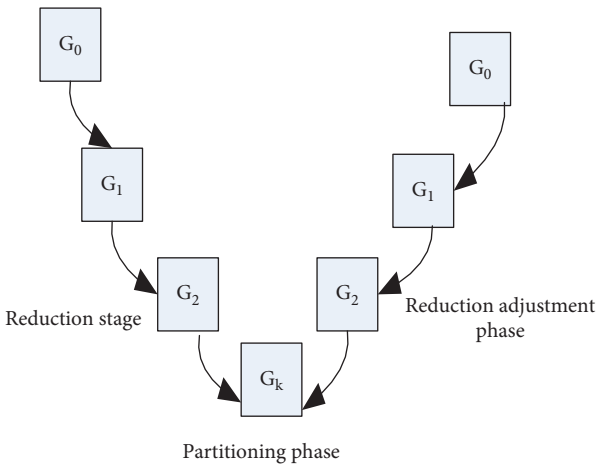

Figure 1: Transformer branch network.

lose reference value, and the control optimization measures in the region may also fail. This principle can be regarded as an extension of the concept of inter-regional decoupling.

(5) Connectivity within a region: there are no isolated nodes within the region or separated by other regions.

(6) Consistency of transformer's branch endpoint: transformer's branch node belongs to the same area.

According to the given transformer network structure and regional operation conditions, the node method was used to make power flow calculation, and the operation state of indoor low-voltage power network was obtained. Taking the symmetry matrix of indoor low-voltage power automatic distributed control as the objective function, the voltage and reactive power of nodes will be constrained. In the above principles, the central node can be determined after the scheme of distributed area was obtained. Principles (5) and (6) will be guaranteed in the algorithm, so the process should focus on meeting principles (2)–(4). The following is a detailed analysis of the controllability and decoupling between regions. Figure 1 shows the branch network of the transformer.

2.1.1. Controllability Analysis of Indoor Area: Electrical Distance of Reactive Power Node. The ability of reactive power source (such as generator and SVC) nodes to control the voltage of controlled nodes can be characterized by quasi-steady-state voltage control sensitivity.

$$\Delta U_L = \frac{\partial U_L}{\partial Q_G}\Delta Q_G = S_{LG}\Delta Q_G, \tag{1}$$

where ΔQ_G is the variation vector of reactive power output of indoor low-voltage electricity distributed control, ΔU_L is the voltage variation vector of controlled node of low-voltage electricity distributed control, G is the reactive power node set, L is the controlled node set (including reactive power node whose reactive power output has reached the upper limit), and S_{LG} is the sensitivity matrix of low-voltage

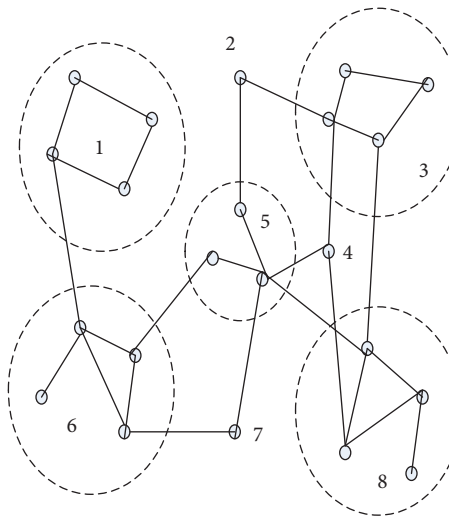

Figure 2: Topology of the power grid.

electricity distributed control. Element $(S_{LG})_{ij}$ represents the voltage variation of the controlled node i when the unit of reactive power output of reactive power source j changes. In order to meet the quasi-steady-state distributed control characteristics of low-voltage electricity system, the successive recursive method is used to solve the problem, that is, when calculating the control sensitivity of a reactive power node, the remaining reactive power nodes are still set as PV nodes [24].

S^i_{LG} is the low-voltage electricity distributed control vector of each reactive power node to the controlled node. Because of the regional characteristics of distributed control of low-voltage electricity system, in S^i_{LG}, the corresponding components of the controlled nodes near the reactive power node i are larger, while the other components are smaller. If the voltage control vectors of reactive power node i and j are similar, it shows that their reactive power reserve can be used to control the voltage level in their vicinity, and the control coupling degree is high. Therefore, the electrical distance of reactive power node can be defined as

$$D\left(S^i_{LG}, S^j_{LG}\right) = 1 - \frac{\left(S^i_{LG}\right)^T S^j_{LG}}{\left\|S^i_{LG}\right\|\left\|S^j_{LG}\right\|}. \tag{2}$$

According to formula (2), the electrical distances of partitions s and t are defined.

$$D\left(G_s, G_t\right) = \max\left(D\left(S^i_{LG}, S^j_{LG}\right)\right), \tag{3}$$

where G_s and G_t are reactive power node sets in distributed area s and t, respectively. If the electrical distances of s and t in the distributed area are similar, it shows that the control function of reactive power sources in the distributed area s and t is similar, and priority should be given to merging in the distributed process to meet the principle of controllability in the area. Figure 2 shows the network topology.

2.1.2. Interregional Decoupling Analysis: Modularity and Optimal Scheme Screening. In the process of decentralization, a series of partitioning schemes are generated, among

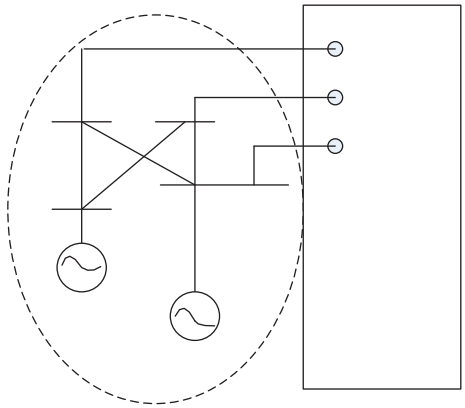

Figure 3: A simplified cluster of nodes with reactive power source nodes.

which the most reasonable one with decoupling property should be chosen as the optimal one. An index for evaluating the quality of partition is proposed. The weighted definition is as follows:

$$M\left(A,\Phi_p\right)=\frac{1}{2m}\sum_i\sum_j\left(A_{ij}-\frac{k_ik_j}{2m}\right)\delta(i,j), \tag{4}$$

where A is the edge weight matrix, element A_{ij} is the edge weight of connecting nodes i and j; Φ_p is the distributed zone scheme; if node i and j belong to the same partition, then $\delta(i,j)=1$, otherwise $\delta(i,j)=1$; $k_i=\sum_i A_{ij}$ is the sum of all edge weights connected with node i, i.e., the degree of node i; $m=1/2\sum_i\sum_j A_{ij}$ is the sum of all edge weights in the network; $k_ik_j/2m$ is the expected value of edge weights between nodes i and j in the case of random network connection to keep the degree of nodes i and j unchanged. By analyzing of formula (4), if the value of M is to be increased, it is necessary to divide the nodes at both ends of the branch whose weight is greater than the expected value (i.e., the connection is close) into the same area, and the nodes at both ends of the branch whose weight is less than the expected value (i.e., the connection is weak) into different areas. Obviously, this is a reasonable way of dividing. Therefore, M can be used to evaluate the quality of zoning. Practical experience shows that when $M>0.3$, the division quality is higher [25, 26]. Figure 3 shows a simplified cluster of nodes with reactive power sources.

In this paper, the power grid is regarded as a weighted undirected connected graph. Nodes and branches are nodes and edges of the graph, respectively. Two modularity indices are proposed to measure the inter-regional decoupling and robustness to faults of the partition scheme.

(1) Interregional Decoupling Modularity M_1. According to the principle of inter-regional decoupling, a reasonable scheme of distributed zone should make the electrical connection of the nodes at both ends of the branch within the region close, and the electrical connection of the nodes at both ends of the branch at the regional boundary weak [27, 28]. In order to reflect the different characteristics of PV node and PQ node, the definition of electrical distance is improved and M_1 is defined.

$$\begin{aligned}
\alpha_{ij}&=\begin{cases}\dfrac{\Delta U_i}{\Delta U_j}=\dfrac{\partial U_i/\partial Q_j}{\partial U_i/\partial Q_j}\,i\in L,\\[2ex] \dfrac{\Delta Q_i}{\Delta Q_j}=\dfrac{\partial Q_i/\partial Q_j}{\partial Q_i/\partial Q_j}\,i\in G,\end{cases}\\
d_{ij}&=d_{ji}=-\ln\left(\alpha_{ij}\alpha_{ji}\right),\\
(A_1)_{ij}&=\begin{cases}\dfrac{1-d_{ij}}{\max\left(d_{ij}\right)}, & y_{ij}\neq 0,\\[2ex] 0, & y_{ij}=0,\end{cases}\\
M_1\left(\Phi_p\right)&=M\left(A_1,\Phi_p\right),
\end{aligned} \tag{5}$$

where U_i and Q_i are the voltage of node i and injection reactive power, respectively; d_{ij} is the electrical connection degree of node i and j; y_{ij} is the admittance value between node i and j. If i is a controlled node, α_{ij} is defined as the voltage change of node i when node j's voltage unit changes; if i is a reactive power node, its voltage does not change; α_{ij} is defined as the variation of node i's reactive power output when node j's reactive power unit changes. The closer the electrical connection between nodes i and j is, the larger the value of α_{ij} is, the smaller the value of d_{ij} and the larger the value of $(A_1)_{ij}$. From the analysis of formula (4), it can be concluded that M_1 can measure the inter-regional decoupling of the distributed zone scheme.

(2) Fault Robustness Modularity M_2. According to the principle of robustness of the distributed zone scheme to faults, if the electrical connection of the nodes at both ends of the branch is greatly weakened due to the fault of the branch, the branch should be regarded as the regional boundary branch. Because it takes more time to calculate the change of electrical connection before and after branch failure one by one, and the divergence of power flow may occur, the sensitivity of the electrical connection of the two ends of the branch to the admittance of the branch is used to characterize the change of electrical connection at the end of the branch before and after the branch break, and the modularity M_2 is defined.

$$\begin{aligned}
\Delta d_{ij}&=\frac{\partial d_{ij}}{\partial y_{ij}}\Delta d_{ij},\\
(A_2)_{ij}&=\begin{cases}\dfrac{1-\Delta d_{ij}}{\max\left(\Delta d_{ij}\right)}, & y_{ij}\neq 0,\\[2ex] 0, & y_{ij}=0,\end{cases}\\
M_2\left(\Phi_p\right)&=M\left(A_2,\Phi_p\right).
\end{aligned} \tag{6}$$

The partial derivative in formula (6) can be calculated by numerical perturbation method. Formula (6) shows that the stronger the robustness of the branch is, the smaller the d_{ij}

value is and the larger the $(A_2)_{ij}$ value is. M_2 can be used to measure the robustness of low-voltage distributed control scheme to faults.

The scheme quality of distributed zone is characterized by M_1 and M_2. The modularity index M_Σ of distributed control is defined.

$$M_\Sigma\left(\Phi_{pi}\right) = \frac{M_1\left(\Phi_{pi}\right)}{\max\left(M_1\left(\Phi_{pi}\right)\right)} + \frac{M_2\left(\Phi_{pi}\right)}{\max\left(M_2\left(\Phi_{pi}\right)\right)}, \quad (7)$$

where Φ_{pi} is the ith partition scheme.

M_Σ takes into account the inter-area decoupling and robustness to faults of the distributed control scheme for indoor low-voltage electricity systems. The scheme corresponding to M_Σ maximum is chosen as the optimal distributed control scheme.

2.2. Automatic Distributed Control Method for Indoor Low-Voltage Electricity Based on Modal Symmetry Algorithm. Based on the optimal distributed area control scheme obtained in Section 2.1, the distributed control matrix of indoor low-voltage electricity system was obtained by using the principle of modal symmetry. Prior to this, the original data need to be prepared, that is, the process of determining the classified objects and extracting the characteristics of each object. The asymmetric modal information of the whole indoor low-voltage electrical device can be obtained by subtracting the average value of the low-voltage electricity linearity collected by two centrosymmetric sensors, thus the asymmetric modal can be extracted from the symmetric modal. Because the asymmetric modal amplitude of some partitions was high, by observing whether the asymmetric modal amplitude of the eigenvector of distributed control for indoor low-voltage electricity had a sudden change, the automatic partition of indoor low-voltage electricity can be accurately processed, which provides conditions for the final distributed control [29].

The universe $U = \{x_1, x_2, \ldots, x_n\}$ is the classified object, where each object is represented by m data that can represent the characteristics of the object, i.e.,

$$x_i = \{x_{i1}, x_{i2}, \ldots, x_{im}\}, \ (i = 1, 2, \ldots n). \quad (8)$$

This forms a raw data matrix R of $m \times n$.

The similarity matrix obtained from the previous step is only reflexive and transitive, and does not have symmetry. It needs to be transformed into equivalent matrix by calculating symmetry coefficient. The concrete method is to start from R and find the square in turn: $R \longrightarrow R^2 \longrightarrow R^4 \longrightarrow \cdots$. When $R^k \cdot R^k = R^k$ appeared for the first time, it shows that R^k has symmetry, and R^k is the symmetry coefficient $t(R)$. Different cut-off values λ were taken and R^k was intercepted to get the required classification. For any $\lambda \in [0, 1]$, $[t(R)]_\lambda = (r_{ij}^\lambda)$ is the λ truncated matrix of $t(R)$, where

$$r_{ij}^\lambda = \begin{cases} 1, & r_{ij} > \lambda, \\ 0, & r_{ij} > \lambda, \end{cases} \quad (9)$$

when $r_{ij}^\lambda = 1$, node i and node j were grouped together. With the change of λ from big to small, classification from fine to coarse is a dynamic process.

The eigenvectors of distributed control for indoor low-voltage electricity describing PQ nodes were determined. Considering the actual process of reactive power and voltage control, the control capability of each generator to the load bus was taken as the eigenvectors of low-voltage electricity distributed control, i.e., $x_i = \{x_{i1}, x_{i1}, \ldots, x_{i\times(k+1)}\}$. The element x_{ij} in x_i represents the sensitivity of generator j to load node i. The specific solutions are as follows:

The iterative equation of reactive power flow based on P-Q decomposition method is

$$-L\Delta V = \Delta Q. \quad (10)$$

The ΔV and ΔQ in this equation correspond to the load bus (PQ node). If the generator bus (PV node) is added to the above modified equation, and the load bus and generator bus are represented by the subscripts D and G, respectively, there are

$$-\begin{bmatrix} L_{DD} & L_{DG} \\ L_{GD} & L_{GG} \end{bmatrix}\begin{bmatrix} \Delta V_D \\ \Delta V_G \end{bmatrix} = \begin{bmatrix} \Delta Q_D \\ \Delta Q_G \end{bmatrix}, \quad (11)$$

where L_{DD} is admittance matrix B'' which does not include the corresponding rows and columns of balanced nodes and PV nodes. L_{DG} and L_{GD} are mutual admittance between generators and load buses, and L_{GG} is self-admittance of generators. The relationship between ΔV and ΔQ is derived from formula (9):

$$\begin{bmatrix} \Delta V_D \\ \Delta V_G \end{bmatrix} = -\begin{bmatrix} L_{DD} & L_{DG} \\ L_{GD} & L_{GG} \end{bmatrix}^{-1}\begin{bmatrix} \Delta Q_D \\ \Delta Q_G \end{bmatrix}. \quad (12)$$

Let

$$\begin{bmatrix} X_{DD} & X_{DG} \\ X_{GD} & X_{GG} \end{bmatrix} = -\begin{bmatrix} L_{DD} & L_{DG} \\ L_{GD} & L_{GG} \end{bmatrix}^{-1}. \quad (13)$$

When the generators' reactive power output changes under the distributed control of indoor low-voltage electricity, assuming that the reactive power of load buses remains unchanged, i.e., $\Delta Q_D = 0$, there are

$$\Delta V_D = X_{DG}\Delta Q_G. \quad (14)$$

X_{DG} is the sensitivity matrix between ΔV_D and ΔQ_G. It has the dimension of impedance. It is a partial sub-matrix related to generator node and load node in the inverse of the augmented B'' matrix. In the previous calculation, X_{DG} is calculated in one time, without considering the quasi-steady-state physical response process of PV nodes. By using the proposed method of constructing reactive power control space, the generator was solved step by step. In the $(m + k + 1)$ node system, it is assumed that all $(k + 1)$ generator nodes were equipped with AVR, which constitutes a set G; m load buses to be partitioned constitute a set D. When calculating the sensitivity of a generator A to other nodes, A was set as PQ node, and the other generator nodes were set as PV nodes. When calculating the sensitivity, the diagonal

elements corresponding to the PV node in the full-dimensional admittance matrix B including the PV node and the balanced node were increased to ensure that the terminal voltage of the node remains unchanged. After constructing such a full-dimensional admittance matrix, the sensitivity of the generator A to the load nodes in the system was solved by calculating X_{DG} according to formula (13). The sensitivity of other generator nodes to load nodes was calculated by this method in turn. In this way, the original data of distributed control matrix $X_{[(m\times(k+1))]}$ for low-voltage electricity was obtained.

It is noteworthy that, reactive power should include generators, switchable capacitors, and SVC which can provide voltage/reactive power support to the system as required in the distributed control of indoor low-voltage electricity. It can be easily extended to other reactive power sources, only by increasing the corresponding dimension in the reactive power space.

In order to unify the characteristic indexes of different dimensions and quantities, the mean standardization method was used to standardize $X_{[(m\times(k+1))]}$, that is,

$$y_{ij} = \frac{x_{ij}}{\overline{x}_j}, \tag{15}$$

where y_{ij} is the standardized data, and $\overline{x}_j$ is the average of column data. After this treatment, the elements in Y are unified within a common range of data characteristics. If it is calculated directly, it may highlight the role of those characteristic indicators with a very large order of magnitude in classification, reduce or even exclude the role of some smaller characteristic indicators in classification, resulting in inaccurate classification results.

When using modal symmetry algorithm for automatic distributed control of indoor low-voltage electricity, a symmetric matrix was established, and the symmetric matrix R was calculated. The elements in matrix R are as follows:

$$r_{ij} = \exp\left(-c\sum_{k=1}^{m}\left|y_{ik} - y_{jk}\right|\right), \tag{16}$$

where r_{ij} is the similarity or proximity between load node i and load node j, the exp operation on r_{ij} is to calculate $e^{-c\sum_{k=1}^{m}|y_{ik}-y_{jk}|}$, and its range is $0 \le r_{ij} \le 1$; c is a specific positive number, and the value makes r_{ij} distribute in [0,1], $c = 1$.

The transfer closure matrix of load nodes was calculated by matrix programming which describes the degree of symmetry between load nodes. Under the threshold $\lambda \in [0, 1]$, different λ can be selected to obtain different λ horizontal truncation matrices, each representing a clustering. When λ changes from 1 to 0, the number of classifications changes from n to 1, which is a dynamic process.

When the number of partitions is unknown, the number of classes c was gradually increased from a smaller value. In this process, the modal symmetry algorithm was used for each selected c. The algorithm block diagram is shown in Figure 4. Obviously, the objective function J decreases monotonously with the increase of c. In the process of increasing c, there will always be some denser points separated. J will decrease, but the speed of reduction will slow down. Thus, the number of partitions can be roughly determined.

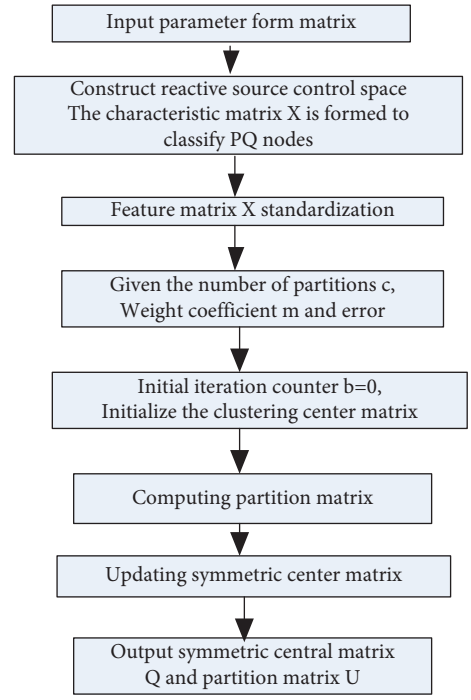

Figure 4: Flow chart of distributed control method for indoor low-voltage electrics.

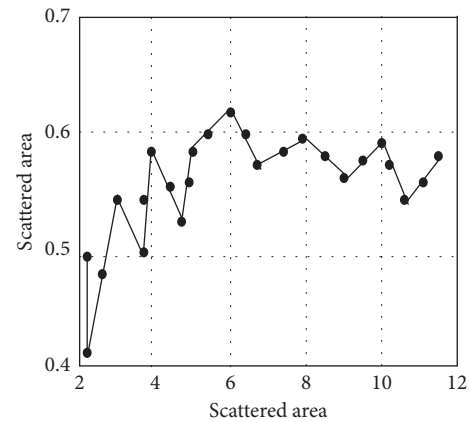

Figure 5: Partition modularity of IEEE 39-node system.

Table 1: Partition results of IEEE39 node system.

Number of distributed area	Node number
1	4, 10, 11, 12, 14, 15, 28
2	1, 2, 4, 16, 24, 26, 30, 35
3	19, 21, 32, 34
4	28, 29, 30
5	16, 22, 24, 26, 36, 37
6	5, 7, 8, 10, 30, 38

Table 2: Comparison of different clustering methods.

Number of tests	Method in reference [17]		Method in reference [18]		Method in reference [19]		The proposed method	
	Modularity	Partition time/s	Modularity	Partition time/s	Modularity	Partition time/s	Modularity	Partition time/s
1	0.4930	1.917	0.5219	1.903	0.5614	1.875	0.6048	1.786
2	0.5568	2.540	0.5677	2.357	0.6076	1.981	0.6408	1.643
3	0.6043	1.835	0.5983	1.833	0.6121	1.764	0.6408	1.738
4	0.6048	2.640	0.6105	2.065	0.6398	1.947	0.6408	1.840
5	0.5743	1.780	0.6059	1.764	0.6316	1.793	0.6408	1.720

Table 3: Verification results of reactive power reserve.

Method of partition	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6
Before partition	33.27	−41.66	24.69	18.16	25.86	74.76
After partition	61.57	80.32	24.69	18.16	25.86	74.76

Table 4: Comparison of modularity of different methods.

Number	Method	Number of distributed zones	Module degree/Q
1	Method in reference [17]	5	0.5643
2	Method in reference [18]	6	0.5701
3	Method in reference [19]	5	0.5755
4	The proposed method	6	0.5991

After selecting the number of partitions and completing the symmetry process of PQ nodes, PV nodes need to be merged. For a PV node connected with only one PQ node, it was merged in the region where the directly connected PQ node was located. Accordingly, the research on automatic distributed control of indoor low-voltage electricity system was completed.

3. Experimental Results and Analysis

The proposed automatic distributed control method for indoor low-voltage electricity system based on modal symmetry algorithm was applied to the standard test system of IEEE-39 nodes and compared with other distributed control methods. The 39-node system consists of 10 generators, 34 lines, and 12 transformers. According to the distributed control method for indoor low-voltage electricity system described above, the maximum number of partitions is 11, that is, the maximum number of iterations of the algorithm is 10. The relationship between modularity M_Σ and number of partitions is shown in Figure 5.

According to the different partition modularity of Figure 5, when the partition number of IEEE39 nodes is 6, the modularity is the highest, and the modularity M_Σ is 0.6049. The results of the preferred partition are shown in Table 1.

Table 2 shows the comparison of modularity and partitioning time of the method in references [17–19] in 6 partition zones. The running environment was Windows 8, and the CPU is i7 quad-core 2.3 GHz. The analysis Table 2 shows that the proposed method has higher stability and shorter partition time than the method in references [17–19]. It can effectively improve the stability margin of the automatic distributed control of indoor low-voltage electricity system.

After checking the optimal zones, it was found that the reactive power reserve index of Zone 2 was 41.67%, which did not meet the requirement of 15% reactive power reserve, and Zone 2 needed to be re-divided. According to the calculation, the feasible dividing nodes in Zone 2 were node 4 (reactive load is 184 Mvar, and the feasible dividing area was Zone 1 and Zone 6) and node 15 (reactive load was 153 Mvar, and the feasible dividing area was Zone 1 and Zone 5). According to the order of reactive load from large to small, the node 4 with larger reactive power was first divided into Zone 1 or Zone 6. If node 4 was divided into Zone 6, the reactive power reserve of Zone 6 will be less than 15%, and Zone 1 of node 4 can ensure the reactive power reserve of all regions. Therefore, node 4 should be divided into partition 1, which effectively improves the margin of low-voltage stability.

The modularity of the six partitions was 0.5992, which was only 0.0057 lower than that of the original partition. Therefore, the new partition had less influence on the inter-regional reactive power coupling and could be used as the final partition scheme. The results of checking and re-partitioning are shown in Table 3.

The proposed method was compared with the methods in references [17], [18], and [19] in terms of partition modularity of the 39-node system. The comparison results are shown in Table 4. It is worth noting that the proposed method is different from other methods, so the modularity values are different, but the results of the same modularity algorithm will not affect the comparison of different partitioning methods.

Table 4 shows that the proposed method has the highest modularity and can effectively improve the margin of voltage stability. The modularity refers to previous M_Σ. At the same time, the proposed method has

some advantages in time complexity and can be used in rapid voltage control zoning after fault or accident in engineering practice.

4. Conclusions

With the development of power network and the emergence of large-scale combined power grid, the problem of voltage stability has become increasingly prominent. Various measures to prevent voltage instability have been proposed, and the voltage hierarchical control system has emerged as the times require. In order to improve the phenomenon of voltage instability and the margin of voltage stability, an automatic distributed control method for indoor low-voltage electricity system based on modal symmetry algorithm is proposed. On the basis of considering the low-voltage electrical characteristics, the principles to be followed in the distribution area were proposed, and the indoor area controllability analysis and inter-area decoupling analysis were made to obtain the optimal distributed area control scheme. The distributed control matrix of indoor low-voltage power system was obtained by using the principle of modal symmetry, and the distributed control of indoor low-voltage power system was completed. The applicability and effectiveness of the designed method were verified through comparative experiments. The experimental results show that the proposed method had the highest module stability and the shortest partition time. It shows that the method in this paper can effectively improve the stability margin of indoor low-voltage power distributed control, which has more advantages than the control method, and can provide valuable reference for low-voltage power system control.

Although this paper has done some useful research and exploration in the field of automatic distributed control of low-voltage electricity system, there are still some problems to be further studied and perfected. When dividing the area, the following criteria are met: strong coupling in the area, weak coupling between the areas; moderate number of voltage control areas; moderate size of each voltage control area; reactive power balance in the area, and a certain amount of reactive power margin left. However, there is a lack of a quantitative criterion to judge the quality of the partition, so the method needs further study.

Data Availability

The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

Conflicts of Interest

It is declared by the authors that this article is free of conflicts of interest.

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Research Article

Stability Analysis of the Dual Half-Bridge Series Resonant Inverter-Fed Induction Cooking Load Based on Floquet Theory

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Induction heating (IH) applications aided power electronic control and becomes most attractive in recent years. Power control plays a vital role in any IH applications in which the stability of the converter is still a research hot spot due to variable frequency operation. In the proposed work, the stability of the converter is carried out based on the Floquet theory for dual-frequency half-bridge series inverter-fed multiload IH system. The dynamic behaviour of the converter is analyzed by developing a small-signal model of the converter. The system with a dynamic closed-loop controller results in poles and zeros lying outside the unit circle, which has poor closed-loop stability and up-down glitches in the frequency response plot. Hence, a proportional-integral (PI) compensator is used to mitigate the said issue, which results in a better response when compared with the open system and works satisfactorily. However, the system becomes unstable when the frequency is varied and the system also possesses a poor time domain response. Hence, the values of the controller gain are optimized with the Floquet theory, which is based on the Eigenvalues of the time domain model. For the optimized gains, the system possesses better stability for the variations in the switching frequency (20 kHz to 24 kHz), and also, the frequency response of the system is better with minimum time domain specifications. The performance of the system is simulated in MATLAB, and the response is noted for various switching frequencies in open loop, with a PI compensator, and with an optimized PI compensator. The output power is varied from 500 W to 18 W at load 1 and 250 W to 9 W at load 2. It is noted from the output response that the rise time is 0.0085 s, the peak time is 0.0001 s, and the peak overshoot is 0.1% with minimum steady-state error. Furthermore, the IH system is validated using a PIC16F877A microcontroller with the optimized PI controller, and the thermal image is recorded using a FLIR thermal imager.

1. Introduction

In recent years, induction heating (IH) has been widely used in several fields, which include medical, industrial, and domestic applications. It is a booming technology due to its meritorious advantages such as hygiene, indirect heat, noncontamination, zero pollution, and higher efficiency [1]. In the IH system, heat is produced on the workpiece due to the electromagnetic principle as it produces more eddy current on the surface of the material [2]. Hence, the rate of heat produced in the heating material depends on the switching frequency selection, which varies from 10 kHz to 1 MHz [3]. This high-frequency switching is achieved using the resonant inverter, which converts 50 Hz AC to high-frequency alternating current (HFAC) with a high power density and soft switching [4]. The selection of a specific converter for the application plays a vital role, in which a series half-bridge (HB) inverter is selected for the maximum power rating of up to 4.5 kW [5, 6]. The drawback of this topology is more switching stress across the switch [7]. In

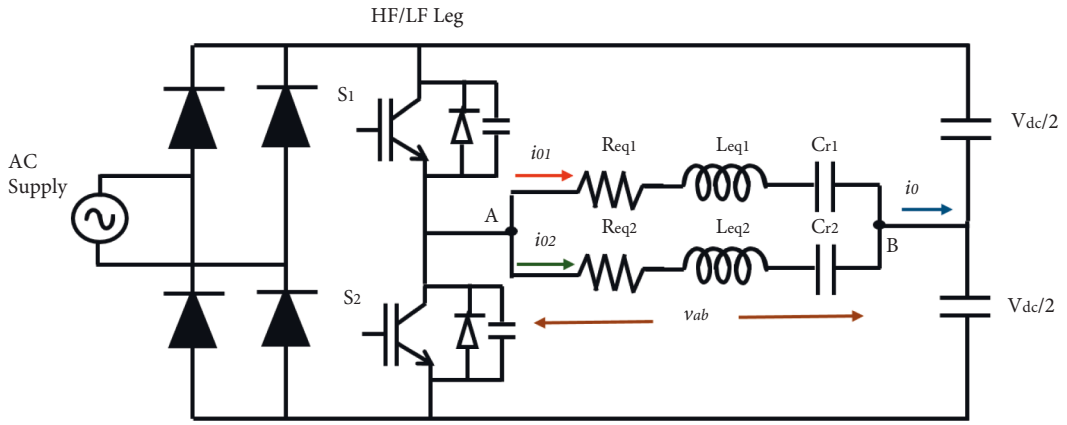


Figure 1: Circuit diagram of dual HB inverter.

[5], the switching stress is reduced using the auxiliary switched capacitor. However, the additional capacitor increases the passive elements and system time constants. This problem is overcome by using a full-bride (FB) inverter in which switching stress is shared by the four semiconductor switches. In addition, they can able to hold more power ratings, which are greater than 5000 W. In [8], a multifrequency FB series resonant inverter is developed into two loads. In the arrangement, the load frequency is selected twice the inverter frequency.

In recent years, a multioutput-based induction cooking scheme has been developed to feed power to many loads [9–13]. The converter topologies developed for feeding power include the modified HB and FB inverters. The novel topology is developed in [9], which includes HB and FB inverters, which are capable of performing the function of two FB inverters. The topology is connected to a single input and two loads with a common leg shared by both. The control algorithm is developed in such a manner that both the load can be controlled independently and simultaneously. In [10], a single-input multiple-load handling converter topology is developed. Power to the multiple loads is fed by the common HB inverter, and each load is controlled simultaneously by the inverter switches. The arrangement of the load is performed in such a manner that all are connected in parallel and independent power control is not feasible. A multioutput HB inverter feeding power to multiple loads is proposed in [11]. On this IH system, the HB inverter acts as the common inverter which converts DC into HFAC. Each load is connected with a series-connected single switch. Simultaneous power control is feasible with the switch.

Sharath Kumar et al. proposed a dual-frequency FB SRI to handle two loads. The output power is deployed using asymmetrical duty cycle (ADC) control in which simultaneous and independent power control is feasible. The proposed inverter consists of two legs, in which one leg takes care of the low frequency and the other one the high-frequency [12]. This control scheme results in the presence of DC components in the output voltage. This problem was overcome by Vishnuram and Ramachandiran [13]. HB inverter was used to feed power to two loads with two different frequencies. The output power is varied using pulse density modulation (PDM) control, in which simultaneous and independent control is feasible. A dual-frequency control is performed for the surface hardening of gear, which is a nonuniform shape [14].

Booma et al. developed the small-signal modelling of the HB inverter-fed IH system using the harmonics balance equation [15]. In this method, nonlinear variables in the state equations are expanded by the Taylor series and the transfer function for output voltage concerning duty cycle and frequency was obtained. The derived function was divided into the sum of cosine and sine terms with fixed frequency and variable duty cycle and with variable duty cycle and fixed frequency. The open-loop stability of the converter was analyzed for variations in duty cycle and frequency. Various researchers proposed the mathematical modelling of rotating and polar coordinate systems based on the traditional state plane method [16, 17]. However, these studies have not investigated the stability issues of the system with the resonant converters. In a small-signal model of a dual HB inverter with a common capacitor for multi-load cooking applications was proposed [18]. An open-loop Bode plot was obtained by providing the small perturbations in the switching frequencies and phase angle between voltage and current. The stability and controllability of a PLL-based IH system were proposed in [19]. The output power was controlled using the AVC control technique, and the power control margin was obtained using pole-zero plots. This method was time-consuming and does not depend on the qualitative analysis of the converter, which is very important for the stability analysis of the system. In addition, stability analysis was carried out in the frequency domain for a dual HB inverter-fed IH system, and a compensator was designed as per the obtained amplitude-phase and gain margin. The system was found to be stable in an open loop and failed in a closed loop. Therefore, it is necessary to obtain the closed-loop stability of the system under uncertain conditions. The stability of the periodic system is estimated by using the Floquet theory with the zero solution method [20]. This method uses the periodic solution of linear and nonlinear differential equations with

the different periodic solutions at the origin. The same has been used in PWM-controlled rectifiers, DC-DC converters, and inverters [21–23].

It is evident from the literature that, there is a quest in proposing the control algorithm to determine the closed stability of the system. In this paper, a methodology is presented using the Floquet theory to estimate the closed system stability for a wide range of load regulations. The small-signal modelling of the dual-frequency converter is obtained, and the stability analysis is determined by the Eigenvalue of the A matrix. The proposed system is validated and stability results are verified by simulation using Bode and polar plots, which provides an efficient scheme of dual-frequency inverter-fed IH system.

2. State-Space Modelling of Dual-Frequency Inverter

The circuit diagram of the dual HB inverter is illustrated in Figure 1. For the fixed frequency, the total resistance referred to the primary (coil) is represented as R_{eq1} and R_{eq2} and the total inductance referred to the primary (coil) is represented as L_{eq1} and L_{eq2}. The resonant capacitors are associated in series with equivalent resistance and inductance of each coil to form a series resonant tank. Modes of operation and switching frequency selection are briefed in [13]. A mathematical model of the system is essential to investigate system stability. Hence, v_{c1}, v_{c2}, i_{o1}, and i_{o2} are considered AC state variables. By approximating the state equations using the harmonic balance principle, state variables are resolved in terms of sine and cosine functions as i_{co1}, i_{so1}, v_{ccr1}, v_{scr1}, i_{co2}, i_{so2}, v_{ccr2}, v_{scr2}. The small-signal modeling of the dual-frequency HB inverter-fed induction cooking system is given as follows:

$$\frac{d\hat{i}_{s01}}{dt} = -\frac{\hat{v}_{scr1}}{L_{eq1}} - \frac{R_{eq1}}{L_{eq1}}\hat{i}_{s01} + \omega_{s1}\hat{i}_{c01} + I_{c01}\hat{\omega}_{s1} + \frac{2V_{in}}{L_{eq1}}\cos(2\pi\ D)\hat{d}, \tag{1}$$

$$\frac{d\hat{i}_{c01}}{dt} = -\frac{\hat{v}_{ccr1}}{L_{eq1}} - \frac{R_{eq1}}{L_{eq1}}\hat{i}_{c01} - \omega_{s1}\hat{i}_{s01} - I_{s01}\hat{\omega}_{s1} + \frac{2V_{in}}{L_{eq1}}\sin(2\pi\ D)\hat{d}, \tag{2}$$

$$\frac{d\hat{v}_{scr1}}{dt} = \frac{\hat{i}_{s01}}{C_{r1}} + \omega_{s1}\hat{v}_{ccr1} + V_{ccr1}\hat{\omega}_{s1}, \tag{3}$$

$$\frac{d\hat{v}_{ccr1}}{dt} = \frac{\hat{i}_{c01}}{C_{r1}} - \omega_{s1}\hat{v}_{scr1} - V_{scr1}\hat{\omega}_{s1}, \tag{4}$$

$$\frac{d\hat{i}_{s02}}{dt} = -\frac{\hat{v}_{scr2}}{L_{eq2}} - \frac{R_{eq2}}{L_{eq2}}\hat{i}_{s02} + \omega_{s2}\hat{i}_{c02} + I_{c02}\hat{\omega}_{s2} + \frac{2V_{in}}{L_{eq2}}\cos(2\pi\ D)\hat{d}, \tag{5}$$

$$\frac{d\hat{i}_{c02}}{dt} = -\frac{\hat{v}_{ccr2}}{L_{eq2}} - \frac{R_{eq2}}{L_{eq2}}\hat{i}_{c02} - \omega_{s2}\hat{i}_{s02} - I_{s02}\hat{\omega}_{s2} + \frac{2V_{in}}{L_{eq2}}\sin(2\pi\ D)\hat{d}, \tag{6}$$

$$\frac{d\hat{v}_{scr2}}{dt} = \frac{\hat{i}_{s02}}{C_{r2}} + \omega_{s2}\hat{v}_{ccr2} + V_{ccr2}\hat{\omega}_{s2}, \tag{7}$$

$$\frac{d\hat{v}_{ccr2}}{dt} = \frac{\hat{i}_{c02}}{C_{r2}} - \omega_{s2}\hat{v}_{scr2} - V_{scr2}\hat{\omega}_{s2}. \tag{8}$$

The state and output equation of the converter is

$$\dot{x} = Ax + B_1u_1 + B_2u_2, \tag{9}$$

$$y = Cx. \tag{10}$$

State variable matrix (x), inputs (u_1 and u_2), and output variable (y) are represented as

$$\begin{aligned} x &= \left[\hat{i}_{s01}\ \ \hat{i}_{c01}\ \ \hat{v}_{scr1}\ \ \hat{v}_{ccr1}\ \ \hat{i}_{s02}\ \ \hat{i}_{c02}\ \ \hat{v}_{scr2}\ \ \hat{v}_{ccr2}\right]^T, \\ u_1 &= \hat{d}, \\ u_2 &= \hat{\omega}_s, \\ y &= \hat{v}_0. \end{aligned} \tag{11}$$

The state matrix A is represented as

$$A = \begin{bmatrix} \frac{-R_{\text{eq1}}}{L_{\text{eq1}}} & \omega_{s1} & \frac{-1}{L_{\text{eq1}}} & 0 & 0 & 0 & 0 & 0 \\ -\omega_{s1} & \frac{-R_{\text{eq1}}}{L_{\text{eq1}}} & 0 & \frac{-1}{L_{\text{eq1}}} & 0 & 0 & 0 & 0 \\ \frac{1}{C_{r1}} & 0 & 0 & \omega_{s1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_{r1}} & -\omega_{s1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-R_{\text{eq2}}}{L_{\text{eq2}}} & \omega_{s2} & \frac{-1}{L_{\text{eq2}}} & 0 \\ 0 & 0 & 0 & 0 & -\omega_{s1} & \frac{-R_{eq2}}{L_{eq2}} & 0 & \frac{-1}{L_{\text{eq2}}} \\ 0 & 0 & 0 & 0 & \frac{1}{C_{r2}} & 0 & 0 & \omega_{s2} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{r2}} & -\omega_{s2} & 0 \end{bmatrix}. \tag{12}$$

Input matrixes B_1 and B_2 are represented as

Table 1: Design specifications of dual half-bridge inverter.

Parameters	Values
V_{in}	50 V (DC)
P_{01}	500–1000 W
$R_{eq1} = R_{eq2}$	11 Ω
C_{r1}	620 nF
f_{r1}	18.5 kHz
f_{r2}	75 kHz
k_p	0.001
T_s	0.67 μs
D	50%
P_{02}	200–500 W
$L_{eq1} = L_{eq2}$	0.12 mH
C_{r2}	38 nF
f_{s1}	20 kHz
f_{s2}	80 kHz
k_i	7.526

$$B_1 = \begin{bmatrix} \frac{2V_{in}}{L_{eq1}}\cos(2\pi D) \\ \frac{2V_{in}}{L_{eq1}}\sin(2\pi D) \\ 0 \\ 0 \\ \frac{2V_{in}}{L_{eq2}}\cos(2\pi D) \\ \frac{2V_{in}}{L_{eq2}}\sin(2\pi D) \\ 0 \\ 0 \end{bmatrix}, \quad (13)$$

$$B_2 = \begin{bmatrix} I_{c01} \\ -I_{s01} \\ V_{ccr1} \\ -V_{scr1} \\ I_{c02} \\ -I_{s02} \\ V_{ccr2} \\ -V_{scr2} \end{bmatrix}.$$

Output matrix is represented as

$$C = \begin{bmatrix} R_{eq1} & R_{eq1} & 0 & 0 & R_{eq2} & R_{eq2} & 0 & 0 \end{bmatrix}, \quad (14)$$

where

$$I_{s01} = \frac{V_{in}\omega_{s1}^2 C_{r1}{}^2 R_{eq1}}{\lambda_1},$$

$$I_{c01} = \frac{V_{in}\omega_{s1}C_{r1}\left(1-\omega_{s1}^2 L_{eq1}C_{r1}\right)}{\lambda_1},$$

$$V_{ccr1} = \frac{V_{in}\left(1-\omega_{s1}^2 L_{eq1}C_{r1}\right)}{\lambda_1},$$

$$V_{scr1} = \frac{V_{in}\omega_{s1}C_{r1}R_{eq1}}{\lambda_1},$$

$$\lambda_1 = \omega_{s1}^4 C_{r1}{}^2 L_{eq1}{}^2 - 2\omega_{s1}^2 C_{r1}L_{eq1} + 1 + \omega_{s1}^2 C_{r1}{}^2 R_{eq1}^2, \quad (15)$$

$$I_{s02} = \frac{V_{in}\omega_{s2}^2 C_{r2}{}^2 R_{eq2}}{\lambda_2},$$

$$I_{c02} = \frac{V_{in}\omega_{s2}C_{r2}\left(1-\omega_{s2}^2 L_{eq2}C_{r2}\right)}{\lambda_2},$$

$$V_{ccr2} = \frac{V_{in}\left(1-\omega_{s2}^2 L_{eq2}C_{r2}\right)}{\lambda_2},$$

$$V_{scr2} = \frac{V_{in}\omega_{s2}C_{r2}R_{eq2}}{\lambda_2}$$

$$\lambda_2 = \omega_{s2}^4 C_{r2}{}^2 L_{eq2}^2 - 2\omega_{s2}^2 C_{r2}L_{eq2} + 1 + \omega_{s2}^2 C_{r2}{}^2 R_{eq2}^2.$$

The perturbed output voltage of load 1 and 2 is

$$\begin{aligned} \hat{p}_{01} &= R_{eq1}\hat{i}_{s01}^2 + R_{eq1}\hat{i}_{c01}^2, \\ \hat{p}_{02} &= R_{eq2}\hat{i}_{s02}^2 + R_{eq2}\hat{i}_{c02}^2. \end{aligned} \quad (16)$$

The transfer function of output to duty cycle (G_{pd}) and output to switching frequency (G_{pf}) in the discrete domain with sampling time (T_s) is

$$\begin{aligned} G_{p\,d}(z) &= \frac{\hat{p}_0}{d} \\ &= C(zI - A)^{-1}\mathbf{B}_1 T_s, \end{aligned} \quad (17)$$

$$\begin{aligned} G_{pf}(z) &= \frac{2\pi\hat{p}_0}{\hat{\omega}_s} \\ &= 2\pi C(zI - A)^{-1}\mathbf{B}_2 T_s. \end{aligned} \quad (18)$$

This work focuses on the stability of the system for varying switching frequencies with a fixed duty cycle.

Table 2: Parameters of the converter and transfer function for each case.

Case	Frequency (kHz)	Z domain transfer function	Remarks
1	20	$\frac{0.21395(z-3.36)(z-0.5789)(z-0.08662)}{(z^2-0.2453z+0.08966)(z^2+0.6937z+0.9399)} / \frac{(z-0.7289)(z-0.5685)(z-0.1437)(z-0.1896)}{(z^2-0.23z+0.0825)(z^2+0.6503z+0.4875)}$	Poles inside the unit circle, zeros lie outside the unit circle, up-down and down-up glitches, multiple zero crossings
2	21	$\frac{-1.0639(z-2.4)(z-0.7276)(z+0.2778)(z+0.1674)}{(z-0.04194)(z^2+0.9781z+0.3445)} / \frac{(z-1.178)(z-0.7253)(z-0.1126)(z-0.0119)}{(z^2-0.5716z+0.08249)(z^2+1.044z+0.4799)}$	Poles and zeros lie outside the unit circle, up-down glitches, multiple zero crossing
3	22	$\frac{0.10256(z+20.32)(z+06576)(z+0.4438)}{(z^2-0.09238z+0.06223)(z^2+0.1188z+0.08069)} / \frac{(z-1.705)(z-0.008356)(z^2+1.297z+0.473)}{(z^2-0.1088z+0.08171)(z^2+0.1216z+0.08247)}$	Poles and zeros lie inside the unit circle, up-down glitches, multiple zero crossings
4	23	$\frac{0.10899(z+13.81)(z+06583)(z+0.4486)}{(z^2-0.4878z+0.06637)(z^2+0.4962z+0.08218)} / \frac{(z-2.296)(z-0.006288)(z^2-1.365z+0.4668)}{(z^2+0.5386z+0.08172)(z^2+0.4966z+0.08245)}$	Poles outside and zeros inside, up-down glitches, single zero crossing
5	24	$\frac{0.020908(z+46.86)(z^2+0.4962z+0.08218)}{(z^2-0.3221zz+0.07516)(z^2+0.9989z+0.3216)} / \frac{(z-2.296)(z-0.004993)(z^2-0.4273z+0.08243)}{(z^2+0.3217z+0.08174)(z^2+01.22z+0.461)}$	Poles outside and zeros inside, unit circle, up-down glitches

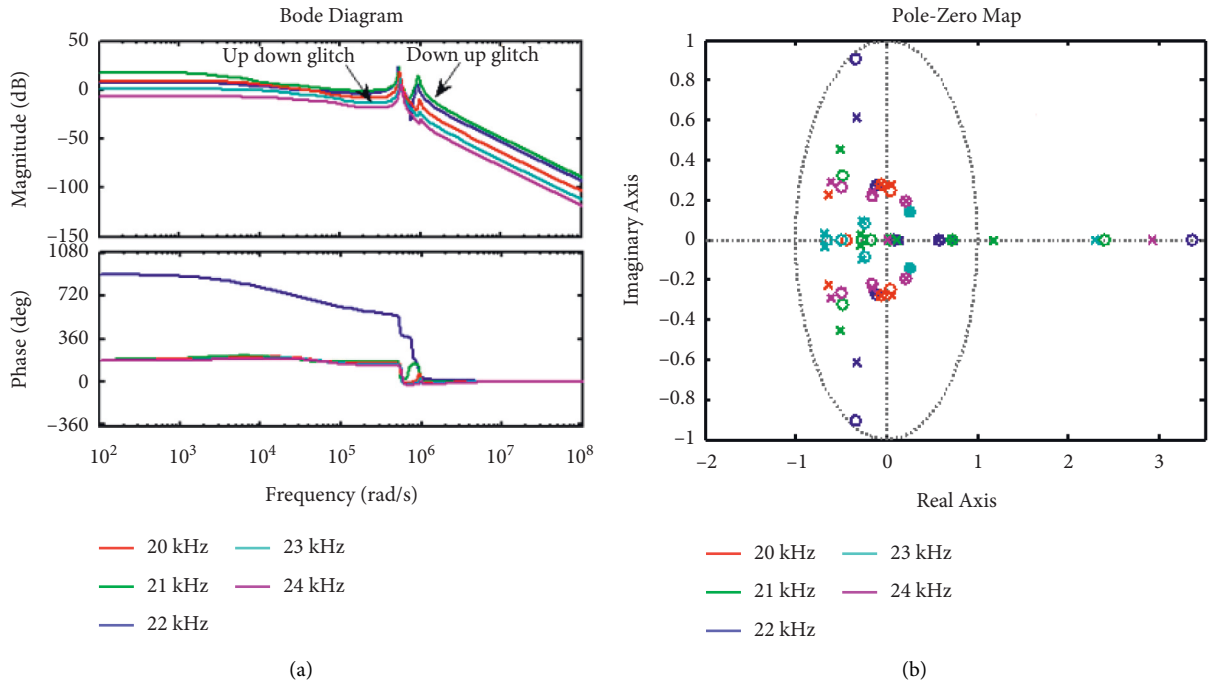


FIGURE 2: Frequency response of converter for different frequencies. (a) Bode diagram, (b) pole-zero map.

3. Analysis of the Dual-Frequency Half-Bridge Inverter-Fed IH Topology

In IH applications, frequency control plays an important role in varying the output power. When the frequency is deployed for real-time applications, the stability of the system needs to be investigated. In this section, frequency domain analysis of the developed IH system is described. Also, the stability of the system is investigated using the PI compensator and Floquet stability criterion.

3.1. Frequency Response of Dual-Frequency HB SRI-Fed IH System. The design of the dual HB SRI-fed IH system is validated using the frequency domain approach. The parameters for evaluating the proposed converter are listed in Table 1. The stability analysis of the IH converter topology is conceded out using pole and zero for the variation in switching frequency. In this work, the frequency of load 2 (f_2) is chosen as four times greater than load 1 (f_1). The capacitor is selected appropriately to make each load respond to its designed frequency (20 kHz for load 1 and 80 kHz for load 2) and it acts as a high impedance for other loads [13]. The stability of the system is investigated for the switching frequencies ranging from 20 kHz to 24 kHz.

The frequency response of the dual half-bridge SRI-fed IH system for various switching frequencies is presented, and an expression for variations in output voltage concerning frequency is given in Table 2. For stability analysis, the s-domain model of the system is converted into a discrete domain using the bilinear transformation method. The sampling time (t_s) is selected as $t_s \gg 1/(2 * \omega_{gc})$, where ω_{gc} is the gain cross-over frequency. The transient response for various f_s is shown in Figure 2, which demonstrates the necessity of improving the dynamic response of the system based on the poles and zeros for the variations in output voltage concerning the frequency. The frequency response using the Bode plot of the open-loop system is illustrated in Figure 2(a), and stability analysis using a pole-zero plot is shown in Figure 2(b), for 5 cases with different switching frequencies. In case 1, all poles lie inside the unit circle and zeros lie outside the unit circle. In the frequency response, there exist the up-down and down-up glitches with multiple zero crossings in the magnitude plot due to low damping of oscillations.

In case 2, poles and zeros lie outside the unit circle, which creates an instability problem. Also, in frequency response, there exist up-down glitches with multiple zero crossings in the magnitude due to the low damping oscillations. In case 3, the system is stable as poles and zeros lie inside the unit circle. However, there are up-down glitches and multiple zero crossings in the frequency response due to which the system becomes conditionally unstable. In case 4, poles lie outside the unit circle and zeros lie inside, which creates conditionally marginal stability in the system. There are also exist the up-down glitches in the frequency response with a single zero crossing in the magnitude plot. In case 5, it is confirmed from the pole-zero plot that poles lie outside the unit circle and zeros lie inside, creating the instability issue, and also there exist up-down glitches in the frequency response of the system. It is confirmed from the analysis that the system is stable only for a 20 kHz switching frequency, whereas there also exist multiple zero cross-over points in the magnitude of the frequency plot. This results in low

damping oscillations and stability issues. Hence, the design of a proper compensator is mandatory to overcome the said issue.

3.2. Compensator Design for Dual-Frequency HB SRI-Fed IH System. The closed-loop PI compensator is designed to supervise the system's stability for various switching frequencies. The block diagram of the closed-loop system with unity feedback ($H = 1$) is illustrated in Figure 3. The expression for the plant G_{Pd} is given in Equation (17). The gain of the VCO (G_{vco}) is fixed at 1000 and the expressions pertaining to the PI compensator are $G_{PI} = k_p + k_i/s$. The values of the proportional gain (k_p) = 0.001 and integral gain (k_i) = 7.526 are designed using the MATLAB SISO tool. The frequency response of the developed IH system is plotted for various values of the switching frequencies, and these are presented as various cases. The values of switching frequencies and the transfer function of the output power to the switching frequency for each case are expressed in Table 3. The frequency response of each case is shown in Figure 4 to illustrate the improvement in the performance of the system when compared with the open-loop study. The Bode diagram and pole-zero plot for various switching frequencies under different cases are illustrated in Figures 4(a) and 4(b), respectively. It is understood from the figures that, in case 1, poles and zeros lie away from the unit circle and there is an up-down glitch in the frequency response. In case 2, poles lie inside the unit circle and zeros lie outside the unit circle, which leads to a nonminimal phase in the system. Also, in frequency response, there exist the up-down and down-up glitches which result in high transients on the output side.

In case 3, the poles of the system lie on the unit circle and zeros lie inside the unit circle. Hence, the system is marginally stable, but there exists the up glitch, up-down, and down-up glitches in the frequency response, which result in the poor transient response of the system. In case 4, poles lie outside and zeros lie inside the unit circle, which leads to instability in the system, and also there existmultiple phase cross-over points with reduced glitches as compared with previous cases. In case 5, poles lie outside and zeros lie inside the unit circle, which results in a down-up glitch and multiple phase cross-over points in the frequency response of the system. This leads to instability issues and poor transient performance of the system. Though the performance of the designed system is satisfactory as compared with the open-loop system, it is necessary to optimize the values of controller gain to make the system stable with an improved dynamic response.

3.3. Optimizing k_p and k_i Using Floquet Stability Criterion. The Floquet theory is used to obtain the stability of the time domain periodic system. The state transition matrix (ϕ) of (9) and (10) is [24]

$$\varphi(t, t_0) = P(t)e^{Q(t-t_0)}P^{-1}(t_0), \tag{19}$$

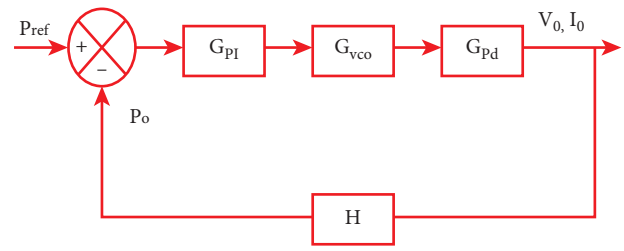


Figure 3: General block diagram of the closed-loop system with PI compensator.

where $P(t)$, Q, and t_0 represent the nonsingular periodic matrix, constant matrix, and arbitrary constant with zero as the initial value, respectively.

The DC operating point of the dual half-series resonant inverter is obtained with steady-state equations of the converter. It is found that, for any value of period T, condition $X(t) = X(t + T)$ is satisfied. Hence, the Floquet theorem can be applied to this system as it is periodic in nature. The expression pertaining to perturbation of duty cycle and switching frequency is given in Equations (1)–(8).

The condition for the system's stability is given by [25]

$$\lim_{n\longrightarrow\infty} = \left\|A^n\right\| = 0. \tag{20}$$

By the final value theorem, the system's stability is confined by the modulus of all eigenvalues of matrix A, which should be less than 1.

A and ϕ matrixes are constant for dual-frequency HB series resonance inverter, and Eigenvalues of the A matrix are obtained by $|\lambda I - A| = 0$. According to the Floquet theorem, a system is stable when the magnitude of the maximum value of the eigenvalue (λ_{max}) is less than one, i.e., $\lambda_{max} = \max |\text{eig (A)}| < 1$ for $T \neq 0$ and unstable for $\lambda_{max} > 1$. This relation helps in obtaining the stability of the dual-frequency converter for variations in output voltage with a fixed duty cycle.

The stability analysis of the dual half-bridge series resonant inverter is obtained by calculating the closed-loop transfer function of matrix A. The steady operating frequency is substituted as 20 kHz for load 1 and 80 kHz for load 2 in (18), and closed-loop controller gain is obtained as $k_p = 0.001$ and $k_i = 7.526$. According to the Floquet theorem, the system is stable for $\lambda_{max} < 1$. The stability of the system is investigated under two conditions as listed below:

Case 1.: In order to obtain the stability of the system, the value of k_p is fixed at 0.001 and k_i is varied from 6 to 14. An Eigenvalues plot for fixed k_p and varying k_i is shown in Figure 5. It is inferred from the plot that, for $k_i = 6$, the maximum value of eigenvalue is less than 1. Hence, according to the Floquet theory, the IH system is stable for $k_i \leq 6$.

Case 2.: Similarly, in order to estimate the k_p value, k_i is selected as 6 and k_p is varied from 0.003 to 0.0008. The respective plot is shown in Figure 6. It is understood

Table 3: Parameters of the converter and transfer function for each case with $k_p = 0.001$ and $k_i = 7.526$.

Case	Frequency (kHz)	Transfer function	Remarks
1	20	$\frac{-0.00054409(z-1.716)(z-0.9785)(z-0.578)}{(z-0.08503)(z^2-0.4584z+0.1942)(z^2-2.792z+2.209)} / \frac{(z-1)(z-1.059)(z-0.9291)(z-0.5766)(z-0.001522)}{(z^2-3.421z+3.056)(z^2-0.4423z+0.1808)}$	Poles, zero far away from the unit circle, up-down glitch
2	21	$\frac{-0.00053575(z-2.98)(z-0.9785)(z-0.7292)}{(z-0.03905)(z^2-1.118z+0.3233)(z^2-0.3049z+0.03889)} / \frac{(z-0.9646)(z-0.7329)(z-0.01836)(z^2+1.075z+0.2972)}{(z^2-0.289z+0.03816)(z^2-0.7794z+0.0385)}$	Poles inside zero outside, up-down and down-up glitches
3	22	$\frac{0.00012195(z+7.676)(z-0.9785)}{(z^2-0.08753z+0.06415)(z^2+0.1664z+0.07043)(z^2-0.1284z+0.1896)} / \frac{(z-0.7329)(z^2+1.964z+0.9842)(z^2+1.707z+0.0715)}{(z^2-0.1504z+0.1078)(z^2-0.08469z+0.213)}$	Poles on the unit circle zero inside, up glitch, up-down, and down-up glitches
4	23	$\frac{5.5486*10^{-5}(z+13.16)(z-0.9785)}{(z^2-0.4947z+0.06768)(z^2+0.4825z+0.07938)(z^2-0.8809z+0.2171)} / \frac{(z-1.84)(z-1.015)(z-0.01396)(z^2+0.4947z+0.06769)}{(z^2-0.4825z+0.07938)(z^2-0.08809z+0.2171)}$	Poles outside and zero inside, multiple phase cross-over point
5	24	$\frac{7.6821*10^{-7}(z+648.3)(z-0.9785)}{(z^2-0.955z+0.2443)(z^2+0.4258z+0.08126)(z^2-0.3234z+0.07547)} / \frac{(z-1.005)(z-1)(z-0.00788)(z^2+1.099z+0.3155)}{(z^2-0.4265z+0.08135)(z^2-0.3303z+0.08281)}$	Poles outside and inside the unit circle, multiple phase cross-over points

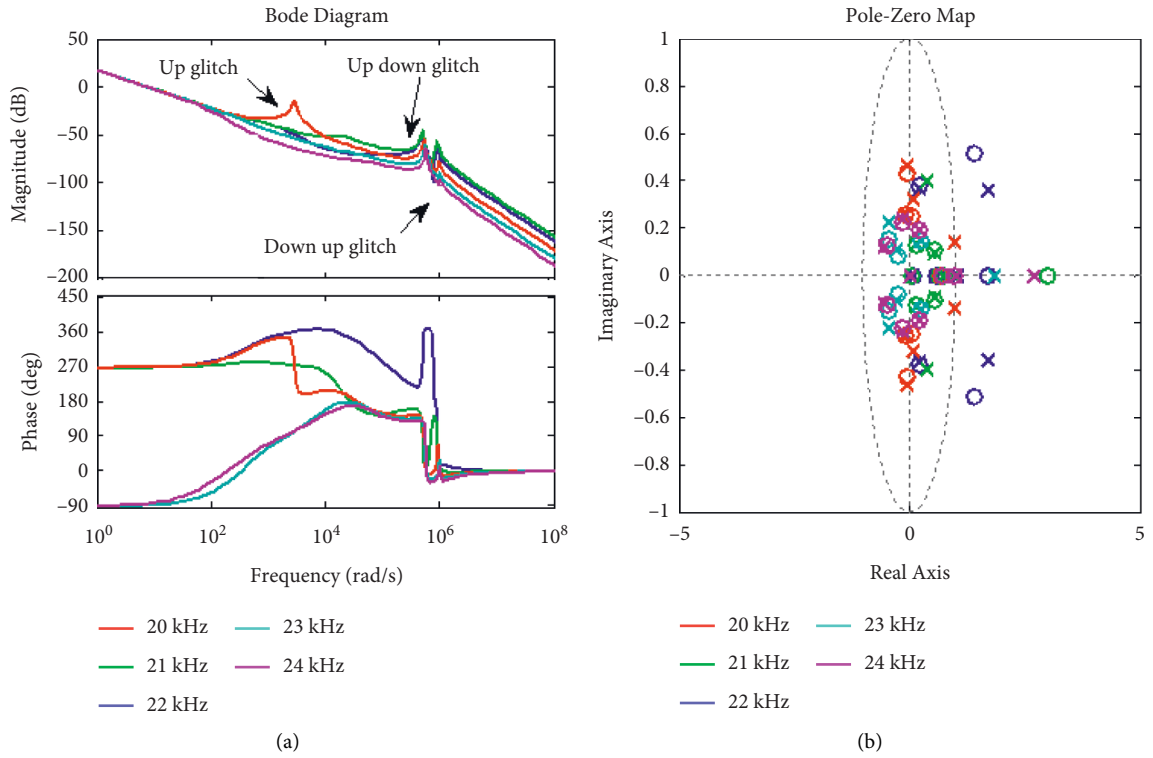


FIGURE 4: Compensated frequency response of the converter for different frequencies. (a) Bode diagram, (b) pole-zero map.

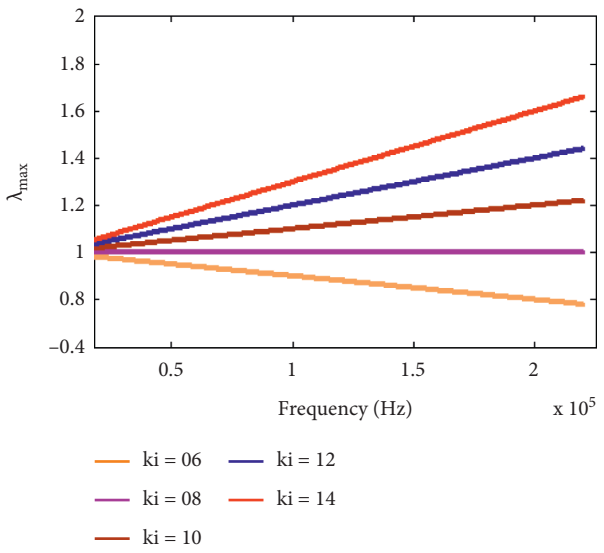


FIGURE 5: Eigenvalues plot for fixed k_p and varying k_i.

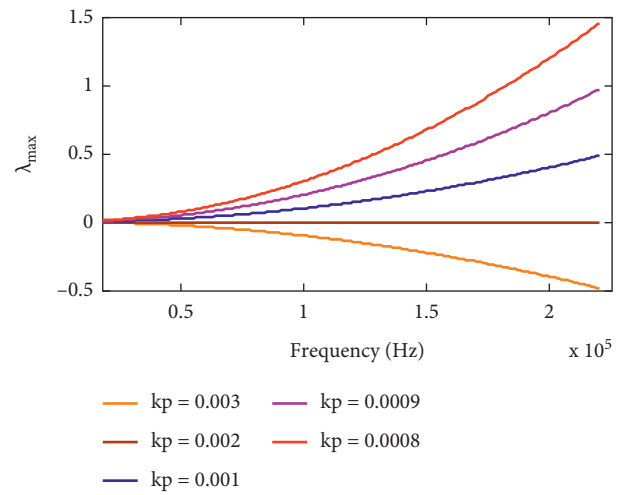


FIGURE 6: Eigen values plot for fixed k_i and varying k_p.

from the plot that the system is stable for $k_p \leq 0.003$, as the value of λ_{max} is greater than 1. Hence, for the stable operation of the system, the marginal values of k_p and k_i should be chosen to be greater than 0.003 and less than 6, respectively.

The frequency response of the converter for the optimized value of $k_p = 0.004$ and $k_i = 4$ is shown in Figure 7. It is inferred from the figure that, for all the five cases, the poles and zeros of the system lie inside the unit circle, which ensures the stability of the system. Also, up-down, down-up glitches are less in all five cases when compared with the compensated frequency response of the converter. The step response of the system with and without optimized values of k_p and k_i for 20 kHz, 22 kHz, and 24 kHz is shown in Figure 8. It is inferred from the response that the system has minimum peak overshoot, faster rise, and settling time for the optimized values of $k_p = 0.004$ and $k_i = 4$.

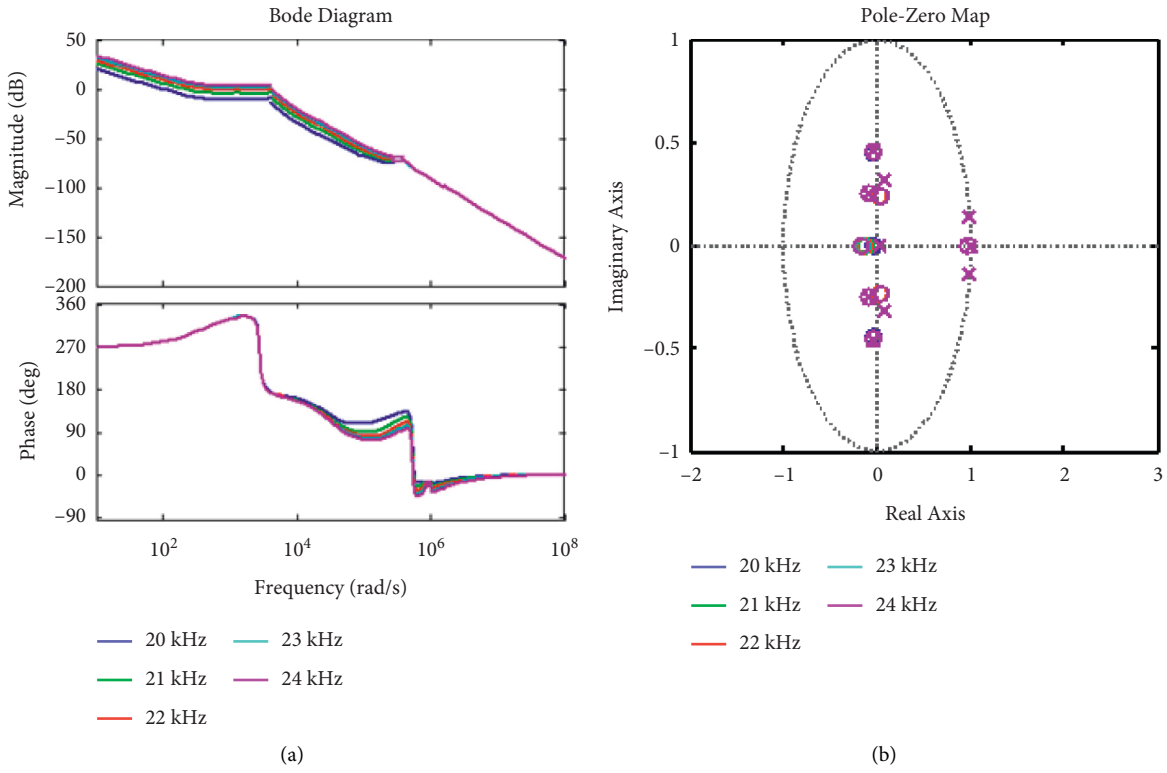


Figure 7: Frequency response of the converter for the optimized value of k_p and k_i. (a) Bode plot, (b) pole-zero map.

4. Simulation Results of the Developed System

Simulation of a dual HB SRI-fed IH system is carried out in MATLAB as per the listed specifications. The performance of the system is studied for different cases, as listed below.

4.1. Open-Loop Response of Dual-Frequency Half-Bridge SRI-Fed IH System. The dual half-bridge SRI is designed to operate with a 20 kHz switching frequency for load 1 and an 80 kHz switching frequency for load 2. The switching frequency ratio is maintained as 1 : 4 so that the capacitor values are chosen appropriately to make each load respond to its frequency and act as a higher impedance path for other frequencies. The power control is achieved by adjusting f_s from 20 kHz to 24 kHz for load 1 and four times greater for load 2. The main waveforms of load 1 and load 2 are illustrated in Figure 9. The output voltage and its expanded waveform are shown in Figures 9(a) and 9(b), respectively. It is inferred from the expanded view that the output voltage includes the superimposition of 20 kHz and 80 kHz output switching frequencies. The output current of load 1 with a 20 kHz switching frequency is illustrated in Figure 9(c), and its expanded view is shown in Figure 9(d). Similarly, the output current of load 2 with an 80 kHz switching frequency is shown in Figure 9(e), and its expanded view is shown in Figure 9(f). The selected capacitors allow 20 kHz current to flow through load 1 and 80 kHz current to flow through load 2 and act as open circuits for other frequencies. The output power waveform of load 1 and load 2 is demonstrated in Figure 9(f). It is inferred that the power dissipation of load 1 is 500 W and load 2 is 250 W at rated operating conditions. Due to the variation in the load impedance of the loads, the power dissipation is not uniform across the loads. It is inferred from Figure 9 that the open-loop system has a high peak overshoot due to the up-down glitches in the frequency response of the converter.

The output power is varied by adjusting the switching frequency of the inverter. In the open-loop study, the output response is noted for a 22 kHz switching frequency for load 1 and 88 kHz for load 2. The main waveform is illustrated in Figure 10. The output voltage waveform is shown in Figure 10(a). Output current of load 1 and load 2 is presented in Figures 10(b) and 10(c) respectively. The RMS value of output current is 4.26 A for load 1 and 3.02 A for load 2. At this switching frequency, there is a 40% decrease in the rated power. Hence, the output power is reduced from 500 W to 200 W in load 1 and 250 W to 100 W in load 2 as illustrated in Figure 10(d). Similarly, the main waveform for the 24 kHz switching frequency for load 1 and the 88 kHz switching frequency for load 2 is presented in Figure 11. The output voltage and current of load 1 and load 2 are shown in Figures 11(a)–11(c) respectively. The RMS value of the output current is 1.28 A for load 1 and 9 A for load 2. At this switching frequency, there is a reduction of 3.6% of the rated power. Hence, the output power is reduced from 500 W to 18 W in load 1 and 250 W to 9 W in load 2, as illustrated in Figure 11(d).

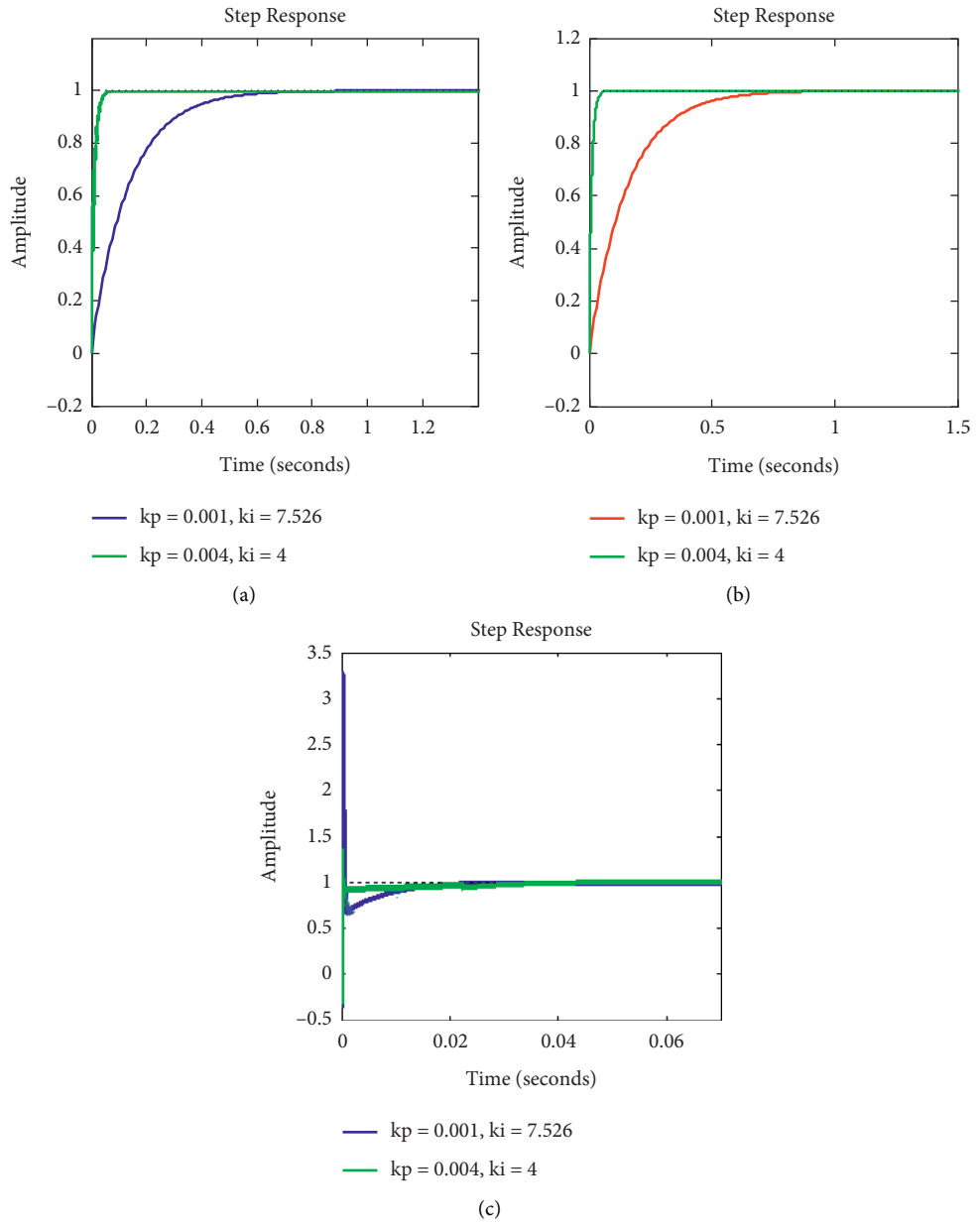


FIGURE 8: Step response of the system with and without optimized k_p and k_i values for the various switching frequencies: (a) 20 kHz, (b) 22 kHz, and (c) 24 kHz.

The computation of output power for various switching frequencies is given in Table 4, and the impact of output power on the switching frequency variations is presented in Figure 12. It is observed from the figure that the output power can be controlled from 100% to 3.6% of the rated power for the variation in switching frequency from 20 kHz to 24 kHz for load 1 and 80 kHz to 88 kHz for load 2.

4.2. Closed-Loop Response of SRI with PI Compensator. Power control plays a vital role in IH applications along with system stability. It is inferred from Figure 2 that the system is stable when operates at a 20 kHz switching frequency (close to resonant frequency) and for other switching frequencies, it is unstable. Hence, the PI compensator is designed to make the system stable, and the performance of the system is included in Table 3. The output response of the system for

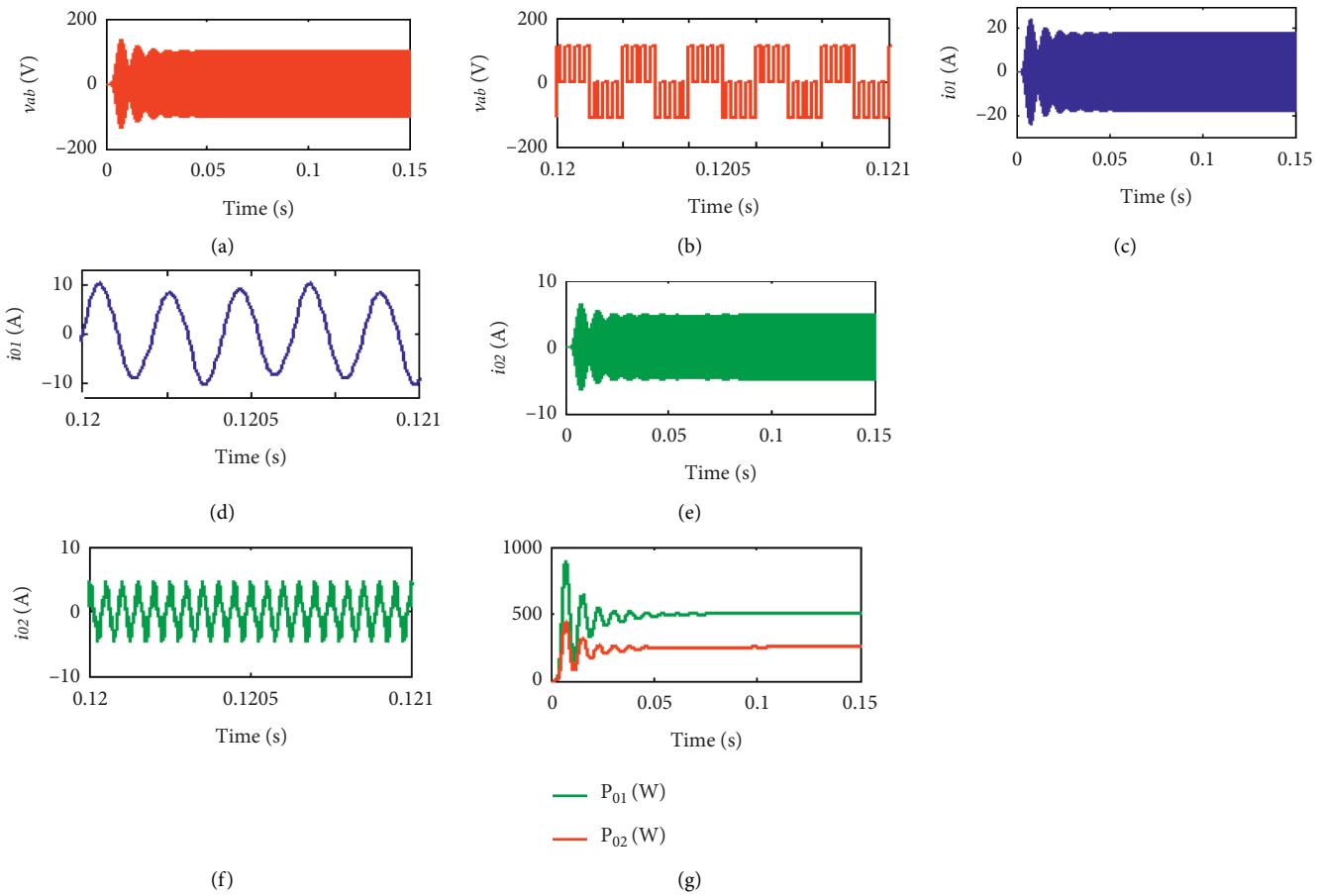


Figure 9: Main waveforms. (a) Output voltage, (b) expanded view of output voltage, (c) output current of load 1 with 20 kHz switching frequency, (d) expanded view of the output current of load 1, (e) output current of load 2 with 80 kHz switching frequency, (f) expanded view of the output current of load 2, and (g) output power.

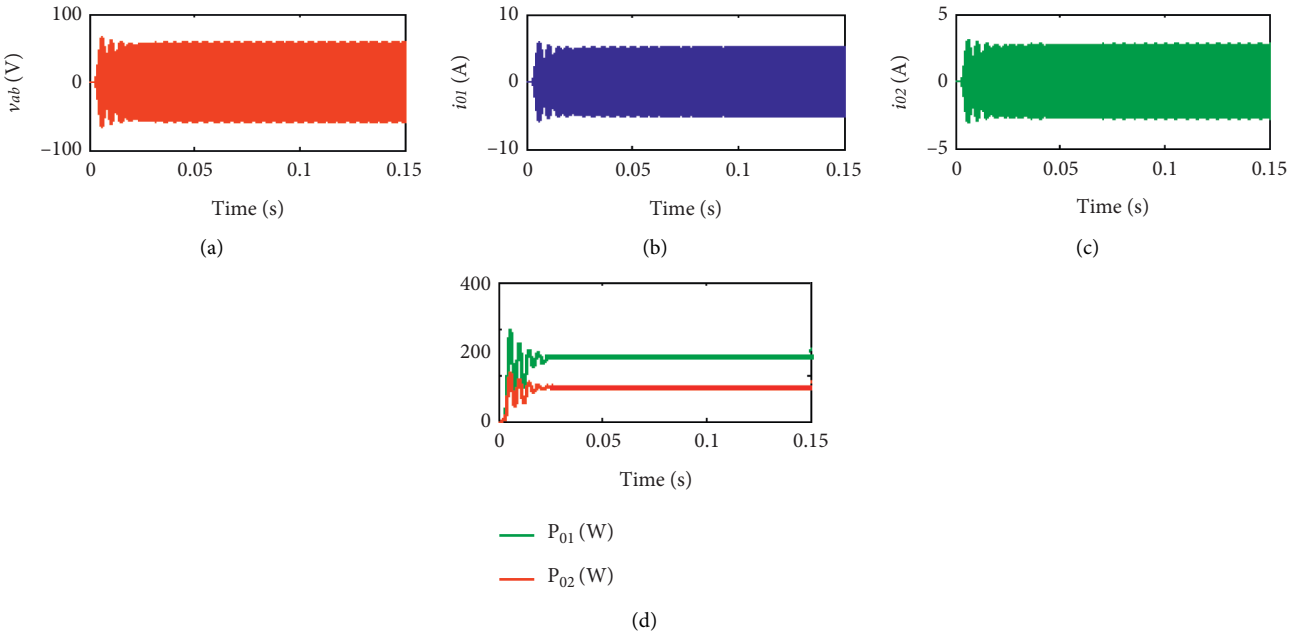


Figure 10: Main waveforms. (a) Output voltage, (b) output current of load 1 for 22 kHz switching frequency, (c) output current of load 2 for 88 kHz switching frequency, and (d) output power.

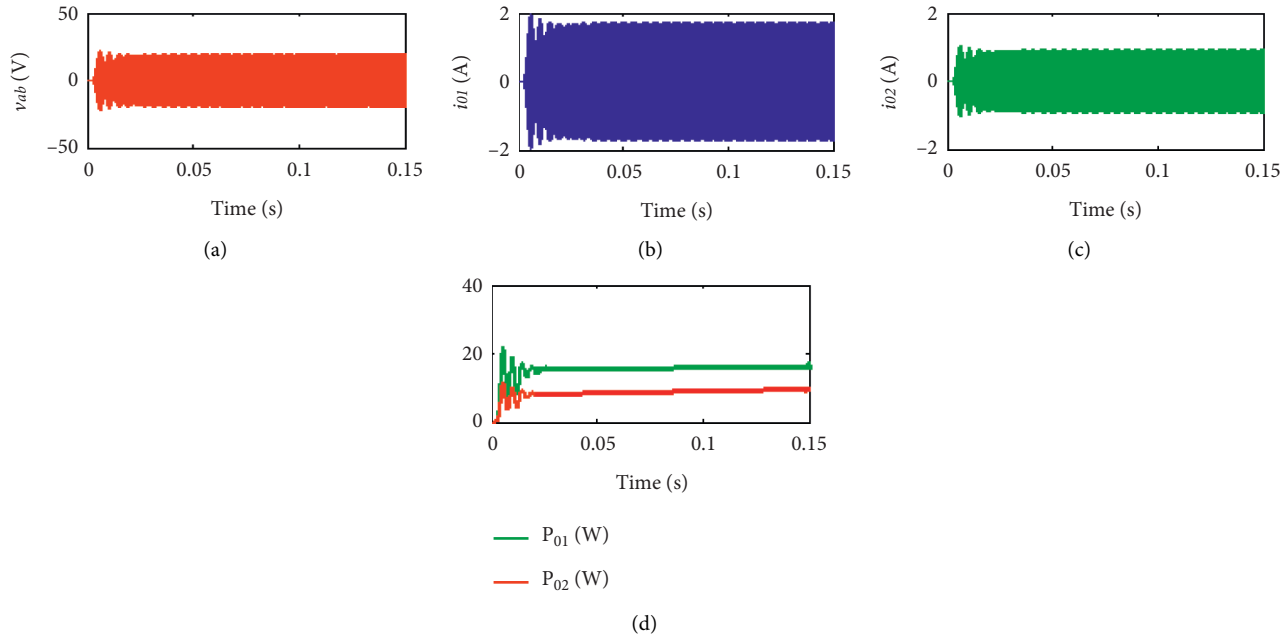


FIGURE 11: Main waveforms. (a) Output voltage, (b) output current of load 1 for 24 kHz switching frequency, (c) output current of load 2 for 48 kHz switching frequency, and (d) output power.

TABLE 4: Computation of output power.

Switching frequency (kHz)		Load 1		Load 2	
Load 1	Load 2	$I_{01(\mathrm{rms})}$ (A)	P_{01} (W)	$I_{02(\mathrm{rms})}$ (A)	P_{02} (W)
20	80	6.74	500	4.77	250
21	82	5.44	325	3.84	162.5
22	84	4.26	200	3.02	100
23	86	3.02	100	2.13	50
24	88	1.28	18	0.90	9

different switching frequencies is obtained using MATLAB/Simulink. The main waveforms for 500 W (load 1) and 250 W (load 2) output power is demonstrated in Figure 13. The output voltage waveform is shown in Figure 13(a). The output current waveform for load 1 and load 2 is illustrated in Figures 13(b) and 13(c), respectively. It is inferred from the figure that the system possesses a better response in terms of peak overshoot (% M_{p}), rise time (t_{r}), peak time (t_p), settling time (t_{s}), and steady-state error (e_{ss}). The output power waveform for load 1 and load 2 is illustrated in Figure 13(d). In order to test the performance of the system, the set power is varied from 18 W for load 1 and 9 W for load 2 respectively. The main waveform is illustrated in Figure 14 and its output voltage is presented in Figure 14(a). The output current waveform for load 1 and load 2 is illustrated in Figures 14(b) and 14(c), respectively. It is inferred from the waveforms that, as the switching frequency of the system is varied, the output power also varies, which is illustrated in Figure 14(d). Though the performance of the system is better when compared with an open-loop system, it is stable only for a 20 kHz switching frequency with an oscillation in the output waveforms. Hence, the values of controller gains need to be optimized to make the system stable with less time domain specifications.

4.3. Closed-Loop Response of SRI with Optimized PI Compensator. Any practical real-time system should be stable with lesser time-domain specifications. Hence, the values of controller gain are optimized using the Floquet stability criterion, and the values of k_p and k_i are chosen as 0.004 and 4, respectively. The output waveform forms for 500 W (load 1) and 250 W (load 2) is illustrated in Figure 15. The output voltage waveform is illustrated in Figure 15(a), and loads 1 current, load 2 current, and output power are illustrated in Figures 15(b)–15(d), respectively. It is observed that the system possesses a good dynamic behaviour, and also it is evident from Figure 7 that the system is stable. In

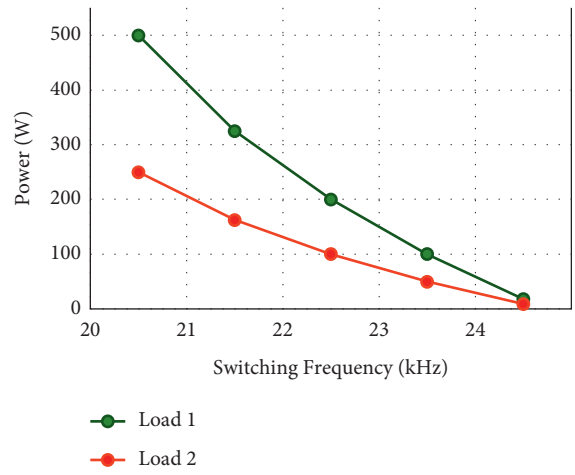


Figure 12: The impact of output power on the switching frequency variations.

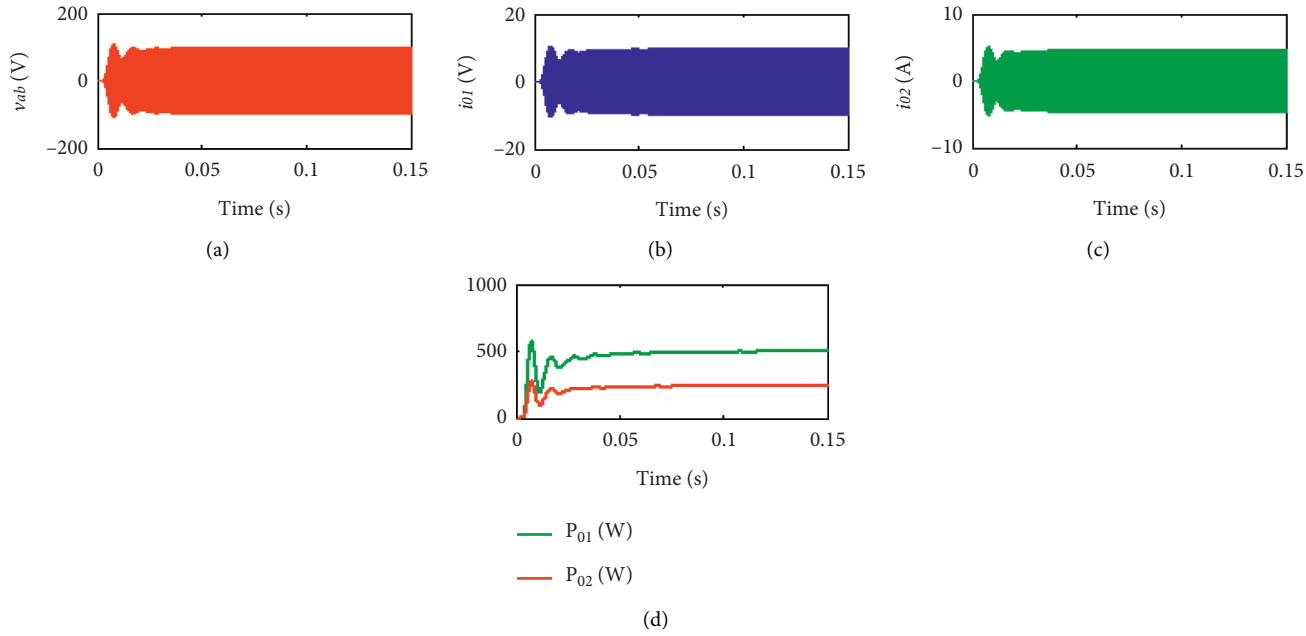


Figure 13: Main waveforms. (a) Output voltage, (b) output current of load 1 for 500 W set power, (c) output current, and (d) output power of load 2 for 250 W set power.

order to validate the performance of the proposed controller, the set power is adjusted from 500 W to 18 W in load 1 and 250 W to 9 W in load 2. The corresponding output voltage, load 1 current, load 2 current, and power waveform is illustrated in Figure 16, and the time domain response of the system is included in Table 5. It is observed that the output response of the system is better at this set power and it is also inferred that the optimized PI compensated system has a better response in terms of t_r, t_p, t_s, $\%M_p$ and e_{ss}.

5. Hardware Results of the Developed System

The validation of the proposed converter with the control algorithm is being performed using the PIC16F877A. The output pulses are amplified using a TLP250 driver IC. The HB inverter is developed with two H20R1203 IGBTs. The load current is measured using a SIGLENT CP4060 current probe and waveforms are recorded using an MDO3024 optical oscilloscope. The temperature rise in the load is studied using the FLIR E75 24° a thermal imager. The photograph of the dual-frequency HB SRI is shown in Figure 17.

From the analysis and simulation study, it is noted that the developed system is stable for the optimized values of k_p and k_i. Hence, the prototype is developed with these optimized values for the set power of 500 W (load 1) and 250 W (load 2). The output voltage and current waveforms are illustrated in Figure 18(a). The expanded view of the output voltage and current waveforms of load 1 and load 2 is

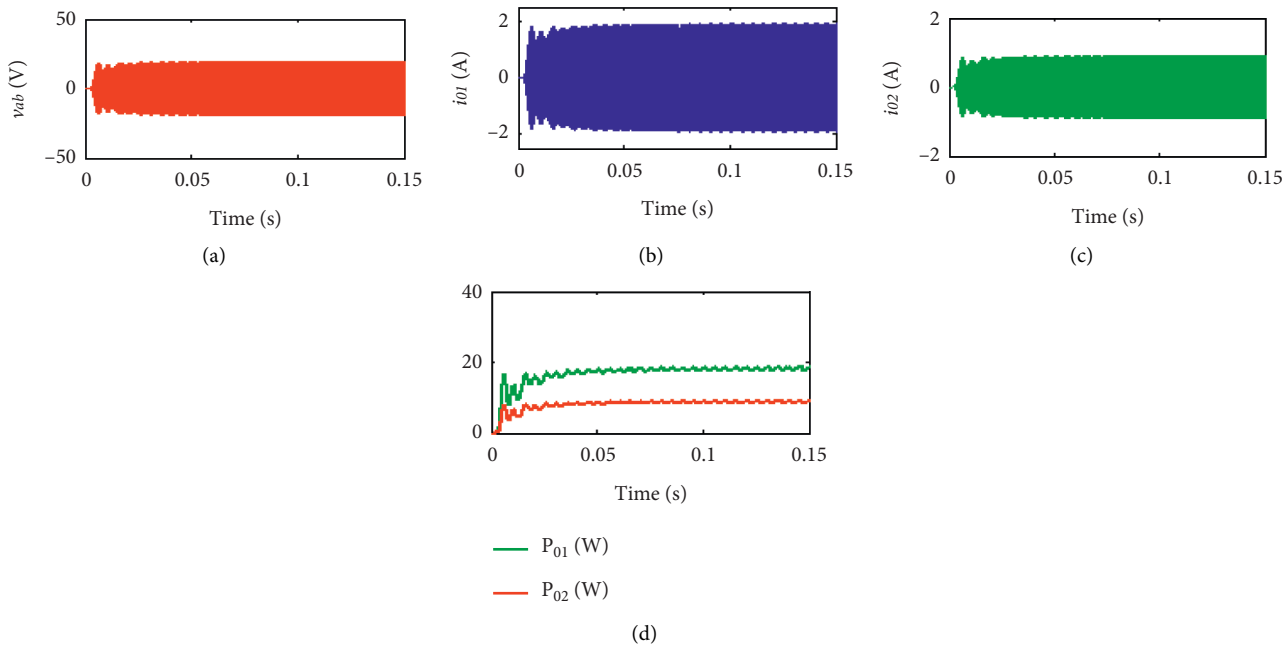


FIGURE 14: Main waveforms. (a) Output voltage, (b) output current of load 1 for 18 W set power, (c) output current, and (d) output power of load 2 for 9 W set power.

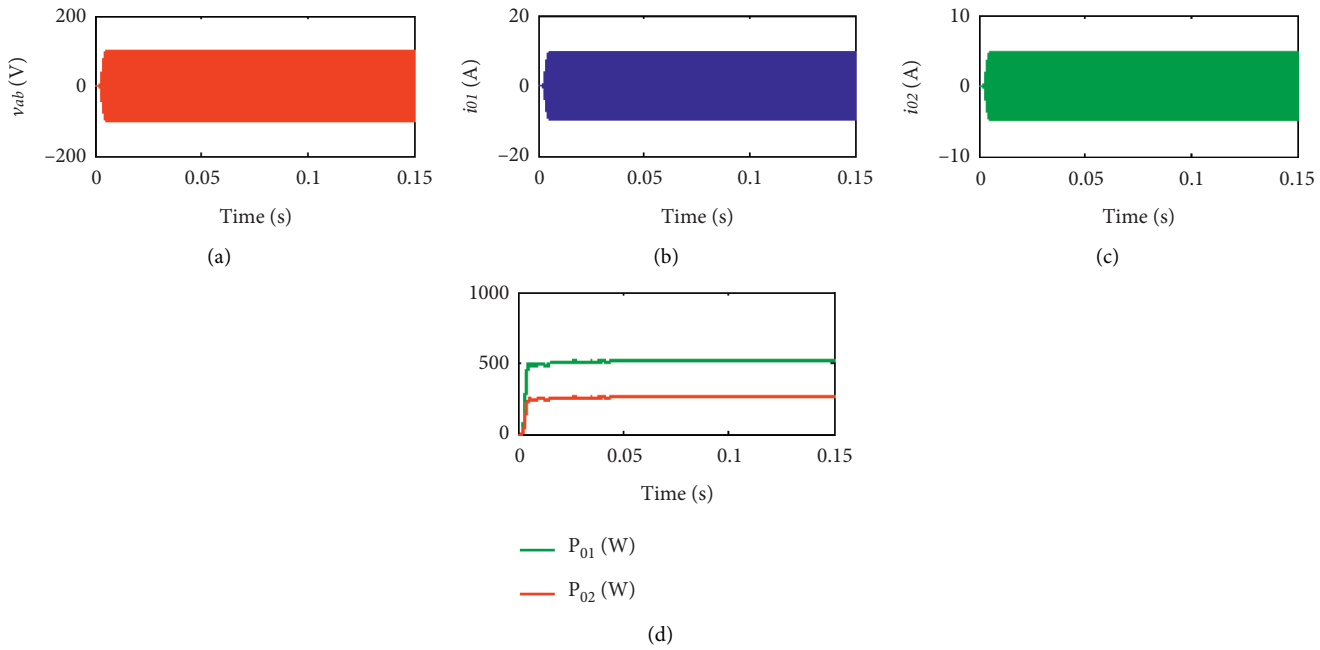


FIGURE 15: Main waveforms. (a) Output voltage, (b) output current of load 1 for 500 W set power, (c) output current, and (d) output power of load 2 for 250 W set power.

illustrated in Figures 18(b) and 18(c), respectively. Similarly, output voltage and current waveforms for 50 W (load 1) and 25 W (load 2) output power are shown in Figure 19. It is inferred from the figure that the output has a smooth response and also the simulation and hardware results are in line with each other.

The temperature study is carried out in the COMSOL Multiphysics software. FEM simulation is analyzed using heat transfer and magnetic field solvers by providing current, switching frequency, and load properties as the input. The system geometry has meshed with 20134 triangular elements. The contour plot of load 1 and load 2 is shown in

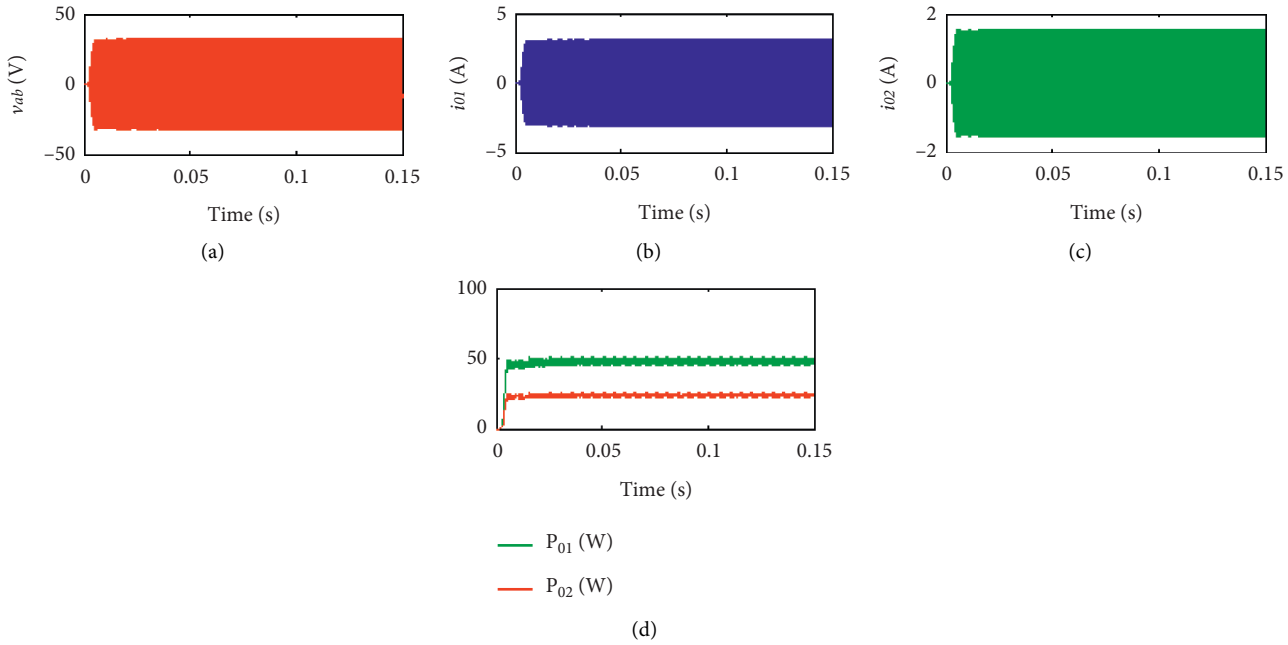


Figure 16: Main waveforms. (a) Output voltage, (b) output current of load 1 for 50 W set power, (c) output current, and (d) output power of load 2 for 25 W set power.

Table 5: Time domain response of the system.

Specifications	t_r (s)	t_s (s)	% M_p	e_{ss}
Open-loop system	0.005	0.05	80	—
PI compensated system	0.003	0.015	40	10 W (load 1) 5 W (load 2)
Optimised PI compensated system	0.0085	0.0001	0.1	0.01 W (load 1) 0.005 W (load 2)

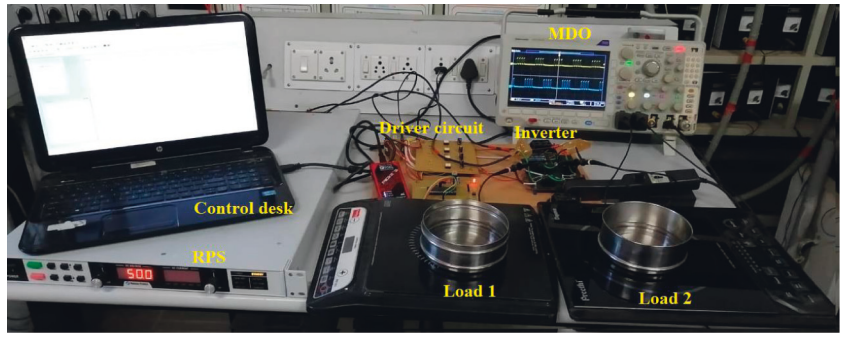
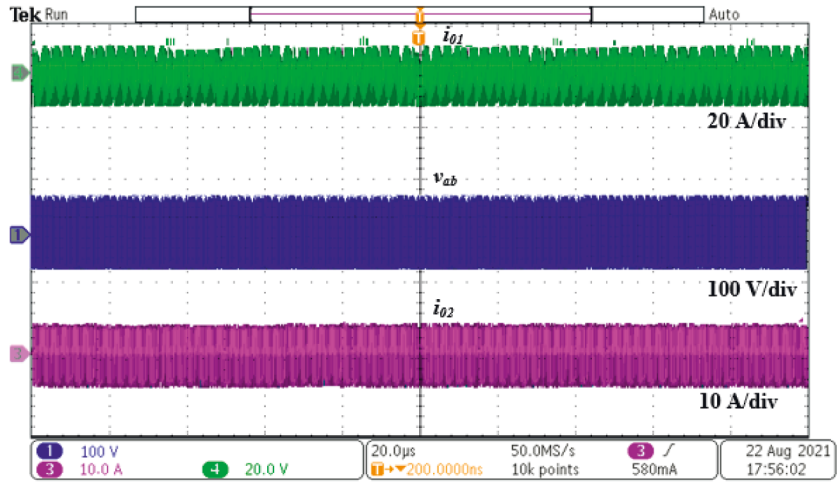


Figure 17: Photograph of the dual-frequency HB SRI.

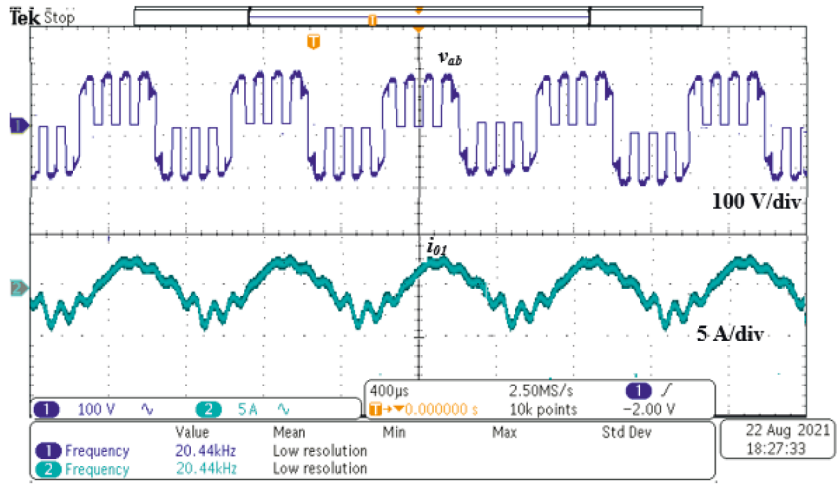
Figures 20(a) and 20(b), respectively. The temperature distribution is evident from the plot. The experimental temperature plot is illustrated in Figure 20(c). The thermal rise is taken at the period $t = 160$ s for both loads. The maximum temperature observed was 77°C on in both the loads. An efficient comparison of the systems is illustrated in Figure 21.

5.1. The Main Achievement of the Research Work. The following points are distinctive concerning the stability analysis of the dual-frequency half-bridge inverter with variable frequency control:

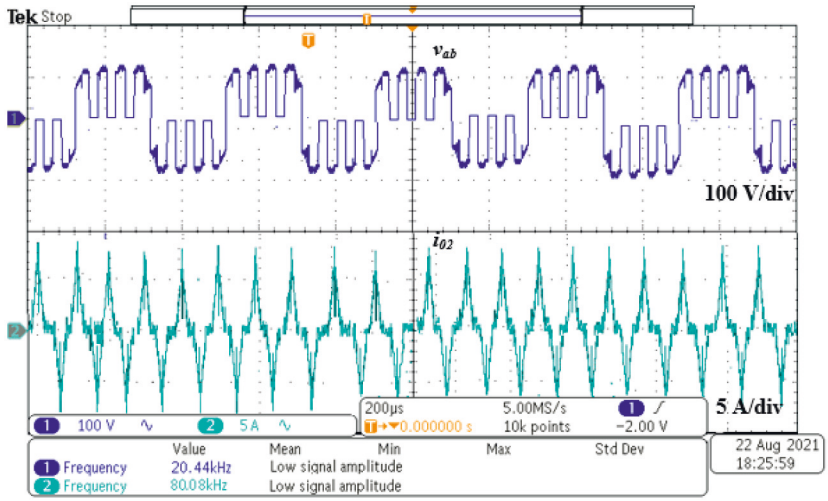
(i) Output power is controlled from 90% to 10% of the rated power.



(a)



(b)



(c)

Figure 18: Main hardware waveforms for the power of 500 W (load 1) and 250 W (load 2). (a) Output voltage and current waveforms, (b) expanded output voltage and current waveforms of load 1, and (c) expanded output voltage and current waveforms of load 2.

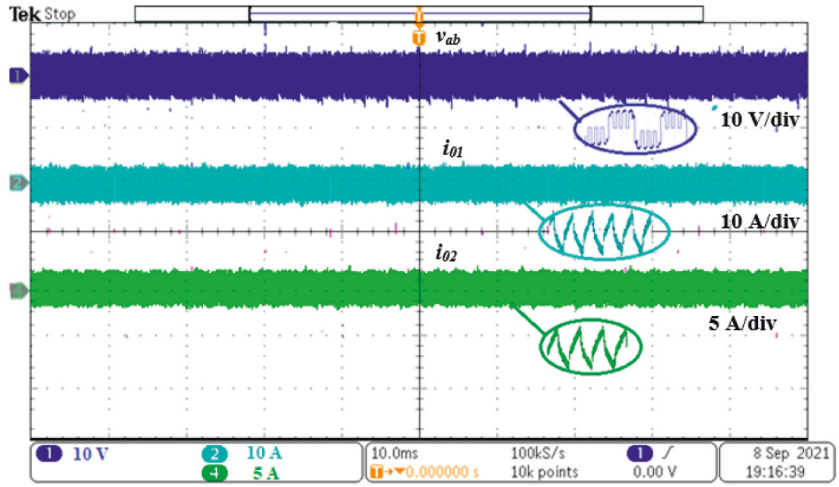
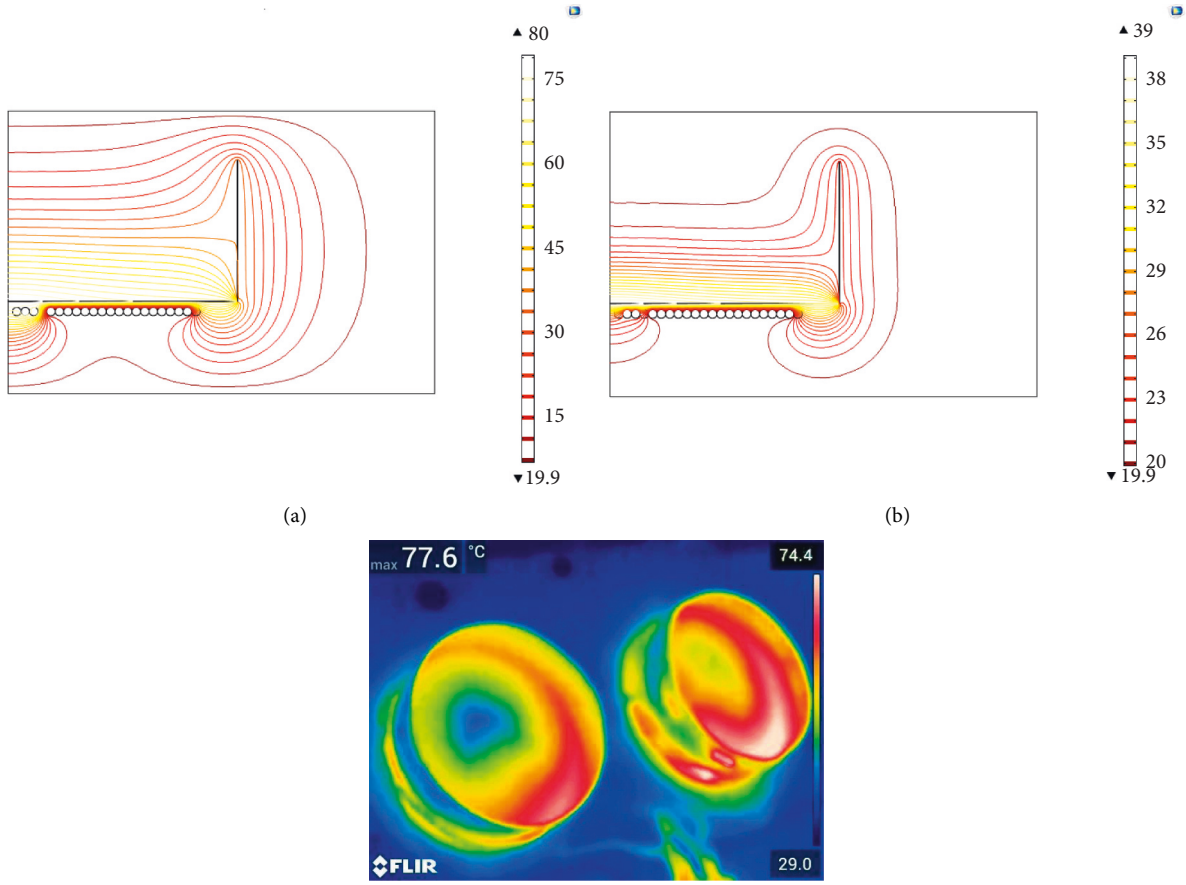


Figure 19: Main hardware voltage and current waveforms for 50 W (load 1) and 25 W (load 2) output power.



(a) (b)

(c)

Figure 20: Thermal image. (a) Contour plot of load 1, (b) contour plot of load 2, and (c) experimental.

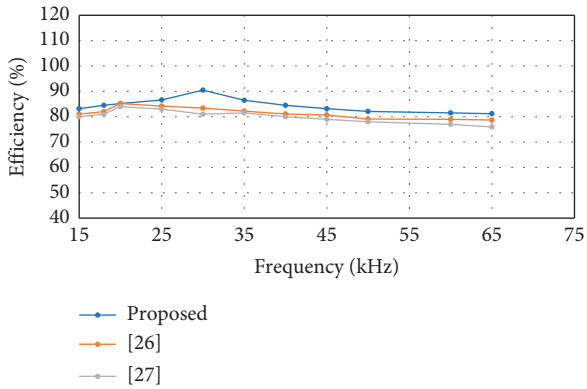


Figure 21: Efficiency comparison of the system.

(ii) The proposed inverter processes at a higher efficiency of 90.5% at the resonant frequency.

(iii) The output power is controlled independently.

(iv) The frequency of the inverter is varied to control the output power.

6. Conclusion

In this work, stability analysis of the converter is carried out based on the Floquet theory with the small-signal model of the inverter. The behaviour of the system is studied in open loop and closed loop using a PI compensator. It is found that the system becomes unstable when the switching frequency is varied. Hence, the values of controller gain are optimized using the Floquet theory to get a stable system with a better time domain response. The stability analysis is carried out for the system with the frequency variation of 20 kHz to 24 kHz for load 1 with the power variation of 500 W to 18 W and with a frequency variation of 80 kHz to 88 kHz for load 2 with a power variation of 250 W to 9 W. It is noted from the output response that the rise time is 0.0085 s, the peak time is 0.0001 s, and peak overshoot is 0.1% with minimum steady-state error. The optimized compensated system possesses better dynamic response as compared to the open-loop system and compensated system. The temperature distribution on the load is studied using FEM software and captured in real time using a FLIR thermal imager.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Authors' Contributions

Belqasem Aljafari conceptualized the study, designed the methodology, wrote the original draft, provided the resources, and performed software analysis. Pradeep Vishnu Ram validated the study, performed the formal analysis, investigation, and visualization, and reviewed and edited the manuscript. Suresh Kumar Alagarsamy reviewed and edited the manuscript and performed the software analysis. Hassan Haes Alhelou supervised the study and administered the project.

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