Mobile Information Systems

Advanced AI Technologies for Industrial Internet of Things Applications

Lead Guest Editor: Lingwei Xu
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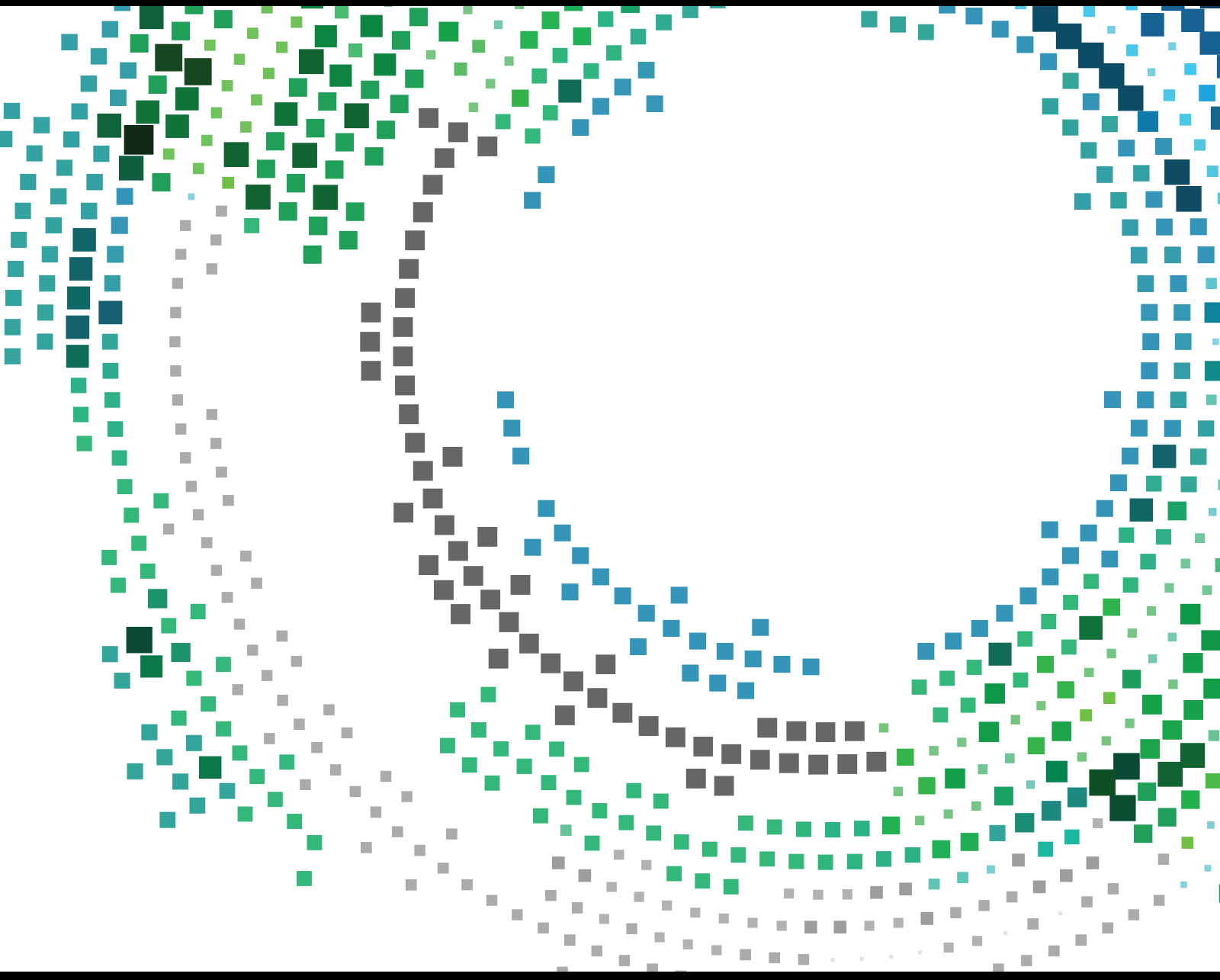

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Research Article

Analysis on Simplified Method of IoT-based HHL Algorithm Corresponding Quantum Circuit for Quantum Computer Application

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Whether it is a traditional industry or a Frontier field, it has unveiled the trend of industrial IoT construction and application, which plays a vital role in building a strong manufacturing country and promoting high-quality economic development in China. HHL algorithm has become one of the important quantum algorithms, but there are few researches on the construction of quantum circuits and the application of quantum sequencing. In this paper, a model based on the quantum circuit corresponding to the HHL algorithm to deal with the quantum application problem is proposed. A quantum circuit based on HHL algorithm is used to solve the linear system, and the numerical solution of the target partial differential equation is obtained. Finally, the experimental analysis shows that, in the process of processing quantum computer application problems based on quantum circuit, it can reduce the computation amount of quantum circuit corresponding to HHL algorithm, improve the simulation efficiency of quantum circuit, and reduce the occupation of hardware resources, which has a certain effectiveness and superiority. This discussion brings new ideas for intelligent IoT technology and provides implications for the study of simplified methods of HHL algorithms corresponding to quantum circuits to deal with computer application problems.

1. Introduction

Along with the development of technology, our country enters into the reform of technology based on the Internet of Things. In addition, artificial intelligence technology is gradually and rapidly developing internationally, gradually forming intelligent IoT system software. Overall, the coming decades will undoubtedly be the era of quantum computing and artificial intelligence, whose research is not only exciting but also full of tests.

At present, the application of quantum algorithms cannot be separated from the process of solving the linear equations, such as partial differential equations corresponding to the problems solved. Solving the linear equations is the basis of solving many problems related to quantum applications. Among them, the HHL algorithm has become one of the important quantum algorithms due to its exponential acceleration effect when solving linear systems [1]. The key to the HHL quantization analysis algorithm is the quantization analysis phase estimation control module, which allows fast exponential value estimation of the characteristic vector material (or phase) of the operator. However, in the process of solving practical problems, how to construct quantum circuits to realize HHL algorithm and realize efficient operation is a very common and difficult problem. Most of the existing solutions are in the theoretical stage, which limits their application scope in the practical application environment [2]. For example, quantum circuits based on the matrix decomposition of the HHL algorithm based on the GLOA (Group Leaders Optimization Algorithm) contain a large number and types of quantum logic gates, resulting in high line complexity, which leads to low

simulation efficiency of quantum circuits and high utilization of hardware resources. The practical application value is not high.

2. Methods and Principles

2.1. Quantum Circuit. Until now, the scientific research of artificial intelligence is basically using traditional computers to implement integrated circuit process of matrix measurement to find. Because this matrix is particularly large, so a long time with a special chip such as a GPU to find it, which is the foothold of quantum computing out. The HHL quantum algorithm is faster than the ordinary computer basically algorithm. When using the problem, only the solution matrix is sparse, the number of preconditions for solving the matrix is relatively low, and the complexity of the time calculation for measuring the absolute value of the solution vector can be reduced from the previous computer's O (NK) to the HHL quantum algorithm [3].

Quantum circuit as an expression of quantum program, also known as quantum logic circuit, is currently the most commonly used general quantum computing model, said abstract concept of quantum bit operation line, its composition includes quantum bits, line (time axis) and various quantum logic gates, and finally often need to perform quantum measurement operation to read out the results.

A true quantum computer is a hybrid structure, consisting of two parts: one is a classical computer, which performs classical calculations and controls; the other part is the quantum device, which is responsible for running quantum programs to perform quantum computations. The quantum program is a series of instructions written by the quantum language such as QRunes language that can be run on the quantum computer, which realizes the support for the quantum logic gate operation and finally, realizes the quantum computation. A quantum program is a series of instructions that operate a quantum logic gate in a certain time sequence [4]. The development of quantum device hardware faces two major problems: a high error rate of quantized bits and a low quantum number of quantum computers.

In practical applications, due to the limitation of the development of quantum equipment hardware, it is usually necessary to conduct quantum computing simulation to verify quantum algorithms and quantum applications. Quantum computing simulation is a process in which the virtual architecture (namely, quantum virtual machine) built with the resources of ordinary computers is used to realize the simulation operation of quantum programs corresponding to specific problems. Often, it is necessary to construct a quantum program that corresponds to a particular problem. The quantum program is a program that represents the quantum bit and its evolution written in classical language, in which the quantum bit and quantum logic gate related to quantum computation are represented by corresponding classical codes.

Quantum circuit as an expression of quantum program, also known as quantum logic circuit, is the most commonly used general quantum computing model, said under the abstract concepts for quantum bit operating line, its composition including quantum bit, a line (timeline), as well as a variety of quantum logic gates, finally often need a quantum measurement operation to the result read out.

Unlike traditional circuits, which are connected by metal wires to transmit voltage or current signals, in a quantum circuit, the wires can be thought of as being connected by time; that is, the state of the qubit evolves naturally over time, following the instructions of the Hamiltonian operator until it meets a logic gate and is operated [5].

2.2. Quantum Linear Analysis. With the continuous development of the big data business and the extensive use of artificial intelligence technology and 5G technology, the scale of data has increased explosively. Quantum computing uses quantum superposition and entanglement to solve the daily tasks of measurement and has certain advantages of speeding up when dealing with practical problems.

A quantum program as a whole should have a total quantum circuit, where the total number of quantum bits in the total quantum circuit is the same as the total number of quantum bits in the quantum program. It can be understood that a quantum program can consist of a quantum circuit, measurement operations of quantum bits in the quantum circuit, registers for saving the measurement results and control flow nodes (jump instructions), and a quantum circuit can contain operations of tens, hundreds, or even thousands of quantum logic gates. Figure 1 shows a classical and quantum circuit performing a "non".

The execution process of a quantum program is the execution process of all quantum logic gates in a certain time sequence. " Timing" refers to the time sequence in which individual quantum logic gates are executed. In classical computing, the most basic unit is the bit and the most basic form of control is the logic gate [6]. The purpose of the control circuit can be achieved by a combination of logic gates. Similarly, one way to deal with quantum bits is through quantum logic gates. Quantum logic gates allow quantum states to evolve. Quantum logic gates are the basis of quantum circuits and are generally represented by a unitary matrix, which is not only a matrix form, but also an operation and transformation. The effect of a general quantum logic gate on a quantum state is calculated by multiplying the left unitary matrix by the corresponding matrix of the right vector of the quantum state [7].

3. Solution Measures and Methods

3.1. Quantum Circuit Model Based on HHL Algorithm. The study of the use of quantum computing in AI is particularly important for the development of AI, and there is no doubt that there should be more frequent and close collaboration among AI researchers, quantum scholars, scientists, and electronic computer scientists. Only in this way, quantum AI can be expected to gain more technicality and power development in the developmental link [8].

This paper tries to solve the problem of dimensionality reduction of high-dimensional data by the quantum method

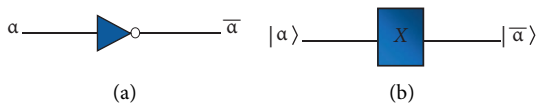

Figure 1: Classical and quantum lines performing "non".

by using the self-developed quantum computing prototype machine, and realizes the sorting application in the prototype machine. We build a quantum circuit based on the HHL algorithm to deal with quantum application problems, as shown in Figure 2.

3.1.1. The Target Partial Differential Equation Is Discretized to Obtain the Corresponding Linear System. The solving process of partial differential equations is also the solving process of corresponding quantum application problems. Can according to the target of partial differential equation of boundary conditions, select the corresponding basis function and form a complete set of nodes, target is given a partial differential equation (the target function) of an approximate linear combination (approximating function, namely, the linear system), namely, the approximating function requirements in all nodes and function (i.e., the original target of the partial differential equation) strictly equal, similar in height on the global. Thus, the lower-order basis function is used to complete the high-precision approximation of the equation solution, which can be called the low-order high-precision advantage [9].

Algorithms are the key to artificial intelligence technology. The Internet platform can link all the factors in industrialized production, the whole industrial chain and customer value, and open the way for the conversion of industrial production expertise to industrial production algorithms, providing a better support point for the establishment of the AI technology base [10].

The HHL algorithm solves A problem of solving linear equations: the input is an $N * N$ matrix A and an n-dimensional vector b, and the output is an n-dimensional vector x, which satisfies $Ax = b$, that is, $x = a - 1b$. The matrix A needs to be invertible, and the dimension of vector B, N, can be expressed as A positive integer power of 2 because of the following need to load the data of vector B onto the quantum circuit [11].

The idea of using the HHL algorithm to solve a system of equations over a finite domain is to transform the system of equations over a finite domain into a Boolean linear system of equations over C., which is then solved by the HHL algorithm, and Figure 3 shows the technical route of the transformation process.

The left end term matrix of the linear system directly constructed by the basis function is relatively dense, and the sparsity is often poor, so it is difficult to cope with the situation of high dimension and large scale, that is, the dimension of differential equation will lead to the rapid expansion of the problem size, and the problem size grows exponentially with the dimension [12]. Therefore, the quantum transformation algorithm can be introduced to transform the linear system into a sparse linear system.

Based on the basis function, we use the corresponding quantum transform algorithm. Here, we choose the quantum shift Fourier transform (QSFT)/quantum cosine transform (QCT) [13]. Both QSFT and QCT can construct corresponding quantum circuits through quantum logic gate operation to realize quantum state transformation, and the operation complexity is low and polynomial logarithmic.

Based on the quantum Fourier transforms, the matrix form of the one-dimensional quantum displacement Fourier transform (QSFT) is defined as follows:

$$F_p^s := \frac{1}{\sqrt{p+1}} \sum_{k,l=0}^{p} \exp\left(\frac{2\pi i\,(k - \lfloor p/2 \rfloor)\,(l - (p+1)/2)}{p+1}\right) |l\rangle\langle k|. \tag{1}$$

Therefore, quantum state transformation can be realized

$$\left|k\right\rangle \longrightarrow \frac{1}{\sqrt{p+1}} \sum_{k=0}^{p} \exp\left(\frac{2\pi i\,(k - \lfloor p/2 \rfloor)\,(l - (p+1)/2)}{p+1}\right) \left|l\right\rangle. \tag{2}$$

Thus, the Fourier transform of dimensional quantum displacement can be defined as follows:

$$F_p^s := p_{j=1}^{d} F_p^s = \frac{1}{\sqrt{(p+1)^d}} \sum_{\|k\|_\infty, \|l\|_\infty \le p} \prod_{j=1}^{d} e^{\left(2\pi i \left(k_j - \lfloor p/2 \rfloor\right)\left(l_j - (p+1)/2\right)/p+1\right)} \left|l_1 \cdots \left|l_d k_1\right| \cdots k_d\right|. \tag{3}$$

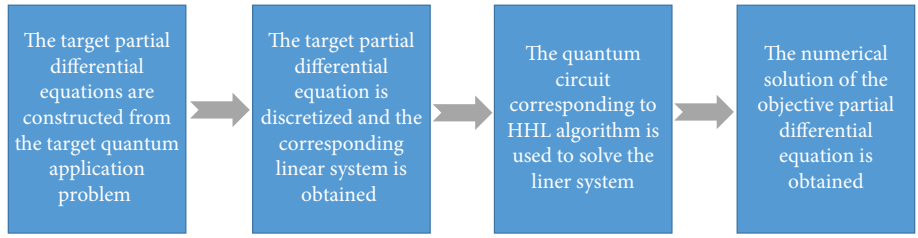

Figure 2: Handling quantum application problems.

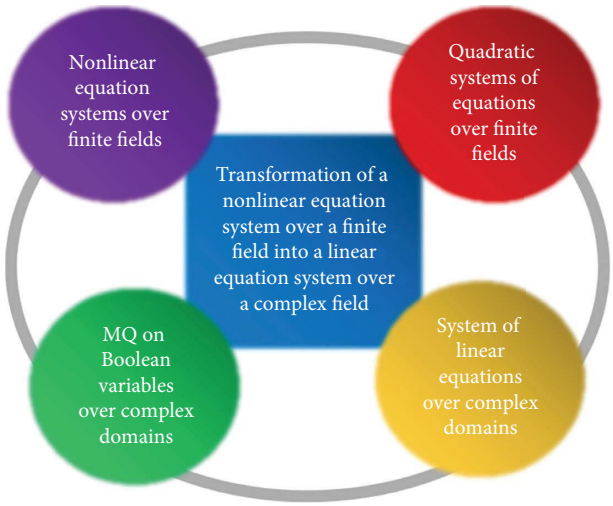

Figure 3: Conversion route of nonlinear and linear equation systems.

Among them, $k = (k_1, \cdots, k_d), k_j \in [p]_0, j \in [d]$,k、 l indicator notation for values 0 through p, $|1|k$ represents the corresponding basis vector, $\|k\|_\infty, \|l\|_\infty$ expressed as the infinite norm, $[p]_0$ expressed as the integer set from 0 to p, $[d]$ is the integer set of 1 to d, and p represent the quantum bit number required for the corresponding quantum line.

In practical application, one-dimensional QSFT can be disassemble:

$$F_p^s = S_p F_p R_p. \tag{4}$$

Among them F_p is the quantum Fourier transform, $S_p$and R_p is the unitary transformation mapped to its own space:

$$\begin{aligned} S_p &= \sum_{k=0}^{p} e^{-(2\pi i \lfloor p/2 \rfloor (l-(p+1)/2)/p+1)} |l\rangle\langle l|, \\ F_p &= \sum_{k,l=0}^{p} e^{(2\pi i k l/p+1)} |l\rangle\langle k|, \\ R_p &= \sum_{k=0}^{p} e^{-(2\pi i k (p+1)/2/p+1)} |k\rangle\langle k|. \end{aligned} \tag{5}$$

The whole QSFT line is obtained by constructing quantum lines, respectively.

The principle that quantum cosine (QCT) transformation can be defined by the discrete cosine transformation (DCT) as follows:

$$\hat{v}_l = \sqrt{\frac{2}{p}} \sum_{k=0}^{p} \delta_k \delta_l \cos \frac{kl\pi}{p} v_k, v, \hat{v} \in \mathbb{C}^{p+1}, l \in [p+1]_0. \tag{6}$$

Among them, $\mathbb{C}^{n+1}$ represents the complex space of the $(p+1)$ dimension, v_k represents the original signal, $\hat{v}_l$ represents the coefficient after the DCT transformation, δ_k, δ_l represents the defined function:

$$\delta_k := \begin{cases} \frac{1}{\sqrt{2}}, k = 0, p, \\ 1, k \in [p-1], \end{cases} \quad \delta_l := \begin{cases} \frac{1}{\sqrt{2}}, l = 0, p, \\ 1, l \in [p-1]. \end{cases} \tag{7}$$

Similarly, the matrix forms of one-dimensional and multidimensional QCT transformations are given, respectively:

$$\begin{aligned} C_p &:= \sqrt{\frac{2}{p}} \sum_{k,l=0}^{p} \delta_k \delta_l \cos \frac{kl\pi}{p} |l\rangle\langle k|, \\ C_p &:= \otimes_{j=1}^{d} C_p = \sqrt{\left(\frac{2}{p}\right)^d} \sum_{\|k\|_\infty, \|l\|_\infty \le p} \\ &\prod_{j=1}^{d} \delta_{k_j} \delta_{l_j} \cos \frac{k_j l_j \pi}{p} |l_1\rangle \cdots |l_d\rangle\langle k_1| \cdots \langle k_d|, \\ k &= (k_1, \cdots, k_d), \\ l &= (l_1, \cdots, l_d), k_j, l_j \in [p+1]_0. \end{aligned} \tag{8}$$

Combined with the good properties of the selected basis function and quantum displacement Fourier transform/quantum cosine transform, the corresponding quantum circuit operation can be constructed to efficiently complete the sparse operation of the linear system [14]. The left end item matrix of the linear system constructed directly by the

basis function is relatively dense, and after this transformation, the left end item matrix becomes sparse, which is conducive to solving high-dimensional large-scale problems.

3.1.2. The Quantum Circuit Corresponding to HHL Algorithm Can Obtain the Numerical Solution of Partial Differential Equations. The HHL algorithm mainly consists of four subprocesses. As shown in Figure 4, the first step is the phase estimation marked by the dotted line in the figure; the second step is controlled R, that is, controlled rotation operation in the middle of the line; the third step is the inverse operation of phase estimation, and the fourth step is quantum measurement. It is firmly believed that with the slow emergence of artificial intelligence out of the small terminal and the stand-alone version of the service mode, it will eventually stimulate the quantum computing sales market, generate a large number of requirements, and open up a broader development prospect [15].

Step 1. Establish the first part of the quantum line corresponding to the phase estimation operation to assist in the decomposition of the initial state of the qubit (corresponding to the uppermost timeline in Figure 2), the initial state of the first qubit (corresponding to the timeline in Figure 2), and the initial state of the second qubit (corresponding to the lower timeline in Figure 2). Wherein the cell matrix U corresponding to the aforementioned matrix A is decomposed into a cell matrix corresponding to a single quantum logic gate carrying controlled information. Among them, the cell matrix corresponding to the single quantum logic gate that satisfies the controlled information is the order unit matrix [16]. The number of first qubits z depends on the accuracy of the phase estimation and the probability of success. The number of second qubits is n, which is the eigenvector of matrix A with amplitude of matrix A.

Step 2. Build the second part of the quantum line corresponding to the controlled rotation operation to extract the value in the ground state onto the quantum state amplitude of the auxiliary quantum bit, and obtain: where the number of auxiliary quantum bits is 1 and C is constant. For example, for four-dimensional vector $b = [b0, b1, b2, b3]$, $N = 4$, you can get $n = 2$.

Then encode the data of vector b onto the amplitude of the quantum state to obtain [1]. Thus, load the data of the vector b onto the quantum state amplitude of two second quantum bits in the quantum line.

Step 3. Build the third part of the quantum circuit corresponding to the phase estimation inverse operation to eliminate $|\lambda_j\rangle$ and obtain

$$\sum_{j=0}^{N-1} \beta_j |0\rangle |\mu_j\rangle \left(\sqrt{1 - \left|\frac{C}{\lambda_j}\right|^2} |0\rangle + \frac{C}{\lambda_j} |1\rangle \right). \tag{9}$$

The inverse operation of phase estimation is the reduction process of phase estimation described above, that is, the transposed conjugate operation of phase estimation. The goal is to eliminate, specifically converting the quantum state as

$$\sum_{j=0}^{N-1} \beta_j |0\rangle |\mu_j\rangle \left(\sqrt{1 - \left|\frac{C}{\lambda_j}\right|^2} |0\rangle + \frac{C}{\lambda_j} |1\rangle \right). \tag{10}$$

Step 4. To construct a quantum measurement operation for the auxiliary qubit so that the quantum state of the auxiliary qubit can be measured, get

$$|x'\rangle = \frac{1}{\sqrt{\sum_{j=0}^{N-1} C^2 |\beta_j|^2 / |\lambda_j|^2}} \sum_{j=0}^{N-1} \frac{C\beta_j}{\lambda_j} |\mu_j\rangle, \tag{11}$$

$|x'\rangle$与$|x\rangle = A^1|b\rangle = \sum_{j=0}^{N-1} \beta_j \lambda_j{}^{-1} |\mu_j\rangle$, is the corresponding relation of amplitude normalization. After the measurement, the state of the auxiliary qubit collapses to a definite state, one of them, Collapse to$|0\rangle$ is the probability for $1 - |C/\lambda_j|^2$, Collapse to$|1\rangle$ is the probability for $|C/\lambda_j|^2$. When the quantum state of the auxiliary qubit is measured for $|1\rangle$, and when $C = 1$, you can get a definite quantum state:

$$|x'\rangle = \frac{1}{\sqrt{\sum_{j=0}^{N-1} |\beta_j|^2 / |\lambda_j|^2}} \sum_{j=0}^{N-1} \frac{\beta_j}{\lambda_j} |\mu_j\rangle. \tag{12}$$

This shows $|x\rangle = A^{-1}|b\rangle = \sum_{j=0}^{N-1} \beta_j \lambda_j{}^{-1} |\mu_j\rangle$, the corresponding results of amplitude normalization are carried out.

The first part of the quantum line, the second part of the quantum line, the third part of the quantum line and the quantum measurement operation are in turn formed into the quantum line corresponding to the HHL algorithm.

3.2. Quantum Line Construction Law Corresponding to HHL Algorithm. The application of artificial intelligence technology in the Internet of Things is bound to bring more changes to the Internet of Things. In order to facilitate the integration of these changes, it is necessary to actively find the best nodes for the scientific research of artificial intelligence technology and Internet of Things technology [17]. The first strategy to improve the whole process of classical optimization is to take the optimization parameters of small systems as the original parameters of large systems. Table 1 proposes the strategy flow of the qubit recursion algorithm.

3.2.1. The Matrix Structure Corresponding to the First Column of the Unitary Matrix of the Quantum Circuit

(1) One-Bit Quantum Circuit. The line unitary matrix has only one element (2, 1) to be set to 0, just construct a specific quantum logic gate $\{C_1\} = \{V\}$ to make $\{V\} \bullet U = I_N$;

(2) Two-Bit Quantum Circuit. Using recursive thinking [18]. That is, the recursion or function (or procedure or program segment) calls directly (or indirectly) on the implementation of its own procedure. Recursion to define endless object

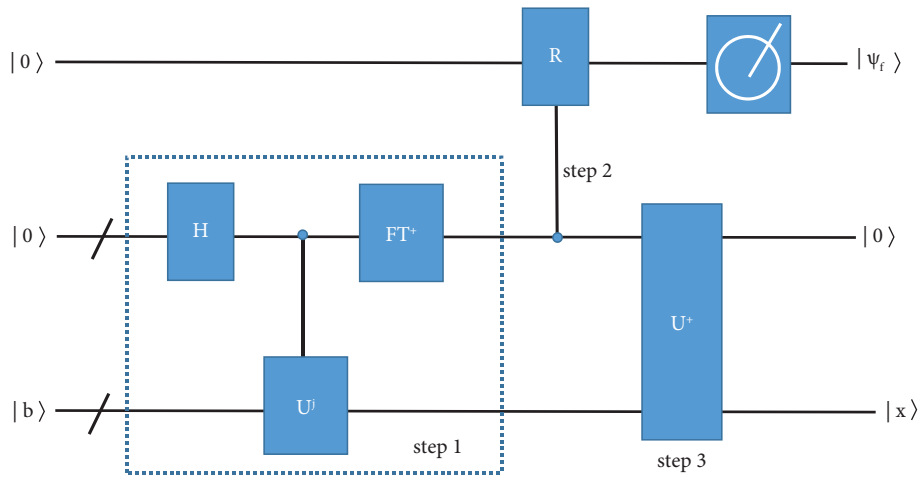

Figure 4: Quantum circuit diagram constructed by the HHL algorithm.

Table 1: Qubit recursion algorithm strategy flow.

Date: system size N, number of target circuit layers M
(1) Initial parameters ⟵ system size $N/2$ tained parameters
(2) **While** fidelity at training convergence < threshold **do**
(3) **If** the number of layers of the current circuit < the number of layers of the target circuit M_{VQE} **then**
(4) Parameters⟵last layer of parameters
(5) **End**
(6) Train the variational circuit until the classical optimization process converges, convergence fidelity F is obtained
(7) $M_{VQE} \longleftarrow M_{VQE} + 1$
(8) **End**

union with a relatively limited sentence. The recursion is characterized by the call itself. Referring to the 1 bit quantum circuit, the unitary matrix of the circuit, except for the last to-be-set 0 element (3, 1), corresponds to the specific quantum logic gate $\{C_n \cdots C_m \cdots C_1\} = \{C_2 C_1\} = \{C_2 V\}$;

For the upper part (2, 1) of the unitary matrix, the most significant qubit is set to be uncontrolled, that is, (2, 1): $\{C_2 V\} = *V\}$; for the lower part (4, 1), determine whether the lower qubit corresponds to 1, if it is not 1, then (4, 1): $\{C_2 V\} = \{1V\}$:, otherwise $\{C_2 V\} = \{*V\}$; the judgment can be: (4, 1) corresponds to (2, 1) of 1 bit quantum circuit: $\{C_2 C_1\} = \{C_2 V\} = \{1V\}$;

The last to-be-placed 0 element (3, 1) is directly set as: $\{C_2 C_1\} = \{V *\}$.

(3) Three-Bit Quantum Circuit. Recursion is divided into immediate recursion and indirect recursion [19]. When you call yourself in a function (or procedure), it's called immediate recursion. If function a calls function b, and function b calls function a, this is called indirect recursion.

Corresponding to the constructed specific quantum logic gate $\{C_n \cdots C_m \cdots C_1\} = \{C_3 C_2 C_1\}$, the upper half of the circuit unitary matrix refers to the 2 bit quantum circuit, and the highest qubit is still set as uncontrolled, that is, $\{C_3 C_2 C_1\} = \{* C_2 C_1\}$, we can get: (2, 1) corresponds to (2, 1) of 2 bit quantum circuit: $\{C_3 C_2 C_1\} = \{* C_2 C_1\} = \{* * V\}$; (4, 1) corresponds to (4, 1) of 2 bit quantum circuit: $\{C_3 C_2 C_1\} = \{* C_2 C_1\} = \{* 1V\}$; (3, 1) corresponds to (3, 1) of 2 bit quantum circuit: $\{C_3 C_2 C_1\} = \{* C_2 C_1\} = \{* V *\}$.

For the lower half, except for the last 0 element (5, 1) to be set, it corresponds to the upper half in order one-to-one, and judges whether the upper two qubits corresponding to the lower two qubits are not 1, if they are both If it is not 1, then $\{C_3 C_2 C_1\} = \{1 C_2 C_1\}$, otherwise $\{C_3 C_2 C_1\} = \{* C_2 C_1\}$; the judgment can be:

(6, 1) corresponding to $\{C_3 C_2 C_1\}$, and (2, 1) corresponding to, the same, that is *, V, and none of them are 1, we can get: $\{C_3 C_2 C_1\} = \{C_3 * V\} = \{1 * V\}$.

Similarly, (8, 1) corresponds to (4,1): $\{C_3 C_2 C_1\} = \{C_3 1V\} = \{* 1V\}$; (7, 1) corresponds to (3, 1): $\{C_3 C_2 C_1\} = \{C_3 V *\} = \{1V *\}$.

The last to-be-placed 0 element (5, 1) is directly set as: $\{C_3 C_2 C_1\} = \{V * *\}$.

By analogy, the matrix structure corresponding to the first column of the unitary matrix of any bit quantum circuit can be realized.

3.2.2. The Matrix Structure Corresponding to the Second Column to the N/2th Column of the Unitary Matrix of the Quantum Circuit. (1) Two-Bit Quantum Circuit, $n = 2$. The second column, column subscript $l = 2$, binary representation 01, binary low bit $l_1 = 1$, high bit $l_2 = 0$; according to the preset inequality $2^{x-1} < l \leq 2^x$, obtain $x = 1$; The bottom half corresponds to the bottom half of the previous column

in order, (3, 2): $\{C_2C_1\} = \{1V\}$; (4, 2): It is the last element to be set to 0 in this column, refer to the corresponding $\{V*\}$ in the first column (3,1): treat * in $\{V*\}$ as 0, perform binary plus 1 operation, * becomes 1, Get $\{C_2C_1\} = \{V1\}$ corresponding to (3, 2).

(2) Three-Bit Quantum Circuit, $n = 3$. The second column, column subscript $l = 2$, binary representation 01, $l_1 = 1, l_2 = 0$; according to $2^{x-1} < l \le 2^x$, get $x = 1$, the upper part (3, 2), (4, 2) refers to the two-bit quantum circuit:

In the $\{C_3C_2C_1\}$ corresponding to (3, 2), the value of C_2C_1 is the same as the $\{C_2C_1\} = \{1V\}$ corresponding to (3, 2) of the two-bit quantum circuit, and C_3 is set to *, that is: $\{C_3C_2C_1\} = \{*1V\}$ corresponding to (3, 2); In the $\{C_3C_2C_1\}$ corresponding to (4, 2), the value of C_2C_1 is the same as the $\{C_2C_1\} = \{V1\}$ corresponding to (4, 2) of the two-bit quantum circuit, and C_3 is set to *, that is: $\{C_3C_2C_1\} = \{*V1\}$ corresponding to (3, 2); The lower part corresponds to the lower part of the first column in order. The matrix $\{C_3C_2C_1\}$ is constructed as follows:

(5, 2) Corresponding $\{C_3C_2C_1\} = \{1 * V\}$;

(6, 2) Corresponding $\{C_3C_2C_1\} = \{V * 1\}$;

(7, 2) Corresponding $\{C_3C_2C_1\} = \{*1V\}$;

(8, 2) Corresponding $\{C_3C_2C_1\} = \{1V*\}$;

The same can be obtained, the third column:

The upper part: (4, 3) corresponds to $\{*1V\}$; the lower part: (8, 3) corresponds to $\{1 * V\}$, (6, 3) corresponds to $\{10V\}$, (5, 3) corresponds to $\{1V*\}$; the last element in this column to be set to 0 (7, 3) Corresponding to $\{V1*\}$;

The fourth column will not be repeated; it can be seen that in the lower half, except for the last element to be set to 0 in each column, the even-numbered column corresponds to the matrix structure of the previous column (odd-numbered column), and the matrix of the odd-numbered column is determined by referring to the first column.

3.2.3. The Matrix Structure Corresponding to the (N/2 + 1)th Column to the Last Column of the Quantum Circuit Unitary Matrix. Refer to the first half of the column 1 to the upper half of the N/2th column, in the order of one-to-one correspondence, change the most significant * to 1, and the rest remain unchanged. Taking the above 3 bit quantum circuit as an example, we can get:

Column 5: $\{1V*\}$;

Column 6: $\{1V1\}$;

Column 7: $\{11V\}$;

No in column 8.

By analogy, the matrix structure corresponding to all the columns of the unitary matrix of any bit quantum circuit can be realized. Specifically, $\{C_n \cdots C_m \cdots C_1\} = I_N + V_n \otimes \cdots V_m \cdots \otimes V_1$, where V_m is equal to: $|0\langle 0|$, if $C_m = 0$; $|1\langle 1|$, if $C_m = 1$; $V - \mathrm{I}_2$, if $C_m = V$; I_2, if C_m is *.

3.3. Simulated Test. The use of power circuit model simulation quantum computer to complete quantum information computing data visualization is an intricate subject of research in computer technology system, which mainly includes interdisciplinary theories and technologies.

The simulation experimental quantum Bolyea transform line is shown in Figure 5, and Table 2 showed the simulation experimental results.

As can be seen from Table 2, both the variation of running time and n cause a consequent increase in the length of the quantum line. As can be seen from the quantum circuit construction law corresponding to HHL algorithm, the computational simulation schematic of HHL algorithm corresponding to quantum circuit is shown in Figure 6, and the quantum circuit sequencing application based on HHL quantum algorithm.

According to the high-speed development of traditional type CMOS process integrated circuit chip has faced shortage, new type of nanomaterials and quantum measurement added new technology enhancement. Along with the high speed development of electronic device design automation, fully automated simulation and integrated optimization algorithms for quantum steganography and quantum metacellular automata suffer from the specific scientific research of intelligent computing methods [20].

To test based on corresponding HHL algorithm and application effect of quantum circuit processing application problems, we use the original quantum cloud platform to implement the HHL algorithm, the parameters of the model were first set, 2 bits HHL algorithm, for example, need two quantum bits and a classic register to hold a measured value, the programming interface, as shown in Figure 7, Parameter configuration is shown in Figure 8. Add relevant quantum logic gate on the main programming interface.

As shown in Figure 9, a simple 2 bit HHL algorithm is implemented on the cloud platform. So this is a bar graph that shows the different measurements on the horizontal axis, and the vertical axis shows the probability that the pair of measurements should be, and here we have a 1, which is 100%, which is what we expected.

3.4. Quantum Artificial Intelligence. In addition, at the present stage, the technical manufacturing process is still far from being able to achieve the mass production and operation of traditional computers at room temperature, which indirectly limits the commercial use of subcomputers. In this environment, the native quantum has developed a cloud computing service based on subcomputing-quantum cloud service platform, which can provide online computing the daily tasks for users and major enterprises and research institutions [21]. The user can submit daily tasks to the quantum technology computer deployed at a remote location through the quantum cloud service platform via the scheduling web server and the Internet, and the subcomputer will then return the results to the user via the scheduling web server and the Internet after such tasks are processed and completed. Figure 10 shows the flow chart of quantum computing.

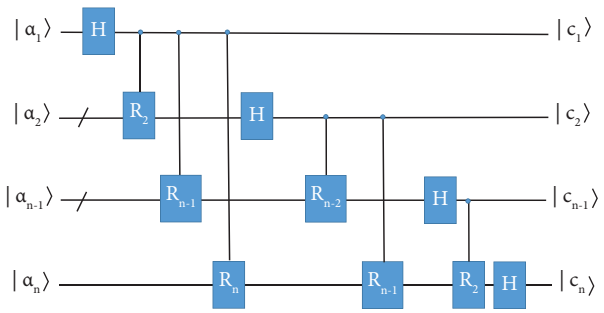

Figure 5: n-quantum bit QFT circuit logic diagram.

Table 2: Simulation experiments.

Quantum bits	13	14	15	16	17	18	19	20	21
Minute(s)	1	3	7	16	34	89	197	435	918

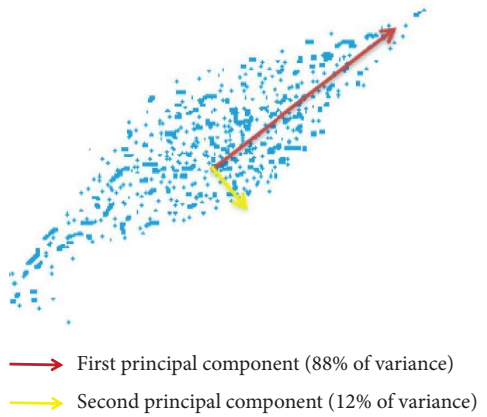

Figure 6: Simulation diagram of quantum circuit calculation by HHL algorithm.

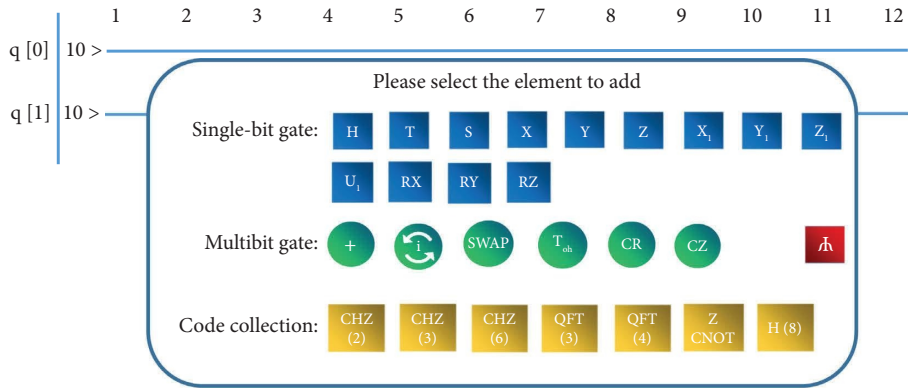

Figure 7: Programming interface of the original quantum cloud platform.

The development and design of artificial intelligence algorithms for the rapid development of artificial intelligence is particularly important, which requires quantum physicists and artificial intelligence researchers, computer experts and scientists to work closely together to generate services to support and hope for the rapid development of artificial intelligence.

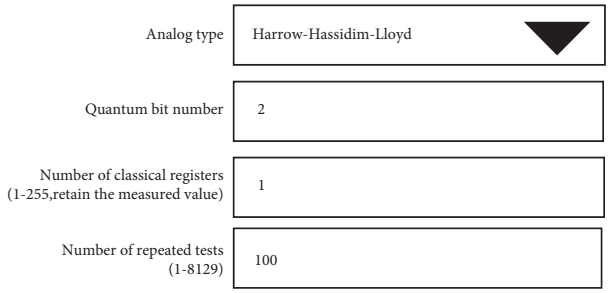

Figure 8: Configuration parameters.

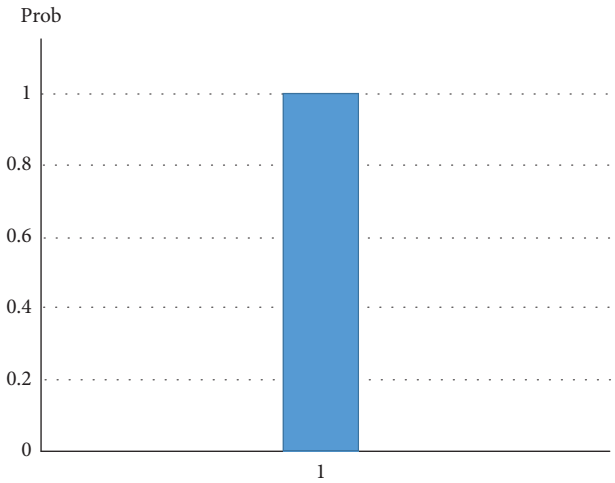

Figure 9: Analysis results of HHL algorithm.

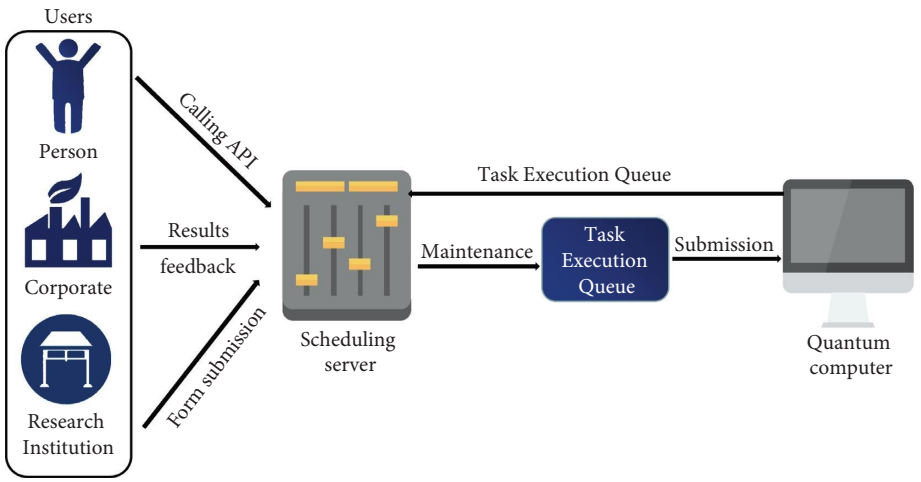

Figure 10: Quantum computing flowchart.

4. Conclusion

Internet technology represents the necessity to analyze and solve massive amounts of information in real time, and the integration of industrial IoT and artificial intelligence is a key development.

Quantum lines include quantum logic gate operations, and the HHL algorithm has become one of the important quantum algorithms. In this paper, a model based on HHL algorithm corresponding quantum lines processing quantum application problems is constructed: by obtaining the target partial differential equation corresponding to the objective quantum application problem, a linear system is obtained by discretizing the target partial differential equation. The numerical solution of the partial differential equation of the target is obtained by solving the linear system using a quantum line based on the corresponding HHL algorithm.

Finally, by analyzing the law of the unitary matrix construction of the quantum line corresponding to the HHL algorithm and experimental measurement data, it is possible to reduce the computational workload of quantum lines corresponding to the HHL algorithm in the process of processing quantum computer applications based on quantum lines, improve the simulation efficiency of quantum lines, at the same time reducing hardware resources. Occupy, has certain validity and superiority. Quantum computing has an exciting future, but reaching this market prospect has many more tests to come. Along with increased awareness comes increased ability to manipulate quantum computing. There is also a lot to be done to produce and manufacture a good working quantum computer. It is difficult to predict and analyze how the future development of quantum computing should trend at what rate. At present, origin quantum has developed a quantum sorting application based on the HHL quantum algorithm, which will provide an important reference for predicting the next spreading point of a novel Coronavirus. The next trend in intelligent IoT technology is to share traditional data in an intelligent app that can be done with the help of artificial intelligence technology. In general, the next few decades will undoubtedly be the era of quantum computing and artificial intelligence, whose research is not only exciting but also full of tests.

Data Availability

The labeled dataset used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest.

Acknowledgments

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Research Article

Design of Intelligent Parking Management System Based on ARM and Wireless Sensor Network

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Motor vehicles are changing the way people live, but they are also putting a huge strain on urban traffic. In the majority of major cities, parking has become the number one problem for car owners to get around. The management efficiency of car parks directly affects the traffic of the whole city. In order to improve the management efficiency of the car park, this paper designs an intelligent parking management system based on ARM and ZigBee wireless sensor network. Firstly, according to the internal environment and economic cost of the car park, ultrasonic sensors are used to monitor whether the parking space is empty or not. The information collected by the ultrasonic sensors is transmitted to the ARM host controller through the ZigBee wireless sensor network, and the ARM host controller determines whether there are free parking spaces based on the collected information. Secondly, Faster R-CNN, a deep learning algorithm, is selected as the license plate recognition model, and the Faster R-CNNN is improved by the residual module. Finally, in order to extend the lifetime of the ZigBee wireless network, the ZigBee routing algorithm is investigated, and an improved routing algorithm based on energy averaging is proposed. The effectiveness of the improved routing algorithm is demonstrated by a simulation analysis through NS2. The test results show that the designed intelligent parking management system is able to complete the functions of parking space detection and license plate recognition normally, thus effectively improving the efficiency of the car park and providing great convenience to motorists.

1. Introduction

With the continuous development of economy and science and technology, people's quality of life has been continuously improved, which is most intuitively reflected in the number of motor vehicles. In 2009, China surpassed the United States and thus became the world's number one country in terms of automobile production and sales [1, 2]. Private cars have now become an important part of consumption in the automotive industry [3, 4]. By the end of June 2021, the number of motor vehicles in China reached 390 million, as shown in Figure 1. The dramatic growth in the number of cars has not only brought convenience to people's travel but also brought various problems to individuals as well as society [5, 6].

At present, the rate of construction of parking infrastructure is much slower than the growth in motor vehicle ownership, resulting in a huge problem in the supply of parking spaces. The parking problem has become the number one problem for car owners when people are travelling by car. The ratio of the number of motor vehicles to the number of parking spaces in large cities is about 1 : 0.8 [7, 8]. In most cities, people need to spend a lot of time searching for a vacant parking space, which not only wastes time but also tends to lead to traffic congestion in the surrounding area. As there is no way to obtain accurate information about available parking spaces in a car park in advance, car owners need to blindly search for available spaces with the naked eye when they arrive on-site [9, 10]. However, the topography of many underground car parks is

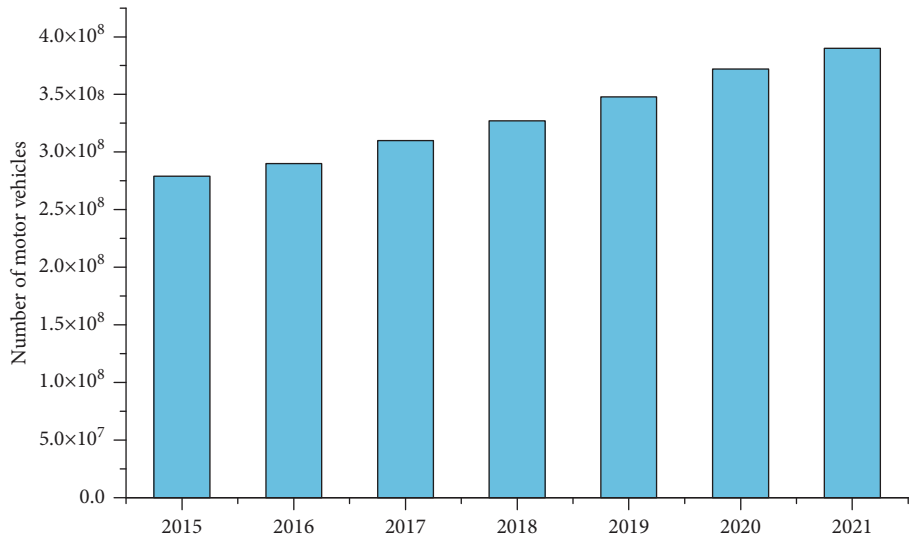

Figure 1: Number of motor vehicles in China.

more complex, and the view inside the car park is not open enough, making it difficult for car owners to find a free space in time. This situation will not only cause confusion inside the car park but also increase the difficulty and cost of car park management.

Both the number of parking spaces and the efficiency of car parks affect the efficiency of the overall transport system [11, 12]. In order to solve the problem of insufficient parking spaces, the government has started to build new parking infrastructure, but it still cannot meet the demand for parking and requires a large amount of financial expenditure. Researchers have tried to use science and technology instead of traditional labour to make parking systems more user-friendly in order to fundamentally improve the efficiency of parking management [13, 14]. Using the latest artificial intelligence and Internet of Things technologies to retrofit car parks, it is possible to share all parking space information on the web, thus making it easier for users to make enquiries.

At present, the application of artificial intelligence technology in vehicle identification has received extensive attention [15]. For example, Geng and Cassandras [16] proposed a vehicle recognition technique based on a BP neural network, which is capable of automatically obtaining license plate information through surveillance video. With the rapid development in the field of deep learning, target recognition using deep learning techniques has achieved satisfactory working results [17–24]. Various deep learning-based target recognition applications are increasingly available in the security, military, and human-computer interaction fields. However, deep learning requires a large amount of computational power to support and therefore requires high performance of the algorithm processing equipment. As a result, most deep learning applications are currently networked, meaning that the images captured by the camera are transmitted to a cloud server via the network, and the results are returned to the underlying device after the algorithm has been processed. This underlying device is called an "edge device" [25–28].

However, this target recognition system based on the networking method requires a high transmission bandwidth and a large transmission delay and therefore cannot achieve a real-time response. The intelligent parking management system places very stringent requirements on the response latency of target recognition. In addition, the network transmission of image data can easily be intercepted by hackers, leading to user privacy leakage or security risks. In recent years, as large data centres have grown in size, their heat dissipation and security issues have become more prominent. As a result, localised offline working methods are gaining attention, and "edge computing" has become the main tool for offline target recognition [29, 30]. For example, Wang et al. [31] proposed an improved convolutional neural network model that has been successfully applied to a variety of edge computing devices, and the ARM family of processors is well suited for edge computing devices due to its powerful computing capabilities.

Compared with other wireless communication methods, wireless sensor networks have become the mainstream technology for various IoT systems with their advantages of low power consumption, low cost, and high quality [32–37]. Wireless sensor networks were born in the late 1990s as a special kind of ad hoc network. A wireless sensor network consists of many sensor nodes. These nodes have functions such as information collection, data processing, wireless communication, and cooperation. These nodes can be randomly or specifically arranged in the area of the monitored environment. All nodes are self-organised through specific protocols and have superb adaptive capabilities. Wireless sensor networks have a very wide range of application prospects and can be used in industrial control, environmental monitoring, intelligent monitoring, and other fields. Currently, the IEEE 802.15.4 (ZigBee) standard is the mainstream technology for wireless sensor networks. ZigBee's self-organising function and wireless transmission function are very suitable for intelligent parking management systems. This study considers ZigBee technology to be a low-cost, low-rate wireless interconnection standard

currently applicable to intelligent parking management systems.

The aim of this research is therefore to design an intelligent parking management system based on ARM and ZigBee wireless sensor network, thus reducing the time taken by users to find parking spaces (increasing the utilisation of parking spaces). In this paper, the Linux embedded operating system was built and ported to the ARM host controller. A ZigBee wireless sensor network was constructed, and a routing improvement algorithm based on energy balancing was proposed. The designed system implements two main functions: (1) parking space detection and (2) license plate recognition. Parking space detection: according to the internal environment of the car park and the economic cost, this paper uses ultrasonic sensors to monitor whether the parking space is empty or not. The information collected by the ultrasonic sensor is transmitted to the ARM main controller via a ZigBee wireless sensor network. License plate recognition: with the help of a computing stick and the ARM host controller, this paper uses deep learning algorithms to process the video captured by the surveillance cameras in the car park in real time and then uses OpenCV tools to carry out plate recognition in order to determine the parking time of each vehicle, thus enabling localised offline computing (without the need for a host computer or cloud platform).

The main innovations and contributions of this paper include the following:

(1) By comparing various deep learning algorithms, Faster R-CNN was found to have higher accuracy. Therefore, Faster R-CNN was selected as the license plate recognition model, but its high computation and transmission costs cannot be effectively used in edge computing devices. Therefore, in this paper, the Faster R-CNN is improved by the residual module.

(2) In order to extend the lifetime of the ZigBee wireless network, the ZigBee routing algorithm was studied, and an improved routing algorithm based on energy averaging was proposed. Simulation analysis was carried out by NS2 to prove the effectiveness of the improved routing algorithm.

The rest of the paper is organised as follows: In Section 2, the overall system design was studied in detail, while Section 3 provides the license plate recognition model based on deep learning. In Section 4, the ZigBee networking was studied in detail, while Section 5 provides the experimental results and analysis. Finally, the paper is concluded in Section 6.

2. Overall System Design

2.1. General Structure of the System. According to the function of the smart car park and the characteristics of ZigBee technology, the smart car park management system designed in this paper uses the ARM processor OMAP3530 as the main controller. The network transmission part of the system consists of a coordinator node, multiple router nodes, and multiple sensor data collection nodes. The overall structure of the system is shown in Figure 2.

At the entrances and exits of the car park, stop bars and surveillance cameras are placed to control the entry and exit of vehicles. When the vehicle arrives at the entrance, the system identifies the vehicle number and records the corresponding time and plate number. At the same time, the ARM controls the stop bar and releases the vehicle. License plate recognition can improve the efficiency of vehicles passing through entrances and exits. License plate recognition technology is currently used in many car parks. Each parking space detector is connected to a ZigBee node. The data detected by the car space detector is sent from the end node to the ARM main control module via a router. The coordinator does not need to add a parking space detection module.

2.2. Workflow of the Parking Management System. The user can observe the display at the entrance to the car park. If a space is available in the car park, the system displays the serial number and location of the available space. The user then drives the vehicle into the car park. At this point, the camera recognises the number plate and records the relevant data. If there is no space available in the car park, no space is displayed. When the user drives the vehicle to the exit of the car park, the camera recognises the number plate. The system charges the user a fee based on the rate and parking time. After the user has paid the fee, the system raises the stop bar and releases the vehicle. The workflow is shown in Figure 3.

2.3. Design of the Hardware System. The OMAP3530-Mini was chosen as the main controller platform for this system. The OMAP3530 is the latest generation of high-performance ARM processors from TI. The OMAP3530 uses the advanced Cortex A8 architecture and is capable of reaching a main frequency of over 1 GHz. The ARM main controller module uses the OMAP3530 processor as the core and contains modules such as LCD, DDR2, Nand Flash, and ZigBee wireless communication module. The structure of the ARM main controller module is shown in Figure 4.

The wireless communication module consists of a ZigBee wireless sensor network. The ZigBee coordinator node is connected to the ARM host controller module via the RS 232 serial port. The ZigBee coordinator node is responsible for data forwarding between the two modules. The ZigBee node consists of the CC2430 core processor, wireless transceiver module, sensors, I/O interface circuit, and power supply module. The structure is shown in Figure 5.

The core CC2430 processor is responsible for controlling the logic, routing protocols, synchronous positioning, power management, and task management of the entire node. The sensors are responsible for collecting the temperature in the designated monitoring area and completing the data conversion. The wireless transceiver module is responsible for wireless communication with other nodes. The power supply module provides energy for the operation of each module in the node. The wireless transceiver chip used is the Chipcon CC2430, which has a high-performance 2.4 GHz DSSS RF transceiver and an 8051 controller (MCU) inside the

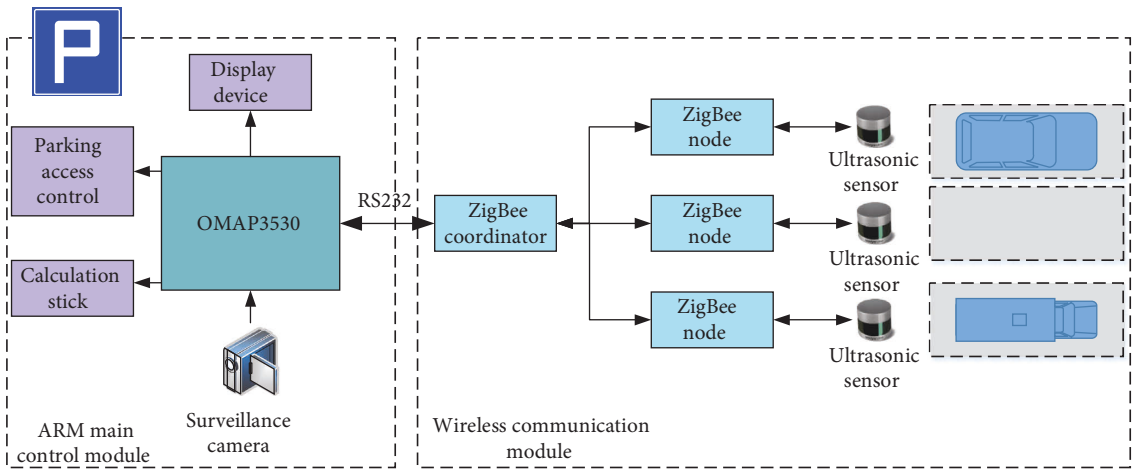

Figure 2: General system architecture.

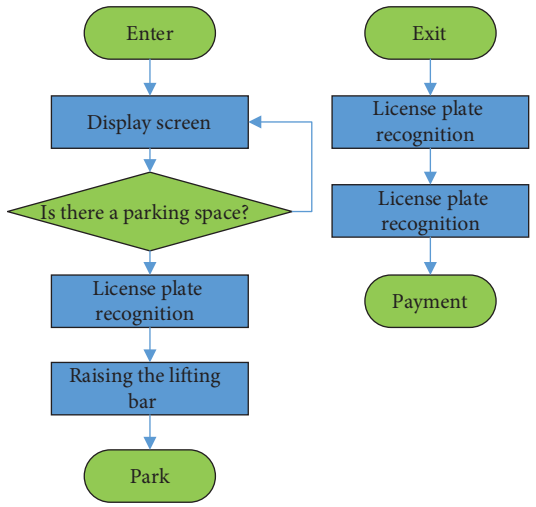

Figure 3: Workflow of the car park management system.

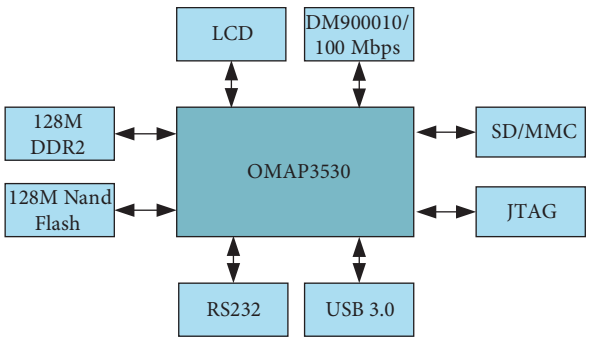

Figure 4: Structure of the ARM host controller module.

CC2430. The main performance parameters of CC2430 are shown in Table 1.

The OMAP3530 and CC2430 require a voltage of 3.3 V, and the other peripheral voltages require 5 V, 3.3 V, and 1.5 V inputs, respectively. Therefore, a DC 5 V switching power supply needs to be converted. The MAX687 is a low-noise linear voltage regulator. The MAX687 will

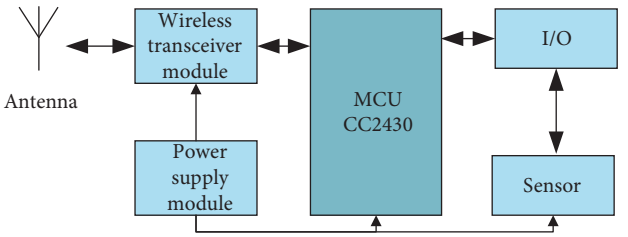

Figure 5: Structure of the ZigBee node.

automatically cut off the output voltage when the output voltage falls below 2.96 V. With an output current of up to 1 A, the MAX687 can fully meet the power supply requirements of the OMAP3530 module.

As the level of the standard RS-232 is different from the signal level of the TTL circuit, the MAX32323 chip was used for level conversion. The pin connections between the OMAP3530 and MAX3232 are shown in Table 2.

2.4. Ultrasonic Sensor-Based Parking Space Detection. In an intelligent parking system, it is necessary to detect parking space information and determine whether there are any vehicles in the parking space. This function is the key part of the whole system. At present, the actual common detection technologies are geomagnetic detection technology, infrared detection technology, video image processing detection technology, ultrasonic detection technology, and so on. Ultrasonic sensors have the advantages of low cost, simple maintenance, strong anti-interference ability, and high measurement accuracy; therefore, this paper uses ultrasonic detection technology for real-time detection of car parking status in the car park. As the ultrasonic sensor is affected by the temperature, temperature compensation measures can be taken.

The ultrasonic distance measuring principle used in the intelligent parking system is shown in Figure 6. T indicates the ultrasonic transmitting device, R indicates the ultrasonic receiving device, D indicates the distance of the ultrasonic device from the ground, and H indicates the distance of the

Table 1: CC2430 main performance parameters.

Parameters	Performance indicators
Size	7 mm × 7 mm
Operating voltage	2.0 V–3.6 V
Operating frequency	2400 MHz–2483.5 MHz
Chip flash	128 K
Chip RAM	8 K
Data transfer rate	≤250 kbps
Communication range	<70 m
Communication protocol standards	IEEE 802.15.4
Modulation method	DSSS
Addressing method	64-bit IEEE address; 8-bit network address
Data encryption	128-bit AES
Error checking	CRC-16/32
Number of channels	16
Interface	21 general purpose I/O pins

Table 2: Pin connections between OMAP3530 and MAX3232.

Pinout of MAX3232	Pinout of OMAP3530
11	PC12
10	PC13
12	PA12
9	PA13

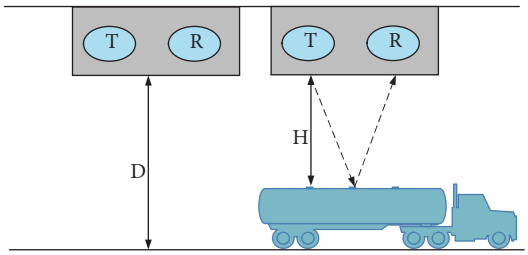

Figure 6: Ultrasonic distance measurement principle.

ultrasonic device from the roof of the car. The model number of the ultrasonic sensor is HC-SR04. The ultrasonic timing is shown in Figure 7.

Ultrasonic sensors calculate distances from the speed of sound and time. Variations in the speed of sound therefore affect the accuracy of the distance measurement. The speed at which ultrasound travels through the air is temperature-dependent. In order to enhance the accuracy of the measurement and the range of application of the system, temperature compensation is considered. Values of the speed of sound at a variety of temperatures are shown in Table 3. The velocity of sound in air as a function of temperature is shown as follows:

$$c = 331.4 \times \sqrt{\frac{1+T}{273}}, \quad (1)$$

where c is the propagation speed of the ultrasound at the current temperature and T is the actual temperature.

As can be seen, temperature has an effect on the speed of sound, and certain measures are required to improve the accuracy of the measurement. Therefore, a temperature compensation module has been added to this paper. The real-time sound velocity is calculated by measuring the current temperature and bringing it into (1). The operating voltage of the temperature sensor DS18B20 is 3.0~5.5 V, and the temperature measurement range is −55~ + 125°C, which can fully meet the system requirements. In this paper, the DS18B20 is chosen to provide temperature compensation for the ultrasonic sensor.

3. Deep Learning-Based License Plate Recognition Model

There are two main categories of deep learning-based recognition algorithms [38, 39]: one-stage algorithms and two-stage algorithms. For the one-stage recognition methods, the You Only Look Once (YOLO) and Single Shot Detector (SSD) are mainly used. For the two-stage algorithms, R-CNN, Fast-RCNN, Faster R-CNN, and Mask R-CNN are mainly used. Through the performance comparison of each algorithm model, it is found that Faster R-CNN in networking mode has higher accuracy [40]. However, its high computational and transmission costs prevent it from being effectively used in edge computing devices.

To address the above issues, the Faster R-CNN model is improved. Firstly, the feature extraction network is clipped by the residual module. Secondly, an adjustable candidate region is designed. By setting the size of the convolution sliding window, the region proposal can be obtained more quickly. Finally, the improved Faster R-CNN model was implemented using an ARM host controller and an Intel neural computing stick (an edge computing device) to obtain better licence plate recognition results.

3.1. Structure of the Model. In order to enable Faster R-CNN to run smoothly on edge computing devices, this paper proposes a new lightweight target recognition model based on the Faster R-CNN algorithm, the overall structure of which is shown in Figure 8.

The improved Faster R-CNN model is divided into three parts: feature extraction, region proposal network, and target recognition. The traditional feature extraction part is

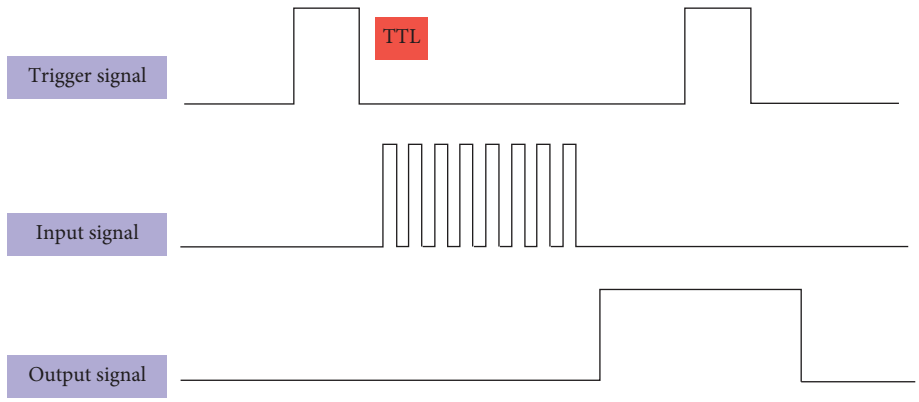

Figure 7: Timing of ultrasound.

Table 3: Velocity of sound in air as a function of temperature.

Temperature (°C)	Speed of sound (m/s)
−20	319
−10	325
O	332
10	338
20	344
30	349

replaced by a residual network. Due to the excessive scale parameters required by the traditional model, an adjustable region proposal network (ARPN) is proposed in this paper. The ARPN assigns respective sliding windows to the three subchannels (corresponding to the three image feature matrices) to obtain anchor at different target scales [41]. The ARPN can obtain the region proposal more quickly.

3.2. The Model's Backbone Network. Darknet53 was selected as the feature extraction part of the improved Faster R-CNN model. Darknet53 combines the advantages of Darknet19 as well as other novel residual networks. The backbone network combines multiple 3×3 convolutional layers and 1×1 convolutional layers. The structure of the backbone network is shown in Table 4.

The proposed model generates three different sets of image feature matrices through the three branches. The convolution kernel extracts shallow features (colour, edges, etc.) at a shallow layer. As the depth of the convolutional layers increases, the model extracts more detailed information. The size of the extracted feature map is inversely proportional to the number of layers.

3.3. Structure of the ARPN. The purpose of the ARPN is to extract a certain number of region proposals from the input image, the structure of which is shown in Figure 9.

The key to generating a high-quality region proposal is to define a reasonable-sized window and anchor for each feature matrix, so a different anchor needs to be assigned to each feature matrix. The specific settings are shown in Table 5.

3.4. Loss Functions. The loss function of the improved Faster R-CNN model is divided into two parts: (1) the ARPN loss function and (2) the target recognition loss function. The ARPN loss function contains both classification loss and regression loss components.

The ARPN loss function is calculated as follows:

$$L(M) = \sum_{n=1}^{3} \sum_{i \in S^n} h_n, \tag{2}$$

where M is the learning parameter of the ARPN network, n represents the number of branches, h_n represents the loss weight of the n-th branch, and S^n is the training sample set of the n-th branch.

The target recognition loss function is calculated as follows:

$$L(M') = \sum_{k=1}^{3} \sum_{i \in S^k} \gamma_k, \tag{3}$$

where $k \in [1, 3]$ represents the k-th branch; γ_k represents the loss weight of the k-th branch; S^k is the training sample set of the k-th branch.

The overall loss function of the improved Faster R-CNN model is calculated as follows:

$$L(M, M') = L(\mathrm{M}) + L(\mathrm{M}'). \tag{4}$$

4. ZigBee Networking

ZigBee nodes in smart parking management systems need to be powered by batteries, so reducing energy consumption is an issue that must be considered in the design of the system; sometimes, a ZigBee node does not need to communicate, but if it is in the communication path between other communicating nodes, the node is still involved in data forwarding and thus consumes energy. In some cases, this problem may also cause network fragmentation or lead to shorter network life cycles. It is therefore essential to investigate and improve the routing of ZigBee networks.

4.1. Principle of ZigBee Routing Algorithm. The routing algorithm primarily provides the best path for the delivery of data. The routing function is implemented in the network

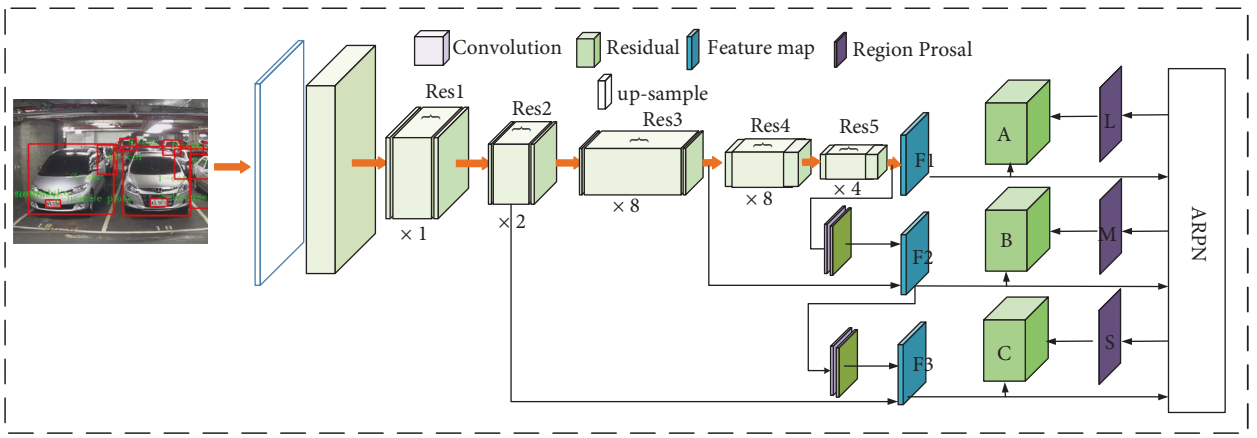

Figure 8: Structure of the improved Faster R-CNN.

Table 4: Structure of the backbone network.

	Type	Size	Filters	Stride
	Convolutional	3 × 3	32	1
	Convolutional	3 × 3	64	2
	Convolutional	1 × 1	32	1
1×	Convolutional	3 × 3	64	1
	Residual	—	—	—
	Convolutional	3 × 3	256	2
	Convolutional	1 × 1	64	1
2×	Convolutional	3 × 3	128	1
	Residual	—	—	—
	Convolutional	3 × 3	256	2
	Convolutional	1 × 1	128	1
8×	Convolutional	3 × 3	256	1
	Residual	—	—	—
	Convolutional	3 × 3	512	2
	Convolutional	1 × 1	256	1
8×	Convolutional	3 × 3	512	1
	Residual	—	—	—
	Convolutional	3 × 3	1024	2
	Convolutional	1 × 1	512	1
4×	Convolutional	3 × 3	1024	1
	Residual	—	—	—

layer. Routing algorithms play a crucial role in routing protocols, and the use of different algorithms often yields different pathfinding results. Currently, three routing algorithms are commonly used for the ZigBee protocol [42]: (1) Cluster-Tree algorithm, (2) AODV algorithm, and (3) AODVjr algorithm.

The Cluster-Tree algorithm uses a tree topology, so the routing process is relatively simple. When there is data to be sent, the next hop node is calculated directly by means of a formula. However, the Cluster-Tree algorithm is generally not used when the number of network nodes is high. This is because of the large time delays in data transmission in a tree structure. Compared to the Cluster-Tree algorithm, the AODV algorithm and the AODVjr algorithm have a much improved network communication rate and effectively avoid the routing loop problem. However, each routing node on the communication link must maintain a routing table. Therefore, how to balance the energy consumption of the whole network is an important research direction for routing algorithms.

4.2. Improvement of ZigBee Routing Algorithm. To address the above problems, this paper proposes an algorithm for energy balancing to achieve the goal of extending the survival cycle of the network. The nodes in the network are classified according to the remaining power. For nodes with sufficient node energy, the normal AODV protocol is used for data transmission. When the remaining power of a router node falls below a threshold value, this router node sends a notification to the child nodes. The child node will look for an auxiliary parent node and establish a communication route with it, thus effectively reducing the communication tasks of the original parent node. An example of the energy shunt is shown in Figure 10.

At the beginning of the ZigBee network, each node has an abundance of energy. The data transfer between nodes 2, 3, and 5 and coordinator 0 passes through node 1. At this point, the energy consumption of node 1 is high. After a certain period of time, the energy of node 1 decreases to a certain threshold. Node 1 notifies nodes 2, 3, and 5. Nodes 2, 3, and 5 each initiate the discovery process for the auxiliary parent node. Node 3 finds the auxiliary parent node 7, while node 5 finds the secondary parent node 6. Through the diversion of these two auxiliary parents, the communication burden on node 1 is greatly reduced. The energy consumption of the entire network tends to be balanced, thus extending the survival cycle of the network.

Let the energy of a node be E and the maximum energy be E_{max}. We classify the residual energy of a node into three classes, as shown in Table 6. Each node is divided into three levels according to its residual energy. When the energy level of a node changes from "A" to "B," the node sends a notification to all its children.

The child node receives notification from the parent node and initiates the auxiliary parent node discovery process. The child node broadcasts a route sending request group RREQ to the neighbouring nodes (in addition to the parent node). After receiving the RREQ, the neighbouring

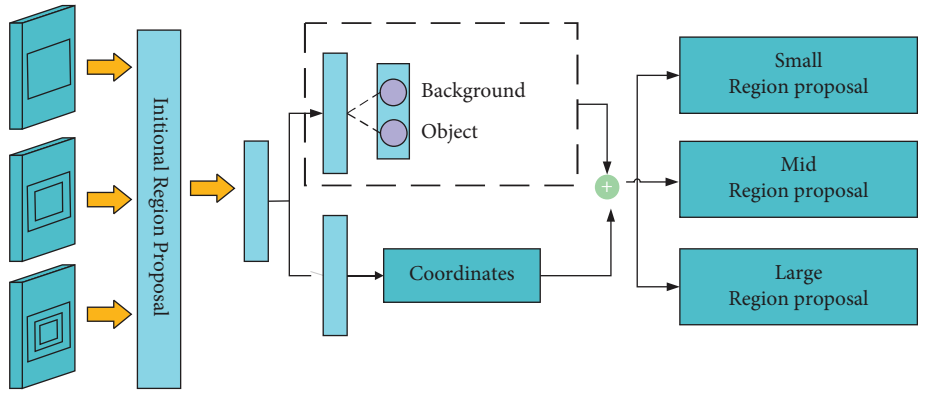

Figure 9: Structure of the ARPN.

Table 5: Specific settings for anchor and windows.

Feature map	Window size	Step length	Anchor	Proportion
F1	5×5	1	200×200	1 : 1, 1 : 2, 2 : 1
	7×7	1	350×350	1 : 1, 1 : 2, 2 : 1
	9×9	1	500×500	1 : 1, 1 : 2, 2 : 1
F2	5×5	1	120×120	1 : 1, 1 : 2, 2 : 1
	7×7	1	150×150	1 : 1, 1 : 2, 2 : 1
F3	7×7	2	60×60	1 : 1

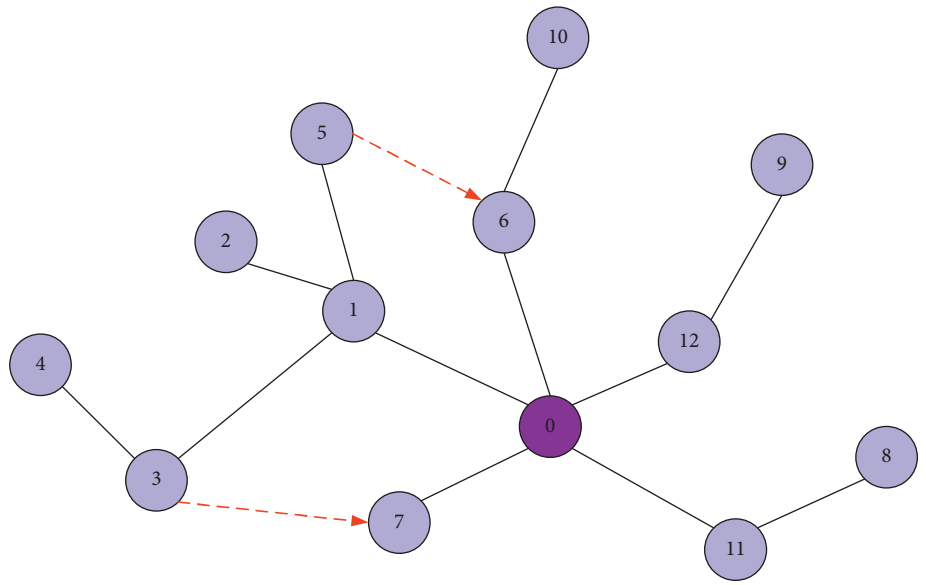

Figure 10: An example of energy diversion.

Table 6: Levels of residual energy for nodes.

$E \geq 50\% \times E_{max}$	$20\% \times E_{max} \leq E \leq 50\% \times E_{max}$	$E \leq 20\% \times E_{max}$
A	B	C

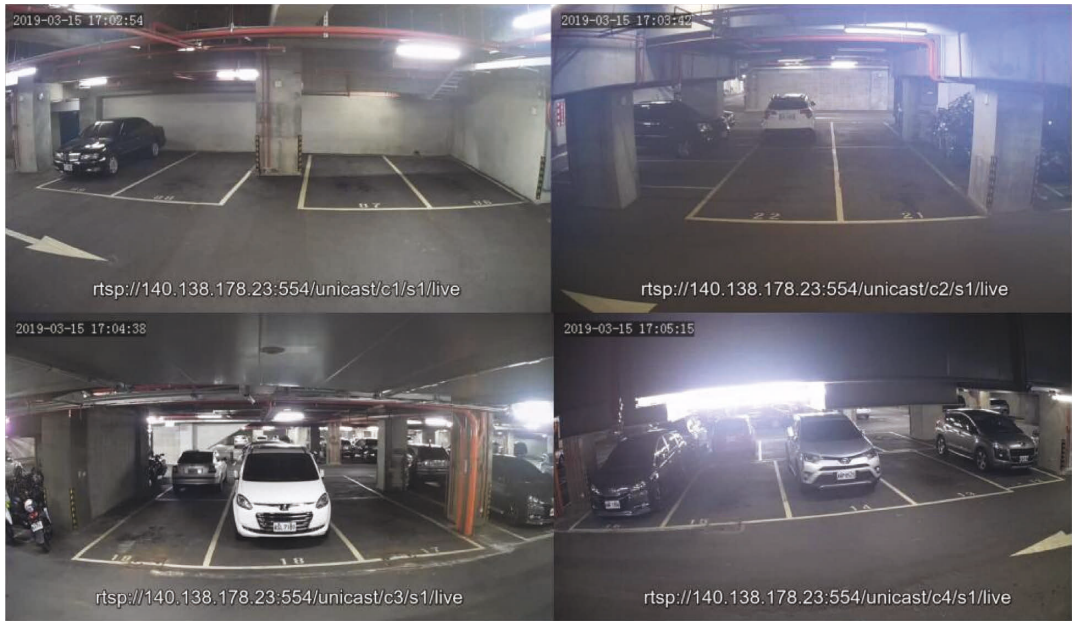

Figure 11: Video footage of the beginning of the car park surveillance.

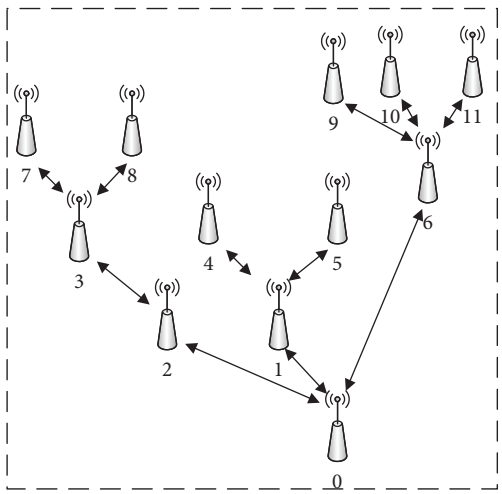

Figure 12: Simulated network scenario.

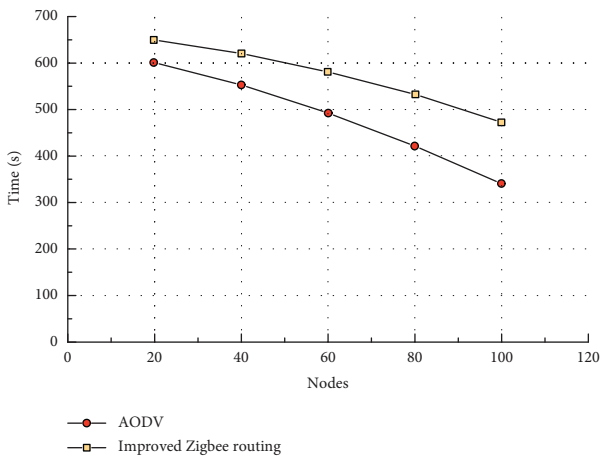

Figure 13: Survival cycle comparison.

router node determines whether it satisfies the network depth and energy level conditions. If it satisfies, it responds to the RREP; otherwise, it discards the RREQ.

Assume that there are n paths from the source node to the destination node. The i-th path has m nodes. E_{ij} indicates the remaining energy of the j-th node on the i-th path. E_1 indicates that the node is in the "A" zone, E_2 indicates that the node is in the "B" zone, and E_3 indicates that the node is in the "C" zone. The minimum residual energy of the node on the i-th path is calculated as follows:

$$E^{i}_{\min} = \min\left\{E_{ij}, 1 \le j \le m\right\}. \tag{5}$$

C_{ij} denotes the energy consumption required by the jth node on the i-th path to send data, and the total energy consumption of the path is calculated as follows:

$$\mathrm{COST}_i = \sum_{j=1}^{m} C_{ij}. \tag{6}$$

5. Experimental Results and Analysis

5.1. Experimental Setup. The designed intelligent parking lot management system was built with hardware such as OMAP3530 processor and Intel neural computing stick. The ARM main controller module has Open CV and NCSDK API installed. The system uses Sony's 8-megapixel RPi camera based on IMX219. The Intel™ neural computing stick is a VPU model with a USB 3.0 interface. Capture the parking lot surveillance video using the cv2 video capture (URL) function. The surveillance video of some cameras in the parking lot is shown in Figure 11.

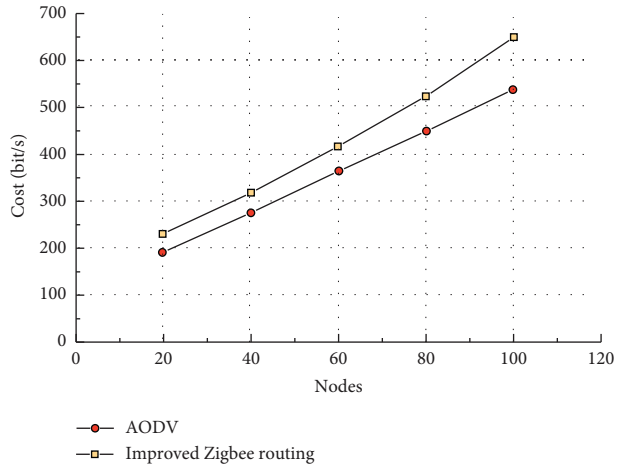

Figure 14: Comparison of routing overheads.

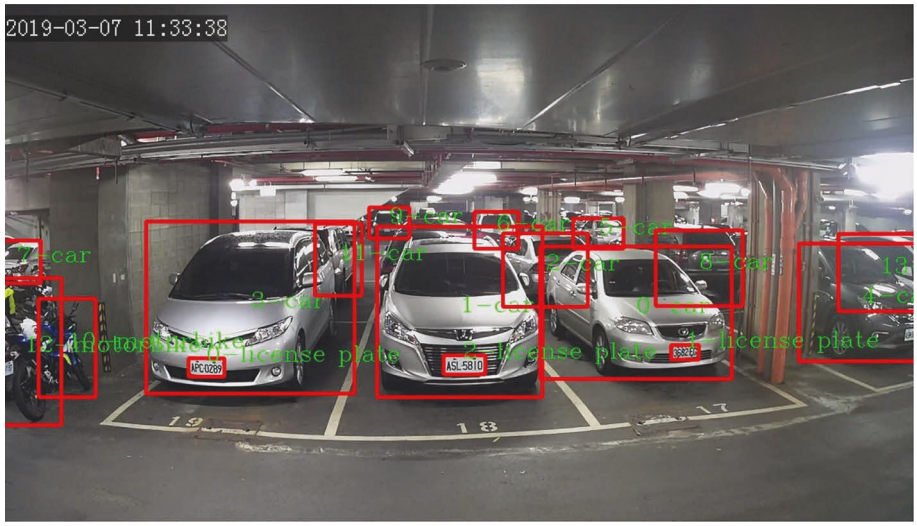

Figure 15: Video test results of licence plate recognition performance.

5.2. Simulation Analysis of Improved ZigBee Routing Algorithm. Firstly, the improved ZigBee routing algorithm is simulated and analysed. The simulation software version is NS-2.32, and the operating system environment is Ubuntu 10.10. A comparison between the AODV algorithm and the improved ZigBee routing algorithm is carried out in this paper. The number of nodes is set to 11, 31, 51, 71, and 91, respectively. Node 0 is the central coordinator node, the simulation area is a square area, the nodes are spaced 10 m apart, and the simulation time is 1000 seconds. Figure 12 shows the simulated network scenario with 11 nodes.

The data source sends packets at a rate of 10 packet/s, and each packet is 100 bytes. The initial energy of the node is 100 J. The node consumes 0.4 J to send a packet and 0.1 J to receive a packet. Based on the simulation data, a comparison of the survival cycles obtained is shown in Figure 13.

It can be seen that, at smaller network sizes, the survival times of the two routing algorithms are not very different. As the network size increases, the survival time of both routing algorithms decreases. The survival time of the AODV algorithm decreases rapidly, while the improved ZigBee routing algorithm decreases relatively slowly. Compared to AODV, the improved ZigBee routing algorithm with an energy balancing mechanism has a significantly higher survival time. This is because the AODV routing algorithm always looks for the shortest path during routing, causing the energy consumption of key nodes in the path to drop too quickly. However, the improved ZigBee routing algorithm was able to effectively reduce the total energy consumption of the network, thus extending the network survival time. A comparison of routing overheads is shown in Figure 14.

It can be seen that the routing overhead of both routing algorithms grows linearly as the network size increases. The improved ZigBee routing algorithm has a slightly higher overhead than the AODV protocol due to the use of energy-controlled packets to adjust the network topology. However, the increased overhead has little impact on the overall

Table 7: Average accuracy rates in the three different difficulties.

Algorithm	Average accuracy rate (%)		
	Easy	Moderate	Hard
R-CNN	30.03	23.84	18.73
Faster R-CNN	85.7	76.91	67.99
Improving Faster R-CNN	84.84	75.19	65.81

Table 8: Comparison of operating speeds.

Evaluation criteria	Faster R-CNN	Improving Faster R-CNN
Single image recognition speed (ms)	83.35849	78.88749
Video detection (FPS)	6.75	7.79

network performance. Although the AODV protocol has lower overhead, the premature failure of its key nodes is difficult to resolve.

5.3. Analysis of Licence Plate Recognition Performance. The video test results of the license plate recognition performance are shown in Figure 15. It can be seen that the improved Faster R-CNN model is able to accurately complete the detection of both close and long-range targets, verifying the strong adaptability to multiple target scales (large and small targets).

To verify the effectiveness of the improved Faster R-CNN model, it was tested against R-CNN and Faster R-CNN. The average accuracies in the three different difficulties are shown in Table 7.

It can be seen that the average accuracy of the improved Faster R-CNN reached 92.84%, 90.19%, and 85.31% in the three different difficulties, respectively. Compared to the original Faster R-CNN, all of them are slightly lower, at 0.86%, 1.72%, and 2.18%, respectively. However, the improved Faster R-CNN after the light weighting process showed a significant improvement in running speed, as shown in Table 8.

It can be seen that the improved Faster R-CNN improves the speed of single image recognition by 4.471 ms and video detection by 1.04 FPS. Collectively, with almost no significant loss in accuracy, the improved Faster R-CNNN effectively improves the speed of license plate recognition with better real-time performance.

6. Conclusion

This paper designs an intelligent car park management system based on ARM and ZigBee wireless sensor network, thus effectively improving the efficiency of the car park. The Linux embedded operating system is built and ported to the ARM host controller. Ultrasonic sensors are used to monitor whether a parking space is empty or not. Localised offline computation was achieved by utilising the Faster R-CNN, a deep learning algorithm, as the licence plate recognition model and using OpenCV tools for licence plate recognition in order to determine the parking time of each vehicle. In addition, the Faster R-CNN was improved with a residual module in order to obtain better real-time performance and security on edge devices. A ZigBee wireless sensor network was constructed, and a routing improvement algorithm based on energy balancing was proposed. ZigBee network simulations and system tests achieved the expected results. Subsequent attempts will be made to use the SSD model for licence plate recognition in order to further improve the accuracy of recognition.

Data Availability

The experimental data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest to report regarding the present study.

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Research Article

Performance Analysis of Synchronous Multilink MAC Protocol with Automatic Repeat Request

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Multilink operation (MLO) is considered a key candidate technique in 802.11be, which allows devices to transmit and receive data using multiple links concurrently, thereby contributing to improving throughput and reducing latency. However, the performance of the MLO scheme will gradually degrade as the channel environment deteriorates. To tackle this problem, in this paper, we propose a synchronous multilink media access control (MAC) protocol with Automatic Repeat Request (called SML-ARQ). With SML-ARQ, in the contention process, MLDs are allowed to perform channel access procedures over multiple links concurrently; in the transmission process, MLDs partition a link packet into multiple blocks and then transmit these blocks using multiple links. Any failed division of a link packet is copied and retransmitted once using multiple channels concurrently; as a consequence, SML-ARQ can mitigate the adverse impact of transmission failure on system performance. A theoretical model is being developed to analyze the performance of the proposed SML-ARQ. Extensive simulations verify the efficiency of SML-ARQ and the accuracy of our theoretical model.

1. Introduction

The wireless local area networking (WLAN) based on the IEEE 802.11 standard, frequently referred to as Wi-Fi, has become a necessity in both business and home environments [1]. According to a report issued by the Wireless Fidelity (Wi-Fi) Alliance [2], more than 9 billion Wi-Fi devices, including smartphones, laptops, tablets, IoT devices, and other devices, are currently in use worldwide. The emergence of new applications (e.g., augmented and virtual reality, video conference, gaming, and cloud computing) is entailing tremendous data traffic transiting over WLAN, demanding tens of gigabit per second data rates and sub 5 ms data transfer latency. To fulfill the peak throughput and stringent latency requirements set by future applications, the Institute of Electrical and Electronics Engineers (IEEE) 802.11 standard organization is going to release a new amendment standard, named IEEE 802.11be Extremely High Throughput (EHT) [3].

According to the 802.11be Project Authorization Request (PAR) approved by the IEEE Standards Board, 802.11be can offer a maximum throughput of at least 30 Gb/s [3] within a frequency range from 1 GHz to 7.25 GHz, while simultaneously improving worst case latency and jitter. For such purposes, 802.11be introduces various candidate significant techniques (such as single-band operation, multilink operation, spatial multiplexing, multiaccess point (multi-AP) coordination, and link adaption) [2, 4–6].

The Multilink Operation (MLO) is one of the most representative main candidate techniques, which allows concurrent data transmission and reception between APs and stations (STAs) using multiple links. The AP/STA device (i.e., a single device with multiple affiliated AP/STAs) that can operate with multiple links is called AP/STA multilink capable devices (MLDs). There are two kinds of transmission modes, namely, asynchronous transmission mode and synchronous transmission mode [7], which can be supported in 802.11be. The former allows an MLD to transmit data frames asynchronously over different links. These

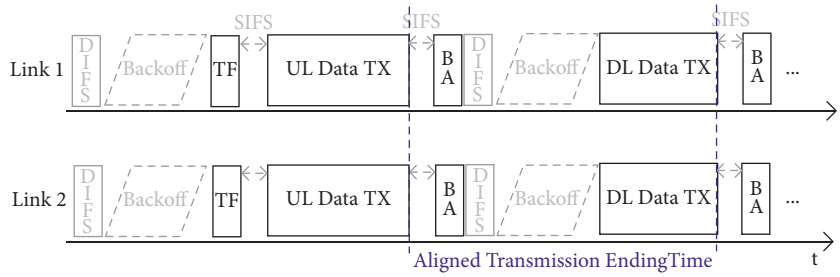

Figure 1: Synchronous transmission mode representation.

affiliated APs/STAs in this MLD can be regarded as multiple independent devices, and these devices can perform concurrent uplink and downlink transmission. Each affiliated AP/STA of an AP/STA STR MLD performs the channel access procedure independently over each link. MLD operating under asynchronous mode is called Simultaneously Transmit and Receive (STR) MLD. The latter allows an MLD to perform synchronized data frame transmissions on multiple links (by using the end time alignment or the defer transmission mechanism [8]). The MLD operating under the synchronous mode is called non-STR MLD. Since STR MLD usually provides poor performance due to the well-known in-device coexistence (IDC) interference, in this paper, we assume that all MLDs use synchronous transmission mode (see Figure 1).

1.1. Motivation. Potential benefits provided by MLO include (1) improving peak throughput by enabling opportunistic and efficient multilink channel access and allowing concurrent data transmission and reception over multiple frequency bands/channels; (2) reducing the end-to-end latency via seamless transitions among different links [2, 6, 9, 10].

However, [11, 12] evaluated the performance of the MLO scheme without retransmission in different channel environments (e.g., Rayleigh and Rician fading environments), which reveals that the potential gains provided by MLO in 802.11be can be decreased in bad channel conditions. Therefore, how to design the retransmission scheme utilizing multiple links to ensure reliable data transmission over noise wireless channels needs to be investigated.

1.2. Our Contribution. This paper aims to design a dynamic redundancy-based multilink retransmission scheme, which is suitable for the scenarios where each 802.11 device supports MLO. To the best of our knowledge, this paper is the first step toward designing a retransmission scheme to fully exploit the potential benefits of multiple links. This scheme can drastically alleviate system performance degradation caused by transmission failure in bad channel conditions. Our contributions are summarized as follows:

(1) We propose a synchronous multilink MAC protocol with Automatic Repeat Request (called SML-ARQ). In the contention process, it allows MLDs to perform channel access procedures over multiple links independently and concurrently. Consequently, compared to a single-link device, an MLD has more opportunities to access the channel than a single-link device. In the transmission process, it partitions a link packet into multiple blocks based on the number of available links of the MLD and then transmits these blocks concurrently using multiple links. If there is at least one block found to have failed after transmission, then those failed blocks will be retransmitted. In this way, the time taken by transmitting a link packet is shortened, and the negative impact of block errors can be efficiently mitigated.

(2) We develop a theoretical model to analyze the system throughput of our protocol. With this model, we are able to evaluate the performance of the system.

(3) We run extensive simulations to verify the accuracy of our theoretical model and demonstrate the superiority of our proposed protocol by comparing it with the synchronous multilink MAC protocol without a retransmission scheme (which is called SML-NARQ hereafter) in terms of system throughput. For example, adopting the same network environment (e.g., network topology, the number of available links, and fading environment), it is shown that there is up to 96.2% throughput gains achieved by using our protocol than that of using SML-NARQ.

2. Related Work

2.1. Retransmission Scheme in IEEE 802.11 Standard. In order to provide reliable data transmission, extensive research efforts have been dedicated to designing and implementing efficient ARQ schemes in wireless networks [13, 14]. Reference [15] designs a novel MAC-defined aggregated selective repeat ARQ scheme with the consideration of frame aggregation in the IEEE 802.11n standard and further proposes a Reed-Solomon (RS) block code-based aggregated hybrid ARQ scheme for achieving better performance under bad channel condition. Reference [16] proposes an adaptive ARQ scheme for aggregate MPDU transmission in the 802.11ac error-prone wireless network environment. Given the optimal parameter pairs (i.e., the number of lost MPDUs and the number of duplicated MPDUs) in duplicated MPDUs transmission, this protocol enhances system performance under worse channel quality.

Reference [17] proposes a QoS-aware backup padding ARQ Scheme suitable for multiuser (MU) transmission, which aims to solve the dummy bits problem and the blocking problem caused by failed packets; therefore, it can provide Quality of Service (QoS) guarantees.

However, most of the existing ARQ algorithms are designed and implemented in conventional 802.11 WLAN scenarios with multiple single-link devices. These designs allow retransmission using only one channel and therefore fail to fully utilize the potential gains of multiple channels in the scenarios where each device supports MLO.

2.2. Multiradio Multichannel Transmission in IEEE 802.11be. Reference [2] gives a comprehensive review of the IEEE 802.11be and evaluates its potential throughput gains of it through system-level simulation results. This paper demonstrates that, by using various candidate significant techniques (such as single-band operation, multilink operation, and link adaption), 802.11be can achieve a remarkable performance improvement with respect to 802.11ax. As one of the most representative features proposed in 802.11be, multilink operation (MLO) offers great potential to enhance system throughput and has thus attracted significant attention [6, 18]. Several studies have been devoted to discussing how to design and implement efficient synchronous channel access schemes supporting MLO. Reference [19] proposes an enhanced channel access mechanism to facilitate multilink utilization. To mitigate the effect of the radio-frequency (RF) power leakage problems, various penalties will be assigned to multilink devices based on specific rules, thus guaranteeing high performance. Reference [20] first indicates the backoff counter overflow problem during the synchronous channel access process and then proposes available solutions to tackle the problem, thereby improving throughput and latency.

Nevertheless, none of these designs for multiradio multichannel transmission focus on designing the retransmission process utilizing the MLO functionality. In the case of bad channel conditions, the performance of these designs drops sharply due to frequent transmission failure.

In contrast, unlike the previous works, our proposed SML-ARQ allows MLDs to utilize multiple links for retransmission, thereby achieving more reliable transmissions within a shorter transmitting period. The remainder of the paper is organized as follows. Section 3 details the MAC layer design of SML-ARQ. Section 4 provides a theoretical model to analyze the system throughput. Section 5 provides the performance evaluation. Section 6 concludes this paper.

3. Mac Layer Design

In this section, we first outline the proposed SML-ARQ and then, respectively, detail the contention process and the retransmission process.

3.1. Overview. Inspired by the multiradio multichannel retransmission scheme specified in [21], we propose a distributed MAC protocol for IEEE 802.11be, called SML-ARQ, by fully exploiting the potential gains of the MLO technique. With SML-ARQ, the goal of efficiently improving the network throughput and reducing latency is achieved.

As depicted in Figure 2(a), considering an infrastructure-based WLAN scenario with 1AP and v nodes, we introduce the proposed SML-ARQ protocol. In this paper, we assume that the system is saturated (each node is assumed to have consecutive uplink traffic flow).

The 802.11be allows MLDs to concurrently utilize multiple channels. For an MLD that possesses the STR mode, asynchronous transmissions can be operated independently on individual links. Each AP/STA that belongs to an AP MLD/non-AP MLD performs channel contention following IEEE 802.11 distributed coordination function (DCF) over different links independently. In this case, the throughput achieved by a STR mode n-link MLD can ideally be exactly n times that achieved by a legacy single-link device. The performance of STR mode MLD is better than that of non-STR mode MLD; however, to avoid the RF power leakage problem (i.e., the RF power leakage of one link ruins the transmission/reception on other links), we assume that all MLDs possess the non-STR mode and operate under the synchronous transmission mode.

Figure 2(b) shows an IEEE 802.11be n-link AP MLD and non-AP MLD. Each time the n-link non-AP MLD transmits an uplink link packet, this link packet will be divided into n blocks, and then each of these blocks will be transmitted over a respective link.

In SML-ARQ, all nodes execute two processes serially (as illustrated in Figure 3): the contention process and the dynamic transmission process (i.e., the transmission duration is variable).

In the contention process, each MLD first senses that the channel remains idle for DCF Interframe Space (DIFS) duration and then performs a channel access procedure following the multilink distributed coordination function (called ML-DCF).

In the transmission process, the MLD that infers that it has won the channel will instantaneously start a dynamic uplink synchronous transmission process with ARQ. Note that the ending time of a transmission performed by each of the affiliated STAs of the MLD is aligned.

3.2. Contention Process. Figure 4 depicts the contention process in SML-ARQ. For an n-link MLD, ML-DCF stipulates that each of n link can be designated as a channel access link (that is, each link has a separate backoff counter). An n-link MLD validates its victory when all of the backoff counters of n links reach zero, and afterwards, it will initiate an uplink data transmission process over n links simultaneously. Among n links, the latest one that has completed its backoff procedure will be set to Primary Link (PL), while the remaining $n-1$ links will be set to Auxiliary Link (AL).

Below, by taking an n-link MLD i as an example, we describe the design of the ML-DCF. As shown in Figure 4, suppose that the backoff counters selected by MLD i on link 2, link 3, . . ., link $n-1$ are all less than or equal to 3, while the backoff counters of link 1 and link n are 4 and 3, respectively.

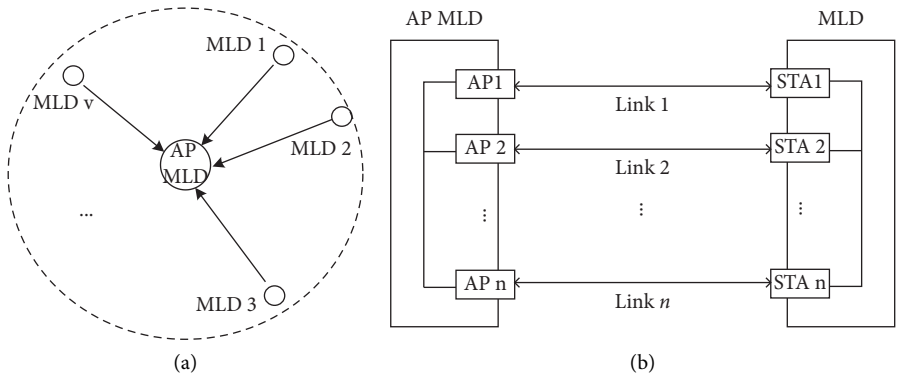

Figure 2: (a) The network topology and (b) IEEE 802.11be multilink devices with n links (where $n \leq 4$).

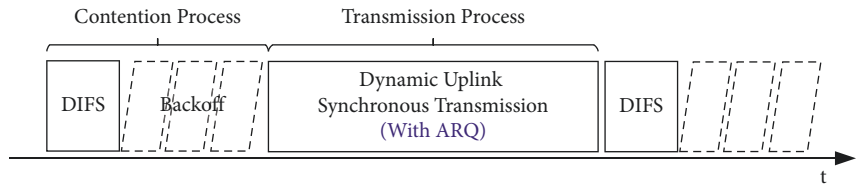

Figure 3: An overview of SML-ARQ design.

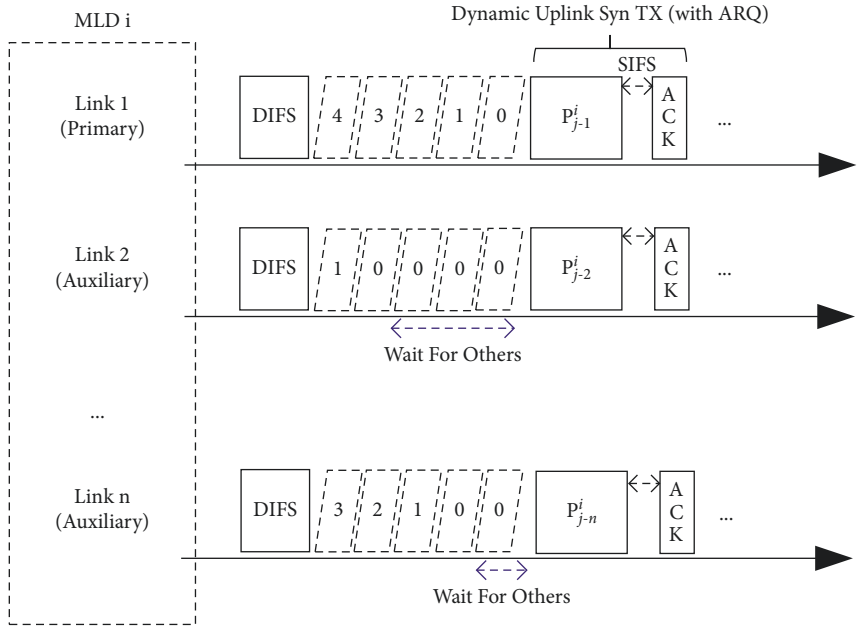

Figure 4: ML-DCF with the longest backoff of the MLD $i (i \in [1, v])$ in the SML-ARQ, where $n \leq 4$.

Therefore, the other links have to wait until the backoff counter of link 1 expires. Here, P^i_{j-f} represents the fth block ($f \in [1, n]$ of jth link packet transmitted by the MLD i. If each link of MLD i has received the acknowledgment frames (ACK) feedback (detailed in Section 3.3), then it will infer that the jth link packet has been received successfully by an AP MLD. In this case, the MLD i does not need to perform a retransmission process. Otherwise, if there is at least one link of MLD i that has received the negative-acknowledgement frames (NACK) feedback, MLD i will initiate a retransmission process (explained in Section 3.3). Note that the ACK time (i.e., transmission times of the ACK) is set equal to the NACK time (i.e., transmission times of the NACK).

Since each link packet will be divided into n blocks and is thereby able to be transmitted concurrently utilizing n channels, the txSlot size in SML-ARQ is set equal to the period of time needed for transmitting a block.

3.3. Retransmission Process. In SML-ARQ, if the receiver (i.e., one affiliated AP) successfully receives a block on a link, then it will send the ACK feedback; otherwise, it will send the

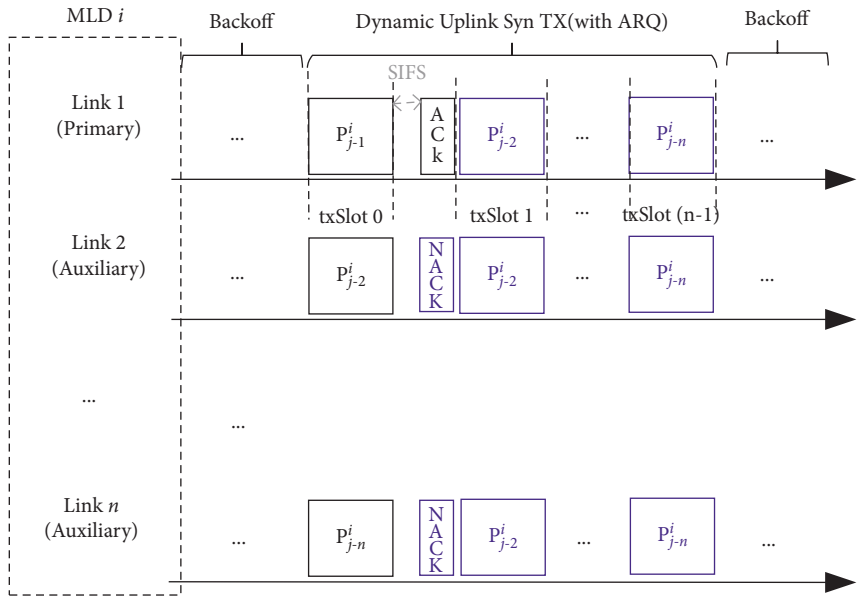

Figure 5: The retransmission process of the MLD i in the SML-ARQ (where the P^i_{j-f} ($f \in [1, n]$) represents the fth block of the jth link packet and $n \leq 4$).

NACK feedback. Based on the receiver feedback, as we mentioned before, if there is at least one block found to have failed after the first transmission slot (i.e., txSlot *0*), then those failed blocks will be retransmitted according to a simple rule: each block that was found to have failed in the first transmission will be retransmitted for only one time, and at each retransmission, it will be duplicated to n copies for concurrently transmitting over n available links. For a link packet composed of n blocks, the order of retransmissions for possible failed blocks is indicated by their failed block indices. As depicted in Figure 5, the indices of failed blocks are $2, \ldots, n$; therefore, n copies of $P^i_{j-2}, \ldots, P^i_{j-n}$ will be sequentially transmitted in, respectively, txSlot *1*, ..., txSlot $n - 1$.

Taking an n-link MLD i as an example, Figure 5 shows the retransmission process in SML-ARQ. Let P^i_{j-f} ($f \in [1, n]$)denote the fth block of the jth link packet transmitted by MLD i. Assume that only link 1 of MLD i has received the ACK feedback, while its other links have received the NACK feedback. In this case, MLD i infers that the P^i_{j-1} (i.e., 1th block of jth link packet transmitted by MLD i) is successfully received by AP MLD, while the other $n - 1$ blocks of jth link packet (i.e., $P^i_{j-2}, \ldots, P^i_{j-4}$) all have failed after the first transmission slot. Therefore, MLD i sequentially transmits n copies of $P^i_{j-2}, \ldots, P^i_{j-n}$ using n links simultaneously in the retransmission process.

In case there is no block found to have failed after the txSlot *0*, the uplink transmission process consists of one txSlot, a short interframe space (SIFS), and an ACK. In case there are k blocks found to have failed after the txSlot 0, the uplink transmission process consists of $k + 1$ txSlot, a SIFS, and an ACK/NACK. In the example in Figure 5, when the value of k is $n - 1$, the time of the dynamic transmission process is the sum of n txSlots and an ACK/NACK time.

4. Theoretical Analysis

In this section, we develop theoretical models to analyze the system throughput of the proposed SML-ARQ. Assuming that the system is saturated (each node is assumed to have consecutive uplink traffic flow) in SML-ARQ, we first calculate the conditional collision probability (i.e.,p) and the probability of the event that an STA of MLD transmits in a randomly selected slot (i.e., τ) and then define and obtain the system throughput.

4.1. The Probability $\mathbf{p}$ *and the Probability* τ. Let TX represent the event that an STA of an n-link MLD ($n \in [1, 4]$) transmits in a randomly chosen slot time, and the probability of TX is denoted by $P(TX)$. Assume that s represents the backoff stage of an STA, and then $s = i$ denotes the event that the backoff stage of the STA is $i (i \in [0, R]$. Let R represent the maximum retry limit. According to Bayes' theorem in [9, 22], we have

$$P(TX) \cdot \frac{P(s = i|TX)}{P(TX|s = i)} = P(s = i), \tag{1}$$

where $P(s = i|TX)$ refers to the conditional probability that the backoff stage of an STA is i assuming that this STA transmits in a randomly chosen slot time, while $P(TX|s = i)$ refers to the conditional probability of an STA transmitting in a randomly chosen slot time assuming that the backoff stage of this STA is i.

For each $i \in [0, R]$, we have

$$P(TX) \cdot \sum_{i=0}^{R} \frac{P(s = i|TX)}{P(TX|s = i)} = \sum_{i=0}^{R} P(s = i) = 1. \tag{2}$$

Then, the τ can be expressed as

$$P(TX) = \tau = \frac{1}{\sum_{i=0}^{R} P(s=i|TX)/P(TX|s=i)}. \quad (3)$$

Let v represent the total number of n-link MLDs. Following [23], the conditional collision probability p is the probability that a transmitted link packet collides, which can be expressed as

$$p = 1 - (1-\tau)^{v-1}. \quad (4)$$

Thus, to compute τ, we first calculate $P(s=i|TX)$ and $P(TX|s=i)$.

For $P(s=i|TX)$, it follows a truncated geometric distribution, with parameters $1-p$ and $R+1$ [22]; thus, we have

$$P(s=i|TX) = \frac{(1-p)p^i}{1-p^{R+1}}. \quad (5)$$

For $P(TX|s=i)$, it is calculated according to [22]

$$P(TX|s=i) = \frac{1}{1+E[b_i]}, \quad (6)$$

where $E[b_i]$ represents the average value of the chosen backoff counter on each link of an n-link MLD, when its current backoff stage is i.

Besides, we calculate the $E[b_i]$. Let discrete r.v. $X_{n.i}$ represent the chosen backoff counter on link$n$ of an n-link MLD after a successful link packet transmission or after a collision when the backoff stage of STA on link n is i. The range of $X_{n.i}$ is given by

$$X_{n.i} \in [0, W_i - 1], \quad (7)$$

where $W_i = 2^i CW_{\min}$.

The chosen backoff counters on each link of an n-link MLD are independent and identically distributed (i.i.d.) from a uniform distribution over $(0, W_i - 1)$

$$X_{1.i}, X_{2.i}, \cdots, X_{n.i} \sim \text{Uniform}(0, W_i - 1). \quad (8)$$

For $r \in [1, m]$, $x \in [0, W_i - 1]$, we have

$$P_{X_{r.i}}(x) = P(X_{r.i} = x) = \frac{1}{W_i}. \quad (9)$$

Let discrete r.v. $Y_{n,i}$ represent the largest one of n chosen backoff counters of n-link MLD when its corresponding backoff stage is i, i.e.,

$$Y_{n,i} = \max(X_{1.i}, X_{2.i}, \cdots, X_{n.i}). \quad (10)$$

Let c represent a constant value ($c \in [0, W_i - 1]$), and then, the cumulative distribution function of $Y_{n,i}$ can be expressed as

$$P(Y_{n,i} \le c) = P(X_{1,i} \le c, X_{2,i} \le c, \cdots, X_{n,i} \le c) = P(X_{1,i} \le c)P(X_{2,i} \le c)\cdots P(X_{n,i} \le c) = \left(\frac{c+1}{W_i}\right)^n. \quad (11)$$

Using (11), we see that

$$P(Y_{n,i} = c) = P(Y_{n,i} \le c) - P(Y_{n,i} \le c-1) = \left(\frac{c+1}{W_i}\right)^n - \left(\frac{c}{W_i}\right)^n. \quad (12)$$

By substituting (12) in (6), we obtain

$$P(TX|s=i) = \frac{1}{1+E[b_i]} = \frac{1}{1+\sum_{c=0}^{W_i-1} c \cdot P(Y_{n,i}=c)} = \frac{1}{1+\sum_{c=0}^{W_i-1} c \cdot \left((c+1/W_i) - (c/W_i)n\right)}, \quad (13)$$

where $n \in [1,4]$, $i \in [0,R]$, and $c \in [0, W_i - 1]$.

Finally, by substituting (5) and (13) in (3), we obtain the expression of τ with p as a parameter. This expression and (4) represent a nonlinear system, which can be solved using fixed point iteration, and the numerical results of τ and p can be obtained.

4.2. Throughput Efficiency. Let S denote the normalized system throughput, defined as the ratio of the MAC Layer throughput and the data rate. Let Γ and R denote the MAC Layer throughput and the data rate, respectively, and we have

$$S = \frac{\Gamma}{R}. \quad (14)$$

Here, the MAC Layer throughput Γ is defined as the average number of uplink bits transmitted successfully in the average length of a generic slot time Ω, i.e.,

$$\Gamma = \frac{P_s P_{tr} \overline{L_p}}{E(\Omega)}, \quad (15)$$

where P_s denotes that a successful transmission occurs after contention stage (i.e., the probability that exactly one n-link MLD transmits a link packet on the channel), the probability that at least one n-link MLD attempts to transmit in a generic slot time, and the average payload size of a successfully received link packet (i.e., when a link packet error does not occur).

According to [23], the P_{tr} and P_s are given by

$$P_{tr} = 1 - (1-\tau)^v, \qquad P_s = \frac{n\tau(1-\tau)^{v-1}}{1-(1-\tau)^v}. \quad (16)$$

Below, to calculate $\overline{L_p}$, we first calculate the average block error rate, which is denoted as $\overline{P_{be}}$. Let b represent the length of each block that is transmitted in one link of n-link MLD, and we have

$$b = L_{phy} + L_{mac} + \frac{1}{n} L_{Payload}. \quad (17)$$

Assuming that n links can all be regarded as identical but independent Nakagami-slow-fading channels corrupted by independent additive white Gaussian noise, let γ $(\gamma > 0)$ represent the instantaneous SNR per bit, considering using M-ary QAM in Nakagami- m $(m \geq 1/2)$ slow-fading channels, following [21], and $\overline{P_{be}}$ is given by

$$\overline{P_{be}} = \int_0^{\infty} P(\gamma)\left(1 - \left(1 - \epsilon_{ins}(\gamma)\right)^b\right) d\gamma, \quad (18)$$

where $\epsilon_{ins}(\gamma)$ represents the instantaneous bit error rate (BER) conditional on γ given in [24, 25]; $P(\gamma)$ represents the probability density function (pdf) of instantaneous signal-to-noise ratio (SNR) per bit that was driven in [26], which is given by

$$P(\gamma) = \frac{m^m \gamma^{m-1} e^{-m\gamma/\overline{\gamma_c}}}{\overline{\gamma_c}^m \Gamma(m)}, \quad (19)$$

where $\Gamma(\bullet)$ represents the Gamma function, and $\overline{\gamma_c}$ denotes the average SNR per bit.

Since the average block success rate is equal to $1 - \overline{P_{be}} 1 - \overline{P_{be}} \in [0, 1])$, let r.v. T follow a binomial distribution with parameters n and $\overline{P_{be}}$; thus, we have

$$T \sim Bn, 1 - \overline{P_{be}}. \quad (20)$$

Let $T = kk \in [0, n])$ represent the event that, within one txSlot, there are exactly k blocks that are successfully received in n blocks transmitted by an n-link MLD. Then, the probability of $T = k$ is expressed as

$$P_r(T = k) = \binom{n}{k} \left(1 - \overline{P_{be}}\right)^k \overline{P_{be}}^{n-k}. \quad (21)$$

Then, $\overline{L_p}$ can be calculated as

$$\overline{L_p} = E\left(T_p\right) = \left(P_r(T = n) + \sum_{i=0}^{n-1} P_r(T = i) \sum_{j=1}^{n} P_r(T = j)^{n-i}\right) \bullet L_{payload}. \quad (22)$$

Finally, we compute the $E(\Omega)$. Let σ denote the duration of an empty slot time in 802.11, and let σ_1 represent/denote the duration of a txSlot ($\sigma_1 = T_{phy} + T_{mac} + 1/nT_{payload}$. We can calculate Ω as follows:

$$\Omega = \begin{cases} T_{difs} + \overline{T_s}, & w.p. P_{tr} P_s, \\ T_{difs} + T_c, & w.p. P_{tr}\left(1 - P_s\right), \\ \sigma, & w.p. 1 - P_{tr}. \end{cases} \quad (23)$$

Hence, $E(\Omega)$ can be expressed as

$$E(\Omega) = \left(1 - P_{tr}\right)\sigma + P_{tr} P_s \left(T_{difs} + \overline{T_s}\right) + P_{tr}\left(1 - P_s\right)\left(T_{difs} + T_c\right), \quad (24)$$

where T_c represents the duration of a collision (i.e., the channel is unavailable for a while due to an unsuccessful link packet transmission), $T_c = (n + 1)\sigma_1 + T_{sifs} + T_{nack}$, while $\overline{T_s}$ represents the average time the channel is sensed busy due to a successful link packet transmission.

Let $T_{ack/Nack}$ represent the transmission times of the ACK/NACK frame (where we assume that the length of the ACK/NACK frame is equal); thus, $\overline{T_s}$ can be calculated as

$$\overline{T_s} = E\left(T_s\right) = \sum_{i=0}^{n} P_r(T = i) t_{s_i}, \quad t_{s_i} = (n - i + 1)\sigma_1 + T_{sifs} + T_{ack/Nack}, \quad (25)$$

where t_{s_i} refers to the duration of the transmission process given that there are exactly i blocks that are successfully received in n blocks transmitted by an n-link MLD after the first txSlot.

5. Performance Evaluation

In this section, we evaluate the performance of SML-ARQ protocol via extensive simulations. Besides, we compare our protocol with the SML-NARQ protocol.

For SML-ARQ, the theoretical throughput efficiency is calculated according to (*14*); and the SML-ARQ simulator is written using C++. Table 1 shows the default parameter settings in our protocols and the SML-NARQ. The number of nodes v is set equal to 30 by default. The slot time size, the distributed coordination function interframe space (DIFS), and the SIFS are set equal to 9 μs, 34 μs, and 16 μs, respectively, which are set in accordance with IEEE 802.11be. In this paper, we consider Nakagami-1/2 slow-fading environments. The data rate is set to 54 Mbps. The length of the MAC payload is 1080 Bytes. The value of each simulation result is an average of over 5 simulation runs, where each run lasts for 100 seconds.

Table 1: Parameter settings in simulation.

v	30	Slot	9 μs
T_{DIFS}	34μs	m	1/2
T_{SIFS}	16μs	R	135 Mbps

In Figures 6–10, curves with labels "ana" and "sim" denote the theoretical and simulation results, respectively; curves labeled "($n = 1$", "($n = 2$", "($n = 3$", and "($n = 4$" represent the results of n-link SML-ARQ when n is equal to 1, 2, 3, and 4, respectively. In Figures 6 and 7, curves labeled "($c = 1$", "($c = 2$", "($c = 3$", and "($c = 4$"represent the simulation results of n-link SML-NARQ when n is equal to 1, 2, 3, and 4, respectively.

Figure 6 plots the normalized throughput efficiency of SML-ARQ and SML-NARQ as the number of nodes varies from 2 to 50, when setting SNR= 12dB and 16-QAM. From this figure, we have the following four observations.

(1) For our protocol, the simulation curves almost overlap the corresponding theoretical curves from (14); the average relative error between them is 1.8%, which demonstrates that our model is very accurate.

(2) The system efficiency in our protocol is higher than that in the compared protocol. In total, there are

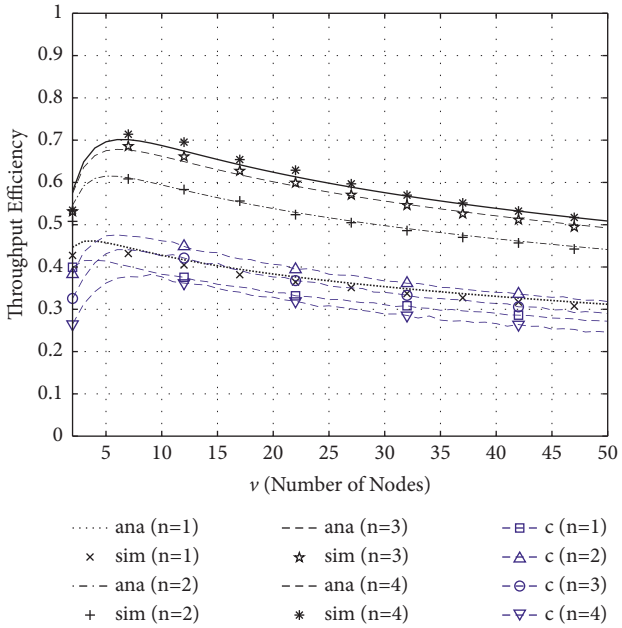

Figure 6: Throughput efficiency versus v.

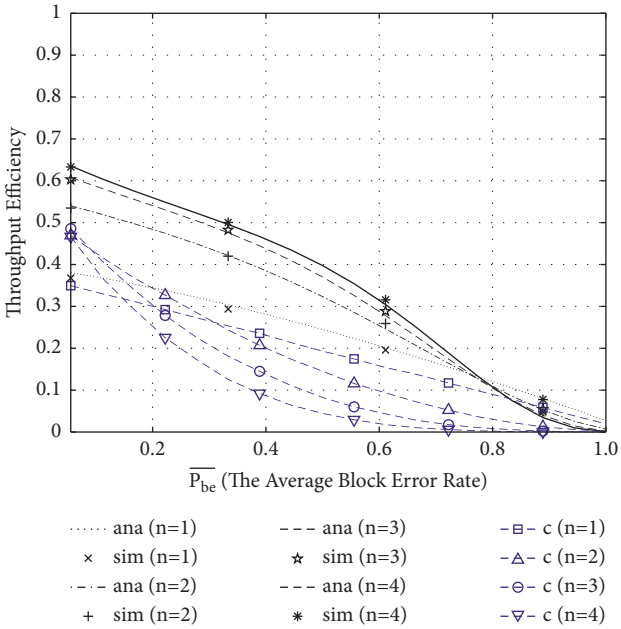

Figure 7: Throughput efficiency versus $\overline{P_{be}}$.

approximately 34.0% and 96.2% throughput gain achievable by *2*-link SML-ARQ and *4*-link SML-ARQ compared to *2*-link SML-NARQ and *4*-link SML-NARQ, respectively. It is obvious in the figure that the improvement in channel utilization is proportional to the number of links (say, the larger the n, the higher the n-link SML-ARQ system efficiency). This is because, for one thing, the n-link SML design fully exploits potential gains of n-link compared with a single-link device. Specifically, it can (1) increase channel access efficiency (i.e., there are far more opportunities to access the channel); (2) shorten the time taken by transmitting a link packet. For another reason, the ARQ mechanism effectively mitigates the negative impact of block errors. Recalling the ARQ design, if a block error occurs on a specific link in the first txSlot, the failed block will be copied n times, and then, these n copies will be, respectively, retransmitted on each of the n links. In the retransmission process, the probability that all n copies will fail is low. Consequently, our design can significantly improve system performance.

(3) The system throughput efficiency in 2-link SML-NARQ exceeds the system throughput efficiency of 3-link SML-NARQ and 4-link SML-NARQ, and the system throughput efficiency of 4-link SML-NARQ is even slightly lower than that of 1-link SML-NARQ. The reason is that, in n-link SML-NARQ, a link packet is divided into n blocks, and these n blocks are transmitted concurrently on n links, respectively. In the absence of a retransmission scheme, if and only if all n blocks have been successfully transmitted (that is, no block error has ever occurred on these n links), the link packet composed of those n blocks can be regarded as successfully received by the receiver. Under the poor channel conditions, the probability of a link packet being successfully received by the receiver is low when using SML-NARQ. Although SML-ARQ significantly shortens the duration of a link packet transmission, frequent occurrence of block errors will offset the gains offered by multilinks.

(4) For both SML-ARQ and SML-NARQ, the throughput efficiency decreases slightly as v increases. The reason is that as the number of nodes participating in the contention increases, collisions caused by two or more nodes choosing identical backoff counters are prone to occur.

Figure 7 plots the normalized throughput efficiency of SML-ARQ and SML-NARQ as the average block error rate varies from 0.0 to 1.0 when setting $v = 30$. In this figure, we can see that:

(1) For our protocol, the theoretical results well match the corresponding simulation results; the average relative error between them is 1.7%, meaning that our theoretical model is very accurate.

(2) For both SML-ARQ and SML-NARQ, the normalized throughput efficiency decreases as $\overline{P_{be}}$ increases. This indicates that the system performance of using either of these two protocols is severely affected by the channel environment. The worse the channel environment, the lower the performance of SML-ARQ and SML-NARQ.

(3) The throughput efficiency in SML-NARQ is almost always lower than that in SML-ARQ. In the case of $\overline{P_{be}} \geq 0.09$, $\overline{P_{be}} \geq 0.15$, and $\overline{P_{be}} \geq 0.26$, the throughput efficiency of 4-link SML-NARQ, *3*-link SML-NARQ, and *2*-link SML-NARQ, respectively, is lower than

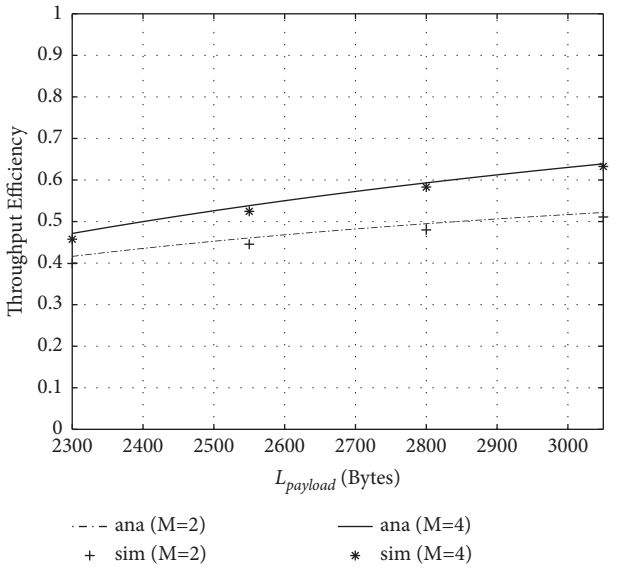

Figure 8: Throughput efficiency versus payload length.

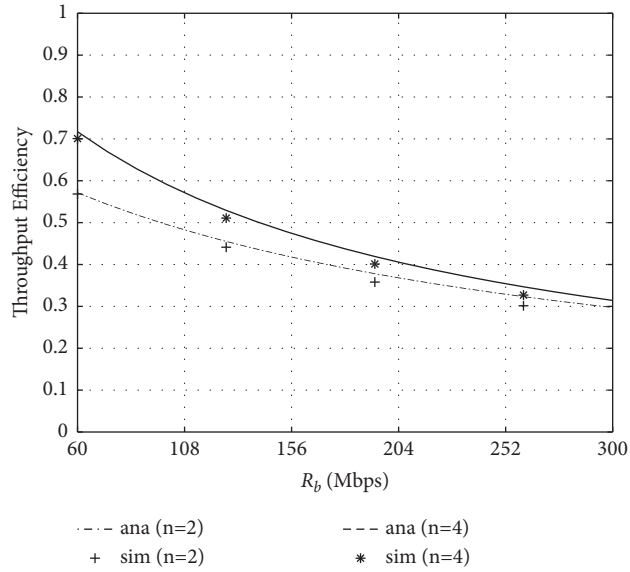

Figure 9: Throughput efficiency versus data rate.

that of *1*-link SML-NARQ. This indicates that, for n-link SML-NARQ, once $\overline{P_{be}}$ exceeds a certain value, frequent block errors in turn severely reduce the throughput gain provided by multi-link. The performance of using n-link SML-NARQ is inversely proportional to n as $\overline{P_{be}}$ increases (that is, the larger the value of n is, the more the throughput efficiency of n-link SML-NARQ tends to descend more rapidly as $\overline{P_{be}}$ increases). Obviously, in the case of bad channel conditions, the negative impact of block errors will seriously degrade the performance of the SML scheme.

(4) There is a gradual decline in the throughput efficiency of SML-ARQ as $\overline{P_{be}}$ increases. This indicates that the multilink retransmission scheme exploited in SML-ARQ can efficiently mitigate the negative impact of the frequent occurrence of block errors. For SML-ARQ, only in extremely bad wireless channel conditions (i.e., when $\overline{P_{be}} \geq 0.78$), the potential throughput gain achievable by multilink retransmission will be offset by a high block error rate.

Figure 8 plots the normalized throughput efficiency of SML-ARQ as the payload length varies from 2300 Bytes, 2400 Bytes, 2500 Bytes, ..., to 3000 Bytes when setting $v = 30$, SNR = 12 dB, and 16-QAM. From this figure, we can see that:

(1) The theoretical results closely match the simulation results. The average relative error between them is 0.9%. This manifests that our model is accurate.

(2) For both 2-link SML-ARQ and 4-link SML-ARQ, the system throughput efficiency increases with increasing $L_{payload}$. The reason is that, in the contention process, SML-ARQ performs time domain channel contention following IEEE 802.11 DCF. Its contention process adopts binary exponential backoff (BEB), during which channel resources are wasted most of the time due to the channel being forced to remain idle in the case of all nodes performing random backoff. Therefore, the larger the payload, the smaller the fraction of time that the contention overhead occupies the channel, which in turn improves throughput efficiency.

(3) The throughput efficiency in 4-link SML-ARQ is always higher than that in 2-link SML-ARQ. This is because (a) the number of available links in 4-link SML-ARQ is larger than that in 2-link SML-ARQ, thus improving the efficiency (that is, the time required to transmit a data packet is shorter); (b) ARQ mechanism effectively compensates for the drawback of failed transmissions caused by block error. Consequently, the 4-link SML-ARQ outperforms the 2-link SML-ARQ in terms of the system throughput.

Figure 9 plots the normalized throughput efficiency of SML-ARQ as the payload length varies from 60 Mbps, 80 Mbps, 100 Mbps, ..., to 300 Mbps when setting $v = 30$, SNR = 12 dB and 16-QAM. From this figure, we can see that:

(1) For our protocol, the theoretical results closely match the corresponding simulation results (the average error between them is 1.6%), manifesting that our theoretical model is very accurate.

(2) For both 2-link SML-ARQ and 4-link SML-ARQ, throughput efficiency decreases with the increase of R_b. The reason is that, with the increase of R_b, the PHY preamble is still transmitted at 6 Mbps; thereby, the fraction of time that the channel is used for transmitting payload gradually decreases.

(3) The throughput efficiency in 4-link SML-ARQ is always higher than that in the 2-link SML-ARQ. This

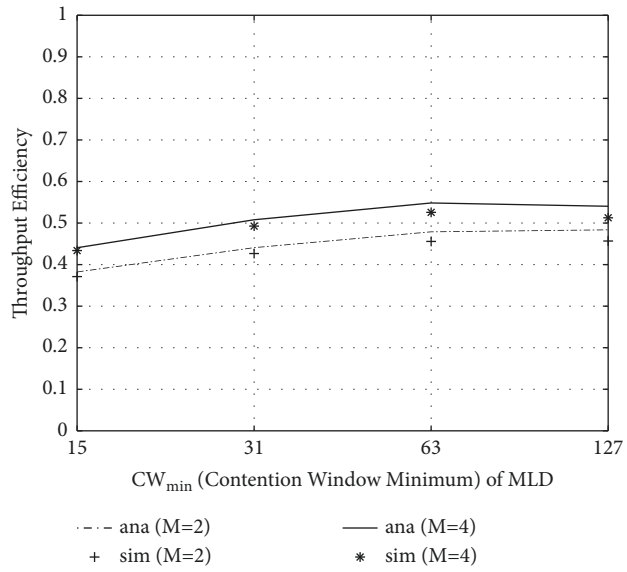

Figure 10: Throughput efficiency versus contention window minimum of MLD.

indicates that the 4-link SML-ARQ can achieve better performance than 2-link SML-ARQ.

Figure 10 plots the normalized throughput efficiency of SML-ARQ as the contention window minimum varies from 15, 31, . . ., to 127 when setting $v = 30$, SNR = 12 dB and 16-QAM. From this figure, we can see that:

(1) For our protocol, the theoretical results well match the simulation results (the average error between them is 3.2%), manifesting that our theoretical model is accurate.

(2) For both 2-link SML-ARQ and 4-link SML-ARQ, the throughput efficiency first gradually increases with the increase of $CW_{\min}$ and then declines with the further increase of $CW_{\min}$. The reason is that a large $CW_{\min}$ leads to a low collision probability and high contention overhead.

(3) The throughput efficiency in 4-link SML-ARQ is always higher than that in the 2-link SML-ARQ, showing that the 4-link SML-ARQ can achieve better performance than 2-link SML-ARQ.

6. Conclusions

Multilink operation (MLO) is considered a key candidate technology in 802.11be, which allows devices to use multiple links to send and receive data simultaneously, thus helping improve throughput and reduce latency. However, as the channel environment deteriorates, the performance of MLO schemes will gradually degrade. To address this issue, in this paper, we first propose a multilink MAC protocol with a dynamic redundancy-based retransmission scheme consistent with the IEEE 802.11be. In the contention process, each MLD exploits multiple links to contend for channels simultaneously, thereby having a higher chance for winning channel contention compared to legacy single-link devices. In the transmission process, a link packet will be partitioned into multiple blocks and then transmitted with multiple links. To ensure the reliability of data transmission, any failed blocks will be copied and retransmitted only one time using multiple links. Next, we develop a theoretical model to calculate system throughput. Finally, extensive simulations verify the accuracy of our theoretical model and the effectiveness of SML-ARQ. [5].

Data Availability

The data underlying the results presented in the study are available within the article.

Conflicts of Interest

The authors declare that are no potential conflicts of interest regarding the publication of this paper.

Acknowledgments

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