International Journal of Photoenergy

Photoenergy: Progress in Si-Related Solar Cells for a Low Cost and High Efficiency

Guest Editors: J. Yi, Eicke R. Weber, C. W. Lan, Stephen Bremner, and D. H. Kim

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Editorial

Photoenergy: Progress in Si-Related Solar Cells for a Low Cost and High Efficiency

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As the global effort dedicated to "sustainable growth and a low-carbon society" has increased, so have the opportunities and challenges for renewable energy technologies, like photovoltaic solar cells. A great amount of investment in solar cells research and subsequent technical break-throughs has been witnessed in the last decade, with the promise of further improvements to both performance and affordability expected. The overwhelming majority of commercially available solar cells remain silicon based, a situation not expected to change in the near-to-medium term due to silicon's abundance and compatibility with existing large-scale electronics manufacturing technologies.

Far from being a fully mature and settled field of research, silicon-based photovoltaics remains dynamic with ever increasing innovations being developed in terms of performance and lowered production costs being reported. Silicon's preeminence in photovoltaics, and the diverse approaches being pursued in photovoltaics in general are reflected in this special issue that is composed of the following selected topics: silicon solar cell devices and technologies, solar cell Process and production-related materials, device and process-related characterizations, Low Cost-related material, device and process, High efficiency approaches and technologies, and other novel solar cell materials and devices.

The articles collected together in this special issue have been sourced in two ways; firstly, roughly half of the articles were presented during the Global Photovoltaic Conference 2011 (GPVC 2011) that was held at Busan, Republic of Korea, in September 2011. Around 300 papers were presented at this conference, with outstanding presentations invited to be submitted as full-length version manuscripts for this special issue. Secondly, an open call was made to the photovoltaics community to submit new and interesting results related to, but not restricted to, silicon-based photovoltaics. The high standard expected is reflected in that only approximately one-third of submitted manuscripts were accepted for publication in this issue.

The range of topics considered in the papers is considerable, spanning numerical studies of conventional crystal growth technologies, novel production methods for conventional silicon solar cells, nanoinspired architectures, dyesensitized approaches, and even a new characterization approach based on microplasma analysis. We, the editorial team, expect, due to the high quality of the articles included in this issue, that not only will good representation of the state of research in silicon based photovoltaics be achieved, but further efforts will be spurred on by the discoveries reported.

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Research Article

Impedance Spectroscopic Study of p-i-n Type a-Si Solar Cell by Doping Variation of p-Type Layer

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We investigated p-i-n type amorphous silicon (a-Si) solar cell where the diborane flow rate of the p-type layer was varied and the solar cell was measured static/dynamic characteristics. The p/i interface of the thin film amorphous silicon solar cells was studied in terms of the coordination number of boron atoms in the p layer. p-type layer and p/i interface properties were obtained from the X-ray photoelectron spectroscopy (XPS) and impedance spectroscopy. One of the solar cells shows open circuit voltage (V_{oc}) = 880 mV, short circuit current density (J_{sc}) = 14.21 mA/cm^2, fill factor (FF) = 72.03%, and efficiency (η) = 8.8% while the p-type layer was doped with 0.1%. The impedance spectroscopic measurement showed that the diode ideality factor and built-in potential changed with change in diborane flow rate.

1. Introduction

In a-Si : H-based p-i-n type solar cells, the device performance is limited by various factors, most important of which is defects in the p-layer and that in the p/i interface. The electron-hole pair, generated in the i-type layer, is collected by the n-type and p-type layers. Thus effective doping of these extrinsic layers is very important in creating the built-in field so that the photo-generated charge carriers are efficiently collected. At the p/i interface there exists a depletion region, a similar depletion layer also exist at the n/i interface. These two depletion regions create localized capacitors, formed by the outer layers of the depletion regions. As the depletion region is free from charge carriers so the defects in these regions become electronically more active. The photo-generated carriers, that pass through the depletion region, will most probably face hindrance in their movement or effective resistance faced by the charge carriers will become high. An impedance spectroscopic measurement can help exploring the interface characteristics to some extent.

We performed impedance spectroscopic measurement of the solar cells that have similar i-type and n-type layers but the doping ratio for the p-type layer was different. The p-type layers of these cells were deposited by increasing diborane doping ratio during its deposition. The impedance spectroscopic analysis was performed by following Cole-Cole principle [1, 2] in which the real and imaginary components of the complex impedance (Z) are plotted for various sinusoidal input signals. Impedance spectroscopy is particularly suitable for studying the properties of junctions, interfaces, and contacts. The p/i interface properties were obtained from the static/dynamic characteristics. The experimental details are given in the following.

2. Experimental

Hydrogenated a-Si solar cells were deposited in a cluster type radio frequency (RF) plasma-enhanced chemical vapor deposition (PECVD), with the RF of 13.56 MHz (for both p-layer and n-layer) and very high frequency of 60 MHz (for

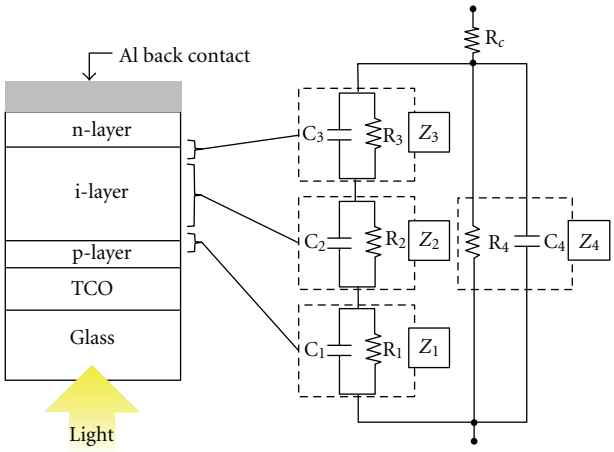

Figure 1: Equivalent circuit diagram of solar cell impedances, formed by a combination of resistors and capacitors.

the i-layer) power source. Prior to deposition, the glass substrates were ultrasonically cleaned by dipping in acetone, isopropyl alcohol, and deionized (DI) water for 10 min. The sample deposition conditions for the p-type layers are summarized in Table 1. The devices were deposited on TCO-coated glasses (Asahi VU-glass).

The boron doping ratio was varied by changing the flow rate of B_2H_6. The optoelectronic properties of these films were measured. Spectroscopic ellipsometry (VASE, J. A. Woollam, 240 nm $< \lambda <$ 1700 nm) was used to measure the thickness, refractive index, absorption coefficient, and optical band gap at an angle of incidence of 65° in the spectral range of 240 nm to 1700 nm. The electrical characteristics were studied by the coplanar method using programmable Keithley 617 electrometer using the samples grown on the glass substrates.

The current-voltage (I-V) characteristics of the cells were measured under light intensity of 100 mW/cm^2 (AM1.5), at a temperature of 25°C. The impedance measurement was carried out using 4192A LF impedance analyzer. The amplitude of the ac test signal was 10 mV. The measurement frequency was in the range of 1 Hz to 1 MHz.

3. Model

We adopt the following assumptions in order to limit our scope of impedance analysis to a few important parameters we are interested in.

(1) We assume the cell has three interfaces of importance, having a combination of resistor-capacitor connected in parallel to each of the interfaces, as shown in Figure 1.

(2) The TCO/p-layer interface does not significantly influence total capacitance of the cell, so we assume that the depletion capacitances at p/i interface, i bulk, and i/n-interface are significant in our study.

Based on the above assumptions we draw the equivalent circuit diagram of the impedance of the solar cell, as shown in Figure 1. The model will help us simplifying the impedance analysis of the Cole-Cole plot.

4. Results and Discussions

In the following we give results and discussions on the effect of boron doping on the p-type material, characteristics of the solar cells, and its impedance analysis. These p-type a-Si : H materials while used in solar cell is expected to show useful photovoltaic characteristics.

4.1. Effect of B_2H_6 Doping on p-Type Layer. The B(1s) XPS peak of pure boron appears at a binding energy of 188 eV. It bonds with Si and shifts to a lower energy state. Figure 2 shows the total B(1s) XPS peak (a) and the deconvoluted B(1s) XPS peak (b). The 186.6 eV represents a threefold coordination and the 187.7 eV a fourfold coordination [3]. The result of the deconvolution analysis, assuming Gaussian functions shows that the boron atoms in the states of both the three- and fourfold coordination increased with the increase of the diborane flow rate. When B_2H_6, SiH_4, and H_2 form a bonding, the boron existed in the state of an inactive threefold coordination and an active fourfold coordination. As the diborane flow rate increased, the fourfold coordination that contributed to the dark conductivity also increased. Increasing the fourfold coordination led to an increase of the positively charged dangling bonds by the "8-N" doping rule [4, 5].

Figure 3 shows dark conductivity (σ_d) and activation energy (E_a) at various doping level. At increased doping the conductivity increases and the activation energy decreases, a change as expected from the change of coordination [6]. The dark conductivity of the p-type layer was measured in planar electrode configuration. The activation energy (E_a) was obtained from the temperature-dependent dark conductivity $\sigma_d(T)$ measurement, following the Arrhenius relation

$$\sigma_d(T) = \sigma_o \exp\left(-\frac{E_a}{kT}\right), \quad (1)$$

where σ_o is a conductivity prefactor, T the absolute temperature, and k Boltzmann's constant. Table 3 shows the characteristic optoelectronic properties of the three layers of the solar cell. The increase in diborane flow rate during deposition of the p-type layer leads to a change in optical absorption spectra of the films, as observed by spectroscopic ellipsometry (SE) measurement. Optical band gap (E_g) was measured using these absorption coefficients and Tauc's formula

$$(\alpha h\nu)^{1/2} = K\left(h\nu - E_g\right), \quad (2)$$

where h is Plank's constant, ν is optical frequency, and K is a constant. Optical absorption coefficients of the films, α, is measured with the help of spectroscopic ellipsometry (SE), and $(\alpha h\nu)^{1/2}$ is plotted with $h\nu$. A linear fit is drawn at the absorption edge region and the intercept of the linear fitting is used as a measure of E_g.

It shows that the E_g and E_a of the p-layer decrease with increasing diborane flow rate, this is a usual phenomena [7–9].

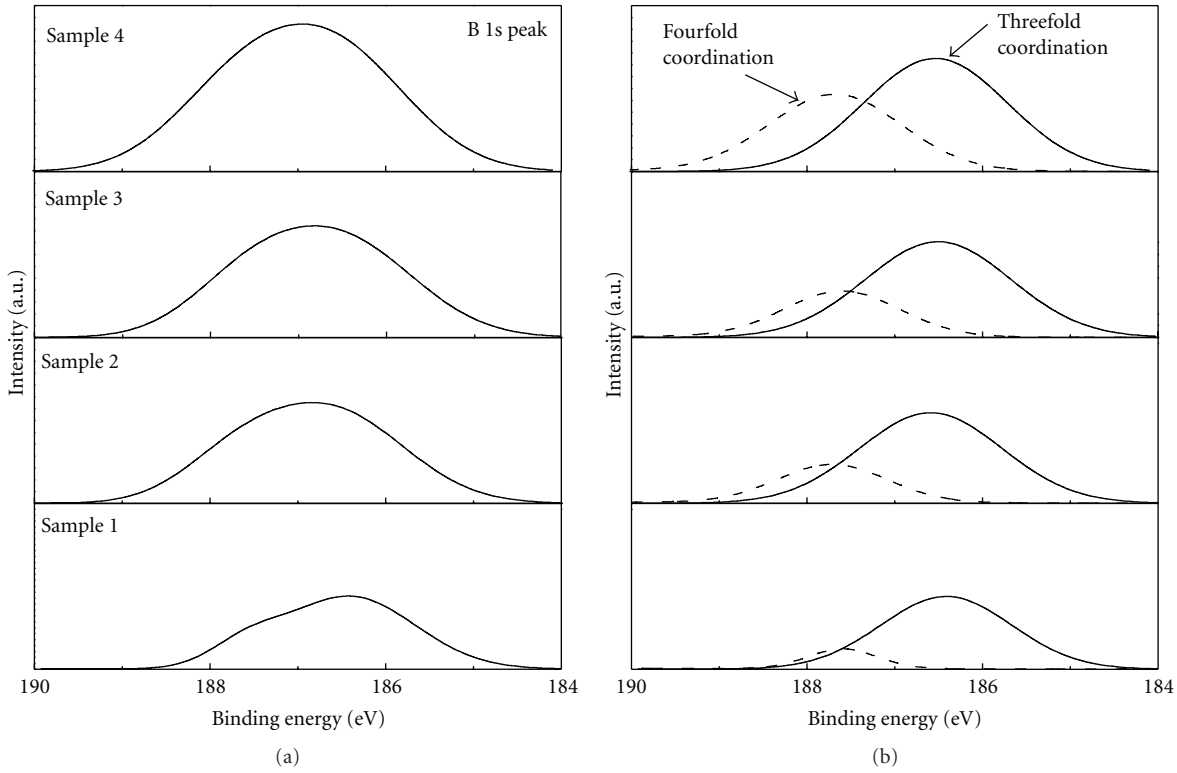

Figure 2: XPS spectrum of the B(1s) signal of the boron-doped amorphous silicon layers. It is deconvoluted into two Gaussian peaks, as shown in (b).

Table 1: The deposition conditions for the p-type a-Si : H layers.

Sample	Gas ratio			Thickness (nm)	Power density (mW/cm^2)	Temp. (°C)	Pressure (mTorr)
	SiH_4	H_2	B_2H_6				
1	1	5	0.05	150	50	175	200
2			0.1				
3			0.3				
4			0.5				

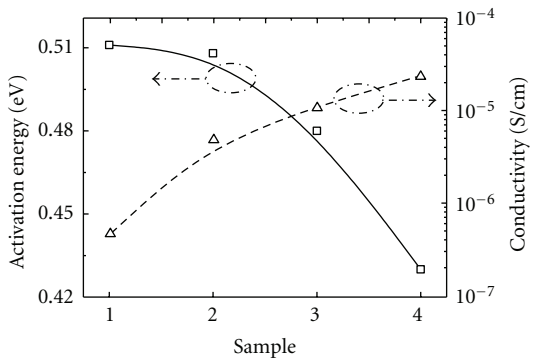

Figure 3: Dark conductivity and activation energy of p-type a-Si : H prepared at various B_2H_6 flow rates.

4.2. Effect of B_2H_6 Doping on Solar Cell. The current-voltage characteristics of the solar cell under light is shown in Figure 4. We have observed an initial improvement in solar cell characteristics in sample 2 from that of sample 1 but afterwards the solar cell characteristics degrade in FF, J_{sc}, V_{oc}, and η. For sample 2 these values are $J_{sc} = 14.21$ mA/cm^2, $V_{oc} = 870$ mV, $\eta = 8.8\%$, and fill factor (FF) = 71.51%.

As it is expected that higher B_2H_6 flow rate will make the p-type layer increasingly doped, it is expected that it will help creating higher built-in potential at the p/i interface, resulting in better collection of electron-hole pairs by the n-type and p-type layer of the solar cell and improved solar cell characteristics. However, as diborane flow rate increases, the defects in the p-layer and p/i interface also increase. The open circuit voltage and fill factor decreased from 880 mV to 800 mV, 72% to 69% with three- and fourfold coordination increased from sample 2 to sample 4. The defects in the p type window layer also increased because boron atoms coordination usually produces doping-induced defects [4, 5]. These increases in the defect resulted in a carrier recombination near the p/i interface and caused the reduction

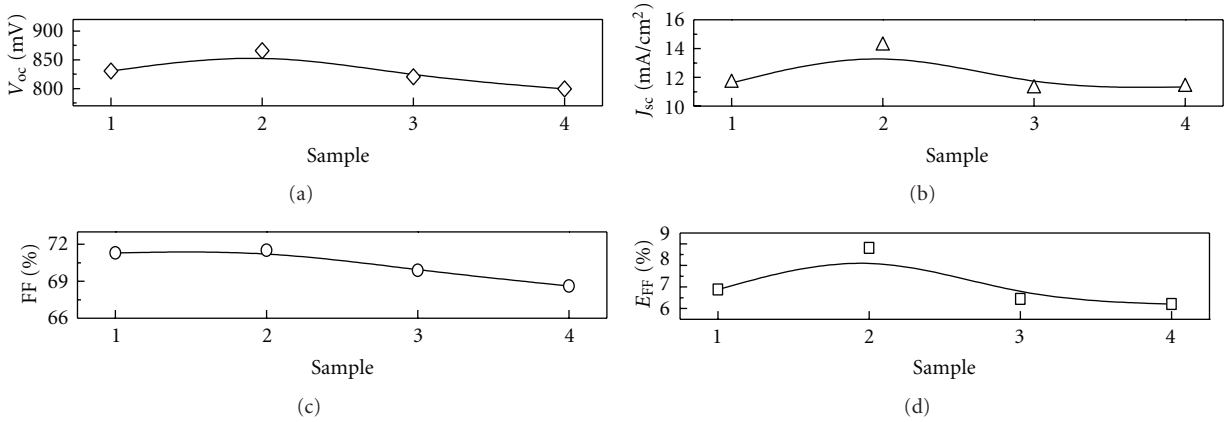

Figure 4: Solar cell parameters measured under AM 1.5 illumination conditions of thin film solar cells, with p-layer having different doping ratio.

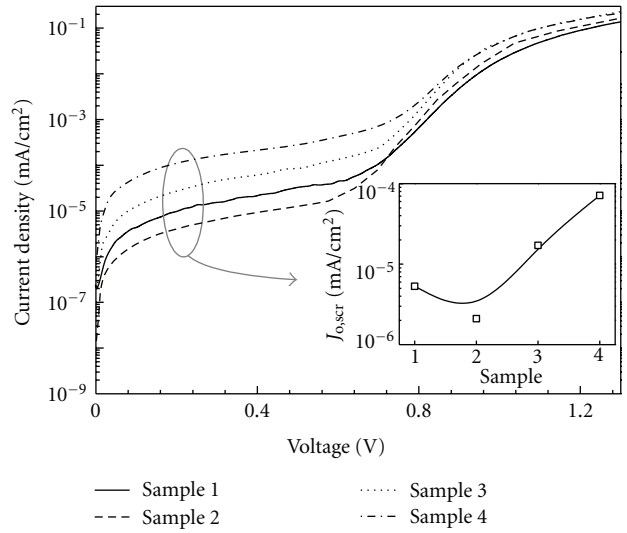

Figure 5: Far forward bias dark J-V characteristics for a-Si thin film solar cells at various B_2H_6 flow rates.

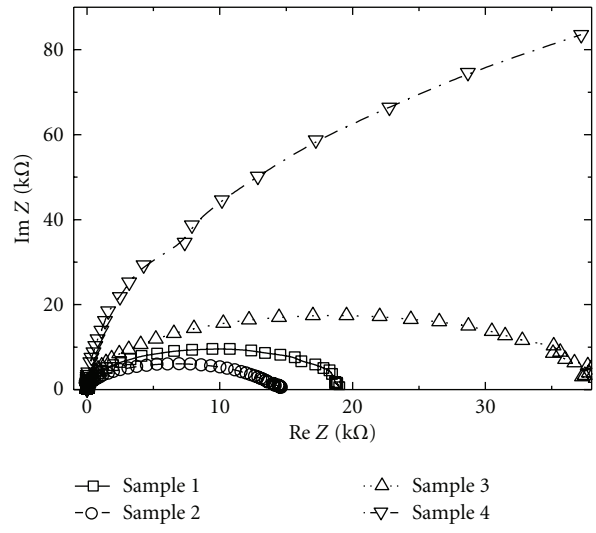

Figure 6: Cole-Cole plot of a-Si solar cell having different p-type layers, under zero DC bias.

in V_{oc} and FF of the highly doped p type window layer with an increase in the saturation current density of the space-charge region [10, 11].

The saturation current density, J_o, obtained by fitting the dark I-V curve to the two diode model in the space-charge region and in the quasineutral region. The space-charge region is mostly affected by the interface, while the quasineutral region is influenced by the bulk. Figure 5 shows dark J-V characteristics of a-Si thin film solar cells at different boron atoms bonding coordinations. With a further increase in three- and fourfold coordinated bonding, the saturation current of a-Si thin film solar cells increased from 2.10×10^{-6} to 7.14×10^{-5} mA/cm^2. It may also be due to doping-induced defects. Increase of the saturation current indicates increase in carrier recombination which can be related to the decrease in V_{oc} as well as FF. In order to investigate this following impedance spectroscopic measurements have been performed.

4.3. Effect of B_2H_6 Doping on p/i-Interface Capacitance. Figure 6 shows the Cole-Cole type plot for the measured impedance (Z) of the cell under 10 mV amplitude sinusoidal potential (AC field), where the Z is the complex AC impedance of the cell. The estimated AC parameters are shown in Table 4. The frequency of impedance and the maximum value of y-axis are given by

$$\omega = 2\pi f = \frac{1}{R_p C_p}, \qquad Z''_{max} = \frac{R_p}{2}. \tag{3}$$

Series resistance (R_s) can be obtained from intercept of the trace with real axis in the high-frequency region, and the total resistance, $R_s + R_p$ is indicated from the low-frequency region [12].

It shows the total diffusion capacitance (C_d) and resistance of the cell, however, as the observed change is because of the change in the doping of the p-type layer so we consider the change as because of the p/i depletion capacitance (C_1)

Table 2: Deposition condition of solar cell layers.

Layer	Gas ratio				Thickness (nm)	Power density (mW/cm^2)	Temp. (°C)	Pressure (mTorr)
	SiH_4	H_2	B_2H_6	PH_3				
p	1	5	0.05~0.5		15	50	175	200
i	1	1			350	42	180	200
n	1	5		1	25	70	200	200

Table 3: Characteristic properties of the layers of solar cell, where σ_{ph} ($S \cdot cm^{-1}$) is photo conductivity.

Layer	E_g (eV)	σ_d ($S \cdot cm^{-1}$) $\times 10^{-7}$	E_a (eV)	σ_{ph} ($S \cdot cm^{-1}$)
p	1.71, 1.68, 1.66, 1.63	5, 48, 107, 233	0.51, 0.51, 0.48, 0.43	
i	1.70	1×10^{-4}	0.80	1×10^{-8}
n	1.95	46×10^{5}	0.17	

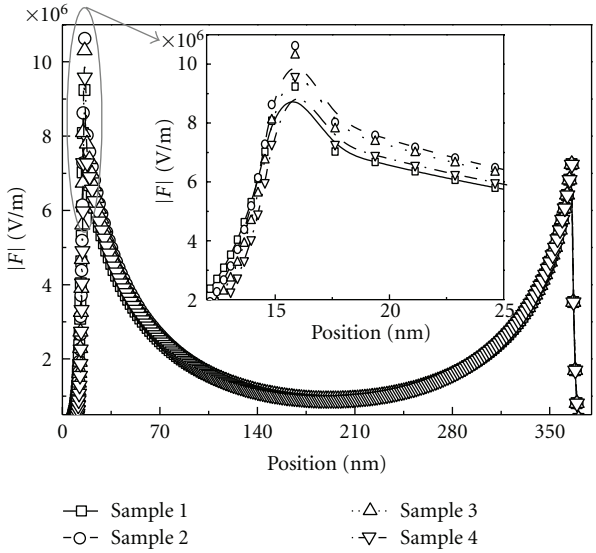

Figure 7: Electric field for a-Si thin film solar cell with different volume fraction of B_2H_6 in SiH_4.

and resistance (R_1). As can be seen from the model of the solar cell equivalent circuit model diagram Figure 1, that the depletion regions are in series, and parallel circuit is correlated with carrier generation and collection. Table 4 shows reduced capacitances at increased boron doping. It must be because of reduced capacitance at the p/i interface depletion region. One of the possibilities that most likely can happen is an increased width of the depletion region with increased B_2H_6 doing of the p-type layer. At higher doping of the p-layer, more holes will be available in this layer that will diffuse through the p/i interface and will create wider depletion region inside the i-layer. However for sample 2 the increase in capacitance has been observed. In spite of the lower doping-induced defects of sample 1, the higher V_{oc} and J_{sc} have been obtained on sample 2, because sample 1 has no sufficient electric field to collect of carriers.

The electric field profile in the p-i-n cell is plotted for different conditions in Figure 7. An increased defect leads to a reduced electric field in the p/i interface, which results in poorer carrier collection from this part of solar cell. The poorer collection is associated with an increased recombination rate [13]. The electric field results can be determine from ASA simulation. Since most of the input parameters describe the optoelectronic properties of individual layers, described in Table 3, it is reasonable to use the experimental data of such individual layers.

Figure 8(a) shows the impedance spectrum from -0.1 to -0.6 V in steps of -0.1 V under reverse bias conditions. It was observed that the impedance spectrum is nearly semicircular in shape under the zero and reverse bias conditions, which implies that the equivalent circuit of the device consists of a single *RC* network with a single time constant. The best-fit curves, obtained using *Z*-plot software, are also shown in the same figure. The obtained values of *R* and *C* are listed in Table 2. The radius of the semicircle increases with the increase in bias voltage as compared to that at zero bias demonstrating the bias dependence of resistance and capacitance values. Figure 8(b) shows the impedance spectrum under the forward bias (from 0.1 to 0.5 V) conditions where in contrast to the reverse bias, opposite behavior was observed. Here the radius of the semicircle decreases with increasing positive bias from its maximum value at zero bias. Another noticeable feature is the deviation from a semicircular shape particularly in the high-frequency regime with biasing. However, no scatter of the data is seen in the low-frequency regime.

From the impedance spectra, the p/i interface capacitance and resistance at different bias voltages were calculated. The *RC* network is composed by two types of capacitances and resistances. They are diffusion and transition capacitances (C_d and C_T) and resistances (R_d and R_T), respectively. C_d and R_d are due to the gradient of the charge density inside the device and the bulk resistance of the space charge region, respectively. R_T is the resistance due to recombination of free carriers in the space charge region and C_T is the space charge layer capacitance. To understand the origin and value of capacitance at different bias voltages, "C_1" is plotted against bias voltages in a logarithm scale for different diborane flow rate and is shown in Figure 9. It can be divided into three distinct regions, that is, one for $-0.6 < V < -0.1$ V and the other for $-1.0 < V < 0.4$ V and other for $V > 0.4$ V. In region I, that is, under reverse bias, the capacitance does not vary much with voltage which is the characteristic

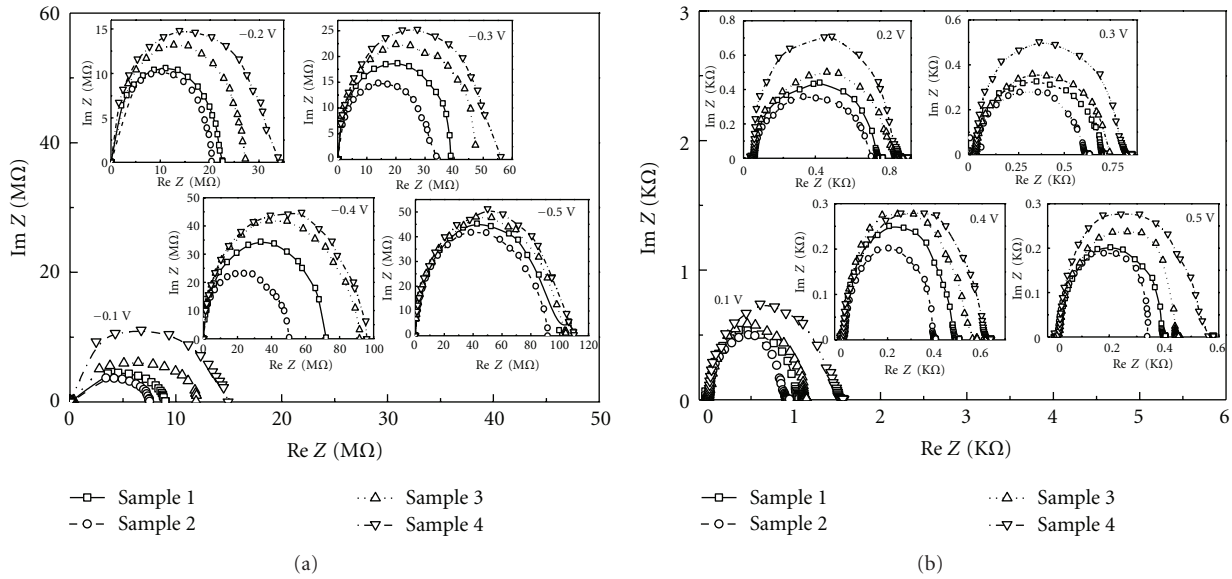

Figure 8: Cole-Cole plot of a-Si solar cell at different (a) reversed biases (-0.1 V ~ -0.5 V) and (b) forward biases (0.1 V $\sim$ 0.5 V) conditions.

Table 4: Parameter of impedance spectra in a dark a-Si thin film solar cell with different volume fraction of B_2H_6 in SiH_4 of p layer.

Sample	R_c (Ω)	Z_1		Z_2		Z_3		Z_4	
		R_1 (Ω)	C_1 (nF)	R_2 (KΩ)	C_2 (nF)	R_3 (Ω)	C_3 (nF)	R_4 (KΩ)	C_4 (nF)
1	8.75	201	248.7	21.1	0.29	18.1	24.5	19.4	281.4
2	8.74	183	261.4	21.1	0.29	18.4	24.7	14.3	294.6
3	8.75	458	200.0	21.1	0.29	18.1	24.7	39.7	227.4
4	8.75	981	189.2	21.1	029	18.0	24.8	68.0	214.2

Table 5: The values of diode ideality factor (n) and built-in potential (V_{bi}) of solar cell with different diborane flow rate of p-type layers.

Sample	Diode ideality factor (n)		Built-in potential (V_{bi})
	Dark I-V (scr region)	C-V (Region II)	
1	1.87	1.81	0.9929
2	1.70	1.69	1.0529
3	1.79	1.78	0.9609
4	2.04	1.95	0.9199

of the transition capacitance. We modified C-V curve to $1/C^2$-V plot. The intercept of this plot on the abscissa gives the value of $(V_{bi} - kT/q)$ which is shown in Table 5. By analyzing the second part, region II, of the C-V curve in the forward bias which is dominantly diffusion capacitance that increases exponentially with bias voltage. It can be utilized for the determination of diode ideality factor. To verify this value, dark I-V measurement has also been done on the device. From the slope of this curve, the diode ideality factor (n) was calculated for cells with the different p-type layers, which is shown in Table 5. It shows that the diode ideality factor increases from 1.69 to 1.95 [14]. Region III occurs because of the junction capacitance. Compared to the static characteristics, the AC characteristics have same tendency and mechanisms of p/i interface properties.

5. Conclusions

In amorphous silicon solar cells, p-type window layer strongly influences cell performance. As the different diborane flow rate, p-type layer and p/i interface properties change with cell performance. Mechanism of this phenomenon is explained by the changes in the three and fourfold coordinated boron atoms observed by XPS. The p/i interface properties were obtained from the static/dynamic characteristics. The DC characteristics were measured from dark/illuminated current-voltage curves, and the AC characteristics were determined from the impedance spectroscopy. The impedance spectroscopy technique is used to measure the capacitance of amorphous silicon solar cell of different diborane flow rate in p-type window layer. It has been shown

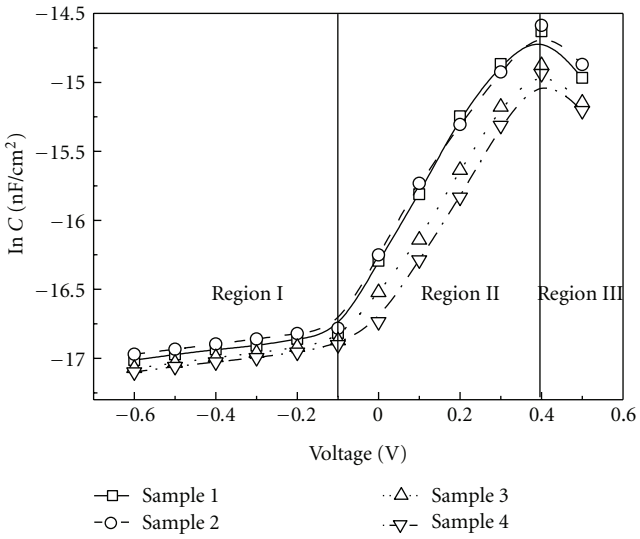

FIGURE 9: The measured capacitance (C_1) as a function of bias voltage in the p-i-n structure.

that the capacitance associated with different biasing can be utilized to gather information related with device such as built-in potential and diode ideality factor. The diode ideality factor, obtained impedance spectroscopy, was estimated and found to be almost equal to the current-voltage data.

Acknowledgments

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Research Article

Development of Well-Aligned TiO_2 Nanotube Arrays to Improve Electron Transport in Dye-Sensitized Solar Cells

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We fabricated well-aligned one-dimensional (1-D) titania nanotubes (TNT) on transparent conducting oxide (TCO) by anodization of Ti foil. Different lengths of TNTs were prepared by varying the applied potential (70 V) time, and we investigated the performance of these TNTs in dye-sensitized solar cells (DSSCs), transplanted onto a 6 μm TNP adhesion layer. The fabricated TNTs arrays (length 15 μm) photoelectrode showed 24% increased efficiency compared to the TNP photoelectrode of 17 μm thickness. We further investigated the performances of DSSCs for the TNTs (1 wt%) incorporated TNP photoelectrode and obtained 22% increased efficiency. The increased efficiency of the pure TNTs arrays and TNT-mixed TNP photoelectrodes was attributed to the directional electron movement of TNTs and light scattering effect of the TNT with the decreased rate of back electron transfer. The anodized and fabricated TNTs and DSSCs were characterized by X-ray diffraction (XRD), scanning electron microscopy (SEM), transmission electron microscope (TEM), and electrochemical impedance spectroscopy (EIS).

1. Introduction

The mesoporous nanostructured film of titanium dioxide (TiO_2) nanoparticles (TNPs) with anatase crystalline polymorph has been used as unique materials over the last two decades as an efficient photoelectrode material for dye-sensitized solar cells (DSSCs) [1–3]. However, the structural disorder or trap states of TNP led to the elongation of electron colleting path and ultrafast scattering of free electrons, which in turn increases the probability of recombination at the interface between TNP and electrolyte or dye to reduce electron collection efficiency [4].

The pioneering work of Mor et al. [5] has led to the recent application of well-ordered one-dimensional (1-D) titanium nanotube (TNT) arrays for DSSCs. TNTs has attracted enormous interest in DSSCs due to their directional electron movement, photoconversion efficiency of over 16.25% and quantum efficiency of over 80% under 320–400 nm illumination [6], incident photon-to-current conversion efficiency (IPCE) of the N719 adsorbed TNT photoelectrode was 70–80% at 450–650 nm wavelength, and the suppressed recombination with improved collection efficiency [7]. Based on the fabrication processes, TNT-DSSCs are classified into front-side illuminated DSSCs and back-side illuminated DSSCs. To fabricate the TNT arrays photoelectrodes of front-side illuminated DSSCs, Ti thin film was generally deposited to FTO glass by d.c. sputtering deposition [8] and sol-gel method [9], which only provide a very thin TNT film. However, for the development of efficient DSSCs, conventional thickness of the TNP layer is around 15 μm [4]. On the other hand, photoelectrodes of back-side illuminated DSSCs are fabricated by anodizing Ti foil and longer TNT arrays can be easily grown on Ti foil. Front-side illuminated DSSCs usually show improved light harvesting compared to the back-side illuminated DSSCs with the same thickness of nanotube arrays, because of the light absorption by the iodine electrolyte and light reflection by platinum (pt) counterelectrode for the latter

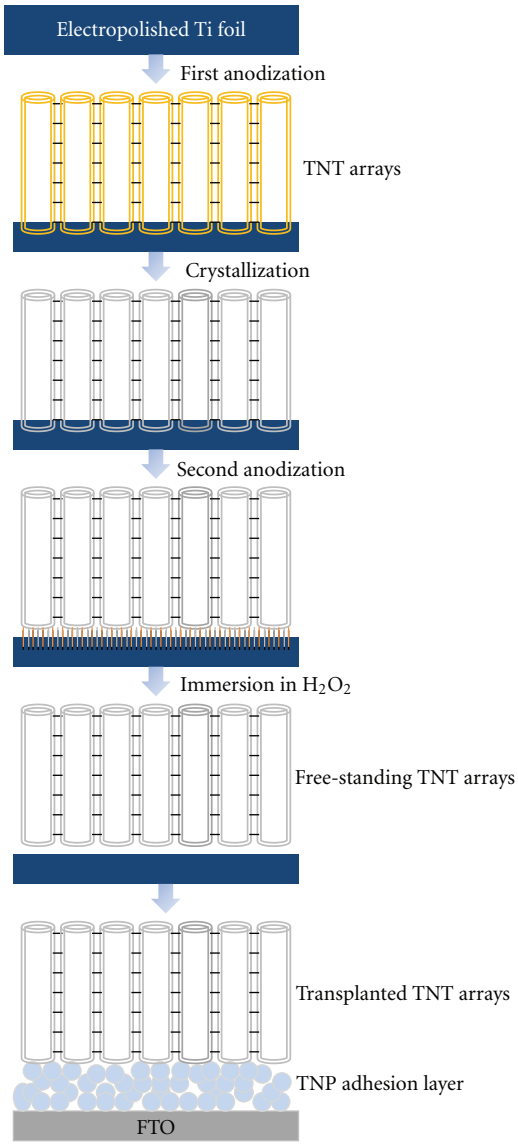


Figure 1: Schematic for the preparation of anodized TNT arrays, detachment, and transplantation onto TNP.

[10]. Therefore, for the development of efficient TNT-DSSCs, longer nanotube arrays with front-side illumination are a prerequisite. There are reports on the development of longer transplanted nanotube arrays onto fluorine doped tin oxide (FTO) for high efficient DSSCs [4, 11, 12].

Herein, we have investigated the performance of DSSCs based on the transplanted longer nanotube arrays for front-side illumination. Varying lengths of the nanotube arrays were transplanted onto the FTO by using a TNP adhesion layer and the performance was compared with the TNP-DSSCs. Moreover, performance of the TNT (1 wt%) incorporated into TNP photoelectrode was also investigated and compared. Figure 1 shows the schematic for the preparation of anodized TNT arrays, detachment, and transplantation onto TNP adhesion layer.

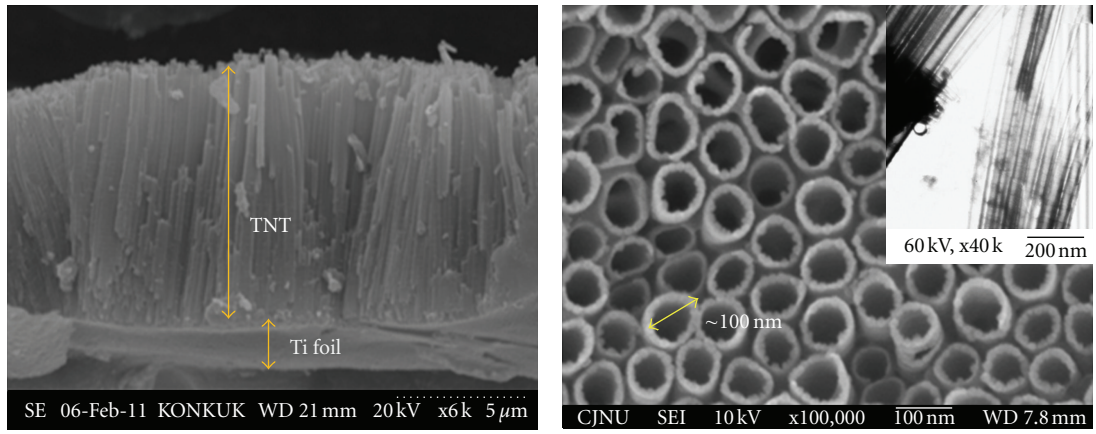
2. Experimental

2.1. Preparation of TNT. Titanium (Ti) foil (0.25 mm thickness, 99.7% purity, Aldrich, USA) was cleaned by using de-ionized (DI) water and acetone, and dried with N_2 purging. The cleaned and dried Ti foil was electropolished into the mixture solution of perchloric acid ($HClO_4$, 60%), butanol, and ethanol (1 : 6 : 9 v/v) for 3 min at −10°C with the applied potential of 20 V. Two-step anodic oxidation was carried out to prepare the well-ordered TNT nanotube arrays. Firstly, the electropolished Ti foil was anodized at a constant potential of 70 V in the ethylene glycol ($C_2H_6O_2$) solution containing ammonium fluoride (NH_4F) (0.38 wt%) and H_2O (1.79 wt%) at 20°C followed by thermal annealing at 500°C for 30 min in an electric muffle furnace (J-FM28, JISICO, Korea) in presence of air. Secondly, the first anodized Ti foil was further anodized in the same solution at a constant potential of 20 V for 3 h at 20°C. The detachment of the anodized TNTs arrays were carried out by immersion in 10% H_2O_2 solution for 24 h.

2.2. Transplanting of TNT Arrays. In order to prevent the recombination between FTO and electrolyte and for the attachment of TNTs arrays on FTO a 6 μm thick adhesion layer of titanium nanoparticles (TNP) (Degussa, P-25, Germany) paste was used. The TNP paste and 1 wt% TNT mixed TNP paste was prepared by the procedure reported elsewhere [2]. Detached TNT arrays were transferred onto the TNP layer on FTO by using tweezers. The transplanted TNTs arrays were then sintered at 500°C for 30 min in the presence of air.

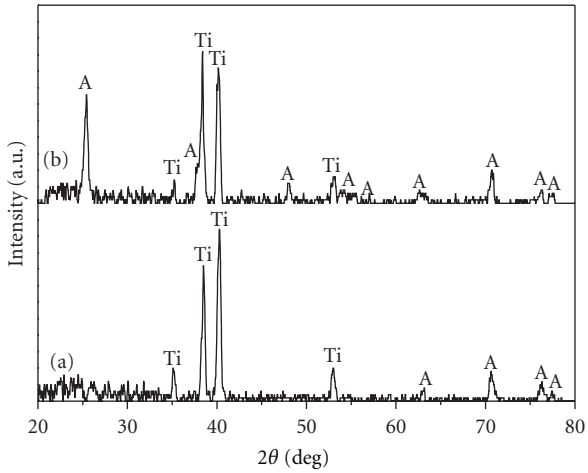
2.3. Preparation of the Photoelectrodes. TNTs arrays photoelectrodes were prepared by transplanting the different lengths of TNT (e.g., 8 μm, 11 μm, and 15 μm) onto the TNP adhesion layer. A 17 μm TNP photoelectrode was also prepared to compare the performance. Front side illumination of the DSSCs having the transplanted TNTs and TNP photoelectrodes were fabricated. For simplicity these cells were denoted as cell type-A. Moreover, the performance of the incorporation of TNTs into TNP photoelectrodes was also investigated, where the thickness of the purely TNP photoelectrodes was 7.5 μm and 13 μm, and 1 wt% TNT (8 μm) containing TNP photoelectrode was 8 μm. These cells were denoted as type-B.

2.4. Device Fabrication. The fabricated and sintered TNTs arrays, TNTs/TNP, and TNP photoelectrodes on FTO were immersed in the 0.4 mM ethanolic solution of *cis*-diisothiocyanato-bis(2,2′-bipyridyl-4,4′-dicarboxylato) ruthenium(II) bis-tetrabutylammonium (N719) dye for 24 h. The counter electrodes were prepared by spin coating of 5 mM ethanolic solution of chloroplatinic acid hexahydrate ($H_2PtCl_6 \cdot 6H_2O$) on FTO and sintered in an electric muffle furnace at 400°C for 20 min. The dye-loaded photoelectrodes (active area *ca.* 0.09 cm^2) and platinized counterelectrodes were sandwiched with 50 μm thick surlyn film as a spacer and sealing agent. The electrolyte solution having composition of



(a) (b)

Figure 2: SEM images of TNT arrays by anodic oxidation of electropolished Ti foil at a constant voltage of 70 V: (a) cross-sectional image of TNT arrays, (b) top view of the TNT arrays with inset showing the TEM images of TNT.



Ti: titanium
A: anatase

Figure 3: XRD pattern of TiO_2 nanotube arrays: (a) as-anodized TiO_2 nanotube arrays, (b) annealed TiO_2 nanotube (TNTs) arrays at 500°C.

0.5 M 1,2-dimethyl-3-propylimidazolium iodide (DMPII), 0.1 M LiI, 0.1 M I_2, and 0.5 M 4-*tert*-butylpyridine (*t*BP) in acetonitrile/valeronitrile (85 : 15 v/v) was injected into the cell through the drilled holes on the counterelectrode and sealed with a transparent scotch tape.

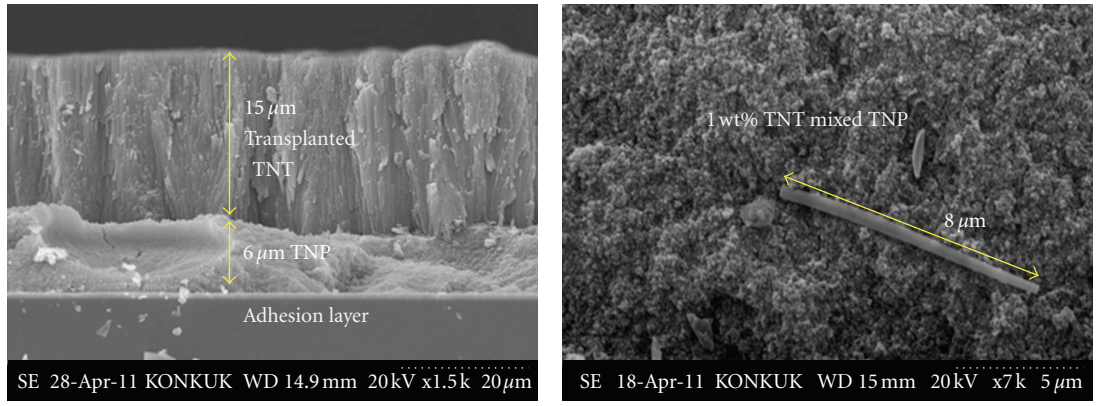
2.5. Instrumentation. Electropolishing and anodization of Ti foil were carried out by using a dc power supply (Sorensen, XHR-150/7, USA). The morphology and structure of the prepared anodized TNTs were characterized by using a scanning electron microscope (SEM, Hitachi S-3000N, Japan), a tunneling electron microscope (TEM, Jeol, JEM-1200 Ex II, Japan), and an X-ray diffractometer (Philips, X'pert, Netherland) using Cu K_α radiation of $\lambda = 0.15406$ nm in the scan range $2\theta = 20$–$80°$.

The simulated light AM 1.5 was generated by using a solar simulator (McScience, Polaronix K201, Korea) furnished with a 200 W Xenon lamp. A photovoltaic power meter (McScience, Polaronix K101 LAB20, Republic of Korea) was used to measure the current density-voltage (*J-V*) curves with the adjusted light intensity to 100 mWcm^{-2} (1 sun) by a standard mono-Si solar cell (PV Measurement Inc, PVM 396, USA), that is certified by the National Renewable Energy Laboratory (NREL, USA). Electrochemical impedance spectra (EIS) were measured by using an impedance analyzer (Zahner-Elektrik GmbH & Co. KG, IM6ex, Germany) under open circuit and dark conditions in the frequency range of 1 MHz–1 mHz with the ac amplitude of 10 mV.

3. Results and Discussion

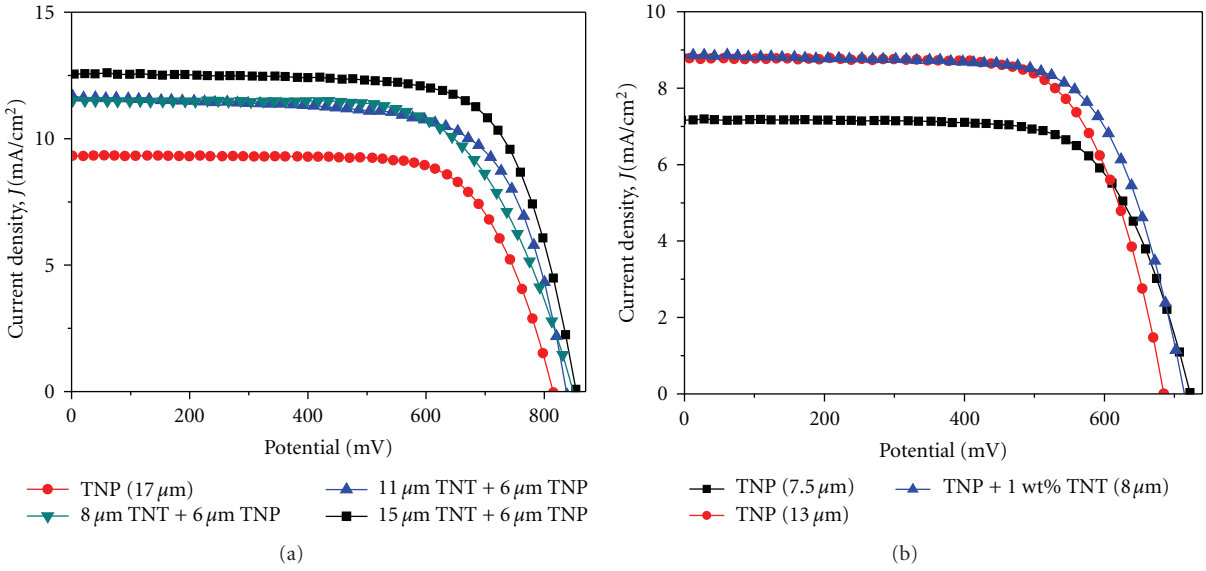
Figure 2 shows the cross-sectional and top-view SEM images of the TNTs arrays on Ti foil obtained by anodic oxidation. Well-ordered TNT arrays were grown successfully onto Ti foil with an average tube diameter and wall thickness of *ca*. 85 nm and 10 nm, respectively. The top view of the SEM image indicated the formation of closed packed and well-ordered nanotube arrays. Inset of Figure 2(b) shows the HRTEM images of the TNTs with the tube diameter ~85 nm that clearly correlated with the SEM data. Figure 3 shows the X-ray diffraction (XRD) pattern of the anodized Ti before and after sintering. This demonstrated that before annealing most of the XRD peaks arose from the Ti due to the amorphous phase of TiO_2 nanotube. After annealing at 500°C for 30 min, the number of peaks and the intensity of anatase polymorph of TiO_2 nanotube increased due to phase transition from amorphous to crystalline.

Figure 4 shows the cross-sectional SEM image of transplanted TNT arrays on FTO and top view of 1 wt% TNT-mixed TNP photoelectrode. The 6 μm thick TNP adhesion layer was used for transplanting TNT arrays. Electrons should pass through the adhesion layer to reach the FTO.



(a) (b)

Figure 4: Scanning electron microscopic images (SEM): (a) cross-sectional image of transplanted TNT onto TNP, and (b) top view of 1 wt% TNT-mixed TNP photoelectrode.



(a) (b)

Figure 5: Current density-voltage (J-V) characteristics of different DSSCs of cell type-A (a) and cell type-B (b).

Although the thickness of adhesion layer in our experiment is too thick for efficient electron movement, the thickness of the adhesion layer should be very low. Figure 4(b) clearly demonstrated the TNTs (1 wt%) incorporated TNP photoelectrode.

The current density-voltage (J-V) characteristics and parameters based on the different types of photoelectrodes (type-A, and type-B) are summarized in Figure 5 and Table 1. The photovoltaic performance of the transplanted TNT-based DSSCs increased by increasing the lengths of TNT that is mainly responsible for increasing the short circuit current density (J_{sc}). The highest J_{sc} of 12.56 mA/cm^2 was observed for the 15 μm transplanted TNT photoelectrode, while the J_{sc} for the 17 μm TNP film was 9.32 mA/cm^2. The J_{sc} of the shorter transplanted TNTs (8 μm and 11 μm) were also higher than the J_{sc} of 17 μm TNP film. This improved J_{sc} of the TNT-array-based DSSCs was attributed to ultrafast and directional electron movement, curtail electron diffusion length, and the light scattering effect [13]. In order to investigate the effect of the anodized TNT on to the TNP photoelectrode, we have further developed DSSCs of type-B. Current density-voltage results demonstrated that the 1 wt% anodized TNT-mixed TNP photoelectrode showed the improved photovoltaic performance compared to the TNP photoelectrode of 7.5 μm and 13 μm thickness. The improved performance of the 1 wt% TNT mixed TNP photoelectrode was mainly for the 24% and 1.13% increased of J_{sc} compared to the two different TNP film, respectively that is assumed to be the responsible for the mentioned physical properties of TNTs.

The kinetics of the electron transfer processes at transplanted TNT arrays photoelectrode|electrolyte, TNP photoelectrode|electrolyte, and 1 wt% TNT-mixed TNP photoelectrode|electrolyte interfaces were studied by electrochemical impedance spectroscopy (EIS). The impedance spectra exhibited in the form of Bode phase plot and

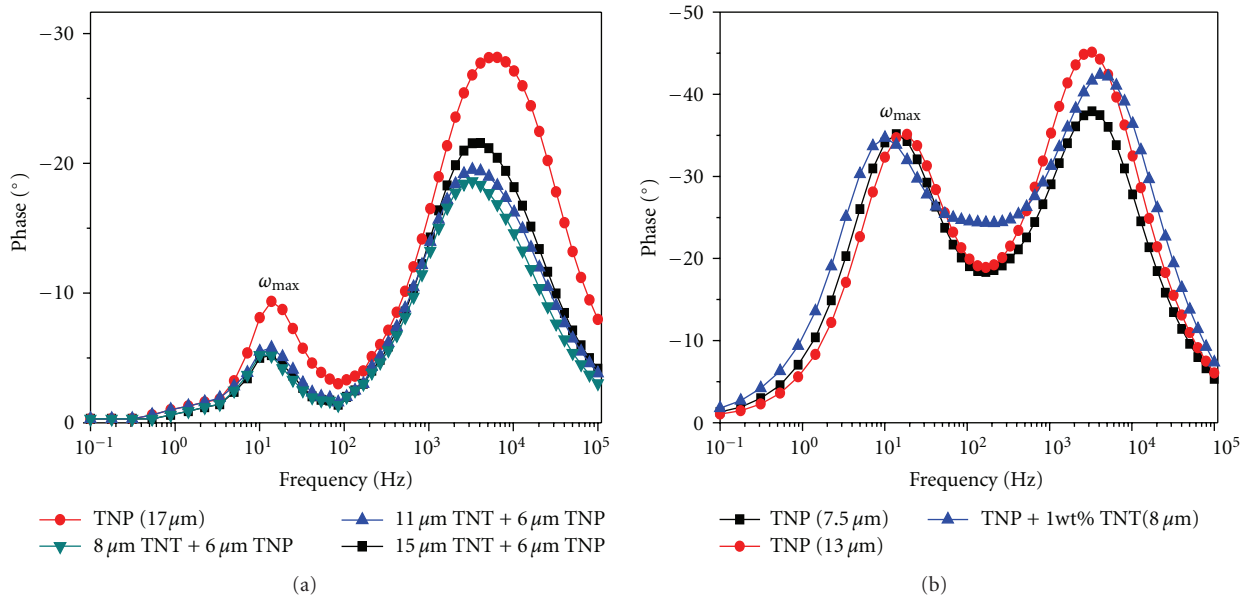


Figure 6: Bode plots from electrochemical impedance measurement of DSSCs under dark conditions of (a) cell type-A, and (b) cell type- B.

Table 1: Photovoltaic and kinetic parameters of cell type-A, and cell type-B based DSSCs.

DSSCs	Photoelectrode	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	η (%)	$k_{T/E}$ (S^{-1})
Cell type-A	TNP (17 μm)	9.32	815	71.75	5.45	13.7
	TNT (8 μm) + TNP (6 μm)	11.50	848	66.57	6.50	11.2
	TNT (11 μm) + TNP (6 μm)	11.68	837	68.79	6.72	11.2
	TNT (15 μm) + TNP (6 μm)	12.56	853	71.76	7.70	11.2
Cell type-B	TNP (7.5 μm)	7.16	722	70.23	3.63	24.7
	TNP (13 μm)	8.78	684	70.45	4.23	32.4
	TNP + 1 wt% TNT (8 μm)	8.88	714	69.92	4.44	18.6

the calculated kinetic information of the cells of type-A and type-B electrodes are summarized in Figure 6 and Table 1. The high frequency peak corresponds to the charge transfer at the Pt-counter electrode, and the uncovered FTO|electrolyte interface; the mid-frequency peak corresponds to the diffusion-recombination at the photoelectrode; the low-frequency peak is related to the ionic diffusion process in the electrolyte, which is often merged with the mid-frequency peak as in our data.

The rates of back electron transfer to I_3^- at the interfaces of different photoelectrodes|electrolyte ($k_{T/E}$) were estimated from the mid-frequency peak according to the following equation [14]:

$$\omega_{max} = k_{T/E}. \quad (1)$$

For the DSSCs of cell type-A, the use of TNT arrays photoelectrode decreased the rate of back electron transfer ($k_{T/E}$) compared to TNP photoelectrode, and our results demonstrated the $k_{T/E}$ values were independent of the nanotube arrays lengths up to 15 μm. The decrease of the back electron transfer using TNTs arrays photoelectrode increases the open circuit potential (V_{oc}) for every case of TNT arrays photoelectrodes, and maximum 38 mV increase of V_{oc} was observed for 15 μm TNT arrays. On the other hand, the $k_{T/E}$ value of the TNT (1 wt%) mixed TNP photoelectrode was decreased from 32.4 S^{-1} to 18.6 S^{-1} compared to 13 μm TNP photoelectrode and thereby increased the V_{oc} of 30 mV.

4. Conclusion

We have applied different lengths of TiO_2 nanotube arrays to front-side illuminated DSSCs with a transplanting process onto a TNP adhesion layer. The performance of the TNT transplanted DSSCs was compared with the TNP-based DSSCs. Front-side illuminated DSSCs based on transplanted TiO_2 nanotube arrays had a better efficiency of 24% than the TNP DSSCs. Further investigation of the 1 wt% TNTs incorporated TNP photoelectrode (8 μm) showed an increased efficiency of 22% and 5% compared to 7.5 μm and 13 μm TNP photoelectrodes, respectively. Therefore, the transplanting process of TNTs along with the incorporation into TNP photoelectrode was an effective method to improve the efficiency of DSSCs and had great potential, which can overcome the limitation of TiO_2 nanoparticle structure.

The DSSCs performance is expected to improve by reducing the thickness of the adhesion layer and making clean surfaces of TNTs arrays. The transplanting TiO_2 nanotube arrays were effective to increase the power conversion efficiency of DSCs.

Acknowledgments

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Research Article

Effect of High-Temperature Annealing on Ion-Implanted Silicon Solar Cells

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P-type and n-type wafers were implanted with phosphorus and boron, respectively, for emitter formation and were annealed subsequently at 950~1050°C for 30~90 min for activation. Boron emitters were activated at 1000°C or higher, while phosphorus emitters were activated at 950°C. QSSPC measurements show that the implied V_{oc} of boron emitters increases about 15 mV and the J_{01} decreases by deep junction annealing even after the activation due to the reduced recombination in the emitter. However, for phosphorus emitters the implied V_{oc} decreases from 622 mV to 560 mV and the J_{01} increases with deep junction annealing. This is due to the abrupt decrease in the bulk lifetime of the p-type wafer itself from 178 μs to 14 μs. PC1D simulation based on these results shows that, for p-type implanted solar cells, increasing the annealing temperature and time abruptly decreases the efficiency ($\Delta\eta_{abs} = -1.3\%$), while, for n-type implanted solar cells, deep junction annealing increases the efficiency and V_{oc}, especially ($\Delta\eta_{abs} = +0.4\%$) for backside emitter solar cells.

1. Introduction

The formation of the emitter in fabricating solar cells is one of the critical processes in the solar cell fabrication process. The emitter is usually formed by diffusing the dopant atom into a silicon wafer surface. There are many ways in creating the emitter, including the standard diffusion process, ion implantation, and epitaxial growth. Of these methods, ion implantation, when applied to the solar cell fabrication, has many advantages compared to the conventional thermal diffusion method [1]. It does not require the etching of the phosphosilicate glass formed during the diffusion process or the additional edge isolation step. Compared to the thermal diffusion method, ion implantation also allows an excellent control over the doping profile. The doping profile can be controlled by modifying the dose or the acceleration during the implantation or by modifying the annealing step, which also acts as a drive-in step [2].

During implantation the implanted dopants are bombarded into the silicon, and this process produces point defects within the lattice. These defects are in the form of Si self-interstitials, created when the ions collide with the Si atoms which then are displaced from their equilibrium positions [2–8].

This damage requires repairing, which is done by performing a postimplant thermal process. This thermal process also activates the dopant ions by establishing them on substitutional sites where they are able to contribute holes (electrons) to the valence (conduction) band [2, 3].

The annealing condition has a major effect on ion-implanted solar cells because they control the activation and the diffusion profile of the ion-implanted dopants. The activation part of the annealing is more critical since the inactivated dopants act as recombination sites, reducing the minority carrier lifetime and decreasing the V_{oc} of solar cells. The previous studies have created solar cells with minimum annealing. The annealing was done at the least after the ions were activated in other studies to form a shallow emitter, which is thought to increase the J_{sc} due to their higher quantum efficiency at short wavelengths.

In this study, however, the ion-implanted emitters were annealed even after they were activated to create deep junctions. Since the total concentration of the dopants is fixed for implanted emitters, high-temperature or long-time annealing lowers the peak concentration at the surface as well as increasing the deep junctions. Lowering of the peak concentration should decrease the surface recombination, increasing the V_{oc} as well as the quantum efficiency at short wavelengths. P-type and n-type wafers were implanted with phosphorus and boron, respectively, for emitter formation and were annealed subsequently to see the effect of the deep junction annealing.

2. Experiments

Phosphorus ions were implanted with an acceleration voltage of 30 keV and a dose of $1e15\,\text{cm}^{-2}$ on p-type c-Si wafers 675 μm thick and a resistivity of 8~12 $\Omega\cdot$cm. Boron ions were implanted with an acceleration voltage of 40 keV and a dose of $5e15\,\text{cm}^{-2}$ on n-type c-Si wafers 675 μm thick and a resistivity of 4~7 $\Omega\cdot$cm. The samples were annealed at 950°C, 1000°C, and 1050°C with varying time with 30, 60, and 90 min. The sheet resistances of the samples were measured using a 4-point probe, the doping concentration profile was measured using secondary ion mass spectrometry (SIMS), and the implied V_{oc} at 1-sun (using the minority carrier lifetime) was measured using quasi-steady-state photoconductance (QSSPC). Dark current-voltage (Dark IV) measurement was done on diode samples with metal contacts that were evaporated on both sides of the wafer. For the p-type wafers, 20 nm of Ni and 200 nm of Ag were evaporated on phosphorus emitters and 20 nm of Ti and 200 nm of Al on the bulk side. For the n-type wafers, 200 nm of Ag was evaporated on boron emitters and 20 nm of Ti 200 nm of Al was on the bulk side. While the samples for measuring the sheet resistance, SIMS, and Dark IV were implanted on only one side, the samples for measuring QSSPC were implanted on both sides and SiN_x was deposited on each side using plasma-enhanced chemical vapor deposition (PECVD). Bare p-type and n-type wafers were also heated with the same annealing conditions to measure the change in their bulk lifetimes.

Using the measured data from the experiments above, PC1D was used to simulate their effect on solar cells. Three types of simulations were done. First, p-type wafers were simulated with phosphorus emitters in the front side of the wafer and boron back surface fields (BSF) in the back. Secondly n-type wafers were simulated with boron emitters in the front and phosphorus BSF in the back. Lastly, n-type wafers were simulated with phosphorus front surface fields (FSF) in the front and boron emitters in the back.

3. Results and Discussion

A SIMS profile of the boron-implanted emitters was taken (shown in Figure 1) and shows that when the annealing is done at 950°C for 30 min, there is a spike in the doping profile, which decreases but remains slightly when annealing

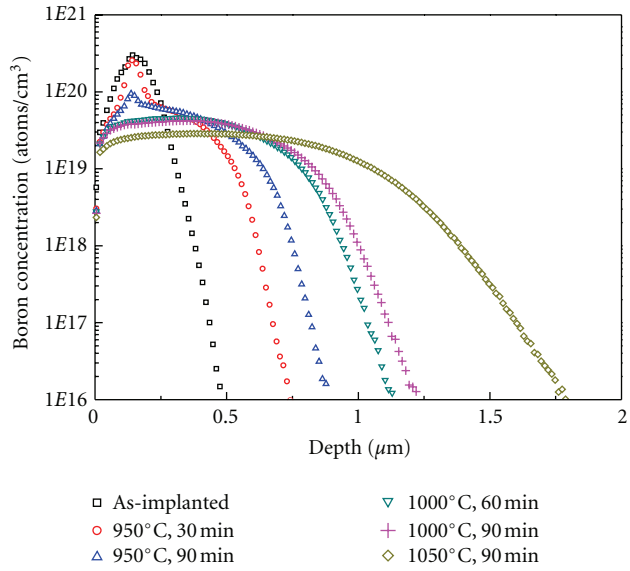

Figure 1: SIMS profiles of boron-implanted emitters as a function of annealing conditions.

is carried on for 90 min, but remains slightly. Because the position of the spike corresponds to the peak of the as-implanted doping profile, the spike can be assumed to be boron clustered formed during the initial stage of the annealing. These clusters are known to be immobile and electrically inactive [4]. The spike disappears when the temperature is increased to 1000°C in this study. This disappearance follows the literature that, while boron clusters start to dissolve at 800°C, the more stable ones require long-time or high-temperature anneals [5]. This implies that the deep junction annealing for the boron-implanted emitter starts at 1000°C. The same result can be seen by comparing the measured and the calculated R_{sheet} (sheet resistance) of the boron emitter (in Figure 2). The horizontal axis is aligned in the order of the total heat during the annealing. The measured R_{sheet} was obtained using a 4-point probe and represents only the activated boron ions, because only the activated ions contribute to the amount of the majority carriers. The calculated R_{sheet} was calculated by using SIMS profiles and the Irvin curve [4]. The mobility of the electrons and holes at each depth was calculated according to the doping profile [5]. Since the calculated R_{sheet} is based on all the implanted boron ions in the SIMS profile it represents the sheet resistance when the activation is complete. The measured R_{sheet} starts with 47.2 $\Omega/\square$ when the annealing condition is 950°C at 30 min, 12.1 $\Omega/\square$ larger than the measured R_{sheet}. The measured R_{sheet} becomes lower than the calculated R_{sheet} when the annealing condition is increased to 1000°C, when the measured R_{sheet} decreases abruptly from 47.2 $\Omega/\square$ to 38 $\Omega/\square$ and then saturates. This complies with the dissolving boron clusters shown in the SIMS profile. When the boron clusters are not activated, there are insufficient mobile carriers and the measured R_{sheet} is larger than the calculated R_{sheet}.

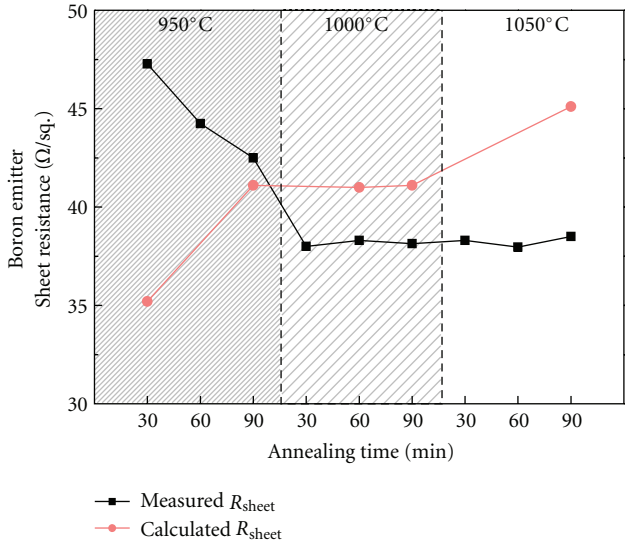

Figure 2: Measured and calculated sheet resistance of boron-implanted samples with different annealing conditions.

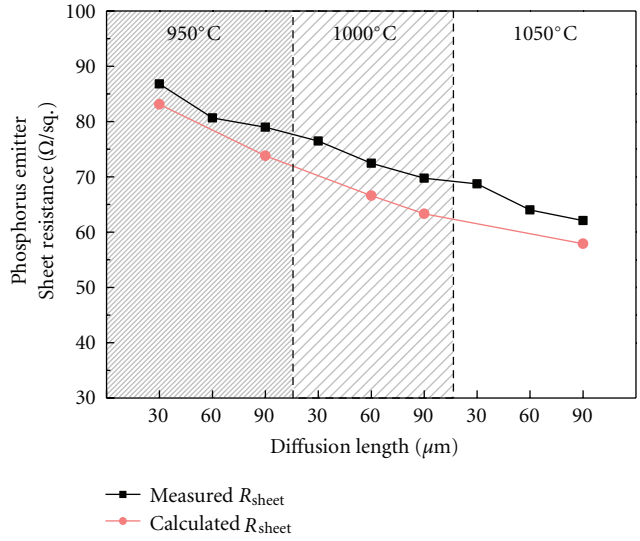

Figure 4: Measured and calculated sheet resistance of phosphorus-implanted samples with different annealing conditions.

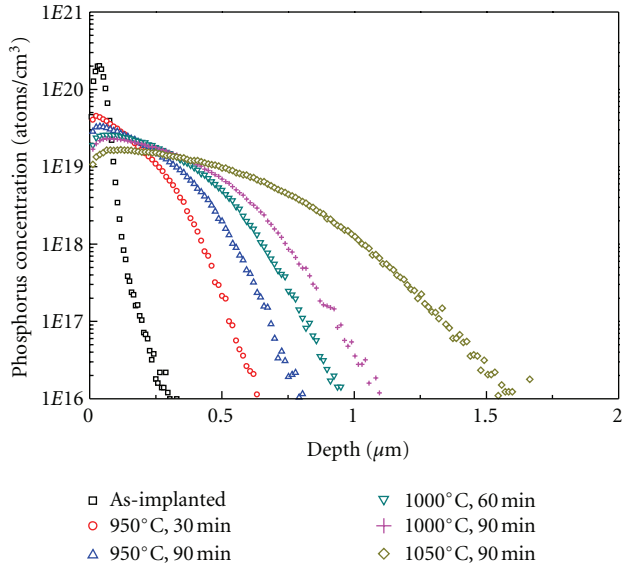

Figure 3: SIMS profiles of phosphorus-implanted emitters as a function of annealing conditions.

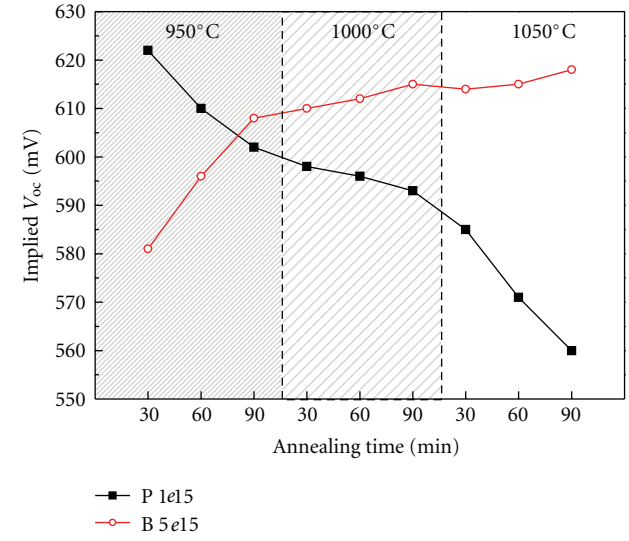

Figure 5: Implied V_{oc} of ion-implanted samples with different annealing conditions measured using QSSPC.

The case of the phosphorus-implanted emitters shows a different trend from the boron emitters. The SIMS profile (Figure 3) of the phosphorus emitters has no spike in any of the profiles. The measured R_{sheet} and the calculated R_{sheet} also follow the same trend in Figure 4. This indicates that the phosphorus-implanted emitter can be assumed to be activated at 950°C. The steady decrease of both the measured and calculated R_{sheet} is due to the increase in the electron mobility as the doping concentration changes with annealing conditions. The implanted phosphorus dopants act as scattering points for the electrons, lowering their mobility when the dopant concentration is high. The mobility of the electrons increases because the average dopant concentration falls as the annealing condition becomes higher or longer. This is why the R_{sheet} of the phosphorus-implanted emitter decreases although the total amount of the phosphorus concentration does not change. The R_{sheet} of the boron emitter does not show this trend because holes, the majority carriers in boron emitters, are not affected by the boron concentration as strongly as the electrons in the phosphorus emitters [5, 6].

Figure 5 shows the implied V_{oc} of the ion-implanted samples from QSSPC. The implied V_{oc} of the boron emitters increases about 30 mV at 950°C when the damage from the implantation is being annealed and about 15 mV more during the deep junction annealing at 1000°C and 1050°C. The increase of the implied V_{oc} at the high temperatures shows

that the deep junction annealing after the activation reduces the recombination as the doping concentration becomes lower as the annealing proceeds [7]. However, the implied V_{oc} of the phosphorus emitters continuously decreases about 60 mV even though the implanted phosphorus ions are already activated.

The J_{01} of the boron and phosphorus emitters (in Figure 6) with different annealing conditions, measured using Dark IV, supports the implied V_{oc} results. As the graph shows, J_{01} of phosphorus emitters increases when it is deep junction annealed after the activation. The J_{01} of boron emitters shows an opposite result, decreasing abruptly during the activation at 950°C and moderately during the deep junction annealing at higher temperatures. As written above, the decrease of the J_{01} during the deep junction annealing is linked to the decrease of the concentration of boron. Higher annealing temperatures and longer times will diffuse the boron more deeply into the wafer as shown in the SIMS profile (in Figure 1). The concentration of boron near the front surface decreases, which leads to a lower front surface recombination velocity (FSRV), which in turn reduces the J_{01}. The increase of the J_{01} for the phosphorus emitters is not due to the recombination in the emitter but the effect of the bulk lifetime.

Figure 7 shows the result of heating bare p-type and n-type wafers with the same conditions as the postimplantation annealing, showing the change in the bulk lifetime according to the annealing conditions. As can be seen, the bulk lifetime of both types of wafers decreases when annealing is done for a long time. While the bulk lifetime of n-type wafers decreases about 40 μs during the annealing process, the bulk lifetime of the p-type wafers decreases over 150 μs. This abrupt decrease of bulk lifetime in p-type wafers is the cause of the drop of the implied V_{oc} in Figure 5. The implied V_{oc} decreases when the J_0 of the sample increases as shown by the formula below

$$J_0 = qn_i^2\left(\left(\frac{D_e}{L_eN_A}\right)_{\text{bulk}} + \left(\frac{D_h}{L_hN_D}\right)_{\text{emitter}}\right),$$
$$V_{oc} = \frac{kT}{e}\ln\left(\frac{I_L}{I_0} + 1\right). \quad (1)$$

The implied V_{oc} is affected by the diffusion length of the bulk, as well as recombination in the emitter. While the high temperature of long-time annealing of the samples makes the junctions deeper and decreases the doping concentration of the surface leading to less Auger recombination and larger hole diffusion length (L_h in the emitter for p-type wafers), the bulk lifetime decreases far abruptly and hence J_0 will be dominated by the electron diffusion length (L_e in the bulk) leading to the decrease of the implied V_{oc} as the annealing proceeds. For n-type wafers, however, the bulk lifetime decreases in a moderate way; this leads to an abrupt increase of implied V_{oc} at 950°C and a moderate increase at higher temperatures.

The dissimilarity in the bulk lifetime of the two wafer types comes from the capture cross-section difference in impurities [8]. Impurities, especially metal impurities, produce deep levels in the band gap which act as recombination

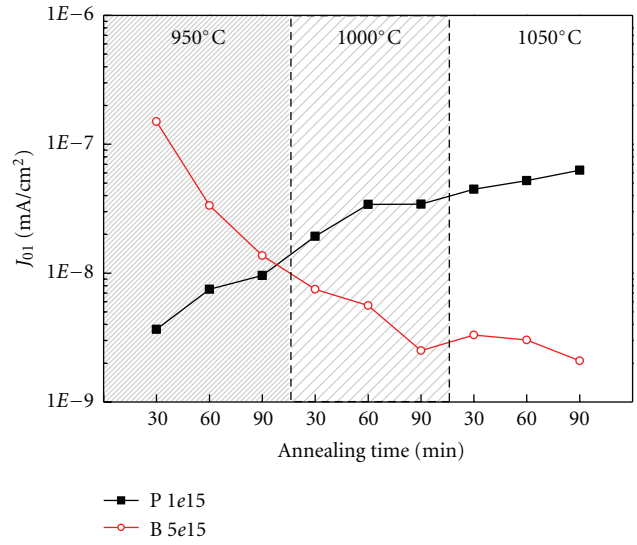

Figure 6: J_{01} of ion-implanted samples with different annealing conditions measured by Dark IV.

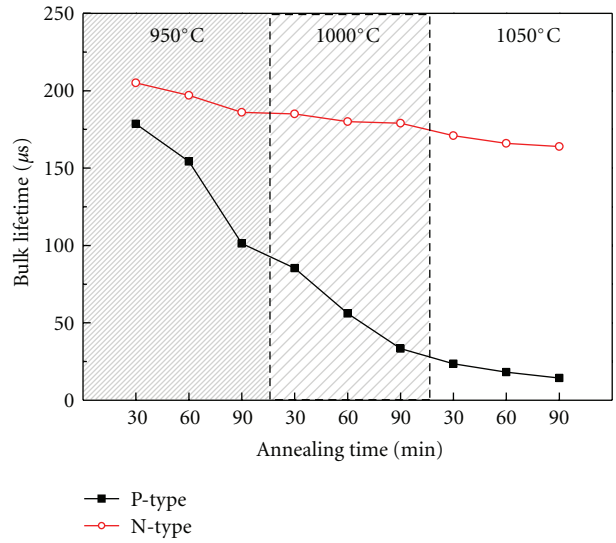

Figure 7: Bulk lifetime of bare wafers treated with annealing conditions measured using QSSPC.

sites according to the Shockley-Read-Hall model. The impurities, when occurring at either interstitial or substitutional lattice sites, act as donor of acceptor models, respectively, and alternate between charge states and neutral states capturing electrons or holes in the process. The capture cross-section for either electrons or holes differs greatly according to the impurity. For donor impurities the capture cross-section for electrons is much greater than that for holes and for acceptor impurities vice versa. When cooling after a high-temperature process, while donor impurities form a moderate concentration of interstitial centers, acceptor impurities form precipitates and only a small concentration of the impurities forms substitutional centers [9, 10]. Since the donor impurities capture electrons an order faster than

Table 1: Results of PC1D simulation using data in this study.

Wafer type	Annealing condition		J_{sc} (mA/cm^2)	V_{oc} (mV)	Efficiency (%)
	Temperatur (°C)	Time (min)			
P-type	1000	60	**34.7**	**638.2**	**18.4**
		90	34.4	632.1	18
	1050	90	33.5	616.2	17.1
N-type	1000	60	34.5	650.9	18.5
		90	34.8	652.1	18.6
	1050	90	**34.7**	**655.9**	**18.6**
N-type (with backside emitter)	1000	60	31.1	652.1	16.7
		90	31.4	652.6	16.9
	1050	90	**31.6**	**656**	**17.1**

holes, the lifetime of electrons, the minority carrier of the p-type wafers, decrease abruptly when the wafer is heated and cooled. This is the reason for the abrupt decrease of the bulk lifetime in Figure 7.

Using the data obtained in this study, a simulation of different wafer types was done using PC1D. The data used based on this study were the SIMS profiles, bulk lifetimes, and the front and back surface recombination velocities (according to the peak concentrations) [11, 12]. The background doping was set to be $1e16\,\text{cm}^{-3}$ for p-type wafers and $5e15\,\text{cm}^{-3}$ for n-type wafers. The reflectance of the antireflection coating used in the simulation had a weighted reflectance of 15.7%. The annealing conditions used in the simulation were 1000°C for 60 min, 1000°C for 90 min, and 1050°C for 90 min. The 950°C annealing conditions were not used because as seen from the sheet resistance, boron is insufficiently annealed at this temperature. In the simulations, both sides of the wafers were assumed to be ion implanted for p-type wafers (P-emitter, B-BSF), n-type wafers (B-emitter, P-BSF), and n-type wafers with backside emitters (B-emitter, P-FSF), respectively. The n-type wafers with backside emitters were simulated to test the effect of deep junction annealing for solar cells with emitters in the back as in interdigitated back contact (IBC) solar cells. The result of the simulation is shown in Table 1. Decrease in the bulk lifetime has a dominating effect for p-type wafers, resulting in a decrease in the efficiency as the annealing proceeds ($\Delta\eta_{abs} = -1.3\%$). Although the deep annealing lowers the doping concentration and hence reduc the Auger recombination and the surface recombination, it also abruptly lowers the bulk lifetime as shown above. The low bulk recombination reduces the L_e, which causes the quantum efficiency (QE) and the V_{oc} to deteriorate. This result shows that for the p-type implanted solar cells the annealing should be stopped when the activation is complete. For n-type solar cells, because the bulk lifetime only decreases slightly with the annealing, the deep junction annealing has a positive effect on the efficiency ($\Delta\eta_{abs} = +0.1\%$). The V_{oc} is increased, and the QE increases as well, leading to the increase of the J_{sc}. The deep junction annealing has the biggest effect in the third group, where the boron emitters are in the back of the n-type wafers ($\Delta\eta_{abs} = +0.4\%$). Since the emitters are in the back, recombination of the minority carriers needs to be reduced, which can be done by the deep junction annealing. These results show that deep junction annealing can be used to increase the efficiency of implanted n-type solar cells.

4. Conclusion

The effect of deep junction annealing after the activation was investigated for ion-implanted emitters. The SIMS profiles and the difference between the measured and the calculated R_{sheet} indicate that the boron emitters are activated above 1000°C, while phosphorus emitters are already activated at 950°C. Above 1000°C, the implied V_{oc} of boron emitters rises with annealing time and temperature about 15 mV even after the activation. The J_{01} also decreases, which indicates that the deep junction annealing decreases the recombination velocity by reducing the surface concentration. Deep junction annealing for the phosphorus emitters, however, decreases the implied V_{oc} and increases the J_{01} with annealing time and temperature. This effect is due to the decrease of bulk lifetime during the annealing at high temperatures, especially for p-type wafers. The dominating decrease in the bulk lifetime for p-type wafers indicates that for annealing implanted solar cells at high temperatures, n-type wafers should be used. Simulations using PC1D conclude this effect showing that for p-type implanted solar cells increasing the annealing temperatures or time decreases the efficiency ($\Delta\eta_{abs} = -1.3\%$). For n-type implanted solar cells, however, deep junction annealing reduces the recombination in the solar cell creating an increase in the efficiency ($\Delta\eta_{abs} = +0.1\%$), especially for n-type solar cells with emitters in the backside of the wafer ($\Delta\eta_{abs} = +0.4\%$). In summary, while the least annealing is suitable for p-type implanted solar cells, for the n-type implanted solar cells deep junction annealing even after complete activation can increase the efficiency.

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Research Article

Structural and Electrical Properties of Polysilicon Films Prepared by AIC Process for a Polycrystalline Silicon Solar Cell Seed Layer

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Polycrystalline silicon (pc-Si) films are produced by aluminum-induced crystallization (AIC) process for a polycrystalline silicon solar cell seed layer, and the structural and electrical properties of the films are analyzed. The used structure is glass/Al/ Al_2O_3/a-Si, and the thickness of Al_2O_3 layer was varied from 2 nm to 20 nm to investigate the influence of the Al_2O_3 layer thickness on the formation of the polycrystalline silicon. The annealing temperature and annealing time were fixed to 400°C and 5 hours, respectively, for the AIC process conditions. As a result, it is observed that the average grain size of the pc-Si films is rapidly smaller with increasing the thickness of Al_2O_3 layer, whereas the film quality, as defects and Hall mobility, was gradually degraded with only small difference. We obtained the maximum average grain size of 15 μm for the pc-Si film with the thickness of Al_2O_3 layer of 4 nm. The best resistivity and the Hall mobility was $6.1 \times 10^{-2}\ \Omega \cdot$ cm and 90.91 cm^2/Vs, respectively, in the case of 8 nm thick Al oxide layer.

1. Introduction

Crystalline silicon thin-film solar cells are an attractive alternative to the conventional bulk silicon solar cell due to its usability of the low-cost substrates like glass [1]. How to approach to such polycrystalline silicon (pc-Si) thin film solar cell on inexpensive substrate was also well presented [2].

To fabricate such pc-Si thin film solar cells, it is normally needed a good quality seed layer on the substrate. For growing crystalline silicon films on glass as a seed layer, aluminum-induced crystallization (AIC) process of amorphous silicon (a-Si) is a useful method which allows a large size grain on the foreign substrates [3].

Many approaches using AIC method are studied to produce pc-Si thin film as a seed layer on the glass substrate. The structure of a-Si/Al/glass is normally used for the AIC process of the pc-Si seed layer. The influence of the thicknesses and the ratio of Al and a-Si layer on the formation of the pc-Si seed layer was investigated [4], and some studies were on the structure with Al-oxide layer between Al/a-Si [5, 6].

Due to the layer exchange during the AIC process with the structure from a-Si/Al/glass to Al/pc-Si/glass, such AIC process for the pc-Si thin film seed layer formation is often called aluminum-induced layer exchange (ALILE) process. The Al-oxide layer, as well as the annealing temperature, is known to play a role in the ALILE process for the formation of the crystal orientation [5]. The preferential crystal orientation depending on the nature of the Al oxide layer was analytically investigated [7]. The most important properties for the pc-Si seed layer are the large grain and the low defects of the film. The formation of the large-sized grain using AIC was investigated in various ways [8], although the low defects films with small-sized grain showed also a possibility for pc-Si solar cells [9].

The Al-oxide layer between Al/a-Si controls the velocity of the crystallization process and the nucleation density and could lead to the formation of continuous pc-Si film [5, 6]. It could be necessary to investigate how much the Al-oxide layer could influence the grain size and defects in the film in the ALILE process.

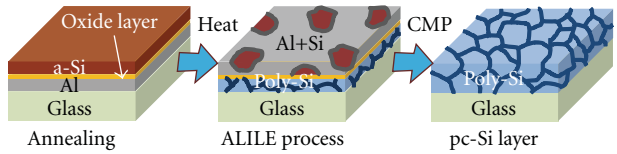


Figure 1: Schematic of the ALILE process.

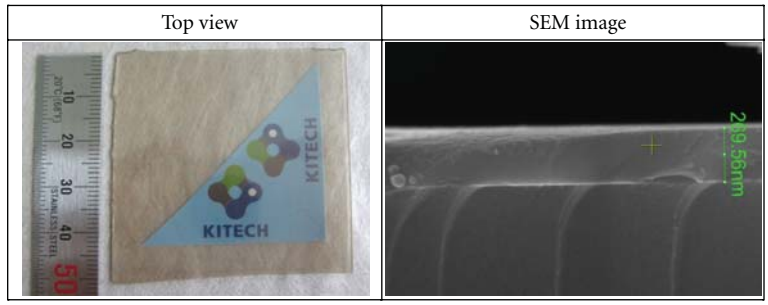


Figure 2: Images of pc-Si film after Al etching and ultrasonic vibration polishing.

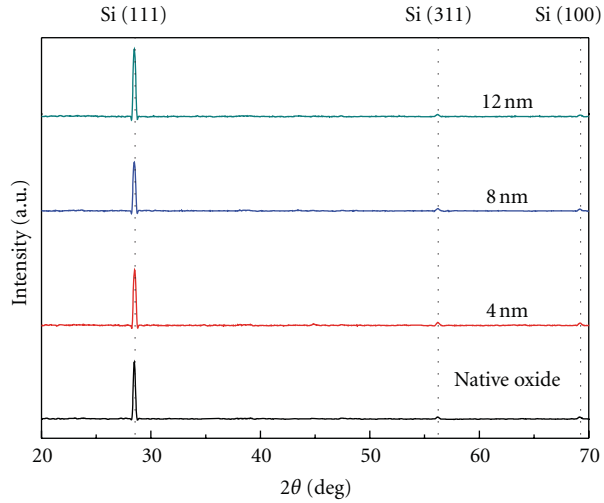


Figure 3: XRD spectra of the pc-Si films after etching and polishing.

Table 1: Experimental procedure of the ALILE process.

Deposition condition	Annealing conditions	Removed condition
(i) Aluminum layer: 300 nm using DC sputter	(i) Equipment: tube furnace	▷ Al layer:
(ii) Al oxide layer: 4~16 nm using RF sputter	(ii) Flow gas: N_2, 20 sccm	Diluted nitric acid, 70°C, 3 min
(iii) a-Si layer: 300 nm using RF-PECVD	(iii) Pressure: atmosphere	▷ Si layer:
(iv) Substrate: eagle 2000, 0.7 mm	(iv) Annealing: 400°C, 5 hours	(i) Amplitude: 60%
	(v) Sample size: 5 × 5 cm	(ii) Force: holder only (400 g)
		(iii) 15 min

Table 2: Electrical properties of pc-Si films produced by AIC process for various Al oxide layer thicknesses.

Sample	Resistivity [Ω·cm]	Carrier density [cm^{-3}]	Hall mobility [cm^2/Vs]
Native oxide	8.2×10^{-2}	8.7×10^{17}	87.62
4 nm	6.1×10^{-2}	1.2×10^{18}	83.54
8 nm	6.1×10^{-2}	1.1×10^{18}	90.91
12 nm	5.7×10^{-2}	1.3×10^{18}	85.12
16 nm	6.2×10^{-2}	1.5×10^{18}	68.78
20 nm	3.1×10^{-1}	1.6×10^{18}	14.14

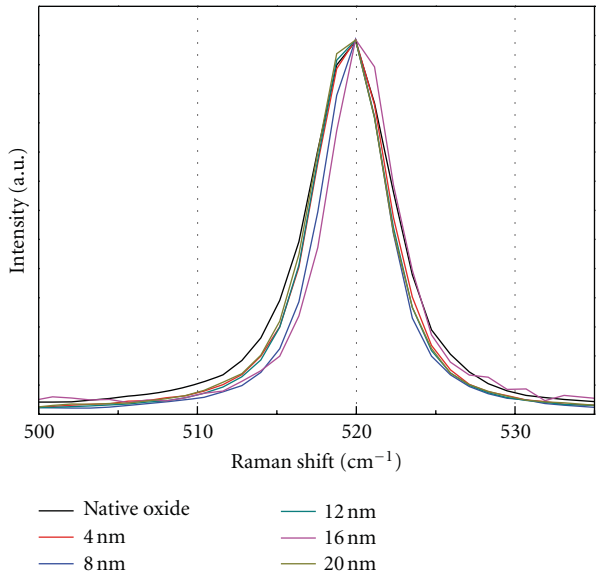


Figure 4: Normalized Raman spectrum of poly-Si films for various Al oxide layer thickness.

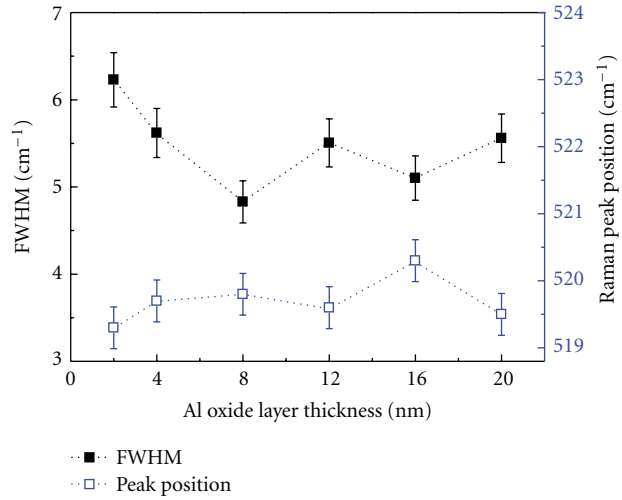


Figure 5: FWHM and Si peak of poly-Si films as a function of the Al oxide thickness.

In this work, we investigated the influence of the Al-oxide layer on the pc-Si seed layer, which are formed on the glass substrate by AIC process, depending on the thickness of the Al-oxide layer. And the structural and electrical properties of the poly silicon films are analyzed.

2. Experimental

For the AIC experiments, the glass/Al/Al_2O_3/a-Si structures were prepared with various Al_2O_3 film thicknesses from 2 nm to 20 nm. The Corning Eagle 2000 (strain point of 666°C), 0.7 mm glass with a size of 5 × 5 cm was used for the substrate. The Al layers were deposited on the glass substrate by a DC sputter. The thickness of Al layers was fixed to 300 nm. The Al oxide layers were prepared by a RF magnetron sputter for the thicknesses of 4~20 nm, whereas the very thin Al_2O_3 layer of ~2 nm was prepared by exposure of the deposited Al film to air for 2 hours at room temperature and the a-Si films were lastly deposited by PECVD method with the fixed thickness of 300 nm on the Al oxide layer.

The AIC process was, then, carried out at the fixed annealing temperature of 400°C and for the annealing time of 5 hours in a tube furnace for all samples. After annealing, the resulted upper layer including Al and Si-islands was removed by diluted nitric acid (H_3PO_4 + HNO_3 + CH_3COOH + H_2O) etching and by ultrasonic vibration polishing with 0.05 μm colloidal, sequentially. The AIC procedure is illustrated in Figure 1, and the detailed conditions for the sample preparation are shown in Table 1.

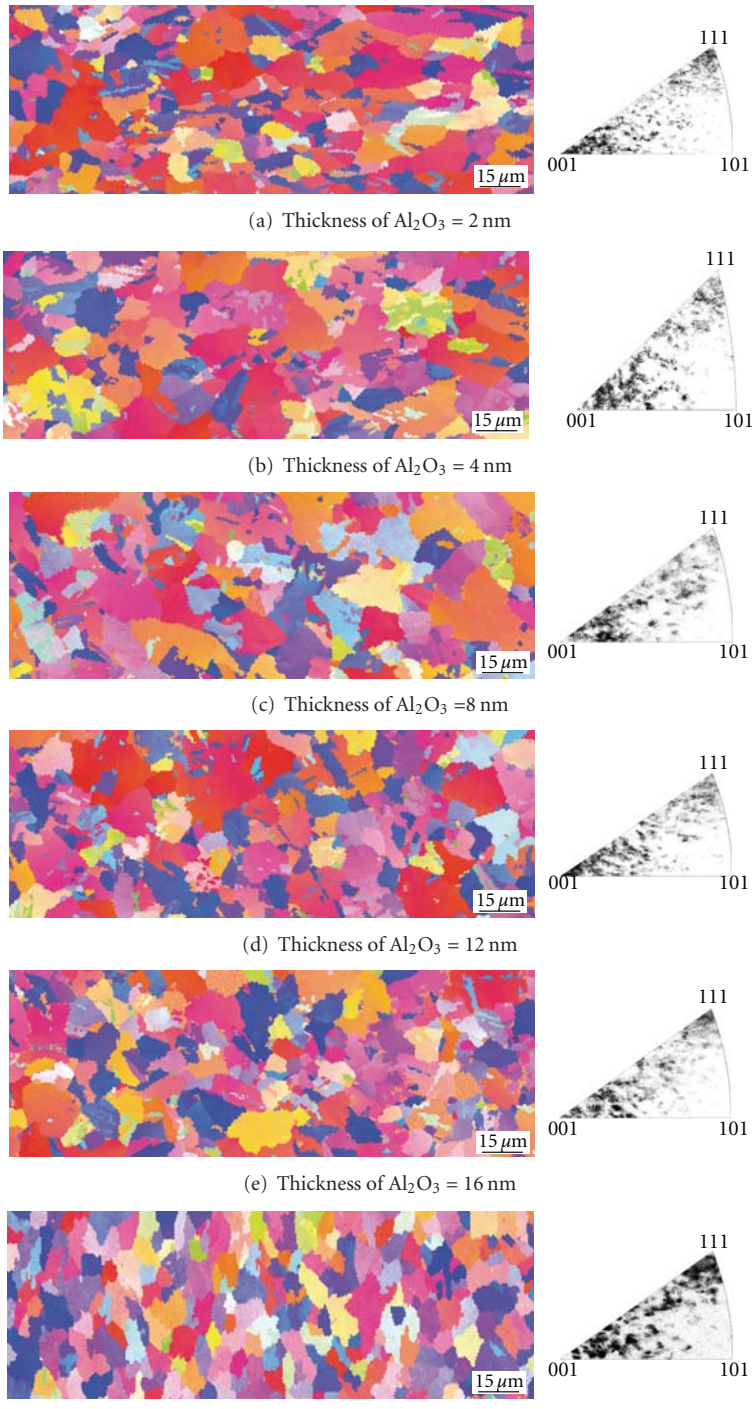
3. Results and Discussion

3.1. pc-Si Films after Removing the Al and Si Islands. Al and the Si islands are successfully removed by Al etchant etching and by ultrasonic vibration polishing from the AIC processed seed layer structure. The resulted structure is pc-Si/glass and the pc-Si film thickness was about 260 nm as shown in Figure 2.

The XRD data (Figure 3) shows the crystallinity of the pc-Si film. Only the silicon peaks with (111), (311), and (100) orientations are seen and Al was clearly removed.

3.2. Structural Properties of pc-Si Films

3.2.1. Crystallization. The crystallization of a-Si to pc-Si could be confirmed by Raman analysis. As the Raman spectra of pc-Si films in Figure 4 show, the peak positions for all samples are in the range of 520 ± 0.4 cm^{-1}. Due to the sharp and symmetric Raman spectra, it is apparent that the crystallization was fully and successfully executed in all the



(a) Thickness of Al_2O_3 = 2 nm

(b) Thickness of Al_2O_3 = 4 nm

(c) Thickness of Al_2O_3 =8 nm

(d) Thickness of Al_2O_3 = 12 nm

(e) Thickness of Al_2O_3 = 16 nm

(f) Thickness of Al_2O_3 = 20 nm

Figure 6: EBSD orientation maps and inverse pole figures of the polysilicon films in normal direction related to various Al oxide thicknesses.

samples. Figure 5 shows the Raman peak position and the full-width at half maximum (FWHM) values, respectively, for the crystalline Si TO phonon mode at 520 cm^{-1}. The peak widths are in the range of 4.7~6.3 cm^{-1} for the FWHM of all the samples. The difference between their FWHMs is so small that obvious tendency of the Al oxide layer thickness on the crystallization could not be shown. Nevertheless, the 8 nm thick sample showed the minimum FWHM value of 4.7 cm^{-1} with the smallest shift in the peak position, suggesting lowest defects.

3.2.2. Grain Size and Crystal Orientation. Using the Electron backscatter diffraction (EBSD) measurement, the grain size and the crystal orientation of the AIC pc-Si films are analyzed.

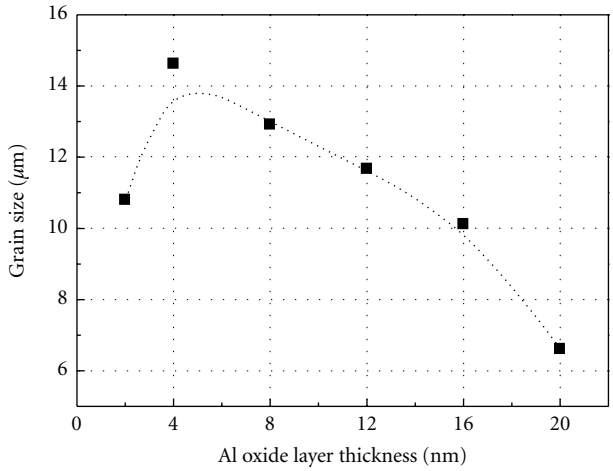


Figure 7: Average grain size extracted from EBSD data of the pc-Si films as a function of Al oxide layer thickness.

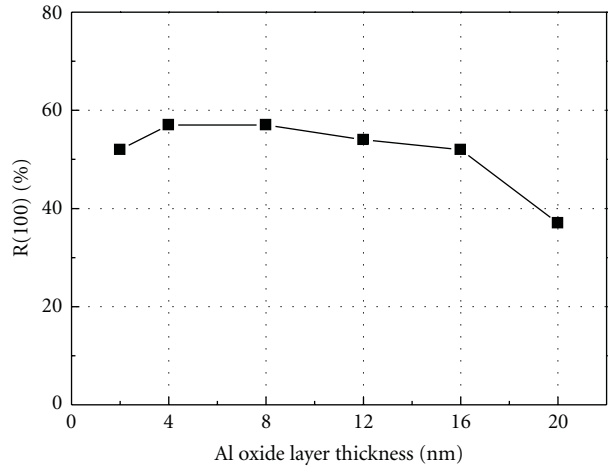


Figure 8: Fraction of preferential (100) orientation, R (100) from EBSD data of the pc-Si films, measured after [7] as a function of Al oxide layer thickness.

Figures 6(a)–6(f) show the EBSD orientation image maps and inverse pole figures for the samples with various Al oxide layer thicknesses. The colors red, blue, and green represent the (100), (111), and (101) Miller indices, respectively. The trend can be seen that the grain size of the pc-Si film gets smaller with the increased thickness of the Al oxide layer. It is also apparent that the volume fraction of the preferential (100) orientation in the pc-Si could be more obtained with the decreased thickness of the Al oxide layer.

In Figures 7 and 8, the calculated average grain size of the pc-Si films and the preferential (100) orientation R (100) after [7] are shown as a function of the Al oxide layer thickness. The optimum thickness of the Al oxide layer for the large grain could be in the near of 4 nm (Figure 7). And the optimum thickness of the Al oxide layer for the preferential (100) orientation could be in the range of 4~8 nm (Figure 8). For the case of 4 nm sample, we achieved an average grain size of 15 μm and the fraction of the preferential (100) orientation more than 58%.

3.2.3. Film Defects. To make extended defects visible, the samples were etched with diluted HF acid (HF + $K_2Cr_2O_7$ + H_2O) at room temperature for 3 seconds and the etch pits were analyzed by scanning electron microscopy (SEM). The quality and defects of the AIC pc-Si films are to see in the SEM images of Figure 9. The grains are well grown with AIC process, and the defects are so small that their boundary is not to be seen in the SEM images for all the samples. The boundaries between the grains could be observed only by EBSD analysis as shown in Figure 6. As consistent from the results of the Raman and EBSD analyses, the defects were larger and the film quality was lower with the increased thickness of the Al oxide layer.

3.3. Electrical Properties of pc-Si Films. As electrical properties of pc-Si films, we measured the resistivity, carrier density, and Hall mobility by a Hall effect measurement system.

The measurement results are shown in Figure 10. The Hall mobility was increased a little up to near 8 nm with the increased thickness of Al oxide layer and then, rapidly decreased, whereas the carrier density gradually increased. The resistivity was almost unchanged up to 16 nm and then sharply increased. Such rapid degradation of the electrical properties for the relatively thick Al oxide layer (>16 nm) could be mainly affected from the defects of the film, that is, incomplete crystallization of the AIC process. But the small property changes for the relatively thin Al oxide layers (<16 nm) may be resulted from the influence of the Al oxide layer on the crystallization.

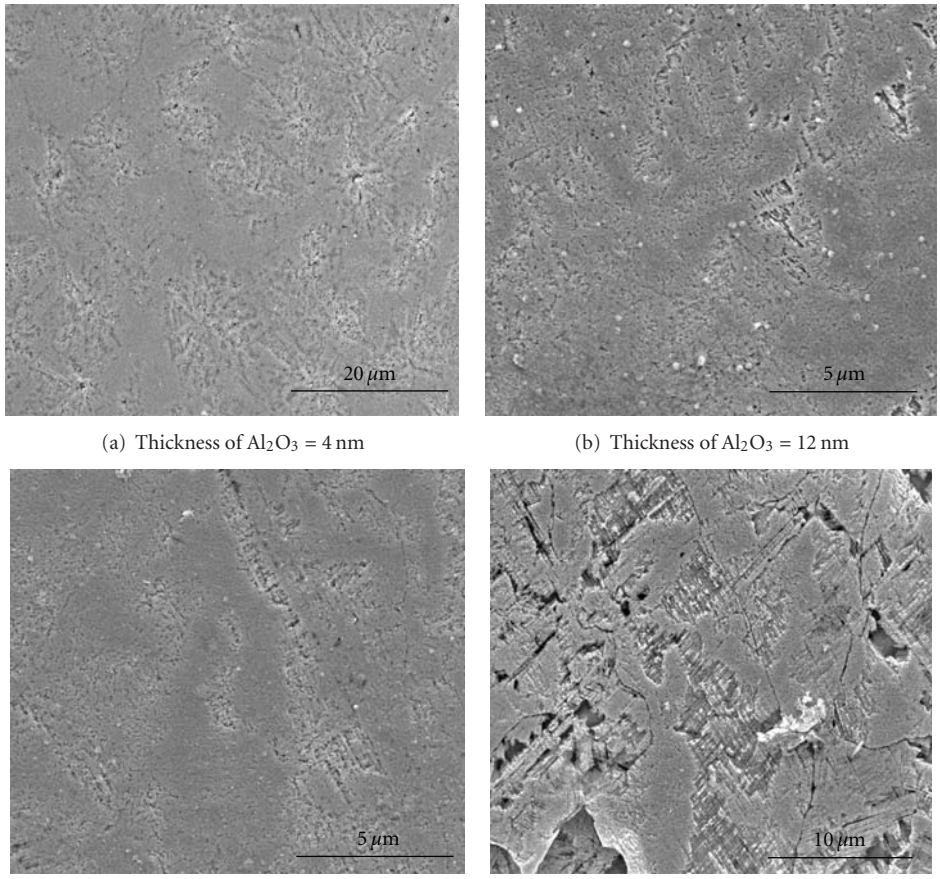
Near 8 nm of Al oxide layer thickness could be the optimum for the electrical properties. In this case, the resistivity, the carrier density, and the Hall mobility were $6.1 \times 10^{-2}\ \Omega\cdot$cm, 1.1×10^{18} cm^{-3}, and 90.91 cm^2/Vs, respectively.

Due to the remained Al content in the pc-Si film by the AIC process, all films show a p-type poly silicon property. The electrical properties of the pc-Si films are shown in Table 2.

4. Conclusion

In this work, we investigated the structural and electrical properties of the pc-Si films produced by AIC process, depending on the thickness of the Al oxide interlayer between Al/a-Si layers.

In conclusion, we showed the influence of the thickness of the Al oxide interlayer between Al/a-Si layers on the properties of the AIC pc-Si film, like the grain size, the crystal orientation, and the film defects. The tendency of the dependence of the structural properties on the oxide layer was consistent with the case of the electrical properties. But the dependence of the structural properties was slightly more sensitive than the case of the electrical properties. In our experimental conditions, the optimum value of the Al oxide thickness could be in the range of 4~8 nm. For the sample of 4 nm thick Al oxide layer, we achieved the average grain size



(a) Thickness of Al_2O_3 = 4 nm

(b) Thickness of Al_2O_3 = 12 nm

(c) Thickness of Al_2O_3 = 16 nm

(d) Thickness of Al_2O_3 = 20 nm

Figure 9: SEM images of pc-Si films for samples with various Al oxide layer thicknesses.

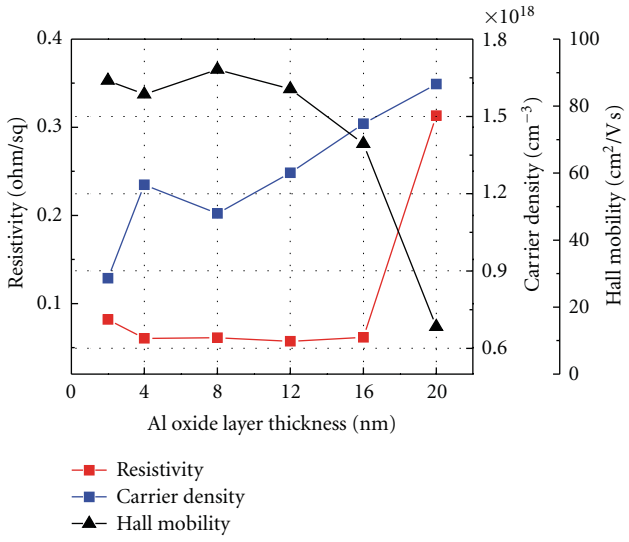


Figure 10: Resistivity, Hall mobility, and carrier density of the pc-Si films as a function of difference Al oxide layer thickness.

of 15 μm and the preferential <100> orientation, R (100), of more than 58%. The Hall mobility and resistivity were 6.1×10^{-2} cm, 90.91 cm^2/Vs, respectively, for the 8 nm thick Al oxide layer as best case.

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Research Article

Numerical Simulation of the Effect of Heater Position on the Oxygen Concentration in the CZ Silicon Crystal Growth Process

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We perform numerical simulations to analyze the effect of the position of the heater on the thermal and flow fields and the oxygen concentration distribution during the industrial Cz silicon crystal growth process. The amount of oxygen released from the silica crucible to the silicon melt during the growth process can be lowered by adjusting the heater position to decrease the temperature on the crucible wall. During growth of the crystal body, there is a significant decrease in the gradient of the oxygen concentration along the melt-crystal interface due to the stronger Taylor-Proudman vortex, which is generated by the crucible and crystal rotation. There is a significant reduction in the average oxygen concentration at the melt-crystal interface for longer crystal lengths because of the lower wall temperature, smaller contact surface between the crucible wall and the melt and the stronger Taylor-Proudman vortex.

1. Introduction

The monocrystalline silicon (sc-Si) solar cell is one of the most important types of solar cells currently in use. However, to ensure grid parity, the quality of mono-Si wafers has to be improved even more. In mono-Si wafers, the oxygen impurity in combination with boron dopant induces light degradation of the solar cell. Therefore, to improve the efficiency of Si solar cells, the oxygen concentration in the crystal has to be controlled. The oxygen impurity originates mainly from the chemical reaction at the interface between the hot wall of the silica crucible and the Si melt. Part of the dissolved oxygen in the melt is incorporated into the crystal, while most oxygen evaporates on the free surface as SiO, which is then transported away from the melt by the argon gas.

There have been many studies in the literature investigating how to control the oxygen concentration in a CZ system. Machida and coworkers [1, 2] installed a gas controller and/or a transverse magnetic field in their study of the effects of the argon gas flow rate and furnace pressure on the oxygen concentration in CZ grown silicon crystal. The oxygen concentration in the silicon crystal grown by a CZ system with a gas controller increases as the argon gas flow rate is reduced and the furnace pressure raised. When a transverse magnetic field is attached to a CZ furnace with a gas controller, there is a significant change in the flow pattern in the melt which causes an opposing trend of the dependence of the oxygen concentration in the CZ grown silicon crystal on the argon gas flow rate and the furnace pressure. Matsuo et al. [3] has shown by thermodynamic analysis that the oxygen concentration in the melt increases when the temperature of the silica wall increases. Chen et al. [4] have shown that the oxygen concentration in the CZ grown silicon crystal may be controlled by the rates of crucible and/or crystal rotation during

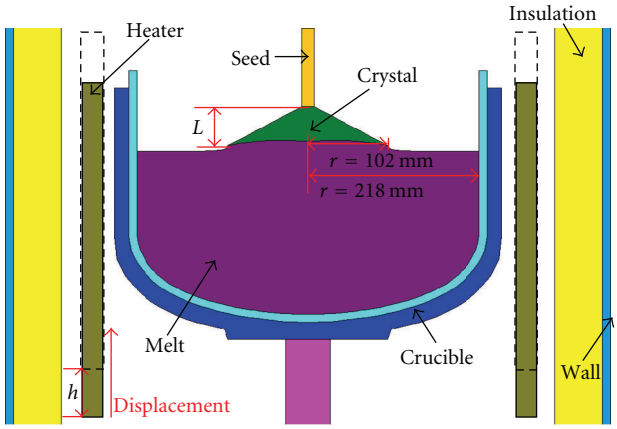

Figure 1: Schematic diagram of the major components of the CZ furnace, where L and h are the crystal length and the relative position of the heater in relation to the original position, respectively.

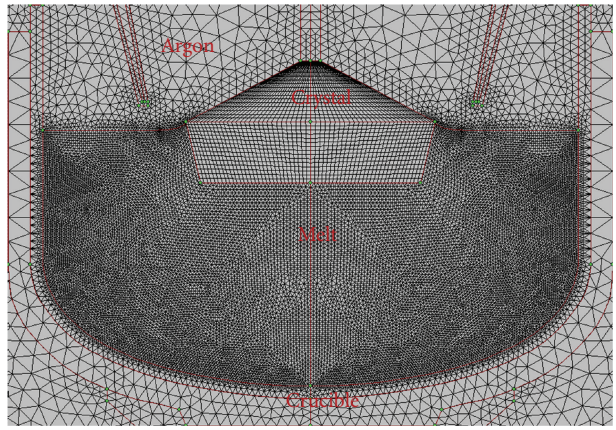

Figure 2: Distribution of the control volumes inside the furnace.

the growth. A lower oxygen concentration can be achieved in the crystal with a suitable combination of the crucible and crystal rotation rates.

The results of Matsuo et al. [3] show that the oxygen concentration level in the melt may be decreased by reducing the temperature of the silica crucible wall during the growth process. The crucible temperature is strongly affected by the arrangement of the heater in the CZ furnace. The appropriate positioning of the heater could possibly lower the temperature of the crucible wall. In the present study, a numerical investigation of the heat, flow fields, and oxygen concentration during the CZ silicon crystal growth process is carried out to determine the effect of the heater positioning on the oxygen concentration level in the crystal.

2. Mathematical Model

Figure 1 show a schematic representation of the conventional CZ furnace used in this study, where h represents the relative position of the heater from the reference position. The furnace is assumed to be axis-symmetric and the growth process is assumed to be quasisteady. The silicon melt is considered to be a Newtonian fluid. The deformation of the free surface is ignored. The argon gas is assumed to be an ideal gas. The crystal diameter is selected to be 8 inches. The crucible, as shown in Figure 1, has a diameter of 438 mm and a height of 303 mm. The amount of silicon in the crucible is 70.2 kg which is massive enough to grow a crystal 800 mm in length. The furnace pressure is kept at 2000 Pa with a 40 lpm argon gas flowrate.

The differential equations governing heat and mass transports are as follows.

In the fluid:

$$\begin{aligned} \nabla \cdot (\rho_i \vec{u}_i) &= 0, \\ (\vec{u}_i \cdot \nabla)\rho_i \vec{u}_i &= -\nabla p_i + \nabla \cdot \tau_i + (\rho_i - \rho_{i,0}) \cdot \vec{g}, \\ Cp_i \nabla \cdot (\rho_i \vec{u}_i T_i) &= \nabla \cdot (k_i \nabla T_i), \\ \nabla \cdot \left(\rho_i \vec{u}_i C_j\right) &= \nabla \cdot \left(D_j \nabla C_j\right), \end{aligned} \tag{1}$$

where ρ, ρ_0, Cp, $\vec{u}$, T, k, p, τ, $\vec{g}$, C, and D are the density, reference density, heat capacity, velocity vector, temperature, thermal conductivity, pressure, stress tensor, gravitational acceleration, impurity concentration, and diffusion coefficient of the impurity, respectively. The subscript i may be g or l, where g and l indicate the argon gas and silicon melt, respectively. The subscript j is O or SiO, where O and SiO indicate the oxygen in the melt and silicon oxide in the argon, respectively.

In the heater:

$$\nabla \cdot (k_h \nabla T_h) = \dot{q}, \tag{2}$$

where $\dot{q}$ is the heat generation from the heater.

The temperature at the melt/crystal interface is equal to the melting temperature of silicon, and the energy balance should satisfy the Stefan condition. The segregation effect of oxygen impurity is taken into account. The boundary conditions for the oxygen concentration at the crucible wall immersed into the silicon melt and for the oxygen concentration at free surface can be referred to our previous study [4]. The SiO concentration at the gas inlet is zero. The flux in the SiO concentration at the gas/solid interface is zero because the effect of deposition is ignored. The flow motion in the Si melt is in the transition regime [4]. The Reynolds average Navier-Stoke equation (RANS) is employed with the one-equation model [5] to simulate the turbulent motion inside the melt. To appropriately increase the dissipation rate near the wall, the Wolfshtein model [6] is used. To account for the turbulence suppression because of the crucible rotation effect, it is changed as a function of the mean strain and rotation rates [7]. For details of the boundary conditions and material properties, refer to [4, 8, 9]. The energy, continuity, momentum, and species equations with boundary conditions are solved with CGSim package, which is based on the finite volume method (FVM). Figure 2 shows the distribution of the control volumes inside the furnace. The effect of the control volume number is examined to find the best results providing sufficient accuracy and requiring less computational time for each case. The total number of the control volumes employed in the present computation is 28,587.

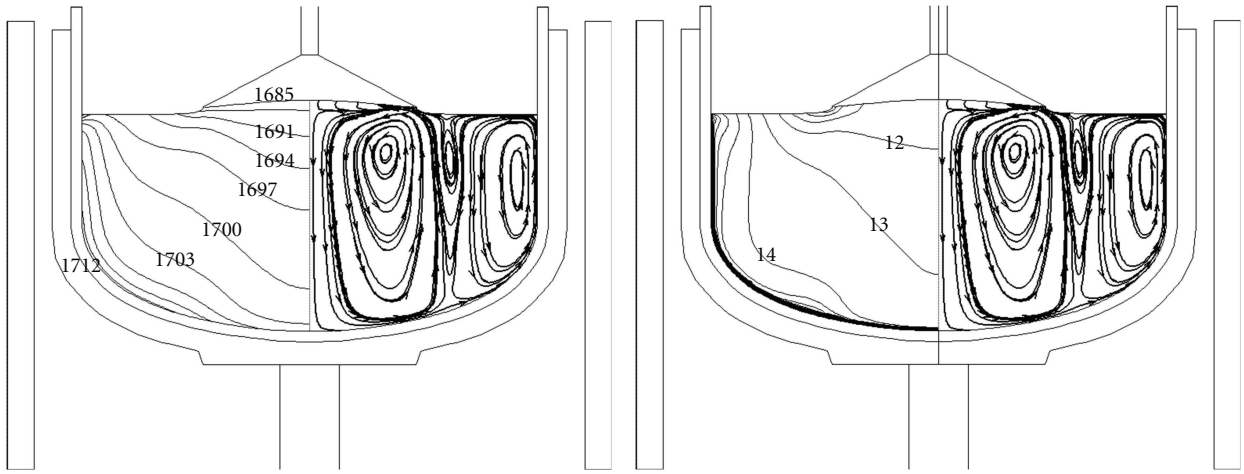

Figure 3: Distribution of the temperature, streamtrace, and oxygen concentration in the melt for $L = 50$ mm in a conventional CZ furnace ($h = 0$ mm): (a) isothermal lines (left) and streamtraces (right); (b) oxygen concentration isolines (left) and streamtraces (right). The units of temperature, velocity vector, and oxygen concentration are K, m/s, and ppma, respectively. The spacing of the isothermal lines and concentration isolines are 3 K and 1 ppma, respectively.

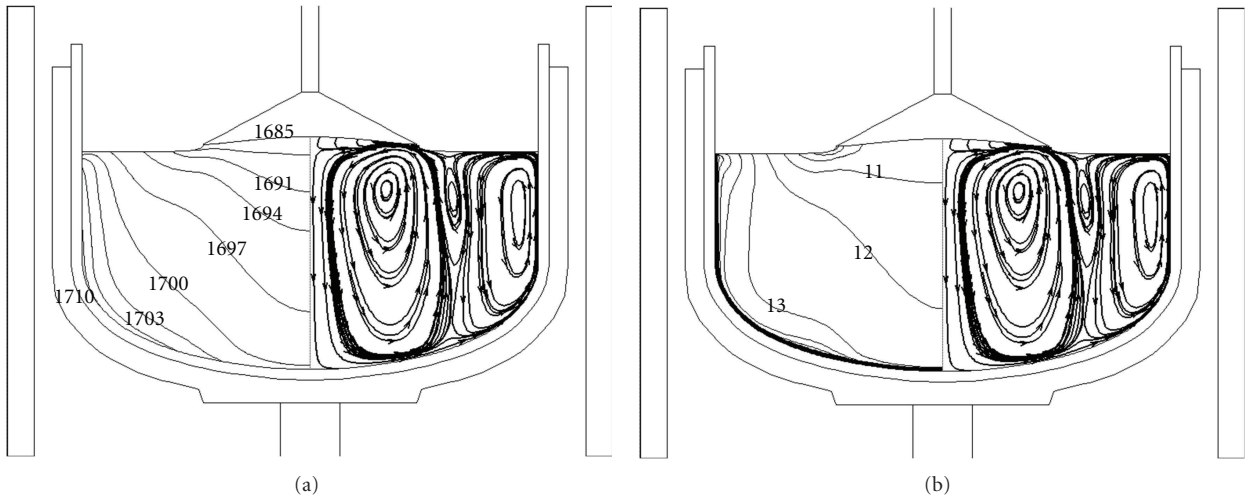

Figure 4: Distribution of temperature, streamtrace, and oxygen concentration in the melt for $L = 50$ mm in a conventional CZ furnace ($h = 50$ mm): (a) isothermal lines (left) and streamtraces (right); (b) oxygen concentration isolines (left) and stream traces (right). The units of temperature, velocity vector, and oxygen concentration are K, m/s, and ppma, respectively. The spacing of the isothermal lines and concentration isolines are 3 K and 1 ppma, respectively.

3. Results and Discussion

According to the study of Chen et al. [4], there is an optimum combination of crucible and crystal rotations for obtaining the lowest oxygen concentration for a CZ furnace. In this study, the crystal and crucible rotation rates are fixed at 13 and −3 rpm, respectively, which indicate the best operating conditions for the lowest oxygen concentration obtained by Chen et al. [4]. The maximum distance of upward movement of the heater from $h = 0$ mm without contact to the side insulation for the present furnace is 50 mm. Three different heater positions of $h = 0$, 30, and 50 mm are considered here. During the crystal growth, the heater position is fixed and the crucible is moved upwards to keep the predetermined gap between the free surface of the silicon melt and the heat shield. The numerical computations are carried out for different crystal lengths L.

Figures 3 and 4 show the temperature, streamtrace, and oxygen concentration distributions in the melt for $L = 50$ mm (crystal crown was formed) with $h = 0$ and 50 mm. There are 3 vortices in the melt: the buoyancy-thermocapillary vortex near the wall, Taylor-Proudman vortex under the crystal, and secondary vortex between them. The oxygen impurity originating from the silica crucible wall is diffused

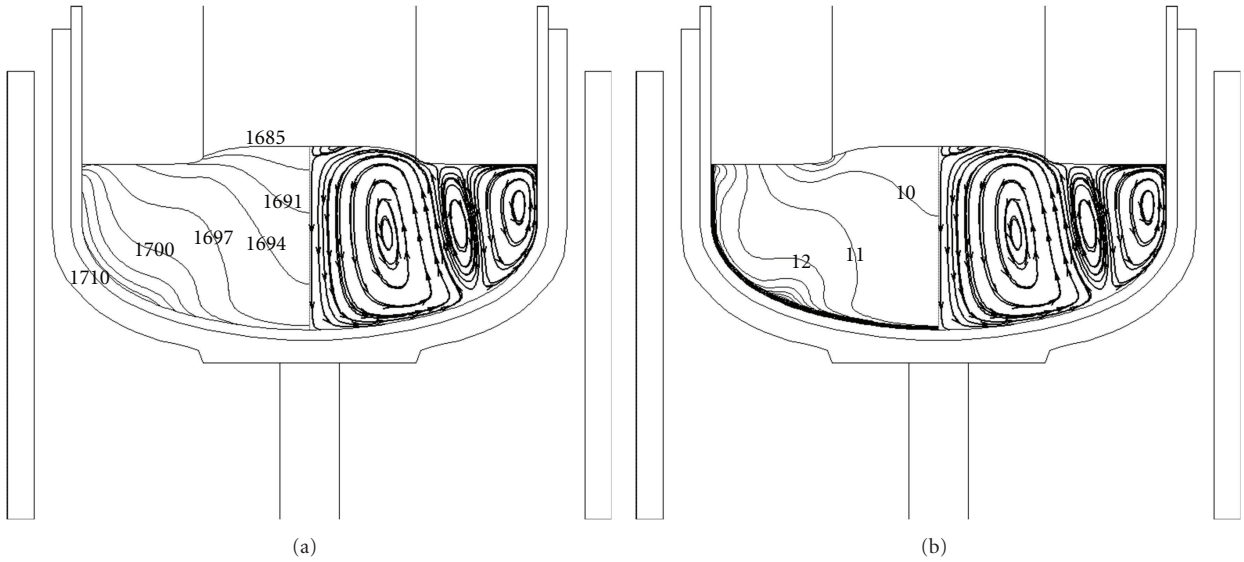

Figure 5: Distribution of temperature, streamtrace, and oxygen concentration in the melt for $L = 300$ mm in a conventional CZ furnace ($h = 0$ mm): (a) isothermal lines (left) and streamtraces (right); (b) oxygen concentration isolines (left) and streamtraces (right). The units of temperature, velocity vector, and oxygen concentration are K, m/s, and ppma, respectively. The spacing of the isothermal lines and concentration isolines are 3 K and 1 ppma, respectively.

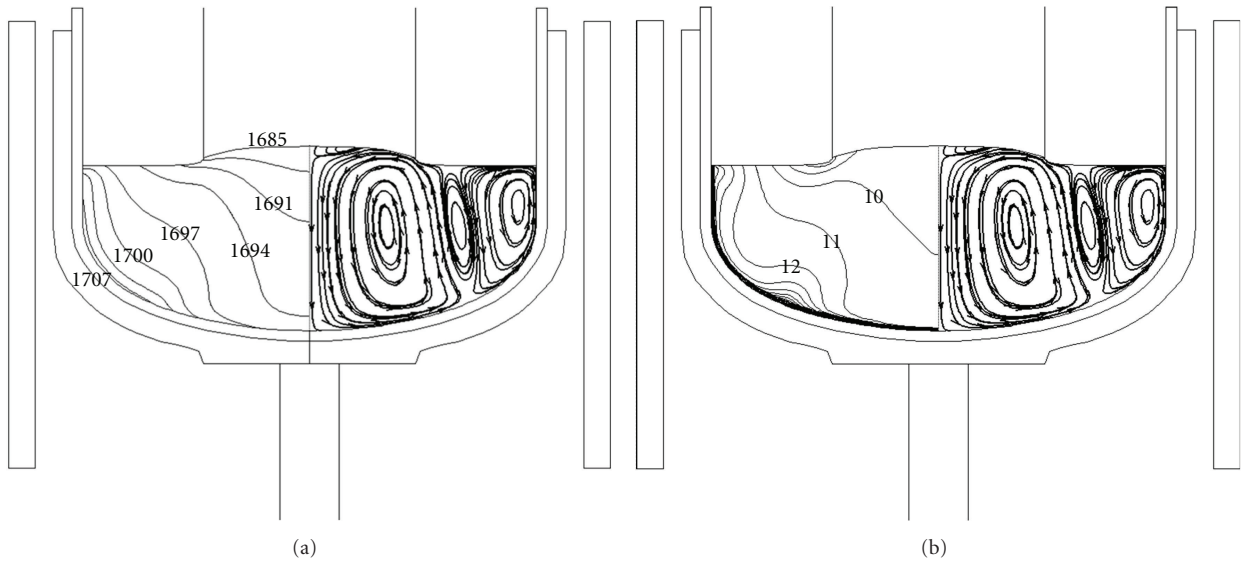

Figure 6: Distribution of temperature, streamtrace, and oxygen concentration in the melt for $L = 300$ mm in a conventional CZ furnace ($h = 50$ mm): (a) isothermal lines (left) and streamtraces (right); (b) oxygen concentration isolines (left) and streamtraces (right). The units of temperature, velocity vector, and oxygen concentration are K, m/s, and ppma, respectively. The spacing of the isothermal lines and concentration isolines are 3 K and 1 ppma, respectively.

into the silicon melt. This is prevented at the crystal-melt interface by the suppression of the flow motion of the Taylor-Proudman vortex and carried to the free surface of the melt by the buoyancy-thermocapillary vortex. The oxygen impurity at the free surface can vaporize to form SiO gas which is removed from the furnace by the motion of the argon gas. The maximum temperature T_{max} at the crucible wall appears at the intersection of the vertical and bottom wall. For $h = 0$ mm, T_{max} is 1712 K, which is higher than that for $h = 50$ mm ($T_{max} = 1710$ K). The melt flow patterns are similar due to the small difference in the maximum temperature between $h = 0$ and 50 mm and the same combination of rotation rates of crucible and crystal. Therefore, the distributions of the isotherms and oxygen concentration isolines in the melt are also similar. The amount of oxygen impurity released from the crucible wall decreases as the temperature of the crucible wall and the amount of contact surface of the melt and the crucible wall decrease. Since

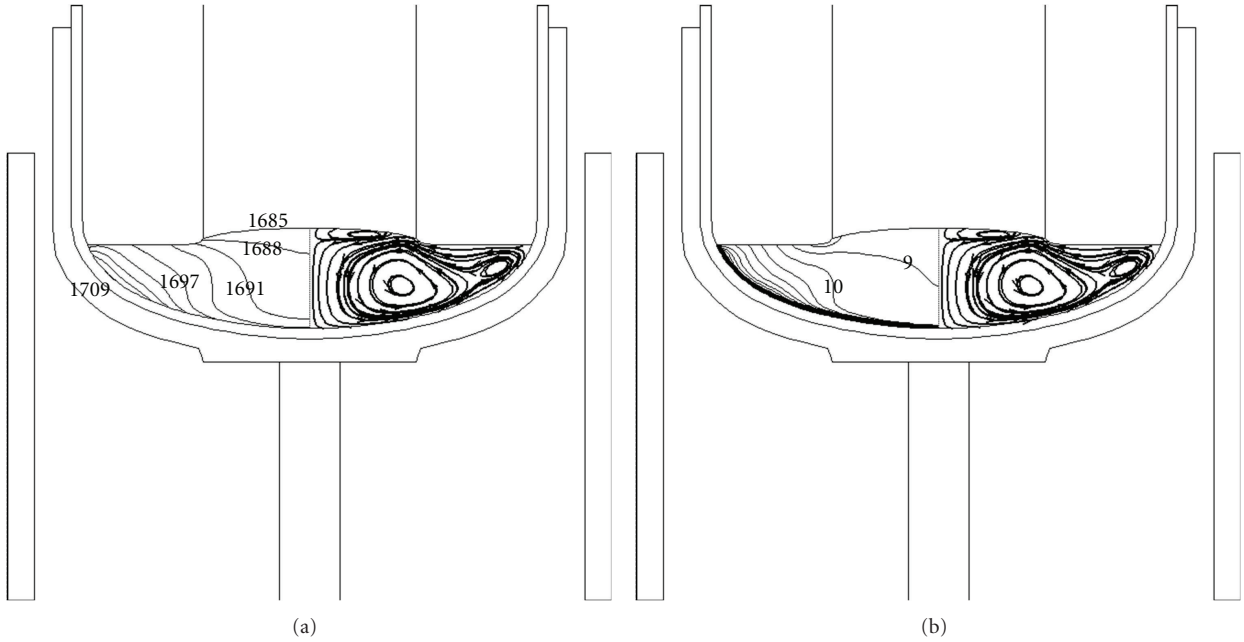

Figure 7: Distribution of temperature, streamtrace, and oxygen concentration in the melt for $L = 700$ mm in a conventional CZ furnace ($h = 0$ mm): (a) isothermal lines (left) and streamtraces (right); (b) oxygen concentration isolines (left) and streamtraces (right). The units of temperature, velocity vector, and oxygen concentration are K, m/s, and ppma, respectively. The spacing of the isothermal lines and concentration isolines are 3 K and 1 ppma, respectively.

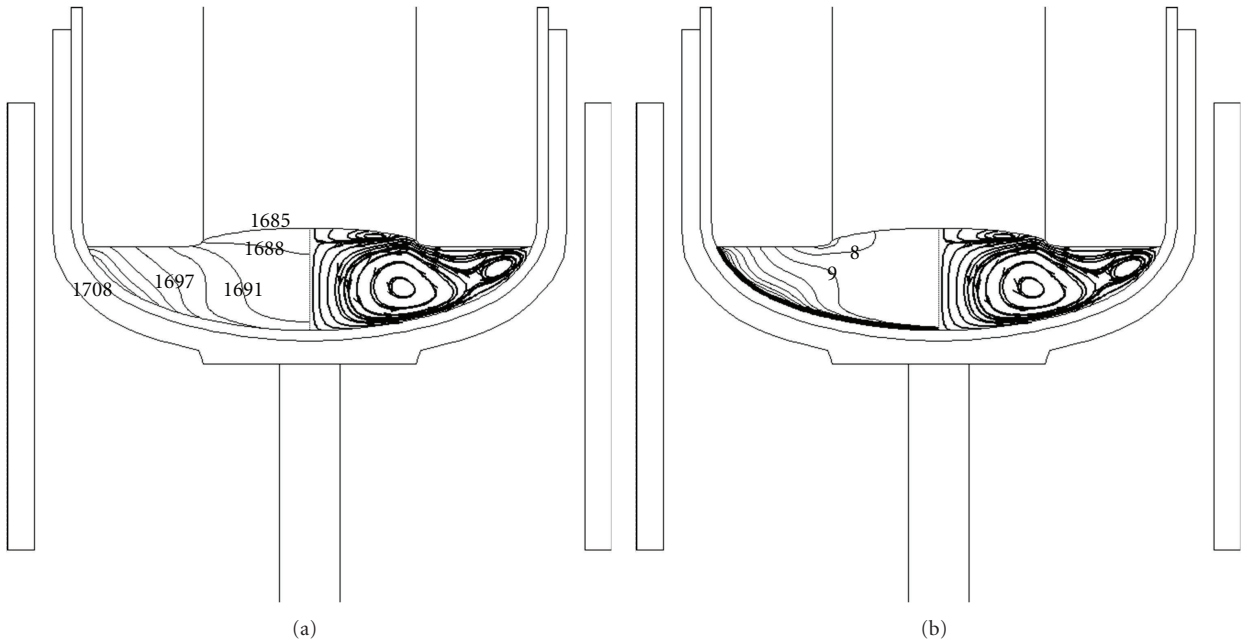

Figure 8: Distribution of temperature, streamtrace, and oxygen concentration in the melt for $L = 700$ mm in a conventional CZ furnace ($h = 50$ mm): (a) isothermal lines (left) and streamtraces (right); (b) oxygen concentration isolines (left) and streamtraces (right). The units of temperature, velocity vector, and oxygen concentration are K, m/s, and ppma, respectively. The spacing of the isothermal lines and concentration isoline are 3 K and 1 ppma, respectively.

the maximum temperature of $h = 50$ mm is lower, the magnitude of oxygen concentration is smaller.

It can be seen in Figures 5 and 6 that the flow, temperature, and oxygen concentration patterns for $L = 300$ mm are similar to those for $h = 0$ and 50 mm. Since the depth of the melt for $L = 300$ mm is much smaller than when $L = 50$ mm, there is a significant reduction in the strength of the buoyancy-thermocapillary vortex for $L = 300$ mm in comparison to the case for $L = 50$ mm. Hence, the Taylor-Proudman vortex for the $L = 300$ mm case becomes stronger.

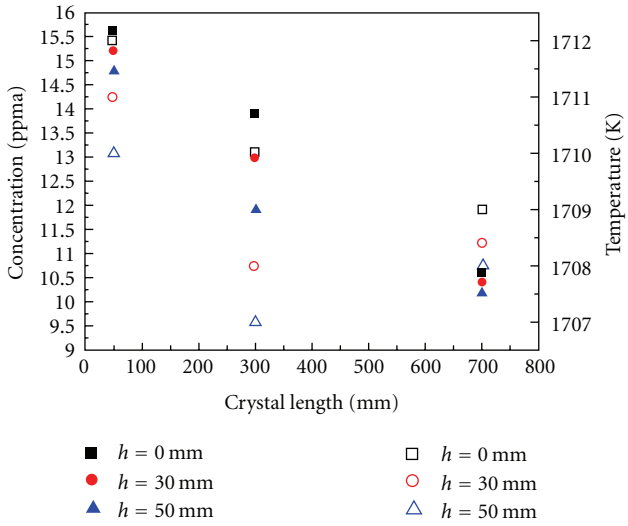

Figure 9: Average oxygen concentration at the crystal-melt interface and maximum temperature of crucible wall versus crystal length L.

The effect of the Taylor-Proudman vortex is totally dominant for $L = 700$ mm (Figures 7 and 8). The temperature and oxygen gradients near the crystal-melt interface become smaller when the length of crystal increases. On the other hand, the magnitude of the temperature and oxygen concentration in the melt decreases for longer crystal lengths (Figures 3–8).

The average oxygen concentration at the crystal-melt interface is defined as the total oxygen concentration at the crystal-melt interface, which is obtained by integrating the oxygen concentration over the entire crystal-melt interface, divided by the crystal-melt area. Figure 9 displays the variation of the average oxygen concentration at the crystal-melt interface and the maximum wall temperature with the crystal height for $h = 0$, 30, and 50 mm. For a fixed crystal length, the average oxygen concentration decreases as h increases. It can be seen that the difference of the maximum temperature for $h = 0$, 30, and 50 mm is more significant for $L = 300$ mm. This may explain the difference in average oxygen concentration for $L = 300$ mm (Figure 9). On the other hand, the heater power increases as the heater position moves upward. The reduction in the temperature of the crucible wall, the contact surface of the melt and the crucible wall and the oxygen gradients along the melt-crystal interface indicates a reduction in the average oxygen concentration when the crystal length increases. As the crystal length increases from $L = 50$ mm to $L = 300$ mm, the input power decreases. When the crystal length further increases from $L = 300$ mm to $L = 500$ mm, it increases.

4. Conclusion

The heater position is one of the important factors affecting the temperature at the crucible wall. In the present study, the oxygen concentration distributions for different heater positions are simulated. When the crucible and crystal rotation rates are determined, the flow pattern in the melt is similar for different heater positions. The oxygen concentration in the melt will be dependent on the temperature of the crucible wall and the amount of contact between the surface of the crucible wall and the melt. For cases considered in the present study, when the heater moves upwards from the reference position, the oxygen concentration becomes lower due to the lower crucible wall temperature. For larger crystal lengths, there is a notable reduction in the length of the gradients of oxygen concentration along the melt-crystal interface, since the Taylor-Proudman vortex generated by the crucible and crystal rotation is more dominant, while the wall temperature and the contact surface of the crucible wall and the melt become lower. Therefore, the oxygen concentration in the melt decreases significantly as the crystal grows longer.

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Research Article

Nanostructural, Chemical, and Mechanical Features of nc-Si:H Films Prepared by PECVD

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This study examined the effects of film thickness on the nanostructural, chemical, and mechanical features of nc-Si:H films deposited by plasma-enhanced chemical vapor deposition. SiH_4 and H_2 were used as the source gases, and the deposition time was varied from 10 to 360 min. The mean nanocrystallites size in the Si films increased from ~6 to ~8 nm with increasing film thickness from 85 to 4150 nm. Moreover, the nanocrystallite concentration and elastic modulus increased from ~7.5 to ~45% and from 135 to 147 Gpa, respectively. In the 4150 nm thick film, the relative volume fraction of Si nanocrystallites and relative fraction of Si–H bonds in the films were approximately ~45% and ~74.5%, respectively.

1. Introduction

Recently, the development of renewable energy systems has attracted considerable attention due to the high oil price and the safety risk of nuclear power systems. In particular, the transformation of solar energy into electrical power is one of the most important scientific and industrial issues mainly because solar energy is clean, infinite, and nontoxic [1]. Among the many types of thin films used in solar devices, hydrogenated nanocrystalline silicon (nc-Si:H) thin films have promising features, such as controllable energy band gap, light absorption coefficient, and electrical conductivity. All these features depend critically on the characteristics of nanometer-sized Si crystallites embedded in an amorphous matrix [2, 3]. For such applications, nc-Si:H thin films have been fabricated mainly by plasma-enhanced chemical vapor deposition (PECVD) [4, 5].

Solar cells based on amorphous silicon thin films consist of p-type, n-type, and intrinsic amorphous silicon layers. The intrinsic layer plays an important role in enhancing the solar cell efficiency [6]. For the intrinsic a-Si:H layers in solar cells, the nanostructural features of the intrinsic layers need to be well controlled in terms of the Si nanocrystallite size and size distribution. The relationship between the film thickness and the efficiency of solar cells has been reported previously [7, 8]. Nevertheless, few studies have examined the effect of the film thickness on the nanostructural, chemical, and mechanical features of the films. In addition, with varying film thickness, the mechanical stress within the film needs to be examined to better understand the nanostructural characteristics of a-Si:H films.

In this study, nc-Si:H films were deposited on Si wafers by PECVD and the formation of Si nanocrystallites along with their nanostructural, chemical, and mechanical features were examined in terms of the film thickness. Local variations in the nanostructural features and mechanical and chemical properties of thick films were also examined using a nanoprobed electron beam.

2. Experimental Details

The nc-Si:H thin films were deposited on a Si (001) wafer and a slide glass at room temperature by PECVD. SiH_4 and H_2 were introduced into a chamber at 4 and 96 sccm, respectively, and were activated with a RF power source. The RF power and frequency were 150 W and 13.56 MHz, respectively. The substrate temperature was fixed to room temperature. The surface of the substrate Si wafer was cleaned in a HF solution to remove the native oxide layer. Table 1 provides details of the deposition conditions for the films.

Table 1: Various deposition conditions of the nc-Si:H thin films.

System	Deposition parameter	Experimental conditions
PECVD	SiH_4 flow rate (sccm)	4
	H_2 flow rate (sccm)	96
	Substrate	Si wafer, glass
	RF power (watt)	150
	Deposition time (min)	10, 30, 60, 180, 360
	Working pressure	4×10^{-2} (Torr)
	Background pressure	1×10^{-6} (Torr)

The size and relative volume fraction of Si nanocrystallites in the films were examined by Raman spectroscopy (Hobin Yvon, T6400). The film thickness was measured by field emission scanning electron microscopy (FE-SEM, Hitachi, S-4300). High-resolution X-ray diffraction (HRXRD, XPET-PRO MDR) was performed to estimate the mean nanocrystallite size in the films. The chemical bonds of the films were analyzed by Fourier Transform Infrared (FT-IR, IFS66v/s, Bruker) spectroscopy. High-resolution transmission electron microscopy (HRTEM, JEOL 2100F) and electron energy loss spectroscopy (EELS) were used to obtain local structural information. Electron microdiffraction was used to identify the presence of crystallites at particular regions of the films; the beam probe was ~1 nm in size. Cross-section TEM specimens (~8 μm × ~6 μm × ~40 nm) were prepared from a 4150 nm thick film using a focused ion beam (FIB) technique. The Young's modulus of the films was analyzed using a nanoindenter (MTS, Nanoindenter XP).

3. Results

3.1. Nanostructural Features. Figure 1 shows cross-section SEM images of the nc-Si:H thin films. The film thickness increased almost linearly from 85 to 4150 nm with increasing deposition time from 10 to 360 min. (Figure 1(d)). The interface between the film and substrate is clearly noticeable, and column-shaped morphology features were observed in the film region.

Figure 2 shows XRD patterns of the nc-Si:H films. The diffraction peak at 28.4° 2θ was assigned to the (111) crystallographic plane of Si. The Si (111) peak intensity increased with increasing deposition time. In particular, the intensity of the peak in spectrum (5) was 8 times as large as that in spectrum (1). The crystallite size was estimated using Sherrer's equation [9].

$$d_{\mathrm{XRD}} = \frac{0.9\lambda}{B\cos\theta}, \tag{1}$$

where λ is the X-ray wavelength, B is the FWHM, and θ is the diffraction angle of the peak. The crystallite size varied from ~6 to ~8 nm. This variation was clearly observed within the resolution of the analysis method.

The Raman spectra of the nc-Si:H films deposited for 10, 180, and 360 min, were obtained (Figure 3). All phonon modes of the transverse acoustic (TA), longitudinal acoustic (LA), longitudinal optical (LO), and transverse optical (TO) modes are active in Raman spectroscopy [10]. The best Gaussian fits of the Raman spectra are illustrated in each spectrum. The broad peak at 480 cm^{-1} indicates the presence of amorphous silicon (a-Si). The shoulder peak at 500~510 cm^{-1} was assigned to the presence of Si nanocrystallites (nc-Si) [11]. The symmetric main peak of bulk Si is centered at 521 cm^{-1}.

Deconvoluted Gaussian fits provide information on the volume fraction of the nanocrystallites as well as the mean crystallite size. Equation (2) was used to obtain the mean crystallite size [12, 13].

$$D_{\mathrm{Raman}} = 2\pi\sqrt{\frac{\beta}{\Delta\omega}}, \tag{2}$$

where $\Delta\omega$ is the peak shift for the Si nanocrystallite compared to that of bulk Si and $\beta = 2.0\,\mathrm{cm^{-1}\,nm^2}$. The Raman spectra of the nc-Si:H films deposited for 10 min clearly show the characteristic features of amorphous Si. With increasing deposition time from 30 to 360 min, there was a significant variation in crystallite size from 6.9 to 8.5 nm. The results obtained by XRD and Raman spectroscopy were well matched to each other; the difference was less than 1 nm for each size.

The volume fraction X_c of the Si nanocrystallites in the films was obtained based on two fits: one (I_a) near 480 cm^{-1} and the other (I_c) for nc-Si. The relative volume fraction of Si crystallites in the film was estimated by the formula, $X_c = I_c/(I_c + \eta I_a)$, where η is a scattering factor that is regarded as ~1.0 for nanocrystallites [14]. The volume fraction of nanocrystallites increased steadily with increasing film thickness. The largest fraction was observed in the 4150 nm thick films; the fraction was approximately ~45%.

3.2. Chemical Bonding Features. Figure 4 shows the FT-IR spectra of the nc-Si:H films prepared for (a) 30, (b) 60 and (c) 360 min. The spectra were deconvoluted and the best fits are illustrated. The spectra show prominent peaks at 2000, 2100, and 2140 cm^{-1}, which were assigned to a stretching vibration of Si–H (monohydride), Si–H_2 (di-hydride) and Si–H_3 (tri-hydride), bonds, respectively [15]. Si–H_2 bonds were dominant in the films prepared for 30 min (X_c = 7.5%), whereas the Si–H and Si–H_3 fractions were quite small. In contrast, the films with X_c = 45% contained a high proportion of Si–H, whereas the Si–H_2 and Si–H_3 fractions were quite small. The Si–H bond can be attributed to the passivation of Si crystallites embedded in an amorphous Si matrix [16]. The Si crystallites on the surface can be surrounded by hydrogen producing monohydrides. On the other hand, dihydrides and trihydrides bonds are easily returned to the plasma or remain in the amorphous phase of the films. The presence of monohydride type bonds in the films indicates the enhancement of Si crystallization. The relative fraction of monohydrides with respect to the total hydrides in the film increased to ~74.5% with increasing film thickness to 4150 nm.

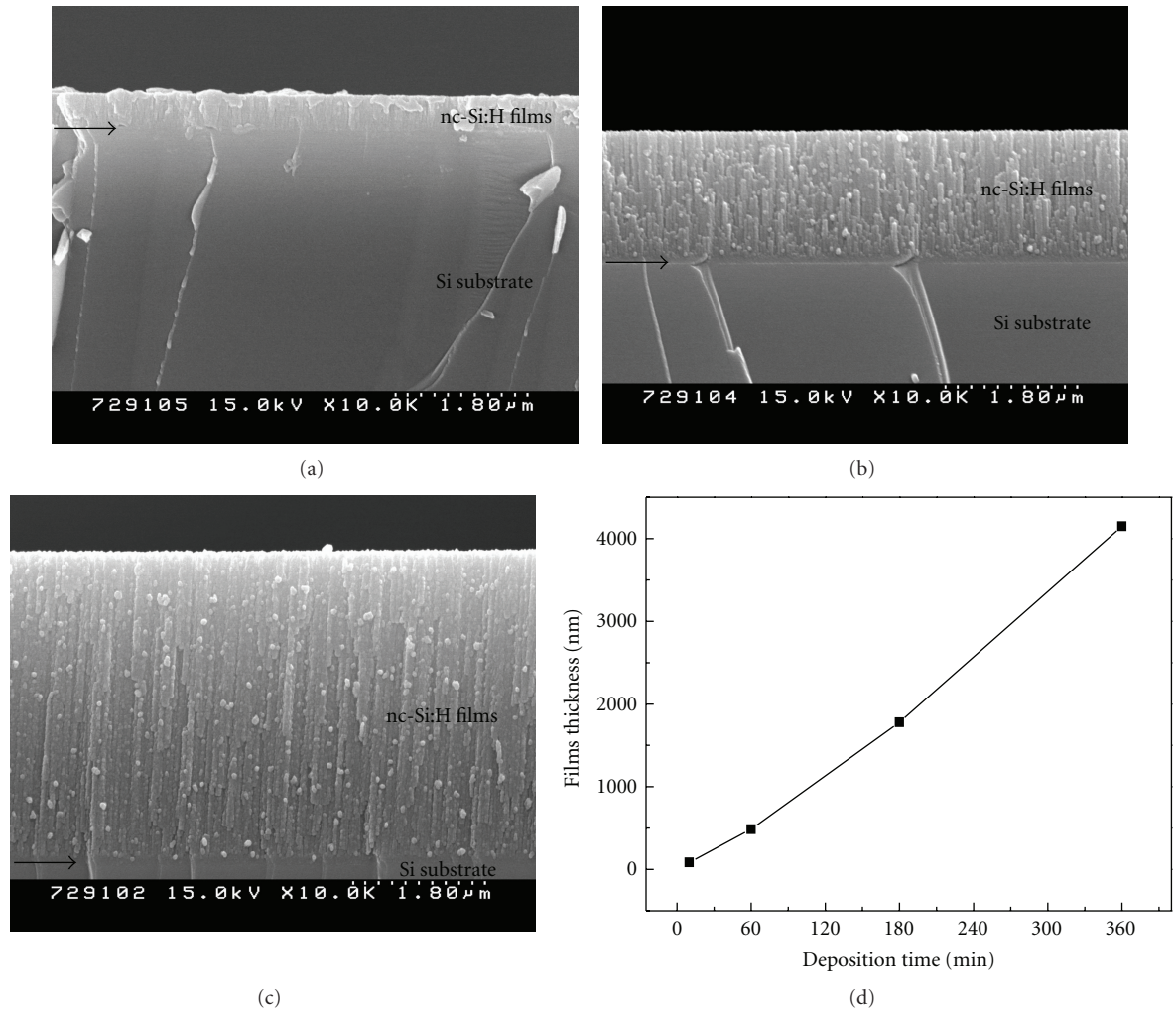

Figure 1: Cross-section SEM images of the films. The films were prepared for 60 (a), 180 (b), and 360 min. (c), respectively. (d) Film thickness versus deposition time. The arrows indicate the interface between the films and Si substrate.

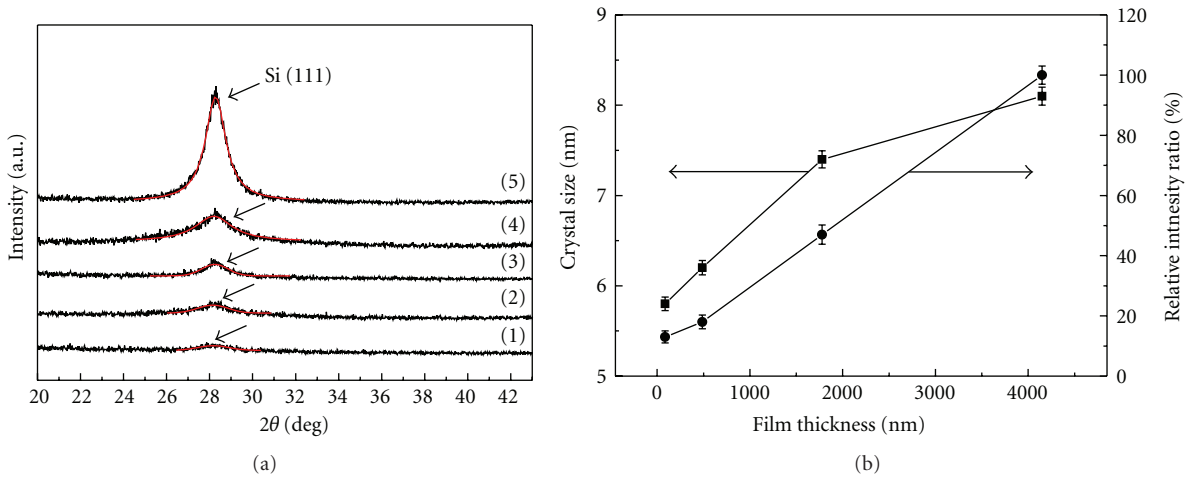

Figure 2: (a) XRD patterns of the Si thin films. The films were prepared at a substrate temperature of R.T. for 10 (1), 30 (2), 60 (3), 180 (4), and 360 min (5), respectively. The arrow indicates the presence of (111) Si peaks in each spectrum. (b) Crystal size and relative peak intensity ratio (relative peak intensity ratio = $(\text{Intensity}_{\text{peak}1,2,3,4,5}/\text{Intensity}_{\text{peak}5}) \times 100\%$) versus film thickness.

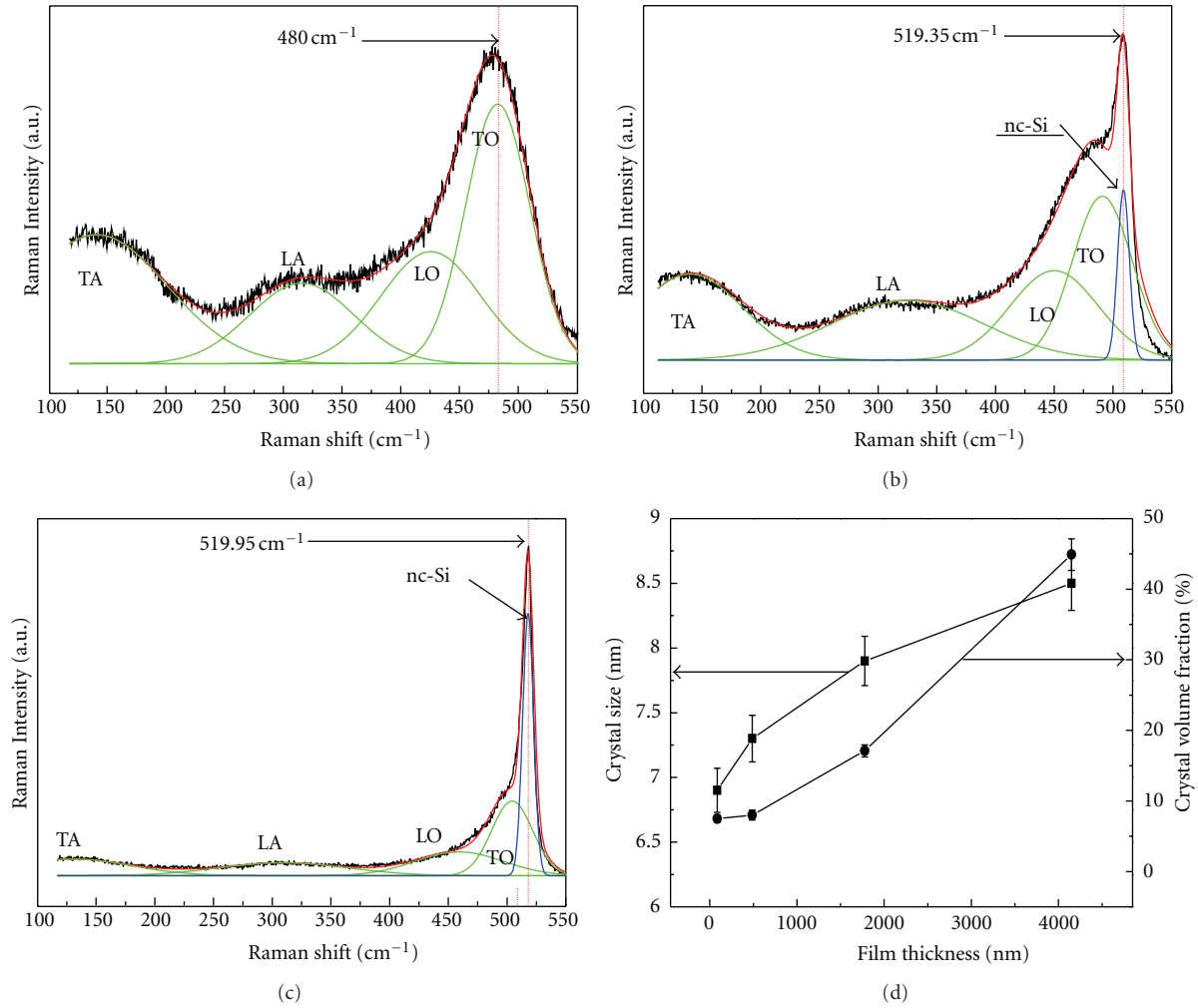

FIGURE 3: Raman spectra of the films. The best fits are superimposed in each spectrum. The films were deposited for (a) 10, (b) 180, and (c) 360 min. (d) Crystal size and volume fraction versus film thickness.

3.3. Mechanical Features. Figure 5 shows the mean elastic modulus results, which was calculated using (3) [17].

$$\frac{1}{E_r} = \frac{1-\nu_s^2}{E_s} + \frac{1-\nu_i^2}{E_i}, \tag{3}$$

where E_r is the elastic modulus of nc-Si:H films. ν_i and ν_s are the Poisson's ratios of the diamond tip (0.07) and a-Si:H (0.23), respectively; E_i and E_s are the Young's modulus of the diamond tip (1141 Gpa) and nc-Si:H, respectively. The highest elastic modulus (157 Gpa) was observed when the film thickness was approximately 85 nm; this film was almost amorphous. The elastic modulus decreased rapidly to ~135 Gpa with increasing thin film thickness from 85 to 260 nm and then increased steadily from ~147 Gpa with further increases in film thickness to 4150 nm.

3.4. Distribution of Si Nanocrystallites in 4150 nm Thick Films. Figure 6 shows a cross-section scanning transmission electron microscopy (STEM) image of nc-Si:H films with a thickness of 4150 nm; the microdiffraction patterns were obtained at various depth positions. The electron microdiffraction patterns obtained at positions P_2 (near top surface of the film), P_3, and P_4 (near middle of the film) clearly exhibit spots related to the presence of nanocrystallites. On the other hand, in the patterns recorded at P_1 (top of the film) and P_6 (bottom of the film), the intensity of the spots appeared to decrease and spread out [18].

Figure 7 shows the EELS spectra obtained from the specimen shown in Figure 6. The peaks at ~99.9 eV were attributed to Si-$L_{2,3}$ [19]. The spectra obtained at P_3 and P_4 appear to have higher intensities than the other spectra. This shows that the distribution of nanocrystallites in the films was not uniform. The stress at the middle of the film, such as regions P_3 and P_4, is expected to be considerably different from that at positions P_1 and P_6, which might be related to local variations in the density of nanocrystallites in the film [20, 21].

4. Discussion

4.1. Nanostructural and Mechanical Features. As observed by SEM, XRD, and Raman spectroscopy, the film thickness was almost proportional to the deposition time. The growth rate

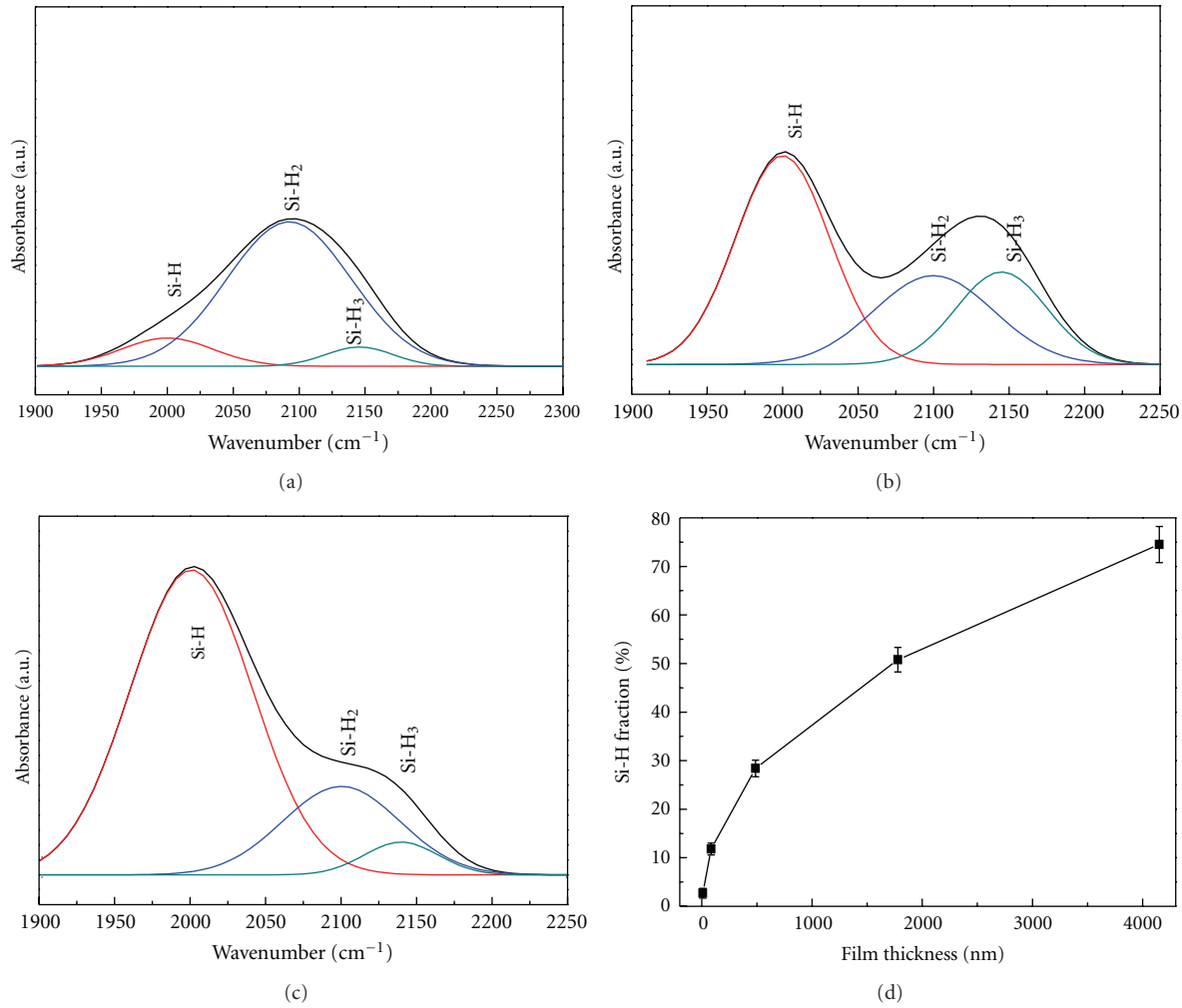

Figure 4: FT-IR results. The spectra were obtained from the films prepared for (a) 30, (b) 60, and (c) 360 min. (d) Si–H bonding fractions versus film thickness.

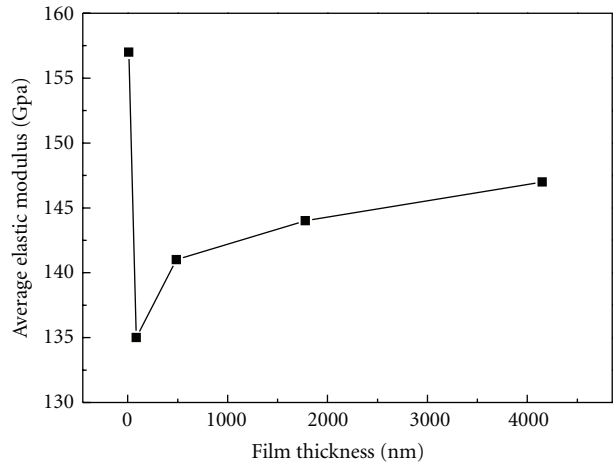

Figure 5: Nanoindentation results of the nc-Si:H films. Variation in the elastic modulus with film thickness.

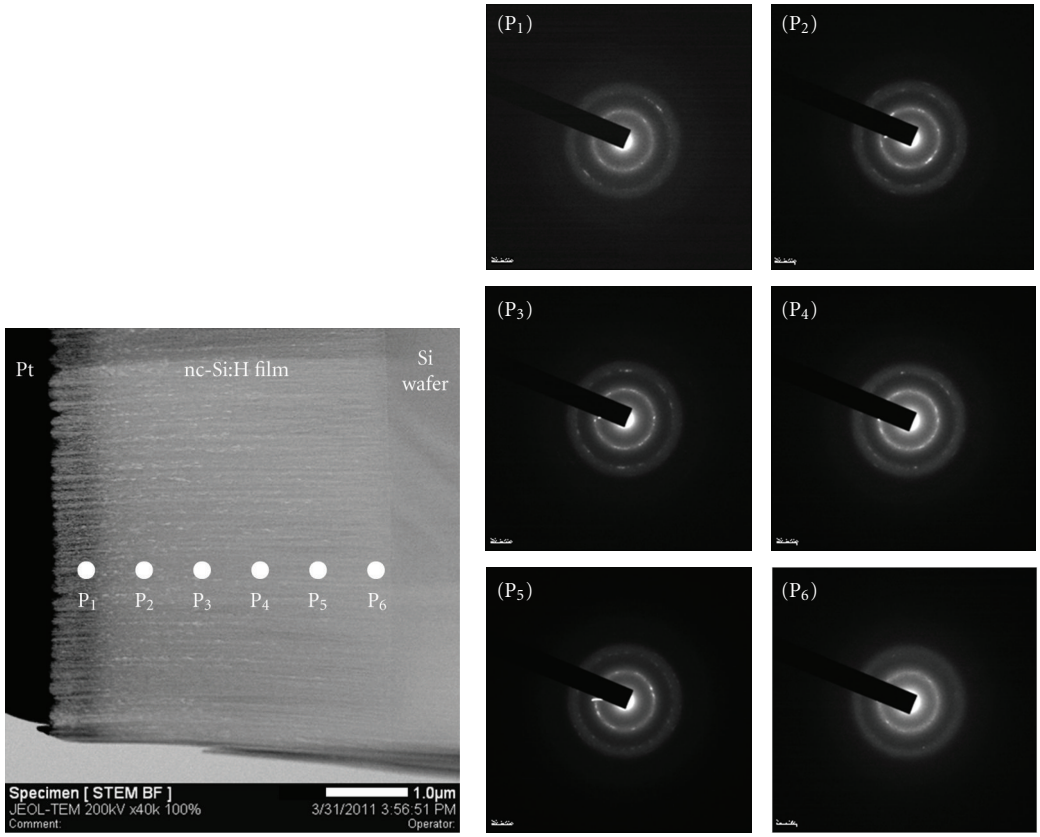

Figure 6: (a) Cross-section STEM image of the nc-Si:H thin films. Arrow m indicates the interface between the substrate (Si-wafer) and nc-Si:H films. (b) Electron microdiffraction patterns were recorded at positions $P_1 \sim P_6$ in (a).

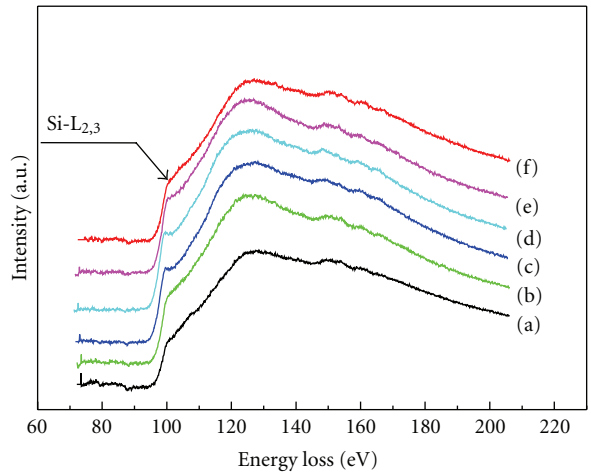

Figure 7: EELS spectra of the nc-Si:H thin films. Spectra (a)~(f) were recorded from positions $P_1 \sim P_6$, in Figure 6.

was ~11.5 nm/min under these experimental conditions. Films <85 nm in thickness were almost amorphous. The relative volume fraction of the crystallites increased to ~45% with increasing film thickness from 260 to 4150 nm. The mean size of the Si nanocrystallites in the films ranged from ~6 to ~8 nm under this experimental range (Table 2).

In the initial stage of film growth (deposition time ≤10 min), the film exhibited a considerably large Young's modulus, which was attributed mainly to the dominant presence of an amorphous Si phase.

The Young's modulus of the film decreased from ~157 Gpa to ~135 Gpa with increasing thickness from

Table 2: Variation in the chemical and physical features of the nc-Si:H thin films with deposition time.

Deposition time (min)	Film thickness (nm)	d_{XRD}* (nm)	$d_{Raman\ S.}$** (nm)	Crystal volume fraction (%)	Monohydride volume fraction (%)	Elastic modulus (Gpa)
10	85	—	—	—	2.7	157
30	260	5.8	6.9	7.5	11.8	135
60	490	6.2	7.3	8.0	28.4	141
180	1780	7.4	7.9	17.7	50.8	144
360	4150	8.1	8.5	45.0	74.5	147

* d_{XRD}: crystal size measured by XRD.
** $d_{Raman\ S.}$: crystal size measured by Raman Spectroscopy.

85 to 260 nm; the Si nanocrystallites were formed in a-Si. On the other hand, the Young's modulus of the films increased with further increased in film thickness to 4150 nm, reaching ~147 Gpa, which is still lower than that for a purely amorphous phase. Moreover, the relative volume fraction of the Si nanocrystallites in the film increased to ~45%. The formation of Si nanocrystallites is believed to be related to the decreasing structural energy of the films during deposition.

The size of Si crystallites is determined mainly by the substrate temperature and the interfacial energy with the amorphous-phased matrix [22]. The structural features of the interface between the crystallites and amorphous matrix are affected by stress in the films. The change in stress within the films appears sensitive to the crystallite-forming species (ions) on the growing film surfaces under these experimental conditions. Consequently the crystallite size increased significantly from ~6 to ~8 nm with increasing thickness from 260 to 4150 nm with a concomitant change in the Young's modulus of the film. More study is currently underway to obtain a better understanding of the interface between the crystallites and amorphous phase.

4.2. Chemical Bonding Features. Si–H, Si–H_2, and Si–H_3 bonds are located at either the surface of the Si nanocrystallites or polymeric Si clusters in the nc-Si:H thin films. Considering that the crystallites embedded in an amorphous matrix are nanosized, the surface of the crystallites is believed to be passivated mainly by Si–H. Si–H_2 and Si–H_3 bonds may contribute to the formation of polymeric chains present in the matrix of the films [23]. Consequently, the change in the relative fraction of the Si crystallites can be related to the relative fraction of Si–H bonds, $[\text{Si–H}]/\sum_{n=1}^{3}[\text{Si–H}_n]_{n=\text{integer}}$, in the films. The relative fraction of Si–H bonds varied from ~2.7 to ~74.5% with increasing film thickness from 85 to 4150 nm. This concurs with the increase in the relative volume fraction of Si crystallites in the film with increasing thickness.

4.3. Local distribution of Si nanocrystallites. The thick film with a thickness of 4150 nm showed local variations in the concentration of Si nanocrystallites, especially with the distance from the film and substrate interface.

In particular, the EELS and electron microdiffraction patterns obtained from a region near the interface (P_6) showed a small concentration of Si crystallites. Such a lack of crystallites appears to be related to the fact that the film with a thickness of 85 nm was mainly amorphous.

On the other hand, the EELS and electron microdiffraction of the middle region (P_3 and P_4) clearly showed the presence of Si crystallites. This corresponds well to the high concentration of crystallites in the films with a thickness range of 1000~3000 nm.

A lower concentration of Si nanocrystallites is expected near the top surface region (P_1) of the thick film, which can be attributed to the local distribution of stress within the film. The size and concentration of Si crystallites are influenced significantly by the local distribution of stress within the films.

5. Conclusion

The effect of film thickness on the nanostructural, chemical and mechanical features of the nc-Si:H films was investigated. The films were deposited by PECVD at a RF power of 150 W using SiH_4 and H_2 as the source gases for a deposition time ranging from 10 to 360 min.

The mean Si nanocrystallite size in the films increased from ~6 to ~8 nm with increasing film thickness from 260 to 4150 nm. The nanocrystallite volume fraction changed from ~7.5 to ~45%, and the elastic modulus increased from 135 to 147 Gpa. The relative proportion of Si–H bonds in the 4150 nm thick films (deposited at 360 min) was ~74.5%. The formation of Si nanocrystallites is closely related to local chemical bonds as well as to the structural energy state of the films.

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Research Article

High-Efficiency 6″ Multicrystalline Black Solar Cells Based on Metal-Nanoparticle-Assisted Chemical Etching

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Multicrystalline silicon (mc-Si) photovoltaic (PV) solar cells with nanoscale surface texturing by metal-nanoparticle-assisted etching are proposed to achieve high power efficiency. The investigation of average nanorod lengths from 100 nm to 1 μm reveals that the Si wafer decorated with 100 nm thick nanorods has optical reflection of 9.5% inferior than the one with 1 μm thick nanorods (2%). However, the short nanorods improve the doping uniformity and effectively decrease metal contact resistance. After surface passivation using the hydrogenated SiO_2/SiN_x (5 nm/50 nm) stack, the minority carrier lifetime substantially increases from 1.8 to 7.2 μs for the 100 nm-thick nanorod solar cell to achieve the high power efficiency of 16.38%, compared with 1 μm thick nanorod solar cell with 11.87%.

1. Introduction

Solar energy is one of the green energy techniques and has drawn a lot of attention more than thirty years. In 2010, global photovoltaic (PV) solar cell production generated 20.5 GW with a growth of 139% Y/Y, compared with 9.86 GW in 2009 [1]. PV solar cell industry becomes a fast-growing energy generation technology in which crystalline silicon (c-Si) as the foundation stone takes the market share about 86.5%, compared with the thin film products at 13.5% [1, 2]. Multicrystalline Si (mc-Si) PV solar cells occupy 55.5% production while single crystalline Si (sc-Si) ones share 31%. The main market trend in solar cells development involves a move toward to mc-Si solar cells due to the cheaper material and fabrication cost and potential application in remote and undeveloped regions where people eagerly need the supply of energy.

In order to increase the competitiveness of mc-Si solar cells, the solar power efficiency currently has to be improved for the replacement of fossil fuels, particularly via reduction of optical loss and eletrical loss. Antireflection (AR) coating plays a significant role on the enhancement of light absorption in the broadband spectrum range from near-UV to near-infrared. Without proper AR treatment on the surface of the c-Si solar cells, nearly 37% solar irradiation is reflected under terrestrial solar irradiation Air Mass 1.5 (AM 1.5) [3]. In the AR coating development of solar cells, the surface texturing techniques using micropyramids and subwavelength nanostructures are widely adopted for increasing light trapping on the Si solar cells [4–18]. Micropyramids with multilayers and graded-index AR coating have demonstrated to effectively reduce optical reflection in broad light spectrum, especially outside the visible band [6, 7]. Nevertheless, AR coating materials such as silicon oxide (SiO_2) and silicon nitride (SiN_x) inevitably absorb sunlight to some degree, reducing light transmission to the underling Si substrate [7, 8]. Subwavelength nanostructures have the characteristics of inherently excellent broadband antireflection properties (a low optical reflection of less than 5% in the wavelength range from 300 to 1000 nm) and become a promising candidate for achieving a high poewer efficiency solar cell due to intensive suppression of optical loss. Several methods such as metal-nanoparticle (NP-) assisted etching [9–16], ICP etching [17–19], and electrochemical etching [20] have been proposed to fabricate Si nanostructures among which the cost-effective metal-NP-assisted etching emerges as a mainstream fabrication technique for texturing large-area Si wafers.

At the present time, nanostructured solar cells do not have the high power efficiency as expected from the advantage of the excellent optical antireflection property. The nanostructures extruding from the silicon substance cause nonuniform distribution of dopants and influence the underlying p-n junction, which lead to the large leakage current and degrade the cell performance. Besides, the numerous surface defects and dangling bonds at the ultrahigh surface area of Si nanostructures accelerate the combination of photogenerated minority carriers, limiting the power efficiency of nanostructured solar cells [9, 10]. In this paper, the nanostructured silicon wafers (black silicon wafers, BSWs) are fabricated into PV solar cells based on metal-NP-assisted etching for increasing the broadband light trapping. The dimension of nanorods on black Si solar cells is investigated to achieve better p-n junction property, lower contact resistance, and higher power efficiency. Besides, the SiO_2/SiN_x stack is proposed to effectively passivate the nanostructured surface and simultaneously improve antireflectivity.

2. Experimental Details

6″ p-type (100) sc-Si and mc-Si solar wafers with thickness of 180 μm and doping density of 10^{15} cm^{-3} were used to characterize the optical antireflection by texturing the surface using metal-NP-assisted etching. All Si wafers were treated by Piranha clean for 10 min and then rinsed by DI water for 10 min. After cleaning, the silicon wafers were immersed into a Teflon bench containing metal-NP-assisted etching mixture at 20°C. The etching mixture contains DI water/HF (49%)/H_2O_2 (30%)/$AgNO_3$(0.1 M) with the volume ratio of 40 : 20 : 4 : 1. underetched for 18 s to 3 min, the nanorods generate different lengths on the Si surface. The as-etched BSWs were cleaned by H_2NO_3 (79%) and H_2O_2 (31%) to remove residual silver (Ag) nanodendrites on the wafer surface. Some fabricated 6″ BSWs were used for investigation on morphology, optical reflection, and carrier lifetime.

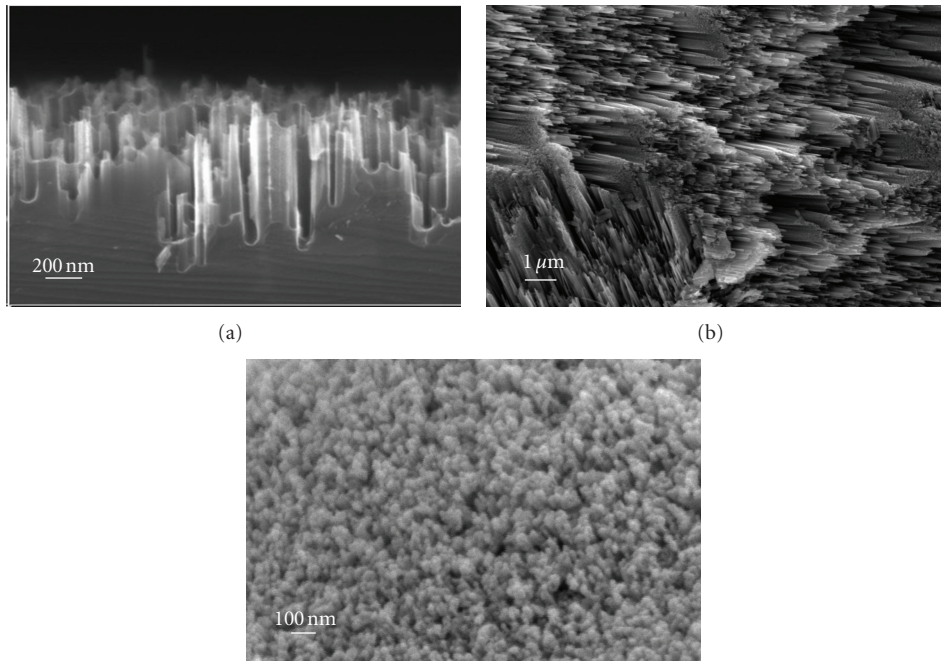
For the solar cell fabrication, n-type emitter was generated by doping the p-type silicon with phosphorus oxychloride ($POCl_3$) diffusion, forming a planar p-n junction underlying the nanorods. The $POCl_3$ diffusion was performed in a quartz tube with a temperature of 930°C. The whole nanorods are ought to be n type after the diffusion. A diluted HF solution was used to remove the phosphosilicate glass (PSG) layer. The surface passivation of the BSWs using SiO_2/SiN_x stack was performed as the following steps. Firstly, rapid thermal oxidation (RTO) was processed in a quartz furnace tube at 900°C for 15 s. A 5 nm-thick SiO_2 was formed on the surface of the silicon nanorods as the intermediate layer. The deposition of a 50 nm-thick Si_3N_4 single layer was followed using high density plasma chemical vapor deposition (HDP-CVD; Duratek system Mutiplex Cluster CVD) at 375°C with a pressure of 30 mTorr. The ion induced plasma (ICP) power was 850 W and the flow rate of processing gas of SiN, NH_3, and SiH_4 was 75, 24, and 12 sccm, respectively. Hydrogenation of BSWs was performed using forming gas (5% H_2 and 95% N_2) at 400°C for 30 min. Thermal evaporation of Al on the back side was used to remove the parasitic p-n junction via the built back side surface field. The front contact grids were screen-printed with a co-firing step. After the process, the fabricated black Si solar cells were used to perform electroluminescence (EL) and power conversion efficiency tests.

The morphology of the silicon nanostructures on the BSWs was observed by field-emission scanning electron microscopy (FESEM, Carl Zeizz, Ultra 55). Optical reflection of the BSWs was characterized using hemispherical reflection spectroscopy with a UV-Vis spectrometer (BWtek, BRC111A) and an integrated sphere (Ocean Optics, ISP 30-6-R). Effective carrier lifetime was obtained by microwave photoconductance decay (μ-PCD) technique (SEMILAB, WT-2000). Electroluminescence technique was used to measure the uniformity of doping. The characteristics of nanostructured Si solar cells were measured using Newport 1000 W class A solar simulator (91192A) with Keithley2400 source meter under AM 1.5 simulation (100 mW/cm^2 at 25°C).

3. Results and Discussion

3.1. Morphology of Black Silicon Wafers. The morphology of silicon nanorods can be affected by either etching mixture concentration or etching time. Both sc-Si and mc-Si wafers were immersed in the etching mixture from 18 s to 3 min to form BSWs. Surface geometry of BSWs was analyzed by FESEM. Figure 1(a) shows the cross-sectional view of the (100) sc-BSW where the randomly distributed nanorods are perpendicular to the wafer surface, indicating the nanorods formed by metal-NP-assisted etching developing mainly along the ⟨100⟩ direction. However, the length of nanorods is randomly distributed and not all the nanorods have the same length because some of the nanorods are laterally attacked by the subsequent supplement of Ag NPs and the violent Si etching under high concentration of HF (49%). For mc-Si, the grains with intrinsic different crystalline orientations were also etched primarily along the ⟨100⟩ direction, leaving the ⟨100⟩ nanorods on the wafer. The nanorod direction is kept the same within one grain but changed abruptly when crossing the grain boundary as shown in Figure 1(b). These random nanorods have an average length of 1 μm after etched for 3 min. Figure 1(c) shows that beign the Si nanorod array on ms-Si has the average nanorod length about 100 nm after etched for 18 s. From the measurement, Si in the metal-NP-assisted etchant has an average etching rate of 0.33 μm/min.

The experiment results show the metal-NPs assisted etching recipe developed by our group etches Si primarily along the ⟨100⟩ direction. The etching mechanism is predominant by the Ag (catalyst) network formed via the deposition of Ag nanoparticles on the Si surface. Ag catalyses the etching behavior of Si underneath the Ag network primarily along two etching directions of ⟨100⟩ and ⟨110⟩, showing anisotropic etching [9–14]. However, Ag nanoparticles sometime penetrate through the protected mask region and spontaneously attacked the silicon substrate underneath the mask [10].



(a) (b)

(c)

Figure 1: After metal-NP-assisted etching, the random size distribution of Si nanorods on black silicon wafers (BSWs) is averaged. (a) 600 nm-thick nanorods formed on ⟨100⟩ silicon wafer. The orientation of nanorods is normal to the silicon surface, revealing that the anisotropic etching is primarily along ⟨100⟩. (b) The nanorods built on grains with different crystalline orientations are clearly distinguished. The nanorods have the average length of 1 μm after etched for 3 min. (c) 100 nm-thick nanorods on mc-BSW after 18 s etching.

3.2. Optical Reflection of Black Silicon Wafers. Reduction of optical reflection is considered a significant step to fabricate a high-efficiency solar cell because it would effectively decrease optical loss and increase the short-circuit current of solar cell. For mc-Si, each grain has distinct crystal orientations separated by the grain boundary, exhibiting different optical reflection in response to normal incidence. For as-cut mc-Si wafer, the average optical reflection can be higher than 28%.

The influence of nanorod length on the optical reflection of mc-BSWs was investigated in a broad spectrum from 400 to 1000 nm. After metal-NP-assisted etching, the average length of nanorods distributed from 100 nm to 1 μm. For each mc-BSW, there was small deviation of optical reflection between grains due to intrinsic crystalline orientation. In Figure 2, the Si surface decorated with average 600 nm-thick nanorods has the optical reflection varied from 5 to 4% (grain A and grain B). Some grains showed up as gray and some appeared as black. The color difference between grains can be easily distinguished by the naked eye. Therefore, there were five different points measured in order to obtain the average value of optical reflection for each BSW. The experimental results are shown in Figure 3. The reflection from BSWs is efficiently suppressed compared with the as-cut solar wafer. The 100 nm-thick nanorods reduced the optical reflection to 9.5% while the 1 μm-thick nanorods had the lowest optical reflection of 2%. The optical reflection is approximately inversely proportional to the nanorod length. The excellent antireflection property may be attributed to the broadband antireflection of the fabricated subwavelength nanorods and the nonstopped adsorption of the incoming light after the multiple reflections in the long nanorods [21].

The BSWs with surface texturing using 100 nm-thick, 600 nm-thick, and 1 μm-thick nanorods were further fabricated into PV solar cells. In Figure 4, the 1 μm-thick nanorod mc-Si solar cell had considerably lower optical reflection of 2% from 400 to 1000 nm, involving the visible light spectrum, which accounts for the dark black color observed by the naked eye. The grain boundary was hardly distinguishable due to the excellent light absorption, compared with the 100 nm-thick nanorod PV cell. The color change indicates that the fabricated nanorods remarkably suppress the optical reflection of the solar wafer, which gives a potential to carry out the high efficiency solar cells.

3.3. Surface Passivation of Black Silicon Wafers. Nanostructured BSWs have the ultrahigh surface area compared with the as-cut silicon solar wafers and the micropyramid textured silicon solar wafers, which bring out more surface defect states and dangling bonds and aggravate the minority carrier trapping. The as-cut solar wafer had a carrier lifetime of 2.0 μs while the 1 μm-thick nanorod BSWs had a shorter average carrier lifetime of 1.8 μs (see Table 1), which inevitably decrease the power efficiency due to the high surface recombination velocity of minorities in Si nanostructure [9–11].

It is of desire to develop a highly effective surface passivation layer with a low optical reflection that not only reduces the density of surface states but also leads to

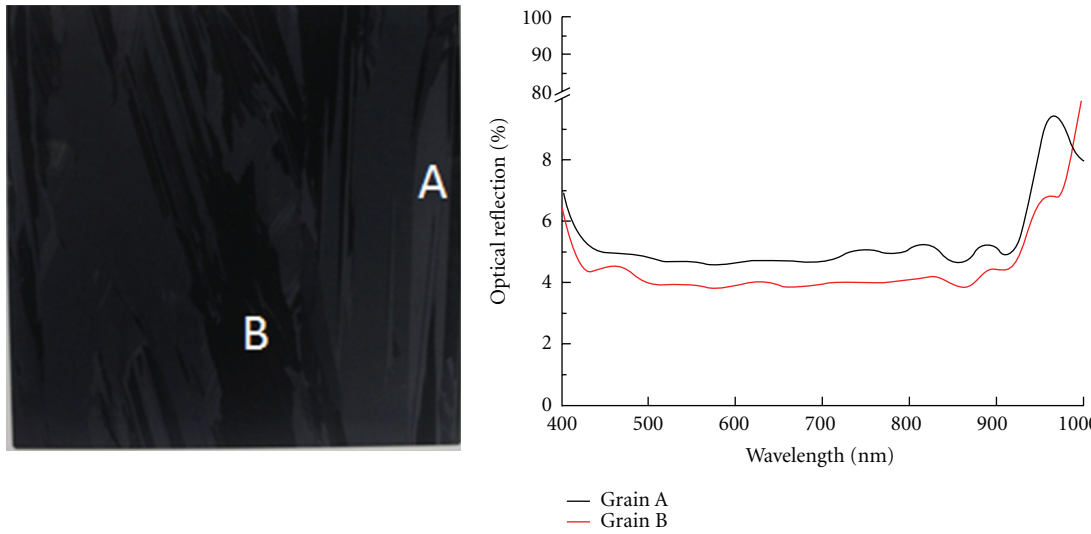


Figure 2: The optical reflection of 6″ mc-BSW with surface texture of 600 nm-thick nanorods. Each grain is easily distinguishable by the grain boundary and exhibits the different optical reflections. Two individual grains (grain A and grain B) show the average optical reflections of 5 and 4% in a broad spectrum from 400 to 1000 nm.

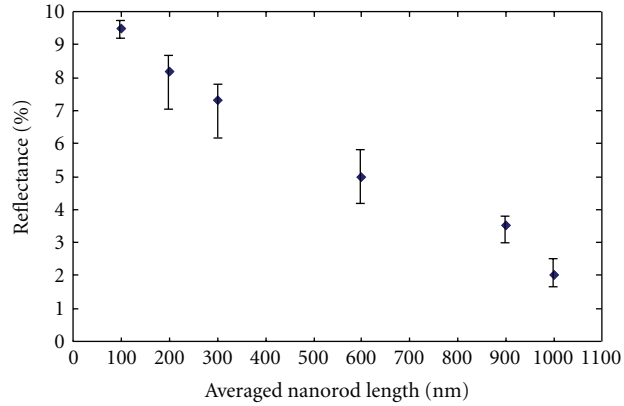


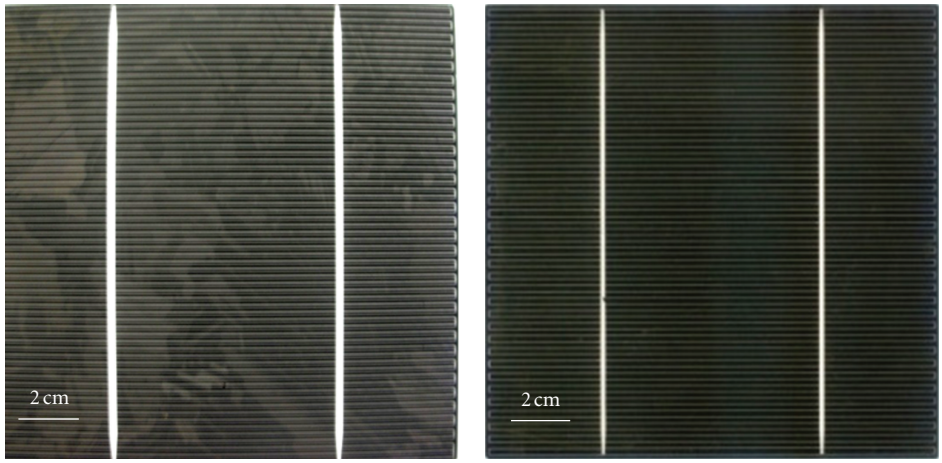
Figure 3: The optical reflection of 6″ mc-BSWs with different nanorod lengths. The average length on BSWs distributes from 100 nm to 1 μm. The reflection is approximately inversely proportional to the average nanorod length. The reflection is about 9.5% for BSW decorated with 100 nm-thick nanorods and suppressed to 2% for BSW with 1 μm-thick nanorods.

Table 1: Effective minority carrier lifetime of Si solar wafers.

Sample	Effective lifetime (μs)
As-cut	2.0
Black	1.8
Black + $SiO_2 + SiN_x$	3.5
Black + $SiO_2 + SiN_x$ (hydrogenated)	7.2

high power efficiency on the nanostructured Si PV solar cells. The SiO_2/SiN_x passivation stack with SiO_2 as the intermediate layer is proposed to improve the conformity of the passivation layer on nanorods. The 5 nm-thick SiO_2 formed by rapid thermal oxidation (RTO) was firstly used to cover the whole surface of SiNWs and subsequently deposited with a layer of 50 nm-thick SiN_x by PECVD. The black solar wafer with SiO_2/SiN_x stack had the effective minority carrier lifetime of 3.5 μs. After further hydrogen passivation, the carrier lifetime substantially increased to 7.2 μs because the hydrogen atoms can penetrate into the defects to build the Si–H bonds, effectively decreasing the defect density. The hydrogenated SiO_2/SiN_x stack passivation has the potential to realize the nanostructured PV solar cells with high power efficiency and used in for passivating the mc-Si PV solar cells.

3.4. Performance of Black Si PV Solar Cells. Nanostructured BSWs have the characteristics of excellent antireflection properties and become the promising candidate for achieving a high-efficiency PV solar cell. However, nanorods extruding from the silicon surface would cause the nonuniform distribution of dopants and influence the conformity of



(a) (b)

Figure 4: 6″ mc-Si photovoltaic (PV) solar cells textured with average (a) 100 nm-thick and (b) 1 μm-thick nanorods. The feature difference is remarkable for the two solar cells. The 1 μm-thick nanorods generate the dark black color easily recognized by the naked eye and the grain boundaries also become nondistinguishable compared with the solar cell with surface textured using 100 nm-thick nanorods.

Table 2: I-V characteristic of black Si solar cells.

Sample	η (%)	V_{oc} (mV)	I_{sc} (mA/cm^2)	FF (%)	R_s(mΩ)	R_{sh}(Ω)
0.1 μm black Si solar cell	16.38	624	36.1	76.2	2.84	35.82
0.6 μm black Si solar cell	14.05	606	31.93	74.05	3.14	33.36
1.0 μm black Si solar cell	11.87	588	31.8	66.32	4.67	18.05

the underlying p-n junction, which leads to the decrease of short circuit current (I_s) and the shunt resistance (R_{sh}) and degrades solar cell performance. Thus, BSWs with different average nanorod lengths (100 nm, 600 nm, and 1 μm) were fabricated into PV solar cells to investigate the length effect on solar cell performance. The current-voltage (I-V) characteristics of nanostructured black Si solar cells were measured under a simulated AM 1.5 illumination condition at room temperature and the results are shown in Table 2.

The 1 μm-thick nanorod Si PV solar cells had the power efficiency (η) of 11.87%, the open-circuit voltage (V_{oc}) of 588 mV, short-circuit current density (J_{sc}) of 31.8 mA/cm^2, and fill-factor (FF) of 66.32. The large series resistance (R_s) of 4.67 mΩ resulted from the poor electrical contact between screen-printed contact grids with the sharp and narrow nanorods led to the low FF and the smaller η. The small shunt resistance (R_{sh}) of 18.05 Ω may be resulted from the nonuniform distribution of dopant below the nanorods. For the solar cells with short nanorods (100 nm), the performance factors of η (16.38%), V_{oc} (624 mV), J_{sc} (36.1 mA/cm^2) and FF (76.2) are better than those of the 600 nm-thick and 1 μm-thick nanorod solar cells. Besides, R_s decreased to 2.84 mΩ due to the smoother short nanorods, which increases the contact conformity between metal and nanorods and reduces the voids existed in sharp nanostructures. R_{sh} of 35.82 Ω is better than 600 nm-thick and 1 μm-thick nanorod solar cell, indicating that the phosphors diffusion is uniformly distributed through the short nanorods and generates a good p-n junction.

PV solar cells with longer Si nanorod array have superior antireflection phenomenon but inevitably suffer from the nonuniformity of the dopant diffusion. The dopant uniformity was investigated by electroluminescence (EL) where EL applies a forward voltage and current on solar cell to generate localized irradiance in the near infrared (NIR) range of the spectrum due to carrier recombination. Figure 5 shows the EL image of solar cells with distinct nanorod lengths including 1 μm, 600 nm, and 100 nm. The dark regions originated from the nonuniform distribution of dopant act as defects in solar cells, largely suppressing the electron-to-photon conversion efficiency. The solar cell with longer nanorods (1 μm) had the largest dark region and the lowest power efficiency (11.87%). On the other hand, the 100 nm-thick nanorod solar cell emitting the strong light intensity of NIR light from almost the sample surface had the superior power efficiency of 16.38%.

A tradeoff between optical antireflection and diffusion uniformity of doping is strongly related to the length of the nanorod. Although short nanorods cannot suppress optical reflection as well as long nanorods [22], they characterized the good doping uniformity and decreased contact resistance. Furthermore, the surface passivation using SiO_2/SiN_x stack intensively reduced the surface electron-hole recombination on the sidewall of the nanorods and contributed to the improvement of the power efficiency of black Si solar cells, compared with other nanostructured solar cells [9–11, 13, 14].

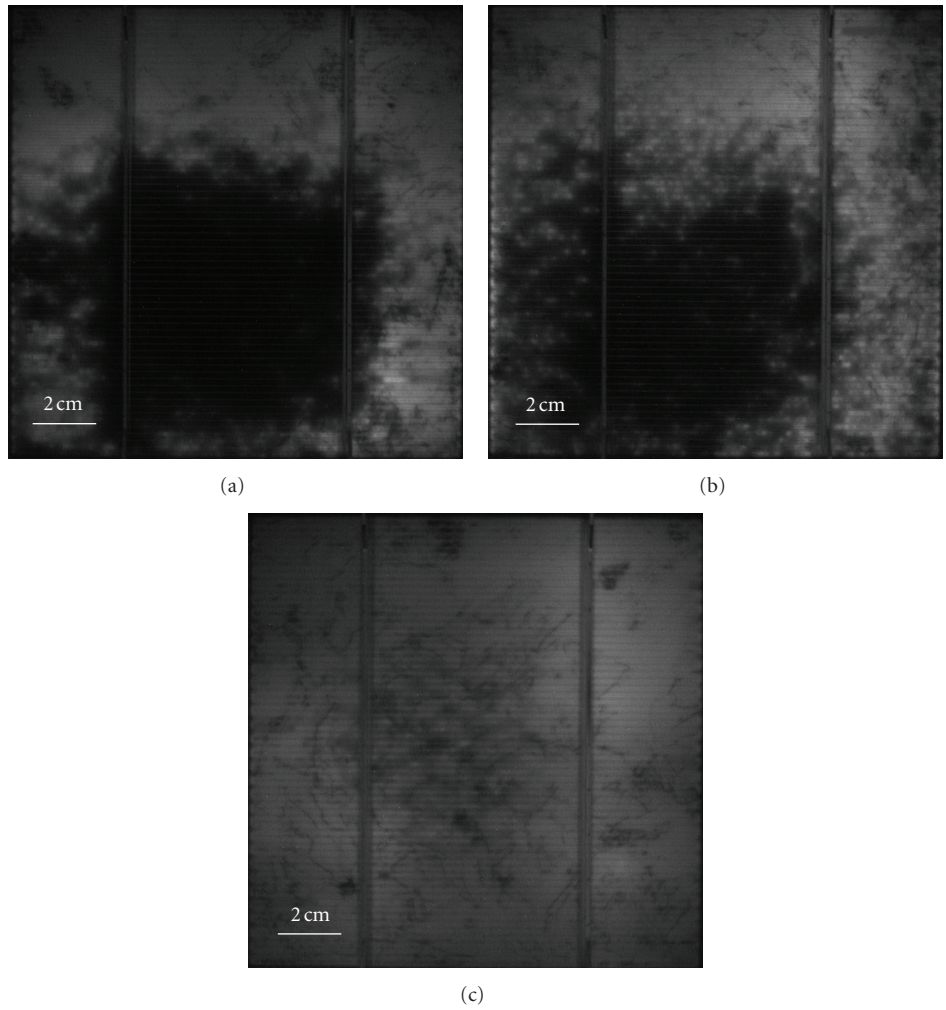


Figure 5: 6″ mc-Si PV solar cells with surface texture using 1 μm, 600 nm, and 100 nm-thick nanorods shown from (a) to (c) are tested by electroluminescence (EL) to investigate the doping uniformity in cells. The lateral nonuniform doping introduces defects (the dark regions) in solar cells, largely suppressing the minority carrier lifetime and the IR light irradiation. The solar cell decorated with 100 nm-thick nanorods has few dark areas, showing the better doping uniformity.

4. Conclusion

Solar cells with surface decoration using pyramids and nanorods have been widely used to improve the light absorption in substrate. However, there is a tradeoff between light trapping, contract resistance, and doping uniformity, reflecting the importance of determining the appropriate nanorod length on the black Si PV solar cells. 6″ mc-Si solar cell using 100 nm-thick nanorod surface texturing has a power efficiency of 16.38% higher than the one with 1 μm-thick nanorod (11.87%). Although the 100 nm-thick nanorods have optical reflection of 9.5% inferior than the 1 μm-thick-nanorods (2%), these short subwavelength structures improve doping uniformity, junction performance, and decrease contact resistance, leading to high power efficiency. The nanostructured solar cells have the same fabrication process as the commercial Si solar cells except for the metal-NP-assisted chemical etching. In the near future, the fabrication of surface nanostructures can be easily integrated into the industrial fabrication process and provides the competitiveness in providing mc-Si solar cells with high power efficiency.

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Research Article

17.6% Conversion Efficiency Multicrystalline Silicon Solar Cells Using the Reactive Ion Etching with the Damage Removal Etching

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For lower reflectance, we applied a maskless plasma texturing technique using reactive ion etching (RIE) on acidic-textured multicrystalline silicon (mc-Si) wafer. RIE texturing had a deep and narrow textured surface and showed excellent low reflectance. Due to plasma-induced damage, unless the RIE-textured surfaces have the proper damage removal etching (DRE), they have a drop in V_{oc} and FF. RIE texturing with a proper DRE had sufficiently higher short circuit current (I_{sc}) than acidic-textured samples without a drop in open circuit voltage (V_{oc}). And in order to improve efficiency of mc-Si solar cell, we applied RIE texturing with optimized DRE condition to selective emitter structure. In comparison with the acidic-textured solar cells, RIE-textured solar cells have above 200 mA absolute gain in Isc. And optimized RIE samples with a DRE by HNO_3/HF mixture showed 17.6% conversion efficiency, which were made using an industrial screen printing process with selective emitter structure.

1. Introduction

In order to improve the solar cell performance, incoming light in the cell has to be coupled into the cell and transformed into electrical energy more effectively. Losses due to reflection and transmission of the incident light have to be reduced to increase the solar cell efficiency. A texture causes a multiple reflection on its surface. Therefore, the amount of collected light into the substrate, depending on the amount reflections, increases. This increase of collection, together with the larger average path length of the light in the substrate, causes an increased possibility of absorption [1].

Numerous techniques for texturing mc-Si have been examined in the past. Many approaches have been based on isotropic wet acidic etching. This method does not provide the extremely low reflection but does have the advantages of being relatively easy to implement and low cost. Some have focused on the use of RIE, either in conjunction with a mask to achieve large, regular features or without a mask to produce much smaller and more random texture [2]. RIE is a kind of plasma etching, not only the chemical etching of the plasma species, but also the kinetic energy of its ions. From the time plasma etching was applied in the semiconductor industry for patterning Si substrates, it is known that plasma etching, under certain conditions, causes a surface texture of a very high roughness [3]. Reflectivity can be minimized to below 1% [4]. Decrease in reflectivity does not automatically lead to an improvement of cell efficiency. It is known that a less rough form of this texture can be used for more effective light coupling into Si substrates [5, 6]. The reflectivity can be well controlled by RIE. This way of texturing is ideal for very fragile substrates. According to previous studies, RIE textured surface has shown extremely low reflectance [7]. However, surface damage may be caused by RIE-texturing [8] and result in a high surface recombination velocity due to the enlarged surface. RIE-textured cells have reduced quantum efficiency in the short wavelength, unless the RIE-textured surface receives the proper DRE [7]. Because problem of RIE may be that the energetic ions can introduce damage in the Si material [9], so Carriers have a large chance of

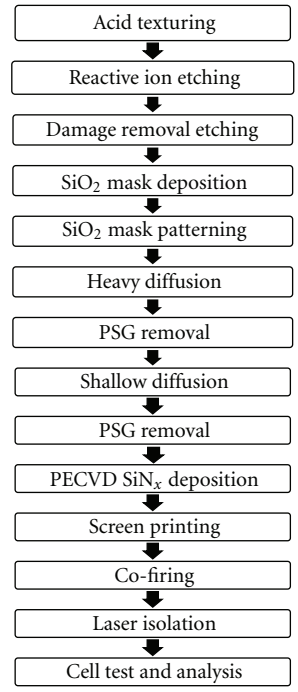

Figure 1: Fabrication process for screen-printed selective emitter mc-Si solar cells with RIE texturing.

recombining at the needles of the surface and will not reach the p-n junction. In order to remove this problem, we studied DRE using HNO_3/HF mixture with various etching time. The aim of this work was to find DRE conditions that create a texture with a low reflectance and without a drop of V_{oc} and FF, which obtains a maximum improvement for I_{sc} and conversion efficiency. And for high efficient mc-Si solar cell, we applied selective emitter technique on screen printing process with RIE texturing.

2. Experiment

The fabrication process is outlined in Figure 1. In this work, solar grade multi-crystalline silicon wafer of size $156 \times 156\,mm^2$, boron doped p-type, was used. And resistivity 1.9 ohm·cm and thickness 200 um were taken. The isotropic texturing of mc-Si wafer was carried out by using acidic solutions. Then acid-textured Si wafers were processed in an RIE reactor. After RIE texturing, we investigated various DRE times with acidic solution (dilute HNO_3 and HF mixture) to determine which produces the highest cell performance with screen-printed solar cell process. A sequence with diluted KOH and HCl/HNO_3 treatments has been found not to affect the visual appearance of the texture structure. The textured surface was analyzed using a scanning electron microscope (SEM). SiO_2 layer was deposited as diffusion barrier mask. To form the selective emitter structure, mask was patterned by etch paste for heavily diffusion. These wafers was doped in conventional tube furnace using $POCl_3$ liquid source. The phosphorous silicate glass (PSG) and remaining SiO_2 was removed with a 10% HF solution simultaneously. A shallow diffused region is created by $POCl_3$ diffusion. A shallow diffused region is created by $POCl_3$ diffusion. After second diffusion, sheet resistance below the contact fingers were 20 Ω/□ and between fingers were 80 Ω/□, respectively. And PSG was removed with a 10% HF solution. The SiNx layer was deposited on the emitter, using direct PECVD. Refractive index and thickness of PECVD SiNx layer were 2.06 and 85 nm, respectively. Next, the Ag and Al pastes were screen-printed onto the front and back of each sample and cofired in a lamp-heated belt furnace. The cells were isolated using a laser, and the cells were tested using the solar simulator.

3. Results and Discussion

To improve cell efficiency, we applied RIE on mc-Si wafer and fabricated selective emitter mc-Si solar cells. First, we compare acidic- and RIE-textured surface morphologies and reflectance. Figure 2 shows SEM images of mc-Si wafer with acid- and RIE-textured surfaces. Figures 2(a) and 2(c) are only acid-textured surface, which has smooth and bowl-like features. Figures 2(b) and 2(d) are RIE-textured surface on acid-textured wafer. This has many nanosized features in dent. And it has many deeper features than only acid-textured surface which provide very dark looks. As can be seen Figure 3, RIE-textured surface have lower reflectance than acidic textured surface in all wavelength. Especially, reflectance of RIE textured surface is less than 10% in short wavelength. This is caused by deep and dense structures, as can be seen in Figure 2.

Table 1 shows the electrical performance parameters of mc-Si solar cells fabricated with acidic- and RIE- textured surface. These cells had 50 Ω/□ homogeneous emitter. As can be seen in Table 1, for the RIE-textured cell, despite the improvement in I_{sc}, cell efficiency decrease comes from a

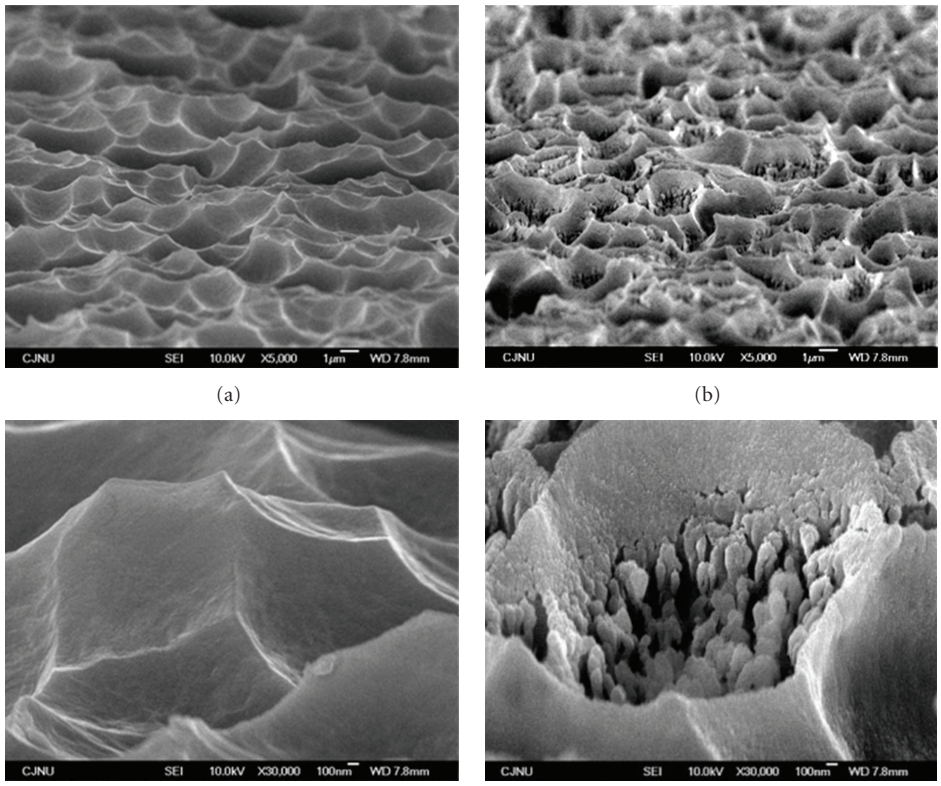

Figure 2: SEM images of textured surfaces: (a) acid textured surface 5000x, (b) RIE-textured surface 5000x, (c) acid textured surface 30000x, and (d) RIE-textured surface 30000x.

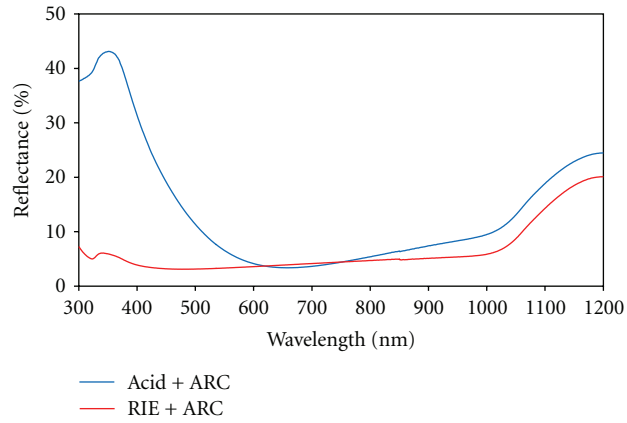

Figure 3: After antireflective coating, reflectance of acidic- and RIE-textured surfaces.

Table 1: The average electrical performance of homogeneous emitter mc-Si solar cell with acidic and RIE texturing.

	V_{oc} (V)	I_{sc} (A)	FF (%)	Eff. (%)
Acid texturing	0.626	8.241	77.97	16.54
RIE texturing	0.619	8.284	76.88	16.20
Difference	−0.007	+0.043	−1.09	−0.34

drop in V_{oc} and FF. The most main cause for this result is surface plasma damage by RIE texturing [8]. Because problem of RIE may be that the energetic ions can introduce damage in the Si material [9], so Carriers have a large chance of recombining at the needles of the surface and will not reach the p-n junction.

In order to remove plasma-induced damage, we studied DRE using HNO_3/HF mixture with various etching times. As can be seen in Figure 4, as DRE time increases, number of nanosized features decreases and textured surface was smoother. This result means that damaged surface was gradually removed by DRE. Figure 5 shows reflectance of acidic- and RIE-textured surfaces with various DRE times after antireflective coating. As DRE time increases, the reflectance

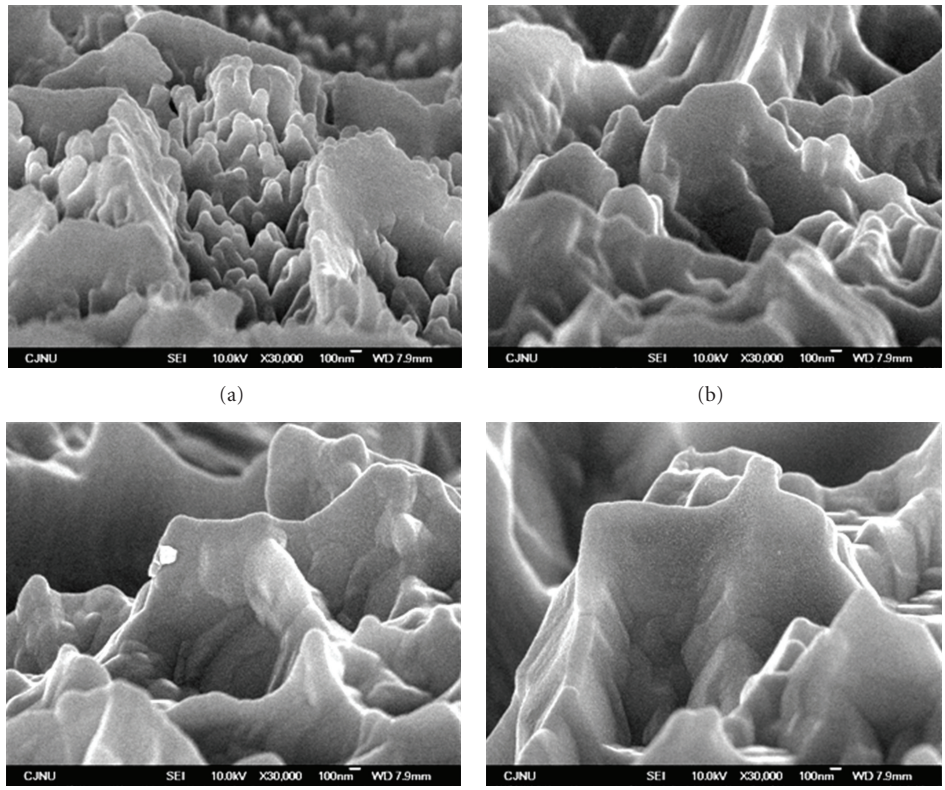

Figure 4: SEM images of RIE textured surface with various DRE times (30000x): (a) No DRE, (b) DRE 20 sec, (c) DRE 40 sec, and (d) DRE 60 sec.

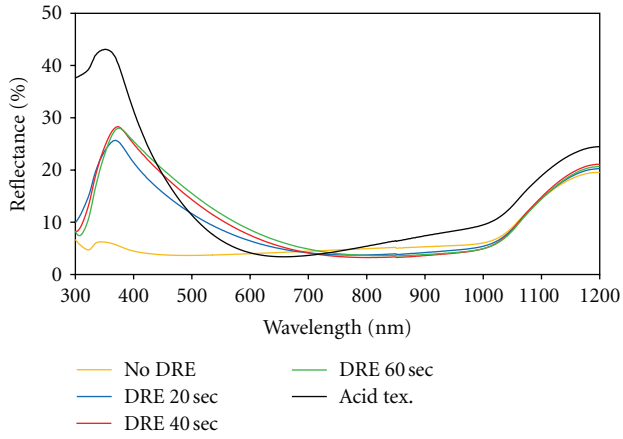

Figure 5: After antireflective coating, reflectance of acidic- and RIE-textured surfaces with various DRE time.

of RIE-textured surface approaches the acidic-textured surface, because the nano sized features formed during RIE process are becoming smooth by DRE. RIE-textured samples with DRE have lower reflectance than acidic-textued samples in the short wavelength region also that you can check again. So we can have a sufficiently higher I_{sc} than wet acidic-textured samples.

Figure 6 shows electrical characteristics of RIE-textured mc-Si solar cells with various DRE times. Applying DRE, all electrical factors (V_{oc}, I_{sc}, FF, and efficiency) of mc-Si solar cell had better results than without DRE. It seems that this was caused by removing plasma-induced damage. As can be seen in Figure 6(a), as the DRE time increases, V_{oc} was increased due to plasma damage etching. But, as the DRE time increases, I_{sc} was decreased as shown Figure 6(b). This is consistent with results of Figures 4 and 5. As DRE time increases, because the reflectance of textured surface gradually was higher, I_{sc} tends to decrease slightly. And we were confirmed the highest efficiency of mc-Si solar cell in DRE condition at 20 and 30 sec and achieved best cell efficiency applying homogeneous emitter structure.

To improve efficiency of mc-Si solar cell, we applied selective emitter structure with RIE texturing and optimized DRE condition. For selective emitter, SiO_2 layer was deposited as diffusion barrier mask and patterned by etch paste for heavily diffusion. These wafers were doped in conventional tube furnace using $POCl_3$ liquid source. The PSG and remaining SiO_2 were removed with a 10% HF solution simultaneously. A shallow diffused region is created by $POCl_3$ diffusion. After second diffusion, sheet resistance below the contact fingers was 20 Ω/□ and between fingers was 80 Ω/□, respectively.

Table 2 shows the result of electrical parameters of selective emitter mc-Si solar cells with acidic and RIE texturing. RIE-textured samples were applied by 20 sec DRE condition. The value of cell efficiency is average results of 5 wafers in an experiment with neighboring wafers in ingot. We achieved above 200 mA absolute I_{sc} gain in 6 inch mc-Si solar

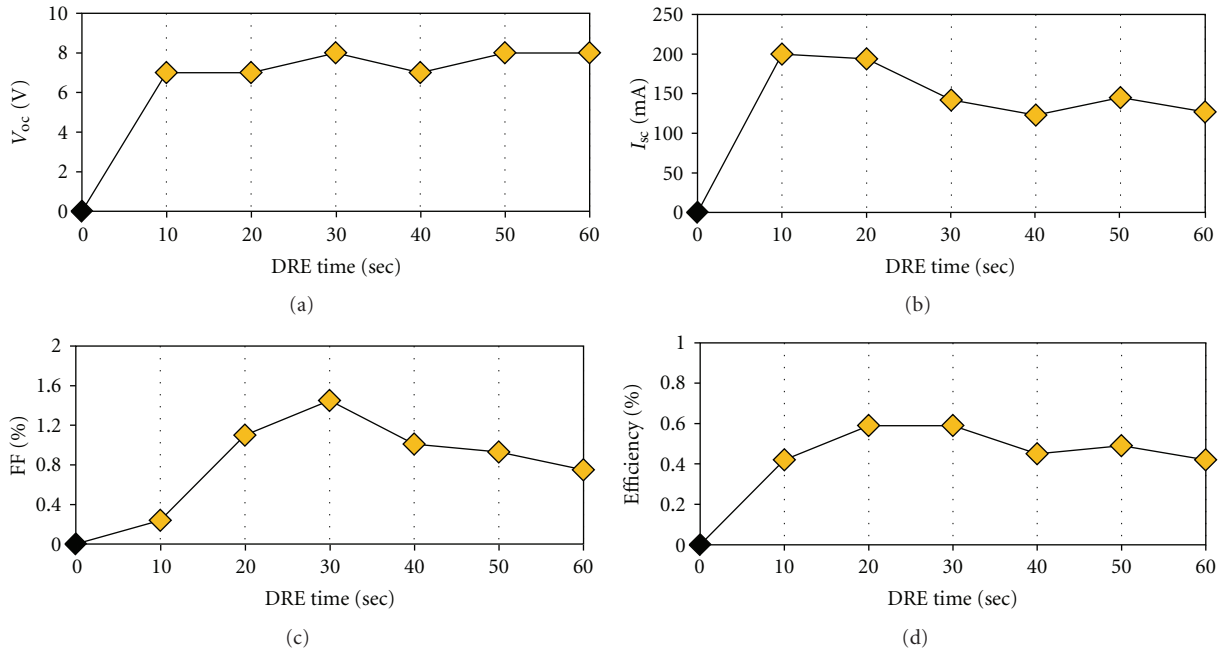

Figure 6: Electrical characteristics of RIE-textured mc-Si solar cells with various DRE times. (a) Open circuit voltage (V_{oc}). (b) Short circuit current (I_{sc}). (c) Fill factor (FF). (d) Conversion efficiency.

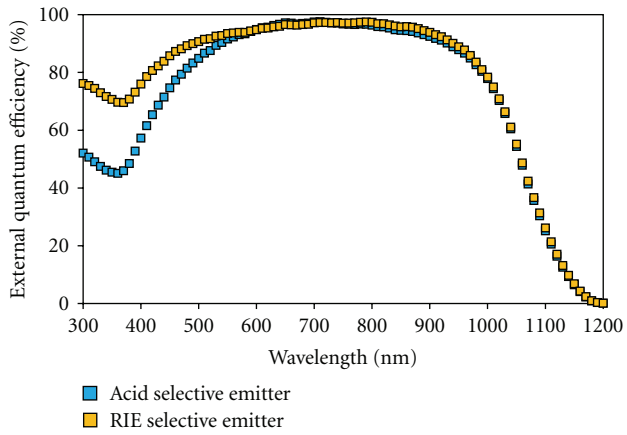

Figure 7: External quantum efficiency (EQE) of selective emitter mc-Si solar cells with acidic- and RIE-textured surface.

Table 2: The average electrical performance of selective emitter mc-Si solar cell with acidic and RIE texturing.

	V_{oc} (V)	I_{sc} (A)	FF (%)	Eff. (%)
Acid texturing	0.633	8.517	78.1	17.3
RIE texturing (DRE 20 sec)	0.632	8.685	77.9	17.6

cell by RIE- than acid-textured cells without drop of V_{oc} and FF. And optimized mc-Si solar cell with RIE-textured surface showed 17.6% conversion efficiency, which were made using an industrial screen printing process with selective emitter structure. And the external quantum efficiency (EQE) measurements are evaluated for the selective emitter solar cells with acidic- and RIE-textured surface, as Figure 7 shows. It is clear that the selective emitter solar cell with the RIE texturing has the improved quantum efficiency compared to acidic texturing for wavelength below 600 nm. This results in low reflectance without plasma-induced damage.

4. Conclusion

RIE texturing had a deep and narrow textured surface and showed excellent low reflectance. Due to plasma-induced damage, unless the RIE-textured surfaces have the proper DRE, they have a drop in V_{oc} and FF. The 20 and 30 sec DRE times with acidic solution (HNO_3 and HF mixture) have the best conversion efficiency by improving the I_{sc} without a drop in V_{oc} and FF. In order to improve efficiency of mc-Si solar cell, we applied 20 sec DRE condition to selective emitter structure. In comparison with the acidic-textured solar cells, mc-Si solar cells with RIE texturing have above 200 mA absolute gain in I_{sc}. Optimized mc-Si solar cell with RIE-textured surface showed 17.6% conversion efficiency, which was made using an industrial screen printing process with selective emitter structure. And EQE measurements show the RIE texturing has the improved quantum efficiency compared to acidic texturing for wavelength below 600 nm. This result in low reflectance without plasma-induced damage.

Acknowledgment

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Research Article

Laser Process for Selective Emitter Silicon Solar Cells

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Selective emitter solar cells can provide a significant increase in conversion efficiency. However current approaches need many technological steps and alignment procedures. This paper reports on a preliminary attempt to reduce the number of processing steps and therefore the cost of selective emitter cells. In the developed procedure, a phosphorous glass covered with silicon nitride acts as the doping source. A laser is used to open locally the antireflection coating and at the same time achieve local phosphorus diffusion. In this process the standard chemical etching of the phosphorous glass is avoided. Sheet resistance variation from 100 Ω/sq to 40 Ω/sq is demonstrated with a nanosecond UV laser. Numerical simulation of the laser-matter interaction is discussed to understand the dopant diffusion efficiency. Preliminary solar cells results show a 0.5% improvement compared with a homogeneous emitter structure.

1. Introduction

Selective emitter technology can provide a significant increase in solar cell efficiency, but today most of the approaches need many processing steps and alignment procedure [1]. In this context, laser processing provides a good opportunity to achieve such a structure with a minimum number of technological steps [2–5] and without alignment when coupled with front side electrochemical metallisation [6]. Recent results have shown that around a 0.5% increase in solar cell efficiency could be obtained when using phosphosilicate glass (PSG) as a source of dopants to form highly doped areas on the emitter side according to Process A in Figure 1. In the perspective of a complete self-aligned process, a reduced number of technological steps is proposed to form selective emitters on the front surface of p-type silicon wafers (Figure 1, Process B). In this process, a homogenous emitter is formed by thermal diffusion of phosphorous. The resulting PSG layer is covered with silicon nitride (SiN_x) for passivation and antireflection purposes. Ablation of the SiN_x coating and dopant diffusion are then performed simultaneously with a pulsed laser before metallisation. Wet chemical etching of the PSG layer is therefore avoided and a self-aligned metallisation process can be developed with electrochemical deposition techniques. Numerical simulation of laser-matter interaction is presented to explain the heat-assisted diffusion mechanism and is compared to sheet resistance measurements. Laboratory scale solar cells are fabricated to compare homogeneous emitter and selective emitter structures. Spectral response and *I-V* measurements are used to characterise the solar cells.

2. Numerical Simulation of the Laser-Matter Interaction

Melting, evaporation, and dopant diffusion are the main mechanisms that result from the laser-matter interaction. In a nanosecond regime, if the optical and thermal penetration depths are much smaller than the diameter of the incident laser beam on the surface, the thermal effects can be described by a two-dimensional heat-transfer equation [7]. The diffusion process can be estimated by solving at the same time Fick's second law. To estimate the impact of the

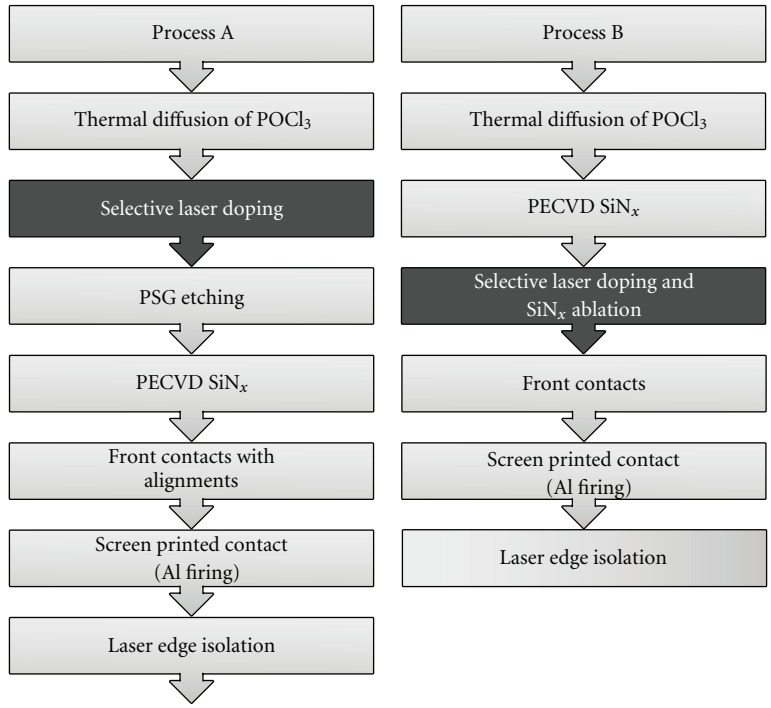

Figure 1: Processes for selective emitter solar cells with (Process A) and without (Process B) chemical etching and alignment steps.

laser parameters on the emitter formation, the finite element software COMSOL was used to solve these two equations [8]:

$$\rho(T)C_p(T)\frac{\partial T}{\partial t} = \nabla[k_{\text{th}}(T)\nabla T] + Q, \tag{1}$$

$$\frac{\partial c}{\partial t} = \nabla[D(T)\nabla c]. \tag{2}$$

$\rho(T)$ is the material density, $C_p(T)$ the specific heat capacity, T the temperature, t the time, k_{th} the thermal conductivity, Q the heat source in the volume due to the absorbed laser power, c the phosphorous concentration in silicon, and $D(T)$ the diffusion coefficient of the phosphorous atoms in silicon. The heat source term Q in the heat-transfer equation corresponds to the absorbed laser power and can be written as follows:

$$Q = (1 - R(T))\alpha(T)P_{\text{in}}(x,t)I(y). \tag{3}$$

$\alpha(T)$ is the material absorption coefficient, $R(T)$ the surface reflectivity, $P_{\text{in}}(x,t)$ the incident laser power, and $I(y)$ the relative intensity given by the Beer-Lambert law. The beam is considered to have a Gaussian shape in time and space:

$$P_{\text{in}}(x,t) = P_0 \exp\left\{-\left(\frac{t-t_0}{\tau/2}\right)^2\right\}\exp\left\{-\left(\frac{x}{r}\right)^2\right\}. \tag{4}$$

P_0 is the peak power of the laser beam, t_0 the time shift, τ the pulse duration, and r the beam radius at half height.

Temperature dependence of the physical properties of the materials was taken into account. The smoothed Heaviside function (flc2hs) implemented in COMSOL was used to describe the abrupt changes of material coefficients with temperatures. Latent heat of fusion was taken into account by reducing the heat-source term for the temperatures above fusion by the quantity $E_{\text{lm}} \cdot \rho/\tau$, where E_{lm} is the latent fusion heat, ρ the density and τ the pulse duration. In a first approximation, the texturation of the surface was not taken into account and a plan of symmetry was considered in order to minimize the calculation time. The absorption coefficient of silicon at 355 nm is around $10^8\ \text{m}^{-1}$ corresponding to a penetration depth around 10 nm. As a consequence, the minimum element size for calculation at the silicon surface was 1 nm. The substrate was divided in different areas in order to have a finer meshing under the irradiated area. The time parameter varied from 0 to 60 ns with a step of 1 ns and 0.1 ns during the laser pulse (from 10 ns to 40 ns). The sample geometry is represented in Figure 2.

For a better understanding of the role of each layer, temperature at the surface of silicon was calculated as a function of the laser fluence (Figure 3) for the different interfaces Si/air, Si/PSG/air, and Si/PSG/SiN_x/air. Temperature variation at the silicon surface can be explained by the thermal properties of the layers (mostly the thermal conductivity) and by the different reflection coefficient R of the surfaces. Laser doping efficiency is dependent on the temperature reached in silicon as the substrate has to be melted to allow efficient phosphorous diffusion into the junction. Indeed, the significant increase of the diffusion coefficient in the liquid state silicon ($\times 10^7$) permits phosphorus diffusion during the short time of laser-matter interaction (tens of nanoseconds). As shown in Figure 3, the structure Si/PSG/SiN_x/air needs

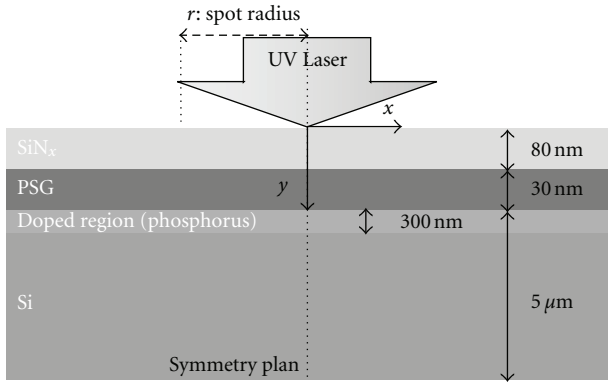

Figure 2: Sample geometry.

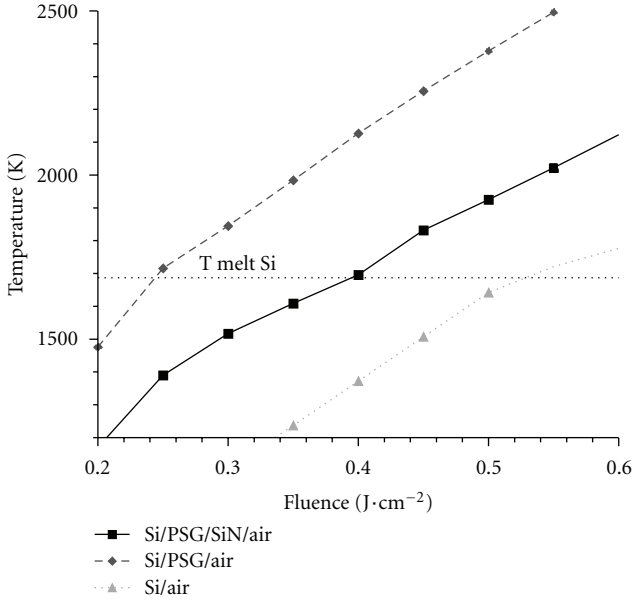

Figure 3: Simulated temperature versus laser fluence for different interfaces (Si/air, Si/PSG/air, Si/PSG/SiN/air).

more laser energy than the structure Si/PSG/air to melt the silicon substrate. Therefore a good control of the laser parameters is necessary to avoid heat-induced damages to the cell junction.

3. Experimental

Monocrystalline Cz silicon wafers with textured surfaces were used. Substrates were p-type with a thickness of 250 μm and a resistivity of 1 $\Omega\cdot$cm. Homogeneous n-doped emitters with sheet resistance of 80 Ω/sq and 100 Ω/sq corresponding to surface doping concentration of 3.5×10^{19} cm^{-3} and 2×10^{19} cm^{-3}, respectively, were fabricated by low-pressure thermal diffusion of $POCl_3$ using the Lydop technology. The PSG layer formed at the wafer surface during thermal diffusion was preserved for use as a doping source during the laser-assisted diffusion process on the 100 Ω/sq samples. The 80 Ω/sq were kept as homogeneous emitters for comparison. An 80 nm thick SiN_x layer was deposited over the PSG layer by conventional PECVD process for passivation and antireflection purposes. A frequency tripled Nd : YAG laser from ROFIN with a wavelength of 355 nm and a pulse duration of 10 ns was used for heat-assisted diffusion.

Simples test structures were fabricated to optimise the laser parameters. Test structures were characterised by optical microscopy, 4-point probe equipment, Transmission Line Method (TLM), and Quasi-Steady-State Photoconductance. Laboratory scale solar cells were characterised by illuminated I-V and spectral response measurements.

3.1. Sheet Resistance Measurements. Figure 4 shows the typical evolution of the sheet resistance with laser fluence and pulse overlap measured on samples with a 100 Ω/sq initial emitter. Complete ablation of SiN_x without debris was observed between 0.4 J$\cdot$cm^{-2} and 0.7 J$\cdot$cm^{-2}. As expected from the simulation, laser-assisted doping was more efficient at low fluence for samples with PSG only. A decrease of the sheet resistance was measured at low fluence (0.25 J$\cdot$cm^{-2}) in PSG-capped silicon while no laser doping was measured for fluence under 0.4 J$\cdot$cm^{-2} in PSG/SiN_x-capped silicon. Moreover, 0.2 J$\cdot$cm^{-2} and 50% overlap was sufficient to reach 65 Ω/sq for a PSG-capped silicon while around 0.45 J$\cdot$cm^{-2} and 50% overlap was necessary to reach the same doping level for a PSG/SiN_x-capped silicon. On the other hand, at high fluence the minimum sheet resistance was lower for PSG/SiN_x-capped silicon (20 Ω/sq) than for PSG-capped silicon (30 Ω/sq).

3.2. Passivation Properties. The influence of the PSG layer on the carrier lifetime was studied on different samples by transient decay photoconductance. FZ wafers with a thickness of 400 μm and a resistivity of 800 $\Omega\cdot$cm were used for thermal diffusion followed by a standard SiN_x deposition on both surfaces. The PSG layer was etched on one sample before SiN_x deposition. FZ samples with or without a PSG layer under the SiN_x coating showed similar lifetime around 200 μs for a 60 Ω/sq emitter. A similar procedure was applied to a lower quality multicrystalline silicon wafer with a thickness of 250 μm and a resistivity of 1 $\Omega\cdot$cm. Samples with PSG, PSG/ SiN_x, and SiN_x on both faces were fabricated. All showed a similar lifetime around 10 μs. These first observations on high and low quality silicon substrates are promising for practical use of PSG/ SiN_x as passivating bilayer.

3.3. Laboratory Scale Solar Cell Results. Selective emitter solar cells were made following a modified version of the Process B presented in Figure 1. Front side metallization was made by Ti/Pd/Ag evaporation preceded by a photolithography step. Homogeneous emitter solar cells were also fabricated following the same procedure without any laser step and with a selective chemical etching of SiN_x. Selective emitter cells were realised on substrate with an initial emitter of 100 Ω/sq and homogeneous emitter cells with an initial emitter of 80 Ω/sq. Laser parameters were chosen to reach a sheet resistance of 40 Ω/sq under the metal contacts of

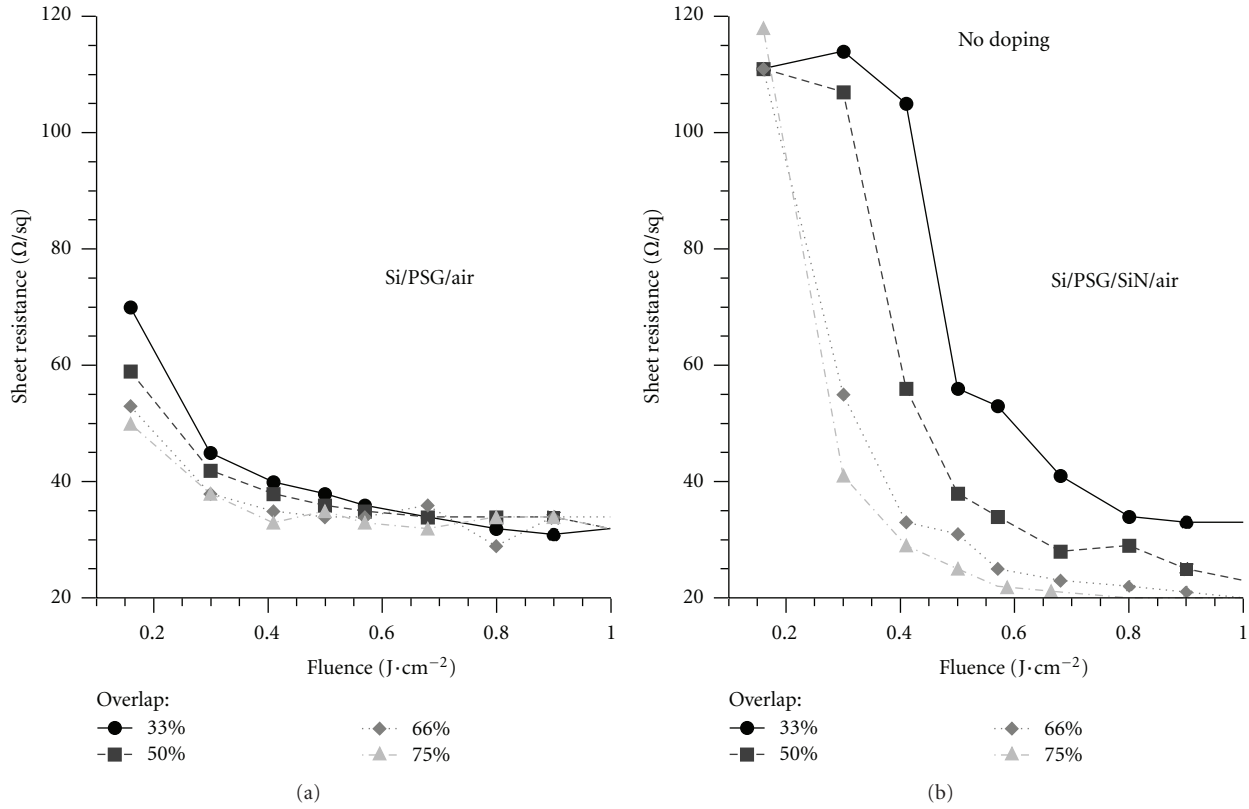

Figure 4: Sheet resistance evolution with laser fluence for 100 Ω/sq initial emitters.

Table 1: Averaged cell parameters from illuminated *I*-*V* results (HE stands for homogeneous emitter and SE selective emitter).

	Initial emitter	V_{oc} (mV)	Efficiency (%)	FF (%)	J_{sc} (mA/cm^2)
HE Average	80 Ω/sq	594	14.1	76.7	30.9
SE Average	100 Ω/sq	604	14.6	75.4	32.1

the selective emitter cells. Table 1 shows the average parameters extracted from the illuminated *I*-*V* measurements with and without laser step. Nine cells (4.1 cm^2) were measured for each process.

The selective emitter cells showed a 0.5% absolute increase in efficiency compared to the homogeneous emitter cells. The overall low efficiency of the solar cells was attributed to nonoptimized technological steps. Figure 5 shows an example of front contact metallisation misalignment that was observed in some of the cells. The laser-treated zone extends under the photoresist on the right hand side of the image. After metal deposition and chemical etching this area without passivation will be exposed to strong recombination. Lack of Ti/Pd/Ag metal sintering and nonoptimised antireflection properties of the PSG/SiN$_x$ stack might also be responsible of the global loss of efficiency. For all cells, shunt resistance appears as the main cause

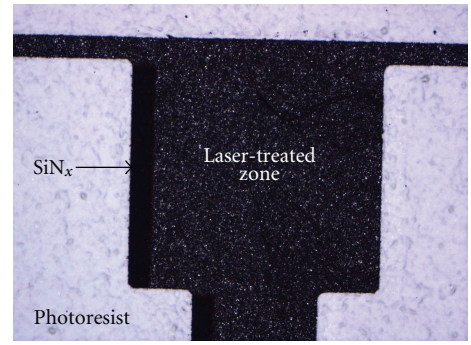

Figure 5: Image of the misalignment between the laser-treated zone and the metal contact area.

of parasitic resistive losses with an averaged value around 670 Ω·cm^2. Series resistance is reasonably low with an averaged value around 0.6 Ω·cm^2. The low values of V_{oc} are mainly attributed to recombination at the front surface.

Figure 6 shows the typical internal quantum efficiencies (IQEs) measured for homogeneous emitter (HE) and selective emitter (SE) cells. As expected, an increase of IQE is visible in the blue part of the spectrum for the selective emitter solar cells suggesting that the surface passivation is not degraded by the presence of the PSG layer at the surface.

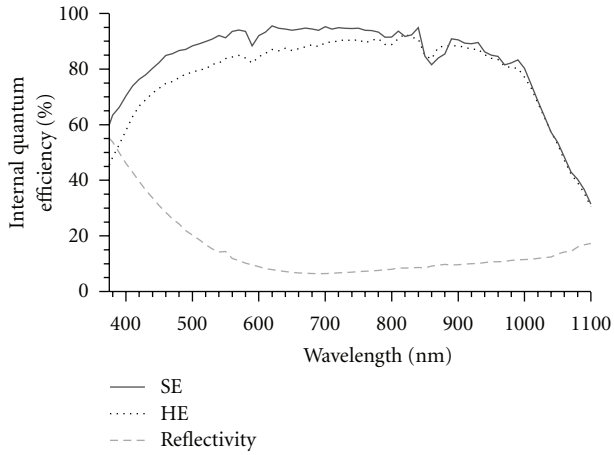

Figure 6: Internal quantum efficiency and reflectivity.

4. Conclusion

Selective emitter solar cells were fabricated with a reduced number of technological steps. Wet etching of the PSG was not necessary as this layer was preserved and covered by silicon nitride before laser-assisted diffusion. This process is potentially self-aligned if electrochemical front side metallisation is used. Preliminary results show reasonably good cell results with a 0.5% improvement compared with a homogeneous emitter structure. Several technological adjustments are foreseen on the antireflection and passivation properties of the PSG/SiN_x stack and on the front metal contact geometry to improve these first results. Long-term stability of the PSG layer has also to be investigated. Furthermore, numerical simulation of the laser-matter interaction is shown to be very useful to predict and understand the heat-assisted diffusion mechanism.

Acknowledgments

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Research Article

Surface Texturing with Hemispherical Cavities to Improve Efficiency in Silicon Solar Cells

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Improvement of solar-cell efficiency at a minimum possible cost addition is constantly sought, and this is often achieved at incremental percentage steps. Among a number of alternatives, antireflective coatings and surface texturing are the most prominent. This paper presents an alternative texturing method of crystalline silicon in an attempt to improve the efficiency of photon transmission through the surface and collection in the bulk. The method relies on anisotropic etching of bulk silicon and requires only a single oxide mask and two etching steps with a KOH or TMAH aqueous solution. The surface texture consists of smooth hemispherical cavities, which do not demand a lithographic mask or intricate technology processes to obtain the hemispherical cavities. This method can be applied to increase the profile area of the originally flat frontal surface exposed to light and consequently increase the effective width of the depletion region. The latter implies a higher probability of photon collection, contributing to the improvement of the conversion efficiency of the device. The textured nontilted silicon solar-cell transmittance under small solar incidence angles at dawn and sunset is improved compared to a flat surface, increasing the photocurrent.

1. Introduction

Very often texturing is employed to increase the solar-cell surface area [1, 2]. In some methods, based on inverted pyramids or laser-induced cone-shaped pillars, internal optical confinement of long-wavelength photons can be enhanced by light trapping [3, 4]. Other methods employ parasitic *hillocks* originating from sticking H_2 bubbles and precipitates, especially in low-concentration etching solutions [5]. More recently, nanostructures and wires have been proposed [6, 7].

The overall efficiency of a solar cell also depends on several aspects, among which, the composition of the semiconductor, temperature, contacts and metallization, antireflection coatings (ARC) type, doping concentration and topology of the cell layers, and encapsulation. As is widely known, silicon is predominantly used for the manufacture of photovoltaic cells because it is abundant in nature, processing technologies are mature and the energy bandgap is compatible with most of the solar spectrum. Nowadays, the world production of solar cells is largely concentrated in multi/micro/polycrystalline (m-Si, μ-Si, p-Si) and monocrystalline silicon (c-Si), with the latter featuring the highest efficiencies.

We present a method to texture the silicon surface to improve optical transmittance into the cell, especially at low sun-elevation angles. In this method a mesh of pyramidal pits in silicon gradually evolves into a mesh of hemispherical cavities by means of a single-step *anisotropic* etching with a KOH aqueous solution [8]. The method was initially proposed for the fabrication of micromirrors and arbitrarily shaped optical surfaces [8, 9]. The cross-disciplinary concept for texturing originated from our previous experience with the method for the latter applications.

Several improvements can be experimented with this texturing technique. Doping after texturing, either by diffusion

or by ion implantation, results in an emitter-base junction that mimics the surface profile, consequently enhancing the volume of the depletion layer and yields a higher probability of photogenerated carrier collection, especially by drift. Alternatively, the textured junction can also be achieved by depositing a doped emitter thin film on the textured substrate. Moreover, the spherical depressions can serve as high-refraction index concave lenses to enhance long-wavelength absorption. Also, the textured surface serves as perfect molding for polymeric or low-temperature glass microlens-array solar concentrators [9].

In this paper we focus primarily on this alternative texturing idea, and present a preliminary performance analysis based on the influence of the proposed texturing on the transmittance at the air-silicon interface, representing the portion of the solar radiation effectively penetrating the cell bulk.

It must be mentioned that, although desirable and important, there has been no attempt so far to compare the hemispherical texturing with any other texturing scheme currently practiced and proposed. Also, for each particular case, a detailed full-cycle cost evaluation needs to be done. This first unambitious analysis might, notwithstanding its primitiveness, incite alternative ideas, based on the proposed technology, either for commodity or custom photovoltaic cells, and propel more in-depth research in this direction.

2. Hemispherical Texturing Method

The method employed to etch the array of smooth hemispherical depressions on the silicon surface is curiously based on bulk micromachining with an *anisotropic* etchant. The process is predictable, as follows, for a ⟨100⟩ c-Si surface; m-Si, μ-Si, p-Si can also be deployed for such a texturing, where the extent of the added value being closely dependent on the density and size of ⟨100⟩-oriented grains on the exposed surface. This texturing technique only requires a single oxide film with a mesh of openings and two etching steps in a KOH : H_2O, or a TMAH : H_2O, solution. The use of a lithographic mask to create the opening mesh in SiO_2 is not strictly necessary. Instead, at least two lower cost options can be deployed: (1) high-quality laser-printed translucent sheets or (2) poor porous sacrificial thermal oxide produced under nitrogen purge. There, the resulting mesh changes from a highly ordered to a random array of openings, both grid- and size-wise.

The texturing method is based on a seldom known subtlety of Si bulk etching: a ⟨111⟩ pyramidal pit formed by a KOH anisotropic etch through an oxide mask eventually evolves into a smooth hemispherical cavity under subsequent maskless etching. An intermediate stage exists when a wider 19.47° ⟨411⟩-faced pyramid replaces the initial 54.74° inverted pyramid. The distance from base to vertex of the ⟨411⟩-faced pyramid determines the depth of the resulting spherical cavity. The complete replacement of the ⟨111⟩ walls by the ⟨411⟩ ones occurs for an anterior wafer thinning h_{off} of approximately 1/3 of the ⟨111⟩ initial pyramidal base dimension (i.e., $d_0/3$). The base dimension d_0 is dictated by the largest dimension of the original opening on the oxide film. It is important to note that the initial film is not limited to SiO_2 and can be actually any material that adheres well to Si, is sufficiently resistant to the etchant used, and that can be easily and inexpensively removed later, as several polymers are. Figure 1 shows the evolution of the etching process after oxide removal.

Figure 2 indicates some useful parameters. The diameter D of the hemispherical depression is determined by the size of the initial opening on the oxide mask d_o and by the etch depth h, whereas its depth s is determined by d_o and the etching conditions. The empirical expression for the cavity diameter is $D = 7.8\, d_o^{0.42}\, h^{0.58}$, and it is valid for etch depths in excess of $2.5\, d_o$ [9]; a perfectly round perimeter is obtained for $h > 11\, d_o$ [10]. The cavity depth, also referred to as sagitta, is $s = \alpha \cdot d_o$, where α is a process parameter that depends on the KOH concentration in the solution and on the temperature. At a thinning h_{off} the wider ⟨411⟩ pyramidal pit completely replaces the original ⟨111⟩-walled one. Additional thinning h^* is required to achieve a hemispherical shape.

The minimum initial opening is limited by the resolution of the exposure mask or by the minimum pore in the sacrificial oxide. Lithographic masks, laser-beam, ion-beam, or e-beam direct writing can define uniform sub-micrometric openings, whereas translucent sheets patterned by a printer define relatively uniform openings that are at least several microns large. Porous thermal SiO_2, on the contrary, results in a random distribution of variously sized and shaped openings.

This method could be additionally combined with the traditional upward random-pyramids method (hillocks) to yield a yet more elaborate surface texture, as depicted in Figure 3, benefiting from the advantages of both.

3. Light Transmittance

Solar radiation can be decomposed into three components striking a ground-level photovoltaic cell: direct, diffuse, and albedo [11]. For the time being, nontilted cells and only the first radiation component are considered in our analysis, which is limited to the comparison between a surface textured with hemispherical cavities and a flat surface. Albedo radiation is mostly taken into account in tilted panels. Diffuse radiation can be as high as 15% of the impinging radiation, but due to its spatially random nature, it has been assumed to have equal contributions to transmittance on both surfaces considered here.

With respect to shading, the critical elevation angle γ_c can be defined as that below which part of the impinging light is shaded by surface features. An orthogonal hemispherical cavity array is prone to increasing shading from a critical angle that depends on the process parameters, as in

$$\gamma_C = tg^{-1}\left(\frac{D}{2s}\right) \tag{1}$$

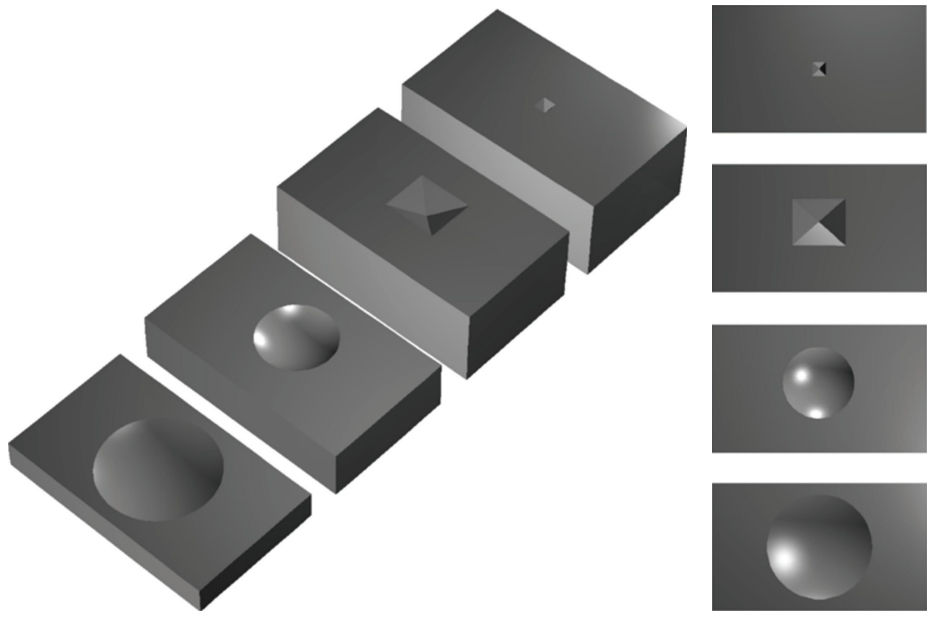


Figure 1: Evolution of an inverted pyramidal pit into a hemispherical depression. On the left one observes the concomitant thinning of the wafer. On the right one sees the cross-section and top view of the process.

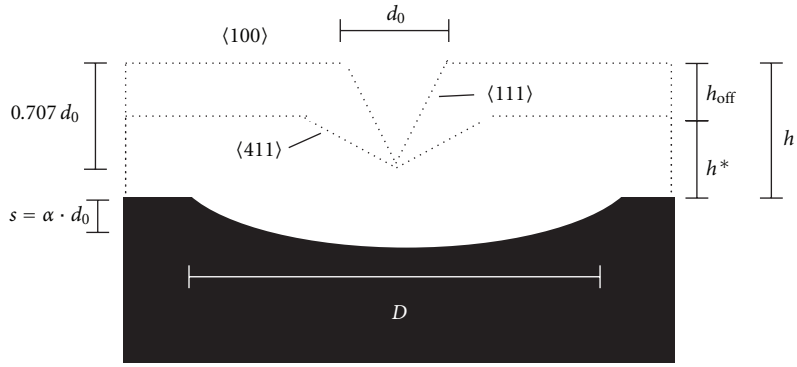


Figure 2: Parameters related to the etching process, from the initial pyramidal pit to the final hemispheric cavity.

or

$$\gamma_C = tg^{-1}\left[\frac{3.9}{\alpha}\left(\frac{h}{d_o}\right)^{0.58}\right]. \quad (2)$$

Figure 4 illustrates the relationship between γ_c and a single cavity.

The analysis that follows considers a 100% fill-factor orthogonal array with sharp edges and sharp peaks at the grid intersection vertices, as is the case with this texturing technology. It does not include a sun-tracking system either. A surface with pyramidal pits, for instance, yields a critical angle $\gamma_c = 54.74°$, whereas the hemispherical approach results in critical angles from 2° to 3°, when the ratio h/d_0 decreases from 5 to 2.5, as Figure 5 shows. Besides, in the hemispherical scheme, maximum shading is only significant when the sun trajectory is at 45° with the matrix orientation, for which each intersection peak casts a shadow towards the center of its respective cavity.

The surface area of a truncated spherical cavity area is given by (3),

$$S_{cav} = 2R\left[-2R \cdot \text{arc}tg\left[\frac{P_{max}^2}{4R\sqrt{-(P_{max}^2/2)+R^2}}\right] + 2P_{max} \cdot \text{arc}tg\left[\frac{P_{max}}{2\sqrt{-(P_{max}^2/2)+R^2}}\right]\right], \quad (3)$$

where $R = D^2/8s$, and P_{max} is the maximum pitch between two cavity centers that still guarantees 100% structural fill-factor. For an orthogonal array, this parameter assumes a value $P_{max} = D/\sqrt{2}$ and for a hexagonal array $P_{max} = 1.5\ (D/\sqrt{3})$. Parameters R and P_{max}, ruling the cavity area, are dependent on design and process parameters d_0 and h,

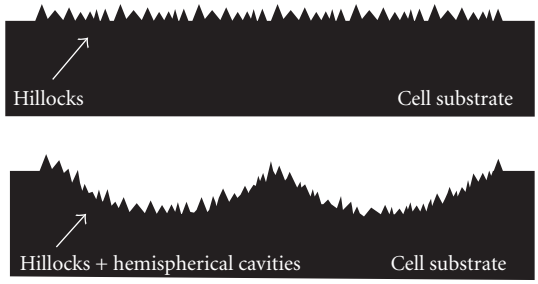


Figure 3: Schematic illustration of (top) front surface textured with the traditional random upward pyramids-hillocks; (bottom) front surface textured with a combination of hemispherical and random pyramids.

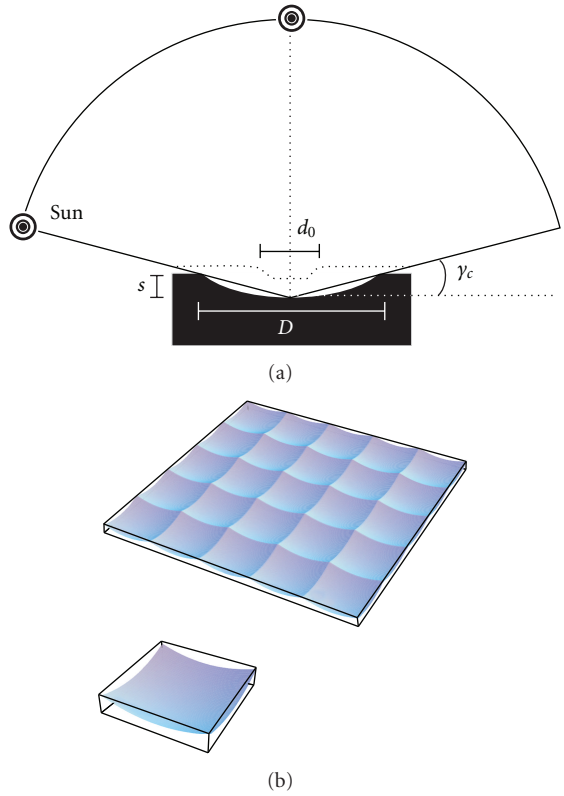


Figure 4: (a) Elevation angle and cell parameters for a single cavity, (b) orthogonal 100% fill factor array, and a single truncated spherical cavity.

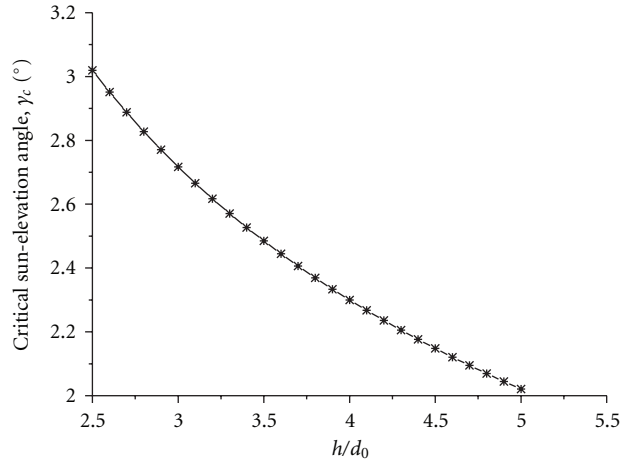


Figure 5: Critical sun-elevation angle γ_c versus process ratio h/d_0. The angle γ is measured from ground level and assumes 90° at the Zenith.

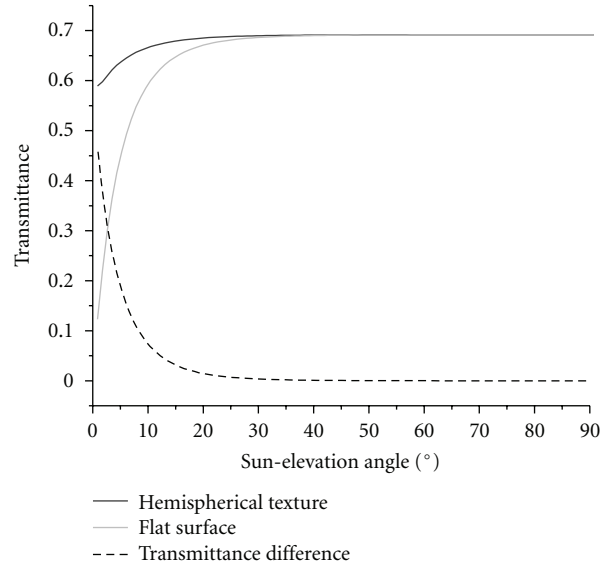


Figure 6: Transmittance as a function of sun-elevation angle γ for nontilted flat and hemispherically textured cells; dashed: difference in transmittance.

respectively. We have found that the area increases as the ratio h/d_0 decreases, resulting in an area gain of 0.35% with respect to a plane surface when $h/d_0 = 2.5$. The area gain is rather low; nevertheless, the effect of the hemispherical shape on the photon transmission should not be neglected.

We developed an algorithm to contrast the transmittance at the air-silicon interface of a flat cell to that of a hemispherically textured one. Sun rays sweep the cells from 0 to 90° and the algorithm outputs the total normalized transmittance over the cell area. There is no sun-tracking mechanism. Figure 6 shows the graphs for the two cases, where the textured surface has been obtained with the ratio $h/d_0 = 2.5$ and $d_0 = 40\,\mu$m.

These results show that the hemispherically textured cell exhibits considerable transmittance gain for elevation angles up to 30°. Using a textured cell, the transmittance can be larger than 30% higher for dawn and dusk hours. From geometrical optics, a factor contributing to this higher gain is the minimization of the highly oblique sun-ray angles with respect to surface loci, as more perpendicular incidence at each surface point yields a larger overall transmittance.

Additionally, we found out that the smaller the h/d_0 ratio and the larger the initial opening in the exposure mask d_0, the larger the transmittance. This leads to the conclusion that a large concave cell would perform the best, compared to a flat

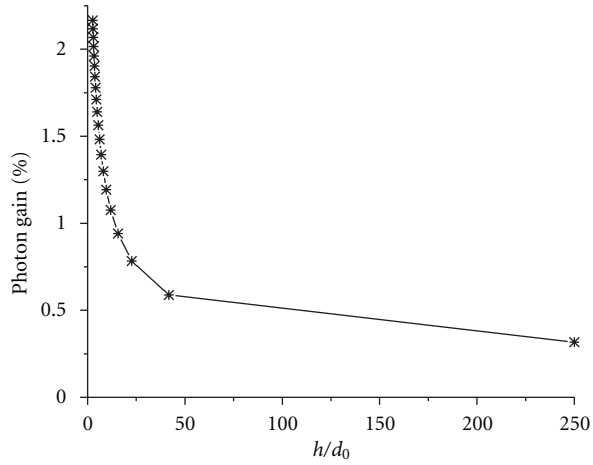


Figure 7: Gain in the number of absorbed photons for a hemispherically textured solar cell, as a function of the process ratio h/d_o, compared to a flat one in a nontilted condition, under the assumptions made in this section.

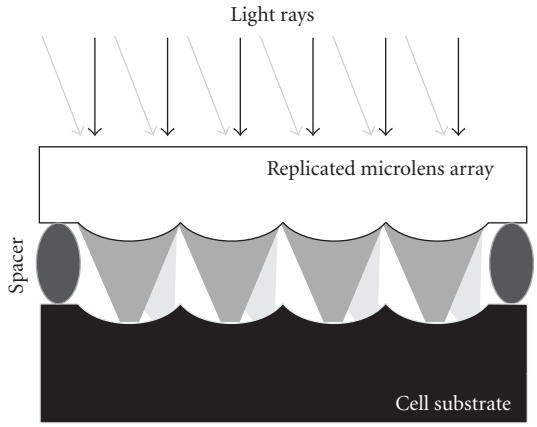


Figure 8: Microlens array replicated from the cell substrate itself. The microlens array is positioned at a distance from the substrate by means of spacers.

or a cavity-array surface. However, maximum d_0 is limited chiefly by the wafer thickness and the thinning $h = 2.5\,d_0$, which cares for the hemispherical shape. In practice this value ranges from 30 μm to 160 μm depending also on the back-end mechanical stability of the substrate. This range discards the need for high-resolution lithographic masks. For 100 cm^2 surface the cost of a custom Cr/Ni-Quartz mask could be reduced from US$300 to about US$5 for high-quality translucent sheets, and to no additional costs with the use of porous thermal oxide as a parasitic mask. Also, a single mask can be used for multiple lithographic exposures on larger surfaces.

To evaluate the benefits of a hemispherically textured cell compared to a flat cell, we calculated the total number of photons effectively penetrating each cell per day taking into account the previously calculated transmittance, and considering the average irradiance in Belo Horizonte, Minas Gerais (latitude 19°55′ S and longitude 43°56′ W). We made a couple of simplifying assumptions with no detriment to our comparative analysis: the general characteristics of both cells are exactly the same, except for the anterior surface texturing; albedo and diffuse radiation are null; cells are at sea level and not tilted; sun-tracking system is absent; average wavelength $\bar{\lambda} = 650$ nm is taken as the center of gravity of the solar spectral distribution (ASTM—G173-03) from 280 to 1100 nm (silicon cutoff wavelength); the sun is up 10 h per day.

Figure 7 shows the gain in number of photons as a function of h/d_0 for the conditions in the previous paragraph. We observe again that the lower h/d_0, the larger the gain. For $h/d_0 = 2.5$, the gain is higher than 2%. Considering that a flat silicon surface absorbs an energy density of ~900 kWh/m^2 over a year [11], due to direct incidence at a location prone to medium irradiation, then a hemispherically textured cell can offer additional 18 kWh/m^2 absorption. This value can range from 12 kWh/m^2 to as high as 25 kWh/m^2 for regions subjected to low and high irradiation levels, respectively.

The process parameter h/d_0 plays an important role in the design of an optimal hemispherical texture for the anterior surface of a solar cell. Although the critical shading angle increases as h/d_0 decreases, the area gain and transmittance gain are the largest for $h/d_0 = 2.5$. Also, the larger the mask opening size is, the largest the transmittance for low sun-elevation angles. This favors the employment of low-cost printing of exposure masks for the texturing patterning, as opposed to high-definition lithographic masks.

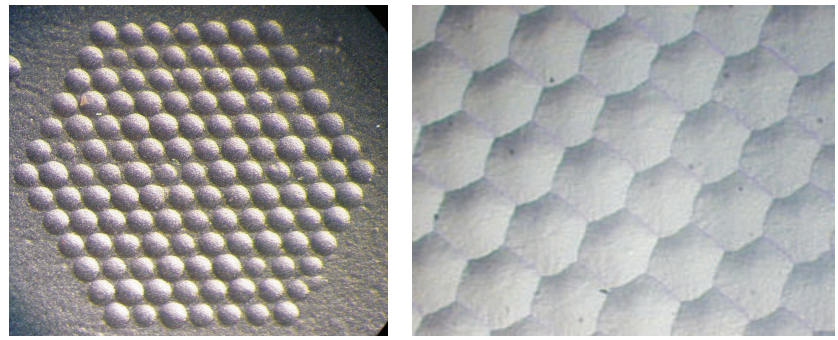
The concave nature of the texturing acts as a high-refraction index diverging lens. This favors a longer propagation path of light inside the semiconductor, therefore increasing the absorption and photogenerated-carrier collection efficiency.

Also, the array of concave depressions can directly serve as a mould for a transparent UV-curable polymer or low-temperature glass microlens array. The perfectly matched array of microlenses can be detached from the substrate and anchored at a small vertical distance from it by spacers. Sunlight through the convex lenses is refracted in such a way as to promote even less oblique incidence and concentrate light at the central region of each depression; also allowing space for a higher density of front-contact metallization, without compromising the effectively exposed area. The refractive microlens-array concentration is depicted in Figure 8.

4. Substrate Fabrication

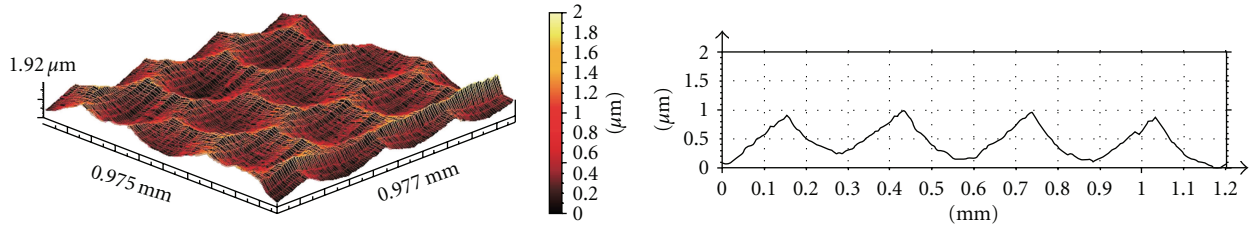
We fabricated two textured 10 mm × 10 mm substrate samples with hexagonal arrays of hemispherical cavities from starting circular openings with $d_0 = 3.4\,\mu$m diameter and a pitch $P = 300\,\mu$m. The substrate is a polished p-type (100) CZ monocrystalline silicon wafer. The oxide was a good-quality thermal wet oxide with 800 nm thickness.

The samples were etched in a 33 wt% KOH : H_2O solution at 85°C and with no magnetic or ultrasound agitation. SiO_2 was stripped with an HF solution. The absence of agitation and accurate temperature control are probably the reasons why there is some inhomogeneity in the cavity sizes



(a) (b)

Figure 9: (a) Photograph of the array etched until most cavities touched each other edges; (b) photograph of the array etched until overlap of cavities resulted in 100% fill factor.



(a) (b)

Figure 10: (a) 3D surface scanning; (b) linear scanning through the center of the sample.

and boundaries across the array, as the release of the etching by-products from the surface might not have been efficient. Results are shown in Figure 9.

Profilometry of the 100%-fill-factor sample with a Taylor-Hobson Series 2 contact profilometer yielded the results shown in Figure 10. The average cavity depth, sagitta, is 0.83 μm.

We fabricated a subsequent 10 mm $\times$ 10 mm sample with the same KOH solution concentration, but etched at 92°C $\pm$ 1°C with magnetic agitation of 590 rpm, and the sample suspended in the vertical position in 800 mL of the solution. Photolithography was realized with direct laser writer equipment (Microtech LW405). AFM analysis of this sample indicated a roughness of 4 nm on the (100) thinned surface and 1.8 nm around the center of the hemispherical cavity, prognosticating lower surface-recombination velocities.

5. Discussion and Conclusions

In this paper we showed that it is possible to etch a texture of (contiguous) hemispherical cavities in monocrystalline Si. Surprisingly, this can be achieved by *anisotropic* etching with smoothness as good as that from conventional chemomechanical polishing, so as to avoid deleteriously high surface recombination effects. The initial oxide openings preceding the texturing etch can be designed either with the high precision of lithographic masks and direct substrate writing, or with the medium precision of high-definition laser printers, or with the random distribution of porous thermal oxide. Also, this texturing technique could be combined with the traditional random-pyramid texture.

Given the shallow nature of the hemispherical cavities, calculations indicate a barely noticeable surface gain compared to a flat surface; however, the photon gain, mostly due to the minimization of oblique ray incidence, especially at dawn and dusk, is significant, resulting in an additional energy density from 12 kWh/m^2 to as high as 25 kWh/m^2 for regions subjected to low and high irradiation levels, under the assumptions specified in Section 3. The practical impact of these results, however, demands a comparison to both the performance and the processing cost of other textured surfaces already in use, which can be thoroughly tackled in a follow-up study.

Investigations need to be extended to include charge-carrier dynamics inside the semiconductor, but it can be already proposed that as the texture also acts as a concave lens, light will be refracted at angles further away from the vector normal to the surface, increasing the chances of absorption inside the material and closer to the emitter-base junction, but also enhancing the diffusion current-density component, influenced by both the diffusion length and the back-surface reflectance.

Another issue that deserves attention is the use of an anti-reflective coating. It is known that a 100 nm thick SiO_2 film enhances by 10–30% the transmittance over a broad range of the Si-sensitive spectrum [12]. The presence of an anti-reflective coating does not invalidate any of the previous

conclusions. On the contrary, it might even enhance these qualities, in addition to passivating surface states, and would benefit both planar and hemispherically textured surfaces.

Among the characteristics already discussed, the hemispherically textured substrate serves itself as a mould for the replication of polymeric or low-temperature glass microlens arrays, useful as local solar concentrators. Nevertheless, reflection and absorption by the microlens array also needs to be evaluated. If doping is performed after texturing, the space-charge region will present an increased volume, as compared to a flat emitter-base junction, and might render higher quantum efficiency, as already verified for photodiodes with wavy junctions [13].

Although the effective contribution of each single feature inherent to this technology can be arguable, the contribution of several features combined might prove useful.

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The authors are thankful to Dr. Oleg Soloviev (OKO Technologies, NL), to Dr. Jeffrey Ketterling (Riverside Research Institute, USA), to Professor Dr. José A. Diniz (Unicamp), to Ms. Márcia Reutemberg (Unicamp), and to Dr. José Roberto T. Branco (CETEC-MG) for the useful discussions, and to FAPEMIG (Fundação de Amparo à Pesquisa do Estado de Minas Gerais, Brazil), CAPES, and CNPq (Conselho Nacional de Desenvolvimento Científico e Tecnológico, Brazil) for the financial support.

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Research Article

Effect of the Phosphorus Gettering on Si Heterojunction Solar Cells

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To improve the efficiency of crystalline silicon solar cells, should be collected the excess carrier as much as possible. Therefore, minimizing the recombination both at the bulk and surface regions is important. Impurities make recombination sites and they are the major reason for recombination. Phosphorus (P) gettering was introduced to reduce metal impurities in the bulk region of Si wafers and then to improve the efficiency of Si heterojunction solar cells fabricated on the wafers. Resistivity of wafers was measured by a four-point probe method. Fill factor of solar cells was measured by a solar simulator. Saturation current and ideality factor were calculated from a dark current density-voltage graph. External quantum efficiency was analyzed to assess the effect of P gettering on the performance of solar cells. Minority bulk lifetime measured by microwave photoconductance decay increases from 368.3 to 660.8 μs. Open-circuit voltage and short-circuit current density increase from 577 to 598 mV and 27.8 to 29.8 mA/cm^2, respectively. The efficiency of solar cells increases from 11.9 to 13.4%. P gettering will be feasible to improve the efficiency of Si heterojunction solar cells fabricated on P-doped Si wafers.

1. Introduction

Solar cells have attracted great attention as a promising alternative energy source and various ways have been investigated to improve their performances. To obtain high-efficiency solar cells, minority carriers should have a long lifetime and a low recombination velocity [1]. Currently, single-, multicrystalline or amorphous silicon-based solar cells show high efficiency because of their reliability, scalability, and performance. However, metal impurities incorporated in Si wafers, such as Fe, Ni, and Cu, are highly mobile, diffuse over long distances, and act as a recombination center [2–4]. Furthermore, solar cell performance is largely limited by the regions of poorest material quality [4]. Such recombination center in the wafers deteriorates carrier collection efficiency. Therefore, impurity gettering has been widely studied to reduce their deleterious effect. Several methods have been investigated, including spontaneously occurring and intentionally formed sinks for the transition metals—at the surface and bulk. Depending on where we capture metal impurities, it is classified to intrinsic and extrinsic gettering. Intrinsic gettering is involving the metal impurity trapping sites mainly in the bulk region. External gettering is that generating stress silicon lattice which acts as a sink by external means such as abrasion grooving or phosphorus diffusion. Extrinsic impurity gettering in Si wafers is appropriate since solar cells employ the whole bulk region which is used as generation points. Furthermore, generated carriers move through the bulk region to electrodes, less recombination sites in bulk goes to better efficiency of solar

cells. Among extrinsic gettering, phosphorus (P) gettering is widely studied because it can be easily prepared by the diffusion of P [5–9].

Si heterojunction solar cells are one of important high efficiency solar cells showing a high open-circuit voltage and a low absorption in the emitter region.

Amorphous Si thin film has a large energy bandgap; Si heterojunction solar cells show a high open-circuit voltage and a low absorption in the emitter region. Since most light is absorbed in the bulk region of heterojunction silicon solar cells, it is important to have less recombination sites at the bulk region which reduce the diffusion length of excess carriers and collection efficiency.

In this work, we introduced extrinsic P gettering into the fabrication process of Si heterojunction solar cells and investigated the effect of P gettering on the performance of solar cells.

2. Experimental

Low-quality n-type monocrystalline Si wafers with the thickness of 170 μm were doped by P into (100) plane and showed the resistivity of 3–5 Ωcm. They underwent saw damage etching (SDE). Then, an aqueous hydrochloric acid and peroxide mixture (HPM) were used to remove metal particles from their surfaces. After finishing each process, the Si wafers were rinsed with DI water. We skipped texturing process to eliminate unwanted process variables.

P gettering has been reported to occur at an optimum temperature as it relies on the transportation of released impurities towards a segregation region near the surface of the samples [10]. Hence, the temperature and duration of P diffusion were expected to affect the gettering efficiency. Therefore, Si wafers were gettered at 750, 800, 850, and 900°C for 30 minutes in a quartz tube furnace, while a reference sample was not gettered. The resistivity of P-gettered Si wafer was measured at 9 points. Phosphosilicate glass (PSG) layers were removed in buffered oxide etch (BOE) solution. To remove the gettered layers where impurities were assumed to be gathered, samples were immersed in potassium hydroxide (KOH) solution for 5 minutes to etch back. The reference underwent the same etch-back process. Bulk lifetime was measured by iodine passivation using microwave photoconductance decay (μw-PCD).

Si heterojunction solar cells of 1×1 cm^2 were fabricated after finishing P gettering. 10 nm intrinsic a-Si:H films were deposited by hot wire chemical vapor deposition (HWCVD) using silane (SiH_4) and H_2 as precursor gases. 10 nm P-doped and 20 nm n-doped a-Si:H films were then formed by plasma enhanced CVD (PECVD) using SiH_4, H_2, and diborane (B_2H_6) or phosphine (PH_3). After deposition of intrinsic a-Si:H films, front and back electrodes were formed by evaporation. Finally, edge isolation process was carried out in a 4 : 1 (HCl : DI water) mixed solution. Processing sequence is described in Figure 1. Generally, it is hard to detect metal impurities concentration in crystalline silicon wafer because of the detection limit. Therefore, we analyzed wafer characteristics and cell characteristics to deduce the P gettering effect. The saturation current and ideality factor of Si heterojunction solar cells were calculated from their dark currents and voltages. Short-circuit current density, open circuit voltage, and fill factor of the solar cells were measured using a solar simulator. External quantum efficiency was analyzed between 400 to 1100 nm wavelength to assess the electron-hole separation and collection at the bulk region.

3. Results and Discussion

The resistivity of Si wafers is 3–5 Ωcm before P gettering. The sheet resistances of P-gettered samples as a function of gettering temperature are shown in Figure 2. Resistivity of gettered sample abruptly decreases at 800°C from 2.7 to 0.9 Ωcm. With the increasing gettering temperature, the resistivity decreases since the rate of P incorporation into substitutional sites of Si is enhanced by increased thermal activation at higher gettering temperature.

The minority carrier lifetime and diffusion length as a function of gettering temperature are shown in Figure 3. The bulk lifetime of the nongettered reference sample is 368.3 μs. Those of the gettered samples at 750, 800, 850, and 900°C are 615.4, 660.8, 343.0, and 301.4 μs, respectively. While the bulk lifetime shows the longest value at 800°C, which is 292.5 μs higher than that of the nongettered sample, the bulk lifetime shows the shortest value at 900°C, which is 56.0 μs shorter than that of the nongettered sample. Average diffusion length varies between 610.5 and 886.5 μm depending on gettering temperature. The diffusion lengths of the gettered samples at 750 and 850°C are 835.9 and 634.6 μm, respectively. While the diffusion length shows the longest value at 800°C, the diffusion length shows the shortest value at 900°C.

Figure 4 shows the mapping of bulk lifetime and its probability distribution for (a) nongettered sample and gettered smaples at (b) 750, (c) 800, (d) 850, and (e) 900°C. The nongettered sample shows that over 90% of the substrate has a bulk lifetime below 407.4 μs and its 10% has a bulk lifetime below 195.0 μs. Its 80% has bulk lifetime between 195.0 and 407.4 μs, while 90% of the substrate for the sample gettered at 800°C shows a bulk lifetime over 501.2 μs. The mapping of bulk lifetime and its probability distribution of the samples gettered at 750 and 800°C are similar, though the sample gettered at 750 shows widely distributed values as compared with those of 800°C.

The variation of lifetime and its probability distribution by gettering temperature can be explained by the diffusion-induced gettering of impurities as shown in Figure 5 [9]. When thermal activation energy is given in Si wafer, impurities are released from energetic binding and diffused through Si wafer. Then they are finally captured where the emitter acted as a sink. Here, experiment data shows that there is an optimized temperature of gettering. Metal impurities elimination efficiency of P gettering depends on the transport of impurities and solubility segregation. It was reported that there is competing effectiveness of two processes responsible for segregation gettering, that is, impurity transport and solubility segregation, the latter

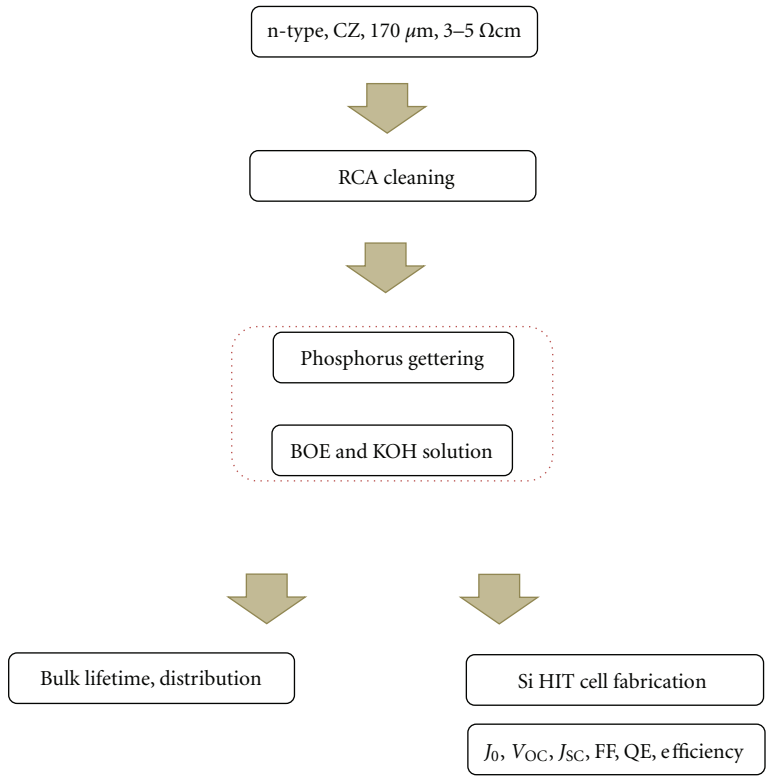


Figure 1: Processing sequence of samples for analysis.

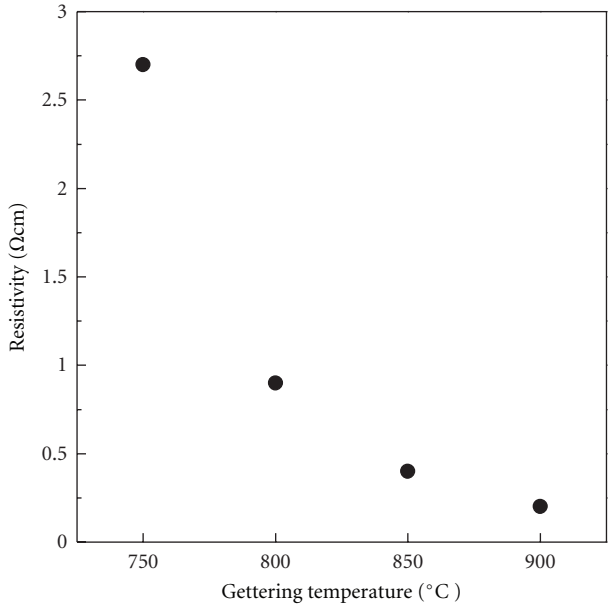


Figure 2: Resistivity as a function of gettering temperature.

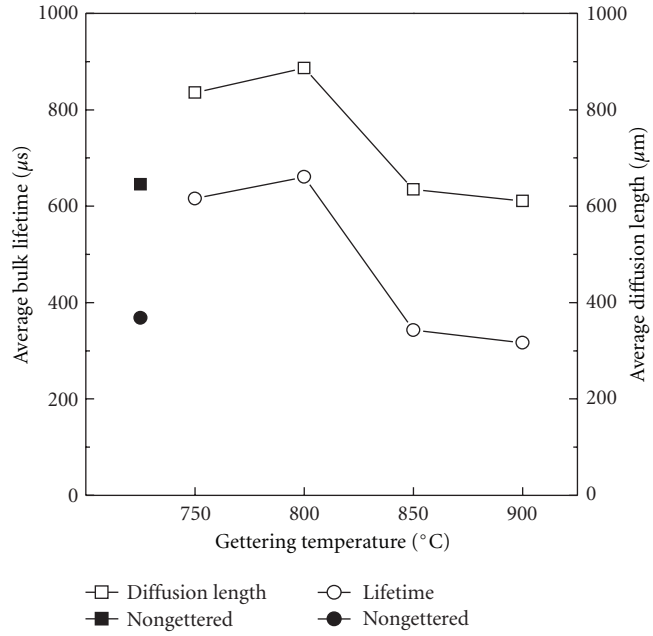
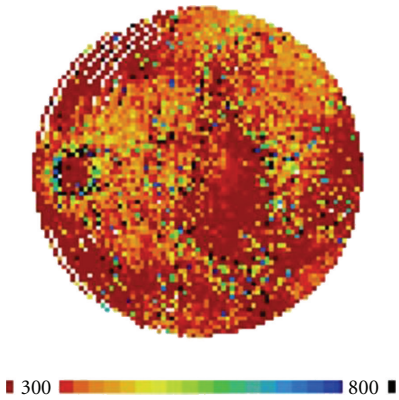
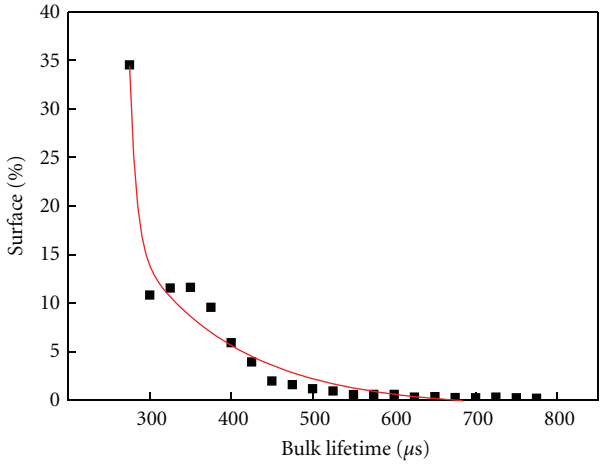


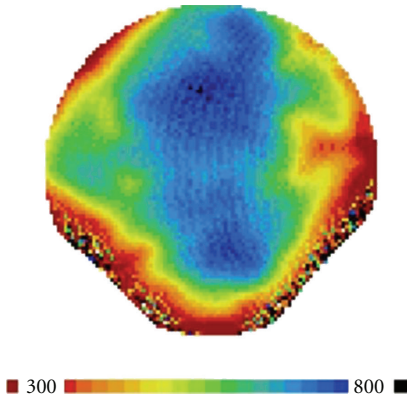
Figure 3: Bulk life time and bulk diffusion length as a function of gettering temperature.

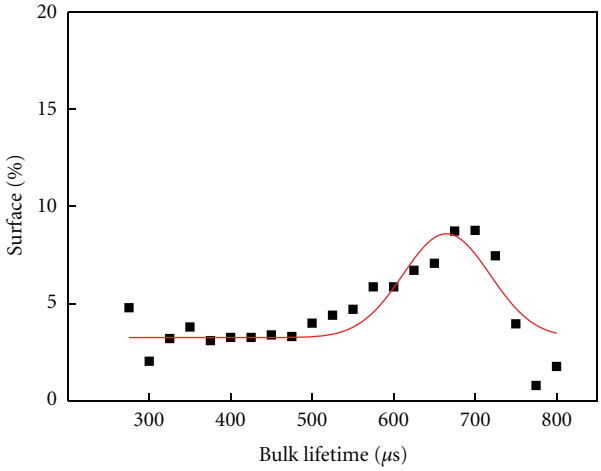
process being characterized by a decreasing segregation coefficient with increasing temperature [8, 11]. At high temperature, metal solubility is large, so required time for precipitation at the gettered region becomes long. However, if the gettering temperature is too high, crystallographic defects are formed [12]. Gettering temperature should be decided after considering the diffusion, precipitate, and segregation of metal impurities.



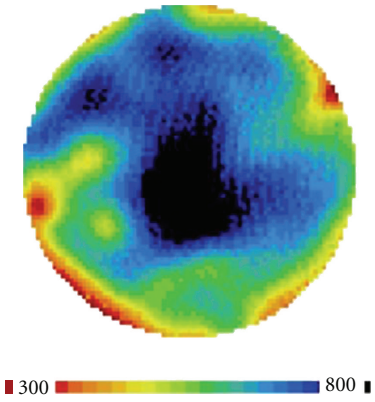


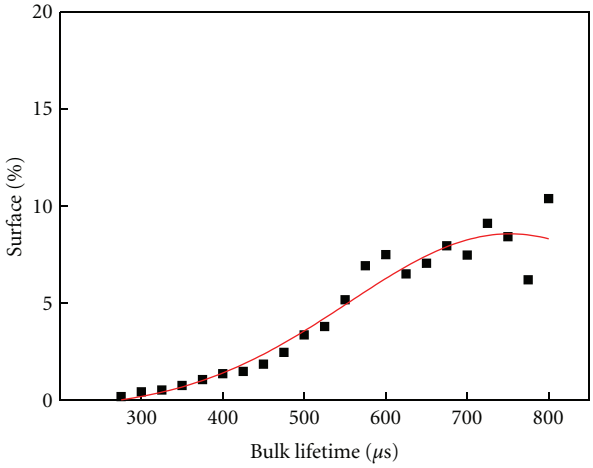
(a)





(b)





(c)

Figure 4: Continued.

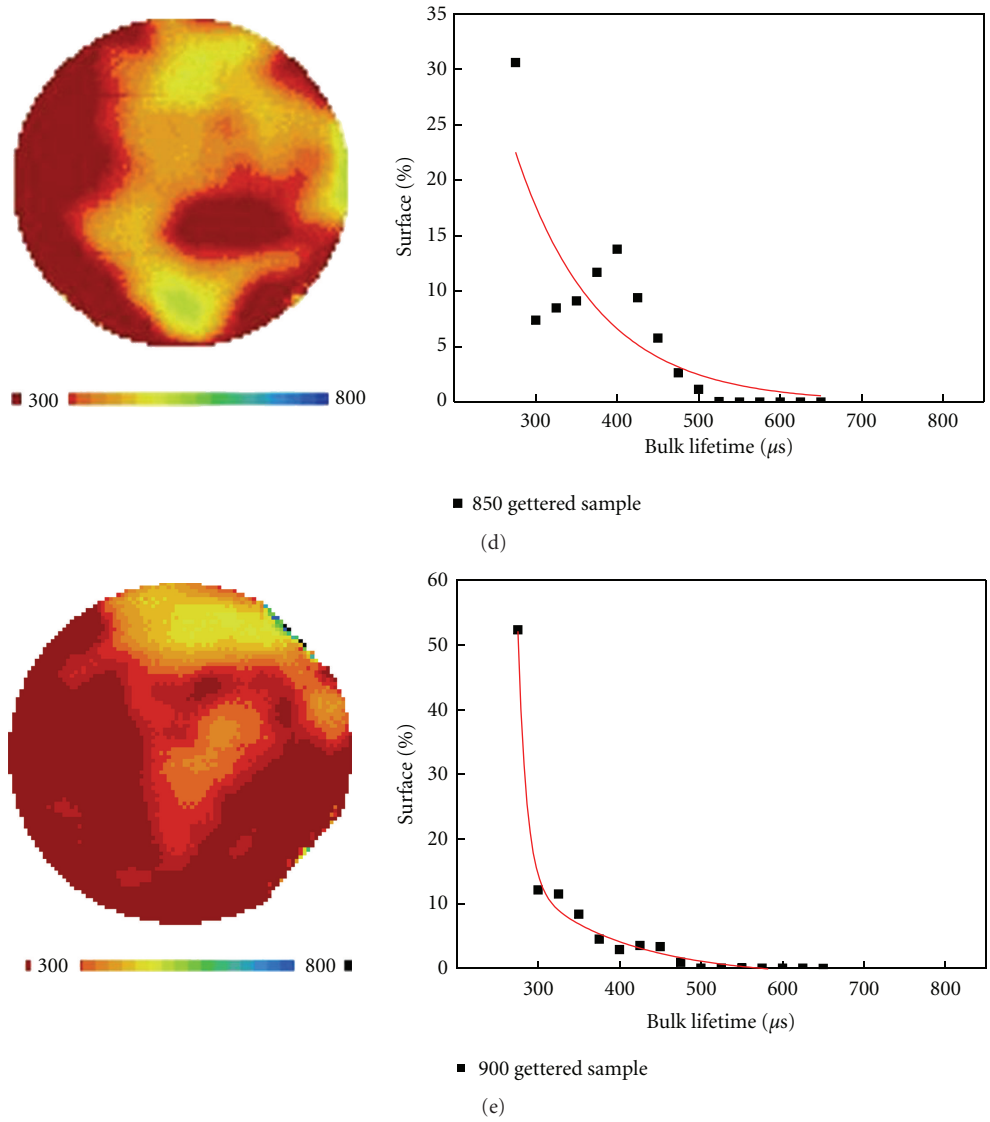


Figure 4: Mapping of bulk lifetime and its probability distribution for (a) nongettered sample and gettered samples at (b) 750, (c) 800, (d) 850, and (e) 900°C.

Figure 6 shows the illuminated current-voltage curves of nongettered and gettered samples. The sample gettered at 800°C shows the highest V_{oc} and J_{sc} values, 598 mV and 29.8 mA/cm^2, respectively. The samples gettered at 850 and 900°C do not show better properties than those of nongettered sample. For all the samples, V_{oc} values are between 581 and 598 mV, and J_{sc} values are between 27.1 and 29.8 mA/cm^2. Fill factor is calculated from the current-voltage curves. With the increasing gettering temperature, the fill factor slightly increases up to 800°C and then slightly increases up to 900°C. The sample gettered at 800°C shows the highest value of 75.3%.

P gettering was undertaken to suppress recombination due to impurities in the bulk region before the fabrication of Si heterojunction solar cells. As P gettering mainly affects the bulk or base region of the cells, we focus on variations in characteristics of quasineutral region than emitter region. From the dark current-voltage curves, ideality factor and saturation current can be calculated. J_0 is obtained by extrapolation to $V = 0$ [12]. Calculated saturation current and ideality factor as a function of gettering temperature are shown in Figure 7. The nongettered sample has a saturation current of 1.5×10^{-8} mA/cm^2 in its quasi-neutral region. With the increasing gettering temperature, the saturation current decreases up to 800°C and then increase up to 900°C. The sample gettered at 800°C shows the lowest value of 0.5×10^{-8} mA/cm^2. Ideality factors were calculated from the relationship [13]

$$n = \frac{q}{l_n mkT} = \frac{q}{2.3mkT}. \quad (1)$$

In the quasi-neutral region, the ideality factor of nongettered sample is 1.65. With the increasing gettering temperature, the ideality factor decreases up to 800°C and then increases up

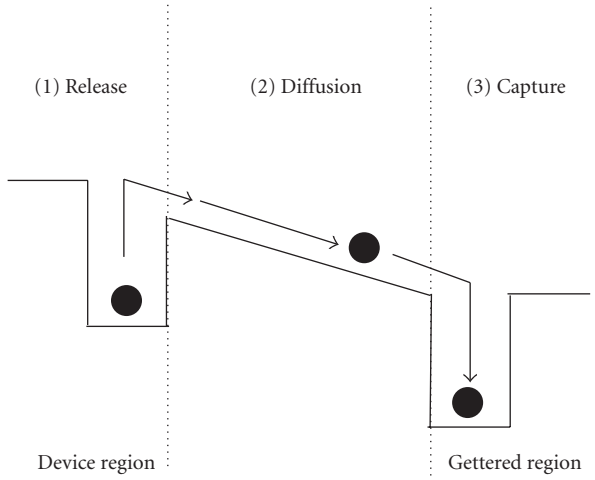


Figure 5: Sketch of the basic principle of diffusion-induced gettering of impurities.

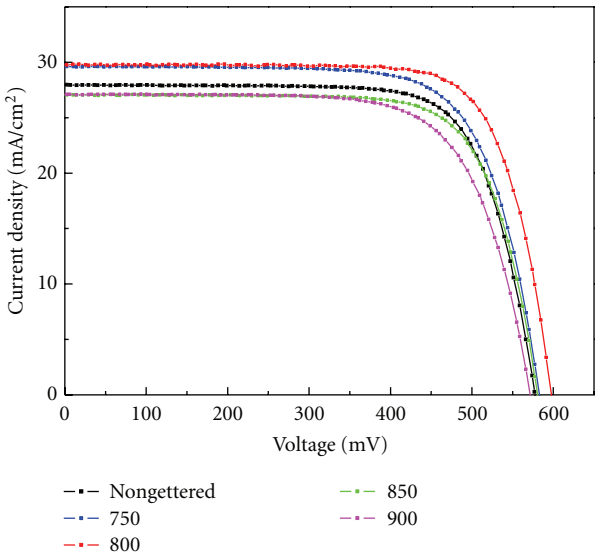


Figure 6: Illuminated current density-voltage curves of nongettered and gettered samples.

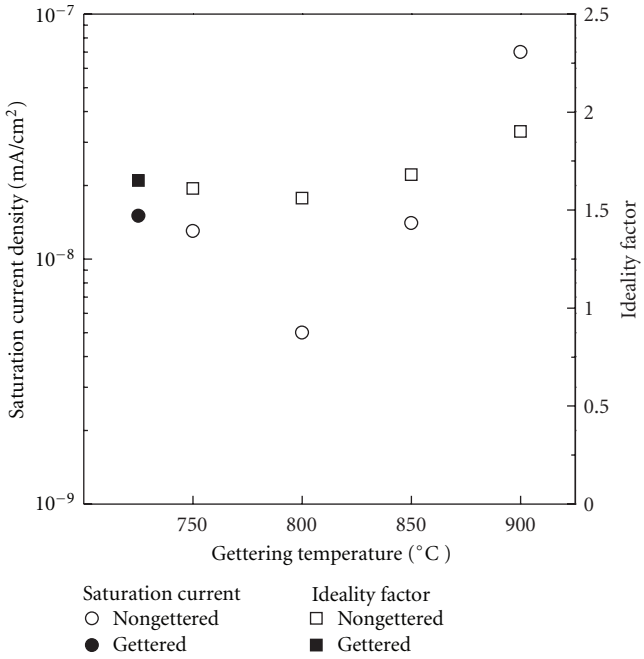


Figure 7: Calculated saturation current and ideality as a function of gettering temperature.

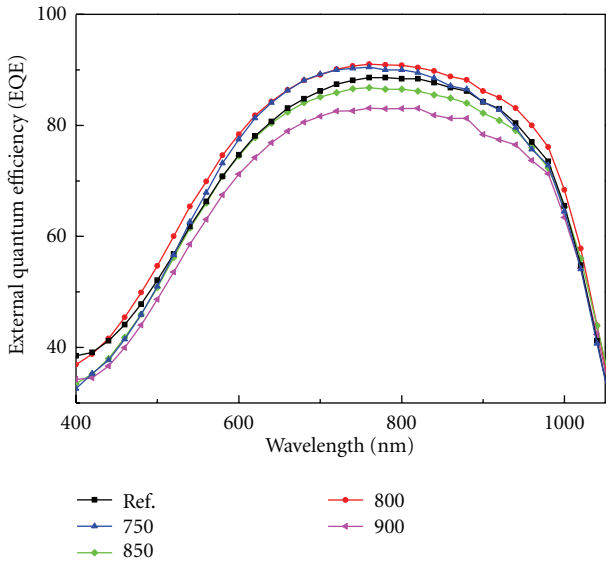


Figure 8: External quantum efficiency (EQE) of nongettered and gettered samples.

to 900°C; this is the same tendency with the dependence of saturation current on the gettering temperature. The sample gettered at 800°C shows the lowest value of 1.56.

External quantum efficiency (EQE) plots of the Si heterojunction solar cells are shown in Figure 8. We consider response to wavelength between 420 to 1100 nm corresponding to the signal from the bulk region. Responses of 750 and 800°C gettered samples show higher signal than that of the nongettered sample. The sample gettered at 800°C shows a superior response over all the wavelengths. However, samples gettered at 850°C and 900°C show a worse response than that of nongettered sample.

Ideality factors, J_0, V_{oc}, J_{sc}, fill factors, and efficiencies are summarized in Table 1. The dependences of these parameters on the gettering temperature as described above explain that the sample gettered at 800°C show the best value, and then the optimized P gettering temperature as a process parameter is to be chosen at 800°C.

4. Conclusions

Extrinsic phosphorus gettering was performed at 750, 800, 850, and 900°C to make high quality of silicon substrates for heterojunction solar cells. 800°C gettered sample shows the best characteristics. Their minority bulk lifetimes are

Table 1: Properties of Si heterojunction solar cells.

Gettering temperature (°C)	Ideality factor	$J_0(10^{-8}$ mA/cm2) Quasi-neutral region	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
Nongettered	1.65	1.4	577	27.8	73.9	11.9
750	1.61	1.3	583	29.6	72.2	12.5
800	1.56	0.5	598	29.8	75.3	13.4
850	1.68	1.4	581	27.1	73.7	11.6
900	1.90	7.4	572	27.1	70.3	10.9

improved from 368.3 to 660.8 μs. V_{OC} and J_{SC} increase from 577 to 598 mV and from 27.8 to **29.8** mA/cm^2. Saturation current and ideality factors decrease to 0.5×10^{-8} mA/cm^2 and 1.56, respectively. It results in efficiency improvement of silicon heterojunction solar cells. While properties of above 850°C gettered samples show degradation, we consider that optimized temperatures exist for extrinsic phosphorus gettering. Through this study, we found the possibility to improve the Si heterojunction solar cells by P gettering.

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Research Article

Low-Frequency Noise and Microplasma Analysis for c-Si Solar Cell Characterization

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This paper brings the comparison of solar cell conversion efficiency and results from a noise spectroscopy and microplasma presence to evaluate the solar cell technology. Three sets of monocrystalline silicon solar cells (c-Si) varying in front side phosphorus doped emitters were produced by standard screen-printing technique. From the measurements it follows that the noise spectral density related to defects is of $1/f$ type and its magnitude. It has been established that samples showing low noise feature high-conversion efficiency. The best results were reached for a group solar cells with selective emitter structure prepared by double-phosphorus diffusion process.

1. Introduction

It is generally accepted that there are some fundamental sources of noise which generate the noise background. This is the case of the thermal noise, shot, noise and, as was shown recently, of the fundamental quantum $1/f$ noise [1]. Besides the fundamental noise, which cannot be eliminated from any device, there exists *excess noise* which is believed to carry information on the device technology and structure defects which are either nonintentionally introduced during the device production or appear as results of the degradation processes during the device operation.

As it is well known, the noise spectral density increases with stress and damage and varies among nominally identical devices. Therefore, the excess noise is not of fundamental origin.

It is common experience that there are "good quality" and "poor quality" specimens. The noise level can vary considerably among nominally identical devices made by the same techniques and even at the same times. The sensitivity of the noise magnitude is typical feature of many samples and is caused by the effect of structure defects and other irregularities. Since the effect is due to a variable which is not controlled, the identification of the actual source is not easy. Very detailed experiments with many variables are needed to give a positive identification.

General conclusions are more common and state that noise depends on

(i) imperfections of the crystal structure, number of grain boundaries, point defects, linear defects, and so forth;

(ii) surface parameters;

(iii) homogeneity of PN junction region

Energy changes of the state of electron in a semiconductor are not indicated by light emission only but are also displayed on resulting current characteristics in both time and voltage dependence. They can be quantitatively evaluated not only by their mean values, but also by other statistical characteristics such as the correlation function or spectral output density. Considering the reality that the defects in silicon crystal grid are sources of oversize noise resulting in degradation of physical and technical parameters, noise characteristics can be used to evaluate

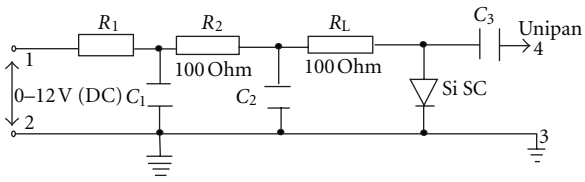

Figure 1: Circuit diagram of a solar cell sample.

the quality and service life of the observed system and its components classified.

As it was already shown in previous publications [1–3], noise spectral density reflects the quality of solar cells, and thus it represents an alternative advanced cell diagnostic tool. This paper deals with comparisons of noise spectroscopy [3] and detection of microplasma noise sources for three types of solar cells with screen-printed metallization varying in emitter structures.

2. Experimental Procedure

The first set of c-Si solar cells (here denoted as group 3149) was prepared with homogeneous emitter doped to the sheet resistance of about 52 Ohm/sq. The second group of samples (3147) represents advanced cell structure concept with selective emitter structure prepared by single phosphorus diffusion where shallow doped regions were formed by using isishape SolarEtch CES etching paste from Merck company. In the third group 3150 the solar cells with selective emitters (SE) were prepared by double "deep" phosphorus diffusion process where the shallow emitters were prepared from deep diffused n+ layer by wet chemical "nanoetching."

Produced solar cells were first characterized by standard techniques such as an illuminated *I-V* curve measurement (sun simulator 1000 W/m^2, AM1.5), LBIC (650 nm), EQE, and Suns-Voc in Solartec. Then all the samples were transported to the advanced characterizations (noise diagnostics and microplasma detection) to the Brno University of Technology.

Figure 1 shows the electronic circuit used to measure the noise characteristic of solar cells samples. A DC voltage from a DC power supply is applied across points 1 and 2. Resistances R_1 and R_2 and capacitors C_1 and C_2 are used to suppress spurious effects of the measuring equipment. The load resistance R_L has been chosen to be 100 Ω. The noise voltage to be analyzed passes through a coupling capacitor C_3 between points 3 and 4 to be fed into the input of Unipan 233-7 low-noise preamplifier, subsequently processed and recorded.

Since the noise voltage across the load resistance is measurable quantity, the testing procedure is based on the load resistance noise voltage data collection. The highest resolution of the current noise spectral density is obtained for the current values corresponding to the power matching condition. The ratio of the total measured noise to the background noise has a maximum value at this point.

The voltage noise spectral density was measured in forward biased voltage [4, 5] being picked up across a load resistance $R_L = 100\,\Omega$ at a band mean frequency of 1 kHz and a bandwidth of 20 Hz [6, 7].

When reverse electric field is applied to a PN junction with some technological imperfections like local shunts, dislocation in PN junction or crystal-grid defects causing nonhomogeneity of parameters it produces enhanced impact ionization in tiny areas called microplasma [8, 9]. It can lead onwards to deterioration in a cell quality or to destruction of PN junction. Energy changes of the state of electron in a semiconductor are not indicated by light emission only but are also displayed on resulting current characteristics in both time and voltage dependence. This is used by noise diagnostic methods based on the fact that owing to the microstructure of a substance material matter, and all processes taking place in the substance are stochastic and are manifested by fluctuations of macroscopically measurable quantities. They can be quantitatively evaluated not only by their mean values, but also by other statistical characteristics such as correlation function or spectral output density. It is going usually of generation-recombination noise in which dependence on frequency is of type $1/f^2$. Microplasma is detectable well before the reverse breakdown of the PN junction.

Microplasma light emission is exhibited in a full spectrum range thus a CCD camera in a dark cryogenic box can be used. The apparatus for the method contains highly sensitive low-noise CCD camera G2-3200 with CCD chip by Kodak KAF-3200ME. It can be cooled down to −20°C. Camera contains set of optical filters, special objectives, and equipment for contacting solar cells. Solar cell is connected to reverse bias DC power source. Signal form CCD camera is analyzed by PC computer. The contact area is placed on dish with LN2. The temperature of underside area is −21°C. Due to the cooling it is possible to observe the smallest defects in solar cells. The number of the visible defects in solar cell depends on connected reversed biased voltage (RBV). During increasing reverse biased voltage, it is possible to observe more shining points. Standard exposure time is about 20 s.

3. Experimental Results

Figure 2 illustrates the voltage noise spectral density versus applied DC voltage. The highest resolution of the noise spectral density is obtained for voltage values corresponding to the power-matching condition ($U_{F1} = 0.3$ V). In a region at a voltage above $U_{F2} = 0.55$ V, we can see an accrual of excess noise component whose source comes from the contact series resistance R_S. Progress of the noise voltage spectral density in this region characterizes the contact series resistance state.

Figure 3 shows a voltage noise spectral density S_U versus frequency at a temperature $T = 300$ K, the noise voltage being picked up from a load resistor $R_L = 100\,\Omega$ for the cells from the 3149 group. The curve labeled $U_F = 0$ V indicates the measuring setup background noise. The shapes of the noise curves for the applied DC forward voltage $U_F = 0.3$ V (various samples) show the excess noise component to be of the $1/f^1$ type or $1/f^2$ type which is typical of the generation-recombination (g-r) noise.

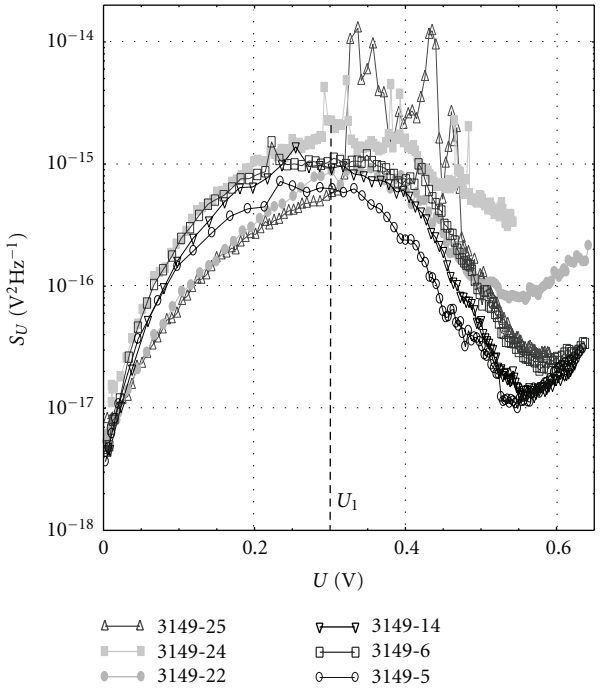

Figure 2: The noise spectral density as a function of forward voltage for group of samples 3149.

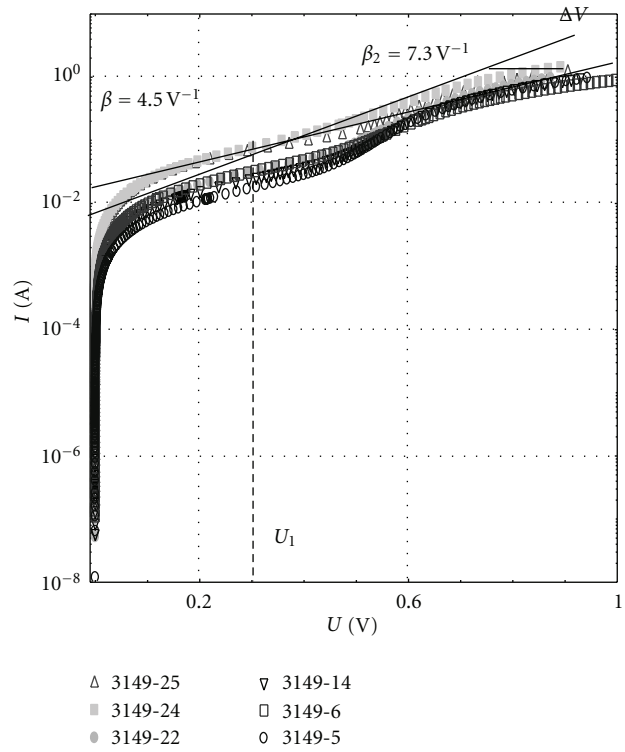

Figure 4: Dark I-V characteristics of the group of solar cells 3149 (homogeneous emitters).

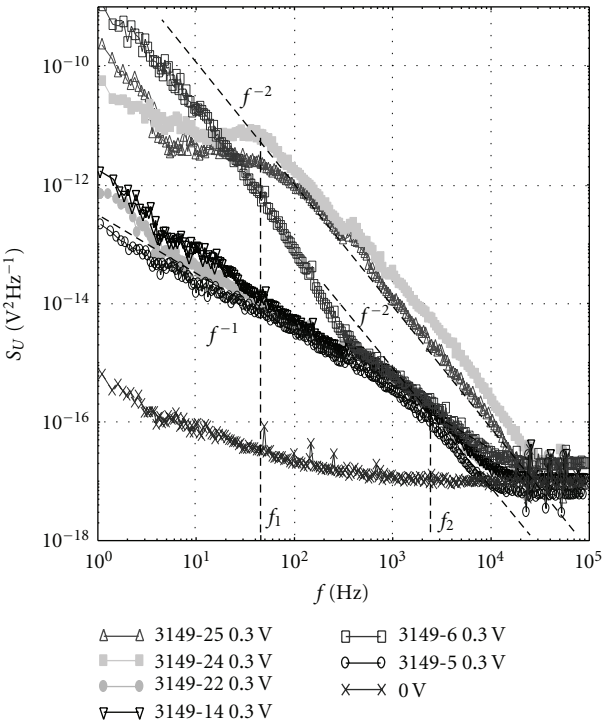

Figure 3: The noise spectral density versus frequency for group of samples 3149.

Excess noise parameters correlate very well with the transport characteristic measurement shown in Figure 4. In the area of $U_{F1} = 0.3$ V, we can for samples no. 24 and no. 25 observe significant component of excess current which is also reflected in the low value of exponent $\beta_1 = 4.5\,V^{-1}$. The value of capacity at a voltage $U_{F1} = 0.3$ V is about 620 nF (surface area 100 cm^2).

Figure 5 shows the dependence of noise spectral density on the applied DC voltage for the solar-cells from the 3150 group. Average value of S_{UMAX} is the lowest of all three studied groups and reached only $S_{UMAX} = 3 \cdot 10^{-16}\,V^2\,Hz^{-1}$.

In Figure 6 the correlation between spectral density S_{UMAX} and solar cell efficiency is shown. We can see high correlation factor in all three groups of samples.

4. Discussion

The generation of microplasma is influenced by several factors. The first of them is defected silicon crystal-grid causing nonhomogeneity of parameters that, in turn, creates visible defect. The second is dislocation and impurities in PN junction. At places where junction is thinner or mechanically damaged, the microplasma discharge and emission of light is present.

Another sign of observed microplasma is noise, which has random spectrum in frequency range. Microplasma noise is measurable even before the creation of light emissions. That provides a way to obtain information about microplasma creation with exiguous reverse voltage.

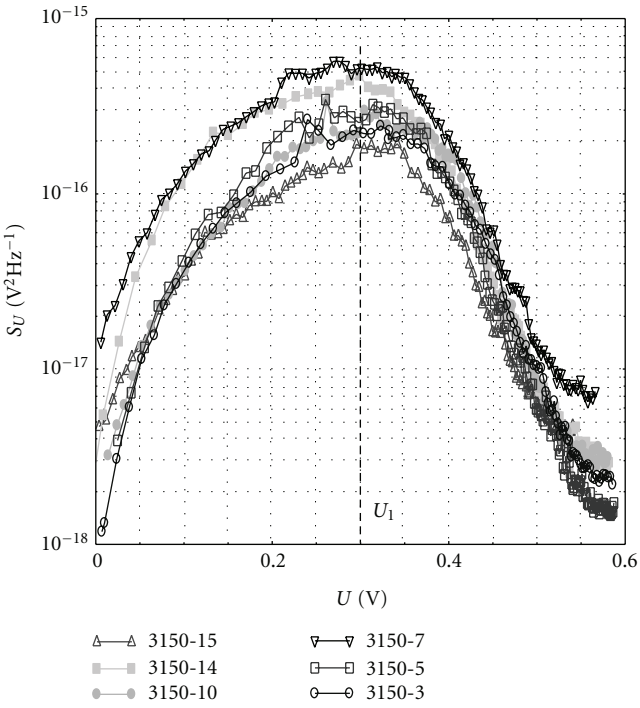

Figure 5: The noise spectral density as a function of forward voltage for group of samples 3150.

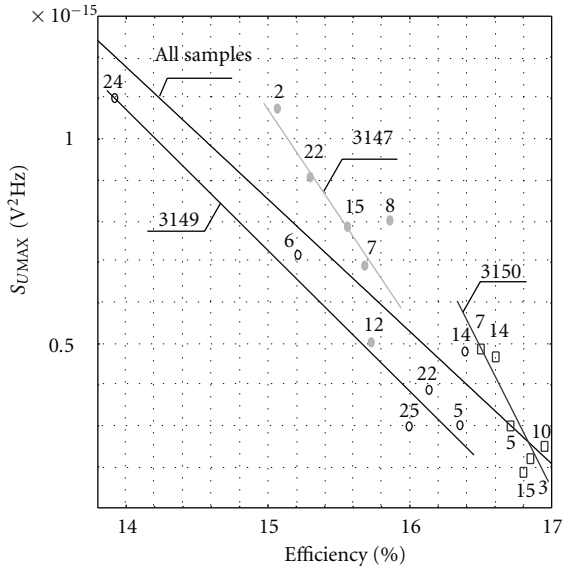

Figure 6: The correlation between spectral voltage density S_{UMAX} and conversion efficiency of the solar cells from all groups.

The microplasma light intensity highly depends on reversed biased voltage. The results from noise diagnostic (see examples nos. 3149-25, 3149-24, and 3149-6) show strong correlation between type of technology (used texture) and noise level. The output from observed microplasma of each cell shows that the correlation between these two methods can exist. For a sample 3150-15, we have observed at a voltage of 4.0 V presence of about 30 microplasma sources

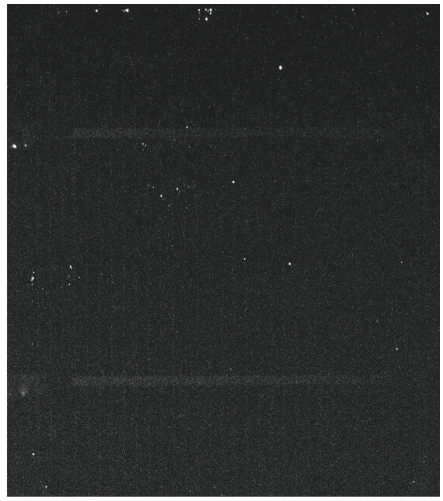

Figure 7: Microplasma method-scanning time 20 s, voltage 4.0 V, current 0.15 A, sample no. 3150-15.

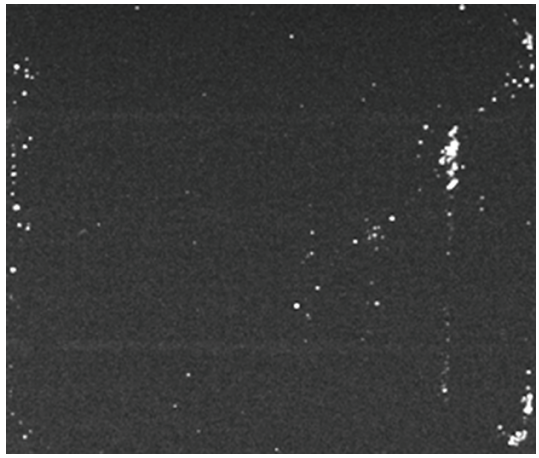

Figure 8: Microplasma method-scanning time 20 s, reverse voltage 4.0 V, current 0.15 A, sample no. 3149-25.

(Figure 6), while, at the sample 3149-25, the number was about 200, this is approximately 6 times higher (Figure 7).

Figure 7 shows results of a microplasma-emitted light for the sample no. 3150-15. This sample generated very small noise voltage spectral density of (for only $S_{UMAX} = 2 \cdot 10^{-16}\,V^2\,Hz$ $U_{F1} = 0.3\,V$), and its efficiency was quite high of about 16.8%.

The number of microplasma counts for sample No. 3149-25 is significantly greater and depends on connected reversed biased voltage (RBV) (Figures 8 and 9). The noise spectral density reaches value over $S_{UMAX} = 1 \cdot 10^{-14}\,V^2\,Hz$ for voltage 0.3 V.

5. Conclusion

The article compares the results from noise spectroscopy, microplasma presence, and solar-cell efficiency. From the measured results, it follows that the noise spectral density

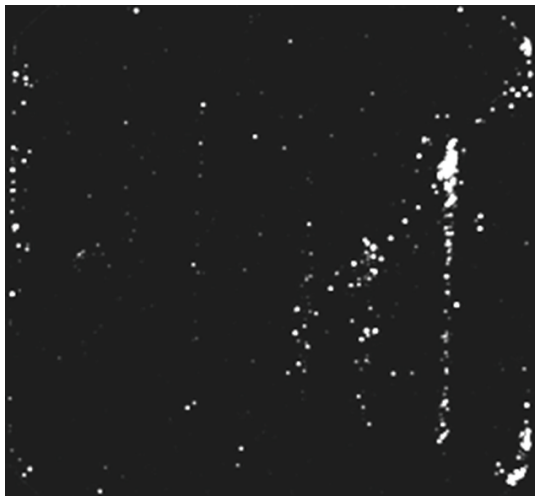

Figure 9: Microplasma method-scanning time 20 s, reverse voltage 8.0 V, sample no. 3149-25.

related to defects is of $1/f$ and generation-recombination types. Samples with lower noise voltage spectral density of only $S_{UMAX} = 2 \cdot 10^{-16}\,\mathrm{V^2\,Hz}$ for $U_{F1} = 0.3\,\mathrm{V}$ have smaller number of microplasma counts around 30 for voltage of 4.0 V and higher efficiency 16.5%–17.0%. Samples with great noise voltage spectral density over $S_{UMAX} = 6 \cdot 10^{-16}\,\mathrm{V^2\,Hz}$ for $U_{F1} = 0.3\,\mathrm{V}$ have the number of microplasma counts greater than 200 for voltage 4.0 V and smaller efficiency 14.0%–16.0%.

Data presented in Figure 6 shows not only good correlation of the spectral voltage density with conversion efficiency of all solar cells but one can identify small variation in the tangent of this relationship corresponding to the cells differing in emitter structure. This behavior will be subject of next intensive study.

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Research Article

The Compromise Condition for High Performance of the Single Silicon Heterojunction Solar Cells

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For optimum performance of the hydrogenated amorphous silicon/crystalline silicon (a-Si : H/c-Si) heterojunction solar cells, featuring a doping concentration, localized states, as well as thickness of emitter layer are crucial, since Fermi level, surface passivated quality, and light absorption have to be compromised themselves. For this purpose, the effect of both doping concentration and thickness of emitter layer was investigated. It was found that with gas phase doping concentration and emitter layer thickness of 3% and 7 nm, solar cell efficiency in excess of 14.6% can be achieved. For high gas phase doping concentration, the degradation of open-circuit voltage as well as cell efficiency was obtained due to the higher disorder in the emitter layer. The heavily doped along with thicker in thickness of emitter layer results in light absorption on short wavelength, then diminishing short-circuit current density.

1. Introduction

Heterojunction solar cells consisting of crystalline silicon (c-Si) and hydrogenated amorphous silicon (a-Si : H) offer a low cost and high efficiency energy conversion alternative to conventional crystalline silicon solar cells. Compared to conventional silicon solar cells with diffused n/p junction and back surface field layers (BSF), noteworthy cost reduction can be obtained due to a completely low temperature (~ 200°C) formation process for both the n/p junction and BSF layer using hydrogenated amorphous silicon technology. Presently, Sanyo's heterojunction with intrinsic thin layer (HIT) solar cells showed the world record efficiency of 23% for double-junction structure [1]. However, for the single-junction HIT solar cell fabricated on polished wafers has reported approximately 13 ~ 14% efficiency [2–6], in which the open-circuit voltage (V_{oc}) did not exceed 580 mV, and the fill factor 74% could be obtained. Beside Sanyo, most research groups have been working on single-junction HIT solar cell using p-type c-Si as a base substrate.

When using a-Si : H and c-Si for junction formation, there are different aspects to be taken into account. Firstly to obtain high open circuit voltage (V_{oc}) and thus efficiency, the Fermi level in the emitter layer should be as close as to the nearest band as possible, which means that doping concentration is as high as it could be. The high doping concentration, nevertheless, also results in the high defect density in the films and leads to enhanced surface recombination [4]. The preferred doping concentration of emitter for HIT solar cell performance is still a matter of discussion. Sanyo's group has held world record efficiency of 23%, despite of, the limitation outside of Sanyo because of improper deposition condition such as doping concentration and so on. E. Conrad et al. suggested an optimal doping concentration (B_2H_6/SiH_4) of around 2000–3000 ppm [7]. Using simulation, N. Hernández-Como et al. proposed that the efficiency increases with increasing emitter doping concentration. Above a concentration of 3×10^{19} (cm^{-3}), the solar cell efficiency reaches its saturation value [8].

Also the emitter thickness variation could determine the short-circuit current as well as built-in potential in case of very thin layer of a-Si : H(p). On raising the emitter thickness, a-Si : H(p) layer incorporated into solar cells acts as a "dead

layer" and no electrons generated within the emitter layer are extracted due to intense carrier recombination within the defect emitter layer [9]. Reports on the optimum conditions varied in the literature and they can be classified roughly into two groups. Most research groups argue that 4 ~ 5 nm is thick enough for good device performances [1, 9]. While, emitter thickness of around 15 nm is mentioned to be thin enough by another [10]. In this paper, the compromise conditions for doping concentration, as well as the thickness of emitter layer, were investigated to set up a baseline for single p/n heterojunction solar cells.

2. Experiment

The commercial Czochralski-grown (CZ) c-Si(n) substrate with <100> orientation, resistivity of 1–10 Ω·cm, and 525 μm thickness has been used to fabricate the HIT solar cells. The crystalline Si substrates were treated by a sequence consisting of (1) acetone/methanol/DIW cleaning, (2) RCA cleaning. Native oxide was removed by a 1 min. dip in 1% hydrofluoric acid right before a-Si : H deposition. To change the doping concentration of the a-Si : H emitter, the gas phase doping concentration, B_2H_6/SiH_4, was varied in range of 2 to 10%, while the thickness of the a-Si : H emitter was fixed at 7 ± 0.05 nm. For the emitter thickness variation set, the gas phase doping concentration was 3%, the optimization condition in previous set, while emitter thickness varied in range of 3–15 nm. For the transparent conductive oxide (TCO), Indium Tin Oxide (ITO) thin film was deposited by rf magnetron sputtering at a substrate temperature of 200°C with thickness of about 80 ± 5 nm, followed by the deposition of silver/aluminum finger as the emitter contacts. Aluminum was evaporated on backside to create a good ohmic contact prior to area defining with mesa etching.

As confirmed previously [11], the a-Si : H(p) layer thickness controlled by spectroscopy ellipsometry (SE) shows excellent agreement with one evaluated from transmission electron microscopy (TEM). Hence, ellipsometry spectra (ψ, Δ) were collected using a rotating-compensator instrument (J. A. Woollam, HR-190) in this study. For the analysis, we used an optical model consisting of ambient/surface roughness layer (a-Si : H(p))/bulk layer (a-Si : H(p))/SiO_2/substrate (*n*-type c-Si), as shown in Figure 1. The dielectric function of the surface roughness layer was modeled as a 50/50 vol.% mix bulk layer material and voids [12]. The dielectric function of the a-Si : H(p) layer was modeled by the Tauc-Larentz (TL) model [12], which is expressed by

$$\varepsilon_{\mathrm{imTL}}(E)\frac{A\cdot E_0\cdot C\cdot\left(E-E_g\right)^2}{\left(E^2-E_g\right)^2+C^2\cdot E^2}\cdot\frac{1}{E}\qquad E>E_g,$$
$$\varepsilon_{\mathrm{imTL}}(E)=0\qquad E\le E_g, \tag{1}$$

where E_0 is the peak transition energy, E_g is the energy gap, and C is a broadening parameter, which can be related to the degree of disorder in the material. A is proportional to the height of imaginary part of the dielectric function. The parameters of the dielectric function, the thickness of the films, and their roughness are obtained by analysis of the spectra using TL model. The values of the various parameters are reported in Table 1. To determine hetero-interface quality, the minority carrier lifetime (τ_{eff}) was measured by the quasi-steady-state photoconductance (QSSPC) method, using a commercial WCT-120 photoconductance setup from Sinton Consulting. The electrical characteristics and activation energy were studied using the coplanar method with a programmable Keithley 617 electrometer using the samples grown on the glasses. The optical transmittance was measured in the wavelength range of 300–1200 nm using UV-Vis spectrophotometer. The external quantum efficiency (EQE) measurements of heterojunction solar cells were performed by using xenon lamp, a monochromator, and optical filters to filter out the high orders with a light probe beam impinging normal on the sample. The solar cells were characterized by current-voltage measurement under AM1.5 conditions at 25°C.

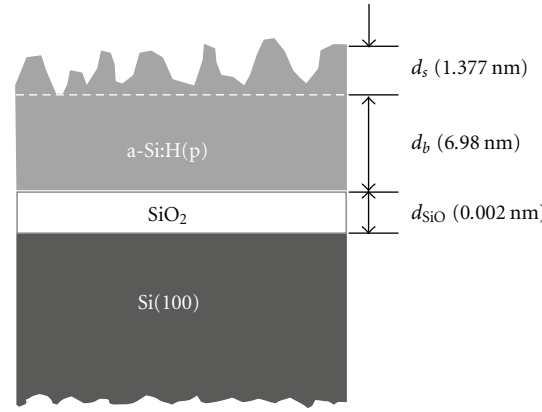

Figure 1: Optical model used for a-Si : H(p) layer formed on Si(100) substrates. The thickness for surface roughness layer, a-Si : H(p) layer, and SiO_2 layer is denoted as d_s, d_b, and d_{SiO}, respectively. The back-surface of the Si(100) substrate was roughened to eliminate back-side light reflection.

3. Results and Discussion

From Figure 2, it is observed that the E_a decreases rapidly when X_g (X_g = $[B_2H_6]/[SiH_4]$) is increased from 2% to 3% and then it seems to saturate with further increase. As evidence from Figure 2(a), the minimum E_a is obtained for X_g = 10% and thus the best device performance should be obtained using this gas phase doping concentration. However, contrary to our expectations, the highest performance of device is observed for X_g = 3%. The efficiency decreases for both higher and lower gas phase doping concentration. A similar variation is also observed for short-circuit current density (J_{sc}). The V_{oc} increases to a value of around 590 mV with the increasing in X_g of 3% and then seems to linearly shrink for further increase of X_g increases.

Figure 3 summarizes the degree of disorder (C) in a-Si:H(p) and minority carrier lifetime (τ_{eff}) of a-Si:H(p)

Table 1: Best-fit parameters extracted from the dielectric function modeling using the Tauc-Lorentz model. The results were obtained from the a-Si : H(p) thin films deposited at different gas phase doping concentrations.

X_g	d_s (nm)	d_b (nm)	d_{SiO} (nm)	A	E_0 (eV)	C	E_g (eV)
2%	1.978	7.082	0.052	80.88	3.97	1.69	1.62
3%	1.377	6.980	0.002	83.67	3.91	1.75	1.62
5%	0.909	7.071	0.154	93.96	3.84	1.82	1.59
10%	1.880	6.992	0.032	95.75	3.83	1.97	1.60

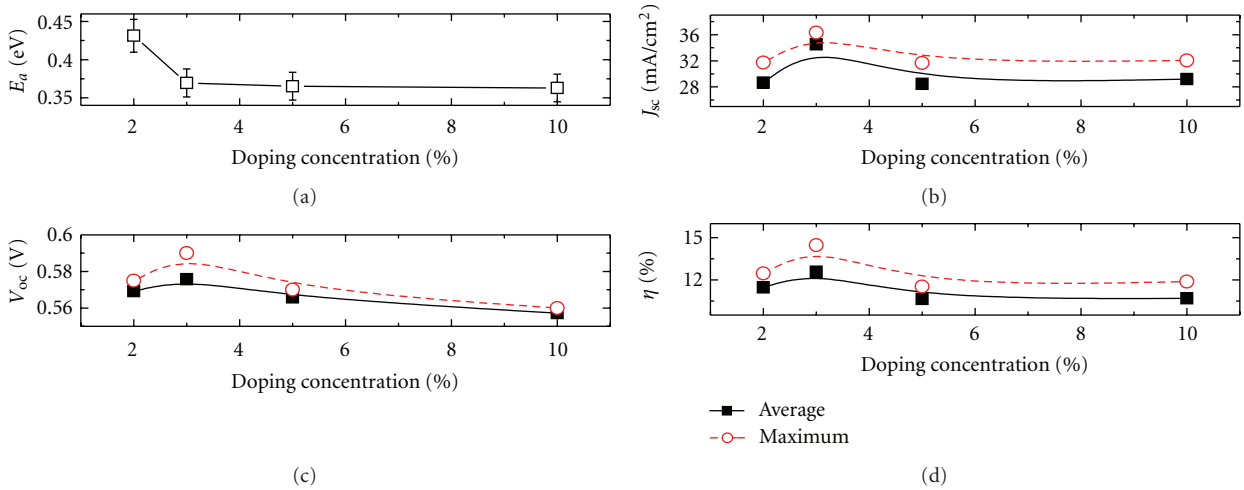

Figure 2: The activation energy, E_a, of a-Si : H(p) deposited on glass (a) and performance of Al/Ag/ITO/a-Si : H(p)/c-Si(n)/Al solar cells (b–d) with varying gas phase doping concentration of the a-Si : H(p).

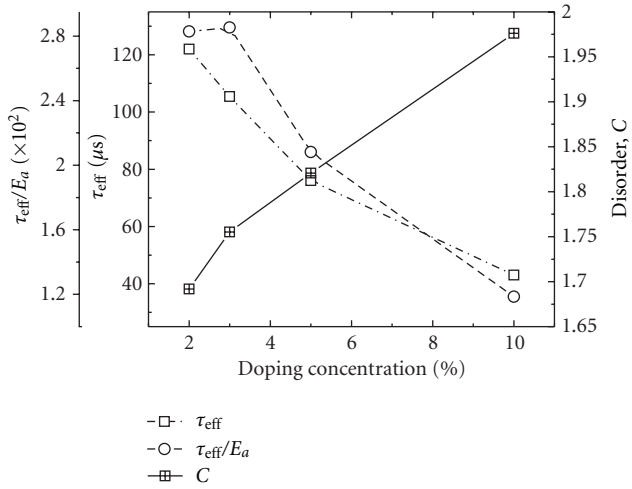

Figure 3: Minority carrier lifetime, τ_{eff}, measured on a-Si : H(p)/c-Si : H(n) structures, the degree of disorder in the a-Si : H(p), C, and trade-off factor, $Opt = \tau_{eff}/E_a$, as a function of the gas phase doping concentration.

deposited on c-Si(n) as a function of gas phase doping concentration of emitter layer. It is note that the C value is obtained from a well fit of the dielectric function of a-Si:H(p) using Tauc-Lorentz model, as discussing in the experimental part. It is clear that the trend of τ_{eff} and C displays a contrary direction and hence this also could be the reason for the reducing of V_{oc} when X_g is increased. As reported by R. A. Street, substitutional doping of a-Si : H(p) leads to the creation of deep defects [13]. This leads to a self-compensation effect in a-Si:H(p). Hence, the disorder in the a-Si : H(p) leads to a higher amount of interface states and thus a decreased minority carrier lifetime of a-Si : H(p)/c-Si(n) heterojunction. By increasing gas phase doping concentration, eventually, on the one hand the band bending increases with increasing gas phase doping concentration, on the other hand the disorder in the a-Si : H layer and interface states (decrease in τ_{eff}) increases. Therefore, we suggest a new factor ($Opt = \tau_{eff}/ E_a$) that may

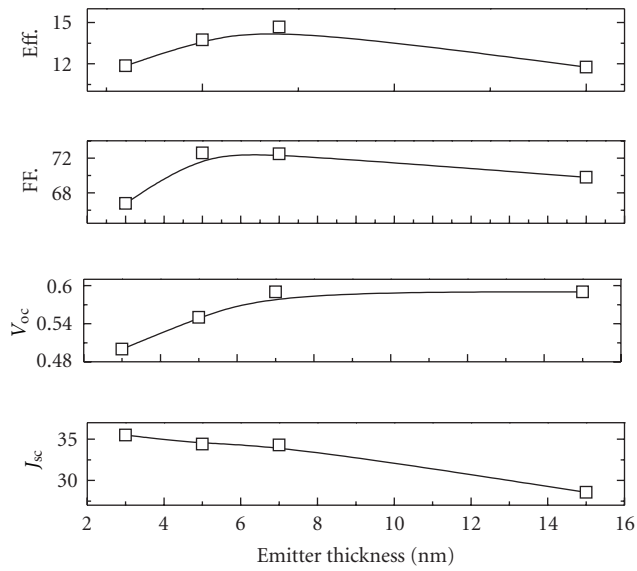

Figure 4: Solar cell parameters, short-circuit current density, open-circuit voltage, fill factor, and efficiency, as a function of a-Si : H(p) thickness for a-Si : H(p)/c-Si(n) heterojunction solar cells.

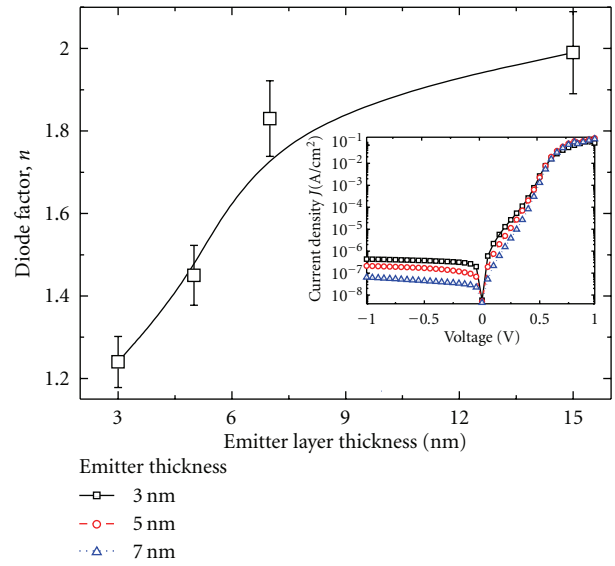

Figure 5: The diode factor n versus emitter layer thickness obtained from dark-current density versus voltage (DIV) with a-Si : H(p)/c-Si(n) solar cells shown in Figure 4. The inset shows DIV for a-Si : H(p)/c-Si(n) solar cells having different emitter layer thickness.

be presented as a trade-off between interface states and the position of the Fermi energy as showed in Figure 3. The highest *Opt* value is achieved at gas doping concentration of 3% and it is also point of merit for achieving highest device performance.

The parameters of an a-Si : H(p)/c-Si(n) solar cell, plotted as a function of the a-Si : H(p) emitter-layer thickness are shown in Figure 4. With increasing emitter-layer thickness up to 7 nm, V_{oc} increases linearly and then saturates beyond this layer thickness. It should be mentioned that for thickness smaller than 7 nm the open circuit voltage drops down to values around 500 mV. According to the usual junction rectification models for HIT solar cell at high forward bias voltage region ($0.4 < V < 0.6$ V), a relation between J and V is presented simply by [9]

$$J = J_0\left[\exp\left(\frac{qV}{nKT}\right) - 1\right] - J_{\text{ph}}, \tag{2}$$

where J_0 and J_{ph} are the saturation current density and photocurrent density, respectively. q, n, k, and T denote electron charge, diode factor, Boltzmann's constant, and temperature, respectively. Since $exp\,[qV/kT] \gg 1$ at $V \sim 0.5$ V and $T = 300$ K, J_0 and n can be determined directly from the intercept and slope of J-V characteristics by applying (2) with using dark-current density versus voltage, as shown in the inset of Figure 5. From Figure 5 we observed that

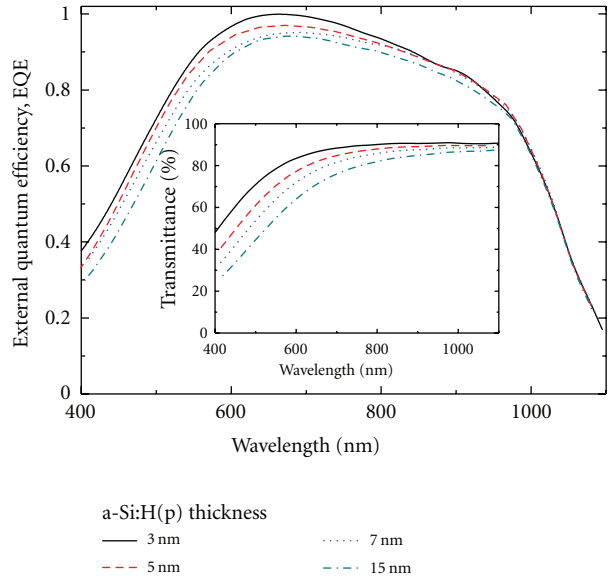

Figure 6: Variation of external quantum efficiency (QE) spectrum with a-Si : H(p) thickness. The inset shows that transmittance of a-Si : H(p) with different thickness was deposited on glass substrate.

$n \approx 1.25$ was obtained for a-Si : H(p) thickness of 3 nm and then this values increase with further increasing in layer thickness. The maximum of $n \approx 1.9$ was observed for layer thickness of 15 nm. Thus conduction mechanisms in our device are shifted from diffusion-recombination to recombination for thicker in emitter layer. The diffusion-recombination dominated for thinner emitter layer could be attributed to a smaller built-in potential in the ITO/a-Si : H(p)/c-Si(n) structure [9], leading to low V_{oc}. A similar variation with V_{oc} is also observed for *FF* with emitter thickness less than 7 nm; however, after passing through an optimum where the *FF* was maximized, a further increasing in emitter layer thickness resulted in a significant decrease of *F.F*. This could be owing to the serial resistance component and also a lesser probability of tunneling of holes through a-Si : H(p) layer as thickness increases.

In contract to V_{oc}, J_{sc} reduces with increasing emitter-layer thickness. As a result, we obtained a solar cell efficiency of 14.6% (V_{oc} = 590 mV, *FF* = 0.72, and J_{sc} =34.3 mA/cm^2) at the optimum thickness of p = 7 nm without the incorporation of surface texture, intrinsic hydrogenated amorphous silicon. In Figure 6, the external quantum efficiency (QE) spectrum as a function a-Si : H(p) thickness was depicted. For convincing, transmittance of a-Si : H(p) layer with difference thickness was also measured and shown in the inset of Figure 6. It is clear that the thicker in emitter layer leads to lower in transmittance due to Lambert-Beer law. Thus, the QE of the thinner film is enhanced especially in the short wavelength region where the absorption of the a-Si : H films is low. Hence, the reduction in J_{sc} shown in Figure 4 may come from the degradation of the short wavelength response. It is well known that heavily doped a-Si : H layers generally exhibit quite high defect densities of $\sim 10^{18}$ cm^{-3}, which is close to the defect densities of our a-Si:H(p) layer ($2.33 \sim 3.70 \times 10^{18}$ cm^{-3}), separately estimated by ellipsometry measurement on a-Si : H(p) films deposited on glass substrate. Due to its structure disorder and high doping, on the one hand, the diffusion length of the carrier in amorphous silicon layer is so small that only drifts current but no diffusion current can occur. On the order hand, the penetration depth of the space charge region in the a-Si : H side is so small that there is no electric field inside the layer. Thus, a heavily doped a-Si : H(p) layer incorporated into the heterojunction solar cells acts as a "dead layer". For that reason it has to be as thin as possible.

4. Conclusion

In conclusion, the a-Si : H(p)/c-Si(n) heterojunction solar cell was set up for future development of high efficiency heterojunction with intrinsic thin (HIT) layer solar cells. The correlation between doping concentration, a-Si : H(p) layer thickness, and cell performance was discussed. An optimum value for gas phase doping concentrations of a-Si : H(p) was found to be 3%. For high gas phase doping concentrations, on the one hand the band bending increases with increasing gas phase doping concentration, on the other hand the disorder in the a-Si : H layer and interface states (decreases in τ_{eff}) increases. Hence, solar cell efficiency degrades. The a-Si : H(p) thickness of 7 nm is optimum for a-Si : H(p)/c-Si(n) heterojunction solar cell. Degradation of open-circuit voltage or short-circuit current density and hence efficiency was observed for thinner or thicker layers. Using optimized conditions, we obtained 14.67% efficiency for the a-Si : H(p)/c-Si(n) structure.

Acknowledgment

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Research Article

Modelling of Light Trapping in Acidic-Textured Multicrystalline Silicon Wafers

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Acidic texturing has been widely used to reduce the reflection losses for silicon solar cells fabricated on multicrystalline wafers, however, there are few available models which attempt to predict the reduced reflection after texturing based on the morphology of the textured surfaces. An optical model which simulates the light trapping and scattering effects of acidic-textured surfaces based on the surface morphology is presented. The developed model was experimentally verified by reflection measurements from multicrystalline silicon wafers textured using different etching conditions. The relationship between weighted average reflection and surface morphology is demonstrated with some of the trends being explained by simulating reflection in different wavelength regions. The developed model could be embedded into solar cell simulation tools or adapted to predict optical properties of diverse surface morphologies.

1. Introduction

Surface texturing is a key process in the fabrication of silicon solar cells both in the laboratory and in commercial production. It provides enhanced light absorption with less front surface reflection, more internal reflection, and increased light path lengths inside the cell [1, 2]. A wide range of physical and chemical methods have been employed for texturing of silicon wafer-based and thin-film solar cells, including lithography [3, 4], mechanical grooving [5, 6], reactive ion texturing [7–9], laser texturing [10–12], alkaline [13–15], and acidic texturing [16–20].

Of these texturing methods, alkaline and acidic texturing have been widely adopted in the commercial production of silicon wafer-based solar cells due to their lower cost, amenability to high-throughput processing, and superior antireflection properties. Alkaline etchants etch the {100} planes of silicon much faster than the {111} planes. This anisotropic etching, when performed at low sodium or potassium hydroxide concentrations and temperatures of 80–90°C, results in the formation of pyramidal structures on {100} orientated monocrystalline silicon. These pyramidal structures trap the incoming light and reduce reflection effectively [2]. However, alkaline texturing performed on multicrystalline silicon results in largely untextured regions (where {111} crystal planes are exposed at the surface) and steps between grains due to the different grain orientations of the multicrystalline silicon [15, 21, 22]. Although acidic texturing of multicrystalline wafers results in higher average reflectance values than typically observed for alkaline texturing of monocrystalline wafers, the acidic texturing process is relatively low-cost and can be effectively performed as an in-line process in a manufacturing line. In fact, because of the ease of implementing acidic texturing compared to alkaline texturing, some silicon solar cell manufacturers select to also texture monocrystalline wafers using acidic texturing, because the difference in surface reflection between alkaline- and acidic-textured surfaces is reduced significantly after application of a silicon nitride antireflection coating and encapsulation.

Acidic texturing has also been employed to texture ZnO : Al transparent conducting oxide (TCO) layers, which serve as window layers in silicon-based thin-film solar cells [23]. It may also find application in the texturing of wafers produced using seeded casting processes [24]. The wafers that result from these new casting processes still contain

grains but have large regions of monocrystalline material. A number of different methods are being developed for large-scale manufacture of this new silicon material [24–26], and because it is likely that grain orientation cannot always be carefully controlled, acidic texturing may also find a role in texturing these new wafer surfaces.

Simulation tools, such as PC1D [27], contain models that simulate the reflection and light trapping for alkaline-textured solar cells and predict the electrical performance of textured solar cell devices. These tools enable higher level solar cell production line simulators, such as the Virtual Production Line (VPL), which has been developed at the University of New South Wales (UNSW) [28, 29], to relate the effects of different alkaline texturing conditions (e.g., chemical composition, time, and temperature) on final device electrical performance. The VPL simulation software is extensively used in the teaching of photovoltaic engineering at UNSW. However, the current version of this software can only simulate the reflectance of alkaline-textured surfaces, which limits its application to current manufacturing processes which involve the use of multicrystalline silicon wafers.

Although the chemical process for acidic texturing can be simulated [29], a model is required to predict the reflectance as a function of wavelength and hence the electrical performance of the textured solar cell device. The light-trapping properties of the acidic-textured surface morphology have not been extensively studied. Earlier studies have considered only the front-surface reflection properties of these surfaces [21, 22]. However, this paper describes a more comprehensive model which considers the reflection from the entire solar power spectrum, bulk absorption, and the contribution of the rear surface to light trapping. These enhancements to the model become critical as thinner wafers are increasingly used in the manufacturing of cells. Acidic texturing experiments were performed and the measured reflectance results were compared to those predicted by the model. The results suggest that the model can predict the reflection for a wide range of wavelengths. Further work is required to integrate this reflection model in solar cell simulators such as PC1D or higher level simulators such as VPL.

2. Model of Acidic-Textured Surfaces

Multicrystalline silicon surfaces textured using the UKN recipe for acidic texturing [18–20] are typified by an irregular array of concavities, or etching pits, as shown in Figure 1. These pits in the textured surface are generated by the etching of surface defects in the crystal structure caused by sawing damage. Unlike in alkaline texturing where an initial saw-damage etching process must be performed before the texturing, in acidic texturing the saw damage is removed during the texturing thus simplifying the manufacturing process. However, the weighted average reflectance (WAR) values achieved by alkaline texturing are significantly lower than those achieved with acidic texturing. Furthermore, if acidic texturing times are used that are longer than optimal, then the textured concavities become larger and flatter and the resulting surface is significantly more reflective [30].

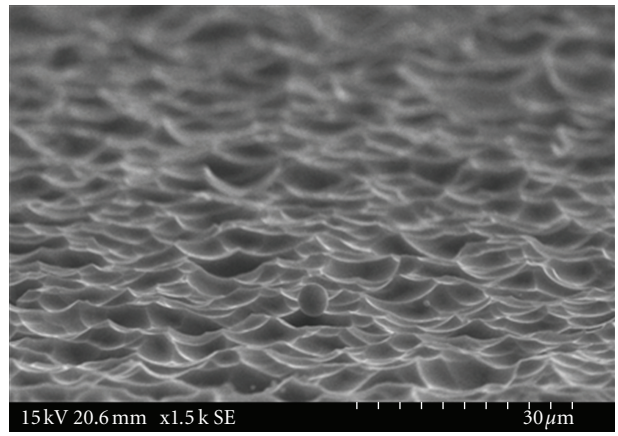

Figure 1: A scanning electron microscope (SEM) image of an acidic-textured multicrystalline silicon wafer surface showing the formation of randomly arranged etching pits on the surface. The surface was textured for 2 mins at 10°C in a solution comprising an $HF : HNO_3 : H_2O$ ratio of 15 : 50 : 35.

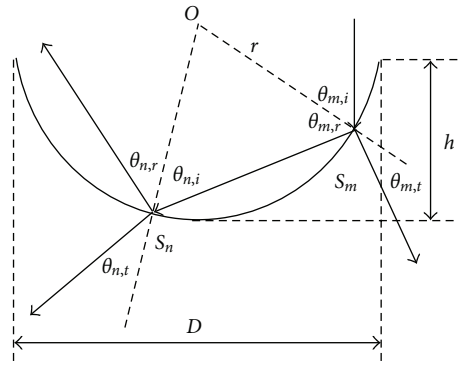

Figure 2: Schematic depicting a cross-section of a spherical cap, and the associated variables, used to model the etch pits of an acidic-textured surface.

To simplify the simulation of the reflection based on surface morphology described in this paper, a spherical cap surface was used to model the etching pit structure of the acidic-textured surface. The front-surface reflection, bulk absorption, rear surface reflection, and further internal reflections of light reaching each part of the etching pit were estimated, with the reflection of the wafer being estimated as the weighted average of all components.

2.1. Front Surface Scattering. The spherical model is shown schematically in Figure 2. The variables O and r denote the centre and radius of the sphere cap, and D and h donate the diameter and height of the sphere cap, respectively. The sphere cap is divided into small annular surface elements, $S_1, S_2, \ldots, S_m, \ldots, S_N$, each element having a subtended angle $d\theta$ to O. The kth-order reflection at the mth annular surface element is denoted using $R_{m,k}$.

It is assumed that incident light is directed perpendicularly to the silicon surface, and hence also perpendicular to the base of the sphere cap. Considering the incident light reaching annular surface element S_m with an incident angle of $\theta_{m,i}$ and a corresponding refracted angle of $\theta_{m,t}$, the primary reflection at the mth annular surface element S_m is given by

$$R_{m,1} = \frac{R_{\mathrm{TE}m,1} + R_{\mathrm{TM}m,1}}{2}, \tag{1}$$

where R_{TE} and R_{TM} represent the reflection of the transverse-electric and transverse-magnetic waves of the incident light, respectively. Light rays having a large incident angle can be reflected more than once as shown in Figure 2. The reflected ray intersects the sphere again at annular surface element S_n with the incident angle, $\theta_{n,i}$ and refracted angle $\theta_{n,t}$, which are equal to $\theta_{m,i}$ and $\theta_{m,t}$, respectively, before being reflected away from the surface. Thus, the front surface reflection R_{Fm} for the mth annular surface element is given by

$$\begin{aligned} R_{Fm} &= \prod_{k=1}^{k_m} R_{Fm,k} \\ &= \left\{ \frac{1}{2} \left[\frac{\sin^2(\theta_{m,t} - \theta_{m,i})}{\sin^2(\theta_{m,t} + \theta_{m,i})} + \frac{\tan^2(\theta_{m,t} - \theta_{m,i})}{\tan^2(\theta_{m,t} + \theta_{m,i})} \right] \right\}^{k_m}, \end{aligned} \tag{2}$$

where k_m donates the highest reflection order and is given by

$$k_m = \left\lfloor \frac{\pi}{\pi - 2\theta_{m,i}} \right\rfloor. \tag{3}$$

The expression in (3) is derived from internal angle sum of the polygon, which consists of the intersection points and O as its vertices.

2.2. Bulk Absorption. Considering the same incident light ray that reached S_m discussed above, the attenuation factor A_m after being absorbed inside the wafer is given by

$$A_m = e^{-\alpha x} = e^{-\alpha t/\cos\theta_{m,n}}, \tag{4}$$

where x denotes the actual light path length, t is the thickness of the wafer, α is the absorption coefficient, and $\theta_{m,n}$ is the refracted angle of light reaching annular surface element S_m referring to the normal direction to the wafer, as shown in Figure 3. This expression shows that the light path is increased due to the textured surface and hence the probability of absorption by the silicon wafer is increased for the light's first pass through the wafer.

2.3. Rear Surface Reflection. The rear surface is modelled using an inverted sphere cap as shown in Figure 4. The incident light reaching S_m on the front surface is scattered with an angle of $\theta_{m,n}$ and has the possibility of reaching the convex sphere surface at the rear of the textured wafer. To evaluate the angle distribution function (ADF) of the rear incident angles, the convex surface of the rear etch pit is divided into annular surface elements perpendicular to the incident light so, for example, light rays reaching different points on pth annular surface element S_p would have the same incident angle of θ_p. The ADF is determined by the projection area of the annular surface elements to the incident direction as represented by

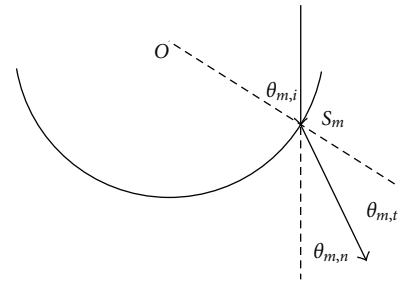

Figure 3: Schematic showing the path of a representative transmitted light ray, $\theta_{m,t}$ scattered within the wafer.

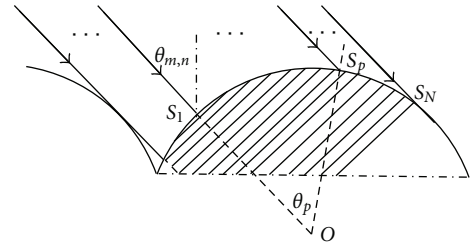

Figure 4: Schematic showing parallel light rays incident on the rear acidic-textured surface.

$$\mathrm{ADF}\left(\theta_p\right) = \frac{dS_p}{\sum_{p=1}^{N} dS_p} = \frac{\left(1 - \eta_p\right)\pi r_r^2 \left(\sin^2\theta_{p+1} - \sin^2\theta_p\right) G_p}{\sum_{p=1}^{N} dS_p}, \tag{5}$$

where dS_p is the projected area of unshaded part of pth rear annular surface element, η_p is the shading percentage of it induced by the adjacent etching pit derived from Figure 4, r_r is the radius of the sphere cap on the rear surface, and G_p is a geometric factor determining the fraction of annular surface element of the sphere cap exposed in the incident direction. The rear surface reflection R_{Rm} of the light, which entered via the mth annular front surface element, is the average of the light reflected from the convex surface of the weighted by the ADF as represented by

$$R_{Rm} = \sum_{p=1}^{N} R\left(\theta_p\right)\mathrm{ADF}\left(\theta_p\right). \tag{6}$$

Based on the primary reflection and absorption calculated above and the assumption that these values remain the same during internal reflection, the overall reflection of incident

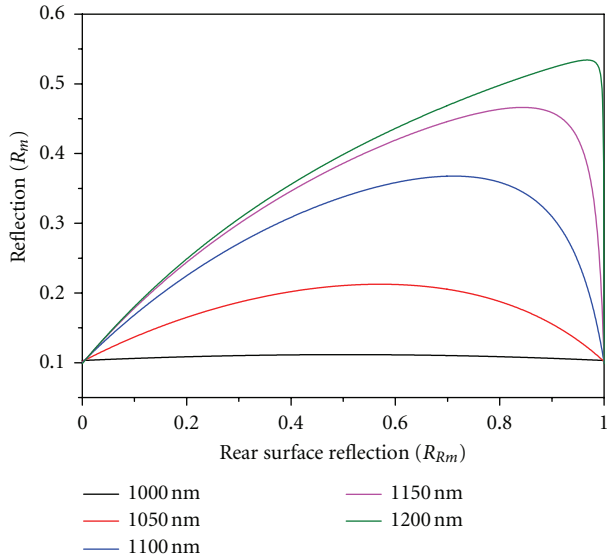

FIGURE 5: Reflection, R_m, as a function of rear surface reflection, R_{Rm}, for different wavelengths of incident light. The values of h/D and wafer thickness used in simulation were 0.25 and 200 μm respectively.

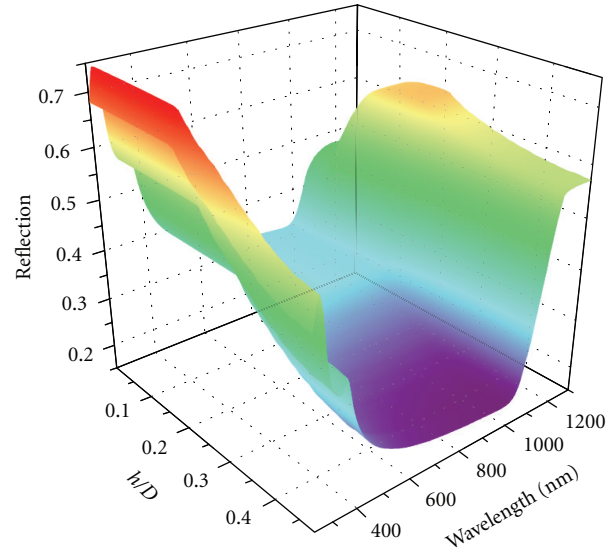

FIGURE 6: Reflection predicted by the model as a function of wavelength and surface morphology indictor h/D. The wafer thickness used in the simulations was 200 μm.

light reaching S_m at the front surface of a free standing acidic-textured bare (i.e., uncoated) silicon wafer can be expressed as

$$\begin{aligned} R_m &= R_{Fm} + (1 - R_{Fm})R_{Rm}(1 - R_{Rm})A_m^2 \\ &\quad + (1 - R_{Fm})R_{Rm}^3(1 - R_{Rm})A_m^4 + \cdots \\ &= R_{Fm} + \frac{(1 - R_{Fm})(1 - R_{Rm})R_{Rm}A_m^2}{1 - R_{Rm}^2A_m^2}. \end{aligned} \tag{7}$$

Figure 5 depicts the dependence of R_m on R_{Rm}. The value of R_m for wavelengths shorter than 1000 nm does not change with increasing values of R_{Rm} due to high absorption coefficient of this light and hence the high probability that this light is absorbed before it reaches the rear surface. However, for longer wavelengths of incident light, R_m first increases and then decreases with increasing R_{Rm}, with a very abrupt decrease being predicted for wavelengths of $\geq$1200 nm. This increase in R_m as R_{Rm} increases for longer wavelength light is due to the light, which is reflected from the rear surface, ultimately escaping from the wafer before absorption. This reflected loss of initially captured light is more likely for longer wavelength light, which has lower absorption coefficient and is more likely to encounter internal surfaces during its light path through the wafer. It is also enhanced for surfaces which are characterised by lower h/D values where light is coupled less obliquely into the wafer.

The overall reflection of the etching pit, R, is the average reflection of all annular surface elements weighted by their projection area, as given by

$$\begin{aligned} R &= \frac{1}{S}\sum_{m=1}^{N} R_m dS \\ &= \frac{1}{\pi(D/2)^2}\sum_{m=1}^{N} R_m \pi r_f^2 (\sin^2\theta_{m+1,i} - \sin^2\theta_{m,i}), \end{aligned} \tag{8}$$

where dS and S are the projected areas of the small annular surface element and sphere cap, respectively, and r_f is the radius of the sphere cap on the front surface, which is not necessarily the same as r_r due to processes like rear etching. Figure 6 shows the reflection calculated from (8) as a function of wavelength and h/D ratio. The calculations use light absorption coefficients and refractive indices at 300 K provided in [31].

3. Experimental

Texturing experiments were performed to examine the accuracy of the developed model. In order to show the relationship between reflection and surface morphology, multicrystalline silicon wafers of thickness 200 μm were textured in solutions comprising HF, HNO_3, and deionised water to achieve a range of etching pit scales by changing the etching conditions (e.g., chemical composition of the solution and reaction temperature).

The dimensions of the spherical cap (i.e., h and D) were estimated from SEM cross-sectional images taken from different locations through the wafer. For each wafer surface, values of h and D were estimated as the average of ~20 measurement points taken from five different SEM cross-sectional images. The reflection from the front surface of

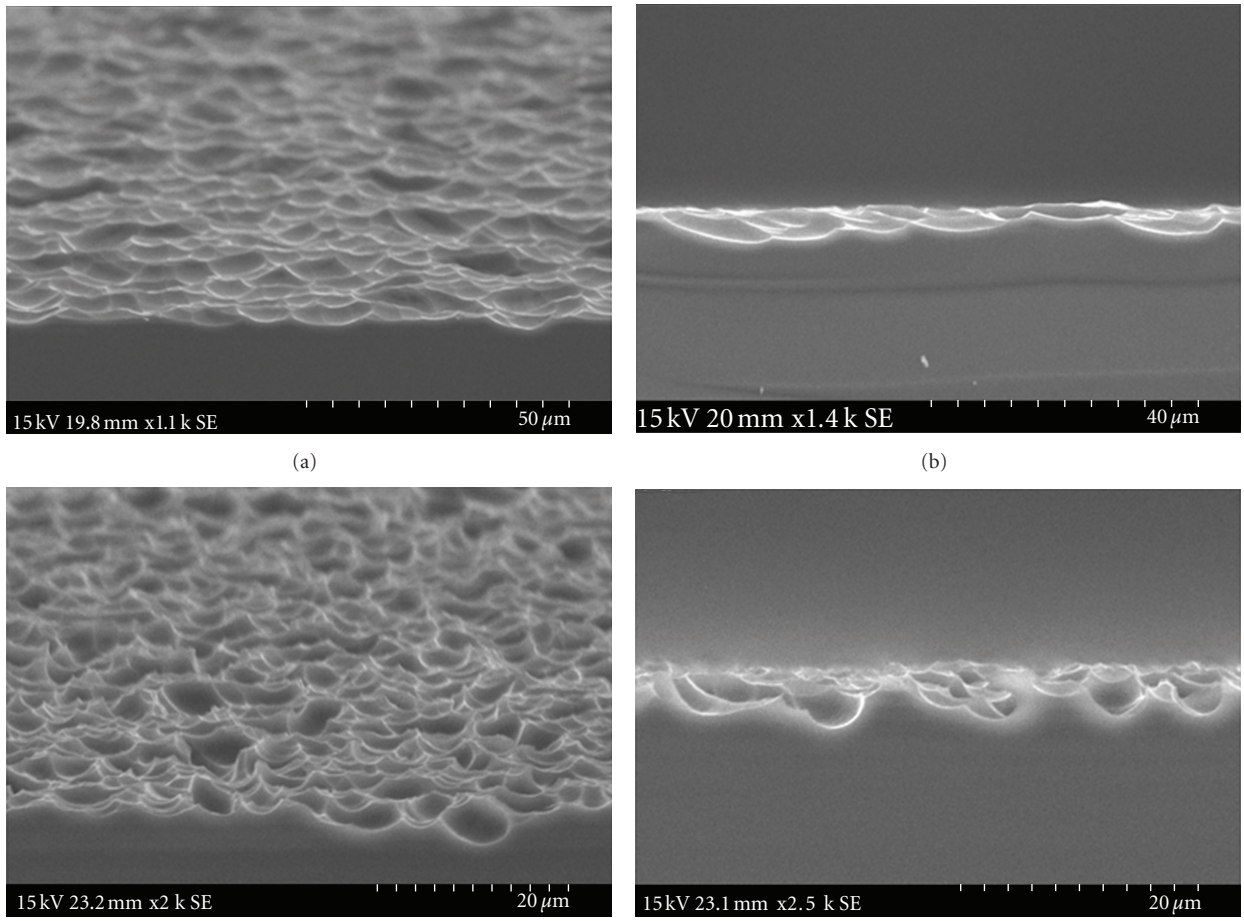

Figure 7: Scanning electron microscope images of the surface and cross sections of multicrystalline silicon wafer surfaces textured under two different conditions: (a,b) $HF : HNO_3 : H_2O = 15 : 50 : 35$, 25°C, 2 min; (c,d) $HF : HNO_3 : H_2O = 24 : 40 : 36$, 10°C, 2 min.

wafers, which had been textured on both sides, was measured for a wavelength range of 250 nm to 1300 nm using a Perkin Elmer spectrophotometer. It was estimated that <1% of the light that was transmitted through the wafer was reflected back into the wafer. Weighted average reflection values were calculated by weighting the measured reflection against the intensity of direct radiation in the AM1.5G spectrum.

4. Results and Discussion

Figure 7 shows SEM images of some of the different wafer surface morphologies that were observed after acidic texturing. It demonstrates how different etch pit geometries can be achieved using different etching conditions, with higher $HF : HNO_3$ ratios and lower texturing temperatures resulting in deeper pits which are characterised by larger h/D values. Figure 8 shows a comparison between simulated and experimental reflection of two textured wafers which had different h/D values over the wavelength range of 250 nm to 1300 nm. The simulated reflection data predicts the main trends in the experimental reflection curves, however, some inaccuracy in the simulated data is to be expected due to the simplified assumptions of the model (e.g., assumptions that the surface is characterised by a single h/D value). Furthermore, mismatches between regions selected for reflection measurement and SEM imaging may contribute to discrepancies between simulated and experimental reflection values. Values of h/D greater than 0.5 were not considered in this analysis because these surfaces involve more coupling of surrounding pits and possible porous silicon formation than surface morphologies that are typically observed with UKN texturing.

The relationship between the WAR and h/D was also investigated, due to the usefulness of WAR values in comparing different texturing methods. Figure 9 shows how the WAR varies with h/D values. The WAR does not vary significantly with increasing h/D until an h/D value of ~0.2, after which it begins to decrease and subsequently plateaus at a value of 0.24. The decrease in WAR, which occurs at ~0.2 in Figure 9, is due to the onset of higher-order reflection (i.e., $k_m = 2$). The critical value of h/D can be calculated from (3)

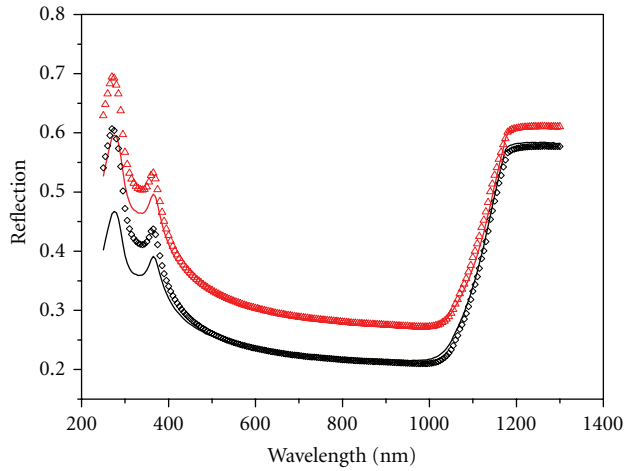

Figure 8: Simulated and measured reflection values graphed as a function of wavelength for two samples with different h/D values. Reflection values for $h/D = 0.25$ are shown in red with the solid line and (red triangle) symbols denoting the simulated and measured values, respectively. Reflection values for $h/D = 0.37$ are shown in black with the solid line and (◊) symbols denoting the simulated and measured values, respectively.

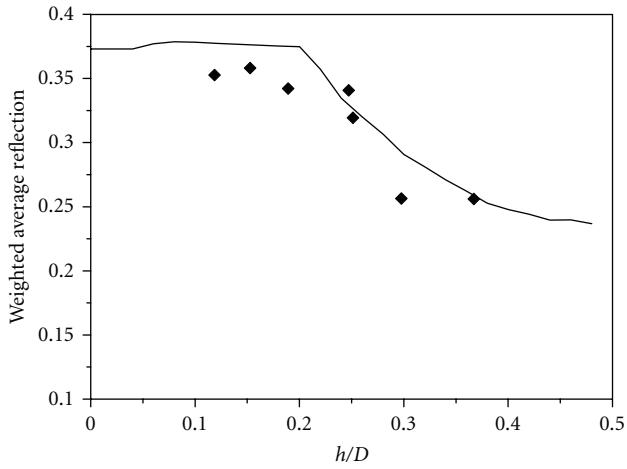

Figure 9: Simulated (solid line) and measured (♦) WAR values, computed using the wavelength range of 300 nm to 1200 nm, as a function of h/D.

to be 0.2071, after which the reflection is reduced due to the reduced front surface reflection.

The contribution of the rear surface reflection to the increased reflection predicted by the model and depicted in Figure 5 suggests that, at least for longer wavelengths when h/D is small and light has a greater probability of reaching the rear surface because of the shorter light path in the wafer, some increase in reflection is expected. By graphing the simulated WAR of the short (550–600 nm) and long wavelengths (1150–1200 nm) of light separately, as shown in Figure 10, this predicted increase in reflection is demonstrated for only the longer wavelength light.

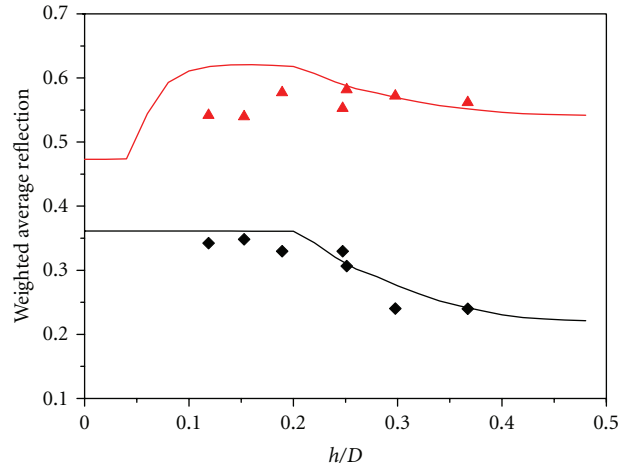

Figure 10: Simulated and measured WAR values for short-wavelength region (550 nm to 600 nm) and long-wavelength region (1150 nm to1200 nm) graphed as a function of h/D. The black solid line and (♦) values represent the simulated and measured values for the short wavelength region and the red solid line and (red triangle) symbols represent the simulated and measured values for the long-wavelength region.

However, although the model predicts the WAR reasonably well for the short wavelength light where the reflection is largely determined by the front surface, it appears to only successfully predict the reflection of long wavelength light for h/D values greater than ~0.25. For the cases where h/D is higher than the critical value of high-order reflection, the WAR of both short- and long-wavelength light decreases as h/D increases because the front surface reflection is effectively reduced by higher-order reflections within etching pits. However, as h/D becomes even larger, higher-order reflection only occurs on a smaller surface of the etching pit, thus the value of the WAR plateaus as the value of h/D approaches 0.5. For the region where h/D is lower than the critical value, the WAR of short wavelength light is substantially unchanged because there is no significant higher-order reflection arising from the front surface. The short wavelength light has a high probability of absorption before reaching the rear surface without requiring a lengthened light path due to front surface scattering.

Increased reflection for long wavelength light at low h/D values is not evident in the experimental data. This is most likely due to higher-order reflection not being considered in the rear surface reflection model described in Section 2.3. This can result in underestimation of the light path length in the wafer and hence higher predicted WAR values for low h/D values. However, the model appears to accurately predict the WAR for larger h/D values, because the longer light paths caused by the increased scattering increases the probability that the light is absorbed in the bulk and therefore reduces the sensitivity of the model to the rear surface reflection as shown in Figure 5. For small h/D values, light is coupled into the wafer at less oblique angles and hence experiences shorter light paths in the wafer and is less likely to be internally reflected.

5. Conclusions

An optical model was presented for the modelling of light trapping in acidic-textured silicon wafers. Sphere caps were used to model the etching pits that form during the texturing when the commonly-used UKN texturing process is used. The developed model was used to predict the reflection from bare acidic-textured multicrystalline wafers on the basis of the surface morphology which was varied by altering the texturing conditions. The model was shown to predict the reflection for a wide range of wavelengths. The model predicted that, for shorter wavelength light, the WAR was constant for small h/D values and then began to decrease at $h/D \sim 0.2$ where higher-order reflection effects became significant resulting in increased scattering of light in the wafer. For longer wavelength light, where the absorption coefficient is significantly reduced, the model predicted a small increase in WAR for small h/D values due to the shorter paths experienced by light that is coupled less obliquely into the wafer. This results in a greater chance of initially captured light escaping from the wafer on subsequent encounters with wafer surfaces. However, this increase in WAR for low h/D values was not observed experimentally. It is proposed that this was due to the fact that the rear surface reflection model used did not take into account the effects of higher-order reflection at the convex surface of the etching pits and thus, most likely, underestimated the length of the internally reflected light path.

The inaccuracies of the rear surface reflection model may not be critical for practical purposes because the rear surfaces of many acidic-textured silicon solar cells are partially planarised by a rear surface etching process used to isolate the junction to the front surface of the cell and then alloyed with aluminium to form a rear-surface field and rear-cell electrode. Consequently, the rear surface reflection model, developed here for bare wafers, will need to be further developed to more accurately represent the light trapping properties of final devices.

Finally, the model has the potential to be adapted for use in solar cell simulators, such as PC1D, or higher-level simulators such as the VPL where it can be used to relate acidic texturing processing conditions to final device efficiency and hence enhance the educational and training experiences for future PV engineers. The accuracy of the model could be enhanced by an improved characterisation of the surface morphology of the textured surfaces which are formed using different processing parameters, and further characterisation of the reflectance from final devices.

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Research Article

Effect of Processing Parameters on Thickness of Columnar Structured Silicon Wafers Directly Grown from Silicon Melts

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In order to obtain optimum growth conditions for desired thickness and more effective silicon feedstock usage, effects of processing parameters such as preheated substrate temperatures, time intervals, moving velocity of substrates, and Ar gas blowing rates on silicon ribbon thickness were investigated in the horizontal growth process. Most of the parameters strongly affected in the control of ribbon thickness with columnar grain structure depended on the solidification rate. The thickness of the silicon ribbon decreased with an increasing substrate temperature, decreasing time interval, and increasing moving velocity of the substrate. However, the blowing of Ar gas onto a liquid layer existing on the surface of solidified ribbon contributed to achieving smooth surface roughness but did not closely affect the change of ribbon thickness in the case of a blowing rate of $\geq 0.65\,\mathrm{Nm}^3/\mathrm{h}$ because the thickness of the solidified layer was already determined by the exit height of the reservoir.

1. Introduction

In the photovoltaic industry growing at rates exceeding 30% per year, crystalline silicon (Si) is the dominant photovoltaic material and accounts for approximately 90% of the total solar cell production [1]. However, the current bottleneck in crystalline Si photovoltaics due to the shortage of Si feedstock increases Si prices and puts additional pressure on the fraction of wafer cost in the module [2].

The direct growth technology of Si ribbon wafer from the molten Si is one of the several routes for responding to increasing Si wafer consumption with almost 100% silicon usage. Technology with no kerf loss and high productivity can significantly lower manufacturing costs for solar cells [3]. The ribbon Si technologies are generally classified in two ways by the transport direction of the solidified ribbon with respect to the movement of the liquid-solid interface during crystallization: (i) liquid-solid interface moves in line with ribbon transport direction (also called vertical growth, e.g., edge-defined film-fed growth (EFG) and string ribbon (SR)); (ii) liquid-solid interface moves almost perpendicular to the ribbon transport direction (also called horizontal growth, e.g., ribbon growth on substrate (RGS)) [4]. Horizontal growth has much faster ribbon growth rate than vertical growth, finally leading to the effective production of silicon wafers with low manufacturing costs and high production rates, because thermal conduction through the directly contacted substrate is more efficient at heat removal from the ribbon.

In addition, one option to make a more efficient use of the Si materials in horizontal growth system is the use of thinner Si wafers. For instance, the total amount of Si used per W_p decreases by about 20% when using $200\,\mu$m wafers instead of $300\,\mu$m wafers [5]. However, the effect of processing parameters such as preheated substrate temperatures, time intervals, moving velocity of substrates, and gas blowing rates on Si ribbon thickness has been rarely reported in order to achieve more effective Si usage in the horizontal growth process so far. The present investigation reports the experimental findings for processing parameters on the control of Si ribbon thickness in the horizontal growth process. These considerations will meet the demands for next-generation solar cell production with the optimum growth conditions for the desired thickness of the Si wafer.

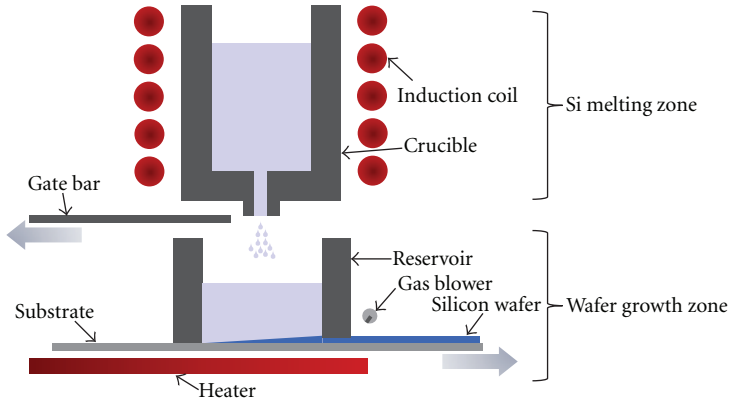


Figure 1: Schematic diagram of a horizontal growth system for ribbon-typed Si wafers.

2. Experimental Procedure

The system for the growth of columnar structured Si wafers shown in Figure 1 is separated into Si melting zones by induction coil and ribbon-type wafer growth zones in a vacuum chamber. After the Si (purity > 9N) in the melting zone is completely melted by heating to 1450°C at a pressure of 10^{-4} Torr, liquid Si is poured into the SiC-coated graphite reservoir positioned at the growth zone. As soon as liquid Si is solidified by releasing the latent heat through the SiC-coated graphite substrate preheated at a range of 700–1000°C and moved underneath the reservoir with a velocity of 315 ~ 926 cm/min after a certain amount of time (hereafter called time interval) at a range of 0.5–2.5 sec, then the solidified Si on the substrate moves away from the exit of the melt reservoir of 1 mm. At the moment, the blowing of Ar gas on a solidified wafer surface removed liquid Si residue at a flow rate of 0.5–1.1 Nm^3/h, which improved the surface roughness of the Si wafer as a consequence. Dense SiC layer with thickness of around 50 μm and surface roughness of around 4 μm was coated on graphite substrate by commercially available chemical-vapor-reaction (CVR) method at 1700°C in vacuum, where the surface modification provided the advantage for preventing the carbon contamination from graphite remaining high thermal conductivity. The dimension of the Si wafer, especially the thickness, could be determined by the control of processing parameters such as substrate temperatures, time intervals, moving velocity of substrates, and gas blowing rates. Horizontal growth systems and experimental procedures of Si wafers are described elsewhere in detail [6].

The thickness of as-grown Si wafers was measured by a sharp-tipped micrometer to be approximately 1mm without an additional polishing step, in which five measurements were carried out and averaged. The Si wafer was etched using a 10% KOH solution to measure the microstructures and defects of the wafer using a differential interference contrast optical microscope (BX60MF, Olympus, Japan).

3. Results and Discussion

The thickness of the ribbon-type silicon wafer grown in a horizontal growth system can be controlled by the shape and height of the reservoir exit if it is possible to perfectly engineer the liquid-solid interface in the reservoir. However, fine control of the liquid-solid interface only with the reservoir structure is very difficult in nature without considering processing parameters such as substrate temperatures, time intervals, moving velocity of substrates, and gas blowing rates. Therefore, this study aims to present a manner to control the thickness of columnar structured-silicon wafers horizontally and directly grown from silicon melts. The area for the growth interface of liquid-solid is now very large compared to the wafer thickness in the horizontal growth system. The latent heat of the silicon melt is extracted mainly by conduction through the substrate and also partially by radiation through the surface of the silicon melt. One of the reasons for the high productivity during the horizontal growth system is the ability of the substrate to dissipate heat through the bottom side that allows for better control of solidification, through the moving velocity and heat extraction rate [7]. Therefore, pull speed of the substrate and heat extraction on the substrate are important variables in optimum Si wafer production. Growth rates of 4–9 m/min in horizontal growth systems have been previously demonstrated [8].

Figure 2 shows the thickness variation of ribbon-type Si wafers depending on the substrate temperature preheated at the range of 700–1000°C at the constant time interval of 2.5 sec, moving velocity of the substrate of 485 cm/min, and blowing rate of Ar gas of 0.8 Nm^3/h. Substrate temperature strongly relates to behaviors of heat extraction of solidified Si wafers. Even though the substrate is preheated up to 1000°C, the onset of solidification starts due to temperature differences between Si melt (~1414°C) and substrates. Solidification rate increases with decreasing substrate temperatures because of larger temperature differences. At the moment, the temperature of the melt can be more rapidly decreased by the heat extraction through the cold ceramic substrate. Therefore, higher substrate temperatures were

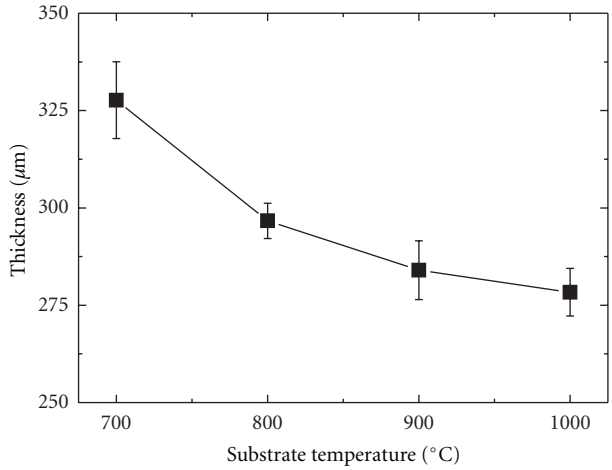


Figure 2: Thickness variation of ribbon-type Si wafers depending on the substrate temperature preheated at the range of 700–1000°C at the constant time interval of 2.5 sec, moving velocity of the substrate of 485 cm/min, and blowing rate of Ar gas of 0.8 Nm^3/h.

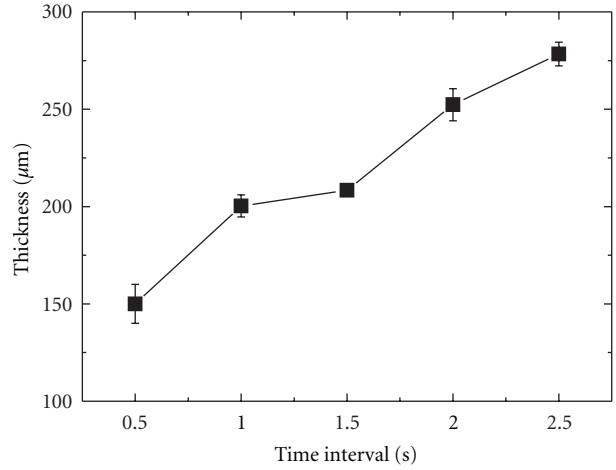


Figure 3: Thickness variation of ribbon-type Si wafers depending on the time interval at the range of 0.5–2.5 sec at the constant substrate temperature of 1000°C, moving velocity of substrates of 485 cm/min, and blowing rate of Ar gas of 0.8 Nm^3/h.

beneficial to obtain thinner Si wafers, which could contribute to reduce the Si consumption.

Assuming steady-state conditions, consideration of thermal flux during the growth of ribbon-type silicon wafers in the horizontal growth system is used to calculate the dependence of wafer thickness on the moving velocity of the substrate at a given temperature gradient between the silicon melt and substrate with (1) as follows [9]:

$$V_p = \frac{4\alpha\lambda_s s}{(2\lambda_s - \alpha t)dL\rho_s}\Delta T, \quad (1)$$

where V_p is the moving velocity of the substrate (pulling speed), α the effective coefficient of heat transfer, s the length of the liquid-solid interface, λ_s the thermal conductivity of solid silicon, d the wafer thickness, ρ_s the density of solid silicon, L the crystallization heat of silicon, t the crystallization time, and ΔT the temperature gradient between the melt and substrate. The substrate temperature determines the ΔT and a lower substrate temperature increases the growth velocity according to the above equation. In this study, the temperature of liquid Si was > 1412°C when the melt was poured. Temperature differences, ΔT, were about > 400°C due to the substrate temperature pre-heated in the range of 700–1000°C. Note that wafer thickness, d, can be easily controlled by operating ΔT if V_p $(= ds/dt)$ is set at a constant moving velocity and the rest of the parameters such as α, s, λ_s, ρ_s, L, t in the equation are fixed. Therefore, thickness, d, decreases with the decreasing temperature gradient, ΔT, by fast solidification time.

In equipment for the growth of Si wafers in this study, the zone for the melting of Si materials and the zone for the growth of Si wafer are separated for the fabrication of more homogeneous wafer quality. Figure 3 shows the thickness variation of ribbon-type Si wafers depending on the time interval in the range of 0.5–2.5 sec at the constant substrate temperature of 1000°C, moving velocity of substrate of 485 cm/min and blowing rate of Ar gas of 0.8 Nm^3/h. The thickness of the wafer increased with an increased time interval because a longer time interval allows for the increase of residence time in a reservoir filled with high-temperature melt, which allows for longer and slower growth time by increasing the solidification time. This is also supported by (1) which indicates that a longer time interval induces a longer crystallization time, t, resulting in a thicker wafer. Slower growth occurring with increasing thickness of the wafer is due to the additional heat transport through the solidified silicon. As soon as silicon melts in the melting zone are poured into the reservoir, crystal growth begins on a cold (below silicon melting temperature) substrate underneath the reservoir. Then, the substrate, pre-heated up to a desired temperature, is continuously moved underneath the reservoir filled with silicon melts after a certain time interval. Once the thickness of the initial wafer is determined during the crystal growth with a certain time interval, the thickness of the following wafer by the movement of the substrate tends to depend on the thickness of the initial wafer. Therefore, the time interval is one of the important factors to control the thickness of ribbon-type silicon wafers especially in a continuous growth system.

Figure 4 shows the thickness variation of ribbon-type Si wafers depending on the moving velocity of the substrate (pulling speed) at the range of 315–926 cm/min at a constant substrate temperature of 1000°C, time interval of 2.5 sec, and blowing rate of Ar gas of 0.8 Nm^3/h. The lowest moving velocity of 315 cm/min in this study induced an excessively increased wafer thickness of 753 μm, but increasing moving velocity up to 926 cm/min drastically reduced the thickness of the wafer up to 145 μm due to decreasing the solidification time. However, defects such as pores were detected on the wafer surface in cases where the moving velocity exceeded above 926 cm/min. Compared to other silicon crystallization methods, the silicon crystal growth rate is very high, which is applicable to enhance a competitive price in the

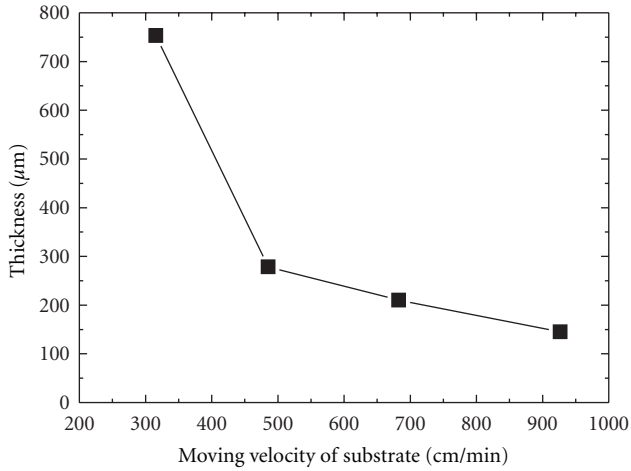


Figure 4: Thickness variation of ribbon-type Si wafers depending on the moving velocity of substrates (pulling speed) at the range of 315–926 cm/min at the constant substrate temperature of 1000°C, time interval of 2.5 sec, and blowing rate of Ar gas of 0.8 Nm^3/h.

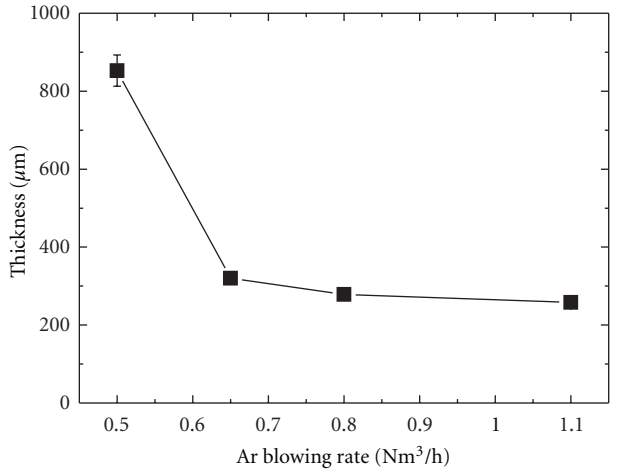


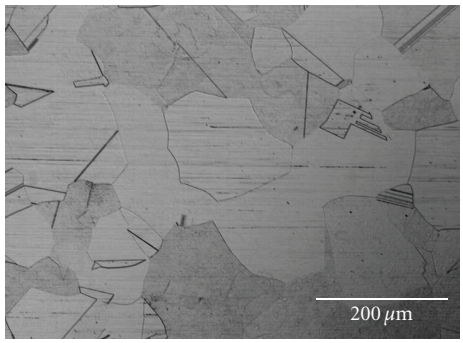
Figure 5: Thickness variation of ribbon-type Si wafers depending on the blowing rate of Ar gas at the range of 0.5–1.1 Nm^3/h at the constant substrate temperature of 1000°C, time interval of 2.5 sec, and moving velocity of substrates of 485 cm/min.

solar cell industry. The moving velocity essentially affects the residence time of the melt mass subject to the heat extraction rate through the substrate [7]. At low moving velocity, the longer residence time affords nearly complete solidification of the upper part of the silicon film. However, high moving velocity with a higher productivity encourages that a substantial portion of the upper layer of silicon wafer is still in liquid phase, which means that wafer thickness should be controllable by following the processing step such as the blowing of Ar gas onto the surface of liquid silicon film on solid silicon film.

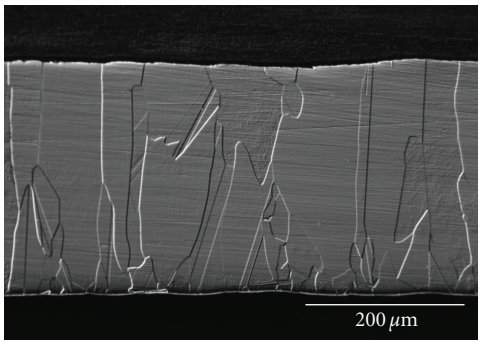
From the results by Schönecker et al. [10], the initial crystal growth velocity is high in the beginning of the process but decreases rapidly. The reason is caused by the facts that (i) the substrate temperature is not constant during crystal growth, (ii) there is a finite heat transfer between liquid silicon and the substrate, which slows down the crystallization speed, and (iii) the silicon melt is most likely in turbulent flow, transporting heat from the hotter top surface of the melt to the liquid-solid interface. Therefore, the crystallization speed affecting wafer thickness is lower in reality, depending on system properties such as silicon-substrate properties, melt temperature, and melt flux behavior. It is very difficult to fabricate continuously grown wafers with uniform thickness with high reliability in the industrial field.

In order to solve the problem, the blowing system of Ar gas is employed in this study. Figure 5 shows the thickness variation of ribbon-type Si wafers depending on the blowing rate of Ar gas at a range of 0.5–1.1 Nm^3/h at the constant substrate temperature of 1000°C, time interval of 2.5 sec, and moving velocity of substrates of 485 cm/min. Thickness was not reduced at the lowest blowing rate of 0.5 Nm^3/h in this study because a low blowing rate is not sufficient to flatten the surface with a liquid portion. However, a blowing rate of more than 0.65 Nm^3/h could considerably reduce the thickness compared to wafer thickness in the case of a blowing rate of 0.5 Nm^3/h. Although there was an effect on the decrease of wafer thickness above 0.65 Nm^3/h, thickness variation is not as large at the range of 0.65–1.1 Nm^3/h. The solidification height (thickness of solid film) is determined at a certain time interval in the reservoir filled with silicon melts, in which solidification rapidly begins as soon as silicon melts make contact with cold substrate. The thickness of casted film (liquid film on solid film) is strongly dependent on the exit height of the reservoir. If the thickness of solid film is determined in the reservoir at a certain time interval before the casted film on the substrate moves to the blowing zone of Ar gas, thickness is no longer reduced to below the thickness of solid film in casted film even with a high Ar gas blowing rate. However, the step of Ar blowing was considerably effective on processing for thin wafers with smooth surface roughness if the melt layer remained on the surface of solidified wafer.

Figure 6 shows optical microscope images for the surface and cross-section of as-grown ribbon-type silicon wafers at a substrate temperature of 1000°C, time interval of 2.5 sec, moving velocity of the substrate of 485 cm/min, and a blowing rate of Ar gas of 0.8 Nm^3/h. While some grains are almost dislocation-free, others contain a high density of dislocations. Silicon wafers grown in a horizontal growth system usually have a high density of grain boundaries, dislocations, twins, and other intragrain defects because large thermal stresses are generated during rapid solidification and subsequent cooling [1]. The inhomogeneous distribution of dislocations is due to the fact that the thermal stress exceeds the critical shear stress only in some particular orientated grains. Grains with none or a low density of dislocations usually contain twin boundaries, while those with highly dislocated grains usually do not have twins. This means that twin planes act as barriers for dislocation propagation and contribute to the inhomogeneous distribution of dislocations across various grains [1]. A typical surface image (Figure 6(a)) of a wafer shows a mean grain size of around 150 μm and rather low densities of



(a)



(b)

Figure 6: Optical microscope images for (a) surface and (b) cross section of as-grown ribbon-type silicon wafers at a substrate temperature of 1000°C, time interval of 2.5 sec, moving velocity of substrates of 485 cm/min, and blowing rate of Ar gas of 0.8 Nm^3/h.

dislocation and twin through the consideration of processing parameters compared to previous reports [1]. However, subsequent steps for increasing grain size and stress relief in wafers are presumably necessary for improved efficiency of solar cells. A cross-sectional image (Figure 6(b)) typically indicates a columnar grain structure and smooth surface roughness by the blowing effect of Ar gas. Although there are relatively few grain boundaries in the up-and-down direction, it is expected that those columnar structures will induce an excellent result through current flows along the grain boundaries in the cells [11].

4. Conclusion

Processing parameters such as a pre-heated substrate temperature, time interval, moving velocity of substrates, and the gas blowing rate to control the thickness of the Si ribbon thickness were investigated for achieving more effective Si usage in the horizontal growth process. The substrate temperature strongly related to the change of ribbon thickness depending on the behavior of heat extraction of solidified the Si wafer. Higher substrate temperatures were beneficial to obtain thinner Si wafers, which could contribute to reduce the Si consumption. A longer time interval allows the increase of residence time in the reservoir, so that ribbon thickness increased by increasing the solidification time. The highest moving velocity of 926 cm/min in this study significantly reduced the thickness of wafers up to 145 μm, because the moving velocity essentially affects the residence time of the melt mass subject to the heat extraction rate through the substrate. The effect of Ar blowing was negligible if the thickness of solid film is determined in the reservoir. However, the step of Ar blowing was considerably effective on processing for thin wafers with smooth surface roughness. Processing conditions were established to grow the desired thickness of the Si ribbon with the columnar grain structure and smooth surface roughness in a horizontal growth process for low-cost solar cell application.

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