

Research Article

Design of a Nanosecond Voltage Comparator with PECL Logic for a Photon-Counting Radiation Imaging System Application

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In this paper, a nanosecond voltage comparator with PECL logic for a photon-counting radiation imaging system is presented. To realize a high-speed comparison of four gamma detector channels in a limited board space, quad comparators MAX9602 with PECL logic are chosen. Each of the four channels is coupled with a PECL to CMOS converter ICS508, which exports CMOS logic data for later use in an FPGA. Simulated findings for cobalt-60 with intensities ranging from 30 Ci to 300 Ci show little count loss caused by using a comparator and indicate ideal propagation delays at all source intensities. While in the laboratory test using a PCB-level system, signals with pulse width less than 3 ns might be dropped, and dispersion of propagation delay occurs. Despite these, the performance is still satisfactory and can meet the requirements of practical applications, as demonstrated by an improved result of 0.9% in the contrast indicator model. Further studies to optimize the circuit design can be conducted to gain improvement.

1. Introduction

The radiation imaging system plays an important role in medical diagnostics and safety checks. To improve its performance, a novel type of detector that operates in a photoncounting mode is being extensively studied. Different from the conventional system utilizing analog current integration, photon-counting system counts individual photons [1], and a comparatively high count rate has appeared in the photoncounting system. For instance, Chmeissani et al. tested the Medipix2 + CdTe photon-counting hybrid detector which has reached the count rate of about $2 \times 10^6 \text{ cps/mm}^2$ [2]. Later, studies have demonstrated higher count rates of $6 \times 10^6 \text{ cps/mm}^2$ [3] and 10^7 cps/mm^2 [4], and both are equipped with CdTe photon-counting detectors. A detailed description of a large container inspection photon-counting system designed by our team is given in [5]. While LYSO scintillation detectors and a silicon photomultiplier (SiPM) are used for high-energy detection in our system, γ

radioisotope cobalt-60 (Co-60) is taken as the source, which is much more preferable in large container inspection [6], for the reason that Co-60 emits γ -rays with higher energy than the X-ray machine and is easier to calibrate and maintain than accelerators. In addition, when the Co-60 intensity varies between 30 and 300 Ci, our system displays a high count rate of $3.44 \sim 34.4 \times 10^5$ /s with a narrow pulse width of only 61.42 ns on average.

The ability to perform energy analysis, also known as amplitude analysis, on each discrete signal is a key benefit of photon-counting systems. Co-60 emits both 1.17 MeV and 1.33 MeV γ photons, with an average energy of 1.25 MeV. Interference signals mainly include scattered photons and electronic noise, and the energies carried by them are less than 1.25 MeV. According to the reaction principle of γ -rays with detectors [7], the voltage peak is proportional to the energy carried by the detected signal. Amplitude analysis can therefore be used to filter out interference signals, and an analog-todigital converter (ADC) and a voltage comparator are commonly used to carry out this operation. However, to discriminate the target signals with high speed and narrow pulse width, ADCs need to reach GHz-scale sampling rates. Consequently, costs and power consumption are exponentially increased, and this drawback impedes the application of massive systems [8]. For example, the AD9625 chip with a 2.6 GHz sampling rate might cost up to \$837 and dissipate up to 4 W; besides, large-scale application will be challenging given the power supply measures and the occupied area. While due to the small number of operations, comparators are crucial circuits to achieve high speed in converting analog signals into digital form [9]. To implement the function of analog-to-digital conversion and eliminate interference signals with smaller amplitudes, we here select a multichannel voltage comparator. For the majority of currently used data capture systems, application specific integrated circuits (ASICs) that do not necessitate autonomous submodule design are frequently used. For instance, Medipix read-out chips developed by the CERNhosted collaboration are directly used in numerous photoncounting systems [2, 10, 11]. Despite the simplicity of use and excellent performance, it cannot be independently manufactured or upgraded.

In this study, independent design and manufacturing are conducted around the selected core comparator component that operates under PECL logic, and to our knowledge, similar studies are rarely seen in the existing literature. We also offer a strategy for converting the less commonly used PECL logic to enable communication between comparators and field-programmable gate arrays (FPGAs). The designed comparator circuits are tested in both simulation and laboratory environments. Finally, the comparators are used in practical applications to mitigate the impact of interference signals on radiation images.

2. System Overview and Signal Characteristics

In a photon-counting radiation imaging system that counts individual photons emitted by the Co-60 γ radioisotope, a high count rate is needed, and thus, narrow pulse width is critical. In order to obtain narrow pulse width, a narrowing filter circuit coupled with a current sensitive preamplifier is placed behind the detector, followed by the voltage comparator and photon-counting modules (see Figure 1). However, the energy resolution will suffer if the signal pulse width is too small. To balance the effects of both, the pulse width is narrowed to about 60 ns while maintaining an energy resolution of 10% (@1.25 MeV) [5].

The detection efficiency (η) of the detector to a 1.25 MeV γ -photon is around 73%. After processing by a narrowing filter circuit, the pulse width (t_w) ranges from 30 to 200 ns with an average value of 61.42 ns. Then, the no-load count rate (\overline{n}) and the pileup rate (P) under different source intensities can be calculated using equations (1) and (2), respectively:

$$\overline{n} = 2n_0 \cdot \frac{d^2}{4\pi r^2} \cdot \eta, \tag{1}$$

$$P = 1 - e^{-\overline{n} \cdot t_w},\tag{2}$$

where n_0 is the initial intensity of Co-60 (unit: Ci, i.e. 3.7×10^{10} /s), d^2 is the entrance window area of the detector unit, and *r* is the distance between the radioactive source Co-60 and the detector. n_0 is multiplied by 2, for the reason that Co-60 emits both 1.17 MeV and 1.33 MeV γ photons. In our system layout, d^2 is 1×1 cm² and *r* is 6 m. With these parameters, the no-load count rate and the pileup rate under different source intensities can be calculated (see Table 1).

Signal characteristics can be summarized from Table 1:

- High-frequency signals with narrow pulse width: The average pulse width is only 61.42 ns, and the signal average frequency under 300 Ci intensity is 3.58 MHz, which is a quite high speed in the field of radiographic imaging.
- (2) Aperiodic stochastic signals that may pile up together: As illustrated in Table 1, the pileup rate under higher intensity is much larger than that under lower intensity. If two signals pile up together as shown in Figure 2, they may be recognized as one signal by the comparator, which will reduce the count rate. Moreover, when the reference voltage (V_{ref}) is lower than the junction value of two pileup signals, one count is bound to be dropped, and this cannot be avoided despite using a good performance comparator. This forms the endogenous factor of measuring errors.

To avoid exogenous causes of measuring errors, higher demands are placed on comparator design. The following requirements are defined: (1) good time response, which is usually expressed by propagation delay time (i.e., time taken by the input signal to compare and propagate to the output [12]), (2) high circuit integration, which can be achieved with a highly integrated multichannel chip and is suitable for massive systems, and (3) an output level that can be accepted by the FPGAs, such as TTL and CMOS, has to be realized.

3. Materials and Methods

3.1. Device Selection. We choose quad-channel comparators to improve circuit integration. The comparator products with the smallest propagation delay from three major manufacturers are compared in Table 2.

Generally, price and power consumption increase with a decrease in propagation delay time. The principle of selection is to give priority to products with low power consumption and price under the premise of meeting application requirements. Therefore, we first simulate MAX961 to test whether a propagation delay of 4.5 ns can meet the demand.

We take pulse signals with 1 V amplitude and 50% highlevel duration as the input, which has equal rise and fall times. Its period (*T*) and the reference voltage (V_{ref}) can be adjusted, as shown in Figure 3(a). Here, the value of V_{ref} is set to 0.5 V. Simulations are conducted in SIMetrix software. Simulation results of MAX961 are shown in Figure 3(b). When the frequency reaches 100 MHz, the low level cannot reach the typical value, but there is still possibility for differential identification to occur, while it works in an unstable



FIGURE 1: Composition and signal flow of a radiation imaging system.

TABLE 1: Characteristics of comparator input signals.

Source intensity (Ci)	Detection efficiency (%)	No-load count rate	Pileup rate (%)	Average pulse width (ns)	
30		$3.58 \times 10^{5}/s$	2.18		
50	72	$5.97 \times 10^{5}/s$	3.60	(1.42)	
100	/3	$1.19 \times 10^{6}/s$	7.07	61.42	
300		$3.58 \times 10^{6}/s$	19.75		

The no-load count rate and the pileup rate under different source intensities are calculated by equations (1) and (2), respectively.



FIGURE 2: Schematic diagram of the pileup effect: when V_{ref} is lower than the junction value, a count loss will occur.

Manufactures	Device	Propagation delay time (ns)	Current supply (mA/comparator)	Output type	Price (\$)
	MAX9602	0.5	10	PECL	7.93
MAXIM N	MAX961	4.5	5	TTL/CMOS	5.54/9.45
	MAX901	8	2.5	TTL	7.53
TI	LMH7324	0.7	4.3	PECL	6.91
	LT1721	4.5	4	TTL/CMOS	5.18

3.6

7

TABLE 2: Parameters of quad-channel comparators from three major manufacturers [13, 14].

condition as the signal frequency increases to 150 MHz. However, the frequency of the two consecutive events (pileup) has great possibility to reach 150 MHz.

AD8564

ANALOG

Between LMH7324 with 0.7 ns delay and MAX9602 with 0.5 ns delay, MAX9602 is more capable for high-speed application in a limited board space with less area occupation. Although their price is similar to the same output type and the power consumption of LMH7324 is lower,

MAX9602 has the advantage of adopting a less complicated power supply approach.

TTL/CMOS

4.29

The pulse signal displayed in Figure 3(a) is also used as the input for testing MAX9602. As shown in Figure 3(c), with the rising frequency, the low level gradually deviates from the typical value (VCCO_-1.72 = 3.28 V). However, even at a 1 GHz input frequency, the output low level is still below the upper limit of VCCO_-1.55 (3.45 V),



FIGURE 3: (a) Input signal diagram. (b) Simulation results of MAX961 and (c) MAX9602. In both simulations, V_{ref} is set to 0.5 V, and only positive output stages are displayed here.

demonstrating the applicability of the MAX9602 voltage comparator in high-speed fields.

3.2. Introduction to PECL. PECL, originating from ECL but using a positive power supply, is suitable for high-speed serial and parallel data links [13]. As can be seen in Table 2, the devices LMH7324 and MAX9602 with a short delay time of less than 1 ns are both PECL output types. The advantages of PECL can be summarized as follows:

(1) With a relatively small swing of only 0.78 V (see Table 3), the charge and discharge time of stray capacitance is quite short when the circuit state is switched, which guarantees the high-speed performance of PECL.

- (2) PECL output impedance is low, typically in the order of $(4-5) \Omega$, which provides superior driving capability.
- (3) Differential input and output structures ensure strong anti-interference capability. The fully differential circuit is preferred to the single-ended circuit because of its noise immunity to external noise [14].
- (4) PECL devices are less sensitive to synchronous changes in supply voltage, sometimes allowing the circuit to have a wide supply voltage range of up to 10%.

In contrast, the disadvantage of PECL logic is that the circuit always works in a conducting state, resulting in high power consumption.

There must be a receiver that can match the PECL output; therefore, the DC-coupling method between the PECL driver and the PECL receiver is noteworthy. A commonly used DC-coupling circuit is shown in Figure 4.

3.3. Circuit Design. The quad comparators, MAX9602, require both positive (VCC) and negative (VEE) supply voltages. Thus, we apply a dual DC/DC converter named LT8471 to provide the ± 5.0 V supply voltages required by MAX9602. MAX9602 has four differential output stages, and the output level of each stage can be different, which is controlled by the corresponding logic supply voltage (VCCO_). As can be seen in Table 3, the difference between high and low levels is always 0.78 V regardless of the value of VCCO_, which is consistent with the high-speed performance of PECL logic. However, the absolute values of high and low levels are related to VCCO_. The simulation results in Figure 5 have confirmed the above statement. We set all the four VCCO_ power supplies to +5.0 V, which can also be provided by LT8471.

The analog input signal should be connected to the positive stage of the differential input pair, with the negative stage providing a reference voltage to achieve the function of comparison. Each input trace has a 49.9 Ω termination resistor to avoid signal reflections. The reference voltage can be adjusted from 0 to 2.5 V by using a potentiometer; then, a voltage follower is connected behind to keep the reference voltage stable.

After the interference signals are eliminated by using the comparator, an FPGA is needed to collect the output highlevel digital signal. However, PECL logic is not among the I/O standard specifications of FPGAs [15]; therefore, the I/O standard should be converted into a logic that FPGAs can accept. A PECL to a CMOS converter, ICS508, is selected in the design. LTC3569, a triple DC/DC converter, is used to provide a 3.3 V supply voltage to the CMOS output buffer of ICS508, which also supplies I/Os of FPGAs. The other two channels of LTC3569 switch 5.0 V to 2.5 V and 1.2 V respectively, in which 2.5 V is used to power the phase-locked loops (PLLs) of FPGAs as well as providing the upper limit of the reference voltage in the comparator circuits and 1.2 V serves as the supply voltage for the internal logic of FPGAs.

As displayed in Figure 4, in order to couple PECL driver MAX9602 and PECL receiver ICS508, the output from the driver needs to drive a 50 Ω load to VCC-2 V. However, the potential of VCC-2 V is not available in the designed network, and it is often preferable to find a Thèvenin equivalent circuit. Figure 6 shows the result of the Thèvenin transformation, where VCC=5.0 V has already been acquired.

The Thèvenin equivalent circuit imposes the conditions:

$$VCC - 2V = VCC\left(\frac{R2}{R1 + R2}\right),$$

$$\left(\frac{R1}{R2}\right) = 50\Omega.$$
(3)

With VCC = 5.0 V, the derived values would be $R1 = 82 \Omega$ and $R2 = 130 \Omega$. Based on the above analysis, the main comparator circuits are shown in Figure 7, taking one

channel as an example, since the connections of the other three channels are the same.

The sketch of the main functional parts and the signal connections are shown in Figure 8(a), and the PCB board is displayed in Figure 8(b). For high-speed differential signals, the differential traces in one pair should be parallel and equidistant to each other. Besides, to minimize crosstalk in high-speed interface implementations, the spacing between the signal pairs must be at least 5 times the width of the trace. This is referred to as the 5 W rule [16]. Adding vias between signal pairs is another method to avoid crosstalk. Other rules, such as avoiding sharp corners and keeping constant trace width to avoid impedance mismatches in the transmission lines, are also important.

4. Results and Discussion

Simulation is carried out under different source intensities with 13240 input signals tested, and the results under 300 Ci intensity are shown in Figure 9. A 0.3 V reference voltage is set to eliminate the interference signals. The count loss under 300 Ci intensity (i.e. 3.58×10^6 /s count rate) with 0.3 V V_{ref} is 7.34%. The voltage comparator has good performance with a 4.06 V output high level, a 3.28 V low level, and a swing of only 0.78 V, which are typical values of PECL logic under 5.0 V supply voltage.

As shown in Table 4, the count loss increases as the source intensity rises and the V_{ref} falls. Here are the explanations: First, the pileup effect will be weakened as the source intensity decreases. As displayed in Figure 10, when $V_{\rm ref}$ is below the junction value, two pileup signals under higher intensity will be regarded as one signal (blue curve), leading to one count loss. Second, the two pileup signals can be isolated from one another as the reference voltage rises because it is more likely to exceed the junction value of two pileup signals. When V_{ref} is above the junction value, the two pileup signals can be separated and the counts at high and low intensities are both equal to 2 without any loss. In the simulation test, the measuring errors nearly exclusively result from the endogenous factor caused by the pileup effect, which can be demonstrated by the first two signals in Figure 9. The losses caused by the exogenous factor are, however, rather small and may even be ignored due to the good performance of MAX9602 comparators and the fact that the influence of PCB-level circuits is not taken into consideration in the simulation test. The same interpretation also applies to the fact that the propagation delay does not deviate from a typical value of 0.5 ns.

Figure 11 presents the setup of the first-step laboratory test and the measured waveform. The PECL differential signals are the intermediate output of the voltage comparator. Then, ICS508 converts a pair of PECL differential signals into a CMOS output with a 50% duty cycle regardless of the signal frequency.

Experiments are performed to observe the propagation delay of the circuits for situations with sine input frequencies of 50 MHz, 100 MHz, and 150 MHz under $0.5 \text{ V} V_{\text{ref}}$. We should first note that the propagation delay is defined as the amount of time it takes for a signal to propagate from the

TABLE 3: PECL output structure of MAX9602 at 25°C.

Parameters	Min	Тур	Max	Units
Output high voltage V _{OH}	VCCO1.10	VCCO0.94	VCCO0.75	V
Output low voltage V _{OL}	VCCO1.95	VCCO1.72	VCCO1.55	V



FIGURE 4: DC-coupling between PECL and PECL [13].



FIGURE 5: Simulation results under different VCCO_. The absolute values of high and low levels are controlled by VCCO_, while their difference is always 0.78 V regardless of VCCO_.

comparator input to the output, and the measured output point is where the output reaches 50% of the stable value (see Figure 12(a)). In Figure 12(b), it is observed that the propagation delays are 0.60 ns and 0.80 ns at 50 MHz and 100 MHz, respectively, while the delay is 0.83 ns at 150 MHz input frequency. It is obvious that, with growth in input frequency, the propagation delay increases. Though in the worst case of 150 MHz, the value of delay is 66% larger than the nominal value of 0.5 ns, and it is still a relatively short and acceptable delay.

A further laboratory test is conducted in the environment shown in Figure 13. The intensity of Co-60 is 8.2 Ci at the time of the experiment (100 Ci in November 2002), and the distance between the radioactive source and the detector is about 3 m. Therefore, according to equations (1) and (2), the count rate equals 3.92×10^5 /s in this laboratory test with a 2.38% pileup rate.

In the collected data, output signals from the detector and preamplifier filter circuits are inputs for the comparator module; then, after being compared by MAX9602 and converted by ICS508, output signals are in CMOS logic with a 3.3 V high level. The reference voltage is set to 0.2 V, 0.3 V, and 0.45 V, respectively. For each of the three scenarios with distinct V_{ref} , 15 sets of data with a combined total of more than 10,000 input signals are collected. The sampling time for each set of data is 2 ms (see Figure 14(a)). Different from the simulation test, where the signals with relatively narrow pulse widths can still be recognized as shown in the penultimate signal of Figure 9, signals with pulse width at V_{ref} less than approximately 3 ns (second signal in Figure 14(b)) might be overlooked by the comparator of the PCB-level. Results demonstrate that, at 0.10 V, 0.20 V, and 0.45 V V_{ref} , respectively, the count losses are 3.13%, 4.17%, and 4.98%, which have an opposite trend to simulation results. In the simulation test, errors are primarily driven by the endogenous factor caused by the pileup effect. A lower count loss is obtained as V_{ref} is raised since there is a greater tendency to surpass the junction value. However, in the laboratory test, the influence of the exogenous factor outweighs the endogenous one, especially in the case where the pileup rate is as low as 2.38%. With an increase in V_{ref} , the corresponding pulse width becomes narrow and is more likely to be dropped by the physical comparator circuits.

The parameters and results of the two laboratory tests are summarized in Table 5. As was already noted, the dispersion of the propagation delay from the nominal 0.5 ns cannot be ignored when looking at the PCB-level performance in laboratory tests. In addition, not every pulse with an amplitude greater than $V_{\rm ref}$ can be recognized, particularly when the pulse width above $V_{\rm ref}$ is less than 3 ns. These measuring inaccuracies are introduced by the physical PCBlevel circuits.

The typical specifications given are not production tested or guaranteed. Due to process and fab variations, in addition to normal statistical variations, the typical value can have quite a wide range. There are several factors that influence the specifications, such as the amount of overdrive, the supply voltage, the output driver supply voltage, capacitive loading, and temperature [17]. The expected values of the propagation delay and minimum recognized pulse width can be achieved only when additional DC tests are performed to guarantee that all internal bias conditions are correct. However, these specifications cannot be measured in automatic handling equipment, so corrections will be costly for systems that already meet performance requirements and do not require as much accuracy.

Finally, the designed comparator board is used in practical applications to alleviate the effect of interference signals on radiation images. The sampling time of each pixel is 25 ms, and an FPGA is used to calculate the count. Here, we choose a contrast indicator (CI) model, which is a commonly used indicator in large container inspection to assess the system performance. In the CI model, an iron



FIGURE 6: Thèvenin equivalent transformation of the DC-coupling circuit [13].



FIGURE 7: Schematic diagram of the main comparator circuits (only the connections of one channel are displayed).



FIGURE 8: (a) Schematic of the modular comparator board with four detector channels and the signal flow. (b) Physical diagram of the PCB board.

absorber is placed behind a 100 mm thick iron plate, and there must be a minimum thickness of the absorber that can still be recognized behind the iron plate. CI is defined as the ratio of the minimum value to the thickness of the iron plate (100 mm). The experimental setup and the geometric arrangement of CI are shown in Figure 15, and the results obtained are displayed in Figure 16. Images after setting 0.6 V $V_{\rm ref}$ (second line in Figure 16) have significantly better image quality than the original images in the first line. After setting proper $V_{\rm ref}$ the indicator CI decreases from 1.0% to 0.9% numerically, indicating improved performance. However, the indicator CI of the current-integration systems in use now can only reach around 1.5% under the same settings [18].



FIGURE 9: Simulation results under 300 Ci intensity with 0.3 V reference voltage, where the blue curve represents the input signal and the orange curve represents the digital output signal of PECL logic.

TABLE 4: Simulation results: comparator count loss under different count rates with various V_{ref} .

No-load photon count rate/10 ⁵ s ⁻¹	3.58	5.97	11.9	35.8
Count loss $(V_{ref} = 0.2V)/\%$	1.08	1.96	3.39	9.55
Count loss $(V_{ref} = 0.5V)/\%$	0.39	0.44	1.23	3.18



FIGURE 10: Illustration of count loss under different source intensities with various V_{ref} . The count of the high intensity signals (blue curve) equals 1 under lower V_{ref} causing one count loss and equals 2 under higher V_{ref} , while for the low intensity signals (orange curve), the count is always 2 under these two V_{ref} .



FIGURE 11: Testing setup and the measured waveform.



FIGURE 12: (a) Diagram of propagation delay. (b) Results of propagation delay at input frequencies of 50 MHz, 100 MHz, and 150 MHz ($V_{ref} = 0.5$ V).



FIGURE 13: Laboratory setup: (a) physical environment and (b) schematic diagram.



FIGURE 14: Laboratory test under 0.45 V V_{ref}. (a) oscilloscope display in 2 ms sample time and (b) diagram of one count loss.

Laboratory test 1			Laboratory	test 2	(with radioac	tive source)
Sine input frequency (MHz)	Propagation delay (ns)	System no-load count-rate	Pileup rate (%)	V _{ref} (V)	Count loss (%)	Minimum recognized pulse width
50	0.60			0.20	3.13	
100	0.80	$3.92 \times 10^{5}/s$	2.38	0.30	4.17	~3 ns
150	0.83			0.45	4.98	

TABLE 5: Parameters of two laboratory tests (with and without radioactive source) and the results obtained.

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FIGURE 15: Laboratory test on the CI model: (a) physical setup and (b) geometric arrangement (unit: mm).



FIGURE 16: Results of CI. First line: the original obtained images. Second line: processed images by setting $0.6 \text{ V} V_{\text{ref}}$. The reached optimal performance is circled with a red frame.

5. Conclusions

A nanosecond voltage comparator with PECL logic for the application in a photon-counting γ -ray radiation imaging system was developed and analyzed. With it, we can improve radiation image quality by deleting the interference signals caused by scattered photons and electronic noise. The selection and design of the voltage comparator were focused on the realization of high-speed comparison for four detector channels operated in a photon-counting mode. The comparator module can be easily expanded to multiple channels and is possible to transfer to any massive systems that require comparison and connection with CMOS data acquisition boards.

Factors affecting measurement accuracy are classified as endogenous and exogenous causes, where the pileup characteristic of the signal itself constitutes the endogenous factor and the performance of comparators forms the exogenous factor. In the simulation test, the endogenous factor is the primary cause of the count loss, where the count loss decreases with a lower count rate and higher $V_{\rm ref}$ to overcome the pileup effect. The performance of the voltage comparator has little impact on the count loss in simulation; meanwhile, the propagation delay is constant at a nominal value of 0.5 ns. Laboratory testing on the PCB-level system, however, reveals that signals with pulse widths of less than 3 ns might be overlooked by the comparator and that the propagation delay expands to 0.83 ns at 150 MHz. Despite the errors, they are still acceptable and can satisfy the needs of practical applications, which have been proved with the CI model. The CI performance can be improved from 1.0% to 0.9% by properly setting proper $V_{\rm ref}$ with comparators.

To achieve accurate nominal values given by the datasheet, DC tests should be performed on internal bias conditions, which are costly. But efforts can be made to approach the expected value and achieve better performance. For instance, follow-up studies on better planning PCB layout, optimizing power supply strategy and lowering the amount of overdrive can be conducted to reduce the dispersion of performance indicators. In addition, further experiments under higher source intensity should be carried out.

Data Availability

The data used to support the findings of this study are included in the article.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this article.

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