Review Article

Overview on Radiation Damage Effects and Protection Techniques in Microelectronic Devices

Yanru Ren [ID],[1] **Min Zhu** [ID],[1] **Dongyu Xu** [ID],[1,2] **Minghui Liu,**[1] **Xuehui Dai** [ID],[1] **Shengao Wang** [ID],[1] **and Longxian Li** [ID][1]

[1]*Naval University of Engineering, Wuhan 430033, China*
[2]*PLA Unit 91049, Sanya 572000, China*

Correspondence should be addressed to Dongyu Xu; 1375708337@qq.com

With the rapid advancement of information technology, microelectronic devices have found widespread applications in critical sectors such as nuclear power plants, aerospace equipment, and satellites. However, these devices are frequently exposed to diverse radiation environments, presenting significant challenges in mitigating radiation-induced damage. Hence, this review aims to delve into the intricate damage mechanisms of microelectronic devices within various radiation environments and highlight the latest advancements in radiation-hardening techniques. The ultimate goal is to bolster the reliability and stability of these devices under extreme conditions. The review initiates by outlining the spectrum of radiation environments that microelectronic devices may confront, encompassing space radiation, nuclear explosion radiation, laboratory radiation, and process radiation. It also delineates the potential damage types that these environments can inflict upon microelectronic devices. Furthermore, the review elaborates on the underlying mechanisms through which different radiation environments impact the performance of microelectronic devices, which includes a detailed analysis of the characteristics and fundamental mechanisms of damage when microelectronic devices are subjected to total ionizing dose effects and single-event effects. In addition, the review delves into the promising application prospects of several key radiation-hardening techniques for enhancing the radiation tolerance of microelectronic devices.

1. Introduction

The reliability and stability of microelectronic devices in high-energy radiation environments have always been a widely studied area of interest. With the development and expanding application range of modern electronic devices, the impact of radiation damage effects on device performance has become increasingly significant [1]. Understanding and addressing these radiation damage effects is crucial for ensuring the long-term reliability of electronic devices [2].

Microelectronic devices can experience various damage effects when exposed to high-radiation environments, including ionizing radiation and neutron radiation. The severity of these damage effects depends on multiple factors, including the type of radiation, its energy, and its flux. For

neutron radiation, the neutron flux and the energy of the radiation are crucial for the impact on microelectronic devices. For example, when the neutron flux reaches 10^6 to 10^{10} n/cm^2/s and the radiation energy is within a few MeV to several tens of MeV, microelectronic devices may suffer from displacement damage and charge accumulation damage. Furthermore, gamma rays also significantly damage microelectronic devices, especially when the energy of gamma rays ranges from several hundred keV to a few MeV. Gamma rays within this energy range can penetrate deep into microelectronic devices, inducing the generation of electron-hole pairs, thereby leading to charge accumulation damage. When the energy of gamma rays exceeds 1 MeV, their penetrating ability further increases, not only generating secondary electrons in semiconductor materials but also possibly causing atomic displacements, leading to more

severe lattice damage. These damages ultimately result in the degradation of device performance, such as reduced speed, increased power consumption, or functional failure. These effects include the formation and accumulation of electron traps, dielectric breakdown, carrier trapping and injection, and the formation of crystal structure defects, among others. These effects not only lead to severe degradation of device performance but also impact the overall reliability of electronic systems, thereby limiting the application of electronic devices in fields such as nuclear energy and aerospace [3]. To mitigate these effects, researchers have made progress in developing protection techniques such as material improvement, structural optimization, and radiation resistance testing [4]. These approaches involve selecting and optimizing materials, designing device structures to minimize radiation impact, and evaluating device performance in radiation environments. By employing these techniques, the radiation resistance and reliability of microelectronic devices can be enhanced.

With the continuous reduction in the size of electronic devices and the lowering of operating voltages, as well as the introduction of new materials and device structures, the study of radiation damage effects in microelectronics faces new challenges and opportunities. For example, at the nanoscale, device structures and interface characteristics can result in radiation damage behaviors that differ from those observed in traditional devices [5]. In addition, the introduction of new materials may bring about more complex radiation responses in electronic devices. In order to ensure the reliability of these complex devices in high-radiation, aerospace, and terrestrial environments, further research and understanding of their radiation response behaviors are required [6]. For instance, in aerospace environments, devices might be exposed to radiation levels ranging from tens of krad (Si) to several hundred krad (Si), while in terrestrial high-radiation environments, such as near nuclear reactors or in certain medical applications, the exposure can vary significantly, potentially reaching up to several MGy (Si).

First, total ionizing dose (TID) effects involve phenomena such as oxide layer damage, increased interface state density, and reduced carrier mobility caused by long-term cumulative irradiation [7]. These changes can lead to parameter drift in devices or even functional failure. Secondly, displacement damage is caused by high-energy particles directly colliding with lattice atoms, causing atomic displacement and defect generation, which impacts the electrical properties of materials. Lastly, single-event effects (SEE) describe transient current pulses produced by the interaction of individual high-energy particles with microelectronic devices, which may result in data errors, logic flips, and even permanent device damage. When high-energy particles, such as protons and heavy ions in cosmic rays, penetrate microelectronic devices, they can generate charge collection in semiconductor materials, leading to transient current pulses [8]. This phenomenon can cause device malfunctions, such as bit flips (single-event upset, SEU), threshold voltage shifts, and even device damage. Rocket launch missions and on-orbit satellites must consider the impact of radiation environments on microelectronic

devices. When exposed to radiation for a long time, microelectronic devices accumulate absorbed doses, leading to device performance degradation, such as changes in threshold voltage, reduction in carrier mobility, and damage to oxide layers. This effect is crucial for space missions because of the radiation in space environments [9]. Various space exploration missions conducted by NASA often need to consider the TID effect on scientific instruments and communication systems.

In current microelectronic device design, enhancing stability and reliability in extreme radiation environments has become a major challenge faced by the scientific research and industrial sectors. This article aims to explore and analyze the primary issues encountered by microelectronic devices in radiation environments and propose corresponding response strategies and improvement measures based on the latest research findings. Through an in-depth study of the impact of radiation effects on the performance of microelectronic devices, we hope to provide guidance for future device design to ensure their stable operation in extreme environments.

2. Irradiation Environment

The radiation damage to semiconductor circuits and devices is mainly influenced by the radiation environment. These radiation sources can come from external sources such as solar radiation or terrestrial radiation or from internal sources such as radiation from nuclear energy equipment, particle accelerators, X-ray devices, and equipment for radioisotope applications. In addition, the sensitivity of semiconductor circuits and devices to radiation varies depending on different operating states. In switch states, high-frequency operation, or high-power operation, circuits may become more sensitive to radiation. Different types of circuits and devices also have varying levels of resistance to radiation interference. The damage to devices from radiation exposure is primarily related to four types of radiation environments: space radiation, nuclear explosion radiation, laboratory radiation, and process radiation.

Galactic cosmic rays, solar event particles, and the Van Allen radiation belts are the main sources of radiation effects on semiconductor devices in space environments [10]. Galactic cosmic rays are high-energy particle streams originating from outside the milky way galaxy. They are generated by cosmic ray acceleration and events such as supernova explosions. These high-energy particles enter the space near Earth and can affect semiconductor devices, causing phenomena like discharge and single-event upsets. Solar event particles are caused by solar activities, including solar flares and charged particles from the solar wind. These charged particles propagate near Earth through the solar wind and can cause temporary or permanent malfunctions in semiconductor devices. The Van Allen radiation belts are belt-shaped regions composed of high-energy charged particles captured by the Earth's magnetic field. They can potentially cause damage to spacecraft and satellites, especially devices operating in low Earth orbit. The space radiation environment in the vicinity of Earth consists of three

different radiation components: trapped particles in the Van Allen belts (protons and electrons), solar particles (protons, electrons, and ions), and galactic cosmic rays (high-energy ions and protons). These are illustrated in Figure 1.

The man-made nuclear radiation environment is mainly composed of neutrons, radioactive particles, gamma rays, and X-rays. The damage of these radiation elements to semiconductor materials mainly comes from the effects of fast neutrons, gamma rays, and X-rays [12]. When the photocurrent generated by radiation enters the device, it may cause changes in the state of timing circuits, flip the information in memory, even trigger incorrect logic signals, or damage the device.

The laboratory radiation environment simulates the radiation effects in space and nuclear explosion environments using devices. In the laboratory, radiation simulators or accelerators can be used to simulate the radiation effects in space and nuclear explosion environments. These devices can generate particle beams or electromagnetic radiation similar to space radiation or nuclear radiation to perform radiation testing on circuits and devices. By simulating space radiation, the behavior of semiconductor circuits and devices in space can be studied, and the reliability and radiation resistance of electronic equipment such as spacecraft and satellites in high-radiation environments can be understood. In addition, simulating the radiation effects of a nuclear explosion environment can be used to study nuclear emergency response and protective measures. By testing the performance of circuits and devices under high-energy particle radiation, their ability to cope with nuclear explosion scenarios can be evaluated, guiding the safety design and protection strategies in fields such as nuclear power plants and nuclear weapon systems. Typically, ^{60}Co gamma radiation sources with energies of 1.17 MeV and 1.33 MeV are used to simulate total dose effects, and proton accelerators can be used to simulate displacement damage effects and assess the risk of radiation damage to devices in orbit.

Some steps in semiconductor manufacturing processes need to be carried out in a radiation environment. For example, ion implantation is used during the doping process to alter the characteristics of the material, and the use of electron beams or X-rays during the etching and lithography processes can cause radiation damage to the devices. These processes can result in varying degrees of radiation damage to the devices.

In the space environment, semiconductor devices are typically subjected to various types of radiation simultaneously, including

(1) Ionizing radiation: It mainly consists of high-energy charged particles such as protons and electrons. When these charged particles pass through semiconductor devices, they interact with the atoms and electrons in the devices, causing scattering and ionization interactions, resulting in energy deposition and ionizing damage.

(2) Neutron radiation: Neutrons are neutral particles that can be produced through nuclear reactions. When neutrons pass through semiconductor
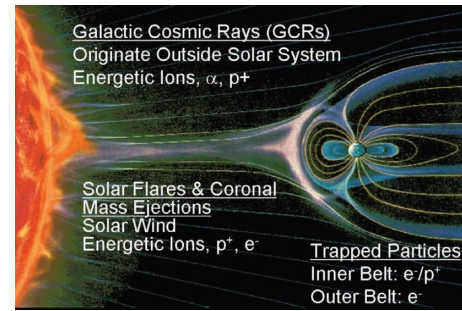

Figure 1: Space radiation environment [11].

devices, they interact with atomic nuclei and displace them, causing displacement damage.

(3) Photon radiation: It mainly refers to gamma rays or X-ray radiation. When these high-energy photons pass through semiconductor devices, they interact with electrons, causing changes in electron energy levels and electron damage.

The radiation effects of these particles can lead to different types of radiation damage in semiconductor devices, including ionizing damage and displacement damage [13]. Table 1 lists several types of particles in radiation environments, their radiation effects on semiconductor devices, and corresponding ground irradiation test simulation devices.

In recent years, researchers have conducted extensive studies on the radiation damage effects of microelectronics and achieved significant results. Through laboratory testing, numerical simulations, and theoretical derivations, the fundamental mechanisms and behavioral patterns of these effects have been explored in depth. Valuable experiences and data have been accumulated through numerous application cases in practical environments, further enhancing our understanding of radiation damage effects in microelectronics. Figure 2 illustrates the interaction relationship between nuclear radiation and space radiation.

3. Research Progress of Radiation Damage Mechanism

3.1. Total Ionizing Dose Effects

3.1.1. Degradation Mechanisms of Total Ionizing Dose Effects. The Total Ionizing Dose (TID) effect refers to the impact on devices after prolonged exposure to radiation environments. When devices are subjected to ionizing radiation, electrons and positrons generate ion pairs and electron-hole pairs within the device. These ion pairs and electron-hole pairs cause energy deposition in the semiconductor lattice, leading to the formation of oxide charges and interface traps. The accumulation of these oxide charges and interface traps gradually alters device parameters, such as threshold voltage drift, reduced transconductance, and increased leakage current. These changes can significantly affect both the static and dynamic characteristics of the device, potentially leading to functional failure. Therefore, when designing and

TABLE 1: Radiation environment, radiation particles, radiation effects and test simulators [14].

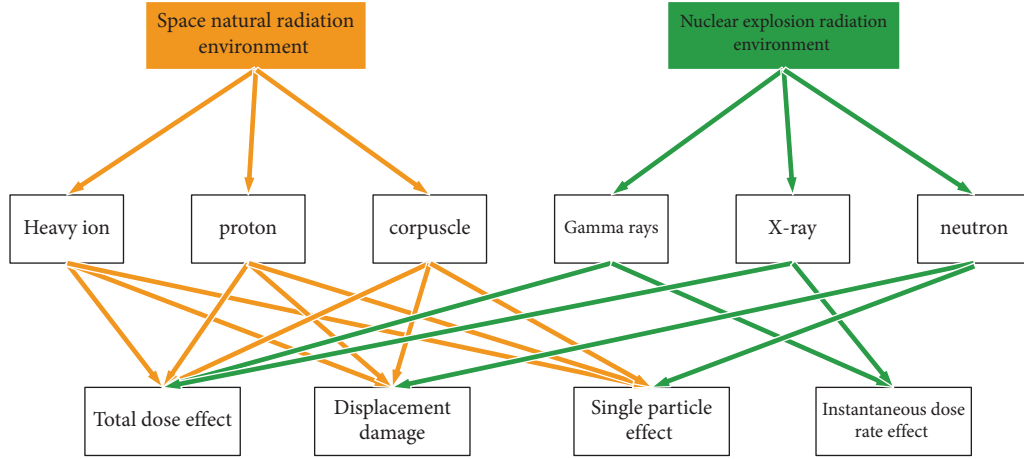| Radiation environment	Radiation particle	Failure mechanism	Test simulation mechanism
Space environment	10 Mev~100 Mev electrons, protons	Total dose effect	^{60}Co-γ Low energy X-ray device
	100 Mev~several GeV electrons, protons	Single particle effect	Cyclotron
Nuclear explosion	Tens to hundreds of grays	Total dose effect	^{60}Co-γ Low energy X-ray device
	100 keV~several MeV neutron flux	Displacement damage Single particle effect	Nuclear reactor
Reactor	Steady state neutron flux	Displacement damage	Nuclear reactor
	Several MeV gamma rays	Total dose effect	^{60}Co-γ Low energy X-ray device

FIGURE 2: The relationship between radiation effects and radiation environment [15].

manufacturing devices intended for use in radiation environments, it is crucial to thoroughly consider and mitigate the effects of TID on device performance and reliability.

The unit of total dose is rad (Si), defined in the CGS (Centimeter-Gram-Second) system as the radiation energy deposition of 100 ergs (1 erg = 10^{-7} J) per gram of silicon. The generation of electron-hole pairs is typically caused by excitations in the energy band. In semiconductor materials, when a high-energy particle such as a photon or a charged particle enters the material, it can interact with the atoms or ions in the material, transferring energy to them. If the transferred energy is large enough to overcome the bandgap, an electron-hole pair is created. The number of generated electron-hole pairs is related to the energy absorbed per unit volume (dw) in the material [16].

$$\frac{dN}{dv} = \frac{dP}{dv} = \frac{1}{w}\frac{dw}{dv}, \tag{1}$$

where N represents the number of electron-hole pairs. The relationship between effective energy, dose, and the number of electron-hole pairs can be expressed by the following equation [17]:

$$\frac{dN}{dv} = \frac{dP}{dv} = \frac{m_v}{w}D. \tag{2}$$

For silicon material, 1 rad (Si) generates 4×10^{13}/cm^3 electron-hole pairs, while for silicon dioxide (SiO$_2$) material, it produces 7.6×10^{12}/cm^3 pairs.

For semiconductor devices, the failure caused by the total dose effect is mainly due to the generation of oxide trap charges and interface trap charges in the device's gate oxide layer after the high-energy particles' impact. When high-energy particles penetrate the gate oxide layer of a semiconductor device, they may interact with the oxide and semiconductor materials, leading to the following steps: (1) Generation of electron-hole pairs: High-energy particles penetrating the oxide layer will generate electron-hole pairs, which form in the oxide layer due to energy deposition. (2) Hole transport: After the generation of electron-hole pairs, holes can be transported through the oxide layer. Hole transport can occur through processes such as oxygen vacancies and ion migration within the oxide layer. (3) Formation of oxide trap charges: In the oxide layer, some defects or other impurity sites may act as traps, capable of capturing and storing electrons or holes. When holes move to these trap sites, the traps capture the holes and form oxide trap charges. (4) Formation of interface trap charges: At the interface between the oxide layer and the semiconductor material, there may also exist some defect sites. When electrons or holes move to these interface trap sites, interface

trap charges are formed by capturing electrons or holes. The physical processes of radiation-induced oxide trap charges and interface states are shown in Figure 3.

The free charges generated under radiation will diffuse into and be trapped in the gate oxide layer, resulting in an increase in the oxide charge in the gate oxide layer. Therefore, in the gate oxide layer, the radiation-induced oxide charge Q_{ox} is directly proportional to the thickness of the oxide layer t_{ox}, as $N_{TH} = -Q_{ox}t_{ox}/\varepsilon_{ox}$, and $\varepsilon_{ox} = C_{ox}/t_{ox}$. As a result, the drift of the threshold voltage ΔV_{TH} is proportional to t_{ox}, and the relationship between the drift of the threshold voltage ΔV_{TH} and the radiation dose D can be expressed as follows [19]:

$$\Delta V_{TH} = -\alpha \frac{q m_v}{\omega \varepsilon_{ox}} t_{ox}^2 D. \tag{3}$$

In the equation, the capture factor α is used to indicate that only a small fraction of charges are captured in the oxide layer. For regular nonhardened oxide layers, it is approximately 0.15, while for radiation-hardened oxide layers, it is approximately 0.05. m_v represents the oxide material density, and ω is the energy required to create an electron-hole pair in the oxide layer, which is 18 eV.

3.1.2. Research Status of Total Ionizing Dose Effects.

Research on total dose radiation effects in electronic devices has a history spanning over 60 years. One of the earliest instances of device failure caused by total dose effects was the failure of the circuitry in the Telstar I communication satellite in 1962. A nuclear test at that time triggered an enhancement of ionization in the Earth's radiation belts, leading to total dose effects in bipolar transistors and resulting in their failure [20].

In the early 1990s, with the widespread application of silicon-on-insulator (SOI) devices, research on the total dose effects of SOI devices gradually expanded. As device feature sizes decreased, the gate oxide layer became thinner, resulting in reduced total dose effects caused by the gate oxide. In contrast, the irradiation effects on the the irradiation effects on the buried oxide (BOX) layer became the main influencing factor. Studies have found a significant relationship between the irradiation effects on the BOX layer in SOI devices and the fabrication process [21].

The radiation model for SOI devices was first proposed by Petrosjanc et al. in 1994 [22]. This model, targeting large-sized SOI devices, considers the threshold voltage drift and parasitic bipolar transistor effects caused by irradiation. Subsequently, Petrosjanc's research group further developed the BSIMRAD model based on the BSIMSOI model and the EKV-SOI radiation model based on surface potential. These models utilize commercial models such as BSIM and EKV, allowing for easy parameter extraction using commercial parameter extraction tools. The equivalent circuit of the macromodel is presented in Figure 4.

In 2011, the Sanchez Esqueda research group at Arizona State University established a model that includes radiation-induced parasitic transistor parameters and leakage current for shallow trench isolation oxide in 0.18 μm and 90 nm bulk

silicon CMOS devices [24]. They studied the effects of total ionizing dose on the characteristics of field oxide field-effect transistors (FOXFETs) manufactured using low-standby-power commercial bulk CMOS technology. Shown in Figure 5 is the cross-sectional diagram of the NW FOXFET device used in this study. The leakage path that is shown in Figure 5 is associated with the defect buildup along the base of the STI oxide and is referred to as an interdevice leakage path that occurs between n-wells or adjacent p-channel devices. Plots of the $I_d - V_{gs}$ response preirradiation and after several levels of TID are shown in Figure 6 for a device with $L = 0.9$ um and 1.5 um using a drain bias of $V_d = 0.1$ V and $V_d = 1$ V. The devices under test were irradiated in a ^{60}Co gamma irradiation chamber at a dose rate of approximately 20 rad (SiO$_2$)/sec. Electrical measurements ($I_d - V_{gs}$ characteristics) were obtained prior to irradiation and after step-stress irradiations up to 20 krad (SiO$_2$), 100 krad (SiO$_2$), 200 krad (SiO$_2$), and 1 Mrad (SiO$_2$). The electrical measurements consisted of obtaining drain current (I_d) vs. gate-to-source voltage (V_{gs}) characteristics for drain biases of $V_d = 100$ mV and $V_d = 1$ V. The experimental verification is obtained through the incorporation of the analytical models with closed-form expressions for ψ_s and I_d resulting in an accurate description of the degraded $I_d - V_{gs}$ characteristics.

In 2015, the Sanchez Esqueda research group developed a model for FDSOI devices based on the influence of oxide trap charges and interface trap charges on surface potential [25]. This model incorporates the effects of total dose irradiation and stress-induced defects into the simulation of metal-oxide semiconductor devices and integrated circuits. The modeling approach was validated on MOS devices. Through TCAD simulations and comparison with the experimental characteristics of irradiated devices, the accuracy of the formulas was verified. The schematic cross-section of an SOI MOSFET, as shown in Figure 7, illustrates the accumulation of oxide trap charges and the generation of interface traps induced by radiation.

In 2010, Jagannathan's team at Vanderbilt University modeled the total dose radiation effects on operational amplifiers (op-amps) by directly establishing macro models [26]. They developed a behavioral model for the LM124 op-amp, capturing the total ionizing radiation dose characteristics of important macroscopic circuit behaviors with high accuracy. In 2010, Vanderbilt University collaborated with Accelicon Technologies to develop a total dose model process design kit (PDK) based on the 90 nm bulk silicon technology [27]. This model can capture the technology-dependent total ionizing dose (TID) response variations. The model describes an automated process for utilizing new test chips, modeling, and simulation to generate a TID-aware process design toolkit. Figure 8 shows a comparison of the characteristics of 90 nm CMOS devices before and after irradiation, comparing the calibrated I–V curve with the average measured curve. Measurements and irradiations were carried out at Vanderbilt University. During the measurements, the drain was biased at V_{dd} 1.2 V. Irradiation was performed at room temperature up to a TID of 300 krad (SiO$_2$) at a dose rate of 31.5 krad (SiO$_2$)/min using an
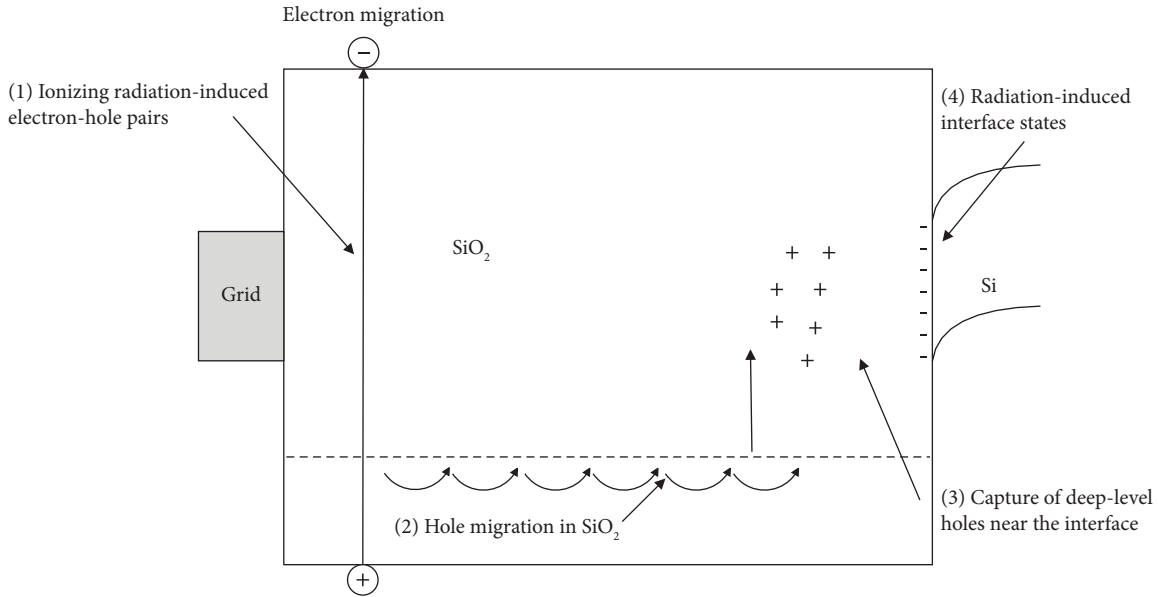
Figure 3: Physical processes of charge and interface states in radiation-sensing oxide traps [18].
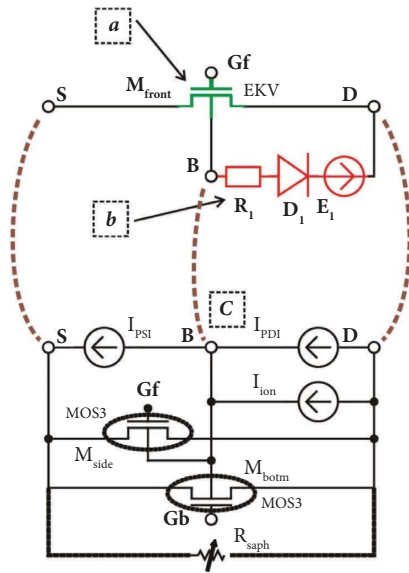

Figure 4: The equivalent circuit of the macromodel [23].

Figure 5: Cross-sectional diagram of n-well-to-n-well (NW) FOXFET [24].

ARACOR 10-keV X-ray irradiation source. Based on Figure 8, it can be observed that the drain current increases with the increase in radiation dose on the device, and the simulation results match well with the experimental results.

China's research on total dose effects began in the 1970s and has primarily focused on engineering applications. In the context of reinforcing integrated circuits against total dose effects, researchers have proposed various approaches from the perspectives of process and device structure. In 2001, Wan Xinheng and others from Peking University's Institute of Microelectronics developed a total dose-effect irradiation model that automatically incorporates bulk depletion conditions, eliminating the need to separate devices into different types [28]. They also conducted simulations on
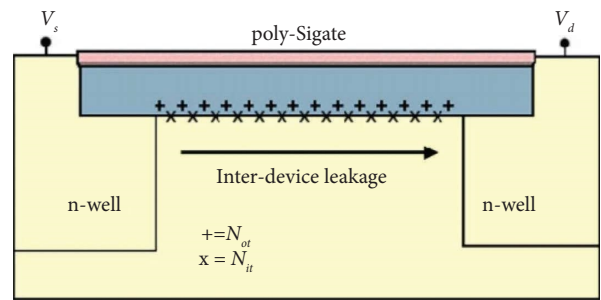
SOI devices using SIMOX technology. Furthermore, Bu Jianhui and colleagues from the Institute of Microelectronics at the Chinese Academy of Sciences developed a total dose BSIM model that takes into account threshold voltage, mobility, and leakage current variations under different bulk biases [29]. This model exhibits good agreement with experimental data. However, due to factors such as limited domestic fabrication capabilities and imperfect testing conditions, China's research on radiation-hardening technology still lags behind its foreign counterparts, particularly in the area of irradiated device modeling.

In response to the problem that traditional empirical radiation fault diagnosis methods are unable to meet the increasingly diverse demands for integrated circuit fault identification and classification, domestic scholars have utilized neural networks to model and predict device radiation damage. In 2020, Liu and others from Xi'an University of Electronic Science and Technology conducted research on the effects of device radiation using behavior-level modeling based on artificial neural networks [30]. They simplified the model to establish equivalent parameter models for radiation-affected devices and verified the
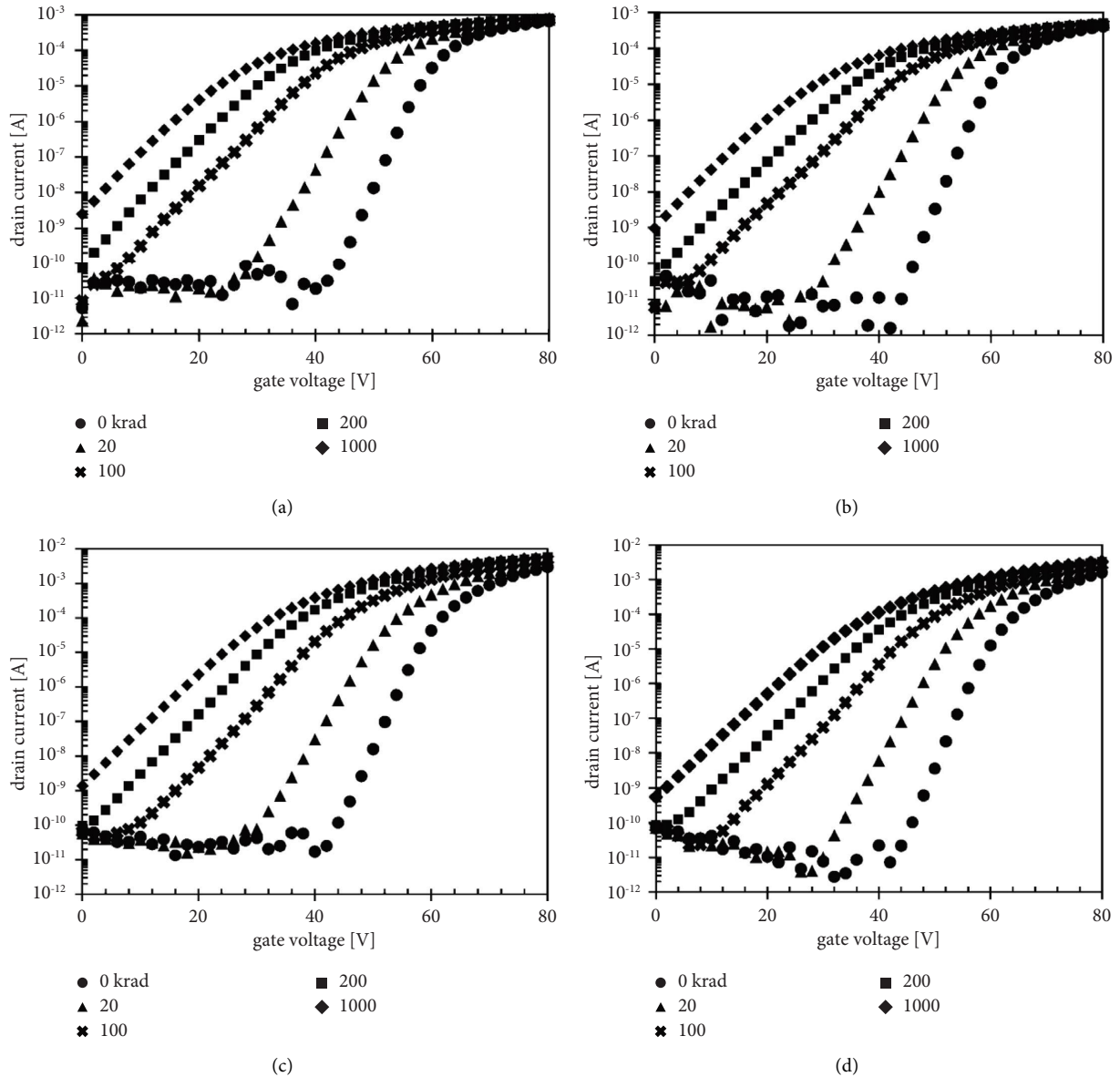
FIGURE 6: $I_d - V_{gs}$ characteristics before irradiation and after 20, 100, 200 and 1000 krad (SiO$_2$) of TID for device [24]. (a) $W = 200$ um, $L = 0.9$ um, $V_d = 0.1$ V, $V_s = V_b = 0$V. (b) $W = 200$ um, $L = 1.5$ um, $V_d = 0.1$ V, $V_s = V_b = 0$ V. (c) $W = 200$ um, $L = 0.9$ um, $V_d = 1$ V, $V_s = V_b = 0$ V. (d) $W = 200$ um, $L = 1.5$ um, $V_d = 1$ V, $V_s = V_b = 0$ V.
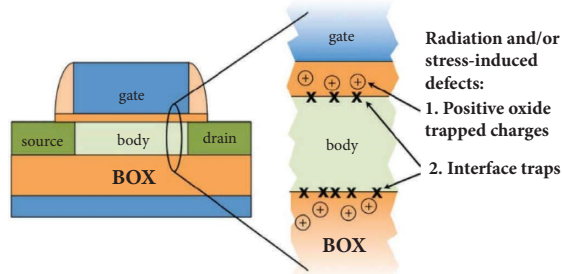

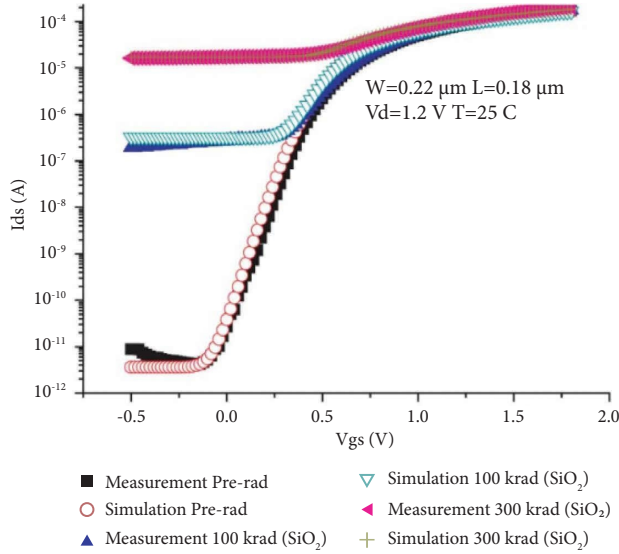FIGURE 7: Schematic cross section of SOI MOSFET [25].

FIGURE 8: Comparison of simulated (with HSPICE) and measured $I_d - V_g$ characteristics before and after irradiation for a 90 nm CMOS device [27].

accuracy of the model by comparing it with measured data. The experiment selected high-power devices of type CS3910S and fitted the transfer characteristic curves of devices 1 and 2. The predicted transfer characteristic curves within the specified range are shown in Figure 9. Experimental requirements for normal conditions are as follows: (1) Radiation environment: normal. (2) Temperature environment: room temperature. (3) Experimental location: Xinjiang Institute of Physics and Chemistry. (4) Device requirements: independently package the bare die devices to prevent oxidation and reinforce the soldering of device pins. (5) Termination condition: When Vs reaches 5 V. (6) Experimental equipment: BC3193 semiconductor discrete device test system, 4200 semiconductor analyzer. (7) Experimental procedure: Select two sets of devices as comparison groups. For each group, fix Vs and measure the transfer characteristics curve from 0 to 5 V with a step size of 0.1 V. The measurement group will also fix Vs with a step size of 0.1 and measure from 0 to 5 V. Under normal conditions, fit the transfer characteristics curves of device 1 and device 2, with drain-source voltage V_{ds} values at 0.1 V, 1.1 V, 2.5 V, 3.5 V, and 4.5 V, as shown in Figures 9(a) and 9(b). To ensure the practicality of the model, provide the transfer characteristics curves of device 1 and device 2 within the range of Vs values from 0.1 V to 2 V, as depicted in Figures 9(c) and 9(d). The fitting results demonstrate a good match, indicating that this model possesses excellent extrapolation capabilities and high accuracy.

In 2022, Yang from Harbin Institute of Technology designed a comprehensive diagnostic system for single radiation faults and coupled radiation faults using a one-dimensional convolutional neural network [31]. The neural network was used for classification, achieving a high accuracy rate of 92.6%. This successfully achieved the goal of integrated circuit fault classification and prediction.

3.2. Space Single-Particle Effect

3.2.1. Degradation Mechanisms of Single-Particle Effects in Space. The single-event effect (SEE) in space refers to the occurrence of a pulse current generated by the collection of electron-hole pairs produced by the ionization of a single particle when it passes through the sensitive region of a device. This pulse current can potentially alter the voltage, current, or charge distribution of the device, leading to soft errors or hard errors [32]. Soft errors caused by single-event effects primarily include single-event upset (SEU), single-event multibit flip (MBU), and single-event transient (SET). Hard errors caused by single-event effects primarily include single-event burnouts (SEB), single-event latche (SEL), and single-event gate rupture (SEGR) [33]. These effects can result in issues such as memory bit flips, logic circuit reversals, and switch failures, thereby impacting the reliability and performance of the device. Table 2 provides a classification and definition of single-event effect failures.

To protect against space single-particle effects, RF, analog, and digital integrated circuits are typically designed and manufactured with a series of radiation-resistant measures. These measures include using radiation-hardened materials, introducing redundant checks and error-correcting codes, and adding electromagnetic shielding, among others, to enhance the radiation resistance of the devices and reduce the impact of space single-particle effects on them [35].

Power devices mainly focus on two single-particle effects: single-particle burnout and single-particle gate rupture [36]. The main factors affecting these effects include the linear energy transfer (LET) value, bias voltage, and incident angle. Particles that can cause single-particle effects include protons, neutrons, and heavy ions [37]. Neutron irradiation can cause functional failure of commercial-grade SiC MOSFET power devices, mainly due to device failure caused by substrate ionization recoil [38]. According to results from heavy ion and proton radiation experiments, ion irradiation with high LET values can cause permanent damage to the devices, including increased gate and source leakage current. LET represents the energy lost by high-energy particles normalized to the density of the incident device material along the unit ionization path length. The definition of LET is as follows:

$$\text{LET} = -\frac{1}{\rho}\frac{dE}{dx}. \tag{4}$$

Among them, ρ represents the density of the incident material. In silicon material, the energy required for an outer electron to escape from the silicon atomic nucleus and form a free electron is called the ionization energy of Si $E_{si} = 3.6 eV/pair$. Therefore, the number of electrons and holes generated by incident particles per unit path length is given by the equation.

$$\frac{dN_e}{dx} = \frac{dN_h}{dx} = \frac{1}{E_{si}}\frac{dE}{dx} = \text{LET} \cdot \frac{\rho}{3.6 eV}, \tag{5}$$
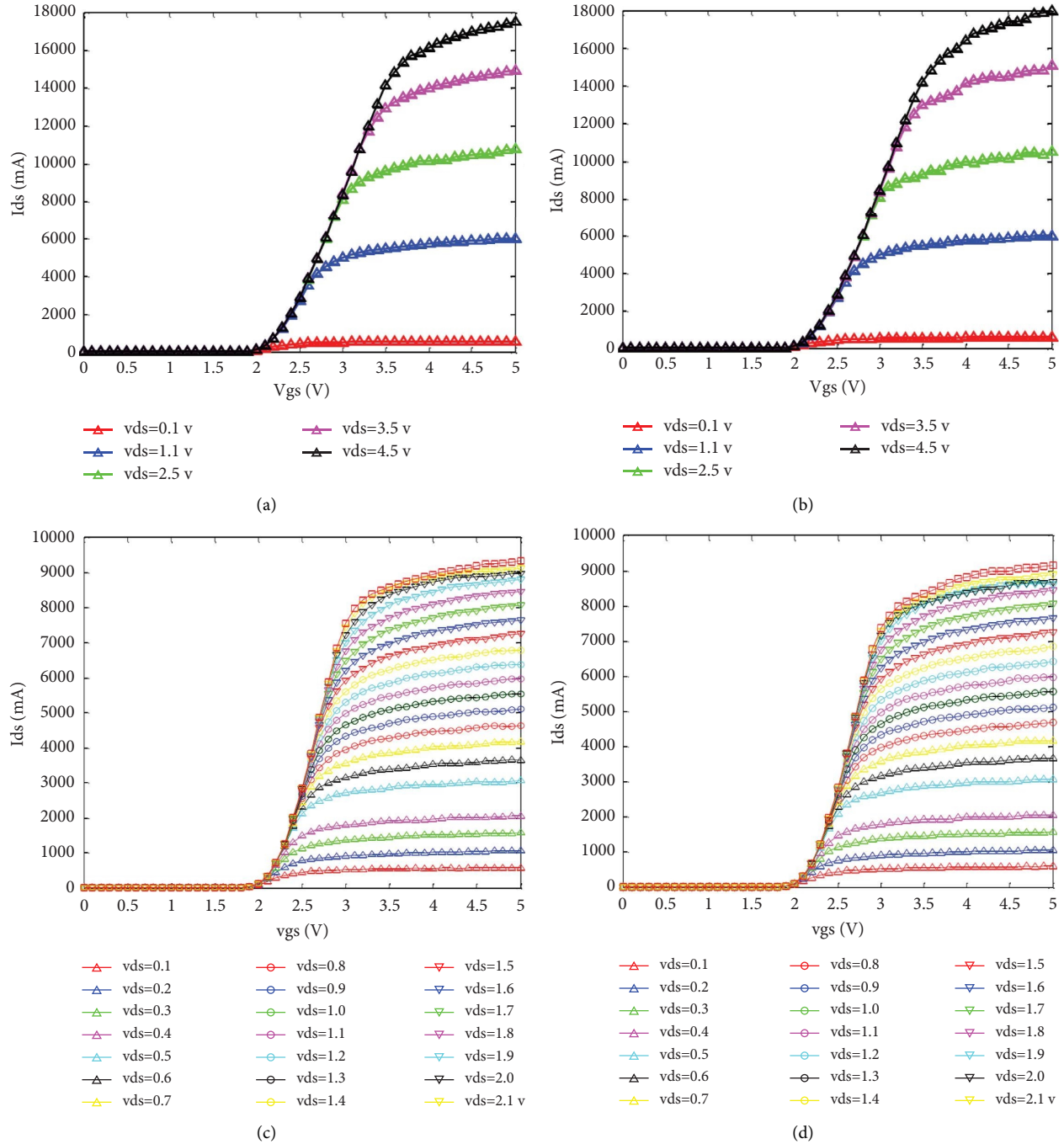
FIGURE 9: Transfer characteristics curves and predicted transfer characteristics curves of devices 1 and 2 [30] (a) Transfer characteristic curve of device 1. (b) Transfer characteristic curve of device 2. (c) Predicted transfer characteristic curve of device 1. (d) Predicted transfer characteristic curve of device 2.

where N_e and N_h represent the number of electrons and holes generated by ionization. pC/um is another unit for linear energy transfer (LET) used in computer numerical simulations in the field of radiation. The conversion relationship between the two units is as follows:

$$\frac{1pC}{\text{um}} = 96.608 MeV \cdot \frac{cm^2}{mg}. \tag{6}$$

3.2.2. The Current Status of Research on Single-Particle Effects in Space. In 1987, Oberg and Wert first used nondestructive single-particle testing methods to study the SEB (single-event burnout) cross-section of power MOSFETs and proposed the concepts of nondestructive single-particle testing and single-particle cross-section [39]. Addressing the challenges of single-particle radiation testing, such as difficulty, long duration, and high cost, Hohl and Galloway

TABLE 2: Classification and definition of single-particle effect [34].

Mistake	Type	Definition
Soft error	Single event upset	Change of logical state in storage units
	Single event multibit flip	Bit storage state change
	Single event disturbances	Transient change in storage unit
	Single event transient	Transient voltage change caused by current
Hard error	Single event latch	Regenerative state of high current in PN structure
	Single event burnout	High current leads to device burnout
	Single event gate rupture	The gate dielectric breaks down due to the large current flowing through it
	Single-event displacement damage	Permanent damage caused by displacement effect
	Single event functional interrupt	Control component malfunction caused by flipping
	Single bit error	Errors that occur in a single bit and cannot be corrected or recovered

proposed the first power MOSFET single-particle burnout analysis model [40] in the second year of SEB effect reporting.

In 2006, Zhang and colleagues conducted research on the failure mechanisms of SiC MOSFET power devices and found that SiC has certain advantages over Si in terms of resistance to single-particle burnout [41]. Devanathan and others studied the main damage states and statistical defects in the cascade displacement of SiC under irradiation effects through modified Tersoff electron potential molecular dynamics simulations [42].

In 2010, Lee et al. conducted a study on high-energy heavy-ion-induced single-event burnout (SEB) in 6H-SiC MOSFETs using TCAD (technology computer-aided design) and simulated the dynamic response of charge carriers caused by these heavy-ion collisions [43]. The TCAD simulation revealed the parasitic bipolar junction transistor (BJT) turn-on mechanism, which drives carrier avalanche and leads to uncontrolled drain current, resulting in SEB occurrence.

In 2018, Witulski et al. investigated heavy-ion-induced single-event burnout (SEB) in high-voltage silicon carbide power MOSFETs [44]. Experimental data for 1200 V SiC power MOSFETs show a significant decrease in SEB onset voltage for particle LETs greater than 10 MeV-cm^2/mg, above which the SEB threshold voltage is nearly constant at half of the rated maximum operating voltage for these devices. TCAD simulations show a parasitic BJT turn-on mechanism, which drives the avalanching of carriers and leads to runaway drain current, resulting in SEB. Figure 10 shows the simulated time variation of the heavy-ion-induced drain current, with a linear energy transfer (LET) of 10 MeV-cm^2/mg, calculated under drain biases of 700 V and 800 V. TCAD heavy-ion simulations of SiC power MOSFET, showing SEB at 800 V at LET = 5 MeV-cm^2/mg with the impact ionization model turned on during TCAD simulation and device recovery at other conditions. The runaway drain current at 800 V with the SiC impact ionization model turned on indicates that SEB has occurred, whereas the device recovers with impact ionization turned off, or if the device is biased at 700 V.

In 2012, Abbate and colleagues conducted single-event effect experiments on commercial 1200 V/20 A SiC MOS-FET power devices using Br ions and I ions at the INFN accelerator [45]. The experimental results, as shown in Figure 11, indicate that as the VDS bias voltage increases, the
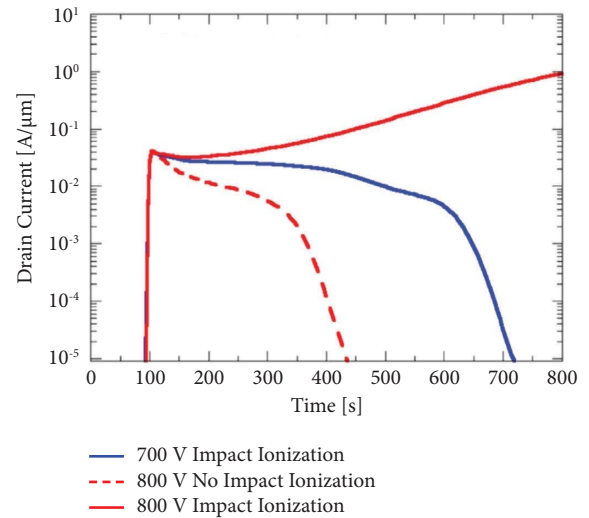

FIGURE 10: TCAD simulations of heavy-ion effects on SiC power MOSFET [44].

average charge quantity exhibits a significant increase. Furthermore, with higher energy of irradiation particles, the growth of the charge quantity becomes more pronounced.

In 2014, Mizuta et al. observed the occurrence of single-event burnout in SiC MOSFET power devices under heavy-ion and proton irradiation conditions through experiments [46]. Mizuta and colleagues conducted single-event burnout effect experiments on commercial 1200 V SiC MOSFET power devices using Kr ions. During the irradiation process, the drain-source voltage (VDS) was increased in increments of 50 V while the gate voltage remained in the off state. By detecting the drain current, they obtained the charge collection information of single-event burnout under different VDS biases. For example, under the condition of a drain voltage of 100 V, a device leakage current of 40 uA was detected, indicating the occurrence of single-event burnout in the device. Figure 12 shows the EPICS spectra on SiC power MOSFETs of Ar ion irradiation. The cross marks indicate the maximum collected charge for each spectrum. Up to 300 V of the drain bias voltage, first and second peaks are apparently observed, as seen on Si power MOSFETs. It suggests that the charge multiplication mechanism of SiC power MOSFETs is the same as one of Si power MOSFETs. The difference between the first and second peaks was
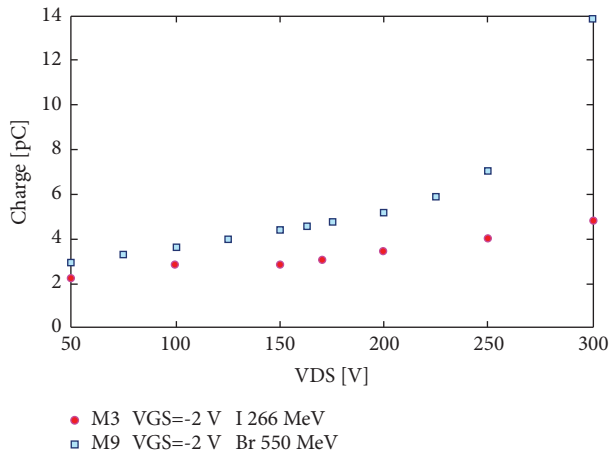
FIGURE 11: The collected mean charge during iodine and bromine irradiations [45].
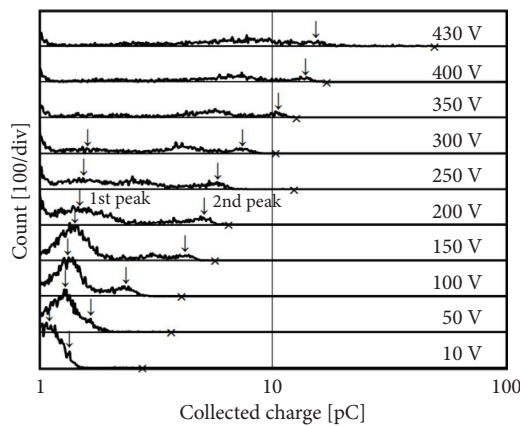

FIGURE 12: Collected charge spectra by Ar ion irradiation with EPICS system [46].

assumed to be the path of the incident ion to the device of generated charges. The second peak also shifted to the right with increased drain bias voltage as Si power MOSFETs. At the drain bias voltage of 350 V and higher, a permanent increase in the leakage current was observed, but no SEB was observed up to the voltage level, and the maximum collected charge was less than 100 pC.

In 2014, Asai and colleagues studied the single-event burnout failure characteristics of SiC MOSFET power devices against ground-level neutrons [47]. The results showed that the failure probability increases exponentially with the applied voltage and is several orders of magnitude lower compared to Si MOSFETs. Collisions between high-energy secondary carbon atoms generated from nuclear reactions and the lattice atoms of SiC devices may play an important role in the SEB triggering mechanism of SiC MOSFET power devices. Figure 13 shows the number of surviving devices normalized to the sample size as a function of fluence for SiC MOSFET-R and SiC MOSFET-C, which indicates an experimental reliability function. The plots mostly decrease monotonically and are fitted by exponential curves. The exponential decay constant increases with increasing

voltage. In Figure 13(a), these curves reproduce the major part of the experimental data (SiC MOSFET-R) fairly well, indicating a constant failure rate (random failure). In Figure 13(b), the poor fit seen in the SiC MOSFET-C data could be due to wear-out at higher bias voltages.

In 2015, Lanenstin and colleagues conducted heavy-ion irradiation experiments on 1200 V SiC MOSFET power devices [48]. The results showed a significant decrease in the safe operating voltage of the devices, along with current decay phenomena. The decrease in safe operating voltage directly affects the reliability indicators of the devices and impacts their space applications. Due to the high-voltage characteristics of SiC MOSFET power devices, they are highly susceptible to burnout and breakdown caused by heavy-ion irradiation.

In 2017, Akturk et al. reported on experimental studies of neutron-induced single-event failures in Si and SiC MOSFET power devices at room temperature [49]. They also investigated the reactive interfaces and low-field failure time curves of the devices and provided possible explanations for the failure mechanisms in SiC devices. The experiments found that compared to Si, the failures induced by neutrons in SiC MOSFET power devices were significantly reduced. Furthermore, within a high bias range, SiC power devices exhibited higher neutron radiation reliability.

In 2019, Abbate et al. presented an experimental characterization of damage in SiC MOSFET power devices induced by heavy-ion irradiation [50]. This study aimed to gain a deeper understanding of the physical mechanisms behind the formation of damage as a prerequisite for finite element simulation research. In the same year, Moreno and others, with the support of the ESA project, conducted research on reinforcement techniques for lateral SiC MOSFETs against radiation [51]. They focused on studying the reinforcement effects related to different gate oxide layer processes and structural designs.

In 2019, Wang and others conducted a study on the single-event burnout (SEB) characteristics and triggering mechanisms of 4H-SiC trench gate (TG) MOSFET structures [52]. As shown in Figure 14, they analyzed and compared the novel N+ island-buffered 4H-SiC TG MOSFET with the traditional 4H-SiC TG MOSFET to investigate whether introducing N+ island regions in the second buffer layer can effectively reduce collision ionization at the N− drift/N+ buffer junction and improve the device's tolerance to SEB. TCAD simulation results demonstrated that the N+ island-buffered hardened structure altered the burnout threshold voltage and significantly enhanced the performance of SEB compared to a simple double-buffered structure.

In 2020, McPherson and others described the failure mechanism of SiC MOSFET power devices under heavy-ion impact [53]. Simulation results showed that the reference device failed around 500 V, which was consistent with the experimental results. The failure occurred near the interface between the epitaxial layer and the substrate layer due to the rapid increase in electric field in that region and the destructive effects of collision ionization on the device.

From the simulation and experimental studies on the radiation-induced damage to microelectronic devices
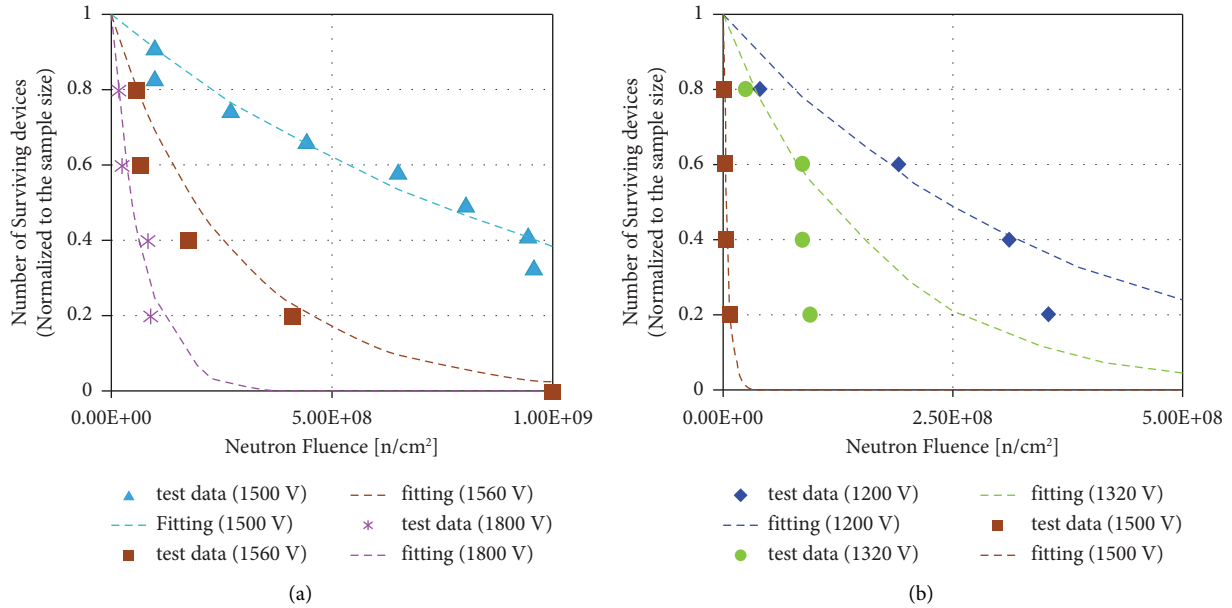
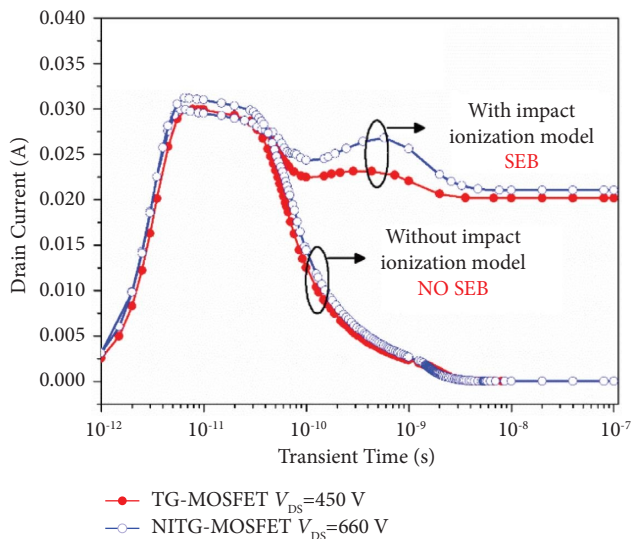Figure 13: Number of surviving devices versus neutron fluence [47]. (a) SiC MOSFET-R. (b) SiC MOSFET-C.

Figure 14: Drain current of the TG-MOSFET and the NITG-MOSFET at the SEB threshold voltage after the ion strike [52].

mentioned above, it can be observed that space particle irradiation can induce physical effects such as SEB (single-event burnout) and SEGR (single-event gate rupture), which significantly impact the performance of the devices. In particular, under single-particle effects, the safe operating voltage of power devices decreases sharply, leading to serious implications for the reliability of power device operation.

4. Radiation Hardening Techniques

4.1. Radiation Hardening Methods for SOI Technology. SOI technology can be traced back to the concept of Insulated Gate Field-Effect Transistors (IGFET), proposed by Lilienfeld in 1926 [54]. In 1963, Manasevit and Simpson

successfully grew silicon films on sapphire that met the device quality requirements, marking the practicalization of SOI technology [55]. In SOI technology, the silicon film is directly placed on top of an insulating layer, typically oxide. Compared to traditional techniques, SOI technology offers unique advantages. The insulating layer in the SOI structure effectively isolates transistors from each other, providing better performance and power characteristics.

Since the 1970s, SiO_2 has gradually been used as the insulating layer material in SOI technology. In the 1990s, technologies such as oxygen implantation isolation and smart cut were introduced, which reduced the cost of SOI materials and improved the quality of silicon films. As a result, the SOI process has become the mainstream CMOS technology [56].

In 2018, Peng et al. investigated two radiation-hardening processes for STI, namely Si implantation and STI oxide nitridation, including their impact on nominal electrical characteristics and radiation hardness [57]. It was found that the TID effects of the NMOS devices are sensitive to the STI radiation-hardening process conditions, and there are optimum process conditions to achieve the best effectiveness of radiation hardening. Then a 130 nm radiation-hardened PDSOI technology has been developed. The radiation hardness is verified by a SRAM with small storage capacities. The radiation hardening by Si^+ implantation and oxide nitridation is shown in Figure 15. As shown in Figure 15(a), a low tilt angle Si^+ implantation is added after liner oxidation. As shown in Figure 15(b), the NO process avoids the introduction of traps related to H atom compared to ammonia (NH_3) process. A NO annealing is added after liner oxidation in the standard STI process flow for thee sample.

SOI devices consist of a three-layer structure: a thin layer of silicon film on top of an insulating layer (such as SiO_2) and a silicon substrate. Compared to bulk silicon devices with the
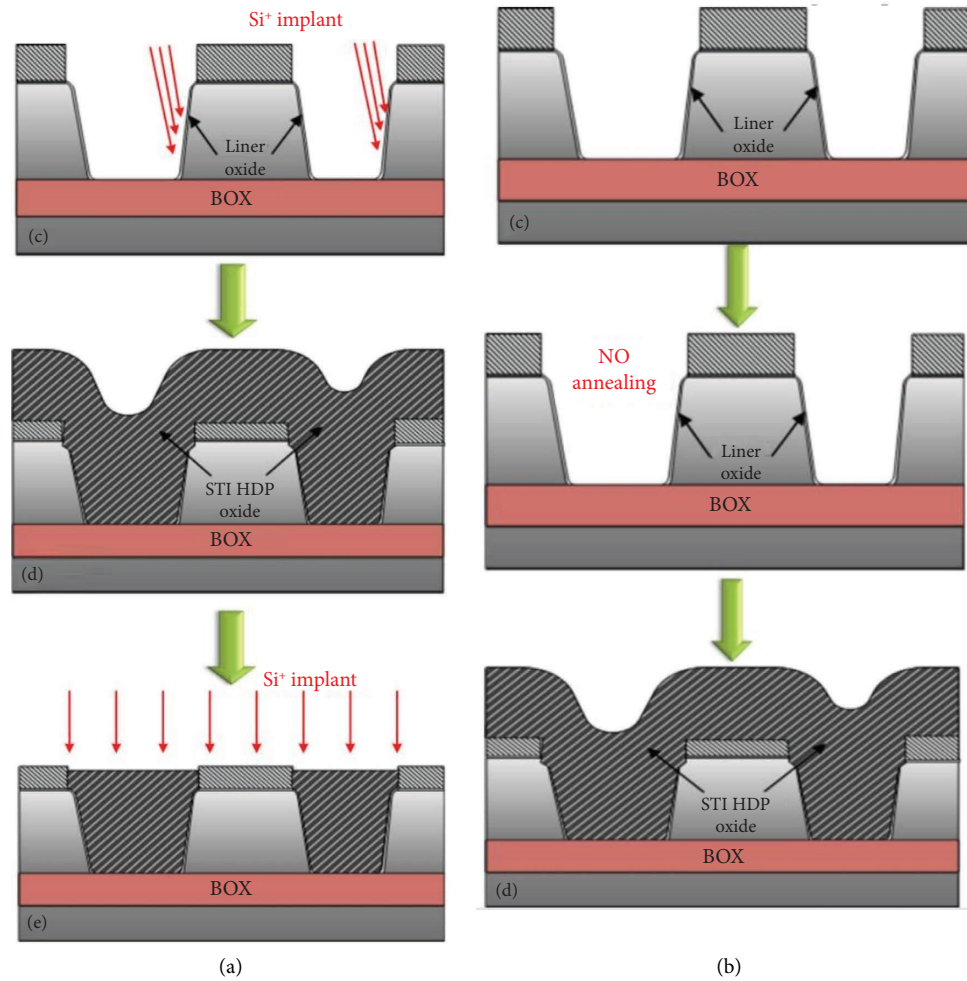
FIGURE 15: Two radiation-hardening processes [57]. (a) Radiation hardening by Si+ implantation in STI. (b) Radiation hardening by STI oxide nitridation.

same feature size, the charge collection in SOI devices is reduced [58]. This is because in the SOI structure, the insulating layer effectively prevents charge diffusion and drift in the substrate, keeping the majority of the charge in the top silicon film. By reducing charge diffusion and drift, SOI technology can achieve better suppression of charge-coupling noise and improve device speed and performance. In addition, SOI technology can reduce power consumption, enhance radiation tolerance, and provide better noise immunity.

SOI technology offers several advantages, including reduced parasitic capacitance and improved performance. When it comes to radiation hardening in SOI technology, certain methods can be employed to enhance its resilience against radiation-induced effects. One common method is the use of radiation-hardened materials specifically designed for SOI technology. These materials exhibit improved resistance to radiation and help mitigate the impact of radiation particles on the devices. Additionally, optimizing the design and fabrication processes can also enhance the radiation tolerance of SOI devices. Techniques such as redundant circuitry and error detection and correction

mechanisms can be employed to improve the devices' ability to tolerate radiation-induced errors.

Another approach is the implementation of shielding techniques. By introducing shielding materials around the devices, the impact of radiation particles can be reduced. Shielding materials can absorb or scatter radiation particles, thereby reducing their energy and quantity. This helps protect the devices from radiation-induced failures.

By combining these radiation-hardening methods, the performance and reliability of SOI devices can be improved in radiation environments. This is particularly crucial for critical applications such as aerospace, nuclear power, and high-energy physics experiments, where devices often need to operate in high-radiation environments.

4.2. Circuit-Level Hardening Methods. Compared to traditional radiation-hardened production lines, circuit-level reinforcement technology can utilize commercial process lines, reducing costs and improving performance. Traditional radiation-hardened chips require special materials, manufacturing processes, and dedicated radiation-hardened

production lines. The relatively low demand for radiation-hardened chips has resulted in high costs. Additionally, radiation-hardened processes often struggle to keep up with the pace of commercial processes, limiting the feature size of radiation-hardened circuits and thus restricting performance aspects such as speed, integration, and power consumption. On the other hand, circuit-level reinforcement technology strengthens circuits at the design level, making them more radiation-resistant without requiring special materials and manufacturing processes. This means that radiation-hardened circuits can be manufactured using commercial process lines, reducing costs and improving performance. However, the applicability of circuit-level reinforcement technology is limited, and for certain high-radiation environments with specific requirements, traditional radiation-hardened production lines are still necessary to meet the demands.

The increasing concern over the soft error rate of combinational logic has led to significant attention on reinforcement techniques for such logic. Due to the diverse nature of combinational logic, it is challenging to distinguish between soft error signals (such as single-event upsets) and normal signals, making reinforcement more difficult. Triple Modular Redundancy (TMR) is a commonly used technique that can enhance the radiation resistance of combinational logic to some extent. To further improve the radiation resistance of combinational logic, various measures can be taken. One approach is to appropriately increase the size of transistors, which can enhance their radiation tolerance. Larger transistors exhibit greater robustness and can better withstand the impact of soft errors. Another method is to enhance the driving capability of gate circuits. Stronger driving capability enables gate circuits to respond to input changes more quickly, thereby reducing the occurrence of single-event transient errors. Additionally, selecting appropriate gate circuit designs, such as employing antinoise techniques or differential circuit designs, can also enhance the radiation resistance of combinational logic.

In circuit design, several commonly used reinforcement techniques can be employed to improve the reliability of combinational logic. These include pulse filtering techniques using Muler C cells [59], reinforcement techniques based on CVSL (Cascode voltage switch logic) gates [60], pulse filtering techniques combining transmission gates and Schmitt triggers [61], pulse elimination techniques using clamping devices [62], and reinforcement techniques for the analog voter in TMR (Triple Modular Redundancy), among others [63].

4.3. System-Level Hardening Methods. At the system level, commonly used reinforcement methods rely on redundancy to improve system reliability. Redundancy can be categorized into two types: spatial redundancy and temporal redundancy. Spatial redundancy is a common technique, such as triple modular redundancy, which involves using multiple identical computing resources in the system to execute programs simultaneously and detect/correct errors by comparing the results. Temporal redundancy is a technique

that detects and corrects errors by executing the same or equivalent program multiple times. It includes forms such as duplicated execution and checkpoint rollback. Encoding techniques such as RESO, EDDI, and ED4I can be combined with temporal redundancy techniques to enhance system reliability [64].

Redundant computing methods can improve system reliability and fault tolerance, but they also introduce additional costs and performance overhead. To mitigate the cost of redundancy, current research focuses on the following aspects: Accurate fault coverage analysis: It is important to accurately assess potential faults in the system and determine the required level of redundancy. Resource optimization: Optimizing the resource utilization of redundant computing is crucial for cost reduction. This includes optimizing the design of redundant units, spatial configuration, and power management. Dynamic adaptability: Dynamically adjusting the level of redundancy and strategies based on real-time system operation is essential to providing sufficient redundancy protection when needed while minimizing performance and cost overhead. Hardware support: designing dedicated hardware accelerators or processors to provide efficient support for redundant computing. Emerging technology research: researching new redundant computing methods and technologies to achieve better performance-cost trade-offs. For example, machine learning-based redundancy optimization methods, novel error correction code schemes, and reconfigurable redundant computing architectures.

Ray et al. proposed a superscalar pipeline method that effectively utilizes idle computing resources to minimize performance loss [65]. In addition, Austin introduced a dynamic verification technique called DIVA (Dynamic Implementation Verification Architecture), which is essentially spatial redundancy [66]. It simplifies the design of the checker processor by incorporating shared branch prediction, instruction prefetching, and other structures. In addition to redundancy computing methods, there is another class of system-level reinforcement methods known as online supervision methods, including control flow detection and watchdogs [67].

5. Conclusion and Outlook

This review aims to delve into the challenges and damage mechanisms faced by microelectronic devices in radiation environments and introduce radiation-hardening techniques to enhance their reliability and stability under extreme conditions. Firstly, through extensive literature review and analysis from domestic and international sources, we have conducted a detailed analysis of the radiation environment that microelectronic devices encounter and the types of damage they may suffer, such as total ionizing dose effects and single-event effects, as well as how these damages impact device stability and reliability. Second, we have summarized the progress made in various radiation-hardening techniques for improving the radiation resistance of microelectronic devices.

In summary, this review emphasizes the importance of understanding the damage mechanisms of microelectronic devices in radiation environments and the significance of radiation-hardening techniques. It highlights the current research progress and challenges faced in this field. With ongoing technological advancements, further in-depth research on these issues will establish a solid foundation for the development and application of microelectronic devices, particularly in high-radiation environments. Through this review, we can further enhance our understanding of the performance damage of microelectronic devices in radiation environments and provide reference for the development of radiation-hardening techniques.

Data Availability

The data supporting this review are from previously reported studies and datasets, which have been cited.

Conflicts of Interest

The authors declare that they have no conflicts of interest to report regarding the present study.

Acknowledgments

References

[1] Q. Huang and J. Jiang, "An overview of radiation effects on electronic devices under severe accident conditions in NPPs, rad-hardened design techniques and simulation tools," *Progress in Nuclear Energy*, vol. 114, pp. 105–120, 2019.

[2] R. D. Schrimpf, *Radiation Effects in Microelectronics*, Springer, Berlin, Germany, 2007.

[3] T. Yano, T. Sawabe, K. Yoshida, and Y. Yamamoto, "High-temperature neutron irradiation effects on CVD-diamond, silicon and silicon carbide," *Journal of Nuclear Materials*, vol. 386–388, pp. 1018–1022, 2009.

[4] Q. Huang and J. Jiang, "A radiation-tolerant wireless monitoring system using a redundant architecture and diversified commercial off-the-shelf (COTS) components," *IEEE Transactions on Nuclear Science*, vol. 12, p. 1, 2018.

[5] L. Yan, M. Zhu, H. Huang, and L. Biao, "Study on molecular dynamics of CL-20/TNT eutectic and blended structures," *Journal of Naval University of Engineering*, vol. 35, no. 2, pp. 107–112, 2019.

[6] D. M. Fleetwood, E. X. Zhang, R. D. Schrimpf, S. T. Pantelides, and S. Bonaldo, "Effects of interface traps and hydrogen on the low-frequency noise of irradiated MOS devices," *IEEE Transactions on Nuclear Science*, vol. 23, p. 1, 2024.

[7] S. Tang, W. Wang, and Q. Ma, "Research on on-line fault diagnosis method for IGBT device of three-level inverter," *Chinese Journal of Scientific Instrument*, vol. 20, pp. 19–30.

[8] R. N. Yastrebinsky, V. I. Pavlenko, A. A. Karnauhov, N. I. Cherkashina, A. V. Yastrebinskaya, and A. I. Gorodov, "Radiation resistance of a structural material based on modified titanium hydride," *Science and Technology of Nuclear Installations*, vol. 2021, no. 110, Article ID 6658431, 13 pages, 2021.

[9] K. C. Nguyen, V. V. Le, T. N. Huynh, B. V. Luong, N. D. Nguyen, and H. N. Tran, "Interim storage of the dalat nuclear research reactor: radiation safety analysis," *Science and Technology of Nuclear Installations*, vol. 2020, Article ID 7327045, 10 pages, 2020.

[10] C. H. Yu, Y. Wang, X. J. Li, J. Q. Yang, M. T. Bao, and F. Cao, "Study of TID radiation effects on the breakdown voltage of buried P-pillar SOI LDMOSFETs," *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 3, pp. 303–309, 2021.

[11] E. Mikkola, *Hierarchical Simulation Method for Total Ionizing Dose Radiation Effects on CMOS Mixed-Signal circuits*, The University of Arizona, Tucson, AZ, USA, 2008.

[12] W. Mao, J. Yu, and T. Wang, "Research on the filling method of missing values of operating parameters of nuclear power plants," *Journal of Naval Engineering University*, vol. 35, no. 3, pp. 8–14, 2023.

[13] Z. Shen and Y. Dekui, "Current situation and development trend of space radiation environment engineering," *Spacecraft Environmental Engineering*, vol. 31, no. 3, pp. 229–240, 2014.

[14] D. M. Fleetwood, "Radiation effects in a post-Moore world," *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 509–545, 2021.

[15] W. Chen, G. U. O. Xiao-qiang, Y. A. O. Zhi-bin et al., "Key basic issues in equivalent gound simulation of space radiation effects," *Modern Applied Physics*, vol. 54, 2017.

[16] D. M. Fleetwood, "Total ionizing dose effects in MOS and low-dose-rate-sensitive linear-bipolar devices," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1706–1730, 2013.

[17] S. Toguchi, E. X. Zhang, M. Gorchichko et al., "Total-ionizing-dose effects on 3D sequentially integrated, fully depleted silicon-on-insulator MOSFETs," *IEEE Electron Device Letters*, vol. 41, no. 4, pp. 637–640, 2020.

[18] S. Xi, Q. Zheng, W. Lu, J. Cui, Y. Wei, and Q. Guo, "Modeling of TID-induced leakage current in ultra-deep submicron SOI NMOSFETs," *Microelectronics Journal*, vol. 102, no. 3, Article ID 104829, 2020.

[19] B. C. Wang, M. T. Qiu, W. Chen, C. H. Wang, and C. X. Tang, "Machine learning-based analyses for total ionizing dose effects in bipolar junction transistors," *Nuclear Science and Techniques*, vol. 33, no. 10, p. 131, 2022.

[20] K. F. Galloway, "TID through the looking glass," *IEEE NSREC Short Course*, vol. 23, 2013.

[21] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2584–2592, 1998.

[22] K. O. Petrosjanc, A. S. Adonin, I. A. Kharitonov, and M. V. Sicheva, *SOI Device Parameter Investigation and Extraction for VLSI Radiation Hardness Modeling with SPICE: Proceedings of 1994 IEEE International Conference on Microelectronic Test Structures*, IEEE, Piscataway, NY, USA, 1994.

[23] K. O. Petrosyants, I. A. Kharitonov, L. M. Sambursky, V. N. Bogatyrev, Z. M. Povarnitcyna, and E. S. Drozdenko, "Simulation of total dose influence on analog-digital SOI/SOS CMOS circuits with EKV-RAD macromodel," *East-West Design & Test Symposium (EWDTS 2013)*, IEEE, Piscataway, NY, USA, 2013.

[24] I. Sanchez Esqueda, H. J. Barnaby, K. E. Holbert, and Y. Boulghassoul, "Modeling inter-device leakage in 90 nm

bulk CMOS devices," *IEEE Transactions on Nuclear Science*, vol. 58, no. 3, pp. 793–799, 2011.

[25] I. Sanchez Esqueda, H. J. Barnaby, and M. P. King, "Compact modeling of total ionizing dose and aging effects in MOS technologies," *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1501–1515, 2015.

[26] S. Jagannathan, D. R. Herbison, W. T. Holman, and L. W. Massengill, "Behavioral modeling technique for TID degradation of complex analog circuits," *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3708–3715, 2010.

[27] Y. Li, N. Rezzak, E. X. Zhang et al., "Including the effects of process-related variability on radiation response in advanced foundry process design kits," *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3570–3574, 2010.

[28] W. Xinheng, Z. Xing, and G. Wenyu, "Modeling of total dose irradiation effect of MOSFETs under high dose irradiation conditions," *Journal of Semiconductors*, vol. 10, pp. 1325–1328, 2001.

[29] W. Kewei, B. Jianhui, and H. Zhengsheng, "Threshold voltage modeling of DSOI MOSFETs considering back-gate current (in English)," *Atomic Energy Science and Technology*, vol. 55, no. 12, pp. 2224–2230, 2021.

[30] J. Liu, *Prediction Model of Total Radiation Dose Based on Artificial Neural Network*, XiDian University, Xi'an, China, 2020.

[31] X. Yang, *Research on Radiation Effects Diagnosis of Integrated Circuits Based on Neural Networks*, Harbin Institute of Technology, Harbin, China, 2022.

[32] F. W. Arthur, D. R. Ball, K. F. Galloway, A. Javanainen, J. M. Lauenstein, and L. Andrew, "Sternberg single-event burnout mechanisms in SiC power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 15, 2018.

[33] C. X. Zhang, E. X. Zhang, D. M. Fleetwood et al., "Effects of bias on the irradiation and annealing responses of 4H-SiC MOS devices," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 2925–2929, 2011.

[34] S. Luo, W. He, Z. Zhang, L. He, J. Cao, and Q. Wu, "Investigation of single-event transient mitigation via pulse quenching in logic circuits," *IOP Conference Series: Earth and Environmental Science*, vol. 69, Article ID 012199, 2017.

[35] P. Hazdra, S. Popelka, V. Záhlava, and J. Vobecký, "Radiation damage in 4H-SiC and its effect on power device characteristics," *Solid State Phenomena*, vol. 242, pp. 421–426, 2015.

[36] A. Griffoni, J. van Duivenbode, D. Linten et al., "Neutron-induced failure in silicon IGBTs, silicon super junction and SiC MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 59, no. 4, pp. 866–871, 2012.

[37] G. Soelkner, W. Kaindl, M. Treu, and D. Peters, "Reliability of SiC power devices against cosmic radiation-induced failure," *Materials Science Forum*, vol. 556-557, pp. 851–856, 2007.

[38] T. Yano, M. Akiyoshi, K. Ichikawa, Y. Tachi, and T. Iseki, "Physical property change of heavily neutron-irradiated Si_3N_4 and SiC by thermal annealing," *Journal of Nuclear Materials*, vol. 289, no. 1-2, pp. 102–109, 2001.

[39] D. L. Oberg and J. L. Wert, "First nondestructive measurements of power MOSFET single event burnout cross sections," *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, pp. 1736–1741, 1987.

[40] J. H. Hohl and K. F. Galloway, "Analytical model for single event burnout of power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, pp. 1275–1280, 1987.

[41] X. Zhang, *Failure Mechanisms in Wideband Semiconductor Power Devices*, University of Maryland, College Park, MD, USA, 2006.

[42] R. Devanathan, W. J. Weber, and F. Gao, "Atomic scale simulation of defect production in irradiated 3C-SiC," *Journal of Applied Physics*, vol. 90, no. 5, pp. 2303–2309, 2001.

[43] K. K. Lee, J. S. Laird, T. Ohshima, S. Onoda, T. Hirao, and H. Itoh, "Current transient effect in N-channel 6H-SiC MOSFET induced by heavy ion irradiation," *Trans Tech Publications Ltd*, vol. 645, pp. 1013–1016, 2010.

[44] A. F. Witulski, D. R. Ball, K. F. Galloway et al., "Single-event burnout mechanisms in SiC power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 1951–1955, 2018.

[45] C. Abbate, G. Busatto, A. Cascio et al., *Single Event Effects Induced by Heavy Ion Irradiation in SiC Power MOSFETs*, 2012.

[46] E. Mizuta, S. Kuboyama, H. Abe, Y. Iwata, and T. Tamura, "Investigation of single-event damages on silicon carbide (SiC) power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 61, no. 4, pp. 1924–1928, 2014.

[47] H. Asai, I. Nashiyama, K. Sugimoto et al., "Tolerance against terrestrial neutron-induced single-event burnout in SiC MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3109–3114, 2014.

[48] J. M. Lauenstein, M. C. Casey, and K. A. LaBel, "Single-event effects in silicon carbide power devices," *NEPP Electronic Technology Workshop*, vol. 45, 2015.

[49] A. Akturk, R. Wilkins, J. McGarrity, and B. Gersey, "Single event effects in Si and SiC power MOSFETs due to terrestrial neutrons," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 529–535, 2017.

[50] C. Abbate, G. Busatto, D. Tedesco et al., "Gate damages induced in SiC power MOSFETs during heavy-ion irradiation—Part I," *IEEE Transactions on Electron Devices*, vol. 66, no. 10, pp. 4235–4242, 2019.

[51] J. Moreno, E. Cordero, D. López et al., "Assessing radiation hardness of SIC MOS structures," in *Proceedings of the 2018 18th European conference on radiation and its effects on components and systems (RADECS)*, pp. 1–8, Gothenburg, Sweden, September 2018.

[52] Y. Wang, M. Lin, X. J. Li et al., "Single-event burnout hardness for the 4H-SiC trench-gate MOSFETs based on the multi-island buffer layer," *IEEE Transactions on Electron Devices*, vol. 66, no. 10, pp. 4264–4272, 2019.

[53] A. McPherson, C. W. Hitchcock, T. P. Chow, W. Ji, and A. A. Woodworth, "Mechanisms of heavy ion-induced single event burnout in 4H-SiC power MOSFETs," *Trans Tech Publications Ltd*, vol. 1004, pp. 889–896, 2020.

[54] C. J. E. Lilienfeld: US Patent 1,745,175, 1930.

[55] H. M. Manasevit and W. I. Simpson, "Single-crystal silicon on a sapphire substrate," *Journal of Applied Physics*, vol. 35, no. 4, pp. 1349–1351, 1964.

[56] L. Palkuti, M. Alles, and H. Hughes, *The Role of Radiation Effects in SOI Technology Development: 2014 SOI-3d-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pp. 1-2, IEEE, 2014.

[57] C. Peng, Z. Hu, Y. En et al., "Radiation hardening by the modification of shallow trench isolation process in partially depleted SOI MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 65, no. 3, pp. 877–883, 2018.

[58] X. Xie, H. Zhu, D. Bi et al., "A comprehensive evaluation of radiation hardening by applying negative body bias and back-gate bias in 130 nm PDSOI technology," *Microelectronics Reliability*, vol. 105, Article ID 113564, 2020.

[59] P. Mongkolkachit and B. Bhuva, "Design technique for mitigation of alpha-particle-induced single-event transients

in combinational logic," *IEEE Transactions on Device and Materials Reliability*, vol. 3, no. 3, pp. 89–92, 2003.

[60] M. C. Casey, B. L. Bhuva, J. D. Black, and L. W. Massengill, "HBD using cascode-voltage switch logic gates for SET tolerant digital designs," *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2510–2515, 2005.

[61] Y. Sasaki, K. Namba, and H. Ito, "Soft error masking circuit and latch using Schmitt trigger circuit," *2006 21st IEEE international symposium on defect and fault tolerance in VLSI systems*, vol. 58, pp. 327–335, 2006.

[62] R. Garg, N. Jayakumar, S. P. Khatri, and G. Choi, "A design approach for radiation-hard digital electronics," in *Proceedings of the 43rd Annual Design Automation Conference*, San Francisco, CA, USA, June 2006.

[63] A. Michels, L. Petroli, C. A. L. Lisboa, F. Kastensmidt, and L. Carro, "SET fault tolerant combinational circuits based on majority logic," *2006 21st IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, vol. 32, pp. 345–352, 2006.

[64] N. Oh, P. P. Shirvani, and E. J. McCluskey, "Error detection by duplicated instructions in super-scalar processors," *IEEE Transactions on Reliability*, vol. 51, no. 1, pp. 63–75, 2002.

[65] J. Ray, J. C. Hoe, and B. Falsafi, "Dual use of superscalar datapath for transient-fault detection and recovery," in *Proceedings of the 34th ACM/IEEE International Symposium on Microarchitecture*, Austin, TX, USA, July 2001.

[66] T. M. Austin, "DIVA: a reliable substrate for deep submicron microarchitecture design," in *Proceedings of the 32nd Annual ACM/IEEE International Symposium on Microarchitecture*, Washington, DC, USA, June 1999.

[67] B. Liang, X. Xu, H. Yuan et al., "A system-level method for hardening phase-locked loop to single-event effects," *Materials Research Express*, vol. 9, no. 9, Article ID 096301, 2022.