

Research Article

Closed-Form Equation of Data Dependent Jitter in First Order Low Pass System

Sangjin Byun

Division of Electronics and Electrical Engineering, Dongguk University-Seoul, 26 Pil-dong 3-ga, Jung-gu, Seoul 100-715, Republic of Korea

Correspondence should be addressed to Sangjin Byun; sjbyun@dongguk.edu

Received 27 June 2014; Revised 29 August 2014; Accepted 31 August 2014; Published 16 October 2014

Academic Editor: Wenjian Yu

Copyright © 2014 Sangjin Byun. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

This paper presents a closed-form equation of data dependent jitter (DDJ) in first order low pass systems. The DDJ relates to the system bandwidth, the bit rate, the input rise/fall time, and the number of maximum consecutive identical bits of the data pattern. To confirm the derived equation, simulations have been done with a first order RC low pass circuit for various system bandwidths, bit rates, input rise/fall times, and data patterns. The simulation results agree well with the calculated DDJ values by the derived equation.

1. Introduction

As bit rate increases, timing jitter becomes more critical to system performances of a high speed serial interface. Timing jitter deteriorates signal quality at the transmitter side and degrades BER performance at the receiver side [1–4]. To guarantee the satisfactory system performances of a high speed serial interface, timing jitter should be accurately predicted and carefully considered when we design system architecture, link budget, and each circuit building block.

Timing jitter is composed of unbounded random jitter (RJ) and bounded deterministic jitter (DJ). The RJ is produced by Gaussian electrical noise within system components and the DJ is categorized into duty cycle distortion (DCD) jitter, data dependent jitter (DDJ), and bounded uncorrelated jitter (BUJ) [5, 6]. Among them, the DDJ is focused on in this paper. The DDJ has an impact on the high speed serial interface especially when the bit rate increases while the system bandwidth is restricted [7, 8]. As shown in Figure 1, the DDJ is generated when a certain data pattern with the bit rate, T_b , passes through a system with the limited bandwidth, f_{BW} .

So far, some papers have been published to predict the DDJ in the general transmission lines [7–9] and in the first order low pass systems [10–14]. The DDJ in the transmission

line may apply to the interconnect channels such as off-chip PCB traces, off-chip cables, and on-chip interconnect lines while the DDJ in the first order low pass system may apply to the transceiver circuit building blocks such as drivers, buffers, amplifiers, and limiters. For the transmission lines, the DDJ has been predicted by using the simulated transient step response and the worst-case input bit sequence to shorten the simulation time [7–9]. On the other hand, for the first order low pass systems, the DDJ has been predicted based on the infinite number of calculated pulse or step responses of all the previous bits while the rise/fall time of the input signal was assumed to be zero ideally. However, because it is not possible to calculate the infinite number of pulse or step responses of all the previous bits, only two or four preceding bits have been considered instead for the actual DDJ prediction [10–14]. So, the calculated DDJ always underestimates the real DDJ and the prediction accuracy may degrade as the bit rate increases relatively to the system bandwidth.

In this paper, a new closed-form equation of DDJ in the first order low pass system is presented. The DDJ is directly derived by solving the differential equation of the first order RC low pass circuit and by using the repetitiveness of the data pattern. Of course, this repetitiveness of the data pattern can be generalized for the real random data by increasing the pattern length to the infinity. The derived DDJ equation

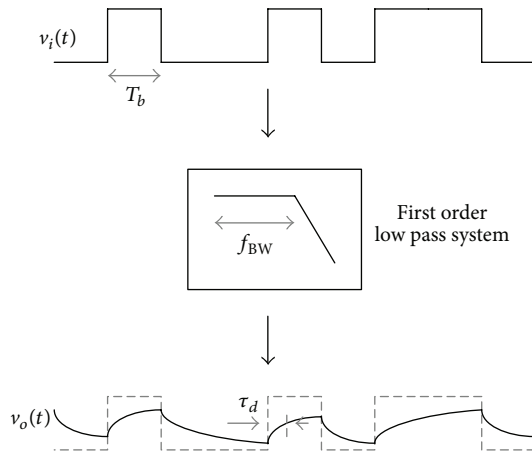


FIGURE 1: Response of first order low pass system.

relates to the system bandwidth, the bit rate, the input rise/fall time, and the number of maximum consecutive identical bits of the data pattern. Contrary to the previous works, the calculated DDJ by the derived equation coincides exactly with the simulated DDJ. Additionally, the effect of nonzero input rise/fall time is also to be considered.

This paper is composed of five sections. In Section 2, the closed-form DDJ equation is derived by assuming zero input rise/fall time. Section 3 extends the derived DDJ equation to the data pattern with nonzero input rise/fall time. To confirm the derived DDJ equation, the simulation results are shown in Section 4 and conclusions are given in Section 5.

2. Calculation of DDJ with Zero Input Rise/Fall Time

2.1. Differential Equation of First Order RC Low Pass Circuit. Given a data pattern, a bit rate, and a system bandwidth, the DDJ can be derived by solving the differential equation of the first order RC low pass circuit shown in Figure 2. Depending on the bit transition patterns, such as 01, 00, 10, and 11, the input signal, $v_i(t)$, and the initial condition, $v_o(nT_b)$, of the first order RC low pass circuit are given differently for each bit duration, T_b , as shown in Figure 3. In the figure, the input rise/fall time is zero ideally. So, $v_i(t)$ is $-A$ or $+A$ for $nT_b < t \leq (n+1)T_b$ and a new variable, $v_{e,n}$, is defined as the voltage difference between $v_i(t)$ and $v_o(t)$ at $t = nT_b$, where n is an integer; that is, $v_{e,n} = |v_i(nT_b) - v_o(nT_b)|$. Also, for the bit transition pattern of 01 or 10, another variable, $\tau_{d,n}$, is defined as the time difference between the threshold crossing times of $v_i(t)$ and $v_o(t)$, as shown in Figures 3(a) and 3(c). The definition of the variables can be found in Table 1.

Because there are four different sets of the input signal, $v_i(t)$, and the initial condition, $v_o(nT_b)$, depending on the bit transition patterns, the below differential equation of the first order RC low pass circuit should be solved for each bit transition pattern:

$$\frac{v_o(t) - v_i(t)}{R} + C \frac{dv_o(t)}{dt} = 0. \quad (1)$$

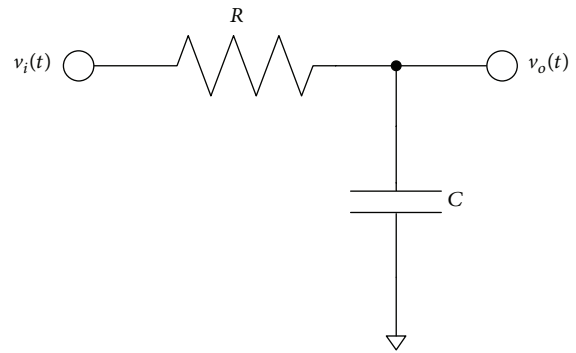


FIGURE 2: First order RC low pass circuit.

First, when the bit transition pattern is 01 as shown in Figure 3(a), the initial condition and the input signal are $v_o(nT_b) = -A + v_{e,n}$ and $v_i(t) = A$ for $nT_b < t \leq (n+1)T_b$, respectively. Then, the output signal is

$$v_o(t) = v_o(nT_b) + \{A - v_o(nT_b)\} (1 - e^{-(t-nT_b)/RC}) \quad (2)$$

for $nT_b \leq t \leq (n+1)T_b$.

By using that $v_o((n+1)T_b) = A - v_{e,n+1}$, the relationship between $v_{e,n}$ and $v_{e,n+1}$ is obtained as

$$v_{e,n+1} = 2Ar - v_{e,n}r, \quad (3)$$

where $r = e^{-(T_b/RC)}$ and, by using that $v_o(nT_b + \tau_{d,n}) = 0$, $\tau_{d,n}$ is obtained as a function of $v_{e,n}$:

$$\tau_{d,n} = T_b \log_r \left(\frac{A}{2A - v_{e,n}} \right). \quad (4)$$

Second, when the bit transition pattern is 00 as shown in Figure 3(b), $v_o(nT_b) = -A + v_{e,n}$ and $v_i(t) = -A$ for $nT_b < t \leq (n+1)T_b$. Then, the output signal is

$$v_o(t) = v_o(nT_b) + \{-A - v_o(nT_b)\} (1 - e^{-(t-nT_b)/RC}) \quad (5)$$

for $nT_b \leq t \leq (n+1)T_b$

and, by using that $v_o((n+1)T_b) = -A + v_{e,n+1}$, another relationship between $v_{e,n}$ and $v_{e,n+1}$ is obtained:

$$v_{e,n+1} = v_{e,n}r. \quad (6)$$

Finally, when the bit transition pattern is 10 or 11 as shown in Figures 3(c) or 3(d), the same relationship between $v_{e,n}$ and $v_{e,n+1}$ can be obtained as (3) or (6) and $\tau_{d,n}$ can be obtained as (4) because Figures 3(c) and 3(d) are just vertically symmetric with Figures 3(a) and 3(b). In summary, (3) and (6) describe how $v_{e,n}$ is updated to $v_{e,n+1}$ per every T_b according to the bit transition pattern and (4) describes how $\tau_{d,n}$ relates to $v_{e,n}$ when a bit transition occurs.

TABLE 1: Definition of the variables.

Variable	Definition
f_{BW}	3 dB bandwidth of the first order low pass system
T_b	Bit duration
f_b	Bit rate, $1/T_b$
ΔT	Rise/fall time of the input signal
$v_{e,n}$	Voltage difference between $v_i(t)$ and $v_o(t)$ at $t = nT_b$
$\tau_{d,n}$	Time difference between the threshold crossing times of $v_i(t)$ and $v_o(t)$ for $nT_b < t < (n+1)T_b$
$a_{i,n}$	Relative bit distance of the i th bit transition backwards from $v_{e,n}$
N	Pattern length
K	Number of bit transitions

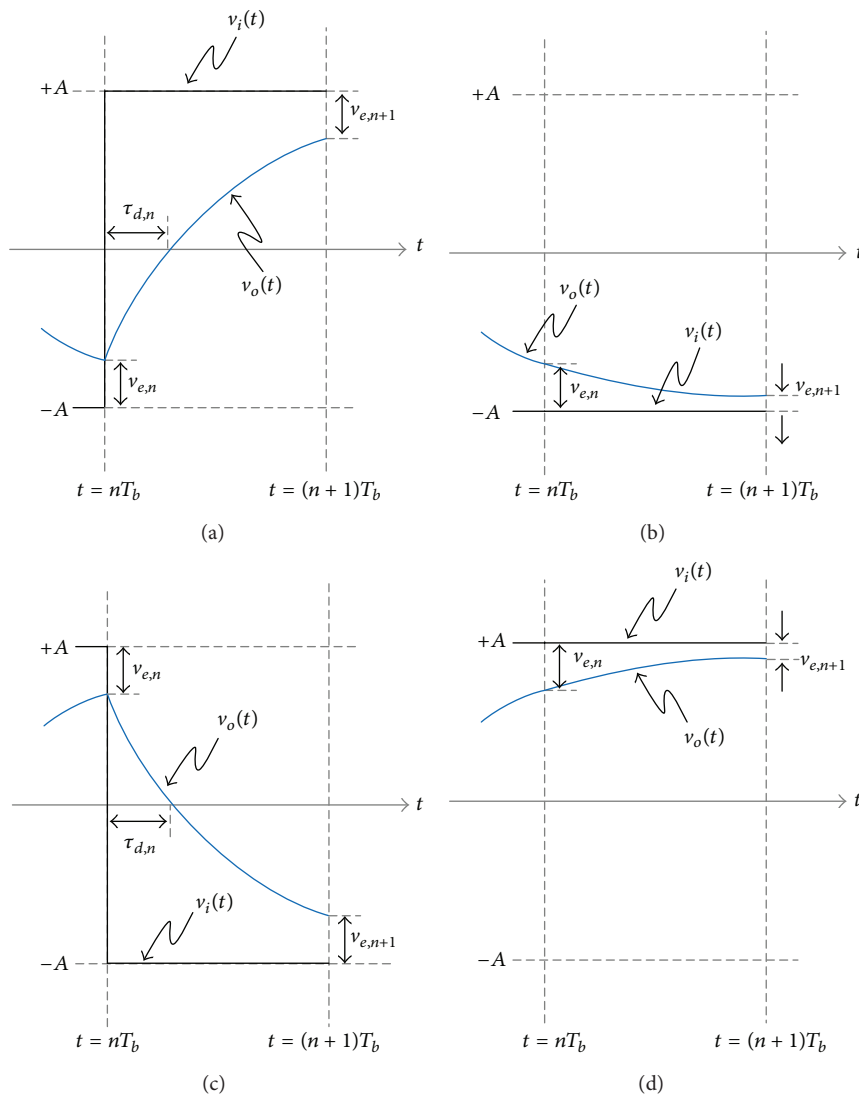


FIGURE 3: Input and output waveforms when the bit transition pattern is (a) 01, (b) 00, (c) 10, and (d) 11 and the input rise/fall time is zero.

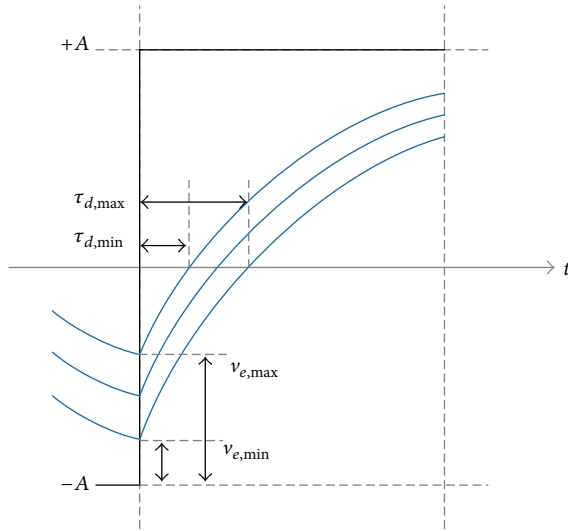


FIGURE 4: Relationship between $v_{e,n}$ and $\tau_{d,n}$.

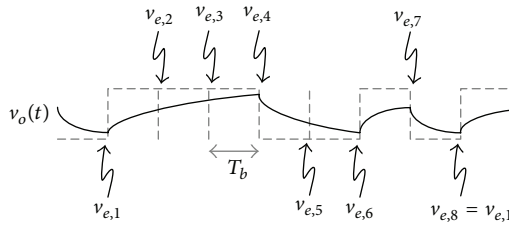


FIGURE 5: Output waveform when the input data pattern is PRBS3 as an example.

2.2. *DDJ Calculation.* By using (3), (6), and (4), the DDJ can be derived through the following steps.

- (i) Calculate $v_{e,n}$ by using (3) and (6) for the repeated data pattern with the finite pattern length of N .
- (ii) Find the maximum and minimum values, $v_{e,max}$ and $v_{e,min}$, among the set of the calculated $v_{e,n}$ values.
- (iii) Calculate $\tau_{d,min}$ and $\tau_{d,max}$ corresponding to $v_{e,max}$ and $v_{e,min}$ by using (4). Note that $\tau_{d,n}$ is inversely proportional to $v_{e,n}$ as shown in Figure 4.
- (iv) Finally, $DDJ = \tau_{d,max} - \tau_{d,min}$. For random data with the infinite pattern length, the DDJ equation should be modified appropriately.

If a data pattern has the finite pattern length of N and passes through a first order RC low pass circuit in a steady state, there should exist N different values of $v_{e,n}$ in the output waveform. For example, if a data pattern is PRBS3, the pattern length is 7 and $v_{e,n}$ is always mapped to one of $\{v_{e,1}, v_{e,2}, v_{e,3}, v_{e,4}, v_{e,5}, v_{e,6}, v_{e,7}\}$ as shown in Figure 5. However, all of $v_{e,n}$ do not need to be considered for calculation of the DDJ. Among $\{v_{e,1}, v_{e,2}, v_{e,3}, v_{e,4}, v_{e,5}, v_{e,6}, v_{e,7}\}$, $v_{e,1}, v_{e,4}, v_{e,6}$, and $v_{e,7}$ are needed because only they are at the bit transition edges of PRBS3. Thus, if the number of bit transitions within a data pattern is K , only K values of $v_{e,n}$ need to be considered for calculation of the DDJ. On the other hand, $v_{e,n}$ has Markov property [15, 16]. A variable is said to have Markov property

if the future value depends only on the present value and not on the past values. As seen from (3) and (6), $v_{e,n+1}$ depends only on $v_{e,n}$ and not on the preceding values of $v_{e,n}$ such as $v_{e,n-1}$ and $v_{e,n-2}$. Thus,

$$\begin{aligned} v_{e,2} &= 2Ar - v_{e,1}r, & v_{e,3} &= v_{e,2}r, \\ v_{e,4} &= v_{e,3}r, & v_{e,5} &= 2Ar - v_{e,4}r, \\ v_{e,6} &= v_{e,5}r, & v_{e,7} &= 2Ar - v_{e,6}r, \\ v_{e,8} &= 2Ar - v_{e,7}r. \end{aligned} \quad (7)$$

By using the repetitiveness of PRBS3, $v_{e,8} = v_{e,1}$ and, thus, $v_{e,1}, v_{e,4}, v_{e,6}$, and $v_{e,7}$ are obtained as follows:

$$v_{e,1} = 2Ar \frac{1 - r + r^3 - r^6}{1 - r^7} \quad (8)$$

$$v_{e,4} = 2Ar \frac{r^2 - r^3 + r^4 - r^6}{1 - r^7} \quad (9)$$

$$v_{e,6} = 2Ar \frac{r - r^4 + r^5 - r^6}{1 - r^7} \quad (10)$$

$$v_{e,7} = 2Ar \frac{1 - r^2 + r^5 - r^6}{1 - r^7}. \quad (11)$$

Before finding $v_{e,max}$ and $v_{e,min}$ from (8) to (11), $v_{e,n}$ can be generalized to

$$v_{e,n} = 2Ar \frac{\sum_{i=1}^K (-1)^{i+1} r^{a_{i,n}}}{1 - r^N} \quad (12)$$

for any data pattern with the finite pattern length of N . Here, K is the number of bit transitions and $a_{i,n}$ is an integer variable defined as the relative bit distance of the i th bit transition backwards from $v_{e,n}$, where $a_{i,n} \in \{0, 1, \dots, N-1\}$. In (12), $a_{i,n}$ is determined by the relative bit transition positions within the data pattern because the relationship between $v_{e,n+1}$ and $v_{e,n}$ is determined by (3) whenever a bit transition occurs like 01 or 10 and by (6) whenever a bit holds like 00 or 11. Figure 6 shows that $a_{1,1} = 0, a_{2,1} = 1, a_{3,1} = 3$, and $a_{4,1} = 6$ for $v_{e,1}$ and $a_{1,4} = 2, a_{2,4} = 3, a_{3,4} = 4$, and $a_{4,4} = 6$ for $v_{e,4}$, respectively, as an example. The obtained values of $a_{i,n}$ in Figure 6 agree well with (8) and (9). Thus, $v_{e,n}$ can be generally represented as (12) for any data pattern with the finite pattern length of N if the data pattern is known.

Now, $v_{e,max}$ and $v_{e,min}$ can be found among $\{v_{e,1}, v_{e,2}, \dots, v_{e,N}\}$. If $v_{e,m} = 2Ar(\sum_{i=1}^K (-1)^{i+1} r^{a_{i,m}} / (1 - r^N))$ and $v_{e,n} = 2Ar(\sum_{i=1}^K (-1)^{i+1} r^{a_{i,n}} / (1 - r^N))$, where $m \neq n$, $v_{e,m}$ and $v_{e,n}$ can be compared by using the following theorems, of which proofs are given in Appendix A.

Theorem 1. If $a_{1,m} > a_{1,n}$, then $v_{e,m} < v_{e,n}$.

Theorem 2. If $a_{i,m} = a_{i,n}$ for all $i = 1, \dots, 2k-1$, where k is an integer and $a_{2k,m} > a_{2k,n}$, then $v_{e,m} > v_{e,n}$.

Theorem 3. If $a_{i,m} = a_{i,n}$ for all $i = 1, \dots, 2k$, where k is an integer and $a_{2k+1,m} > a_{2k+1,n}$, then $v_{e,m} < v_{e,n}$.

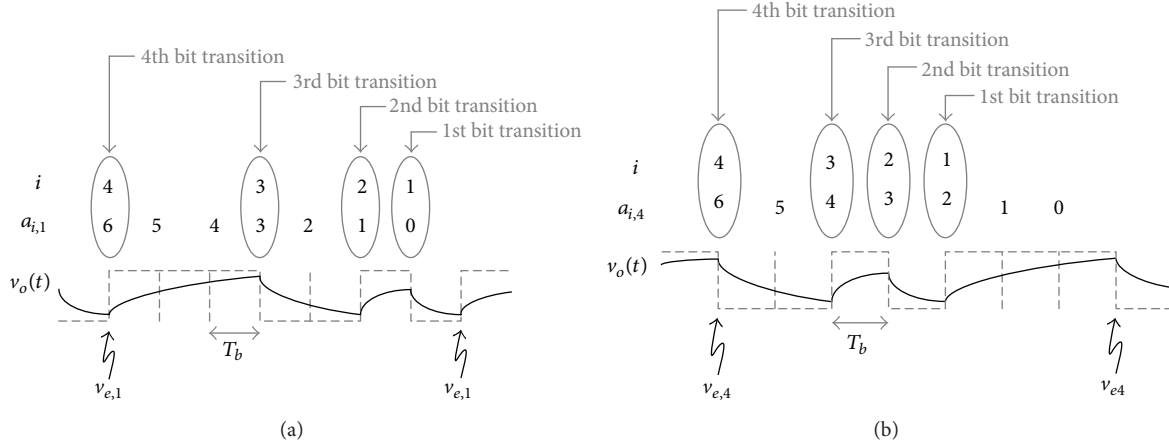


FIGURE 6: How to determine (a) $a_{i,1}$ of $v_{e,1}$ and (b) $a_{i,4}$ of $v_{e,4}$ when the input data pattern is PRBS3 as an example.

For PRBS3, $v_{e,min} = v_{e,4}$ by Theorem 1 because $a_{1,1} = a_{1,7} = 0 < a_{1,6} = 1 < a_{1,4} = 2$ and $v_{e,max} = v_{e,7}$ by Theorem 2 because $a_{2,1} = 1 < a_{2,7} = 2$ as seen from (8)~(11). These theorems can be generally applied to any data pattern with the finite pattern length. However, if a data pattern is random and has the infinite pattern length, there are infinite numbers of $v_{e,n}$ and so $v_{e,max}$ and $v_{e,min}$ are obtained in the different way. In that case, the number of maximum consecutive identical bits is also infinite so that $v_{e,min} = 0$ from (12) and $v_{e,max} = 2Ar$ from (3).

After $v_{e,max}$ and $v_{e,min}$ are found, $\tau_{d,max}$ and $\tau_{d,min}$ are obtained by (4) as

$$\begin{aligned} \tau_{d,max} &= T_b \log_r \left(\frac{A}{2A - v_{e,min}} \right) \\ \tau_{d,min} &= T_b \log_r \left(\frac{A}{2A - v_{e,max}} \right) \end{aligned} \quad (13)$$

and the DDJ is finally derived as

$$DDJ = \tau_{d,max} - \tau_{d,min} = T_b \log_r \left(\frac{2A - v_{e,max}}{2A - v_{e,min}} \right). \quad (14)$$

Thus, for PRBS3,

$$DDJ = T_b \log_r \left(\frac{1 - r + r^3 - r^6}{1 - r^3 + r^4 - r^5} \right) \quad (15)$$

and, for random data,

$$DDJ = T_b \log_r (1 - r). \quad (16)$$

Additionally, for other PRBS data patterns like PRBS4 and PRBS5, the DDJ can be derived as shown in Appendix B. Carefully observing (15), (16), (B.1), and (B.2), the DDJ can be generally approximated to

$$DDJ \approx T_b \log_r \left(\frac{1 - r}{1 - r^M} \right) \quad (17)$$

for any data pattern by using the number of maximum consecutive identical bits, M . For any PRBS M data patterns,

the number of maximum consecutive identical bits equals M . Finally, the calculated $v_{e,max}$, $v_{e,min}$, $\tau_{d,max}$, $\tau_{d,min}$, and DDJ are compared for various data patterns in Table 2. The DDJ of PRBS M approaches the DDJ of random data as the number of maximum consecutive identical bits, M , increases to the infinity.

3. Calculation of DDJ with Nonzero Input Rise/Fall Time

3.1. Differential Equation of First Order RC Low Pass Circuit. Now, the effect of the nonzero input rise/fall time on the DDJ can be considered. The differential equation of (1) should be solved again for four different bit transition patterns, such as 01, 00, 10, and 11, when the input rise/fall time is ΔT as shown in Figure 7. Although there are more accurate models for the rising/falling edges of the input signal, $v_i(t)$, the first order model is adopted for simplicity of calculation to derive the closed-form DDJ equations in this paper.

First, when the bit transition pattern is 01 as shown in Figure 7(a), the initial condition is $v_o(nT_b) = -A + v_{e,n}$ and the input signal is $v_i(t) = -A + (2A/\Delta T)(t - nT_b)$ for $nT_b < t \leq nT_b + \Delta T$ and $v_i(t) = A$ for $nT_b + \Delta T < t \leq (n + 1)T_b$, respectively. Then, the output signal is

$$\begin{aligned} v_o(t) &= -A + \frac{2A}{\Delta T} (t - nT_b - RC) \\ &+ \left(\frac{2A}{\Delta T} RC + v_{e,n} \right) e^{-(t-nT_b)/RC} \end{aligned} \quad (18)$$

$$\begin{aligned} &\text{for } nT_b < t \leq nT_b + \Delta T, \\ v_o(t) &= v_o(nT_b + \Delta T) \\ &+ \{A - v_o(nT_b + \Delta T)\} \left(1 - e^{-(t-nT_b-\Delta T)/RC} \right) \end{aligned} \quad (19)$$

for $nT_b + \Delta T < t \leq (n + 1)T_b$.

By using that $v_o((n + 1)T_b) = A - v_{e,n+1}$, the relationship between $v_{e,n}$ and $v_{e,n+1}$ is obtained as

$$v_{e,n+1} = 2ASr - v_{e,n}r, \quad (20)$$

TABLE 2: Calculated $v_{e,\max}$, $v_{e,\min}$, $\tau_{d,\max}$, $\tau_{d,\min}$, and DDJ values for various data patterns. The input rise/fall time is zero. $T_b = 100$ ps and $f_{\text{BW}} = 2$ GHz.

Data pattern	PRBS3	PRBS4	PRBS5	Random
$v_{e,\max}$ (V)	0.52	0.56	0.57	0.57
$v_{e,\min}$ (V)	0.04	0.01	0.00	0.00
$\tau_{d,\max}$ (ps)	53.70	54.75	55.02	55.16
$\tau_{d,\min}$ (ps)	30.99	29.23	28.67	28.51
DDJ (ps)	22.71	25.52	26.35	26.65

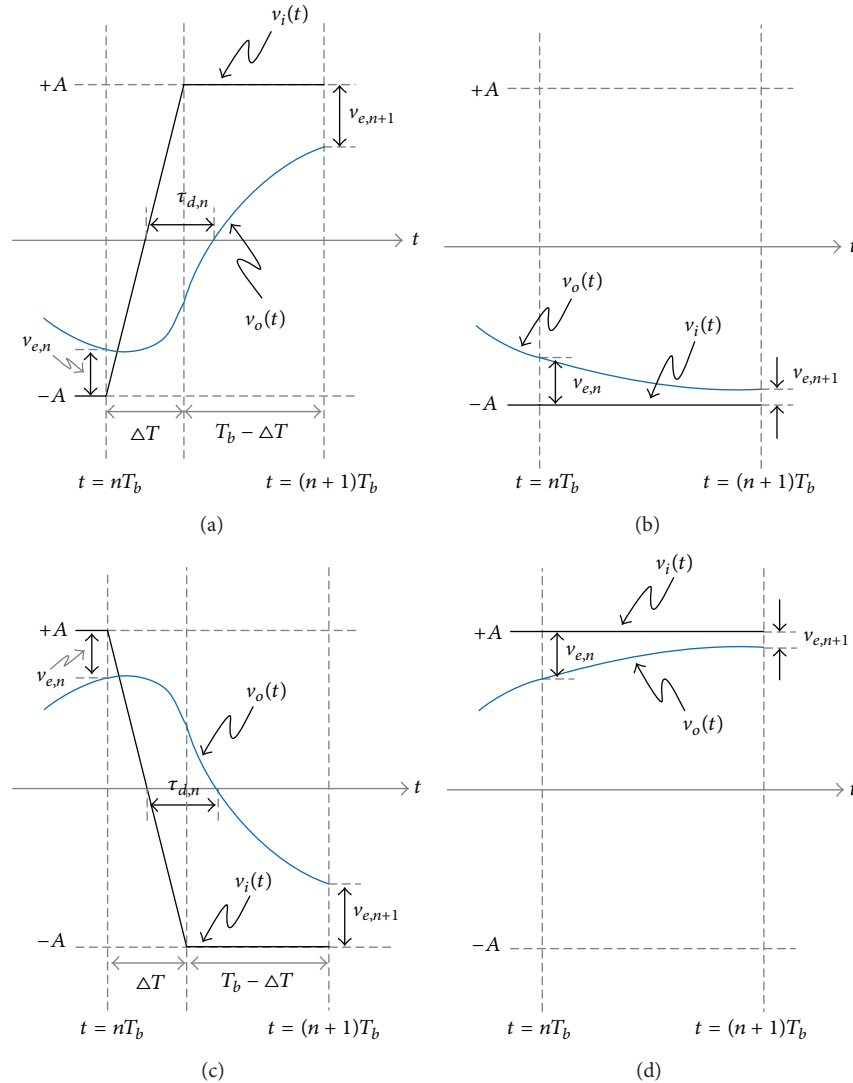


FIGURE 7: Input and output waveforms when the bit transition pattern is (a) 01, (b) 00, (c) 10, and (d) 11 and the input rise/fall time is nonzero.

where $r = e^{-(T_b/RC)}$ and $S = (RC/\Delta T)(e^{\Delta T/RC} - 1)$. Also, by using that $v_o(nT_b + (\Delta T/2) + \tau_{d,n}) = 0$, $\tau_{d,n}$ can be obtained as a function of $v_{e,n}$. However, to solve $v_o(nT_b + (\Delta T/2) + \tau_{d,n}) = 0$, (18) should be used if $\tau_{d,n} < \Delta T/2$ and (19) should be used if $\tau_{d,n} > \Delta T/2$. Because $v_o(nT_b + \Delta T) < 0$ is equivalent to $\tau_{d,n} > \Delta T/2$ in Figure 7(a), we can say that (18) should be

used if $v_o(nT_b + \Delta T) > 0$ and (19) should be used if $v_o(nT_b + \Delta T) < 0$. Figure 8 shows the sufficient condition for $\tau_{d,n} > \Delta T/2$ regardless of $v_{e,n}$ as region 1 and $\tau_{d,n} < \Delta T/2$ regardless of $v_{e,n}$ as region 2, respectively. Region 3 is located between region 1 and region 2, in which $\tau_{d,n}$ can be larger or less than $\Delta T/2$ depending on $v_{e,n}$. The regions 1, 2, and 3 of Figure 8 can

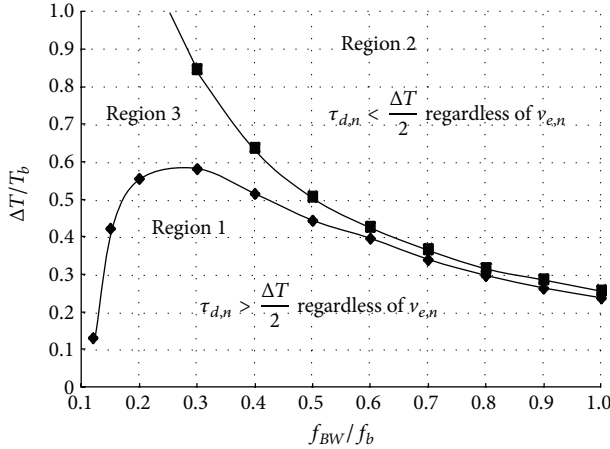


FIGURE 8: Sufficient conditions for $\tau_{d,n} > \Delta T/2$ and $\tau_{d,n} < \Delta T/2$ regardless of $v_{e,n}$.

be obtained by solving $v_o(nT_b + \Delta T) = 0$. Here, f_{BW} is the 3 dB bandwidth of the first order low pass system which is defined as $f_{BW} = 1/2\pi RC$. Thus, $\tau_{d,n}$ is obtained as

$$\tau_{d,n} = T_b \log_r \left(\frac{A}{2AS - v_{e,n}} \right) - \frac{\Delta T}{2} \quad (21)$$

from (19) in region 1 and

$$\tau_{d,n} = T_b \log_r \left\{ \frac{(2A/\Delta T)(RC - \tau_{d,n})}{(2A/\Delta T)RC + v_{e,n}} \right\} - \frac{\Delta T}{2} \quad (22)$$

from (18) in region 2, respectively. In region 3, either (21) or (22) should be appropriately chosen for $\tau_{d,n}$ but after both (21) and (22) are evaluated and compared with $\Delta T/2$ because (21) is used if $\tau_{d,n} > \Delta T/2$ and (22) is used if $\tau_{d,n} < \Delta T/2$. Second, when the bit transition pattern is 00 as shown in Figure 7(b), the initial condition and the input signal are equal to those of Figure 3(b) so that the same relationship between $v_{e,n}$ and $v_{e,n+1}$ is obtained:

$$v_{e,n+1} = v_{e,n}r. \quad (23)$$

Finally, when the bit transition pattern is 10 or 11 as shown in Figures 7(c) or 7(d), the same relationship between $v_{e,n}$ and $v_{e,n+1}$ can be obtained as (20) or (23) and $\tau_{d,n}$ can be obtained from (21) or (22) because Figures 7(c) and 7(d) are just vertically symmetric with Figures 7(a) and 7(b), respectively.

3.2. DDJ Calculation. As seen from (20) and (23), $v_{e,n}$ has Markov property also when the input rise/fall time is ΔT . Thus, $v_{e,n}$ can be generally represented as

$$v_{e,n} = 2ASr \frac{\sum_{i=1}^K (-1)^{i+1} r^{a_{i,n}}}{1 - r^N} \quad (24)$$

for any data pattern with the finite pattern length of N by following the same steps explained in Section 2.2. Here, K is the number of bit transitions within the data pattern and $a_{i,n}$ is

an integer variable defined as the relative bit distance of the i th bit transition backwards from $v_{e,n}$, where $a_{i,n} \in \{0, 1, \dots, N - 1\}$. The only difference between (24) and (12) is the additional multiplication factor, S , in (24). So, $v_{e,\max}$ and $v_{e,\min}$ can be found among $\{v_{e,1}, v_{e,2}, \dots, v_{e,N}\}$ by comparing only $a_{i,n}$ values based on the same theorems stated in Section 2.2. Of course, if a data pattern is random and has the infinite pattern length, $v_{e,\min} = 0$ and $v_{e,\max} = 2ASr$. For any data pattern, $\tau_{d,\max}$ and $\tau_{d,\min}$ can be obtained from either (21) or (22) depending on f_{BW}/f_b and $\Delta T/T_b$. If f_{BW}/f_b and $\Delta T/T_b$ are in region 1 of Figure 8,

$$\begin{aligned} \tau_{d,\max} &= T_b \log_r \left(\frac{A}{2AS - v_{e,\min}} \right) - \frac{\Delta T}{2} \\ \tau_{d,\min} &= T_b \log_r \left(\frac{A}{2AS - v_{e,\max}} \right) - \frac{\Delta T}{2} \end{aligned} \quad (25)$$

from (21) and if f_{BW}/f_b and $\Delta T/T_b$ are in region 2,

$$\begin{aligned} \tau_{d,\max} &= T_b \log_r \left\{ \frac{(2A/\Delta T)(RC - \tau_{d,\max})}{(2A/\Delta T)RC + v_{e,\min}} \right\} - \frac{\Delta T}{2} \\ \tau_{d,\min} &= T_b \log_r \left\{ \frac{(2A/\Delta T)(RC - \tau_{d,\min})}{(2A/\Delta T)RC + v_{e,\max}} \right\} - \frac{\Delta T}{2} \end{aligned} \quad (26)$$

from (22). Otherwise, if f_{BW}/f_b and $\Delta T/T_b$ are in region 3, the appropriate equations should be chosen from (25) and (26) for calculation of $\tau_{d,\max}$ and $\tau_{d,\min}$ by comparing the calculated values of $\tau_{d,\max}$ and $\tau_{d,\min}$ with $\Delta T/2$. Consequently, the DDJ is derived as

$$DDJ = \tau_{d,\max} - \tau_{d,\min} = T_b \log_r \left(\frac{2AS - v_{e,\max}}{2AS - v_{e,\min}} \right) \quad (27)$$

in region 1 and the DDJ is calculated by using (26) in region 2. Although (27) and (14) look a bit different, the DDJ equation of (27) equals the DDJ equation of (14) since $v_{e,\min}$ and $v_{e,\max}$ are linearly proportional to the multiplication factor, S , as shown in (24) and thus S is cancelled out from (27). This means that the DDJ value does not depend on ΔT in region 1 and equals the DDJ value when $\Delta T = 0$. On the other hand, the DDJ value in region 2 is slightly larger than the DDJ value when $\Delta T = 0$. However, the difference is quite small and acceptable because the system bandwidth is relatively large compared to the bit rate in region 2 as shown in Figure 8 and so the DDJ value is very small in itself.

4. Simulation Results

Figure 9 shows the eye diagrams of the simulated input and output waveforms when the data pattern is (a) PRBS3 and (b) random, respectively. The input rise/fall time is zero, the bit rate is 10 Gb/s, and the system bandwidth is 2 GHz. All the waveforms were obtained by running Cadence Spectre. In Figure 9(a), among $\{v_{e,1}, v_{e,4}, v_{e,6}, v_{e,7}\}$, $v_{e,\max} = v_{e,7}$ and $v_{e,\min} = v_{e,4}$, as discussed in Section 2.2. So, $\tau_{d,\max} = \tau_{d,4}$, $\tau_{d,\min} = \tau_{d,7}$, and $DDJ = \tau_{d,4} - \tau_{d,7}$. In Figure 9(b), $v_{e,\min} = 0$ and $v_{e,\max} = 2Ar$, and $\tau_{d,\max}$ and $\tau_{d,\min}$ correspond to $v_{e,\min}$

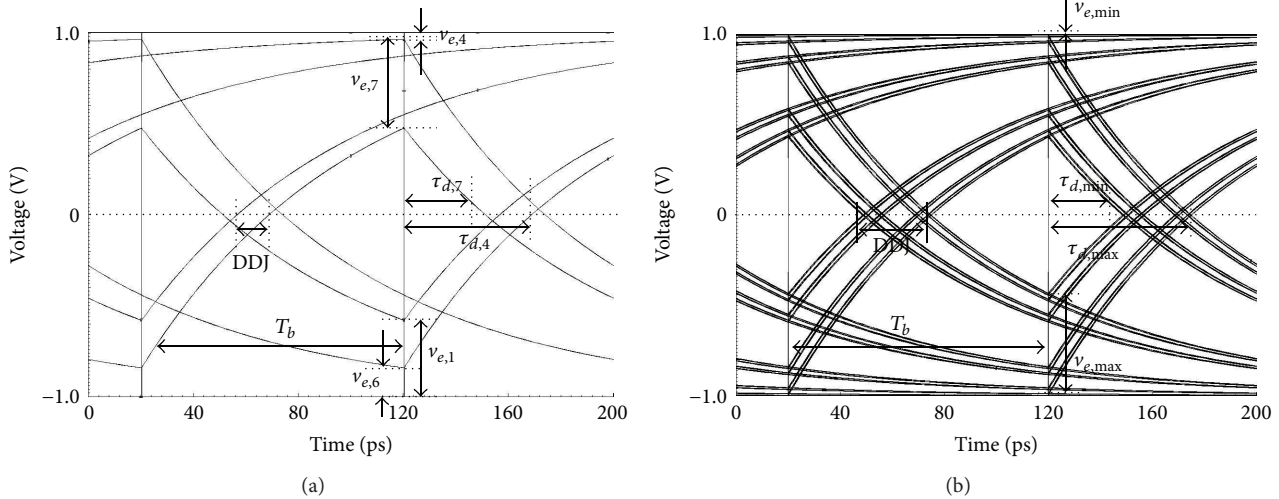


FIGURE 9: Eye diagrams of the simulated input and output waveforms when the input data pattern is (a) PRBS3 and (b) random. The input rise/fall time is zero. $T_b = 100$ ps and $f_{BW} = 2$ GHz.

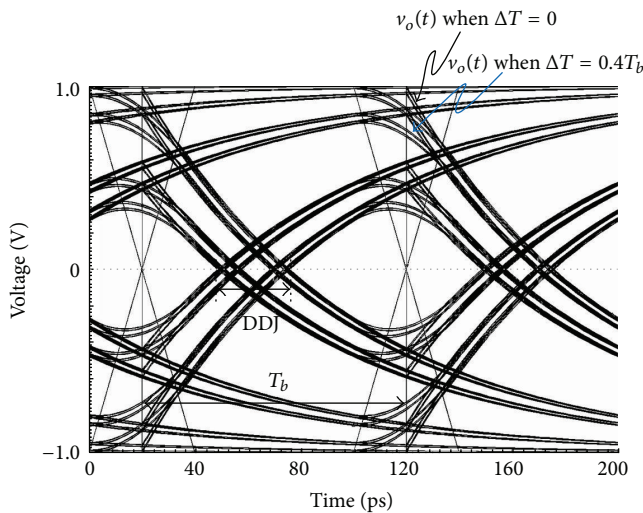


FIGURE 10: Comparison of eye diagrams of the output waveforms when $\Delta T = 0$ and $\Delta T = 0.4T_b$. $T_b = 100$ ps and $f_{BW} = 2$ GHz.

and $v_{e,max}$, respectively. All the simulated $v_{e,max}$, $v_{e,min}$, $\tau_{d,max}$, $\tau_{d,min}$, and DDJ for various data patterns agree exactly with the calculated values in Table 2.

Figure 10 compares the eye diagrams of the simulated output waveforms for $\Delta T = 0$ and $\Delta T = 0.4T_b$. The data pattern is random, the bit rate is 10 Gb/s, and the system bandwidth is 2 GHz. The input signal, of which rise/fall time is modeled by ΔT as first order approximation, is applied to the first order low pass system. As shown in Figure 10, two output waveforms slightly differ from each other only around the transition edges of the input signals; however, they exactly coincide with each other around the transition edges of the output signals. Thus, the simulated DDJ when $\Delta T = 0.4T_b$ equals the simulated DDJ when $\Delta T = 0$. This coincidence between $\Delta T = 0$ and $\Delta T = 0.4T_b$ is due to the fact that f_{BW}/f_b and $\Delta T/T_b$ are in region 1.

Figure 11(a) shows the comparison of the simulated DDJ with the calculated DDJ by (16) in this work and the calculated DDJ by (10) in [10]. The calculated DDJ in this work better estimates the simulated DDJ. As the system bandwidth, f_{BW} , decreases, the calculated DDJ by (10) in [10] underestimates the simulated DDJ because (10) in [10] was derived by using only two preceding bits as discussed in Appendix C. Figure 11(b) shows the simulated DDJ for various input rise/fall times. ΔT varies from 0 to $0.75T_b$. If f_{BW}/f_b and $\Delta T/T_b$ are in region 1, the simulated DDJ does not depend on ΔT ; however, in region 2, the simulated DDJ starts to deviate as ΔT increases. Even in this case, the deviation of the simulated DDJ is smaller than 0.008 UI because the absolute DDJ value is very small in itself, that is, less than 0.01 UI, in region 2. The system bandwidth, f_{BW} , is relatively large compared to the bit rate, f_b , in region 2 as shown in Figure 8.

Additionally, the simulated DDJ values when the low pass system has the additional second pole, f_{p2} , are summarized in Table 3. As shown in the table, the calculated DDJ values by the derived equations agree well with the simulated results with the accuracy of less than 0.021 UI when the second pole is larger than 5 times of the first pole, that is, 10 GHz. However, if the second pole approaches the first pole, the system bandwidth now decreases less than the first pole so that the simulated results start to deviate from the calculated DDJ values.

5. Conclusion

The closed-form equation of DDJ in a first order low pass system has been derived. If the bit rate, the system bandwidth, the input rise/fall time, and the number of maximum consecutive identical bits are given, the DDJ can be calculated exactly in region 1 and accurately in regions 2 and 3. The simulated DDJ agrees well with the calculated DDJ. Because the DDJ in the transmission line may apply to

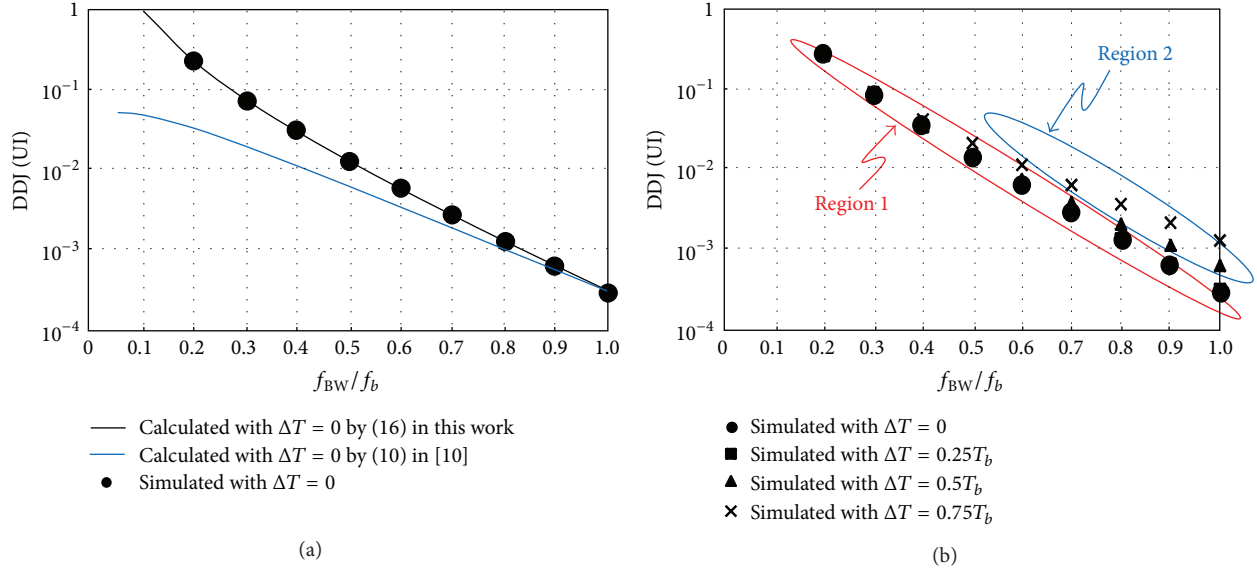


FIGURE 11: (a) Comparison of the DDJ values calculated by (16) in this work and by (10) in [10] and (b) the simulated DDJ values versus various input rise/fall times.

TABLE 3: Simulated DDJ values when the low pass system has the additional second pole, f_{p2} . The input rise/fall time is zero. $T_b = 100$ ps and $f_{p1} = 2$ GHz.

Second pole	Data pattern			
	PRBS3	PRBS4	PRBS5	Random
No second pole	22.71	25.52	26.35	26.65
$f_{p2} = 20$ GHz	22.81	25.68	26.52	26.83
$f_{p2} = 10$ GHz	24.35	27.48	28.41	28.75
$f_{p2} = 5$ GHz	32.23	36.86	38.48	38.81

the interconnect channels such as off-chip PCB traces, off-chip cables, and on-chip interconnect lines and the DDJ in the first order low pass system may apply to the transceiver circuit building blocks such as drivers, buffers, amplifiers, and limiters, the derived equation can be generally used for a high speed serial interface when we design system architecture, link budget, and each circuit building block which can be modeled as a first order low pass system.

Appendices

A. Proofs of Theorems 1, 2, and 3

Proof of Theorem 1. Subtracting $v_{e,m}$ from $v_{e,n}$ leads to

$$\begin{aligned} v_{e,n} - v_{e,m} &= \frac{2Ar}{1-r^N} \left\{ \sum_{i=1}^K (-1)^{i+1} r^{a_{i,n}} - \sum_{i=1}^K (-1)^{i+1} r^{a_{i,m}} \right\} \\ &> \frac{2Ar}{1-r^N} (r^{a_{1,n}} - r^{a_{2,n}} - r^{a_{1,m}}), \end{aligned} \quad (\text{A.1})$$

because $r^{a_{i,n}} - r^{a_{i+1,n}} > 0$. By using the fact that $r^{a_{1,n}} - r^{a_{2,n}} - r^{a_{1,m}}$ is minimum when $a_{2,n} = a_{1,n} + 1$ and $a_{1,m} = a_{1,n} + 1$,

$$\begin{aligned} v_{e,n} - v_{e,m} &> \frac{2Ar}{1-r^N} (r^{a_{1,n}} - r^{a_{1,n}+1} - r^{a_{1,n}+1}) \\ &= \frac{2Ar}{1-r^N} r^{a_{1,n}} (1-2r) > 0, \end{aligned} \quad (\text{A.2})$$

because r is smaller than 0.5 as far as the system bandwidth, f_{BW} , is larger than 11% of the bit rate, $f_b = 1/T_b$, which is typical of the high speed serial interface systems [8]. \square

Proof of Theorem 2. Subtracting $v_{e,n}$ from $v_{e,m}$ leads to

$$\begin{aligned} v_{e,m} - v_{e,n} &= \frac{2Ar}{1-r^N} \left\{ \sum_{i=1}^K (-1)^{i+1} r^{a_{i,m}} - \sum_{i=1}^K (-1)^{i+1} r^{a_{i,n}} \right\} \\ &> \frac{2Ar}{1-r^N} (-r^{a_{2k,m}} + r^{a_{2k,n}} - r^{a_{2k+1,n}}) \end{aligned} \quad (\text{A.3})$$

because $r^{a_{i,n}} - r^{a_{i+1,n}} > 0$. By using the fact that $-r^{a_{2k,m}} + r^{a_{2k,n}} - r^{a_{2k+1,n}}$ is minimum at $a_{2k,m} = a_{2k,n} + 1$ and $a_{2k+1,n} = a_{2k,n} + 1$,

$$\begin{aligned} v_{e,m} - v_{e,n} &> \frac{2Ar}{1-r^N} (-r^{a_{2k,n}+1} + r^{a_{2k,n}} - r^{a_{2k,n}+1}) \\ &= \frac{2Ar}{1-r^N} r^{a_{2k,n}} (1-2r) > 0 \end{aligned} \quad (\text{A.4})$$

because r is smaller than 0.5. \square

Proof of Theorem 3. Subtracting $v_{e,m}$ from $v_{e,n}$ leads to

$$v_{e,n} - v_{e,m} = \frac{2Ar}{1-r^N} \left\{ \sum_{i=1}^K (-1)^{i+1} r^{a_{i,n}} - \sum_{i=1}^K (-1)^{i+1} r^{a_{i,m}} \right\} > \frac{2Ar}{1-r^N} (r^{a_{2k+1,n}} - r^{a_{2k+2,n}} - r^{a_{2k+1,m}}), \tag{A.5}$$

because $r^{a_{i,n}} - r^{a_{i+1,n}} > 0$. By using the fact that $r^{a_{2k+1,n}} - r^{a_{2k+2,n}} - r^{a_{2k+1,m}}$ is minimum at $a_{2k+2,n} = a_{2k+1,n} + 1$ and $a_{2k+1,m} = a_{2k+1,n} + 1$,

$$v_{e,n} - v_{e,m} > \frac{2Ar}{1-r^N} (r^{a_{2k+1,n}} - r^{a_{2k+1,n}+1} - r^{a_{2k+1,n}+1}) = \frac{2Ar}{1-r^N} r^{a_{2k+1,n}} (1-2r) > 0 \tag{A.6}$$

because r is smaller than 0.5. □

B. Closed-Form DDJ Equations of PRBS4 and PRBS5

Following the same steps explained in Section 2.2, the DDJ can be derived for other PRBS data. For PRBS4

$$DDJ = T_b \log_r \left(\frac{1-r+r^4-r^8+r^9-r^{10}+r^{11}-r^{13}}{1-r^4+r^5-r^6+r^7-r^9+r^{11}-r^{12}} \right) \tag{B.1}$$

and for PRBS5

$$DDJ = T_b \log_r \left(\left((1-r+r^5-r^6+r^7-r^8+r^9-r^{12}+r^{13}-r^{15}+r^{18}-r^{23}+r^{25}-r^{27}+r^{28}-r^{29}) \times (1-r^5+r^7-r^9+r^{10}-r^{11}+r^{13}-r^{14}+r^{18}-r^{19}+r^{20}-r^{21}+r^{22}-r^{25}+r^{26}-r^{28})^{-1} \right) \right). \tag{B.2}$$

C. Comments on the DDJ Equation of (10) in [10]

In [10], the closed-form DDJ equation of (10) has been calculated for the first order low pass system by considering only two preceding bits, a_{-1} and a_{-2} , as follows:

$$DDJ = \frac{\tau}{2} \ln \left(\frac{1+\alpha}{1-\alpha+\alpha^2} \right), \tag{C.1}$$

where $\tau = 1/2\pi f_{BW}$ and $\alpha = e^{-2\pi f_{BW} T_b}$. However, as the bit rate increases relatively to the system bandwidth, α increases and the impact of additional bits such as a_{-3} and a_{-4} should be considered as shown in Figure 3 of [10]. Consequently, the calculated DDJ by (10) in [10], which is rewritten in (C.1), underestimates the simulated DDJ as shown in Figure 11(a).

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

This work was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (NRF-2012R1A1A1008324). The CAD tools were supported by IDEC.

References

- [1] W.-Y. Lee and L.-S. Kim, "A 5.4-Gb/s clock and data recovery circuit using seamless loop transition scheme with minimal phase noise degradation," *IEEE Transactions on Circuits and Systems I*, vol. 59, no. 11, pp. 2518–2528, 2012.
- [2] S. Byun, C. H. Son, J. Hwang, B.-H. Min, M.-Y. Park, and H.-K. Yu, "1–5.6 Gb/s CMOS clock and data recovery IC with a static phase offset compensated linear phase detector," *IET Circuits, Devices & Systems*, vol. 7, no. 3, pp. 159–168, 2013.
- [3] H. Liu, Y. Wang, C. Xu et al., "A 5-Gb/s serial-link redriver with adaptive equalizer and transmitter swing enhancement," *IEEE Transactions on Circuits and Systems I*, vol. 61, no. 4, pp. 1001–1011, 2014.
- [4] M.-S. Chen, Y.-N. Shih, C.-L. Lin, H.-W. Hung, and J. Lee, "A fully-integrated 40-Gb/s transceiver in 65-nm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 627–640, 2012.
- [5] "Fibre channel-methodologies for jitter and signal quality specification (MJSQ)," Technical Report Review, International Committee for Information Technology Standardization (INCITS), 2004.
- [6] Maxim Application Note 1916, "An introduction to jitter in communications systems," March 2003, <http://www.maximintegrated.com/app-notes/index.mvp/id/1916>.
- [7] W. Yu, R. Shi, and C.-K. Cheng, "Accurate eye diagram prediction based on step response and its application to low-power equalizer design," *IEICE Transactions on Electronics*, vol. E92-C, no. 4, pp. 444–452, 2009.
- [8] R. Shi, W. Yu, Y. Zhu, C.-K. Cheng, and E. S. Kuh, "Efficient and accurate eye diagram prediction for high speed signaling," in *Proceedings of the International Conference on Computer-Aided Design (ICCAD '08)*, pp. 655–661, San Jose, Calif, USA, November 2008.
- [9] D. Kim, H. Kim, and Y. Eo, "Analytical eye-diagram determination for the efficient and accurate signal integrity verification of single interconnect lines," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 10, pp. 1536–1545, 2012.
- [10] J. Buckwalter, B. Analui, and A. Hajimiri, "Predicting data-dependent jitter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 9, pp. 453–457, 2004.
- [11] B. Analui, J. F. Buckwalter, and A. Hajimiri, "Data-dependent jitter in serial communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3388–3397, 2005.
- [12] D. Hong and K. T. Cheng, "An accurate jitter estimation technique for efficient high speed I/O testing," in *Proceedings of*

the 16th Asian Test Symposium (ATS '07), pp. 224–229, October 2007.

- [13] J. F. Buckwalter and A. Hajimiri, “Analysis and equalization of data-dependent jitter,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 3, pp. 607–620, 2006.
- [14] T. Xia and D. Mu, “High speed interconnect data dependent jitter analysis,” *Microelectronics Journal*, vol. 41, no. 6, pp. 371–379, 2010.
- [15] A. Papoulis and S. U. Pillai, *Probability, Random Variables and Stochastic Processes*, McGraw-Hill, New York, NY, USA, 4th edition, 2002.
- [16] S. Miller and D. Childers, *Probability and Random Process*, Academic Press, New York, NY, USA, 2nd edition, 2012.

